TEXAS INSTRUMENTS
THVD1410
THVD1450, THVD1451, THVD1452
JAJSFG1E – MAY 2018 – REVISED MAY 2019

THVD14xx ±18kV IEC ESD 保護機能搭載、3.3V～5V、RS-485 トランシーバ

1 特長

- TIA/EIA-485A 標準の要件に合致、または上回る仕様
- 電源電圧: 3V～5.5V
- 5V電源で差動出力が2.1Vを超えるためPROFIBUSと互換
- バスI/O ESD保護
  - ±30kV HBM
  - ±18kV IEC 61000-4-2接触放電
  - ±25kV IEC 61000-4-2エアギャップ放電
  - ±4kV IEC 61000-4-4高速過渡バースト
- 拡張動作同相範囲 ±15V
- 低EMIで500kbpsおよび50Mbpsのデータレート
- レシーバの大きなヒステリシスによるノイズ除去
- 低消費電力
  - スタンバイ時消費電流: 1µA未満
  - 動作時電流: 3mA未満
- 拡張周囲温度範囲: -40℃～+125℃
- グリッチなしの電源オン/オフによるホット・プラグイン能力
- 開放、短絡、アイドル・バスのフェイルセーフ
- 1/8の単位負荷(最大256のバス・ノード)
- 小型のVSONおよびVSSOPパッケージによる基板面積の削減、またはSOICによりドロップイン互換を実現

2 アプリケーション

- モータ駆動
- ファクトリ・オートメーション/制御
- 電力網インフラストラクチャ
- ビルディング・オートメーション
- HVACシステム
- ビデオ監視
- プロセス分析
- ワイヤレス・インフラ

3 概要

THVD14xxは、過酷な産業環境で動作するように設計された、ノイズ耐性の高いRS-485/RS-422トランシーバ・ファミリです。これらのデバイスのバス・ピンは、高レベルのIEC電気的高速過渡(EFT)およびIEC静電放電(ESD)事象に対する耐性があるため、システム・レベルの保護部品を追加する必要がありません。

これらの各デバイスは3V～5.5Vの単一電源で動作します。このファミリのデバイスは拡張同相電圧範囲に対応し、長い距離のケーブルを通したマルチポイントのアプリケーションに適しています。

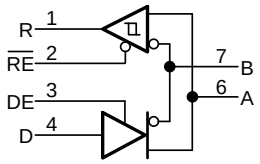
THVD14xxファミリのデバイスは小型のVSONおよびVSSOPパッケージで供給され、スペースに制約のあるアプリケーションで使用できます。このデバイスは、−40℃～125℃の周囲自由通気温度範囲で仕様が規定されています。

製品情報(1)

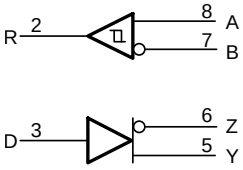
型番	パッケージ	本体サイズ(公称)
THVD1410	VSSOP (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
THVD1450	VSON (8)	3.00mm×3.00mm
	VSSOP (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
THVD1451	VSON (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
THVD1452	VSSOP (10)	3.00mm×3.00mm
	SOIC (14)	8.65mm×3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

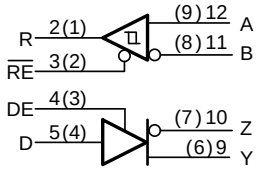
THVD1410およびTHVD1450の概略回路図



THVD1451の概略回路図



THVD1452の概略回路図



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4 改訂履歴

Revision D (March 2019) から **Revision E** に変更 **Page**

- THVD1451 を「*製品プレビュー*」から「*量産データ*」に変更 ... 1

Revision C (February 2019) から **Revision D** に変更 **Page**

- THVD1410 を「*製品プレビュー*」から「*量産データ*」に変更 ... 1

Revision B (December 2018) から **Revision C** に変更 **Page**

- THVD1452 を「*製品プレビュー*」から「*量産データ*」に変更 ... 1

Revision A (May 2018) から **Revision B** に変更 **Page**

- 「*特長*」に「5V電源で差動出力が2.1Vを超え...」を追加 ... 1
- 「*特長*」の「±18kV IEC 61000-4-2エアギャップ放電」を「±25kV IEC 61000-4-2エアギャップ放電」に変更 ... 1
- THVD1451にSOIC (8)パッケージを追加 ... 1
- Added Thermal Pad to the THVD1450 DRB package ... 5
- Added Thermal Pad to the THVD1451 DRB package ... 6
- Changed all pins HBM ESD rating from 4 kV to 8 kV ... 8
- Changed IEC ESD air-gap discharge rating from 18 kV to 25 kV ... 8
- Changed THVD1410 power dissipation numbers ... 9
- Changed THVD1410 driver t_r, t_f TYP from 400 ns to 460 ns and MAX from 600 ns to 680 ns ... 11
- Changed THVD1410 receiver t_r, t_f TYP from 13 ns to 10 ns ... 11
- Changed THVD1410 receiver $t_{PH}L$, t_{PLH} TYP from 60 ns to 35 ns ... 11
- Added Typical Characteristics, THD1450D ... 14

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- Added condition to 図 8 to 図 3 14
- Added Typical Characteristics, THD1410 15
- Changed A to A/Y and B to B/Z in 図 20 to 図 24 16
- Added 3rd paragraph to the *Overview* section 18

2017年11月発行のものから更新 **Page**

- ドキュメントのステータスを「*事前情報*」から「*量産混在*」データに変更 1

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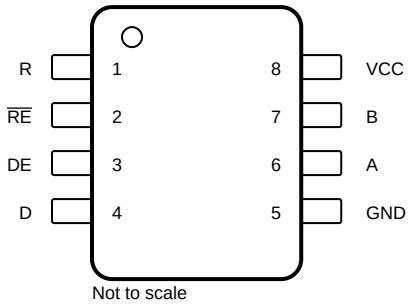
5 Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1410	Half	DE, $\overline{RE}$	up to 500 kbps	256
THVD1450	Half	DE, $\overline{RE}$	up to 50 Mbps	
THVD1451	Full	None		
THVD1452	Full	DE, $\overline{RE}$		

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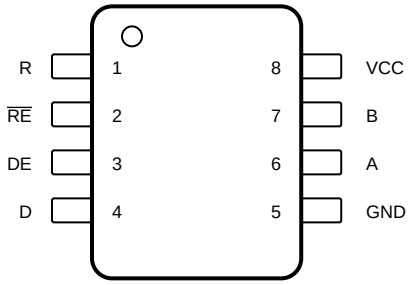
6 Pin Configuration and Functions

THVD1410, THVD1450 Devices
8-Pin D Package (SOIC)
Top View



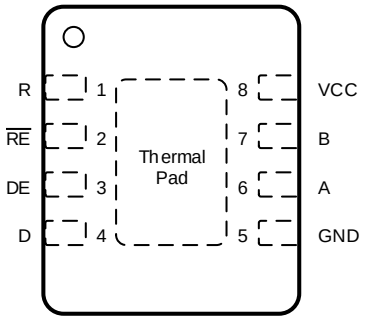
Not to scale

THVD1410, THVD1450 Devices
8-Pin DGK Package (VSSOP)
Top View



Not to scale

THVD1450 Device
8-Pin DRB Package (VSON)
Top View



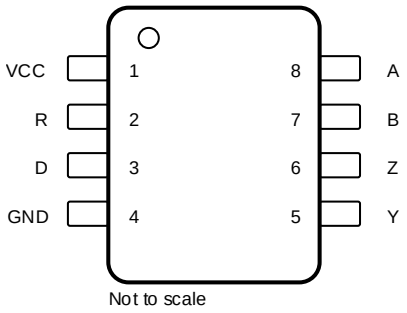
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Pin Functions

PIN				I/O	DESCRIPTION
NAME	D	DGK	DRB		
A	6	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	4	4	Digital input	Driver data input
DE	3	3	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	5	5	5	Ground	Device ground
R	1	1	1	Digital output	Receive data output
V_{CC}	8	8	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	2	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)
Thermal Pad	—	—		I/O	No electrical connection. Should be connected to GND for optimal thermal performance.

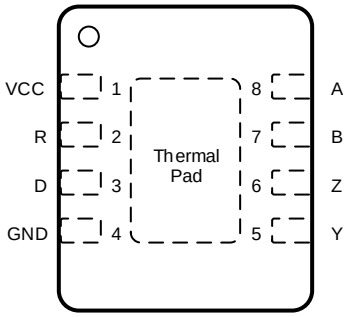
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THVD1451 Device
8-Pin D Package (SOIC)
Top View



Not to scale

THVD1451 Device
8-Pin DRB Package (VSON)
Top View



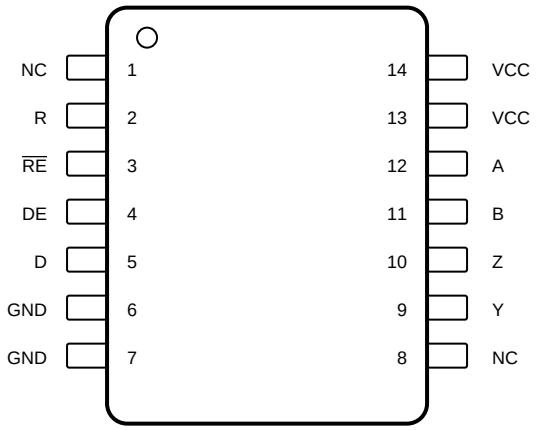
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Pin Functions

PIN			I/O	Description
NAME	D	DRB		
A	8	8	Bus input	Bus input, A (complementary to B)
B	7	7	Bus input	Bus input, B (complementary to A)
D	3	3	Digital input	Driver data input
GND	4	4	Ground	Device ground
R	2	2	Digital output	Receive data output
V_{CC}	1	1	Power	3.3-V to 5-V supply
Y	5	5	Bus output	Digital bus output, Y (Complementary to Z)
Z	6	6	Bus output	Digital bus output, Z (Complementary to Y)
Thermal Pad	—		I/O	No electrical connection. Should be connected to GND for optimal thermal performance.

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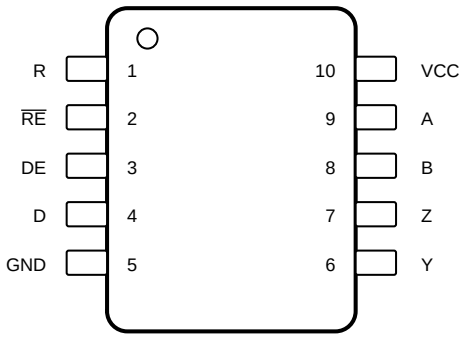
THVD1452 Device
14-Pin D Package (SOIC)
Top View



Not to scale

NC – No internal connection

THVD1452 Device
10-Pin DGS Package (VSSOP)
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D	DGS		
A	12	9	Bus input	Bus input, A (complementary to B)
B	11	8	Bus input	Bus input, B (complementary to A)
D	5	4	Digital input	Driver data input
DE	4	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	6, 7 (1)	5	Ground	Device ground
NC	1, 8	—	—	Internally not connected
R	2	1	Digital output	Receive data output
V_{CC}	13, 14 (1)	10	Power	3.3-V to 5-V supply
Y	9	6	Bus output	Digital bus output, Y (Complementary to Z)
Z	10	7	Bus output	Digital bus output, Z (Complementary to Y)
$\overline{RE}$	3	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)

(1) These pins are internally connected

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	-0.5	7	V
Bus voltage	Range at any bus pin (A, B, Y, or Z) as differential or common-mode with respect to GND	-18	18	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$)	-0.3	5.7	V
Receiver output current	I_O	-24	24	mA
Storage temperature range		-65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND	±30	kV
			All other pins	±8	kV
		Charged device model (CDM), per JEDEC JESD22-C101(2)	All pins	±1.5	kV
		Machine model (MM), per JEDEC JESD22-A115-A	All pins	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus pins and GND	±18	kV
		Air-gap discharge, per IEC 61000-4-2	Bus pins and GND	±25	kV
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus pins and GND	±4	kV

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7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		5.5	V
V_I	Input voltage at any bus terminal(1)	-15		15	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	-15		15	V
I_O	Output current, driver	-60		60	mA
I_{OR}	Output current, receiver	-8		8	mA
R_L	Differential load resistance	54			Ω
$1/t_{UI}$	Signaling rate: THVD1410			500	kbps
$1/t_{UI}$	Signaling rate: THVD1450, THVD1451, THVD1452			50	Mbps
T_A	Operating ambient temperature	-40		125	℃
T_J	Junction temperature	-40		150	℃

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.5 Thermal Information

THERMAL METRIC(1)		THVD1410 THVD1450 THVD1451	THVD1452	THVD1410 THVD1450	THVD1452	THVD1450 THVD1451	UNIT
		D (SOIC)	D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	DRB (VSON)	
		8 PINS	14 PINS	8 PINS	10 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.3	86.4	155.2	155.6	48.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.7	43.7	47.2	49.3	49.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.7	42.5	76.1	77.1	21.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.8	10.2	3.9	4.5	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57	42.2	74.8	75.7	21.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Power Dissipation

PARAMETER	Description	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125°C, 50% duty cycle square wave at 500kbps signaling rate, THVD1410	Unterminated: R_L = 300 Ω, C_L = 50 pF		360		mW
		RS-422 load: R_L = 100 Ω, C_L = 50 pF		370		mW
		RS-485 load: R_L = 54 Ω, C_L = 50 pF		410		mW
	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125°C, 50% duty cycle square wave at 50Mbps signaling rate, THVD145x devices	Unterminated: R_L = 300 Ω, C_L = 50 pF		360		mW
		RS-422 load: R_L = 100 Ω, C_L = 50 pF		320		mW
		RS-485 load: R_L = 54 Ω, C_L = 50 pF		330		mW

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7.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -15 V ≤ V_{test} ≤ 15 V (See 図 20)(1)		1.5	3.5		V
		R_L = 60 Ω, -15 V ≤ V_{test} ≤ 15 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, (See 図 20)		2.1			V
		R_L = 100 Ω (See 図 21)		2	4		V
		R_L = 54 Ω (See 図 21)		1.5	3.5		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω (See 図 21)		-200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -7 V ≤ V_O ≤ 12 V		-250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12V		50	125	µA
			V_I = -7V	-100	-65		µA
		DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 15V		60	125	µA
			V_I = -15V	-200	-130		µA
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of ± 15 V		See(2)	-100	-20	mV
V_{TH-}	Negative-going input threshold voltage			-200	-130	See(2)	mV
V_{HYS}	Input hysteresis				30		mV
V_{OH}	Output high voltage	I_{OH} = -8 mA		V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}		-1		1	µA
Logic							
I_{IN}	Input current (D, DE, $\overline{RE}$)	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}		-6.2		6.2	µA
Device							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE}$ = 0 V , DE = V_{CC}, No load		2.4	3	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2	2.5	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		700	960	µA
		Driver and receiver disabled	$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1	µA
T_{SD}	Thermal shutdown temperature				170		℃

(1) $|V_{OD}|$ ≥ 1.4 V when T_A > 85 ℃, V_{test} < -7 V and V_{CC} < 3.135 V.
(2) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than $V_{TH–}$.

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7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: THVD1410						
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See 図 22	250	460	680	ns
t_{PHL}, t_{PLH}	Propagation delay			250	500	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				10	ns
t_{PHZ}, t_{PLZ}	Disable time			80	200	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V, See 図 23 and 図 24		100	600	ns
		$\overline{RE}$ = V_{CC}, See 図 23 and 図 24		4	11	µs
Receiver: THVD1410						
t_r, t_f	Output rise/fall time	C_L = 15 pF, See 図 25		10	20	ns
t_{PHL}, t_{PLH}	Propagation delay			35	110	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time			30	60	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$,	Enable time	DE = V_{CC}, See 図 26		60	140	ns
		DE = 0 V, See 図 27		6	14	µs
Driver: THVD1450, THVD1451, THVD1452						
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See 図 22	1	3	6	ns
t_{PHL}, t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				3.5	ns
t_{PHZ}, t_{PLZ}	Disable time			15	25	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V, See 図 23 and 図 24		20	50	ns
		$\overline{RE}$ = V_{CC}, See 図 23 and 図 24		2.5	10	µs
Receiver: THVD1450, THVD1451, THVD1452						
t_r, t_f	Output rise/fall time	C_L = 15 pF, See 図 25		2	6	ns
t_{PHL}, t_{PLH}	Propagation delay			25	40	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				3.5	ns
t_{PHZ}, t_{PLZ}	Disable time			14	28	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$,	Enable time	DE = V_{CC}, See 図 26		50	110	ns
		DE = 0V, See 図 27		4	14	µs

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7.9 Typical Characteristics: All Devices

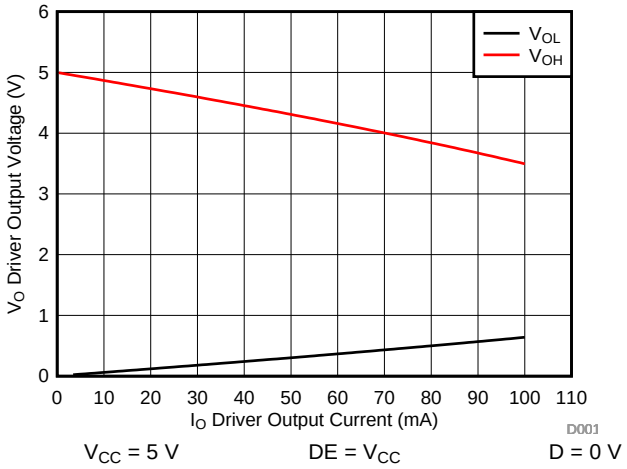


図 1. Driver Output Voltage vs Driver Output Current

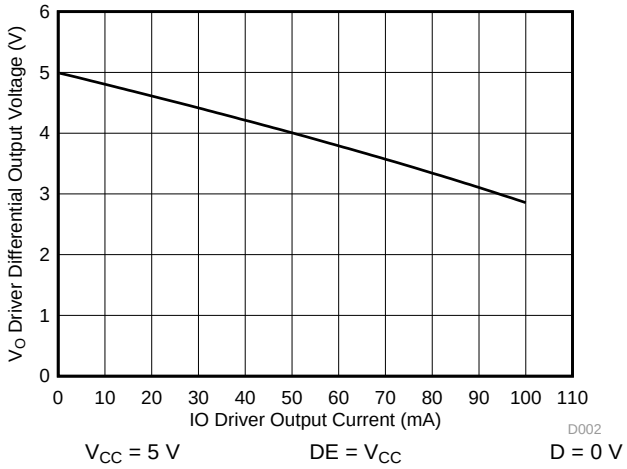


図 2. Driver Differential Output voltage vs Driver Output Current

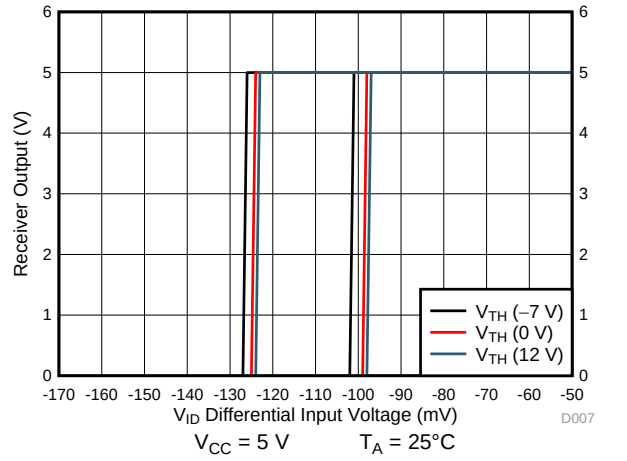


図 3. Receiver Output vs Input

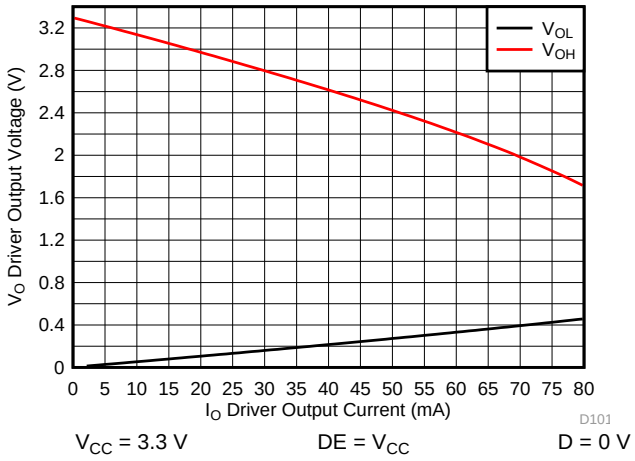


図 4. Driver Output Voltage vs Driver Output Current

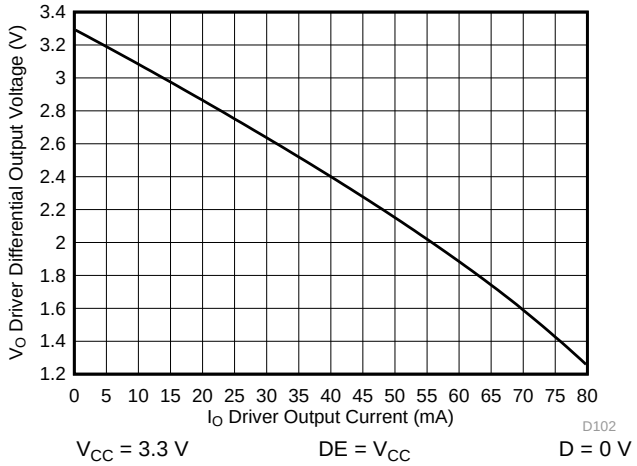


図 5. Driver Differential Output Voltage vs Driver Output Current

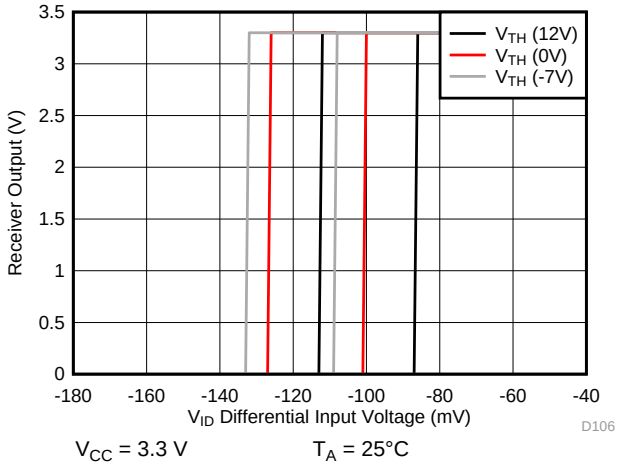
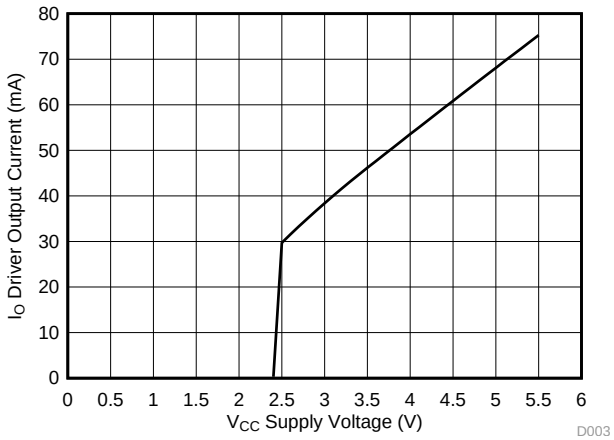


図 6. Receiver Output vs Input

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Typical Characteristics: All Devices (continued)

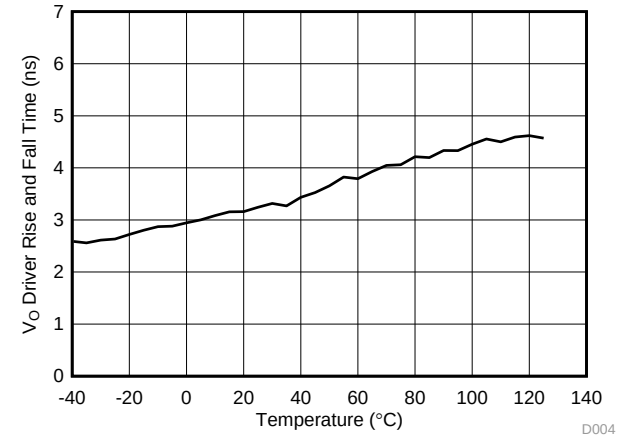


T_A = 25°C
R_L = 54 Ω
DE = V_{CC}
D = V_{CC}

図 7. Driver Output Current vs Supply Voltage

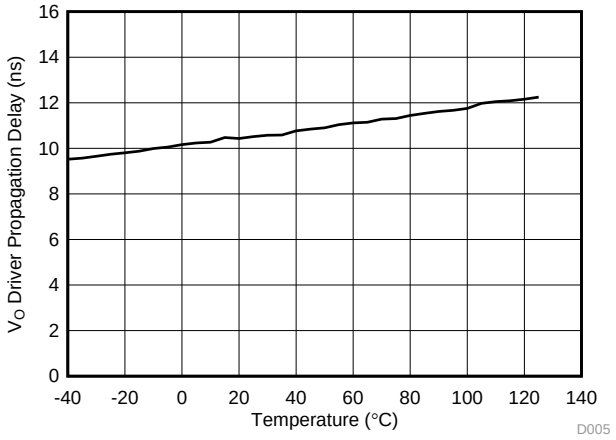
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7.10 Typical Characteristics: THD1450, THVD1451 and THVD1452



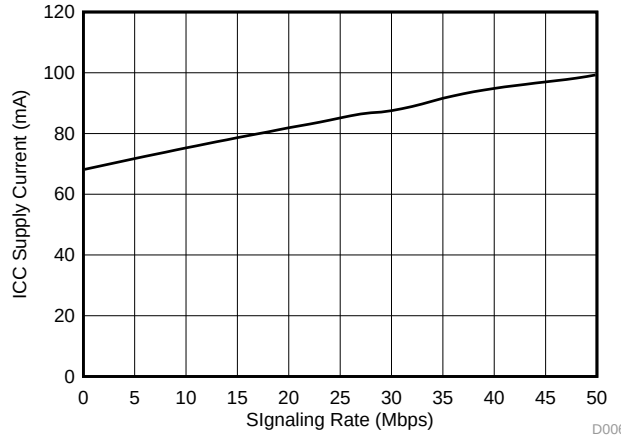
V_{CC} = 5 V

図 8. Driver Rise or Fall Time vs Temperature



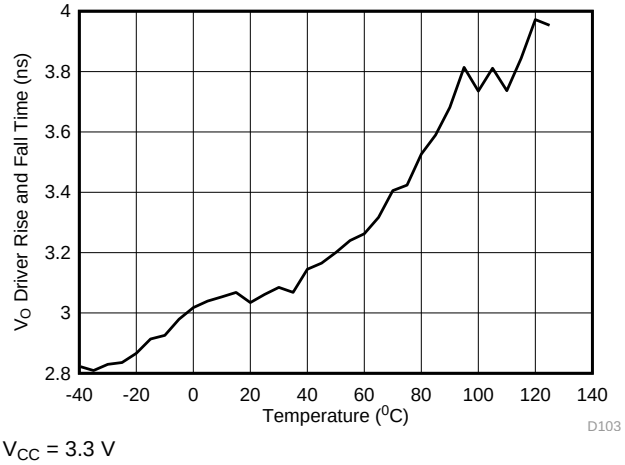
V_{CC} = 5 V

図 9. Driver Propagation Delay vs Temperature



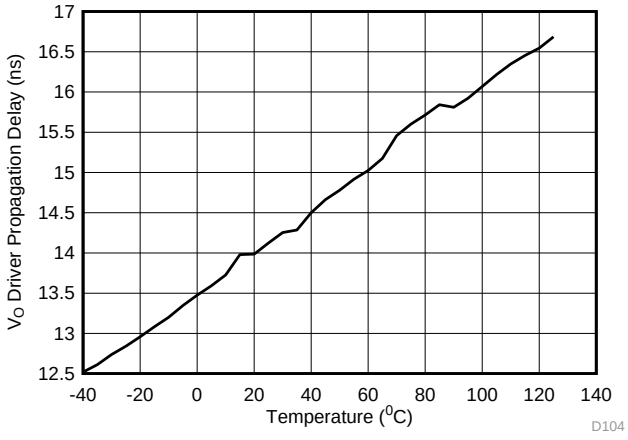
R_L = 54 Ω V_{CC} = 5 V T_A = 25°C

図 10. Supply Current vs Signal Rate



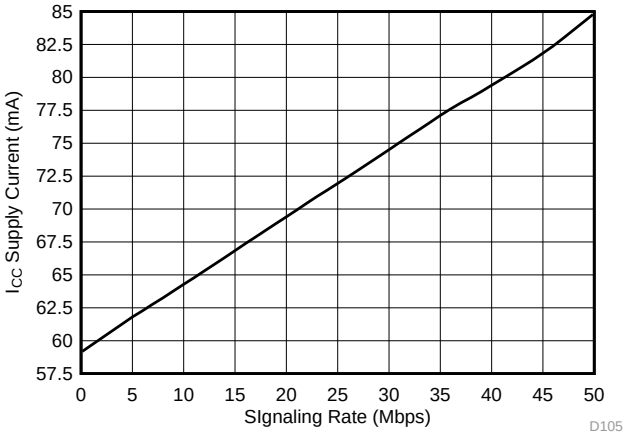
V_{CC} = 3.3 V

図 11. Driver Rise or Fall Time vs Temperature



V_{CC} = 3.3 V

図 12. Driver Propagation Delay vs Temperature



R_L = 54 Ω V_{CC} = 3.3 V T_A = 25°C

図 13. Supply Current vs Signal Rate

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7.11 Typical Characteristics: THVD1410

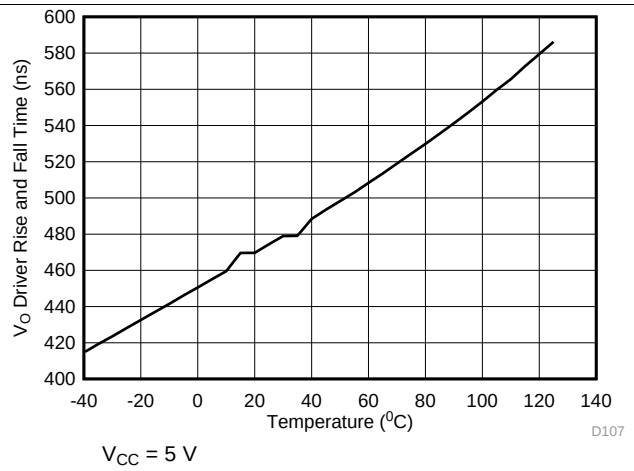


図 14. Driver Rise or Fall Time vs Temperature

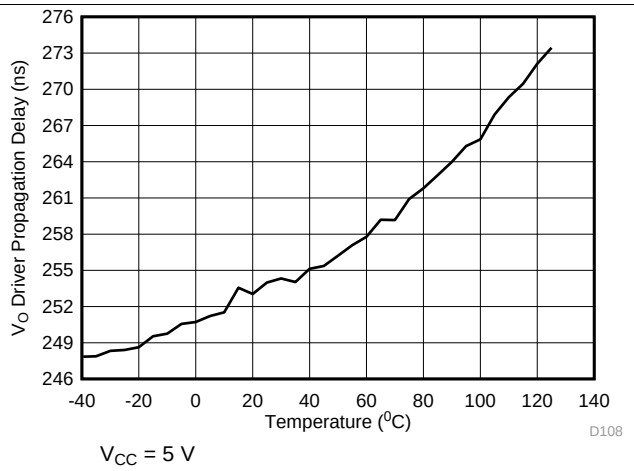


図 15. Driver Propagation Delay vs Temperature

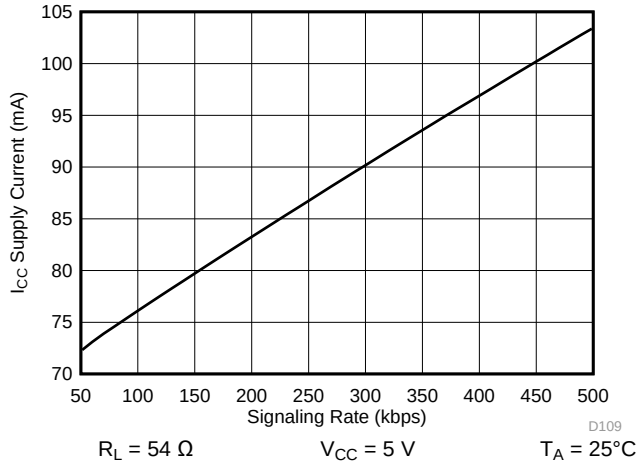


図 16. Supply Current vs Signal Rate

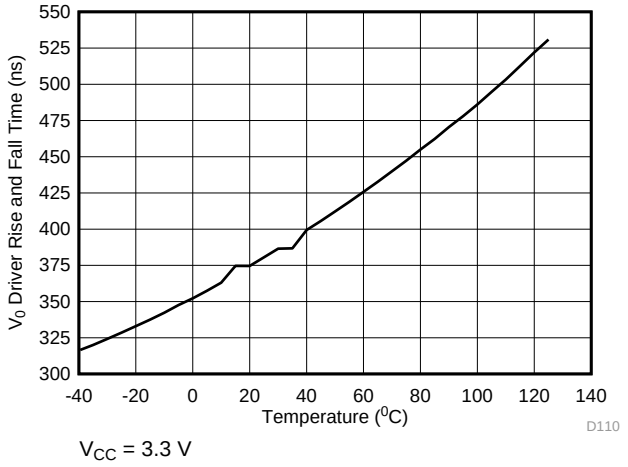


図 17. Driver Rise or Fall Time vs Temperature

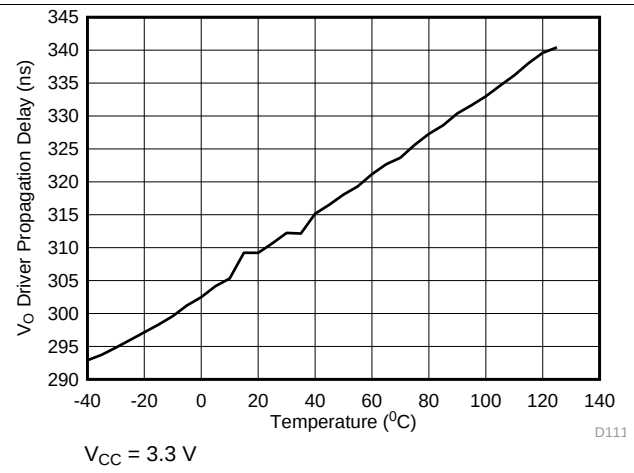


図 18. Driver Propagation Delay vs Temperature

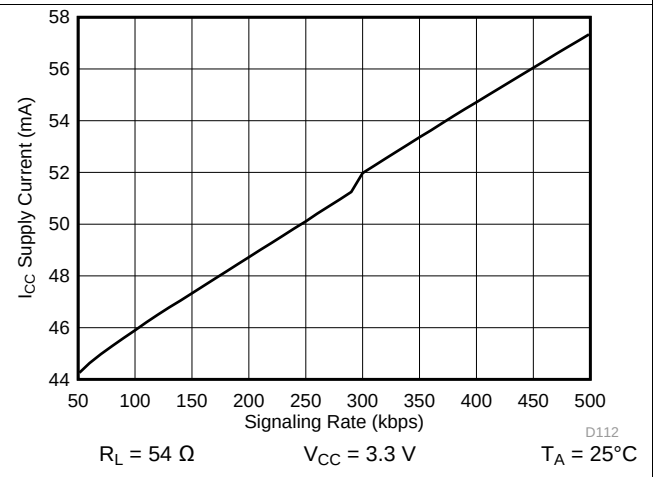


図 19. Supply Current vs Signal Rate

8 Parameter Measurement Information

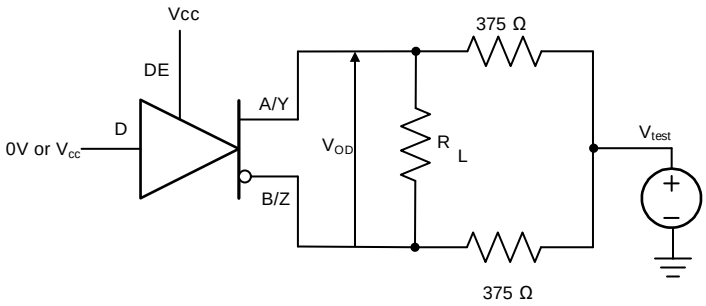


図 20. Measurement of Driver Differential Output Voltage With Common-Mode Load

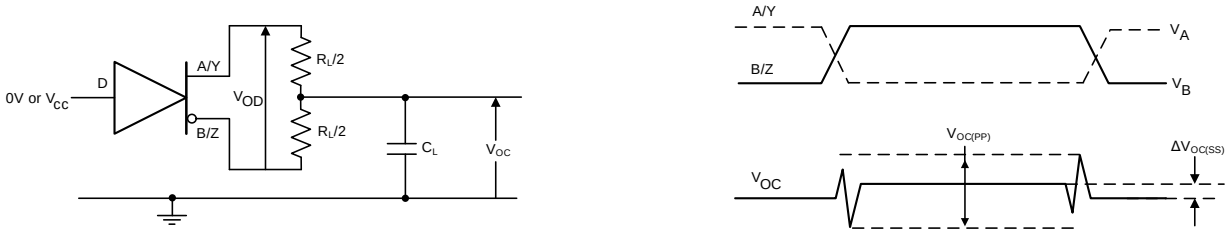


図 21. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

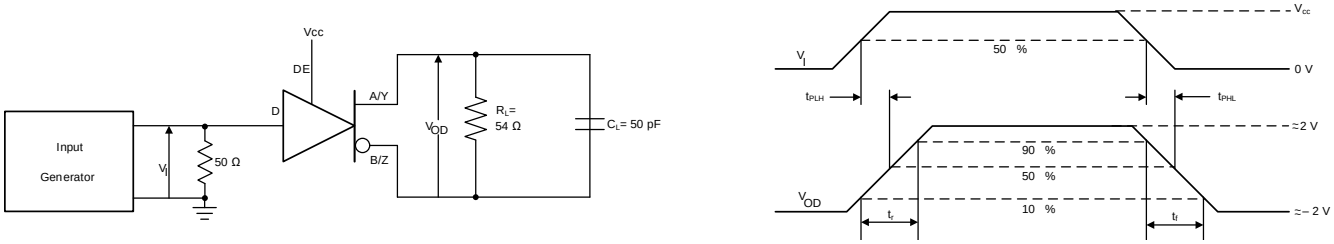


図 22. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

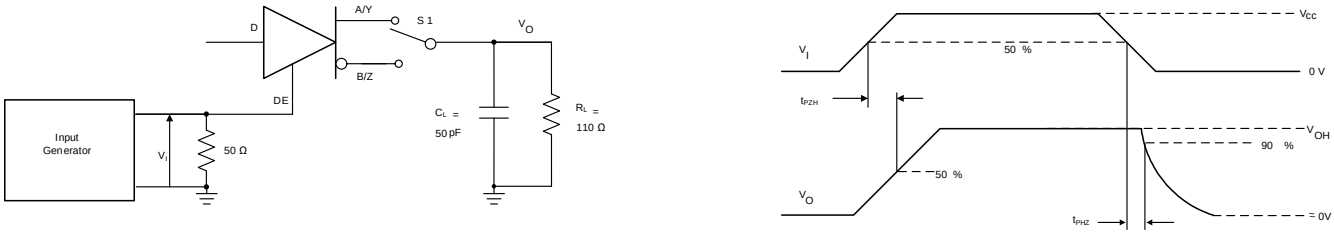


図 23. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

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Parameter Measurement Information (continued)

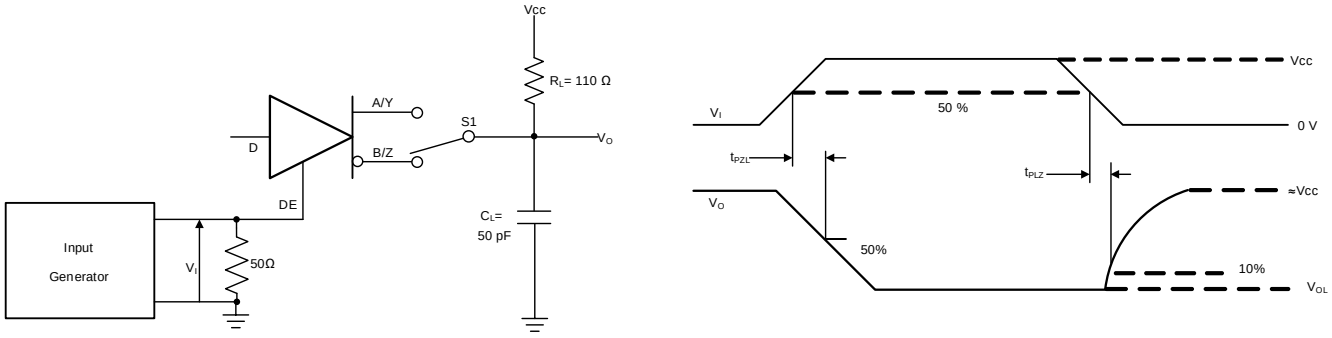


図 24. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

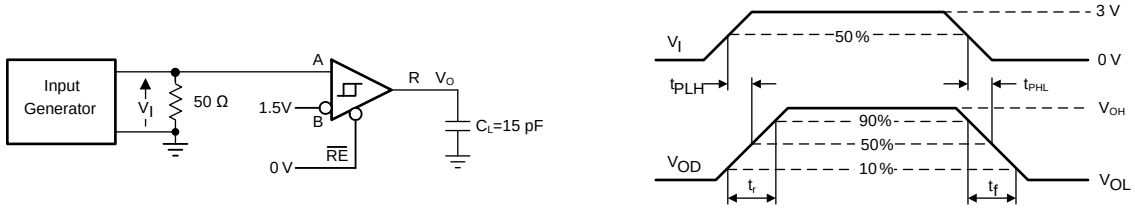


図 25. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

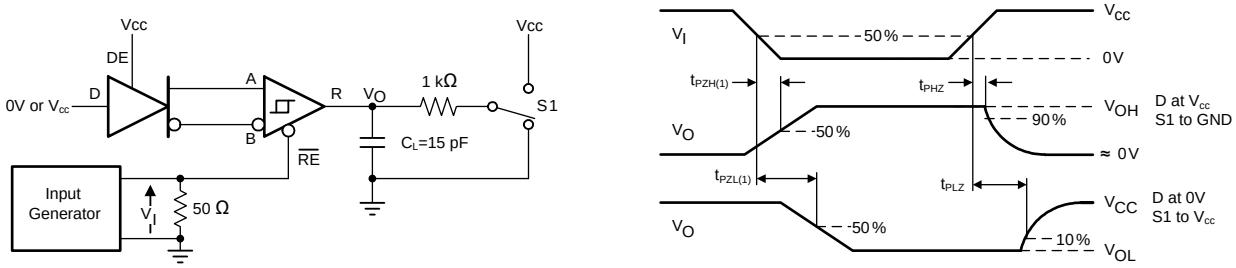


図 26. Measurement of Receiver Enable/Disable Times With Driver Enabled

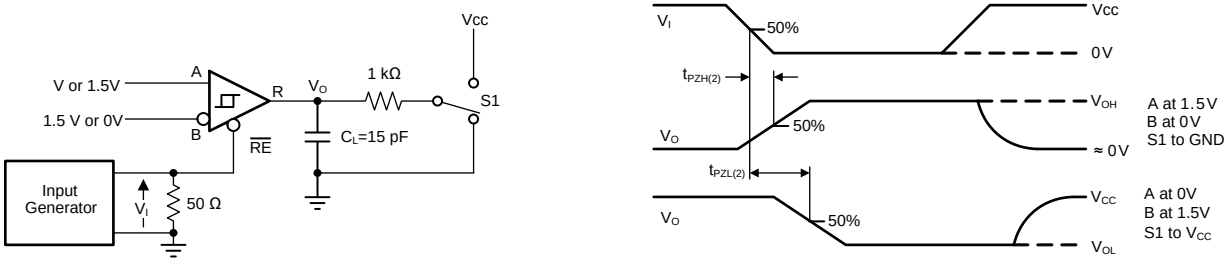


図 27. Measurement of Receiver Enable Times With Driver Disabled

9 Detailed Description

9.1 Overview

THVD1410 and THVD1450 are low-power, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 500 kbps and 50 Mbps respectively.

THVD1451 is fully enabled with no external enabling pins. THVD1452 has active-high driver enable and active-low receiver enable. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

THVD14xx family of devices have a higher typical differential output voltage (V_{OD}) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1 V is specified with V_{CC} voltage of 5 V ±10% to meet the requirements of PROFIBUS applications.

9.2 Functional Block Diagrams

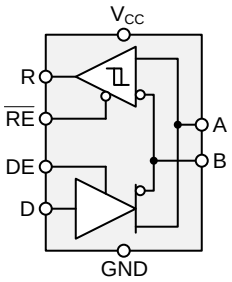


図 28. THVD1410 and THVD1450

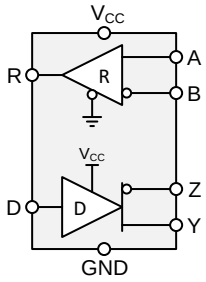


図 29. THVD1451

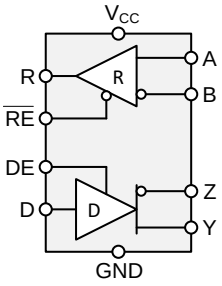


図 30. THVD1452

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9.3 Feature Description

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±18 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. With careful system design, one could achieve ±4 kV EFT Criterion A (no data loss when transient noise is present).

The THVD14xx device family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. The receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

9.4 Device Functional Modes

9.4.1 Device Functional Modes for THVD1410 and THVD1450

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 1. Driver Function Table for THVD1410 and THVD1450

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table for THVD1410 and THVD1450

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

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9.4.2 Device Functional Modes for THVD1451

For this device, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and VOD is negative. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 3. Driver Function Table for THVD1451

INPUT	OUTPUTS		FUNCTIONS
D	Y	Z	
H	H	L	Actively drive bus high
L	L	H	Actively drive bus low
OPEN	H	L	Actively drive bus High by default

When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is less than the negative input threshold, $V_{TH–}$, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and $V_{TH–}$ the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 4. Receiver Function Table for THVD1451

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	R	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

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9.4.3 Device Functional Modes for THVD1452

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 5. Driver Function Table for THVD1452

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 6. Receiver Function Table for THVD1452

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

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10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The THVD14xx family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

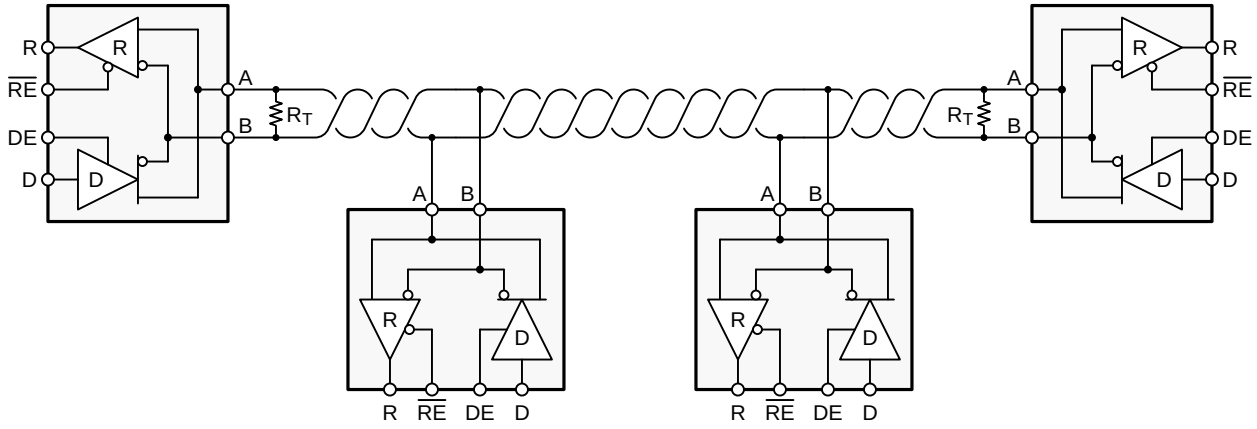


図 31. Typical RS-485 Network With Half-Duplex Transceivers

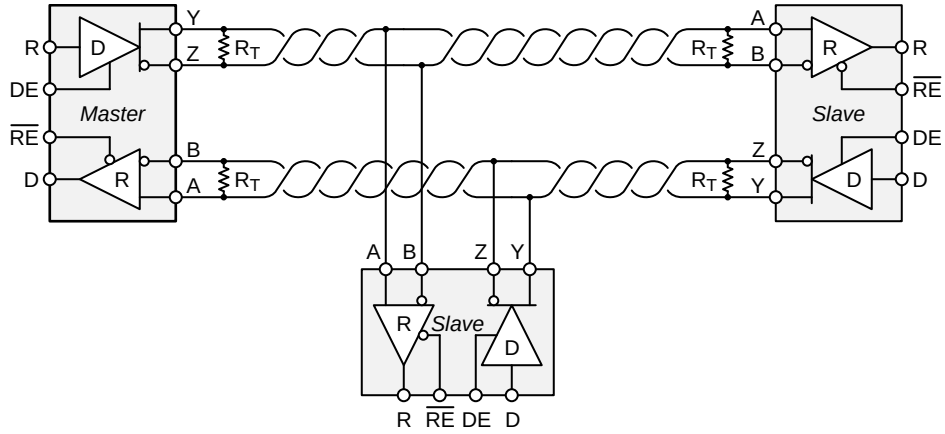


図 32. Typical RS-485 Network With Full-Duplex Transceivers

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Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

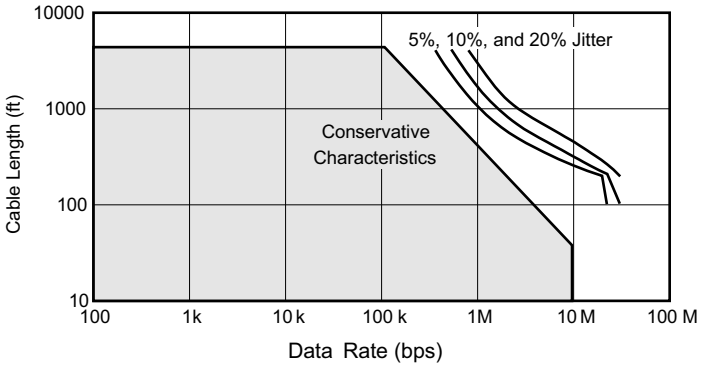


図 33. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD1450, THVD1451 and THVD1452) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD14xx family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

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Typical Application (continued)

10.2.1.4 Receiver Failsafe

The differential receivers of the THVD14xx family are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS} (the separation between V_{TH+} and $V_{TH–}$). As shown in the table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output will be High. Only when the differential input is more than V_{HYS} below V_{TH+} will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

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Typical Application (continued)

10.2.1.5 Transient Protection

The bus pins of the THVD14xx transceiver family include on-chip ESD protection against ±30-kV HBM and ±18-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

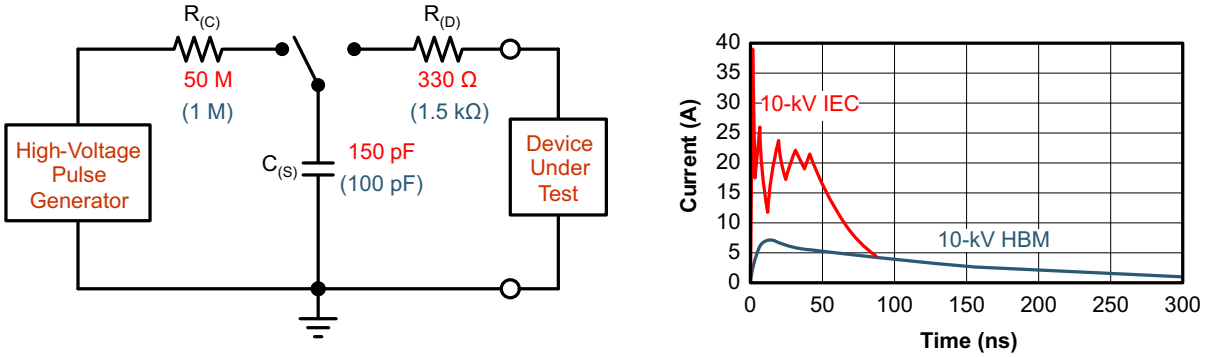


図 34. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

図 35 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

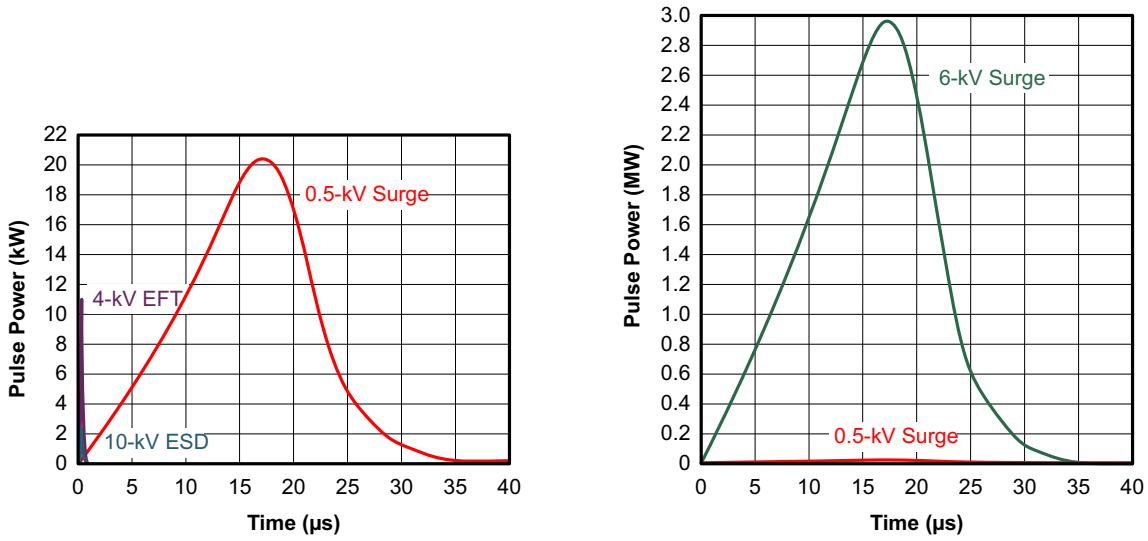


図 35. Power Comparison of ESD, EFT, and Surge Transients

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Typical Application (continued)

If the surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 図 36 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

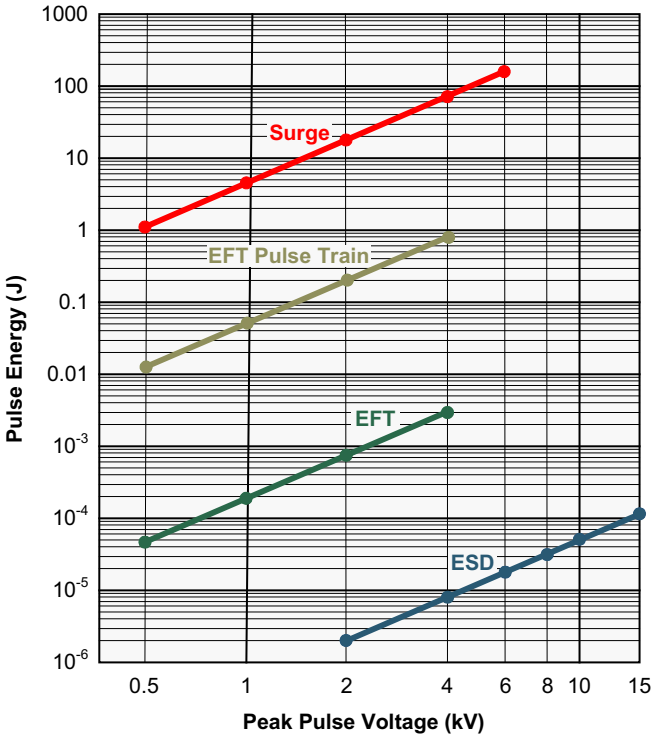


図 36. Comparison of Transient Energies

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Typical Application (continued)

10.2.2 Detailed Design Procedure

図 37 and 図 38 suggest a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 7 shows the associated bill of materials.

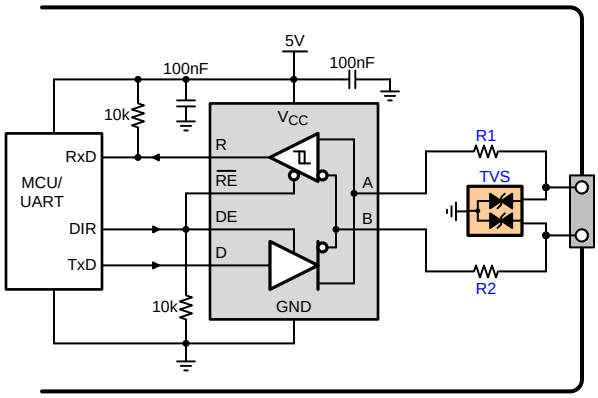


図 37. Transient Protection Against Surge Transients for Half-Duplex Devices

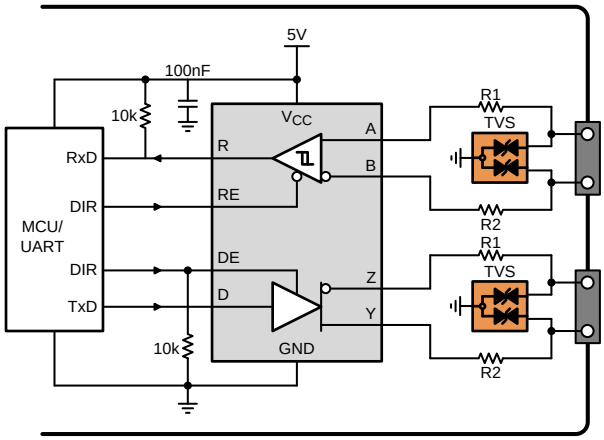


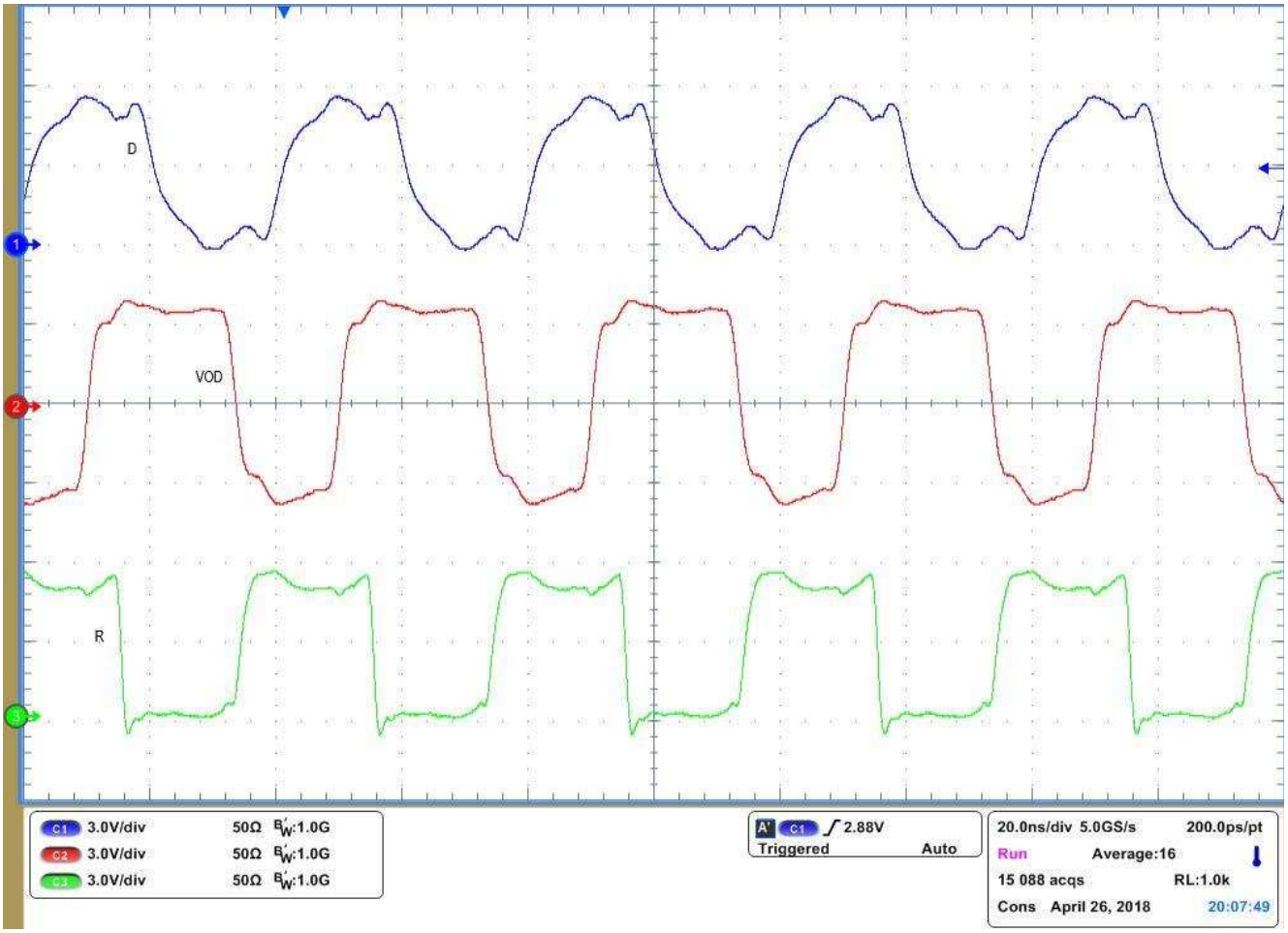
図 38. Transient Protection Against Surge Transients for Full-Duplex Devices

表 7. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD14xx	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

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10.2.3 Application Curves



50 Mbps V_{CC} = 5 V

図 39. THVD1450 Waveforms with 54-Ω Termination

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

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12 Layout

12.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

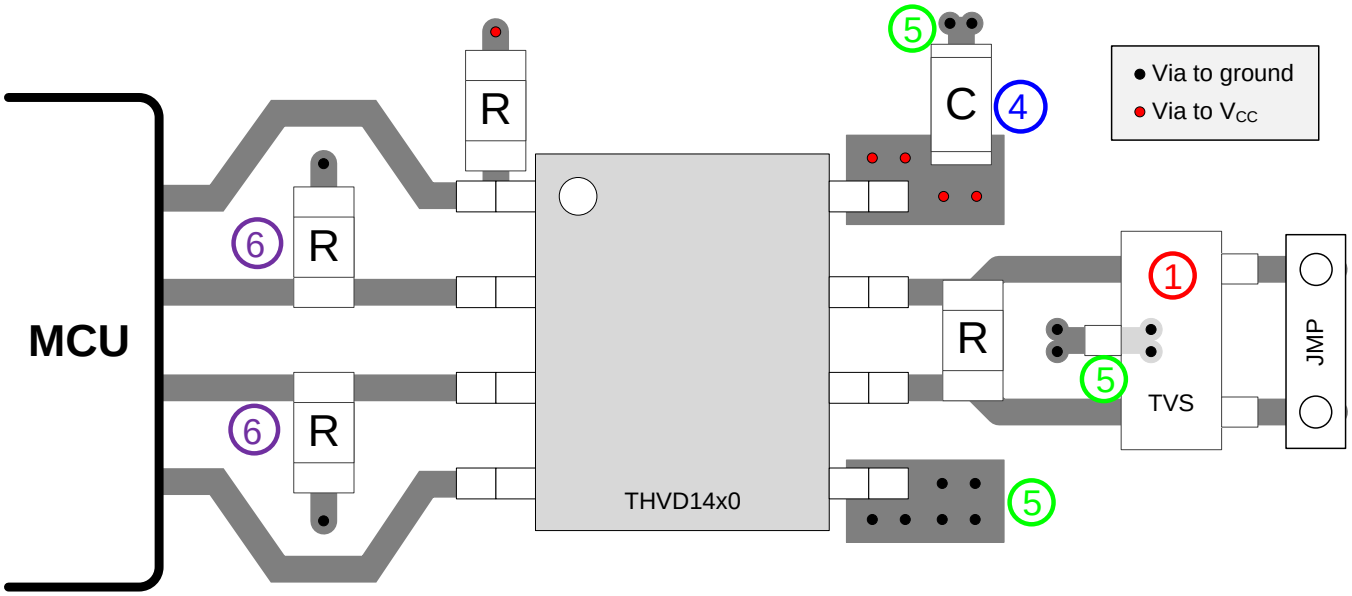


図 40. Half-Duplex Layout Example

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.2 デベロッパー・ネットワークの製品に関する免責事項

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表 8. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
THVD1410	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1450	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1451	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
THVD1452	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1410D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1410
THVD1410D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1410
THVD1410DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1410
THVD1410DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1410
THVD1410DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1410
THVD1450D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1450
THVD1450DRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1450

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1450DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1450DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450
THVD1451D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451
THVD1451D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451
THVD1451DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451
THVD1451DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451
THVD1451DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451
THVD1451DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1451
THVD1451DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1451
THVD1451DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1451
THVD1451DRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1451
THVD1452D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452
THVD1452DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

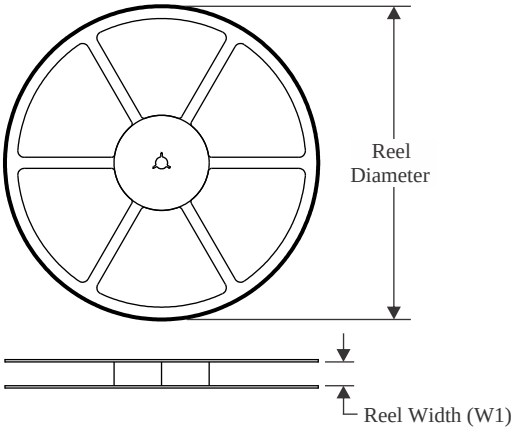
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

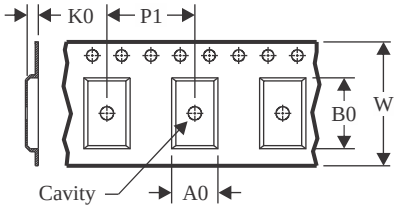
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

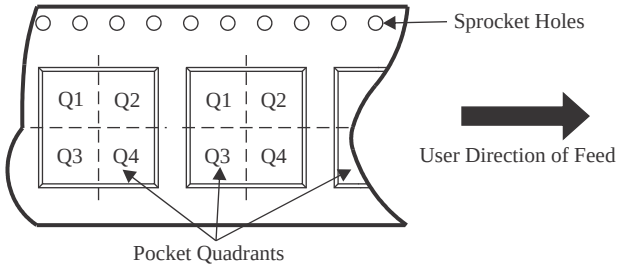


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

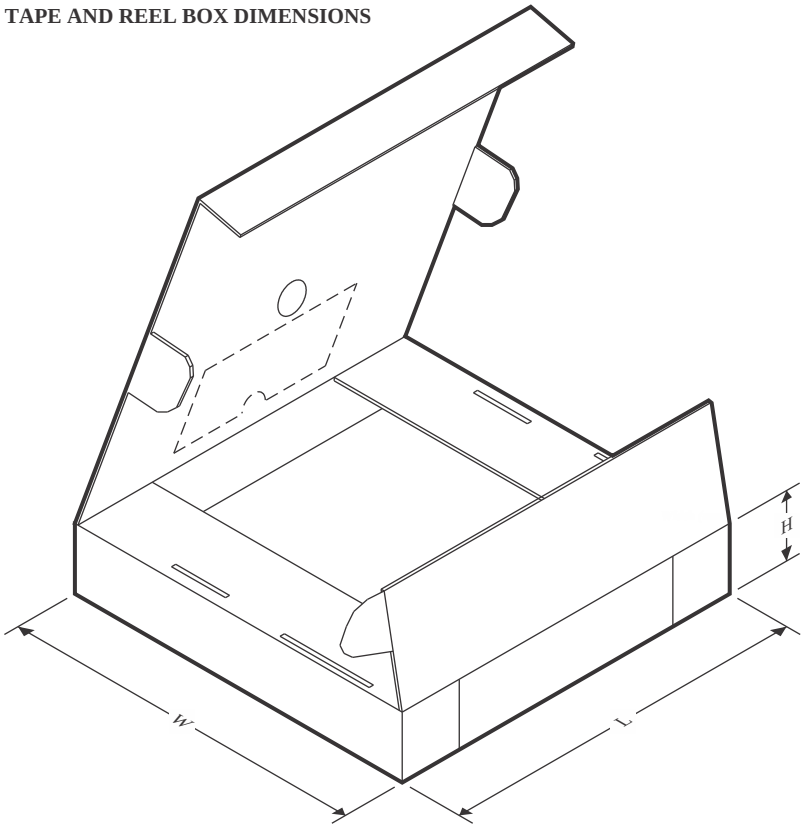
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1410DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1410DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1450DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1450DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1450DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1450DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1450DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1450DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1451DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1451DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1451DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1452DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1452DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

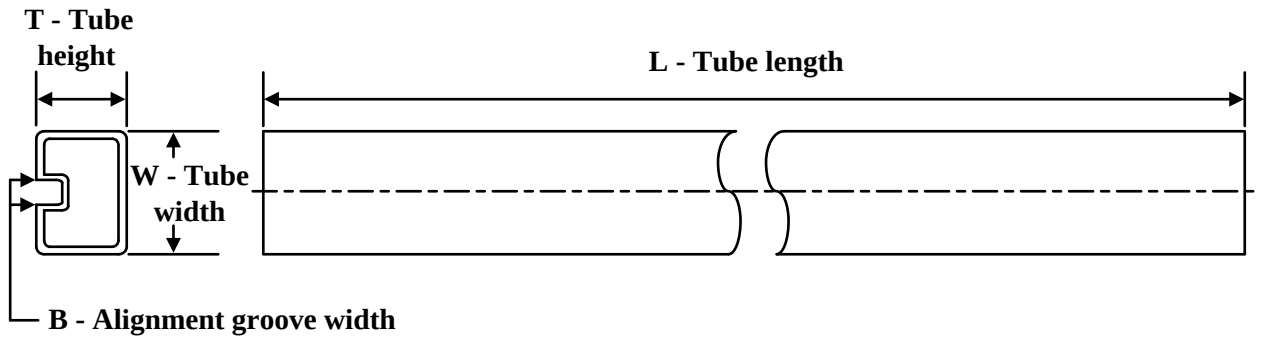
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1410DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THVD1410DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1410DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1410DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1450DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
THVD1450DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1450DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1450DRBR	SON	DRB	8	3000	346.0	346.0	35.0
THVD1450DRBT	SON	DRB	8	250	200.0	183.0	25.0
THVD1450DRG4	SOIC	D	8	2500	353.0	353.0	32.0
THVD1451DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1451DRBR	SON	DRB	8	3000	346.0	346.0	35.0
THVD1451DRBT	SON	DRB	8	250	200.0	183.0	25.0
THVD1452DGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
THVD1452DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

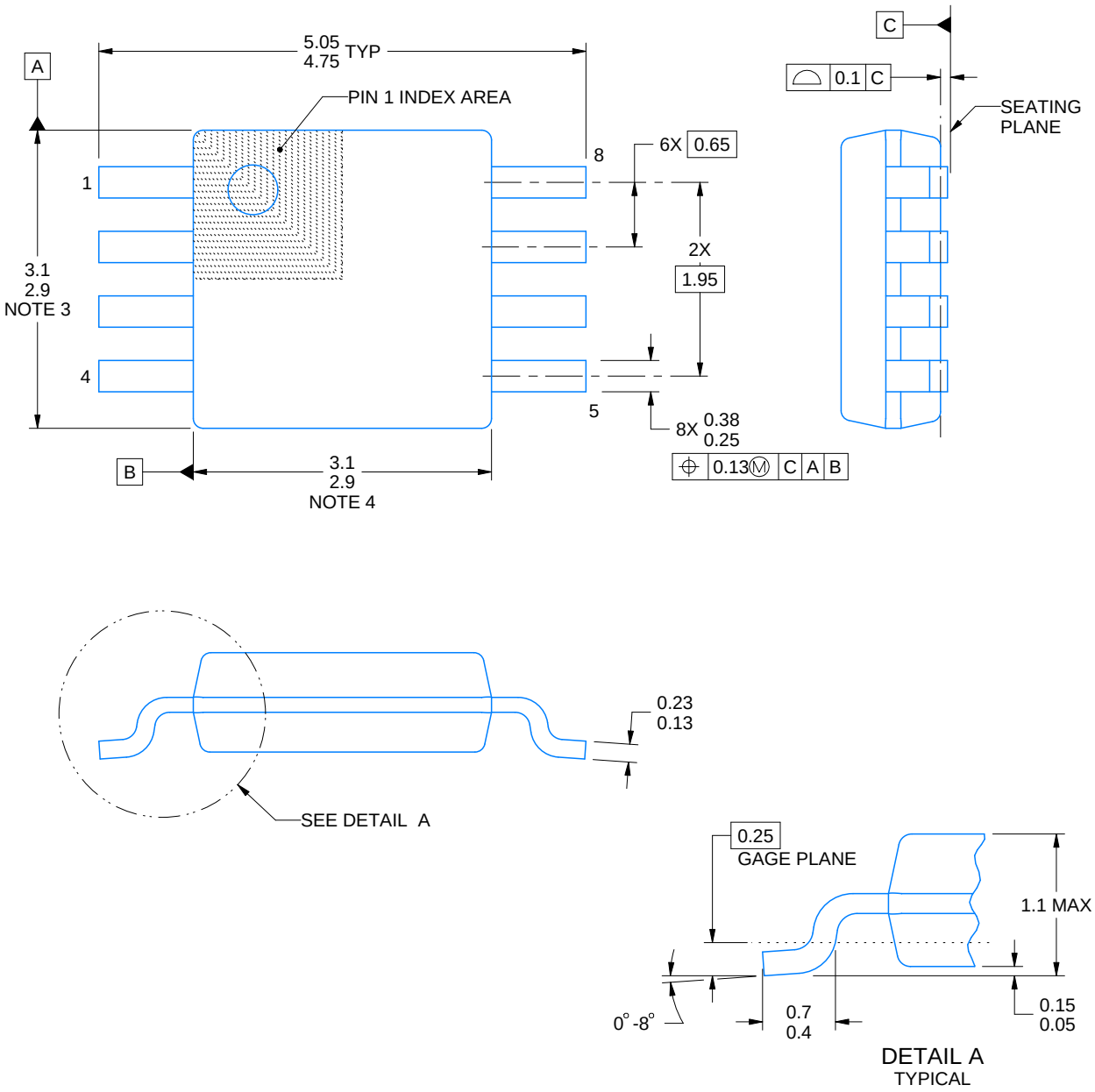
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THVD1410D	D	SOIC	8	75	507	8	3940	4.32
THVD1410D.A	D	SOIC	8	75	507	8	3940	4.32
THVD1410DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1410DGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1450D	D	SOIC	8	75	507	8	3940	4.32
THVD1450D.A	D	SOIC	8	75	507	8	3940	4.32
THVD1450D.B	D	SOIC	8	75	507	8	3940	4.32
THVD1450DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1450DGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1451D	D	SOIC	8	75	507	8	3940	4.32
THVD1451D.A	D	SOIC	8	75	507	8	3940	4.32
THVD1452D	D	SOIC	14	50	507	8	3940	4.32
THVD1452D.A	D	SOIC	14	50	507	8	3940	4.32
THVD1452DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
THVD1452DGS.A	DGS	VSSOP	10	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

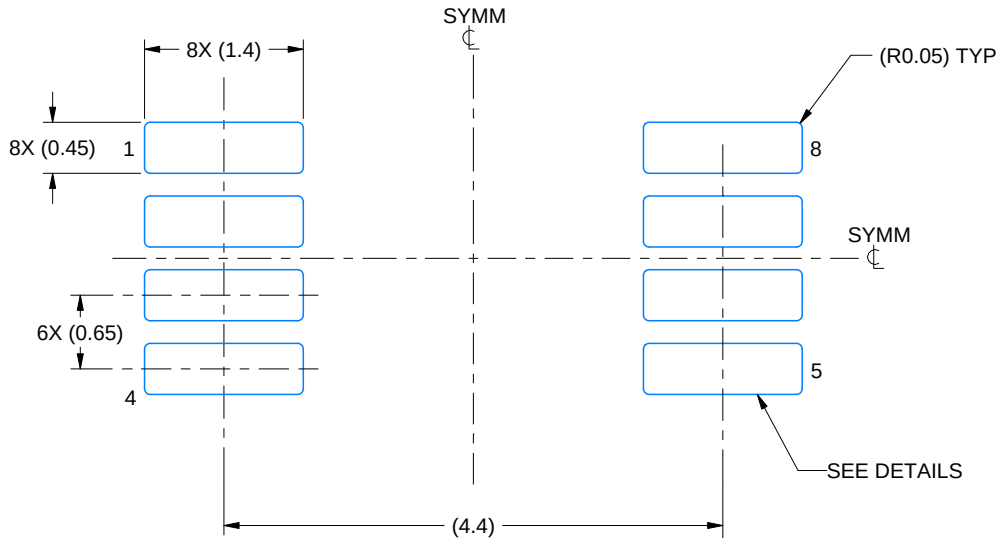
SMALL OUTLINE PACKAGE



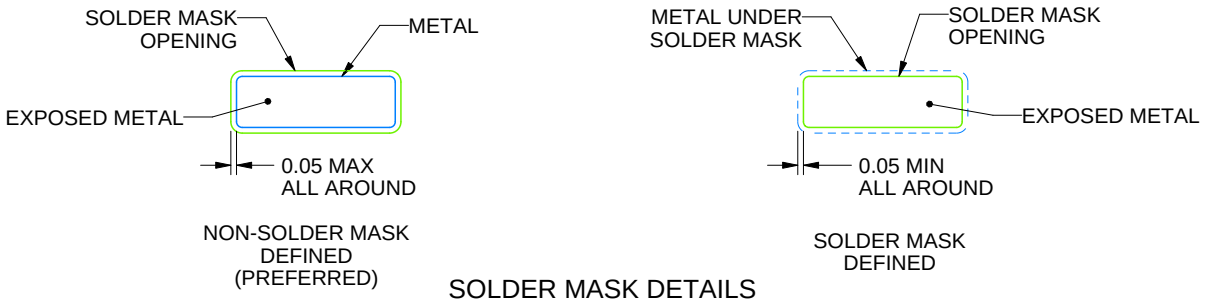
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

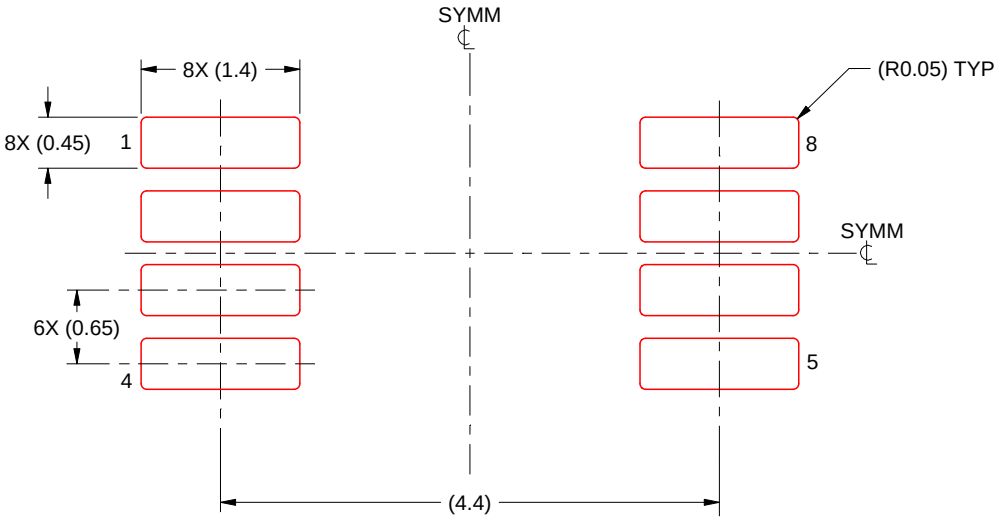


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

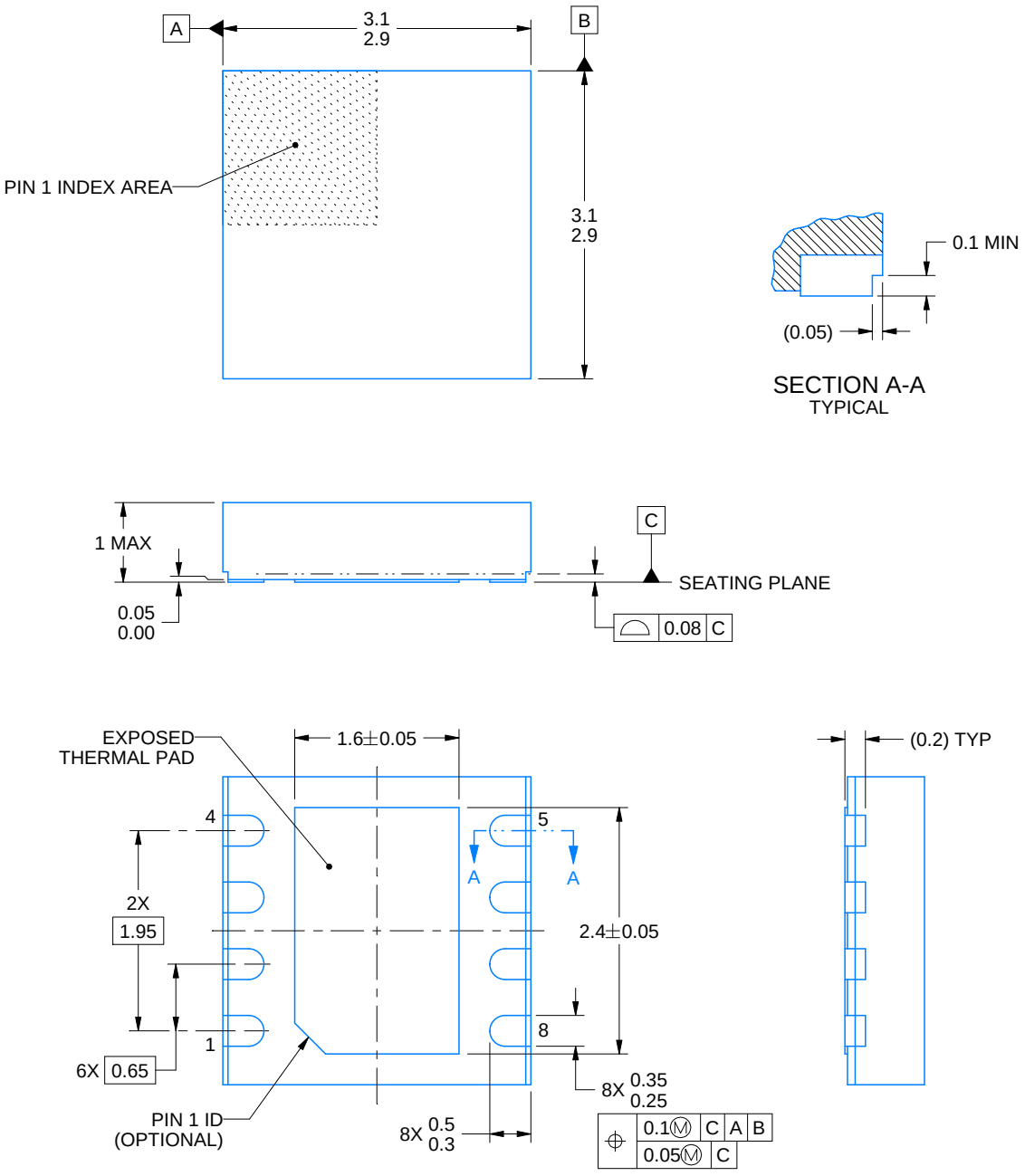
4203482/L

DRB0008F

PACKAGE OUTLINE

VSON - 1 mm max height

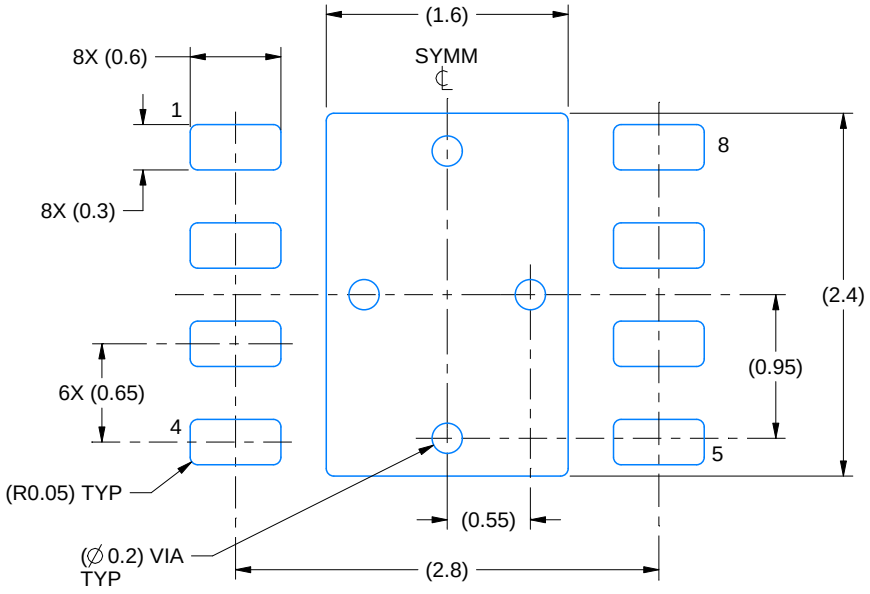
PLASTIC SMALL OUTLINE - NO LEAD



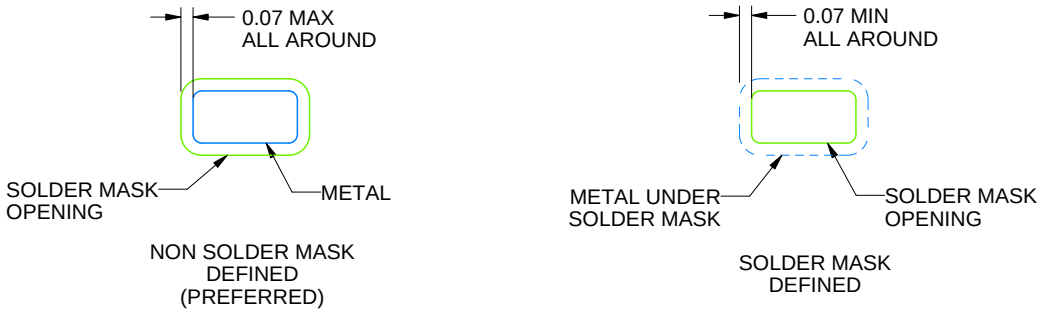
4222121/C 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

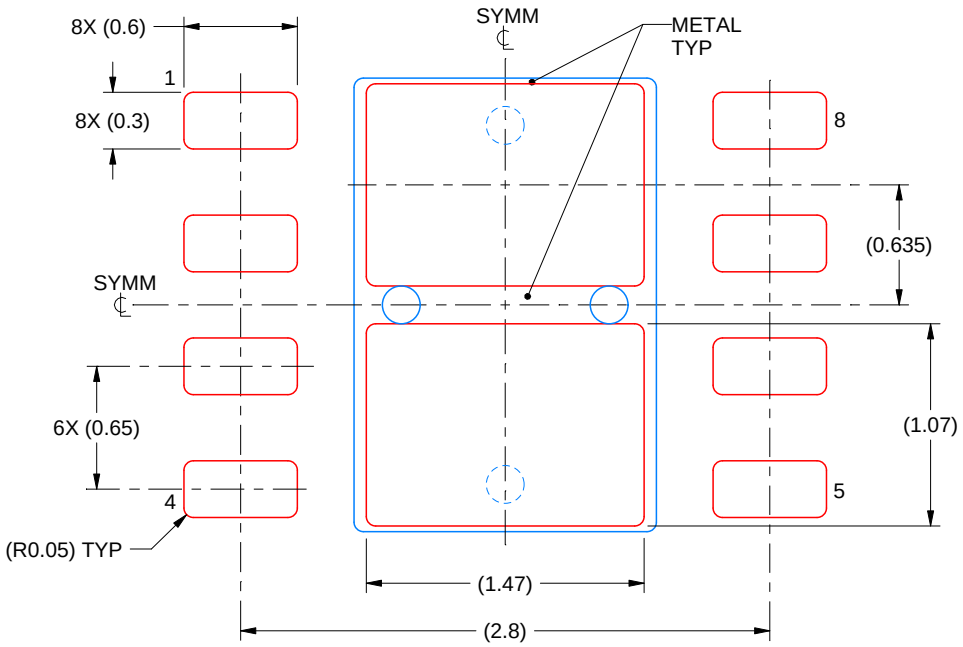


SOLDER MASK DETAILS

4222121/C 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



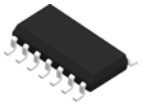
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

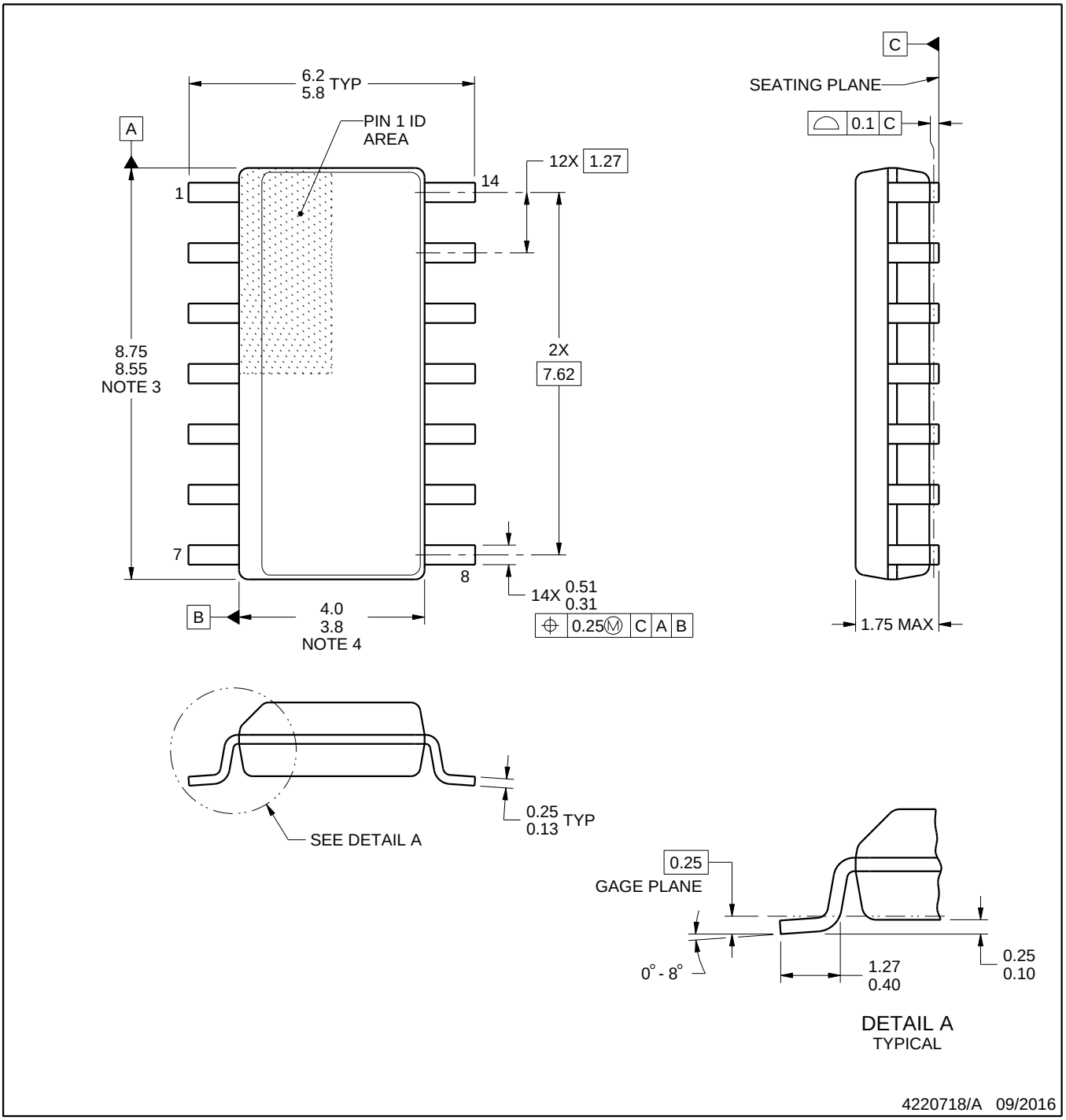


PACKAGE OUTLINE

D0014A

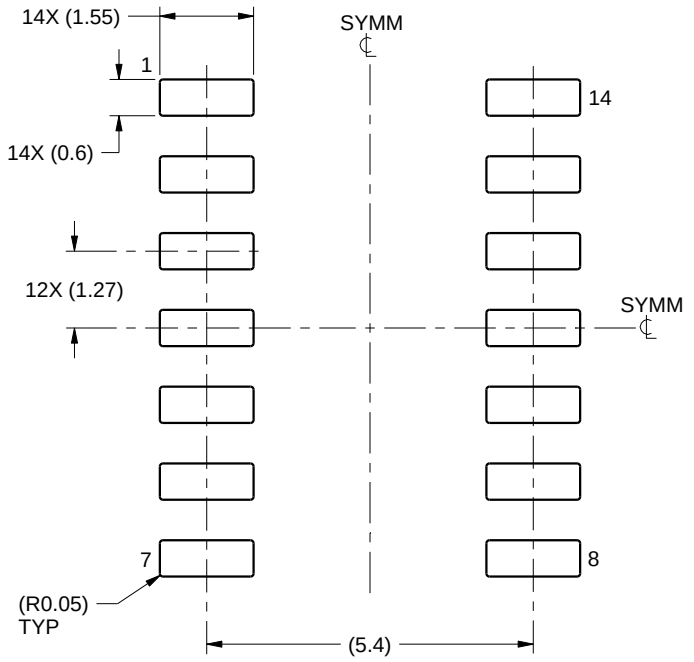
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

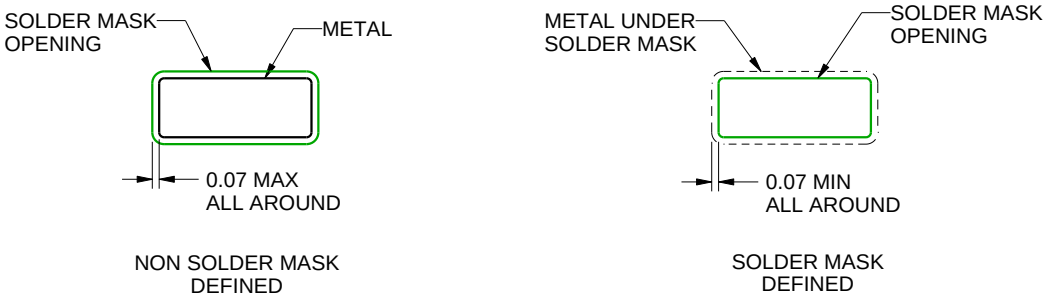


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

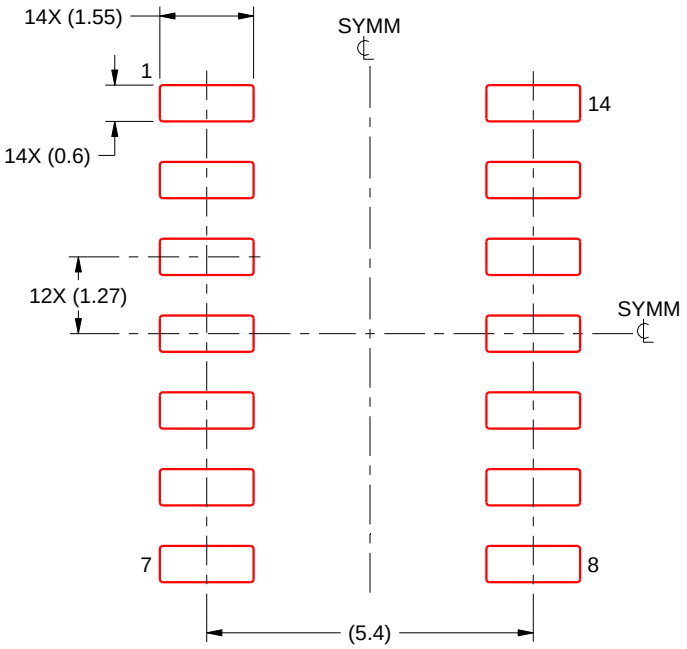
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

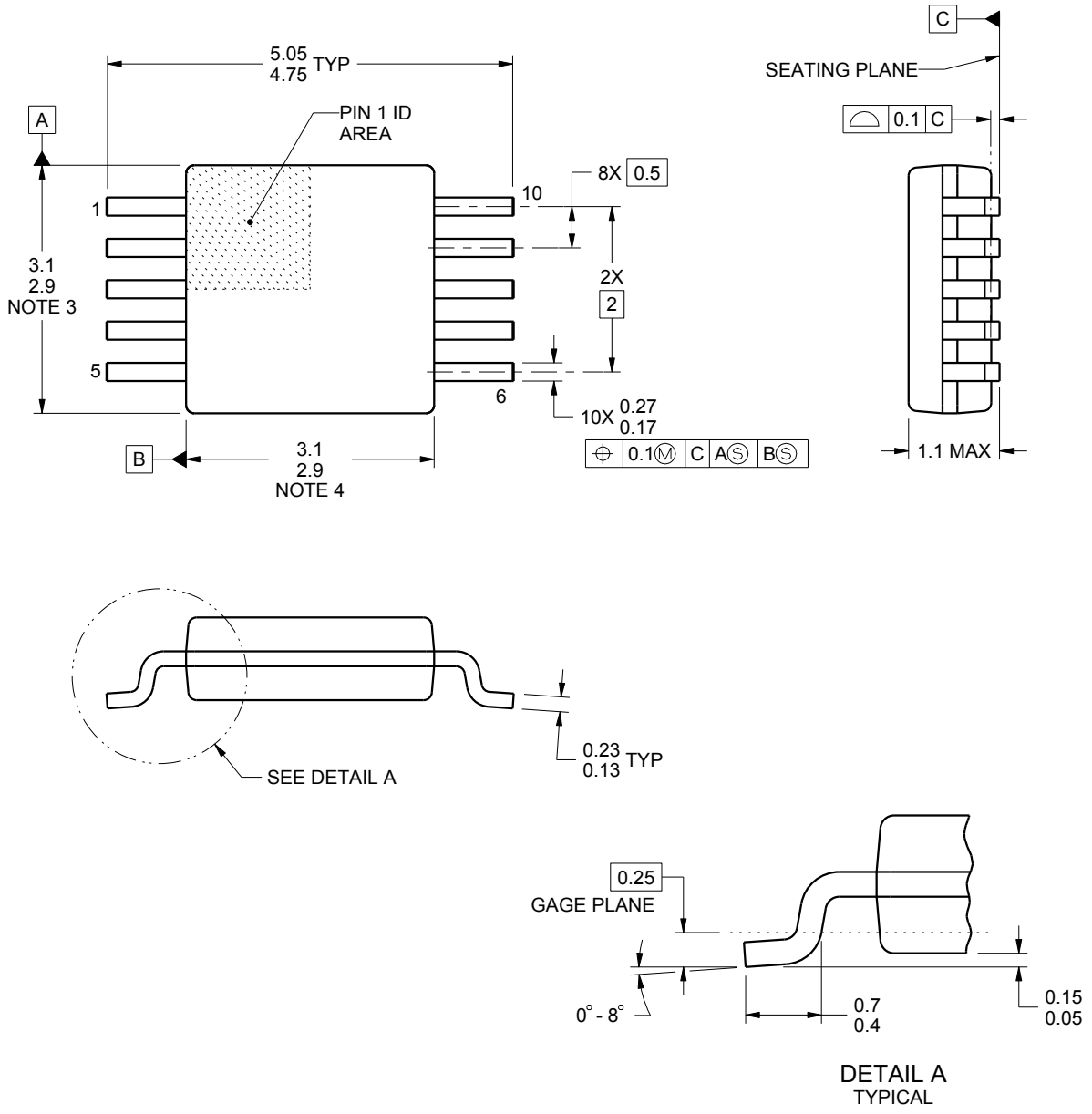
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

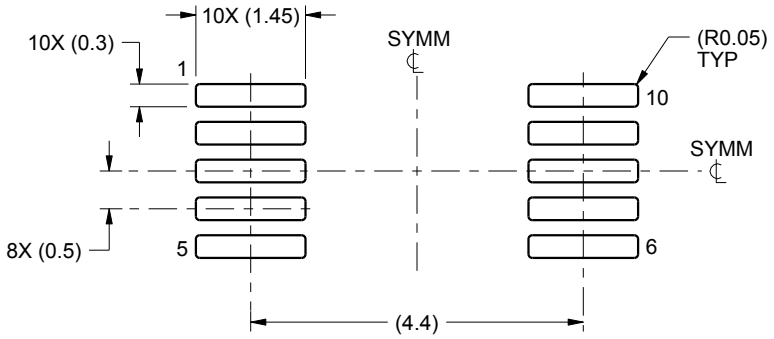
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

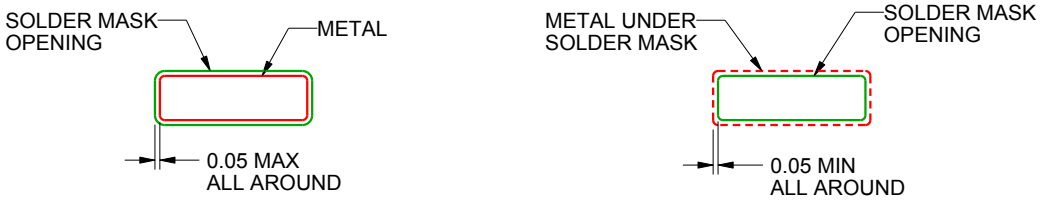


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

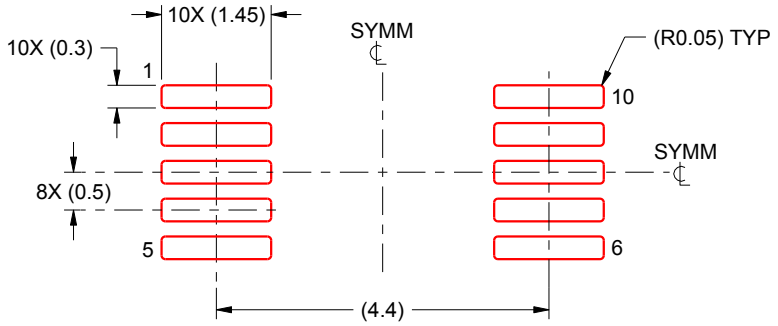


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

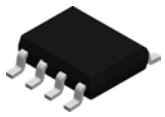


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

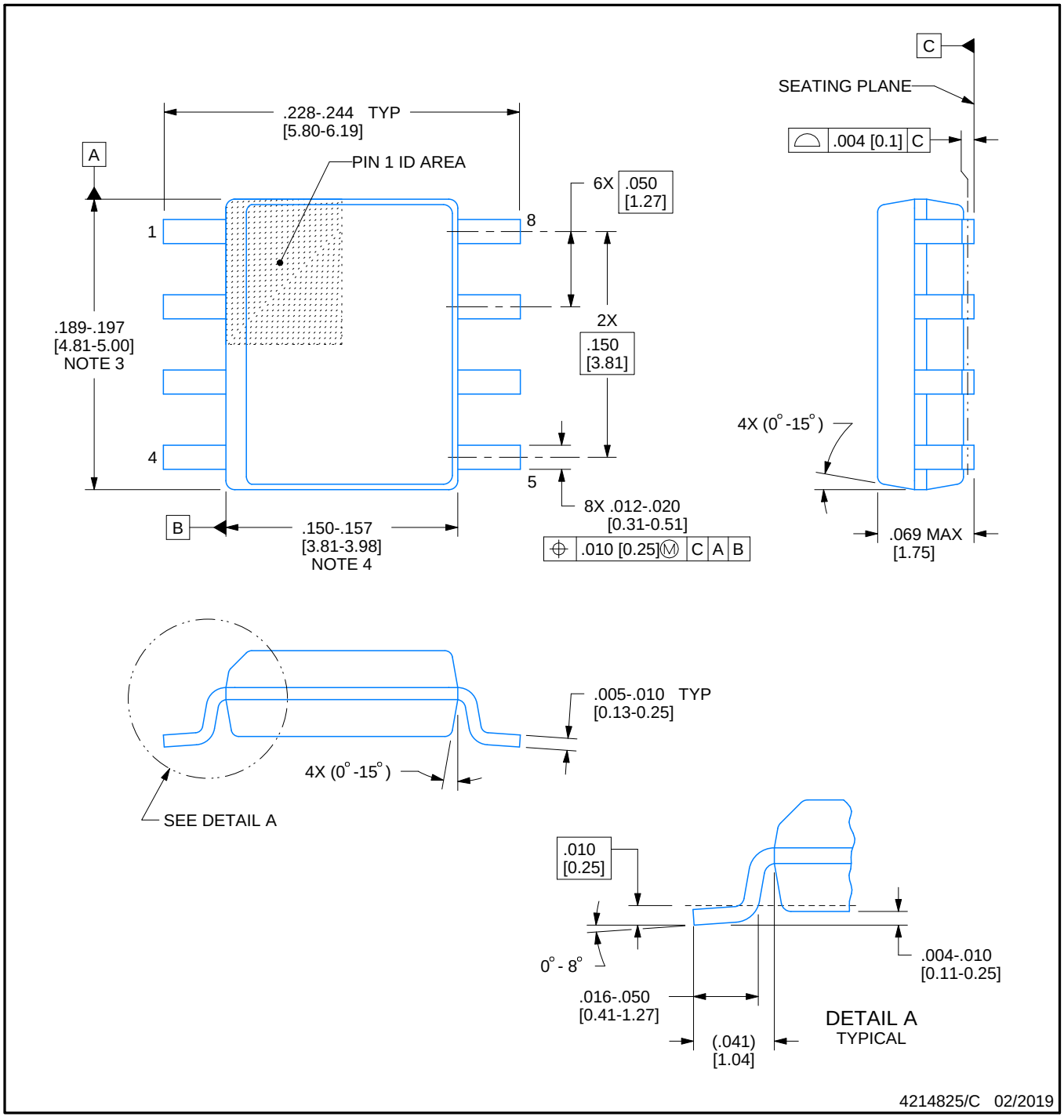


PACKAGE OUTLINE

D0008A

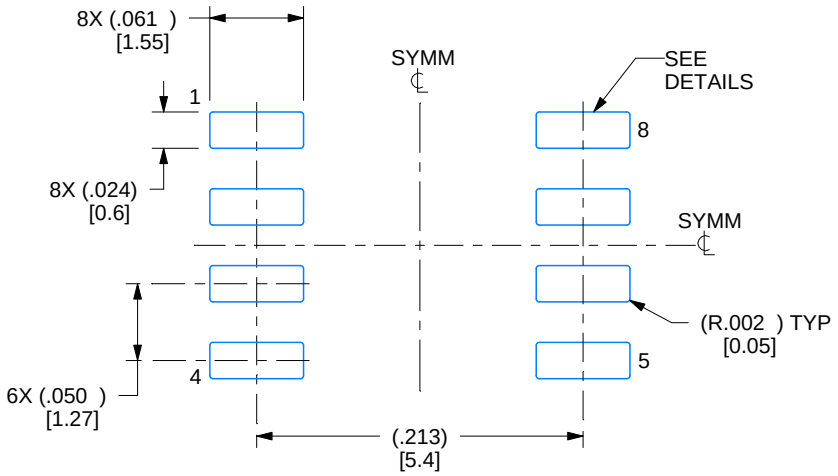
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

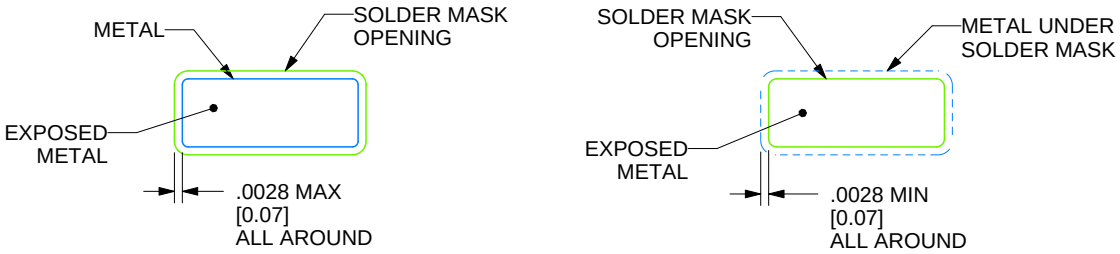


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

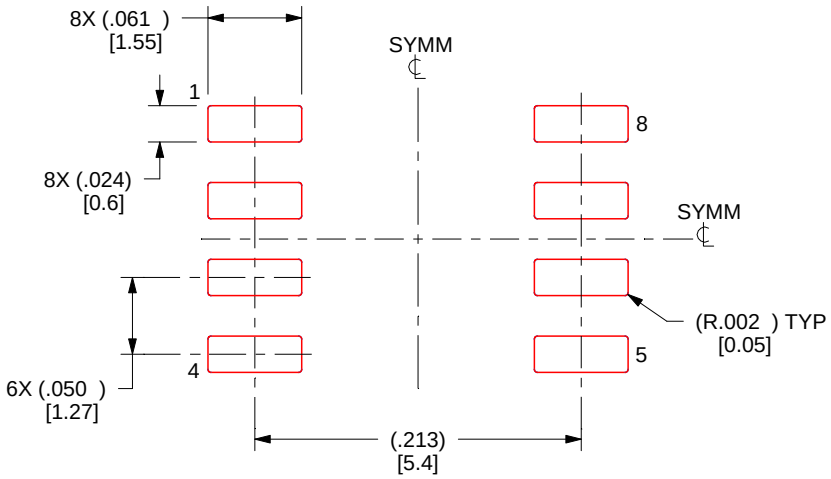
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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