

THVD24x9 小型パッケージに封止したサージ保護および高バス フォルト保護機能搭載、3V~5.5V RS -485 トランシーバ

1 特長

- TIA/EIA-485A 規格の要件に適合またはそれを上回る性能
- 電源電圧: 3V~5.5V
- 9mm² パッケージに封止した業界最小のサージ統合型 RS-485 デバイス
- 1.65V~V_{CC} 電源電圧レベルの V_{IO} をサポート
- バス I/O 保護
 - ±3kV/42Ω IEC 61000-4-5 1.2/50μs サージ (SOIC)
 - ±1.5kV/42Ω IEC 61000-4-5 1.2/50μs サージ (VSON)
 - ±8kV IEC 61000-4-2 接触放電
 - ±4kV IEC 61000-4-4 電気的高速過渡
 - ±15kV HBM ESD
 - DC ± 42V バス フォルト
- 2 つの速度グレードで供給
 - THVD2419: 250kbps
 - THVD2429: 20Mbps
- 広い周囲温度範囲: -40°C~125°C
- 広い動作同相範囲: ± 25V
- 大きなレシーバ ヒステリシスによるノイズ除去
- シャットダウン モード時に低電力消費: 5μA 未満
- グリッチのない電源投入 / 切断によるホット プラグイン 機能
- 開放、短絡、アイドル バスのフェイルセーフ
- 1/8 単位負荷 (最大 256 のバス ノード)
- 業界標準の 8 ピン SOIC によるドロップイン互換
- 小型サージ統合型 RS-485 デバイス、3mm × 3mm リードレス (VSON) パッケージ

2 アプリケーション

- ワイヤレス インフラ
- ファクトリ オートメーション
- モーター ドライブ
- ビル オートメーション
- HVAC
- グリッド インフラストラクチャ

3 概要

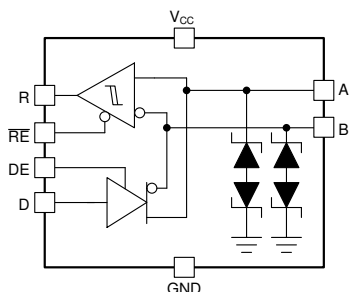
THVD24x9 デバイスは、サージ保護機能を備えた半二重 RS-485 トランシーバです。標準の 8 ピン SOIC (D) パッケージ、また小型の 10 ピン VSON パッケージに過渡電圧抑制 (TVS) ダイオードを内蔵することで、サージ保護機能を実現しています。この機能は、データ ケーブルに結合するノイズ過渡に対する耐性を高めることで信頼性を向上させ、外付け保護部品を不要にします。

標準ピン配置 SOIC パッケージの THVD24x9 デバイスは、3.3V または 5V の単一電源で動作します。さらに、10 ピン VSON パッケージの THVD24x9 デバイスは、最低 1.65V の電源電圧で IO を動作させるため、追加の V_{IO} 電源をサポートしています。このファミリのデバイスは同相電圧範囲が広いと、長いケーブルを使用するマルチポイント アプリケーションに適しています。

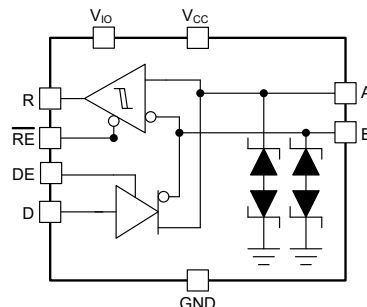
パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
THVD2419	SOIC (8)	4.9mm × 6mm
THVD2429	VSON (10)	3mm × 3mm

- (1) 詳細については、[セクション 12](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



THVD24x9 のブロック図 (SOIC パッケージ)



THVD24x9 のブロック図 (VSON パッケージ)



Table of Contents

1 特長	1	8.2 Functional Block Diagrams.....	14
2 アプリケーション	1	8.3 Feature Description.....	14
3 概要	1	8.4 Device Functional Modes.....	18
4 Device Comparison Table	2	9 Application and Implementation	19
5 Pin Configuration and Functions	3	9.1 Application Information.....	19
6 Specifications	4	9.2 Typical Application.....	19
6.1 Absolute Maximum Ratings.....	4	9.3 Power Supply Recommendations.....	22
6.2 ESD Ratings.....	4	9.4 Layout.....	23
6.3 ESD Ratings - IEC Specifications.....	4	10 Device and Documentation Support	24
6.4 Recommended Operating Conditions.....	5	10.1 Device Support.....	24
6.5 Thermal Information.....	5	10.2 ドキュメントの更新通知を受け取る方法.....	24
6.6 Power Dissipation.....	5	10.3 サポート・リソース.....	24
6.7 Electrical Characteristics.....	6	10.4 Trademarks.....	24
6.8 Switching Characteristics 250kbps.....	8	10.5 静電気放電に関する注意事項.....	24
6.9 Switching Characteristics 20Mbps.....	8	10.6 用語集.....	24
6.10 Typical Characteristics.....	10	11 Revision History	24
7 Parameter Measurement Information	12	12 Mechanical, Packaging, and Orderable Information	24
8 Detailed Description	14		
8.1 Overview.....	14		

4 Device Comparison Table

PART NUMBER	PACKAGE	V _{IO}	SIGNALING RATE	NODES
THVD2419	SOIC-8	No	up to 250kbps	256
THVD2429			up to 20Mbps	
THVD2419	VSON-10	Yes	up to 250kbps	
THVD2429			up to 20Mbps	

5 Pin Configuration and Functions

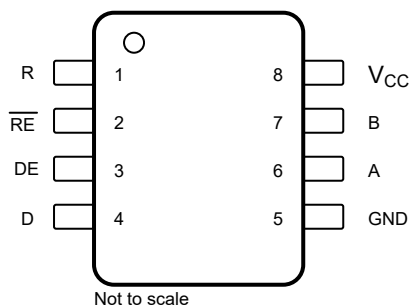


図 5-1. THVD2419, THVD2429, 8-Pin (SOIC)
(Top View)

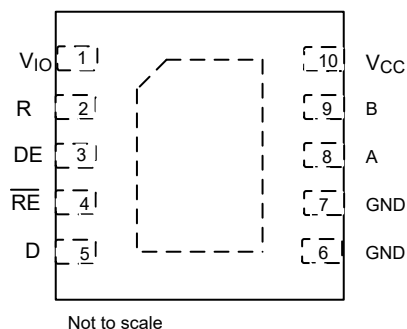


図 5-2. THVD2419, THVD2429, 10-Pin (VSON)
(Top View)

NAME	PIN		TYPE	DESCRIPTION
	SOIC-8	VSON-10		
V _{IO}	-	1	P	1.8V to 5V supply for R, D, and RE and DE
R	1	2	O	Receiver data output
RE	2	4	I	Receiver enable, active low (integrated pull-up)
DE	3	3	I	Driver enable, active high (integrated pull-down)
D	4	5	I	Driver data input (integrated pull-up)
GND	5	6, 7	-	Device ground
A	6	8	I/O	Bus I/O port, A (complementary to B)
B	7	9	I/O	Bus I/O port, B (complementary to A)
V _{CC}	8	10	P	3.3V to 5V supply for the device

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Logic supply voltage	V_{IO}	-0.5	$V_{CC} + 0.2$	V
Bus supply voltage	V_{CC}	-0.5	6.5	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-42	42	V
Input voltage	Range at any logic pin (D, DE, SLR or RE) for devices with VIO pin	-0.3	$V_{IO} + 0.2$	V
Input voltage	Range at any logic pin (D, DE, SLR or RE) for devices with no VIO pin	-0.3	$V_{CC} + 0.2$	V
Receiver output current	I_O	-24	24	mA
Storage temperature	T_{stg}	-65	170	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1,500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, bus terminals	Contact discharge, per IEC 61000-4-2 ⁽¹⁾	Bus terminals and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2 ⁽¹⁾	Bus terminals and GND	±15,000	
$V_{(SURGE)}$	Surge	Per IEC 61000-4-5, 1.2/50-8/20μs CWG (DRC Package)	Bus terminals and GND	±1500	V
$V_{(SURGE)}$	Surge	Per IEC 61000-4-5, 1.2/50-8/20μs CWG (D Package)	Bus terminals and GND	±3,000	V

- (1) For optimised IEC ESD performance, it is recommended to have series resistor ($\geq 50 \Omega$) on all logic inputs to minimize transient currents going into or out of the logic pins.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3		5.5	V
V _{IO}	I/O supply voltage (devices with VIO pin)	1.65		V _{CC}	V
V _{IH}	High-level input voltage (D, DE, RE)	0.7		1	V _{IO}
V _{IL}	Low-level input voltage (D, DE, RE)			0.3	V _{IO}
V _{IH}	High-level input voltage (D, DE, RE)	0.7		1	V _{CC}
V _{IL}	Low-level input voltage (D, DE, RE)			0.3	V _{CC}
V _I	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾	–25		25	V
V _{ID}	Differential input voltage	–25		25	V
I _O	Output current, driver	–60		60	mA
I _{OR}	Output current, receiver	V _{IO} = 1.8V or 2.5V (devices with VIO pin)		4	mA
I _{OR}	Output current, receiver	V _{IO} = 3.3V or 5V (devices with VIO pin) or V _{CC} = 3.3V or 5V (devices without VIO pin)		8	mA
R _L	Differential load resistance	54	60		Ω
1/t _{UI}	Signaling rate	THVD2419		250	kbps
		THVD2429		20	Mbps
T _A	Operating ambient temperature	–40		125	°C
T _J	Junction temperature	–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		THVD2419, THVD2429		UNIT
		DRC (VSON)	D (SOIC)	
		10 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	65.2	117.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	41.7	40.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	36.4	65.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.4	3.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	36.3	64.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	24.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Power Dissipation

PARAMETER	TEST CONDITIONS	VALUE	UNIT
P _D	Unterminated R _L = 300Ω, C _L = 50pF (driver)	THVD2419 250kbps	180
		THVD2429 20Mbps	310
	RS-422 load R _L = 100Ω, C _L = 50pF (driver)	THVD2419 250kbps	180
		THVD2429 20Mbps	310
	RS-485 load R _L = 54Ω, C _L = 50pF (driver)	THVD2419 250kbps	270
		THVD2429 20Mbps	325

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5V$, $V_{IO} = 3.3V$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60\Omega$, $-25V \leq V_{test} \leq 25V$ (See Figure 7-1)	1.5	2.8		V
		$R_L = 60\Omega$, $-25V \leq V_{test} \leq 25V$, $4.5V \leq V_{CC} \leq 5.5V$ (See Figure 7-1)	2.1	3.3		V
		$R_L = 100\Omega$ (See Figure 7-2)	2	2.9		V
		$R_L = 54\Omega$ (See Figure 7-2)	1.5	2.5		V
$\Delta V_{OD} $	Change in differential output voltage	$R_L = 54\Omega$ or 100Ω (See Figure 7-2)	-50		50	mV
V_{OC}	Common-mode output voltage		1	$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		-50		50	mV
I_{OS}	Short-circuit output current	$DE = V_{IO}$, $-42V \leq (V_A \text{ or } V_B) \leq 42V$, or A shorted to B	-250		250	mA
Receiver						
I_I	Bus input current	$DE = 0V$, V_{CC} and $V_{IO} = 0V$ or $5.5V$	$V_I = 12V$	90	125	μA
			$V_I = 25V$	200	250	μA
			$V_I = -7V$	-100	-80	μA
			$V_I = -25V$	-350	-240	μA
V_{TH+}	Positive-going input threshold voltage ⁽¹⁾	Over common-mode range of $\pm 25V$	20	125	200	mV
V_{TH-}	Negative-going input threshold voltage ⁽¹⁾		-200	-125	-20	mV
V_{HYS}	Input hysteresis			250		mV
V_{TH_FSH}	Input fail-safe threshold		-20		20	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, $f = 1MHz$		50		pF
V_{OH}	Output high voltage	$I_{OH} = -8mA$, $V_{IO} = 3$ to $3.6V$ or $4.5V$ to $5.5V$	$V_{IO} - 0.4$	$V_{IO} - 0.2$		V
V_{OL}	Output low voltage	$I_{OL} = 8mA$, $V_{IO} = 3$ to $3.6V$ or $4.5V$ to $5.5V$		0.2	0.4	V
V_{OH}	Output high voltage	$I_{OH} = -4mA$, $V_{IO} = 1.65$ to $1.95V$ or $2.25V$ to $2.75V$	$V_{IO} - 0.4$	$V_{IO} - 0.2$		V
V_{OL}	Output low voltage	$I_{OL} = 4mA$, $V_{IO} = 1.65$ to $1.95V$ or $2.25V$ to $2.75V$		0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	$V_O = 0V$ or V_{IO} , $RE = V_{IO}$	-1		1	μA
Logic						
I_{IN}	Input current (DE, SLR)	DRC: $1.65V \leq V_{IO} \leq 5.5V$, $0V \leq V_{IN} \leq V_{IO}$ D: $3V \leq V_{CC} \leq 5.5V$, $0V \leq V_{IN} \leq 5.5V$			5	μA
I_{IN}	Input current (D, RE)	DRC: $1.65V \leq V_{IO} \leq 5.5V$, $0V \leq V_{IN} \leq V_{IO}$ D: $3V \leq V_{CC} \leq 5.5V$, $0V \leq V_{IN} \leq 5.5V$	-5			μA
Thermal Protection						
T_{SHDN}	Thermal shutdown threshold	Temperature rising	150	180		°C
T_{HYS}	Thermal shutdown hysteresis			10		°C
Supply						
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}			2.3	2.6	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}		1.95	2.2		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}			150		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}			1.4	1.6	V

6.7 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5V$, $V_{IO} = 3.3V$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}			1.2	1.3		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				120		mV
I_{CC}	Supply current (quiescent), $V_{CC} = 4.5V$ to $5.5V$	Driver and receiver enabled	$\overline{RE} = 0V$, $DE = V_{IO}$, No load		3.5	5.7	mA
		Driver enabled, receiver disabled	$\overline{RE} = V_{IO}$, $DE = V_{IO}$, No load		2.5	4.4	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0V$, $DE = 0V$, No load		1.8	2.4	mA
		Driver and receiver disabled (devices without VIO pin)	$\overline{RE} = V_{CC}$, $DE = 0V$, D = open, No load		1.7	5	μA
		Driver and receiver disabled (devices with VIO pin)	$\overline{RE} = V_{IO}$, $DE = 0V$, D = open, No load		0.1	3	μA
I_{CC}	Supply current (quiescent), $V_{CC} = 3V$ to $3.6V$	Driver and receiver enabled	$\overline{RE} = 0V$, $DE = V_{IO}$, No load		3	4.6	mA
		Driver enabled, receiver disabled	$\overline{RE} = V_{IO}$, $DE = V_{IO}$, No load		2.2	3.3	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0V$, $DE = 0V$, No load		1.6	2.2	mA
		Driver and receiver disabled (Devices without VIO pin)	$\overline{RE} = V_{CC}$, $DE = 0V$, D = open, No load		1	4	μA
		Driver and receiver disabled (Devices with VIO pin)	$\overline{RE} = V_{IO}$, $DE = 0V$, D = open, No load		1	2	μA
I_{IO}	Logic supply current (quiescent), $V_{IO} = 3$ to $3.6V$, Devices with VIO pin	Driver disabled, Receiver enabled	$DE = 0V$, $\overline{RE} = 0V$, No load		3.3	8.4	μA
		Driver disabled, Receiver disabled	$DE = 0V$, $\overline{RE} = V_{IO}$, No load		0.1	2	μA

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-} .

6.8 Switching Characteristics 250kbps

250kbps (THVD2419) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5V$, $V_{IO} = 3.3V$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
Driver								
t _r , t _f	Differential output rise/fall time	R _L = 54 Ω, C _L = 50 pF See 7-3	V _{CC} = 3 to 3.6V, Typical at 3.3V	400	625	1200	ns	
			V _{CC} = 4.5 to 5.5V, Typical at 5V	500	725	1200	ns	
t _{PHL} , t _{PLH}	Propagation delay	R _L = 54 Ω, C _L = 50 pF See 7-3		510		750	ns	
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}			5		70	ns	
t _{PHZ} , t _{PLZ}	Disable time	See 7-4 and 7-5	RE = X	45		75	ns	
t _{PZH} , t _{PZL}	Enable time		RE = 0V	80		290	ns	
			RE = V _{IO}	2.5		4.5	μs	
t _{SHDN}	Time to shutdown		RE = V _{IO}	50		500	ns	
Receiver								
t _r , t _f	Output rise/fall time	C _L = 15 pF See 7-6		3		20	ns	
t _{PHL} , t _{PLH}	Propagation delay			750		1270	ns	
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}			5		45	ns	
t _{PHZ} , t _{PLZ}	Disable time	DE = X		30		40	ns	
t _{PZH(1)}	Enable time			80		130	ns	
t _{PZL(1)}	Enable time	See 7-7		800		1320	ns	
t _{PZH(2)} , t _{PZL(2)}	Enable time	See 7-8	DE = 0V	3		5.4	μs	
t _{D(OFS)}	Delay to enter fail-safe operation	See 7-9	C _L = 15pF	7		11	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation			540		750	1260	ns
t _{SHDN}	Time to shutdown	See 7-8	DE = 0V	50		500	ns	

(1) A, B are driver output and receiver input terminals for Half duplex devices. A, B are RX input, Y/Z are driver output terminals for Full duplex device

6.9 Switching Characteristics 20Mbps

20Mbps (THVD2429) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5V$, $V_{IO} = 3.3V$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t _r , t _f	Differential output rise/fall time	R _L = 54Ω, C _L = 50pF See 7-3		3.5	5	15	ns
t _{PHL} , t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF See 7-3		6	15	30	ns
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}	R _L = 54Ω, C _L = 50pF See 7-3			0.5	3	ns
t _{PHZ} , t _{PLZ}	Disable time	See 7-4 and 7-5	RE = X		20	35	ns
t _{PZH} , t _{PZL}	Enable time		RE = 0V		16	40	ns
			RE = V _{IO}		2.5	4.5	μs
t _{SHDN}	Time to shutdown		RE = V _{IO}		50		500
Receiver							
t _r , t _f	Output rise/fall time	C _L = 15pF, See 7-6			1.5	6	ns
t _{PHL} , t _{PLH}	Propagation delay			25	35	60	ns
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}					5.5	ns
t _{PHZ} , t _{PLZ}	Disable time	DE = X			18	25	ns
t _{PZH(1)} , t _{PZL(1)}	Enable time	See 7-7	DE = V _{IO}		55	82	ns

6.9 Switching Characteristics 20Mbps (続き)

20Mbps (THVD2429) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5$ V, $V_{IO} = 3.3$ V, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	See 図 7-8	DE = 0V		2.5	4.5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	See 図 7-9	$C_L = 15$ pF	7	10	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			19	35	50	ns
t_{SHDN}	Time to shutdown	See 図 7-8	DE = 0V	50		500	ns

- (1) A, B are driver output and receiver input terminals for Half duplex devices. A, B are RX input, Y/Z are driver output terminals for Full duplex device

6.10 Typical Characteristics

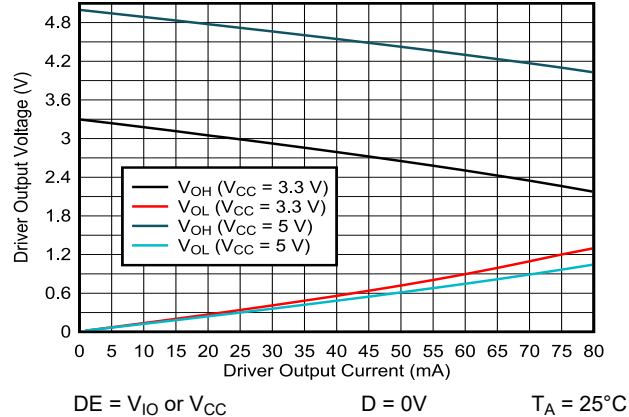


Figure 6-1. Driver Output Voltage vs Driver Output Current

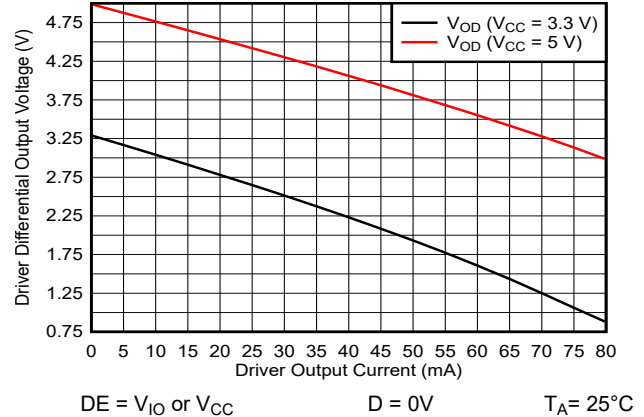


Figure 6-2. Driver Differential Output Voltage vs Driver Output Current

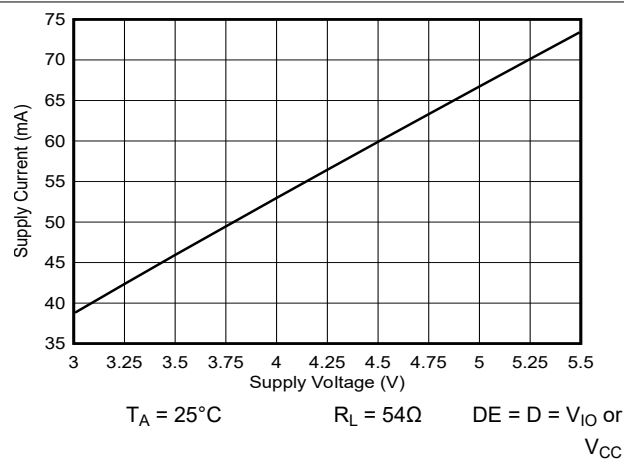


Figure 6-3. Driver Output Current vs Supply Voltage

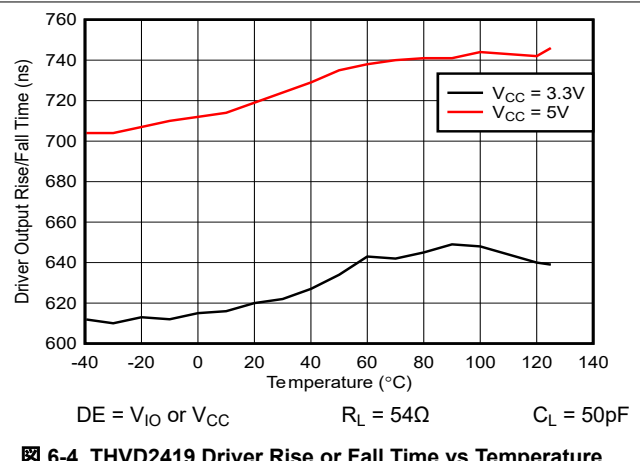


Figure 6-4. THVD2419 Driver Rise or Fall Time vs Temperature

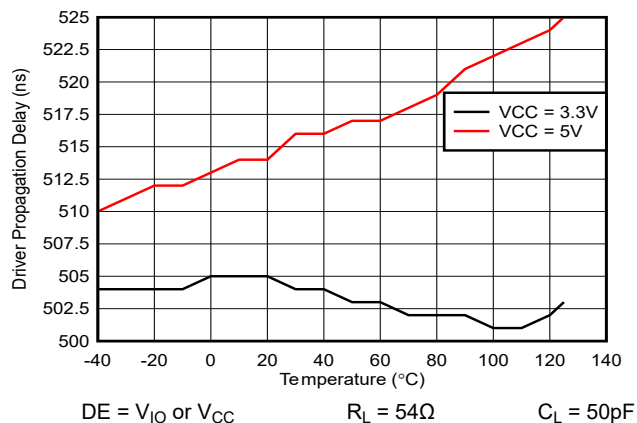


Figure 6-5. THVD2419 Driver Propagation Delay vs Temperature

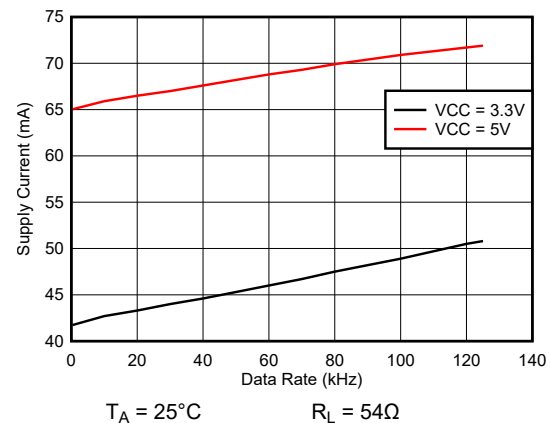
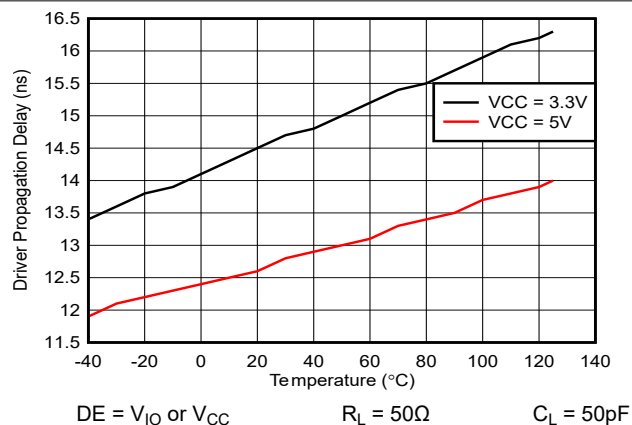
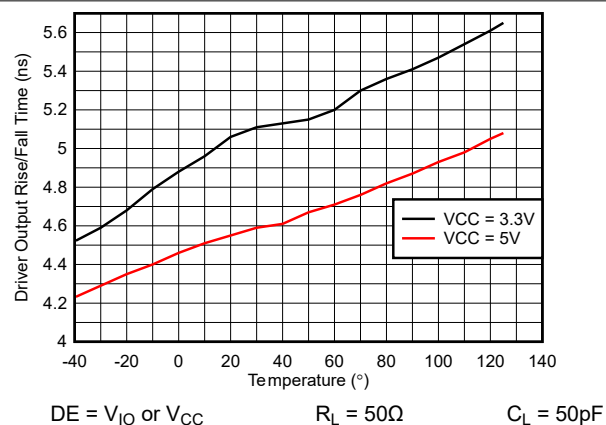


Figure 6-6. THVD2419 Supply Current vs Signal Rate

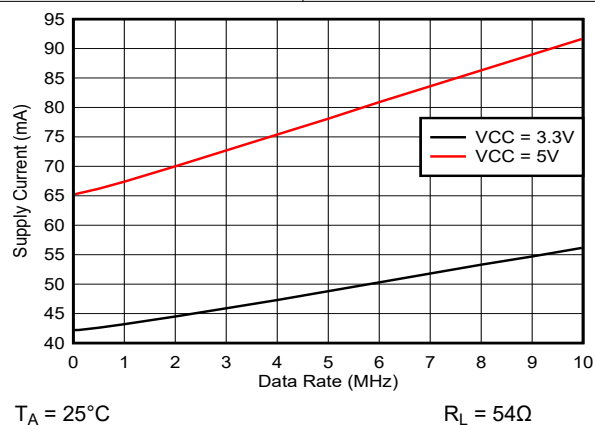
6.10 Typical Characteristics (continued)



6-7. THVD2429 Driver Propagation Delay vs Temperature



6-8. THVD2429 Driver Rise or Fall Time vs Temperature



6-9. THVD2429 Supply Current vs Signal Rate

7 Parameter Measurement Information

注

Note: Digital input/output supply in the diagrams below could either be V_{CC} (devices without V_{IO} pin) or V_{IO} (devices with V_{IO} pin)

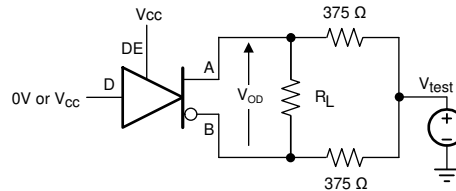


図 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

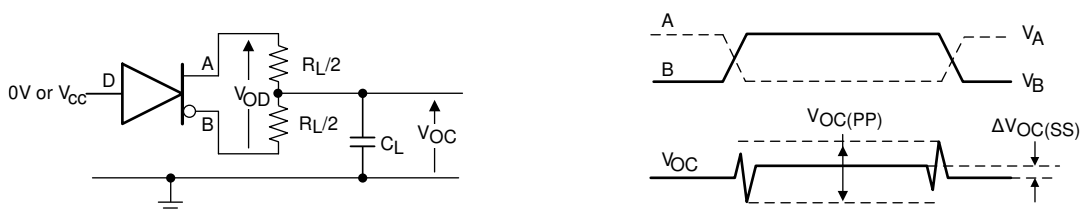


図 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

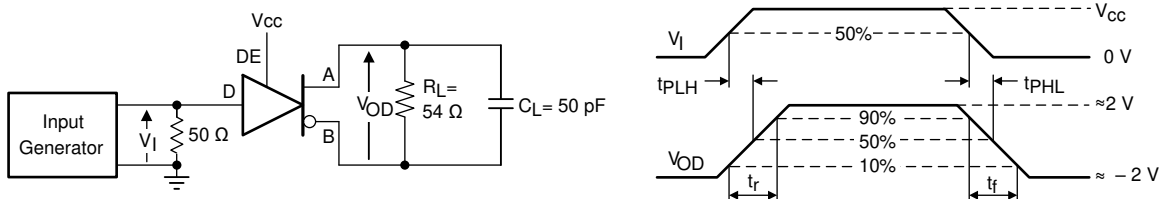


図 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

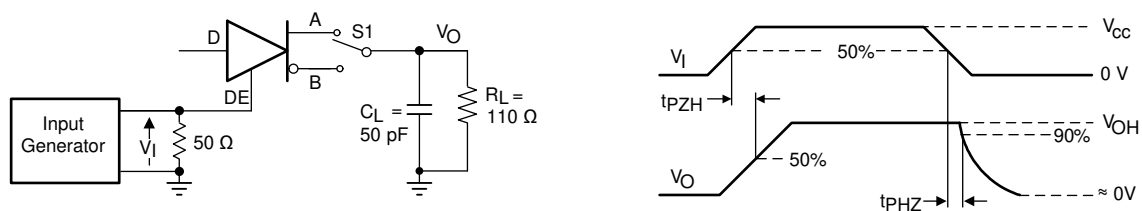


図 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

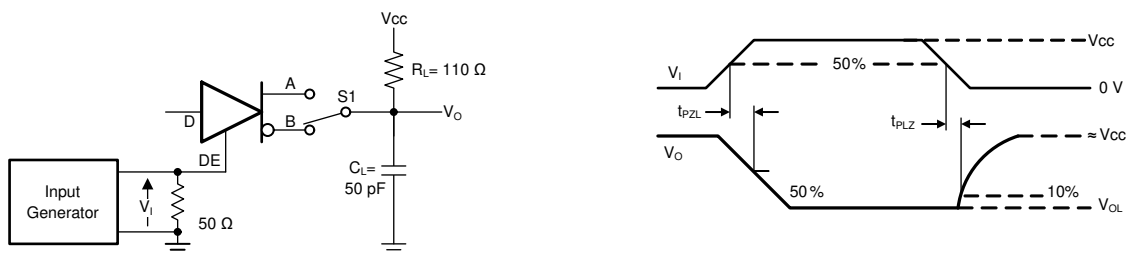
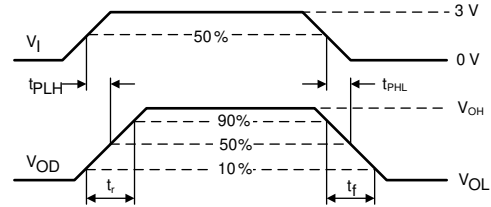
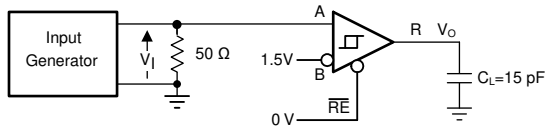
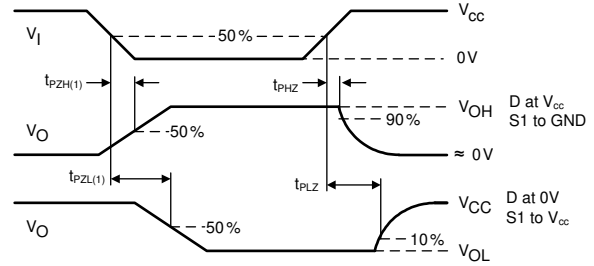
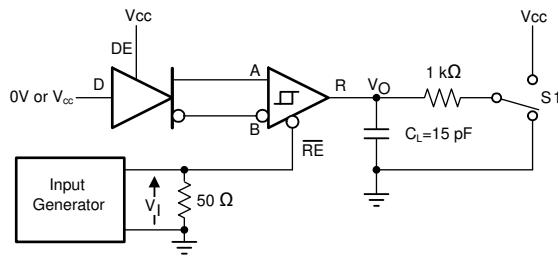


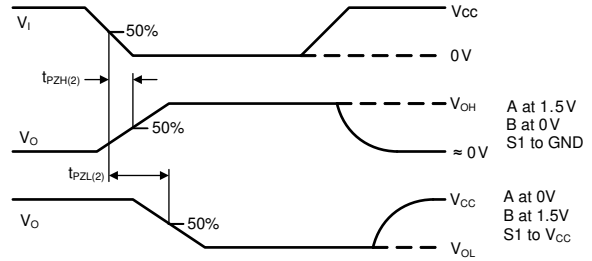
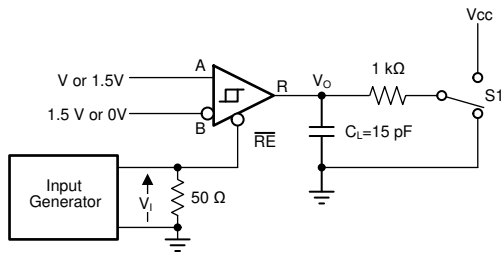
図 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load



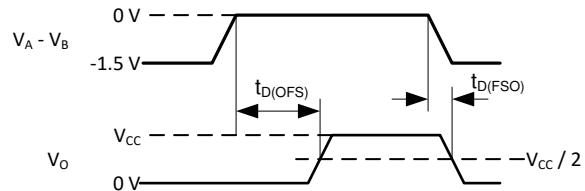
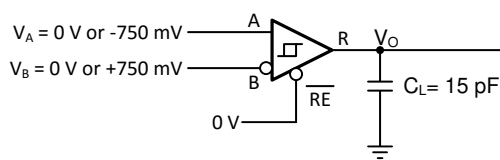
7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays



7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled



7-8. Measurement of Receiver Enable Times With Driver Disabled



Copyright © 2017, Texas Instruments Incorporated

7-9. Fail-Safe Delay Measurements

8 Detailed Description

8.1 Overview

THVD24x9 devices are surge-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 250kbps and 20Mbps respectively. Surge protection is achieved by integrating transient voltage suppressor (TVS) diodes in the standard 8-pin SOIC (D) package and a small 10-pin leadless package.

THVD2419 and THVD2429 devices have active-high driver enables and active-low receiver enables. A low standby current can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagrams

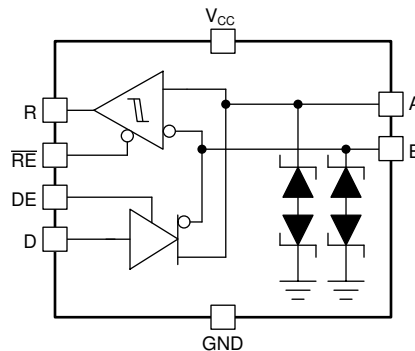


图 8-1. THVD2419 and THVD2429 Block Diagram (SOIC Package)

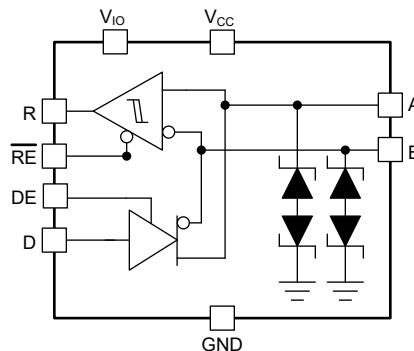


图 8-2. THVD2419 and THVD2429 Block Diagram (VSON Package)

8.3 Feature Description

8.3.1 Electrostatic Discharge (ESD) Protection

The bus pins of the THVD24x9 transceiver family include on-chip ESD protection against $\pm 15\text{kV}$ HBM and $\pm 8\text{kV}$ IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

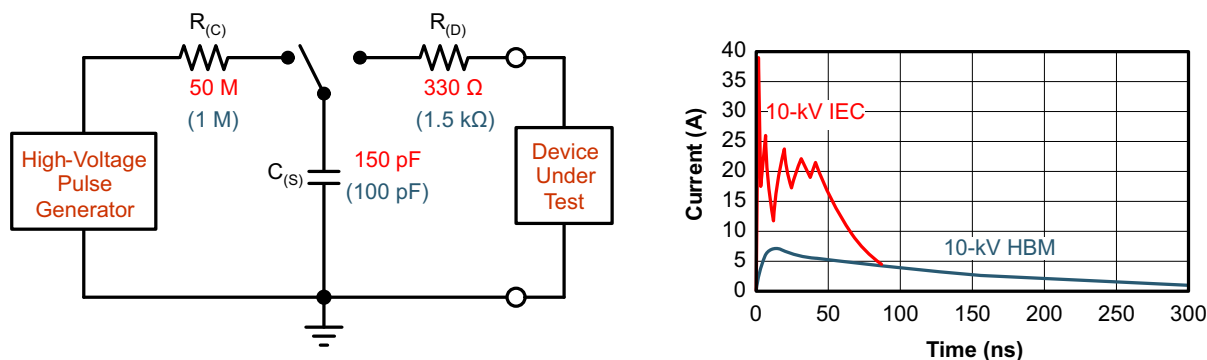


図 8-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables.

8.3.2 Electrical Fast Transient (EFT) Protection

Inductive loads such as relays, switch contactors, or heavy-duty motors can create high-frequency bursts during transition. The IEC 61000-4-4 test is intended to simulate the transients created by such switching of inductive loads on AC power lines. 図 8-4 shows the voltage waveforms in to 50Ω termination as defined by the IEC standard.

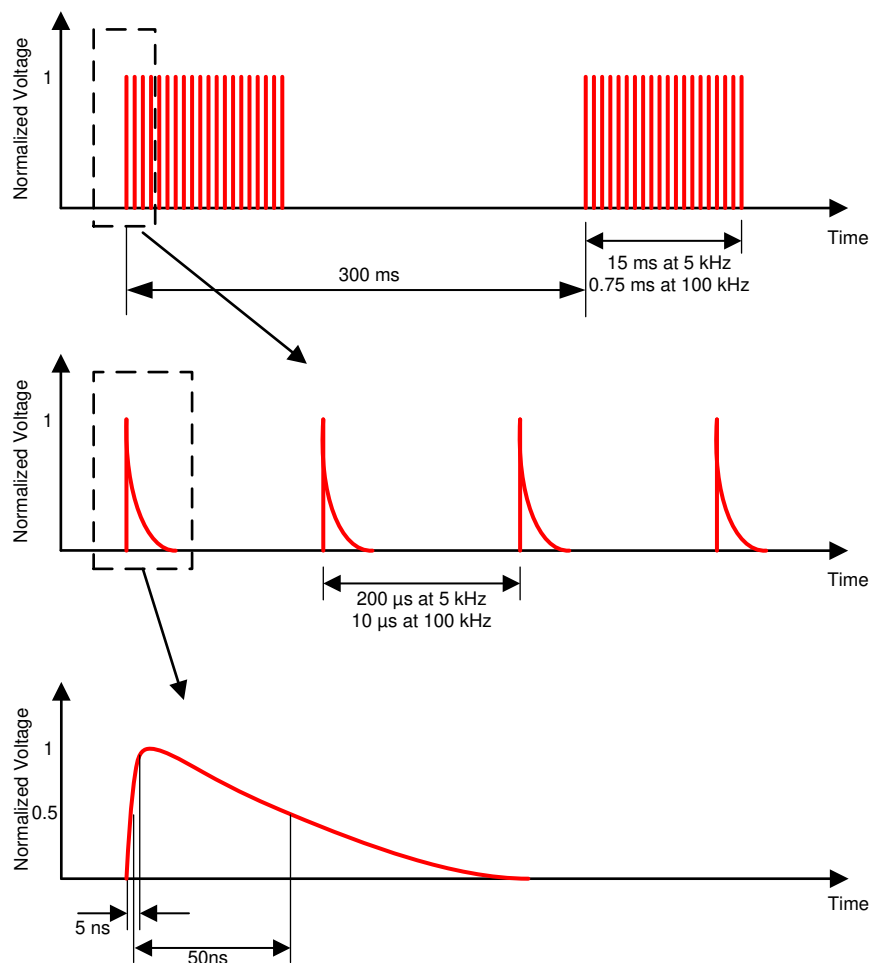


図 8-4. EFT Voltage Waveforms

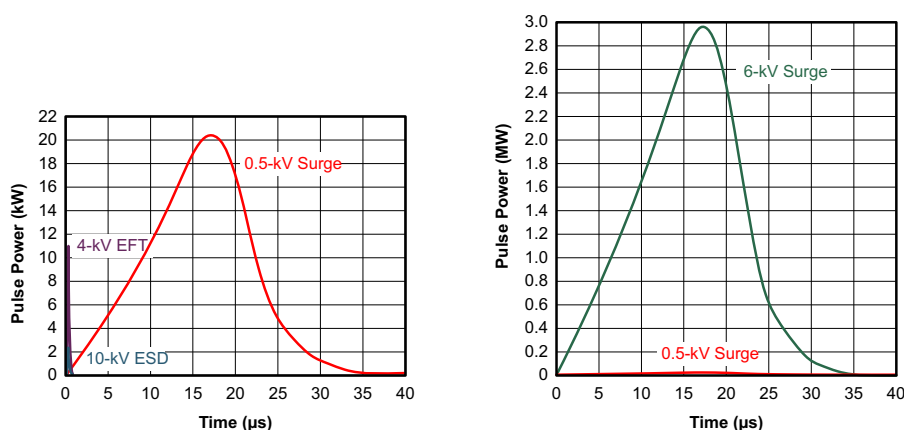
Internal ESD protection circuits of the THVD24x9 protect the transceivers against $\pm 4\text{kV}$ EFT. With careful system design, one could achieve EFT Criterion A (no data loss when transient noise is present).

8.3.3 Surge Protection

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

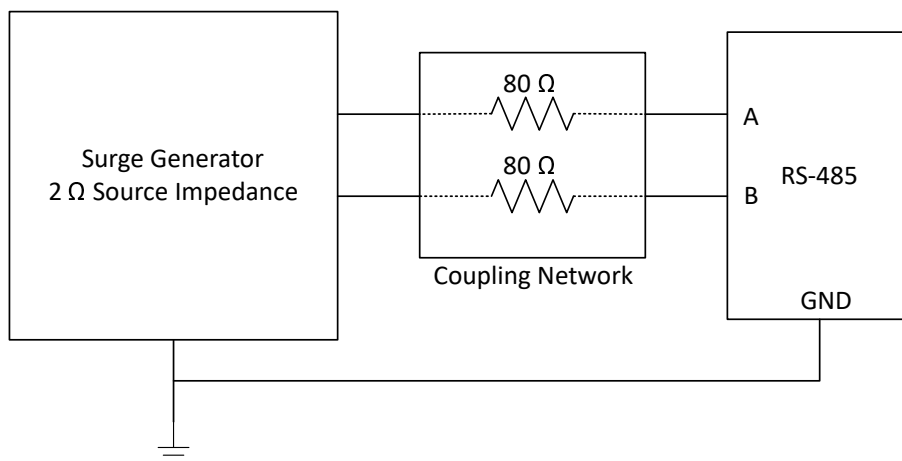
✎ 8-5 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The diagram on the left shows the relative pulse-power for a 0.5kV surge transient and 4kV EFT transient, both of which dwarf the 10kV ESD transient visible in the lower-left corner. 500V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The diagram on the right shows the pulse-power of a 6kV surge transient, relative to the same 0.5kV surge transient. 6kV surge transients are most likely to occur in power generation and power-grid systems.



✎ 8-5. Power Comparison of ESD, EFT, and Surge Transients

✎ 8-6 shows the test setup used to validate THVD24x9 surge performance according to the IEC 61000-4-5 1.2/50μs surge pulse.



✎ 8-6. THVD24x9 Surge Test Setup

THVD24x9 product family is robust up to $\pm 3\text{kV}$ surge transients without the need for any external components. The bus pin voltage is clamped by the integrated surge protection diodes such that the internal circuitry is not damaged during the surge event.

8.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24x9 family feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250mV (typical) hysteresis displays excellent noise immunity.

8.3.5 Failsafe Receiver

The differential receivers of the THVD24x9 family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFs)}$ at less than $|V_{TH_FSH}|$.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. The differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground. When left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} ; thus, when left open while the driver is enabled, output A turns high and B turns low.

表 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+} , the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-} , the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} , the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	\overline{RE}	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	Indeterminate	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

THVD24x9 are half-duplex RS-485 transceivers with integrated system-level surge protection. Standard 8-pin SOIC (D) package allows drop-in replacement into existing systems and eliminate system-level protection components.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , with a value that matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

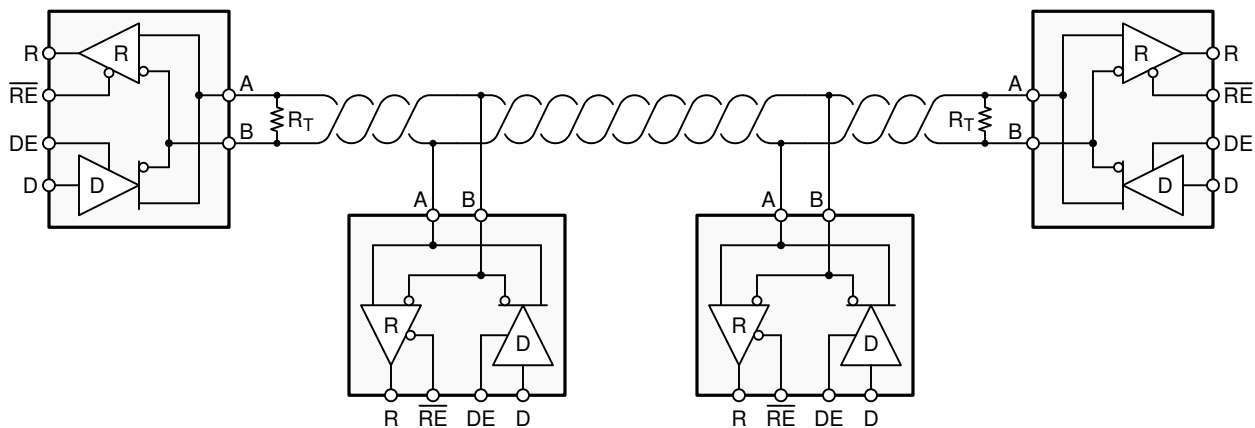


図 9-1. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

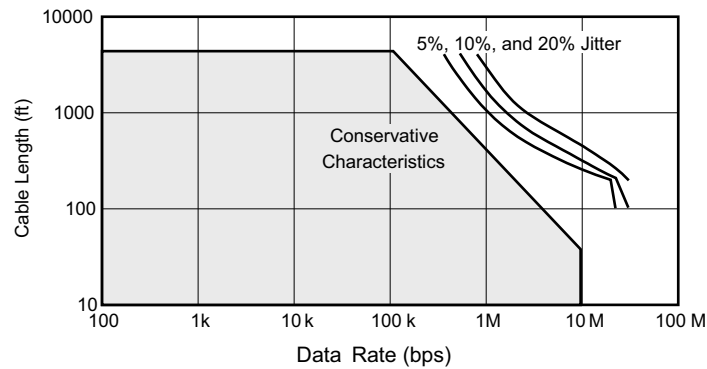


図 9-2. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 20Mbps for the THVD2429) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(\text{STUB})} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the THVD24x9 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.2 Detailed Design Procedure

RS-485 transceivers operate in noisy industrial environments typically require surge protection at the bus pins. [Figure 9-3](#) compares the surge protection implementation with a regular RS-485 transceiver (a), against that with a surge-integrated RS-485 transceiver (b), such as the THVD24x9 family. The internal TVS protection of the THVD24x9 achieves up to $\pm 3\text{kV}$ IEC 61000-4-5 surge protection (SOIC package) without any additional external components, reducing system level bill of materials.

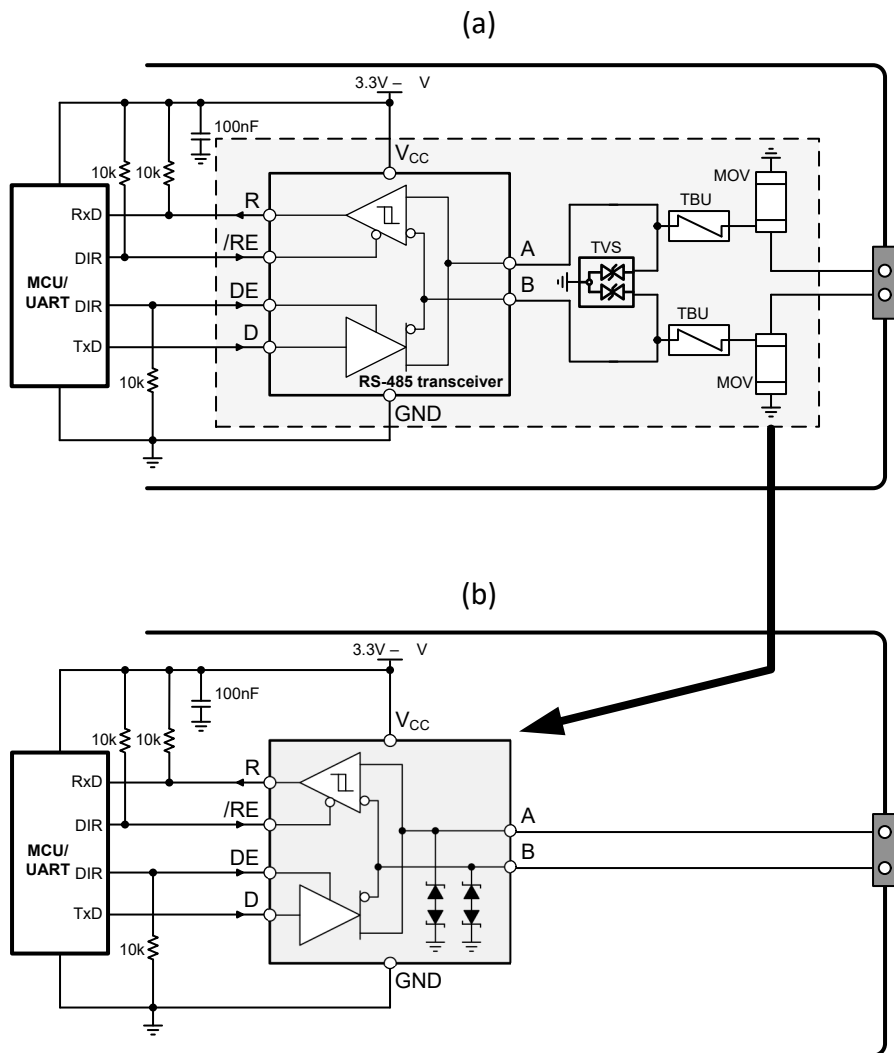
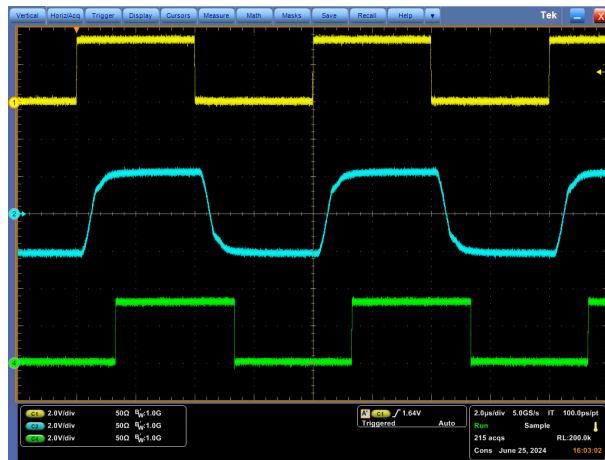


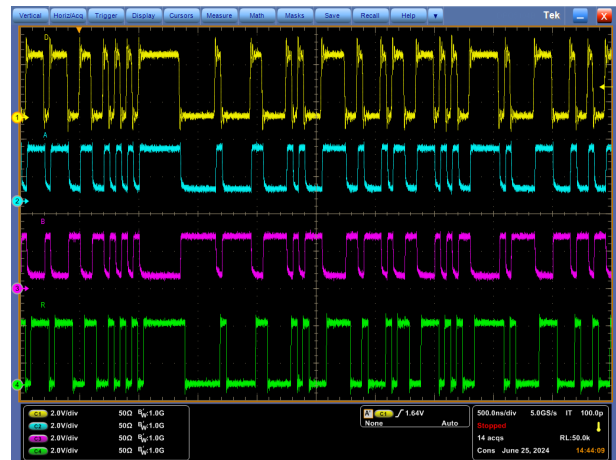
図 9-3. Implementation of System-Level Surge Protection Using THVD24x9

9.2.3 Application Curves



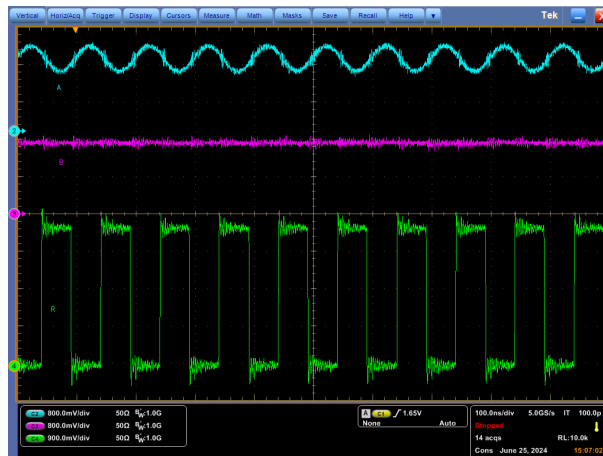
Ch 1: D Input, Ch2: V_A Ch3: V_B Ch4: R $V_{CC} = 3.3V$
Output Data rate: 20Mbps

図 9-4. THVD2419 Waveforms with 54Ω Termination and $V_{CC} = 3.3V$



Ch 1: D Input, Ch2: V_A Ch3: V_B Ch4: R $V_{CC} = 3.3V$
Output Data rate: 20Mbps

図 9-5. THVD2429 Waveforms with 54Ω Termination and $V_{CC} = 3.3V$



Ch 2: Input A ($\pm 200mV$ sine input over 1.5V DC offset)

Ch3: Input B (1.5V)

Ch 4: Output R

図 9-6. THVD2429 Receiver Waveform with $\pm 200mV V_{ID}$

9.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout Guidelines

Additional external protection components generally are not needed when using THVD24x9 transceivers.

1. Use V_{CC}/V_{IO} and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance. Apply 100nF to 220nF decoupling capacitors as close as possible to the V_{CC}/V_{IO} pins of transceiver, UART and/or controller ICs on the board.
2. Use at least two vias for V_{CC}/V_{IO} and ground connections of decoupling capacitors to minimize effective via inductance.
3. Use 1k Ω to 10k Ω pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.

9.4.2 Layout Example

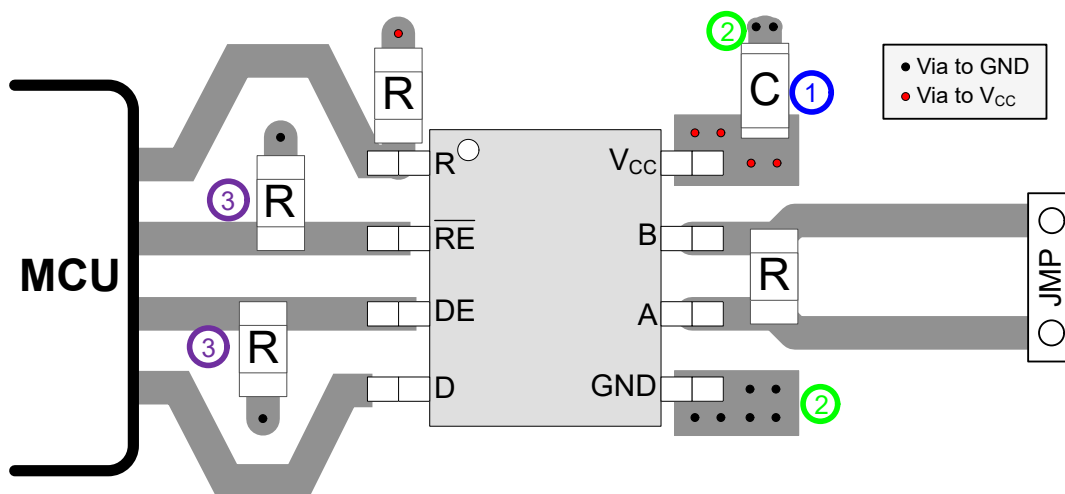


図 9-7. THVD2419, THVD2429 Layout Example (SOIC Package)

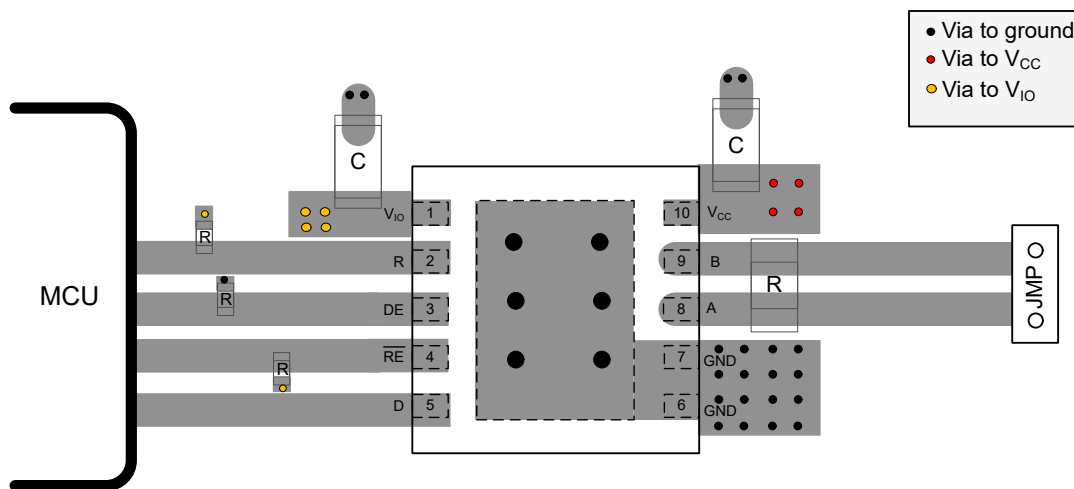


図 9-8. THVD2419, THVD2429 Layout Example (VSON Package)

10 Device and Documentation Support

10.1 Device Support

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2024) to Revision A (August 2024)

Page

- | | |
|---|---|
| • ドキュメントのステータスを「事前情報」から「量産データ」に変更 | 1 |
|---|---|

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD2419DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV2419 D2419
THVD2419DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV2419 D2419
THVD2419DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
THVD2419DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T2419
THVD2419DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T2419
THVD2419DRCR.B	Active	Production	VSON (DRC) 10	5000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
THVD2429DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV2429 D2429
THVD2429DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV2429 D2429
THVD2429DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
THVD2429DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T2429
THVD2429DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T2429
THVD2429DRCR.B	Active	Production	VSON (DRC) 10	5000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

Technical drawing showing the front and side views of a mechanical part, likely a bracket or support structure. The drawing includes dimensions and symmetry indicators.

Front View (Left):

- Top horizontal dimension: $8X (.061)$ [1.55]
- Vertical dimension from top to first hole center: 1
- Vertical dimension between first and second hole centers: $8X (.024)$ [0.6]
- Vertical dimension between second and third hole centers: 4
- Bottom horizontal dimension: $6X (.050)$ [1.27]

Side View (Right):

- Top horizontal dimension: $(.213)$ [5.4]
- Vertical dimension from top to first hole center: 8
- Vertical dimension between first and second hole centers: 5
- Bottom horizontal dimension: $(R.002)$ TYP [0.05]

Symmetry and Detail Callouts:

- Two vertical centerlines labeled "SYMM" indicate symmetry about the vertical axis.
- A horizontal centerline labeled "SYMM" indicates symmetry about the horizontal axis.
- An arrow points to the top right corner with the text "SEE DETAILS".

4214825/C 02/2019

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

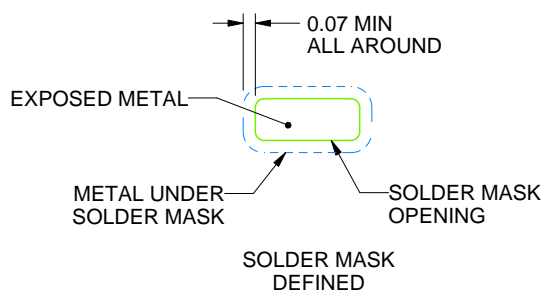
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月