THVD2410, THVD2450
JAJSHN2B – JULY 2019 – REVISED OCTOBER 2021

THVD24x0 IEC ESD 対応、±70V フォルト保護機能搭載、3.3V～5V RS-485 トランシーバ

1 特長

- TIA/EIA-485A および TIA/EIA-422B 規格の要件に適合またはそれを上回る性能
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 電源電圧：3V～5.5V
- 5V 電源で 2.1V を超える差動出力により PROFIBUS に準拠
- バス I/O 保護
  - ±70V DC バス・フォルト
  - ±16kV HBM ESD
  - ±12kV IEC 61000-4-2 接触放電
  - ±12kV IEC 61000-4-2 エアギャップ放電
  - ±4kV IEC 61000-4-4 高速過渡バースト
- 2 つの速度グレードに対応する半二重デバイス
  - THVD2410：500kbps
  - THVD2450：50Mbps
- 広い周囲温度範囲：
  -40℃～125℃
- 広い動作同相範囲：
  ±25V
- レシーバのヒステリシスを大きくすることでノイズ耐性を確保
- 低い消費電力
  - 低いシャットダウン時消費電流：1µA 未満
  - 動作時電流：5.6mA 未満
- グリッチなしの電源オン / オフによる活線挿抜機能
- 開放、短絡、アイドル・バスのフェイルセーフ
- サーマル・シャットダウン
- 1/8 単位負荷 (最大 256 のバス・ノード)
- 基板面積を削減できる小型 VSON および VSSOP パッケージ、またはドロップイン互換の SOIC パッケージ

2 アプリケーション

- モーター・ドライブ
- ファクトリ・オートメーション / 制御
- HVAC システム
- ビル・オートメーション
- グリッド・インフラストラクチャ
- 電気メーター
- プロセス分析
- ビデオ監視

3 概要

THVD2410 および THVD2450 は、±70V のフォルト保護機能を備えた半二重 RS-422/RS-485 トランシーバであり、3V～5.5V の単一電源で動作します。バス・インターフェイス・ピンは全動作モードで過電圧条件から保護されるため、厳しい産業環境でも堅牢な通信を確立できます。

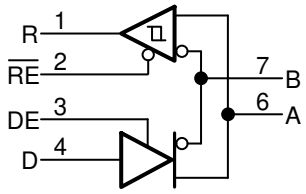
IEC ESD 保護機能を内蔵しているため、システムレベルの外部保護部品は不要です。入力同相範囲が ±25V と広いため、長いケーブルを使用する場合やグランド・ループ電圧が大きい場合でも信頼性の高いデータ通信を確保できます。250mV の大きなレシーバ・ヒステリシスにより、高いノイズ除去性能を実現します。また、レシーバのフェイルセーフ機能により、入力が開放または短絡した場合、出力が確実に論理 HIGH に固定されます。

THVD24x0 は、スペースに制約がある用途向けに、小型の VSSOP および VSON パッケージで供給されます。このデバイスは、–40℃～125℃の周囲自由通気温度範囲で仕様が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
THVD2410 THVD2450	VSON (8)	3.00mm × 3.00mm
	VSSOP (8)	3.00mm × 3.00mm
	SOIC (8)	4.90mm × 3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



THVD2410 および THVD2450 の概略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

Changes from Revision A (October 2019) to Revision B (October 2021) **Page**

- 「*特長*」に「機能安全対応」を追加 ... 1

Changes from Revision * (July 2019) to Revision A (October 2019) **Page**

- アプリケーションを削除地震実験装置 ... 1
- 「製品情報」表の THVD2410 から製品プレビューの注を削除 ... 1

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5 Pin Configuration and Functions

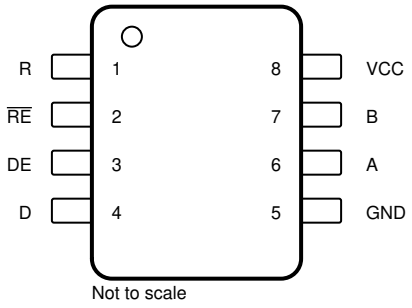


図 5-1. D (SOIC) and DGK (VSSOP), 8-Pin Packages, Top View

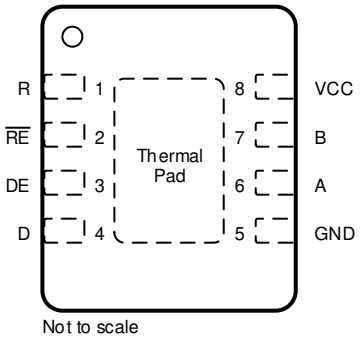


図 5-2. DRB (VSON), 8-Pin Package, Top View

表 5-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	D	DGK	DRB		
A	6	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	4	4	Digital input	Driver data input
DE	3	3	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	5	5	5	Ground	Device ground
R	1	1	1	Digital output	Receive data output
V_{CC}	8	8	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	2	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)
Thermal Pad	—	—	—	—	No electrical connection. Should be connected to GND plane for optimal thermal performance

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	7	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	–70	70	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$)	–0.3	5.7	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	170	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±8,000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±12,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±12,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

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6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–25		25	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2			V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)				0.8	V
V_{ID}	Differential input voltage		–25		25	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	THVD2410			500	kbps
		THVD2450			50	Mbps
T_A	Operating ambient temperature		-40		125	°C
T_J	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.5 Thermal Information

THERMAL METRIC(1)		THVD2410 THVD2450 D (SOIC) 8 PINS	THVD2410 THVD2450 DGK (VSSOP) 8 PINS	THVD2410 THVD2450 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.9	164.0	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.1	49.5	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.1	85.5	20.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.1	5.1	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.2	83.7	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Dissipation

PARAMETER		TEST CONDITIONS			VALUE	UNIT
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, random data (PRBS7) at signaling rate	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	THVD2410	500 kbps	130	mW
			THVD2450	50 Mbps	340	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	THVD2410	500 kbps	170	mW
			THVD2450	50 Mbps	340	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	THVD2410	500 kbps	240	mW
			THVD2450	50 Mbps	370	

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6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, –25 V ≤ V_{test} ≤ 25 V (See 図 7-1)			1.5	3.3		V
		R_L = 60 Ω, –25 V ≤ V_{test} ≤ 25 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See 図 7-1)			2.1	3.3		V
		R_L = 100 Ω (See 図 7-2)			2	4		V
		R_L = 54 Ω (See 図 7-2)			1.5	3.3		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω or 100 Ω (See 図 7-2)			–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See 図 7-2)			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See 図 7-2)			–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -70 V ≤ (V_A or V_B) ≤ 70 V			–250		250	mA
Receiver								
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	125	μA
				V_I = 25 V		150	250	
				V_I = –7 V	–100	–40		
				V_I = –25 V	–250	–150		
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of ± 25 V			40	125	200	mV
V_{TH-}	Negative-going input threshold voltage(1)				–200	–125	-40	mV
V_{HYS}	Input hysteresis					250		mV
V_{TH_FSH}	Input fail-safe threshold				–40		40	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz				50		pF
V_{OH}	Output high voltage	I_{OH} = –8 mA			V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA				0.2	0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	μA
Logic								
I_{IN}	Input current (DE)	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}					5	μA
I_{IN}	Input current (D, $\overline{RE}$)	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}			–5			μA
Thermal Protection								
T_{SHDN}	Thermal shutdown threshold	Temperature rising			150	170		°C
T_{HYS}	Thermal shutdown hysteresis					10		°C
Supply								
I_{CC}	Supply current (quiescent)	Driver and receiver enabled		$\overline{RE}$ = 0 V, DE = V_{CC}, No load		3.5	5.6	mA
		Driver enabled, receiver disabled		$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2.5	4.4	mA
		Driver disabled, receiver enabled		$\overline{RE}$ = 0 V, DE = 0 V, No load		1.8	2.4	mA
		Driver and receiver disabled		$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1	μA

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.

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6.8 Switching Characteristics: THVD2410

500-kbps device (THVD2410) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See 図 7-3	240	280	600	ns
t_{PHL}, t_{PLH}	Propagation delay				275	350	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					10	ns
t_{PHZ}, t_{PLZ}	Disable time		See 図 7-4 and 図 7-5		45	95	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			175	270	ns
		$\overline{RE}$ = V_{CC}			1.5	4	µs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{CC}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 図 7-6		13	20	ns
t_{PHL}, t_{PLH}	Propagation delay				50	80	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					7	ns
t_{PHZ}, t_{PLZ}	Disable time				30	40	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = V_{CC}	See 図 7-7		90	120	ns
		DE = 0 V	See 図 7-8		2	4	µs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 図 7-9	7	10	18	µs
$t_{D(FSO)}$	Delay to exit fail-safe operation			35	45	60	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 図 7-8	50		500	ns

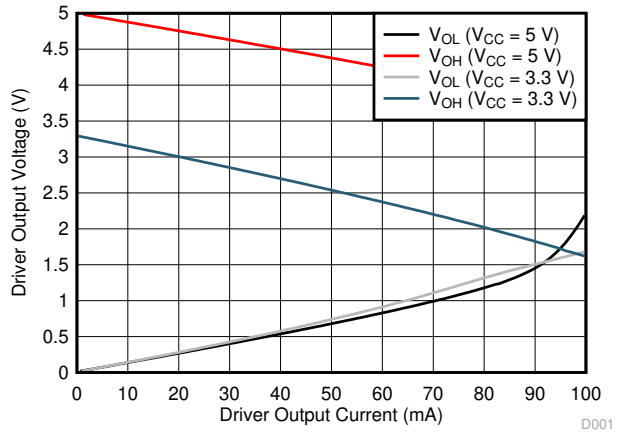
6.9 Switching Characteristics: THVD2450

50-Mbps device (THVD2450) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See 図 7-3		5	7	ns
t_{PHL}, t_{PLH}	Propagation delay			5	10	16	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					3.5	ns
t_{PHZ}, t_{PLZ}	Disable time		See 図 7-4 and 図 7-5		11	30	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			8	25	ns
		$\overline{RE}$ = V_{CC}			1.5	4	µs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{CC}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 図 7-6		2	6	ns
t_{PHL}, t_{PLH}	Propagation delay				40	55	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					4	ns
t_{PHZ}, t_{PLZ}	Disable time				7	15	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = V_{CC}	See 図 7-7		50	70	ns
		DE = 0 V	See 図 7-8		2	4	µs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 図 7-9	7	10	18	µs
$t_{D(FSO)}$	Delay to exit fail-safe operation			25	35	50	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 図 7-8	50		500	ns

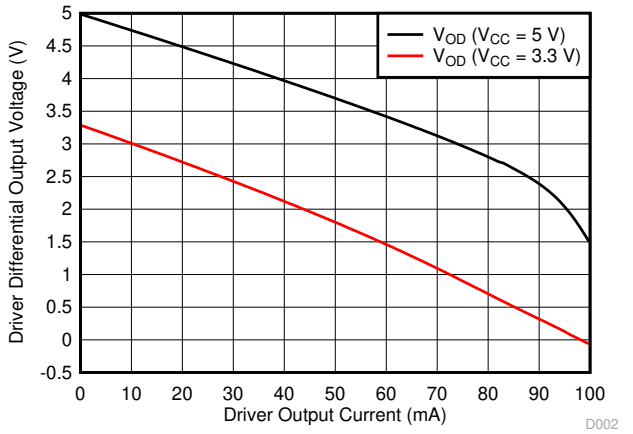
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6.10 Typical Characteristics



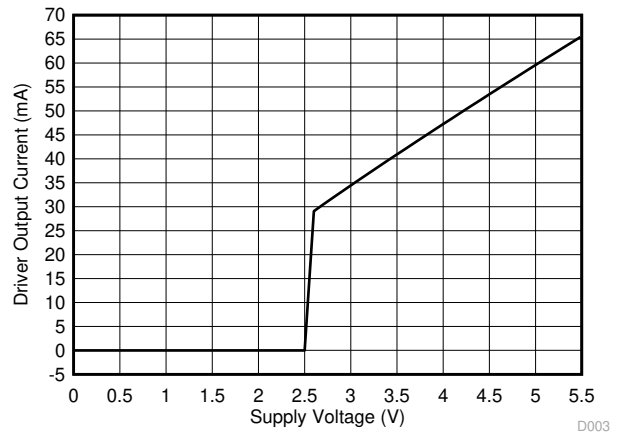
DE = V_{CC} D = 0 V T_A = 25 °C

図 6-1. Driver Output Voltage vs Driver Output Current



DE = V_{CC} D = 0 V T_A = 25 °C

図 6-2. Driver Differential Output voltage vs Driver Output Current



T_A = 25 °C DE = D = V_{CC} R_L = 54 Ω

図 6-3. Driver Output Current vs Supply Voltage

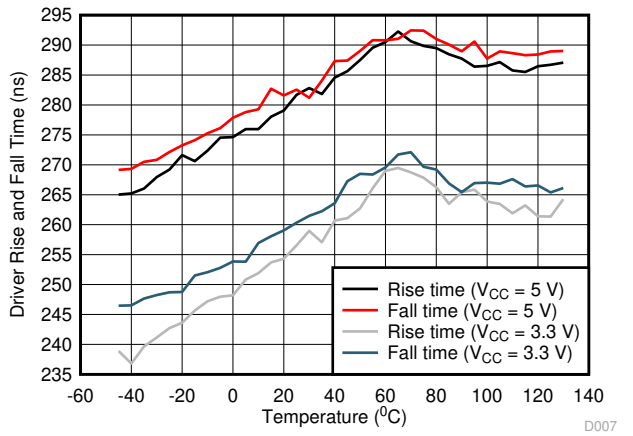


図 6-4. THVD2410 Driver Rise or Fall Time vs Temperature

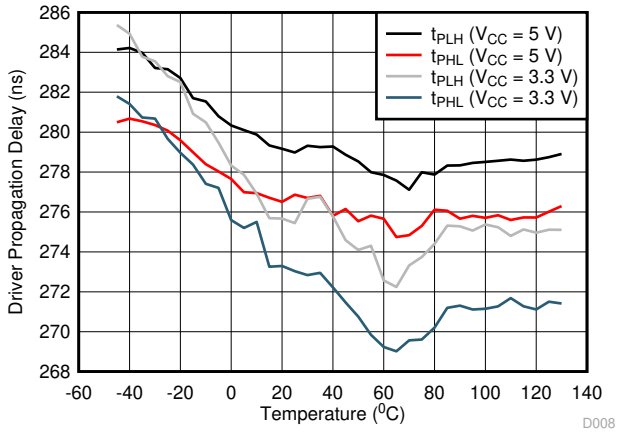
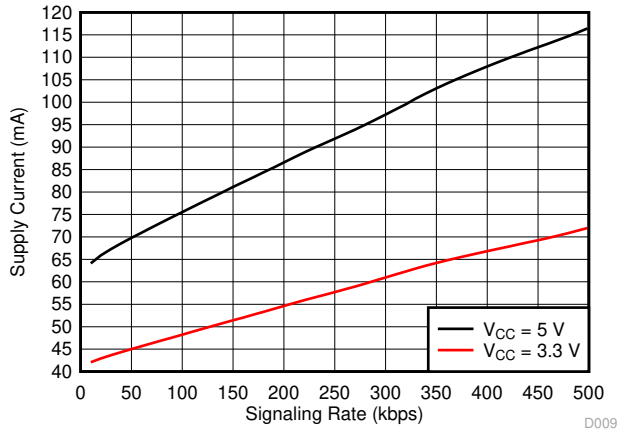


図 6-5. THVD2410 Driver Propagation Delay vs Temperature



T_A = 25 °C R_L = 54 Ω

図 6-6. THVD2410 Supply Current vs Signal Rate

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6.10 Typical Characteristics (continued)

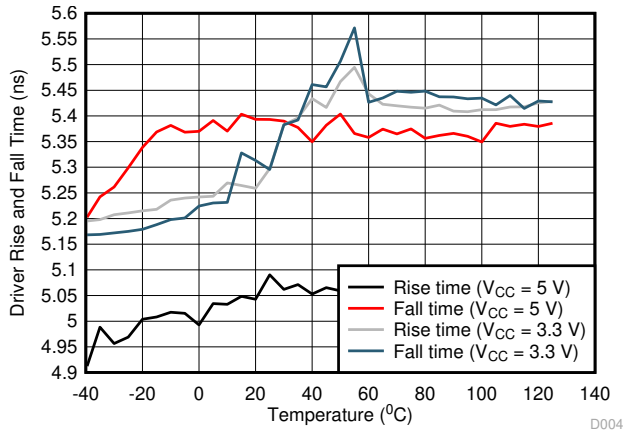


図 6-7. THVD2450 Driver Rise or Fall Time vs Temperature

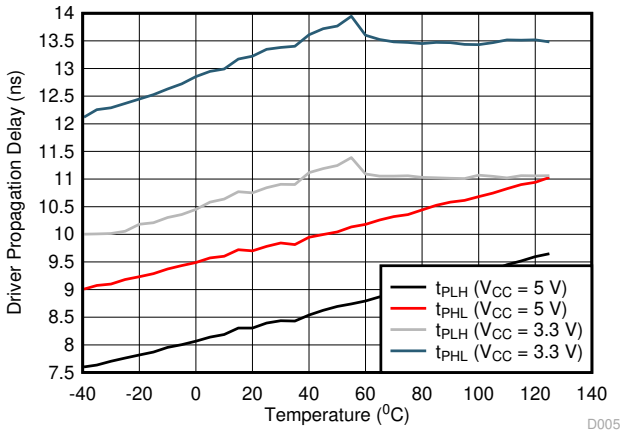
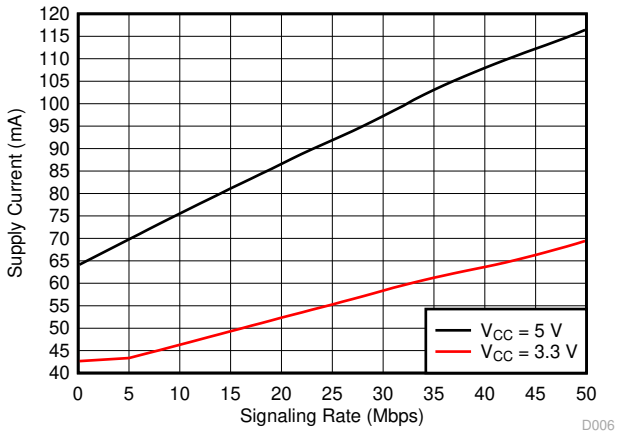


図 6-8. THVD2450 Driver Propagation Delay vs Temperature



T_A = 25 °C R_L = 54 Ω

図 6-9. THVD2450 Supply Current vs Signal Rate

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7 Parameter Measurement Information

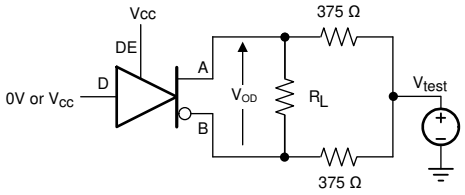


図 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

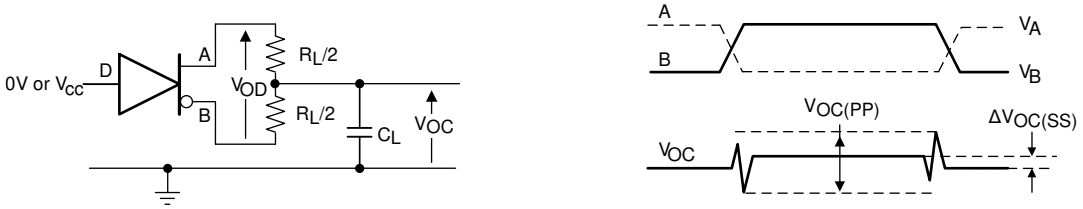


図 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

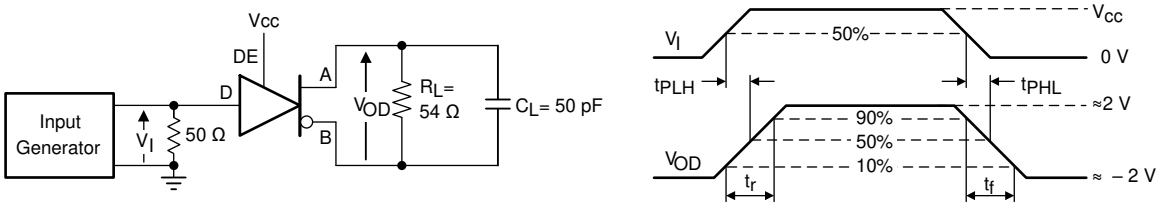
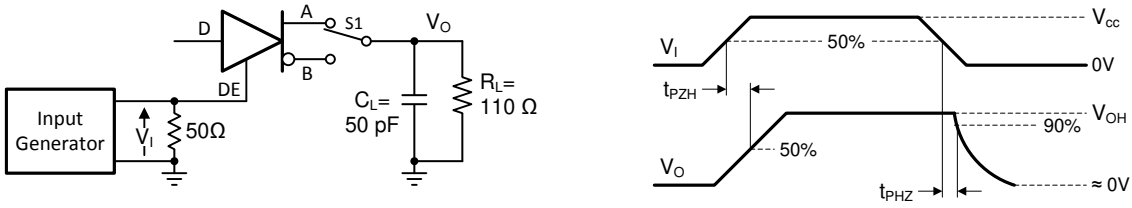
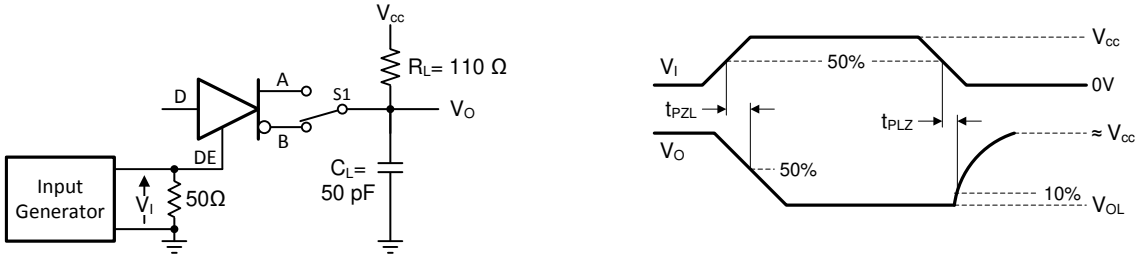


図 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



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図 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load



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図 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

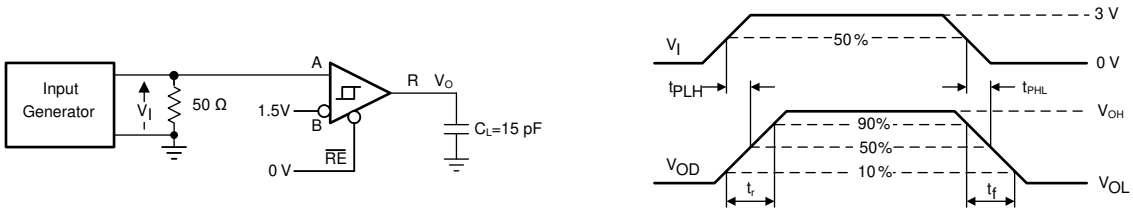


図 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

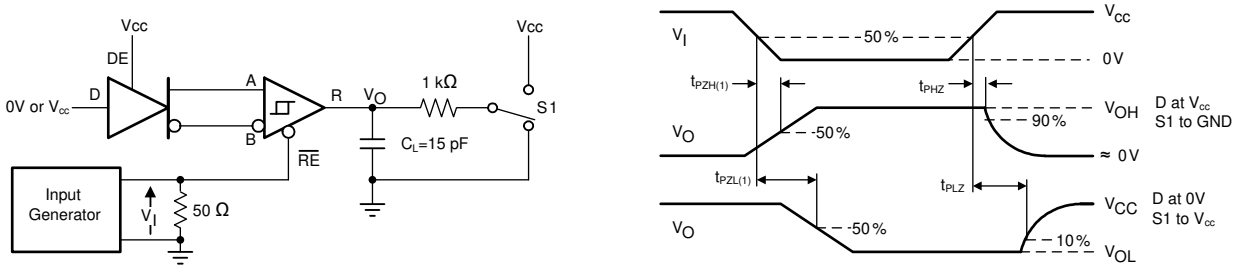
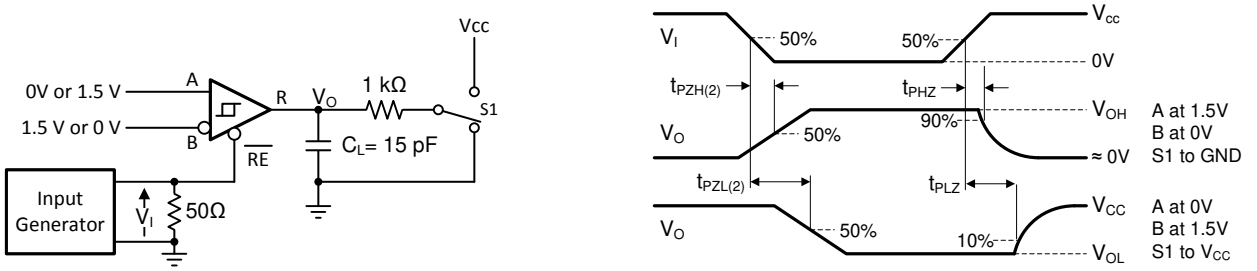
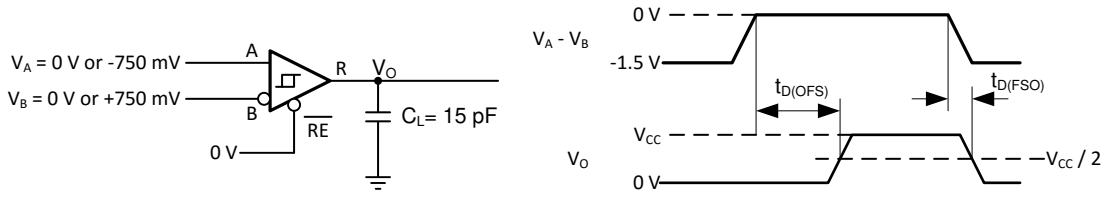


図 7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled



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図 7-8. Measurement of Receiver Enable Times With Driver Disabled



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図 7-9. Measurement of Fail-Safe Delay

8 Detailed Description

8.1 Overview

THVD2410 and THVD2450 are fault-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 500 kbps and 50 Mbps respectively. The devices have active-high driver enables and active-low receiver enables. A shutdown current of less than 1 µA can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagrams

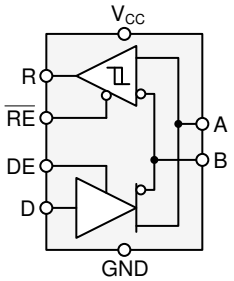


図 8-1. THVD2410 and THVD2450 Block Diagram

8.3 Feature Description

8.3.1 ±70-V Fault Protection

THVD24x0 transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7 V to +12 V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, THVD24x0 devices are protected up to ±70 V without the need for any external components.

8.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. THVD24x0 ESD structures help to limit voltage excursions and recover from them quickly that they allow EFT Criterion A at the system level (no data loss when transient noise is present).

8.3.3 Driver Overvoltage and Overcurrent Protection

The THVD24x0 drivers are protected against any DC supply shorts in the range of -70 V to +70 V. The devices internally limit the short circuit current to ±250 mA in order to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ±5 mA if the output fault voltage exceeds |±25 V|.

All devices feature thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

8.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24x0 feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) hysteresis ensures excellent noise immunity.

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8.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH_FSH}|$.

8.3.6 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500 ns puts the devices into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50 ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

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When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), or he bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

THVD2410 and THVD2450 are fault-protected, half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

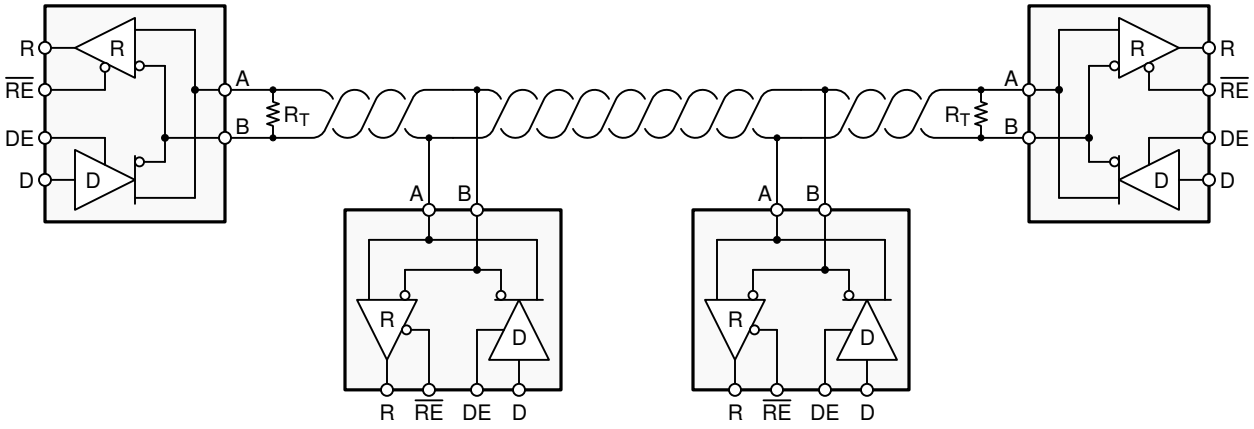


図 9-1. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

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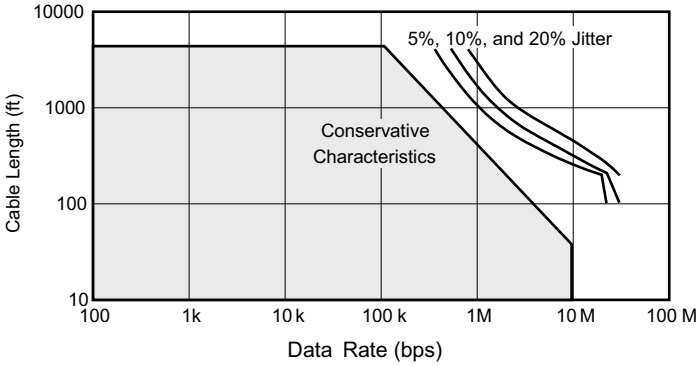


図 9-2. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD2450) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD24x0 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

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9.2.1.4 Transient Protection

The bus pins of the THVD24x0 transceivers include on-chip ESD protection against ±30-kV HBM and ±12-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

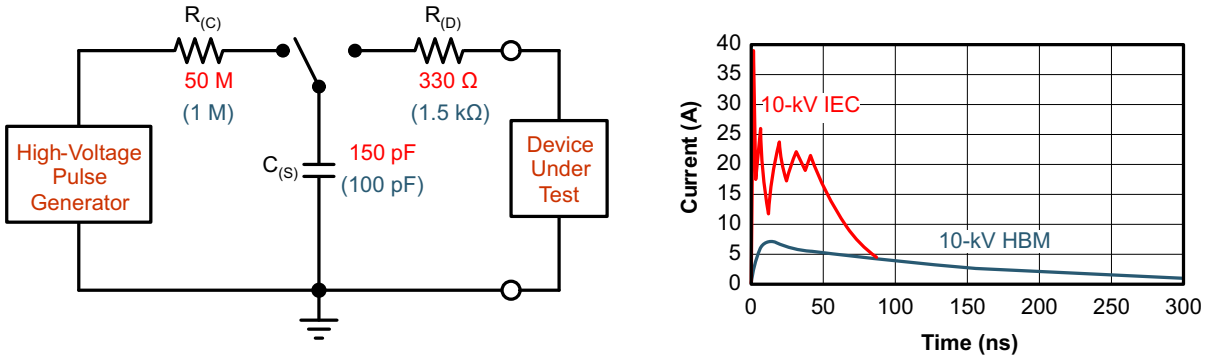


図 9-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

図 9-4 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

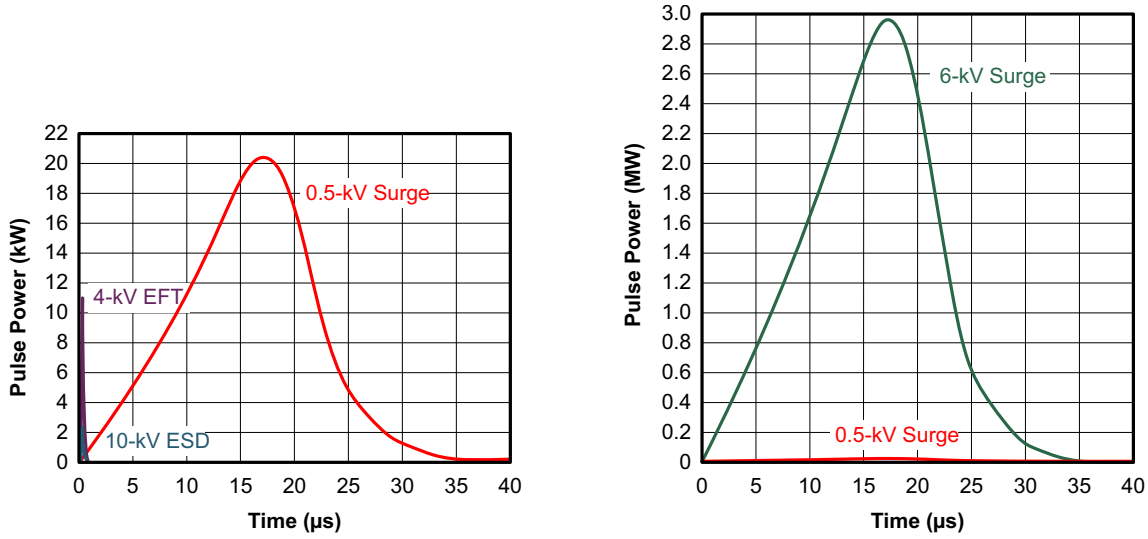


図 9-4. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 図 9-5 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

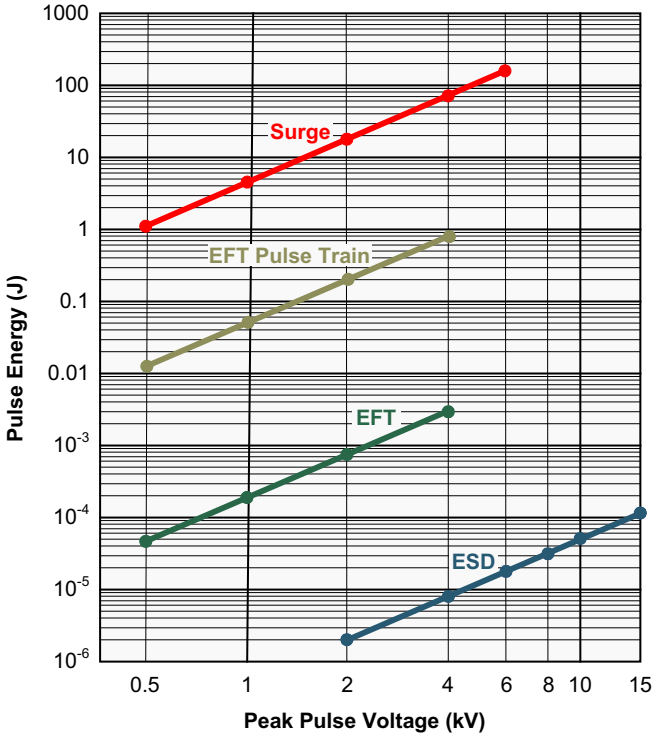


図 9-5. Comparison of Transient Energies

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9.2.2 Detailed Design Procedure

図 9-6 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 9-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30 V. This ensures the protection diodes do not conduct if a direct RS-485 bus shorts to 24-V DC industrial power rail.

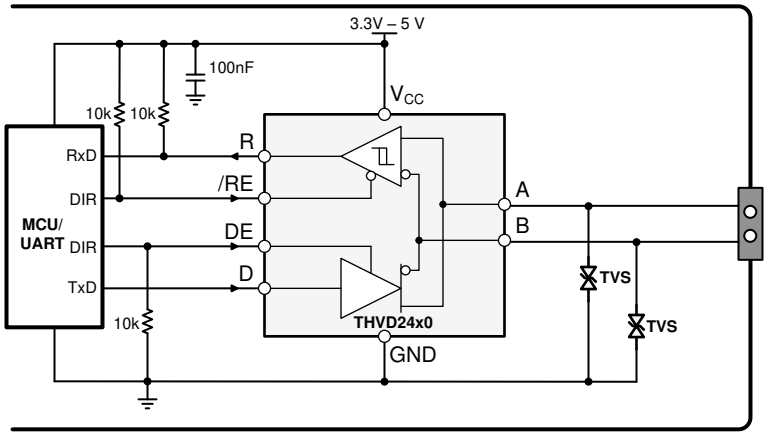


図 9-6. Transient Protection Against Surge Transients for Half-Duplex Devices

表 9-1. Components List(1)

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD24x0	TI
TVS	Bidirectional 400-W transient suppressor	SMAJ30CA	Littelfuse

(1) See Device Support

9.2.3 Application Curves



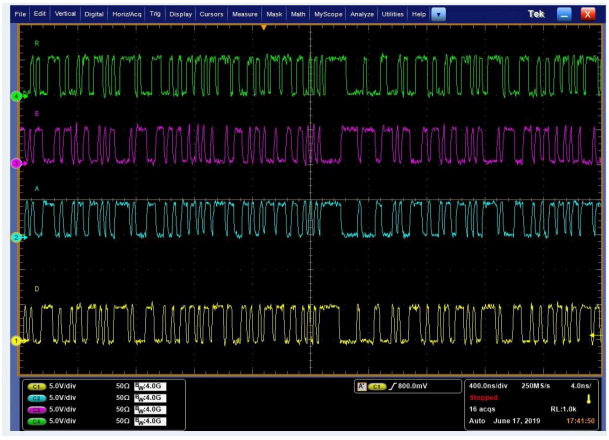
THVD2410 V_{CC} = 5 V R_L = 50 Ω
Random (PRBS7) data at 500 kbps

図 9-7. THVD2410 Waveforms at V_{CC} = 5 V



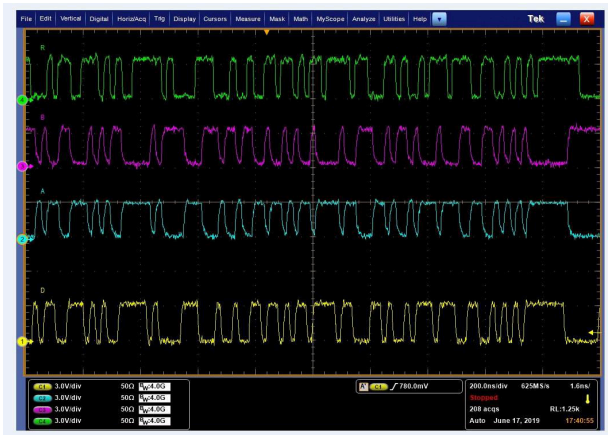
THVD2410 V_{CC} = 3.3 V R_L = 50 Ω
Random (PRBS7) data at 500 kbps

図 9-8. THVD2410 Waveforms at V_{CC} = 3.3 V



THVD2450 V_{CC} = 5 V R_L = 50 Ω
Random (PRBS7) data at 50 Mbps

図 9-9. THVD2450 Waveforms at V_{CC} = 5 V



THVD2450 V_{CC} = 3.3 V R_L = 50 Ω
Random (PRBS7) data at 50 Mbps

図 9-10. THVD2450 Waveforms at V_{CC} = 3.3 V

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

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11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

11.2 Layout Example

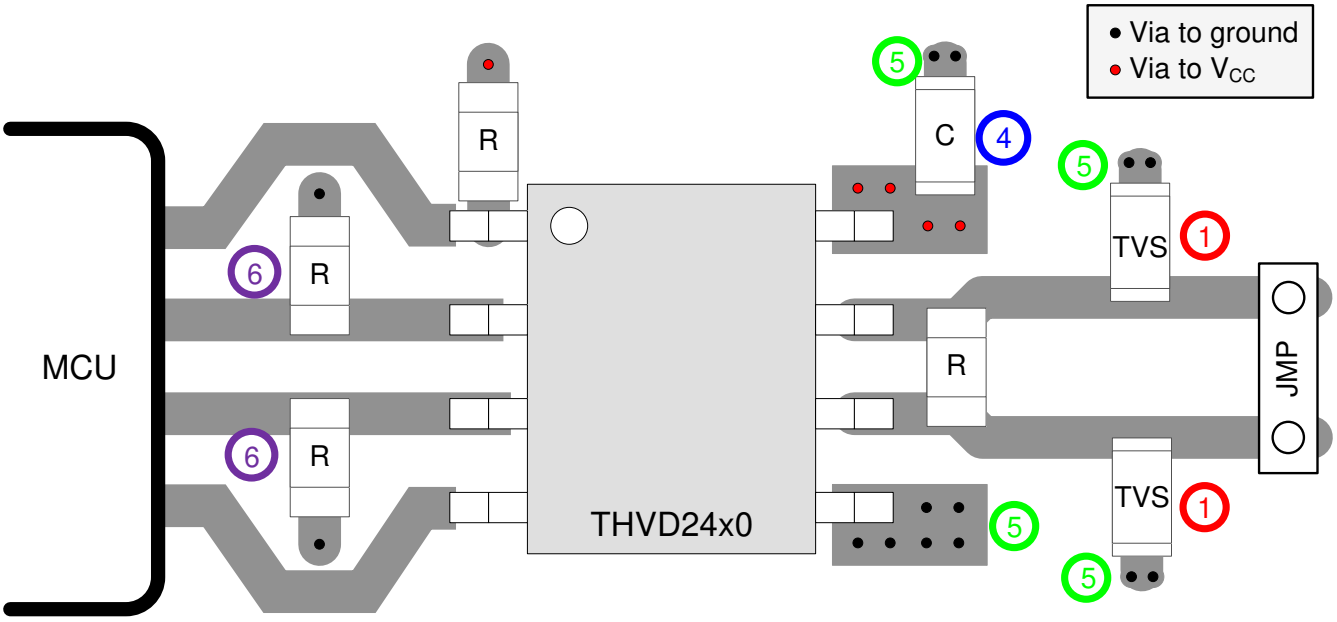


図 11-1. Half-Duplex Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD2410DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2410
THVD2410DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2410
THVD2410DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2410
THVD2410DGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2410
THVD2410DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2410DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2410DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2410DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2410DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2410DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2450DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DRBRG4.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

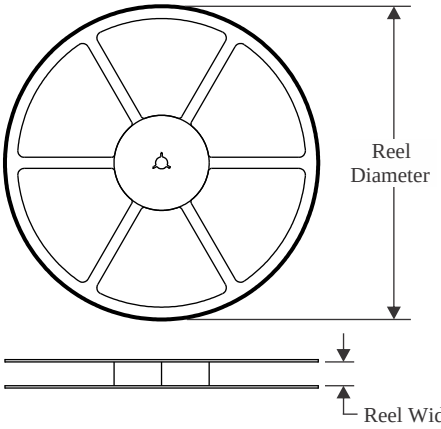
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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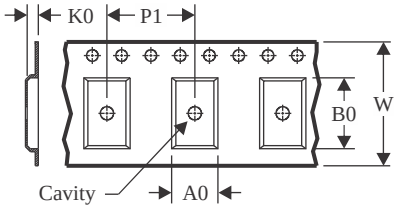
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

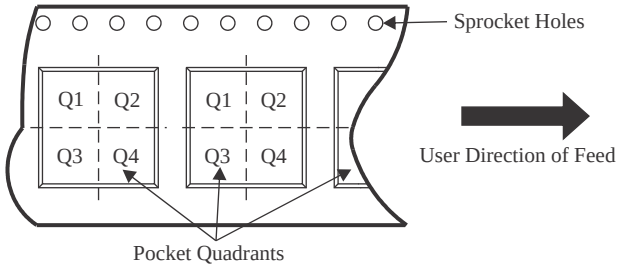


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

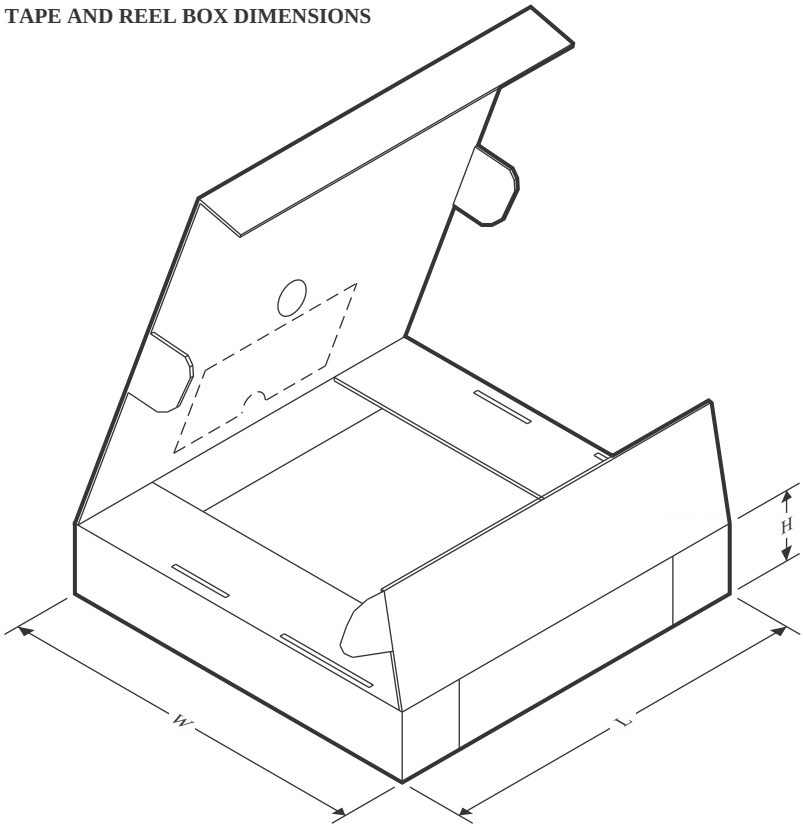
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD2410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD2410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD2410DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD2410DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD2410DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2410DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD2450DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD2450DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD2450DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD2450DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2450DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2450DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD2410DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THVD2410DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD2410DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD2410DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD2410DRBR	SON	DRB	8	3000	356.0	356.0	36.0
THVD2410DRG4	SOIC	D	8	2500	353.0	353.0	32.0
THVD2450DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD2450DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD2450DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD2450DRBR	SON	DRB	8	3000	356.0	356.0	36.0
THVD2450DRBRG4	SON	DRB	8	3000	367.0	367.0	35.0
THVD2450DRG4	SOIC	D	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

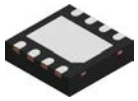
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

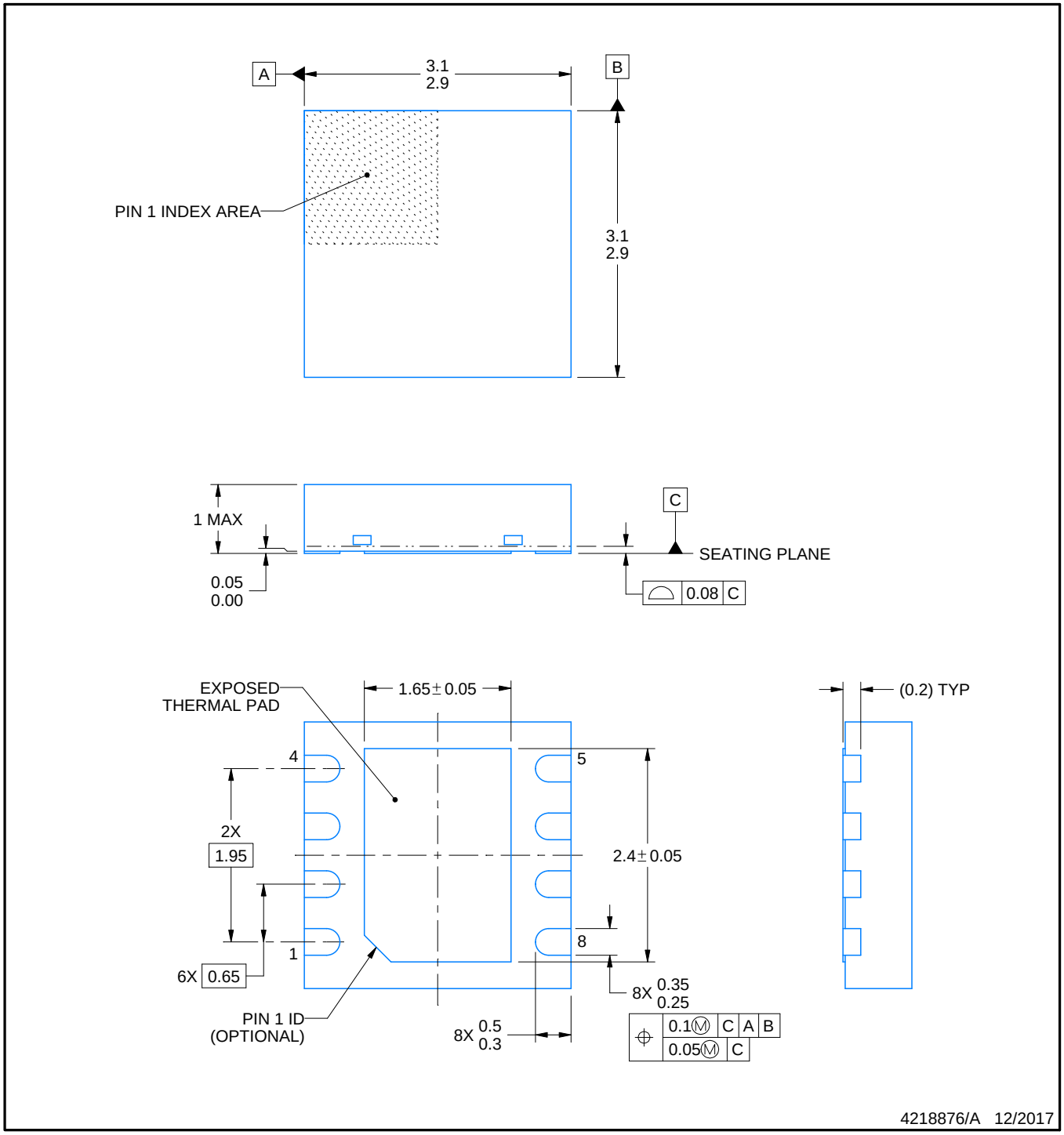
DRB0008B



PACKAGE OUTLINE

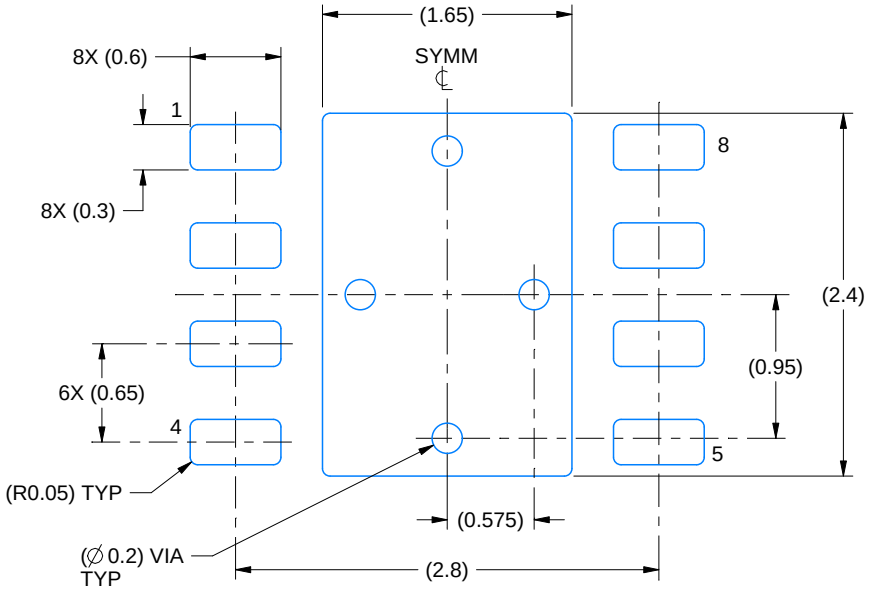
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

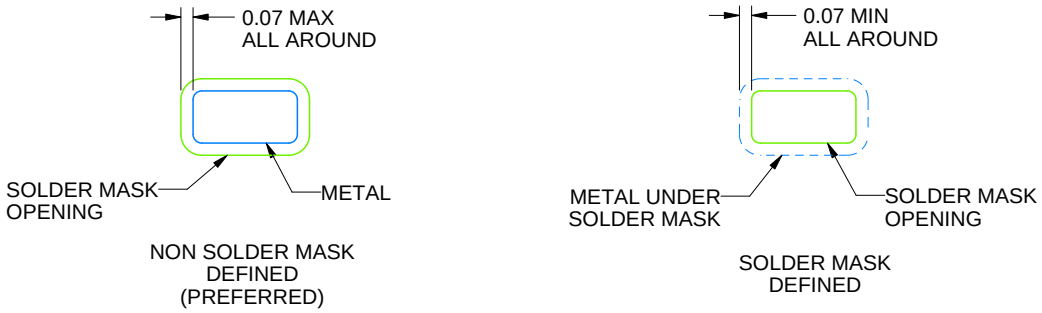


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

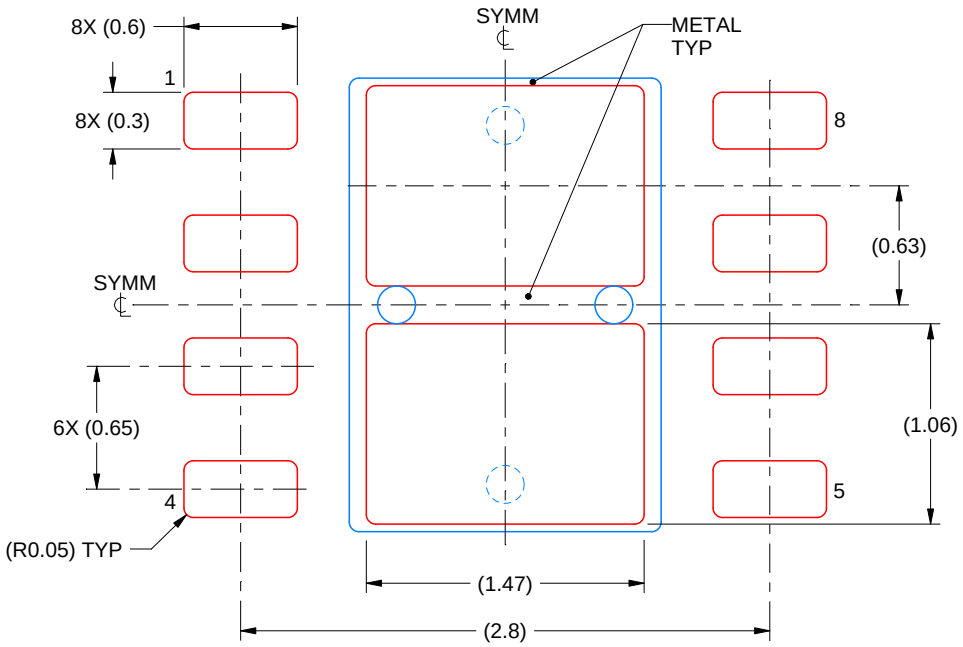


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



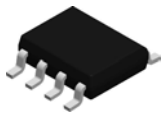
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

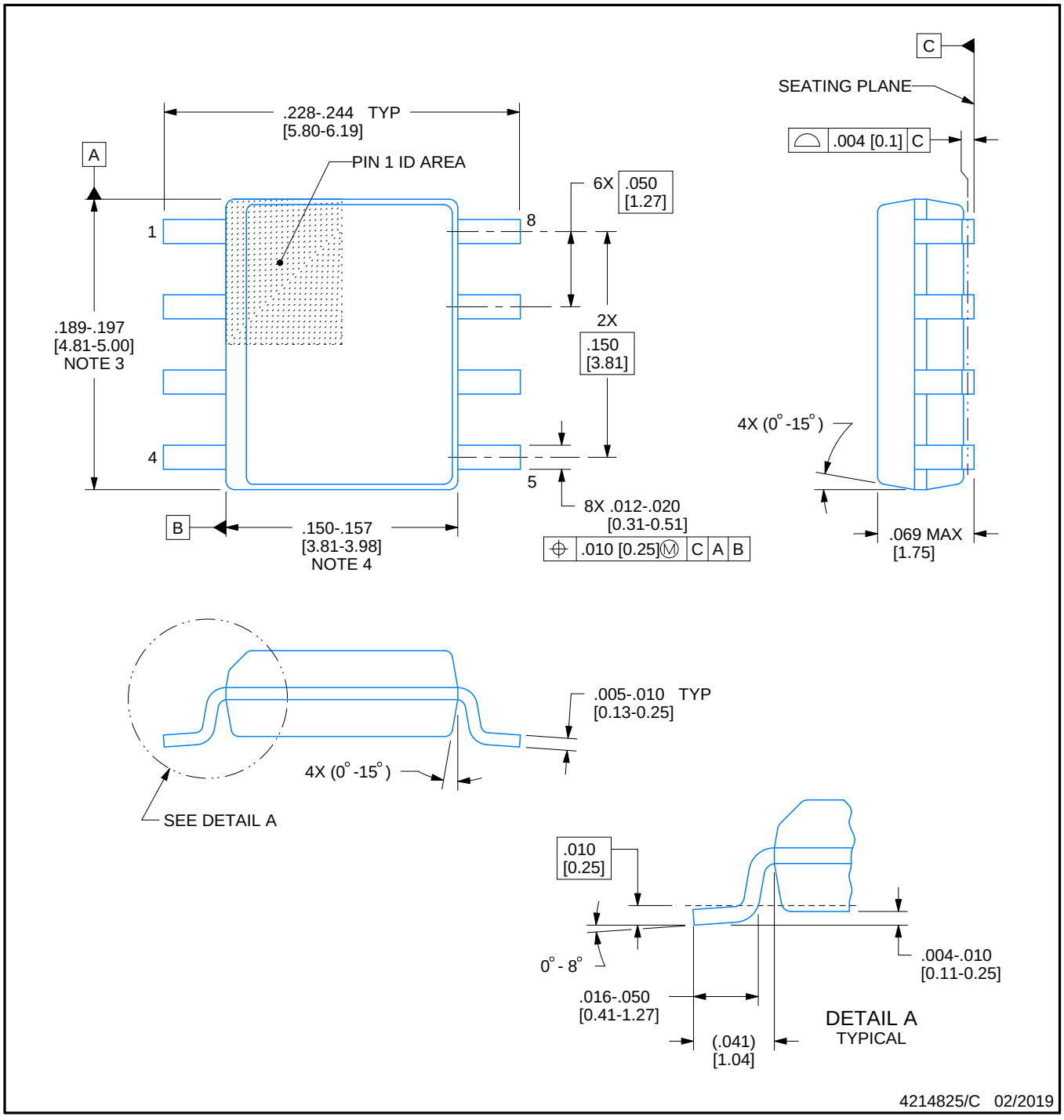


PACKAGE OUTLINE

D0008A

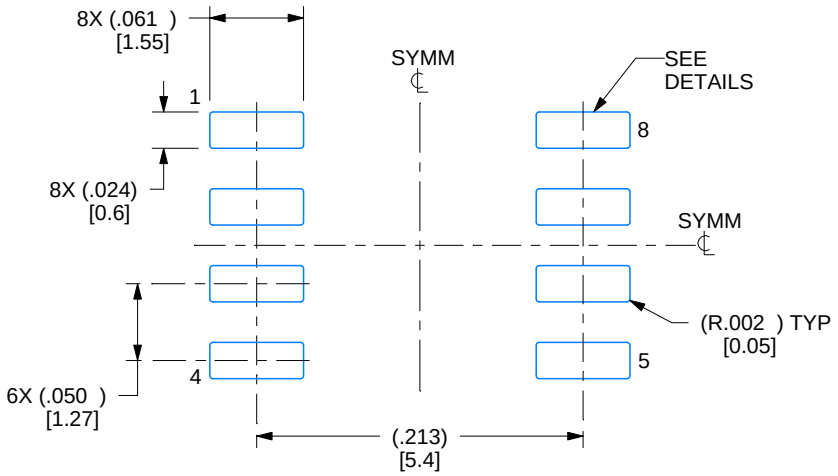
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

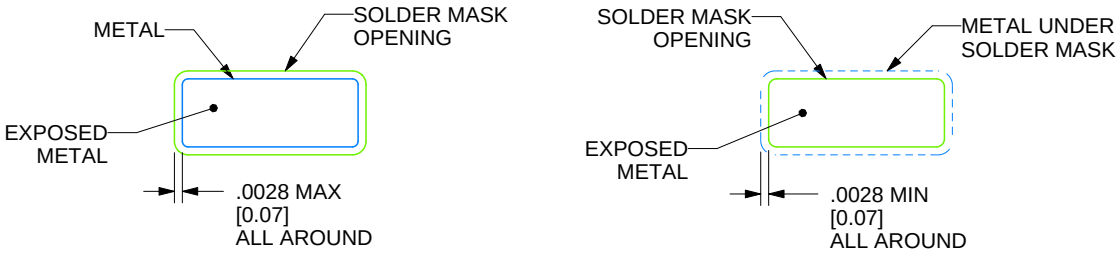


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

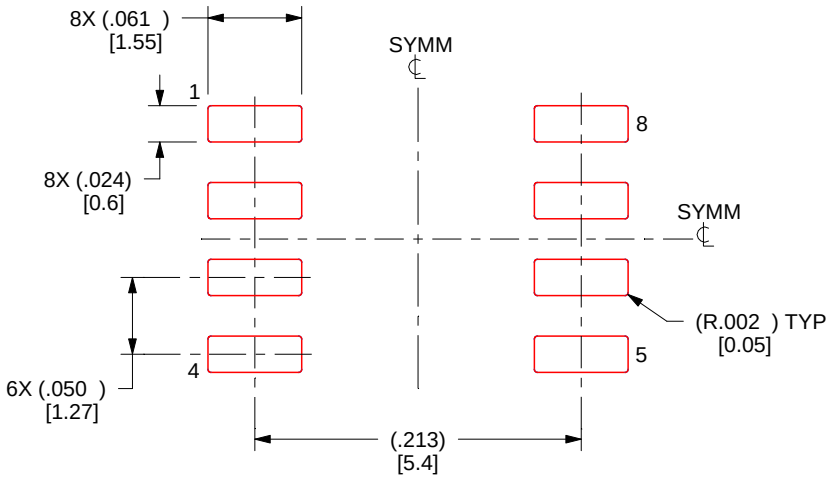
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

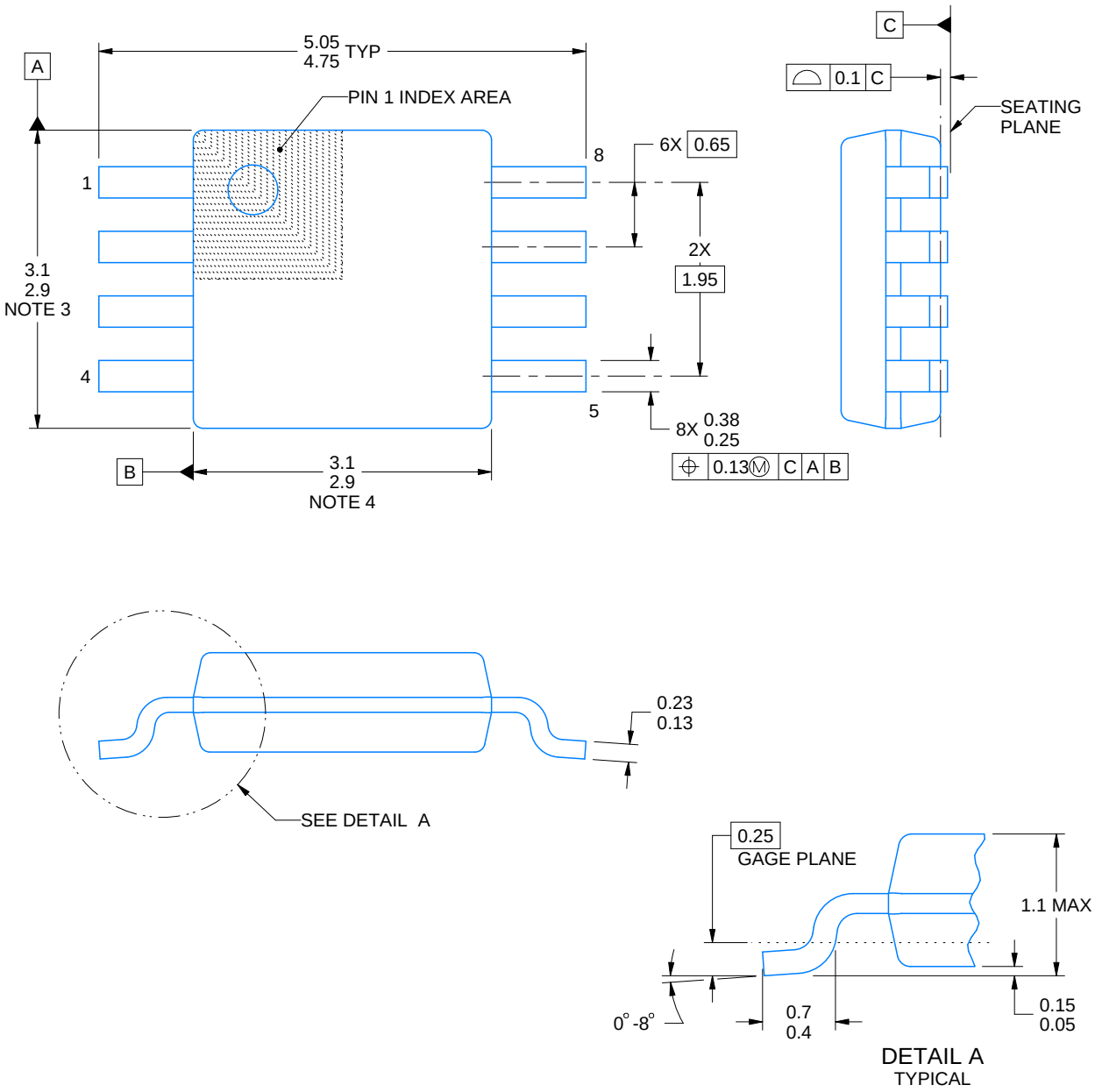
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

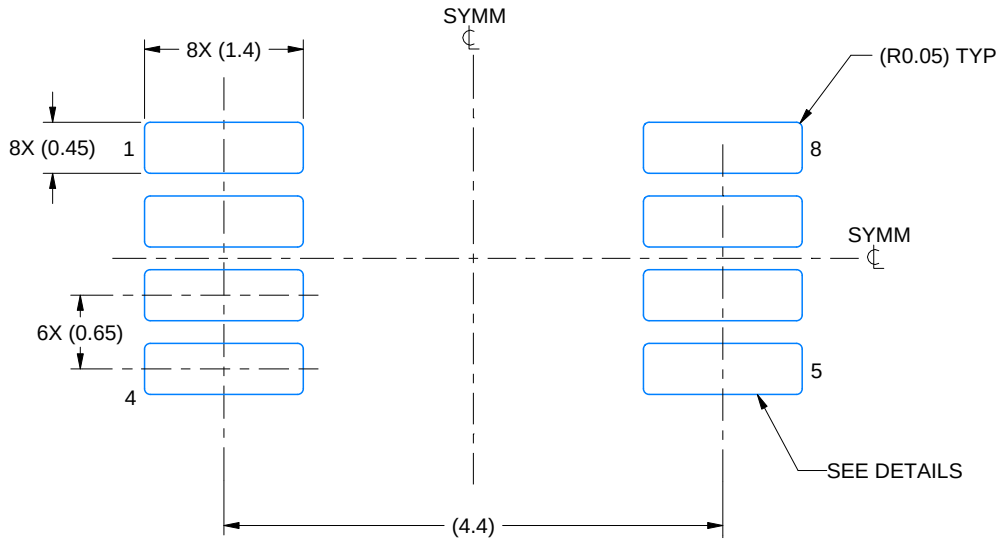
SMALL OUTLINE PACKAGE



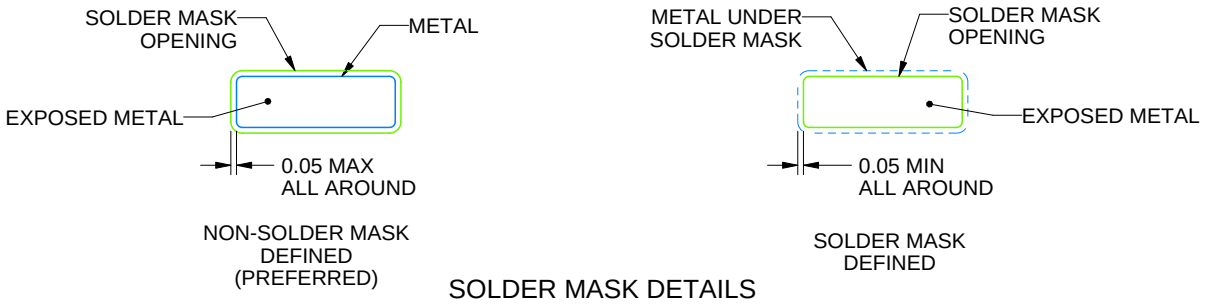
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

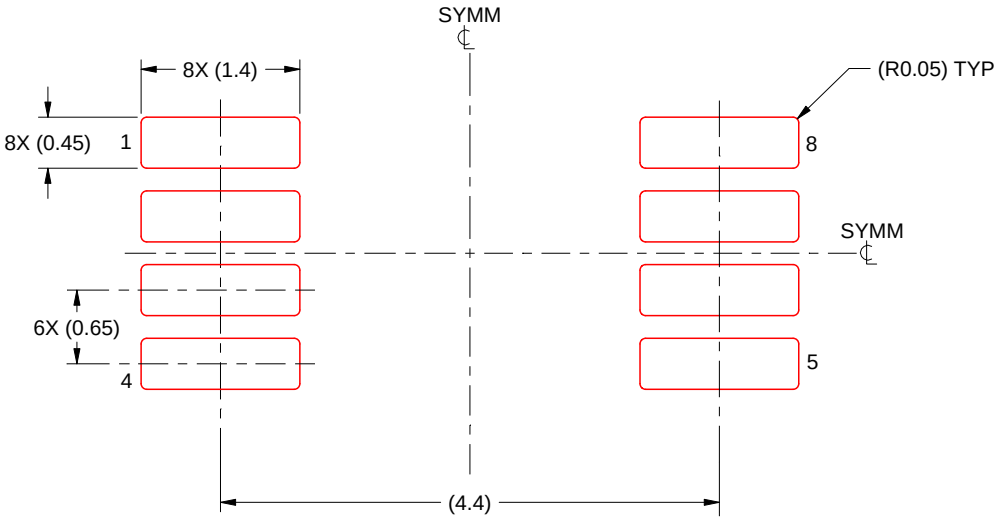


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月