TL28L92 3.3V～5V デュアル、ユニバーサル非同期レシーバ / トランスミッタ

1 特長

- 3.3V～5V、–40°～85°C および 68xxx または 80xxx バス インターフェイス
- デュアル、全二重、独立した非同期レシーバ / トランスミッタ、各レシーバおよびトランスミッタに 16 文字の FIFO
- ピン プログラミングにより 68xxx または 80xxx バス インターフェイスを選択
- プログラマブル データ フォーマット
  - 5 データ ビットから 8 データ ビット + パリティ
  - 奇数、偶数、パリティなし、または強制パリティ
  - 1 ストップ、1.5 ストップ、または 2 ストップ ビットを 1/16 ビット インクリメントでプログラム可能
- 16 ビットのプログラマブル カウンタおよびタイマ
- 各レシーバおよびトランスミッタは次の範囲でボーレートをプログラム可能:
  - 28 固定レート:50Bd～230.4kBd
  - その他のボーレートは 16 倍の 1MHz まで
  - プログラマブル カウンタとタイマから求めた、プログラマブルなユーザー定義のレート
  - 外部 1x または 16x クロック
- パリティ、フレーミング、オーバーラン エラー検出
- 不正スタート ビットの検出
- ライン ブレーク検出と生成
- プログラマブル チャネル モード
  - 通常 (全二重)
  - 自動エコー
  - ローカル ループバック
  - リモート ループバック
- マルチファンクション、7 ビット入力ポート (IACKN を含む)
  - クロック入力または制御入力として機能可能
  - 4 つの入力の状態変化を検出するには、通常は > 100kΩ のプルアップ抵抗を使用します
  - モデム制御用の状態変化検出器
- マルチファンクションの 8 ビット出力ポート
  - 個別のビット設定およびリセット機能
  - 出力をステータス信号および割り込み信号にプログラム可能
  - DMA インターフェイスの FIFO ステータス
- 汎用割り込みシステム
  - 8 つのマスク可能割り込み条件を持つ単一割り込み出力
  - 出力ポートは、OR 接続可能な合計 5 つまでの個別の割り込み出力を供給するように構成可能
  - 各 FIFO は、4 つの異なる割り込みレベルにプログラム可能
  - 各レシーバのウォッチドッグ タイマ
- 最大データ転送レート: 1× – 1Mbits, 16× – 1Mbit/s
- 開始 / 終了ブレーク割り込みおよびステータス
- キャラクタの途中で発生するブレークを検出
- オンチップの水晶発振器
- パワーダウン モード
- レシーバのタイムアウト モード
- 3.3V または 5V の単一電源電圧
- JEDEC 14C ESD の要件を満たす (または上回る) 性能

2 概要

TL28L92 は 3.3V または 5V 電源で動作し、追加機能とより深い FIFO を備えています。パワーアップ時の構成は、16 文字のレシーバ、16 文字の送信 FIFO、各レシーバのウォッチドッグ タイマ、モード レジスタ 0 の追加、拡張ボーレートと全体的な高速化、プログラム可能なレシーバ、トランスミッタ割り込みです。

ピン プログラミングにより、デバイスは Motorola または Intel バスインターフェイスで動作可能です。MR0A レジスタのビット 3 により、デバイスは 8 バイト FIFO モードで動作可能です。

テキサス・インスツルメンツの TL28L92 デュアル ユニバーサル非同期レシーバ / トランスミッタ (DUART) は、シングルチップの CMOS-LSI 通信デバイスで、2 つの全二重非同期レシーバ / トランスミッタ チャネルを 1 つのパッケージに搭載しています。このデバイスはマイクロプロセッサと直接接続して、モデムおよび DMA インターフェイスを備えたポーリングまたは割り込み駆動のシステムで使用できます。

各チャネルの動作モードとデータ フォーマットは、別々にプログラム可能です。さらに、各レシーバおよびトランスミッタは、28 の固定ボーレート、プログラム可能なカウンタ / タイマから生成された 16× クロック、または外部の 1× または 16× クロックのいずれかを動作速度に選択できます。ボーレート ジェネレータおよびカウンタ / タイマは、水晶振動子、または外部クロック入力で直接動作できます。レシーバとトランスミッタの動作速度を別々にプログラムできるため、DUART はクラスタ化された端末システムなどのデュアルスピード チャネル アプリケーションで使用すると特に能力を発揮します。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

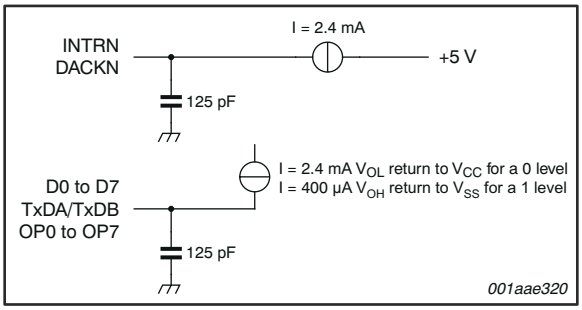
各レシーバおよびトランスミッタは、8 文字または 16 文字の FIFO でバッファされ、レシーバのオーバーラン、トランスミッタのアンダーランの可能性を最小限に抑え、割り込み駆動システムでの割り込みオーバーヘッドを低減します。さらに、レシーバ バッファがフルになったときにリモート トランスミッタをディスエーブルにするために、RTS/CTS 信号によってフロー制御機能が提供されます。TL28L92 には、多目的の 7 ビット入力ポートと多目的の 8 ビット出力ポートも搭載されています。これらは汎用 I/O ポートとして使用することも、プログラム制御の下で特定の機能 (クロック入力、ステータス / 割り込み出力など) を割り当てることもできます。

TL28L92 は、現在 44 ピンの QFP (FR) で供給されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TL28L92	QFP (FR)	12.4mm x 12.4mm

(1) 詳細については、セクション 9 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



出力のテスト条件

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3 Pin Configurations and Functions

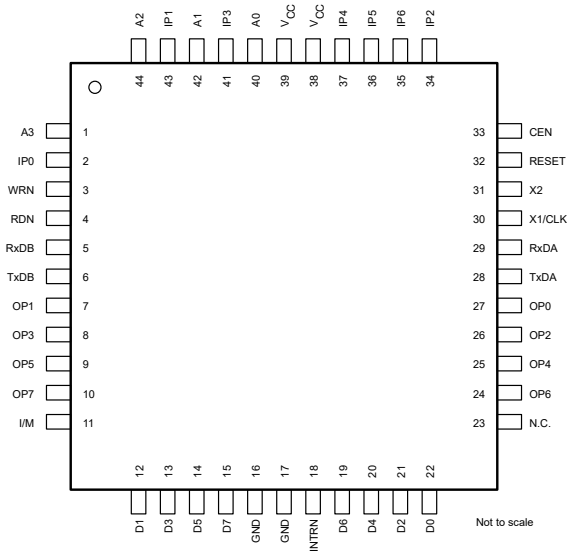


図 3-1. 80xxx Mode FR (QFP) Package (Top View)

表 3-1. Pin Functions for 80xxx Interface

PINS		TYPE	DESCRIPTION
NAME	QFP (FR) PIN NO.		
A0, A1, A2, A3	40, 42, 44, 1	I	Address inputs: Select the DUART internal registers and ports for read/write operations.
CEN	33	I	Chip enable: active LOW input signal. When LOW, data transfers between the CPU and the DUART are enabled on D0 to D7 as controlled by the WRN, RDN and A0 to A3 inputs. When HIGH, places the D0 to D7 lines in the 3-state condition.

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表 3-1. Pin Functions for 80xxx Interface (続き)

PINS		TYPE	DESCRIPTION
NAME	QFP (FR) PIN NO.		
D0, D1, D2, D3, D4, D5, D6, D7	22, 12, 21,13, 20, 14, 19, 15	I/O	Data bus: Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
GND	16, 17	Pwr	Ground
IP0	2	I	Input 0: General purpose input or channel A clear to send active LOW input (CTSAN).
IP1	43	I	Input 1: General purpose input or channel B clear to send active LOW input (CTSBN).
IP2	34	I	Input 2: General-purpose input or counter/timer external clock input.
IP3	41	I	Input 3: General purpose input or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	37	I	Input 4: General purpose input or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	36	I	Input 5: General purpose input or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	35	I	Input 6: General purpose input or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
I/M	11	I	Bus configuration: When HIGH or not connected configures the bus interface to the conditions shown in this table.
INTRN	18	O	Interrupt request: Active LOW, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. This pin requires a pull-up device.
N.C.	23	–	Not connected
OP0	27	O	Output 0: General purpose output or channel A request to send (RTSAN, active LOW). Can be deactivated automatically on receive or transmit.
OP1	7	O	Output 1: General-purpose output or channel B request to send (RTSBN, active LOW). Can be deactivated automatically on receive or transmit.
OP2	26	O	Output 2: General purpose output, or channel A transmitter 1× or 16× clock output, or channel A receiver 1× clock output.
OP3	8	O	Output 3: General purpose output or open-drain, active LOW counter/timer output or channel B transmitter 1× clock output, or channel B receiver 1× clock output.
OP4	25	O	Output 4: General purpose output or channel A open-drain, active LOW, RxA interrupt ISR[1] output.
OP5	9	O	Output 5: General-purpose output or channel B open-drain, active LOW, RxB interrupt ISR[5] output.
OP6	24	O	Output 6: General purpose output or channel A open-drain, active LOW, TxA interrupt ISR[0] output.
OP7	10	O	Output 7: General-purpose output, or channel B open-drain, active LOW, TxB interrupt ISR[4] output.
RDN	4	I	Read strobe: When LOW and CEN is also LOW, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
RESET	32	I	Reset: A HIGH level clears internal registers (SRA, SRB, IMR, ISR, OPR and OPCR), puts OP0 to OP7 in the HIGH state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (HIGH) state. Sets MR pointer to MR1. See 図 4-2.

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表 3-1. Pin Functions for 80xxx Interface (続き)

PINS		TYPE	DESCRIPTION
NAME	QFP (FR) PIN NO.		
RxDA	29	I	Channel A receiver serial data input: The least significant bit is received first. See note on drive levels at block diagram (図 5-1).
RxDB	5	I	Channel B receiver serial data input: The least significant bit is received first. See note on drive levels at block diagram (図 5-1).
TxDA	28	O	Channel A transmitter serial data output: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, Idle or when operating in local loopback mode. See note on drive levels at block diagram (図 5-1).
TxDB	6	O	Channel B transmitter serial data output: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, Idle, or when operating in local loopback mode. See note on drive levels at block diagram (図 5-1).
V_{CC}	38, 39	Pwr	Power supply: 3.3 V ± 10% or 5 V ± 10 % supply input.
WRN	3	I	Write strobe: When LOW and CEN is also LOW, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
X1/CLK	30	I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see 図 4-9).
X2	31	O	Crystal 2: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see 図 4-9). If X1/CLK is driven from an external source, this pin must be left open.

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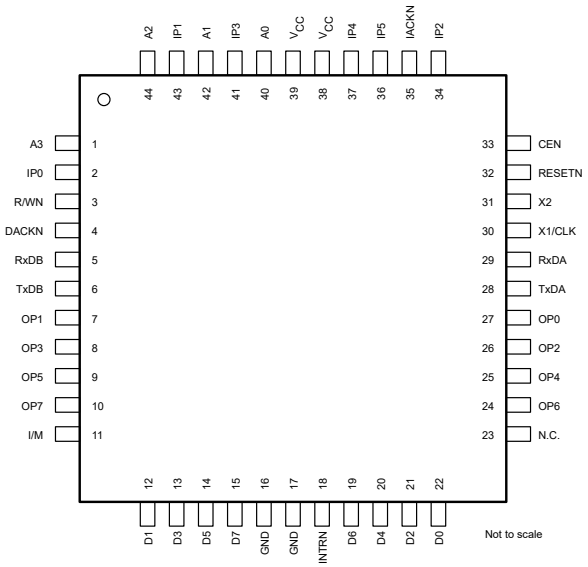


図 3-2. 68xxx Mode FR (QFP) Package (Top View)

表 3-2. Pin Functions for 68xxx Interface

PINS		TYPE	DESCRIPTION
NAME	QFP (FR) PIN NO.		
A0, A1, A2, A3	40, 42, 44, 1	I	Address inputs: Select the DUART internal registers and ports for read/write operations.
CEN	33	I	Chip enable: active LOW input signal. When LOW, data transfers between the CPU and the DUART are enabled on D0 to D7 as controlled by the WRN, RDN and A0 to A3 inputs. When HIGH, places the D0 to D7 lines in the 3-state condition.
DACKN	4	O	Data transfer acknowledge. Active low output. DACKN is asserted low during a write, read, or interrupt. Acknowledge cycle to indicate data transfer between the CPU and the TL28L92.
D0, D1, D2, D3, D4, D5, D6, D7	22, 12, 21,13, 20, 14, 19, 15	I/O	Data bus: Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
GND	16, 17	Pwr	Ground
IACKN	35	I	Interrupt acknowledge. An active low input indicates an interrupt acknowledge cycle. Typically asserted by the CPU in response to an interrupt request. When IACKN is asserted, the TL28L92 places the interrupt vector on the bus and asserts DACKN.
IP0	2	I	Input 0: General purpose input or channel A clear to send active LOW input (CTSAN).
IP1	43	I	Input 1: General purpose input or channel B clear to send active LOW input (CTSBN).
IP2	34	I	Input 2: General-purpose input or counter/timer external clock input.
IP3	41	I	Input 3: General purpose input or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	37	I	Input 4: General purpose input or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	36	I	Input 5: General purpose input or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

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表 3-2. Pin Functions for 68xxx Interface (続き)

PINS		TYPE	DESCRIPTION
NAME	QFP (FR) PIN NO.		
I/M	11	I	Bus configuration: When HIGH or not connected configures the bus interface to the conditions shown in this table.
INTRN	18	O	Interrupt request: Active LOW, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. This pin requires a pull-up device.
N.C.	23	–	Not connected
OP0	27	O	Output 0: General purpose output or channel A request to send (RTSAN, active LOW). Can be deactivated automatically on receive or transmit.
OP1	7	O	Output 1: General-purpose output or channel B request to send (RTSBN, active LOW). Can be deactivated automatically on receive or transmit.
OP2	26	O	Output 2: General purpose output, or channel A transmitter 1× or 16× clock output, or channel A receiver 1× clock output.
OP3	8	O	Output 3: General purpose output or open-drain, active LOW counter/timer output or channel B transmitter 1× clock output, or channel B receiver 1× clock output.
OP4	25	O	Output 4: General purpose output or channel A open-drain, active LOW, RxA interrupt ISR[1] output.
OP5	9	O	Output 5: General-purpose output or channel B open-drain, active LOW, RxB interrupt ISR[5] output.
OP6	24	O	Output 6: General purpose output or channel A open-drain, active LOW, TxA interrupt ISR[0] output.
OP7	10	O	Output 7: General-purpose output, or channel B open-drain, active LOW, TxB interrupt ISR[4] output.
RESETN	32	I	Reset. Active low. When RESETN is asserted the following registers are cleared: SRA, SRB, IMR, ISR, OPR, and OPCR. Outputs OP0 and OP7 are driven to a logic high state, the counter/timer is stopped, and channels A and B are placed in the inactive state with the TxDA and TxDB outputs in the high state.
RxDA	29	I	Channel A receiver serial data input: The least significant bit is received first. See note on drive levels at block diagram (図 5-2).
RxDB	5	I	Channel B receiver serial data input: The least significant bit is received first. See note on drive levels at block diagram (図 5-2).
R/WN	3	I	Read/Write: Input. When CEN is low and R/WN input is high this indicates a read cycle. When CEN is low and R/WN is low this indicates a write cycle.
TxDA	28	O	Channel A transmitter serial data output: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, Idle or when operating in local loopback mode. See note on drive levels at block diagram (図 5-2).
TxDB	6	O	Channel B transmitter serial data output: The least significant bit is transmitted first. This output is held in the Mark condition when the transmitter is disabled, Idle, or when operating in local loopback mode. See note on drive levels at block diagram (図 5-2).
V_{CC}	38, 39	Pwr	Power supply: 3.3 V ± 10% or 5 V ± 10 % supply input.
X1/CLK	30	I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see 図 4-9).
X2	31	O	Crystal 2: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see 図 4-9). If X1/CLK is driven from an external source, this pin must be left open.

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4 Electrical Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
T_{amb}	Ambient temperature(2) (3)		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C
V_{CC}	Voltage from V_{CC} to GND(3)		–0.5	7	V
V_S	Voltage from any pin to GND(3)		–0.5	V_{CC} + 0.5	V
P_D	Package power dissipation	QFP44 package		1.78	W
		HVQFN48 package		0.5	
P_{der}	Dissipation derating factor (above 25°C)	QFP44 package		14	mW/°C
		HVQFN48 package		28	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For operation at elevated temperatures, the device must be derated based on 150°C maximum junction temperature.
(3) Parameters are valid over specified temperature range.

4.2 Static Characteristics for 5V Operation

V_{CC} = 5V ±10 %; T_{amb} = –40°C to 85°C (unless otherwise noted) (1) (2)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage	Except pin X1/CLK		2.4	1.5		V
		Pin X1/CLK		0.8 × V_{CC}	2.4		
V_{OL}	Low-level output voltage	I_{OL} = 2.4mA			0.2	0.4	V
V_{OH}	High-level output voltage	Except open-drain outputs(3); I_{OH} = –400µA		V_{CC} – 0.5			V
$I_{I(1XPD)}$	Power-down mode input current on pin X1/CLK	V_I = 0V to V_{CC}		0.5	0.05	0.5	µA
$I_{IL(X1)}$	Low-level operating input current on pin X1/CLK	V_I = 0V				0	µA
$I_{IH(X1)}$	HIgh-level operating input current on pin X1/CLK	V_I = V_{CC}				130	µA
I_I	Input leakage current	V_I = 0V to V_{CC},	All except input port pins	–0.5	0.05	0.5	µA
			Input port pins(4)	–8	–2	0.5	
I_{OZH}	High-level output OFF current (3-state data bus)	V_I = V_{CC}				0.5	µA
I_{OZL}	Low-level output OFF current (3-state data bus)	V_I = 0V		–0.5			µA
I_{ODL}	Low-level output current in OFF state (open drain)	V_I = 0V		–0.5			µA
I_{ODH}	High-level output current in OFF state (open drain)	V_I = V_{CC}				0.5	µA
I_{CC}	Power supply current	CMOS input levels, (5)	Operating mode		7	10	mA
			Power-down mode		25	40	µA

(1) All voltage measurements are referenced to ground. For testing, all inputs swing between 0.4V and 3V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 0.8 × V_{CC}. All time measurements are referenced at input voltages of 0.8V and 2V, and output voltages of 0.8V and 2V, as appropriate.
(2) Typical values are at 25°C, typical supply voltages, and typical processing parameters.
(3) Test conditions for outputs: C_L = 125pF, except open-drain outputs. Test conditions for open-drain outputs: C_L = 125pF, constant current source = 2.6mA.
(4) Input port pins have active pull-up transistors that will source a typical 2µA from V_{CC} when the input pins are at VSS. Input port pins at V_{CC} source 0µA.
(5) All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} – 0.2V and V_{SS} + 0.2V.

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4.3 Static Characteristics for 3.3V Operation

V_{CC} = 3.3V ±10 %; T_{amb} = –40°C to 85°C (unless otherwise noted)(1) (2)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage				0.65	0.2 × V_{CC}	V
V_{IH}	High-level input voltage			2.4	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 2.4mA			0.2	0.4	V
V_{OH}	High-level output voltage	except open-drain outputs(3); I_{OH} = –400µA		V_{CC} – 0.5	V_{CC} – 0.2		V
$I_{I(1XPD)}$	Power-down mode input current on pin X1/CLK	V_I = 0V to V_{CC}		0.5	0.05	0.5	µA
$I_{IL(X1)}$	Low-level operating input current on pin X1/CLK	V_I = 0V				0	µA
$I_{IH(X1)}$	HIgh-level operating input current on pin X1/CLK	V_I = V_{CC}				130	µA
I_I	Input leakage current	V_I = 0V to V_{CC},	all except input port pins	–0.5	0.05	0.5	µA
			input port pins(4)	–8	–2	0.5	
I_{OZH}	High-level output OFF current (3-state data bus)	V_I = V_{CC}				0.5	µA
I_{OZL}	Low-level output OFF current (3-state data bus)	V_I = 0V		–0.5			µA
I_{ODL}	Low-level output current in OFF state (open drain)	V_I = 0V		–0.5			µA
I_{ODH}	High-level output current in OFF state (open drain)	V_I = V_{CC}				0.5	µA
I_{CC}	Power supply current	CMOS input levels,(5)	Operating mode		4	6	mA
			Power-down mode		15	25	µA

(1) All voltage measurements are referenced to ground. For testing, all inputs swing between 0.4V and 3V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 0.8 × V_{CC}. All time measurements are referenced at input voltages of 0.8V and 2V, and output voltages of 0.8V and 2V, as appropriate.
(2) Typical values are at 25°C, typical supply voltages, and typical processing parameters.
(3) Test conditions for outputs: C_L = 125pF, except open-drain outputs. Test conditions for open-drain outputs: C_L = 125pF, constant current source = 2.6mA.
(4) Input port pins have active pull-up transistors that will source a typical 2 µA from V_{CC} when the input pins are at VSS. Input port pins at V_{CC} source 0µA.
(5) All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} – 0.2V and V_{SS} + 0.2V.

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4.4 Dynamic Characteristics for 5V Operation

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset Timing (see 図 4-2)						
t_{RES}	Reset pulse width		100	18		ns
Bus Timing(5) (see 図 4-3)						
t_{AS}	A0 to A3 set-up time to RDN, WRN LOW		10	6		ns
t_{AH}	A0 to A3 hold time from RDN, WRN LOW		20	12		ns
t_{CS}	CEN set-up time to RDN, WRN LOW		0			ns
t_{CH}	CEN hold time from RDN, WRN LOW		0			ns
t_{RW}	WRN, RDN pulse width (LOW time)		15	8		ns
t_{DD}	Data valid after RDN LOW	125 pF load; see 図 4-1 for smaller loads		40	55	ns
t_{DA}	RDN LOW to data bus active		0(6)			ns
t_{DF}	data bus floating after RDN or CEN HIGH				20	ns
t_{DI}	RDN or CEN HIGH to data bus invalid		0			ns
t_{DS}	Data bus set-up time before WRN or CEN HIGH (write cycle)		25	17		ns
t_{DH}	Data hold time after WRN HIGH		0	–12		ns
t_{RWD}	HIGH time between read and/or write cycles		17	10		ns
Port Timing (5) (see 図 4-7)						ns
t_{PS}	Port in set-up time before RDN LOW (Read IP ports cycle)		0	–20		ns
t_{PH}	Port in hold time after RDN HIGH		0	–20		
t_{PD}	OP port valid after WRN or CEN HIGH (OPR write cycle)			40	60	
Interrupt Timing (see 図 4-8)						
t_{IR}	INTRN (or OP3 to OP7 when used as interrupts)	Read Rx FIFO (RxRDY/FFULL interrupt)		40	60	ns
		Write Tx FIFO (TxRDY interrupt)		40	60	
		Reset command (delta break change interrupt)		40	60	
		Stop C/T command (counter/timer interrupt)		40	60	
		Read IPCR (delta input port change interrupt)		40	60	
		Write IMR (clear of change interrupt mask bit(s))		40	60	

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4.4 Dynamic Characteristics for 5V Operation (続き)

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Timing (see 図 4-9)						
t_{CLK}	X1/CLK HIGH or LOW time		30	20		ns
f_{CLK}	X1/CLK frequency		0.1(7)	3.686	8	MHz
t_{CTC}	C/T clock (IP2) HIGH or LOW time (C/T external clock input)		30	10		
f_{CTC}	C/T clock (IP2) frequency		0(7)		8	MHz
t_{RX}	RxC HIGH or LOW time	16×	30	10		ns
f_{RX}	RxC frequency	16×	0(7)		16	MHz
		1×(8)	0(7)		1	
t_{TX}	TxC HIGH or LOW time	16×	30	10		ns
f_{TX}	TxC frequency	16×			16	MHz
		1×(8)	0(8)		1	
Transmitter Timing, External Clock (see 図 4-10)						
t_{TXD}	TxD output delay from TxC LOW (TxC input pin)			40	60	ns
t_{TCS}	Output delay from TxC output pin LOW to TxD data output			6	30	ns
Receiver Timing, External Clock (see 図 4-11)						
t_{RXS}	RxD data set-up time to RxC HIGH		50	40		ns
t_{RXH}	RxD data hold time from RxC HIGH		50	40		ns
68xxx or Motorola Bus Timing (see 図 4-3, 図 4-4, and 図 4-5)(9)						
t_{DCR}	DACKN LOW (read cycle) from X1 HIGH			15	35	ns
t_{DCW}	DACKN LOW (write cycle) from X1 HIGH			15	35	ns
t_{DAT}	DACKN high-impedance from CEN or IACKN HIGH			8	10	ns
t_{CSC}	CEN or IACKN set-up time to X1 HIGH for minimum DACKN cycle		16	8		ns

(1) Parameters are valid over specified temperature and voltage range.
(2) All voltage measurements are referenced to ground. For testing, all inputs swing between 0.4V and 3V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 0.8 × V_{CC}. All time measurements are referenced at input voltages of 0.8V and 2V, and output voltages of 0.8V and 2V, as appropriate.
(3) Test conditions for outputs: C_L = 125pF, except open-drain outputs. Test conditions for open-drain outputs: C_L = 125pF, constant current source = 2.6mA.
(4) Typical values are the average values at 25°C and 5V.
(5) Timing is illustrated and referenced to the WRN and RDN Inputs. Also, CEN may be the strobing input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
(6) Specified by characterization of sample units.
(7) Minimum frequencies are not tested but are specified by design.
(8) Clocks for 1× mode should maintain a 60/40 duty cycle or better.
(9) Minimum DACKN time is ((t_{DCR} or t_{DCW}) t_{CSC} + 2 X1 edges + rise time over 5ns). Two X1 edges is 273ns at 3.6864MHz. For faster bus cycles, the 80xxx bus timing may be used while in the 68xxx mode. It is not necessary to wait for DACKN to insure the proper operation of the SC28C92. In all cases, the data is written to the TL28L92 on the falling edge of DACKN or the rise of CEN. The fall of CEN initializes the bus cycle. The rise of CEN ends the bus cycle. DACKN LOW or CEN HIGH completes the write cycle.

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4.5 Dynamic Characteristics for 3.3V Operation

over operating free-air temperature range (unless otherwise noted)(1) (2) (3) (4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset Timing (see 図 4-2)						
t_{RES}	Reset pulse width		100	20		ns
Bus Timing(5) (see 図 4-3)						
t_{AS}	A0 to A3 set-up time to RDN, WRN LOW		10	6		ns
t_{AH}	A0 to A3 hold time from RDN, WRN LOW		33	16		ns
t_{CS}	CEN set-up time to RDN, WRN LOW		0			ns
t_{CH}	CEN hold time from RDN, WRN LOW		0			ns
t_{RW}	WRN, RDN pulse width (LOW time)		20	10		ns
t_{DD}	Data valid after RDN LOW	125pF load; see 図 4-1 for smaller loads		46	75	ns
t_{DA}	RDN LOW to data bus active		0(6)			ns
t_{DF}	data bus floating after RDN or CEN HIGH			15	20	ns
t_{DI}	RDN or CEN HIGH to data bus invalid		0			ns
t_{DS}	Data bus set-up time before WRN or CEN HIGH (write cycle)		43	20		ns
t_{DH}	Data hold time after WRN HIGH		0	–15		ns
t_{RWD}	HIGH time between read and/or write cycles		27	10		ns
Port Timing (5) (see 図 4-7)						ns
t_{PS}	Port in set-up time before RDN LOW (Read IP ports cycle)		0	–20		ns
t_{PH}	Port in hold time after RDN HIGH		0	–20		
t_{PD}	OP port valid after WRN or CEN HIGH (OPR write cycle)			50	75	
Interrupt Timing (see 図 4-8)						
t_{IR}	INTRN (or OP3 to OP7 when used as interrupts)	Read Rx FIFO (RxRDY/FFULL interrupt)		40	79	ns
		Write Tx FIFO (TxRDY interrupt)		40	79	
		Reset command (delta break change interrupt)		40	79	
		Stop C/T command (counter/timer interrupt)		40	79	
		Read IPCR (delta input port change interrupt)		40	79	
		Write IMR (clear of change interrupt mask bit(s))		40	79	

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4.5 Dynamic Characteristics for 3.3V Operation (続き)

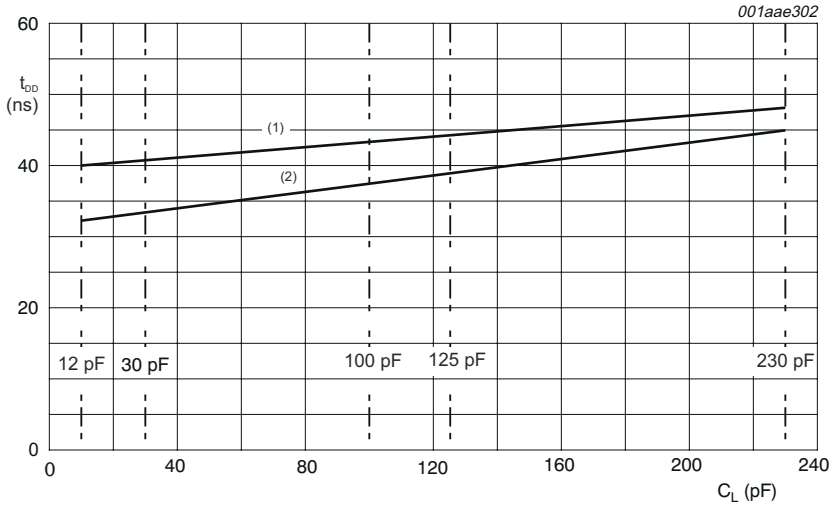
over operating free-air temperature range (unless otherwise noted)(1) (2) (3) (4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Timing (see 図 4-9)						
t_{CLK}	X1/CLK HIGH or LOW time		35	25		ns
f_{CLK}	X1/CLK frequency		0.1(7)	3.686	8	MHz
t_{CTC}	C/T clock (IP2) HIGH or LOW time (C/T external clock input)		30	15		
f_{CTC}	C/T clock (IP2) frequency		0(7)		8	MHz
t_{RX}	RxC HIGH or LOW time	16×	30	10		ns
f_{RX}	RxC frequency	16×	0(7)		16	MHz
		1×(8)	0(7)		1	
t_{TX}	TxC HIGH or LOW time	16×	30	15		ns
f_{TX}	TxC frequency	16×			16	MHz
		1×(8)	0(8)		1	
Transmitter Timing, External Clock (see 図 4-10)						
t_{TXD}	TxD output delay from TxC LOW (TxC input pin)			40	78	ns
t_{TCS}	Output delay from TxC output pin LOW to TxD data output			8	30	ns
Receiver Timing, External Clock (see 図 4-11)						
t_{RXS}	RxD data set-up time to RxC HIGH		50	10		ns
t_{RXH}	RxD data hold time from RxC HIGH		50	10		ns
68xxx or Motorola Bus Timing (see 図 4-3, 図 4-4, and 図 4-5)(9)						
t_{DCR}	DACKN LOW (read cycle) from X1 HIGH			18	57	ns
t_{DCW}	DACKN LOW (write cycle) from X1 HIGH			18	57	ns
t_{DAT}	DACKN high-impedance from CEN or IACKN HIGH			10	15	ns
t_{CSC}	CEN or IACKN set-up time to X1 HIGH for minimum DACKN cycle		30	10		ns

(1) Parameters are valid over specified temperature and voltage range.
(2) All voltage measurements are referenced to ground. For testing, all inputs swing between 0.4V and 3V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 0.8 × V_{CC}. All time measurements are referenced at input voltages of 0.8V and 2V, and output voltages of 0.8V and 2V, as appropriate.
(3) Test conditions for outputs: C_L = 125pF, except open-drain outputs. Test conditions for open-drain outputs: C_L = 125pF, constant current source = 2.6mA.
(4) Typical values are the average values at 25°C and 5V.
(5) Timing is illustrated and referenced to the WRN and RDN Inputs. Also, CEN may be the strobing input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
(6) Specified by characterization of sample units.
(7) Minimum frequencies are not tested but are specified by design.
(8) Clocks for 1× mode should maintain a 60/40 duty cycle or better.
(9) Minimum DACKN time is ((t_{DCR} or t_{DCW}) t_{CSC} + 2 X1 edges + rise time over 5ns). Two X1 edges is 273ns at 3.6864MHz. For faster bus cycles, the 80xxx bus timing may be used while in the 68xxx mode. It is not necessary to wait for DACKN to insure the proper operation of the SC28C92. In all cases, the data is written to the TL28L92 on the falling edge of DACKN or the rise of CEN. The fall of CEN initializes the bus cycle. The rise of CEN ends the bus cycle. DACKN LOW or CEN HIGH completes the write cycle.

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4.6 Typical Performance



(1) V_{CC} = 3.3 V; Tamb = 25°C
(2) V_{CC} = 5.0 V; Tamb = 25°C
Bus cycle times:
80xxx mode: $t_{DD} + t_{RWD}$ = 70 ns for V_{CC} = 5 v or 40 ns for V_{CC} = 3.3 V + rise and fall time of control signals.
68XXX mode: $t_{CSC} + t_{DAT}$ + 1 cycle of the X1 clock for = 70 ns for V_{CC} = 5 V + rise and fall time of control signals.

図 4-1. Port Timing as a Function of Capacitive Loading at Typical Conditions

4.7 Timing Diagrams

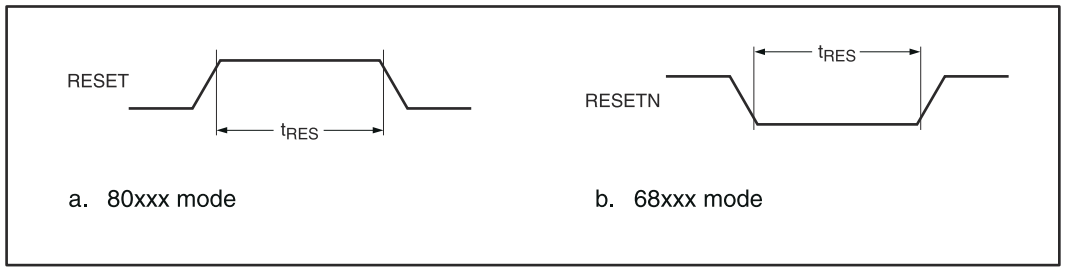


図 4-2. Reset Timing

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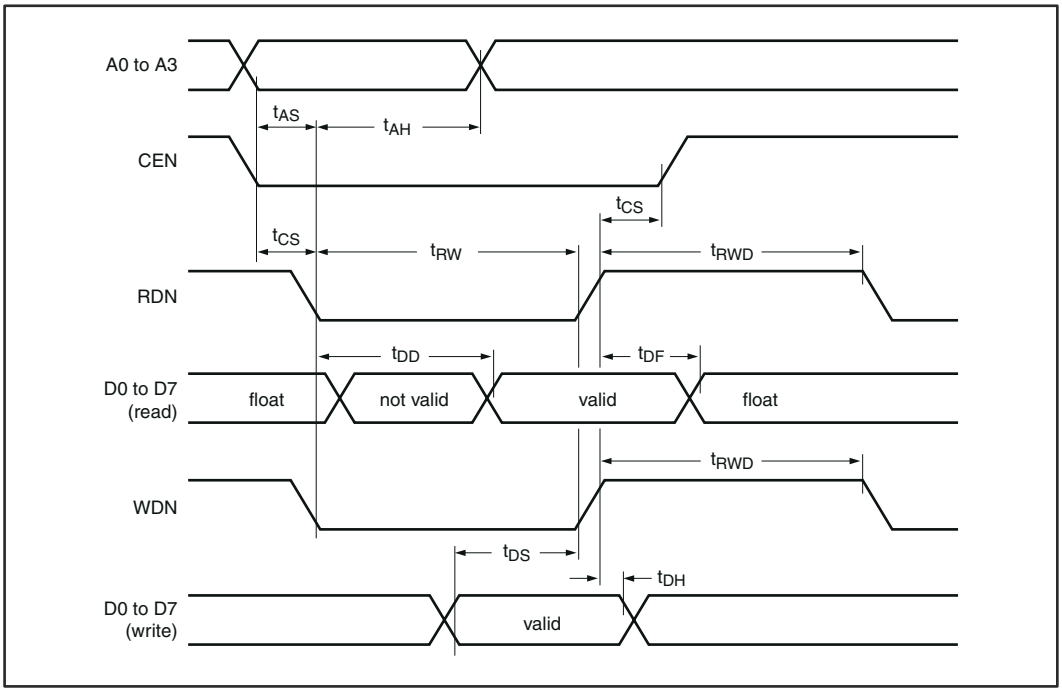


図 4-3. Bus Timing (80xxx Mode)

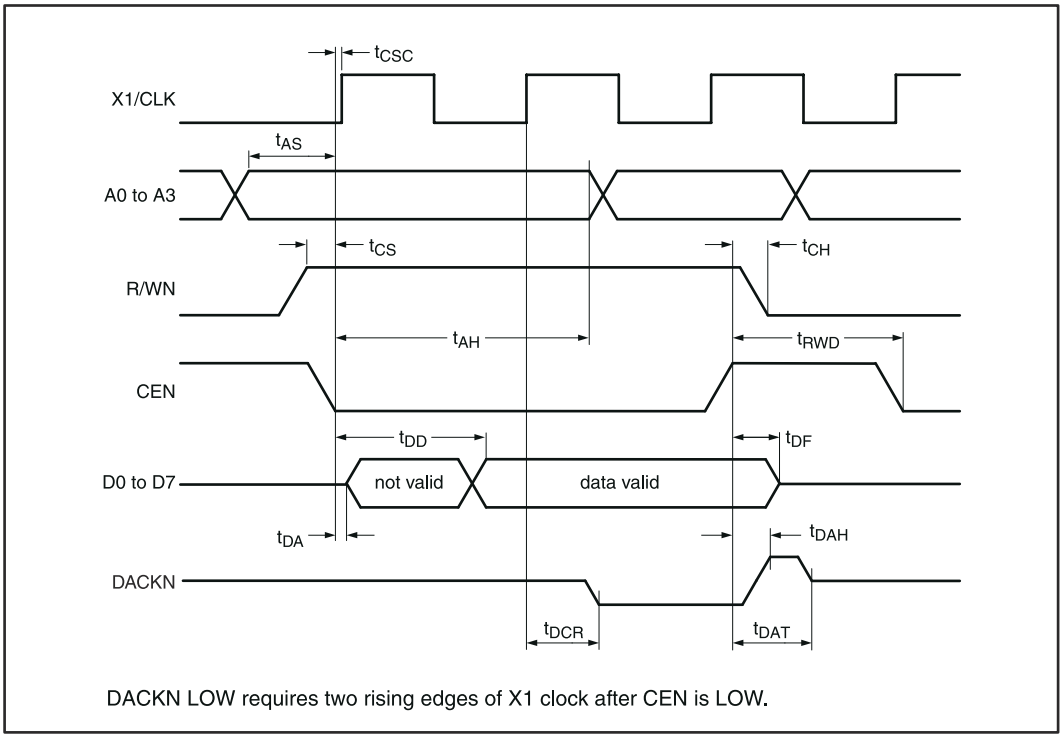
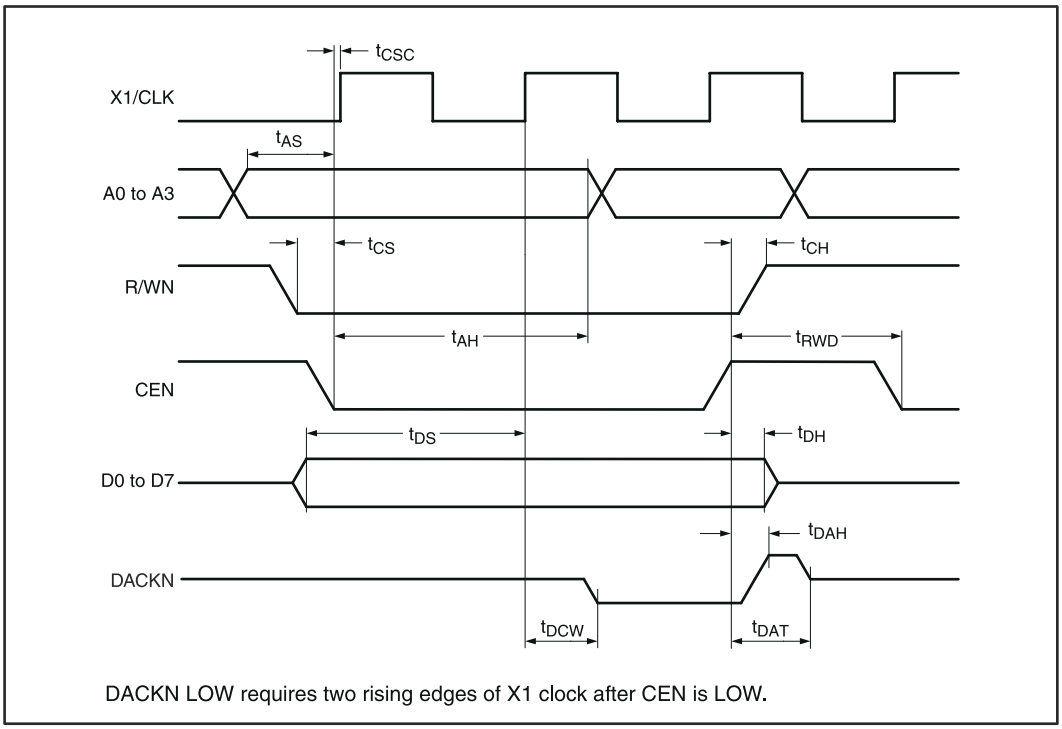


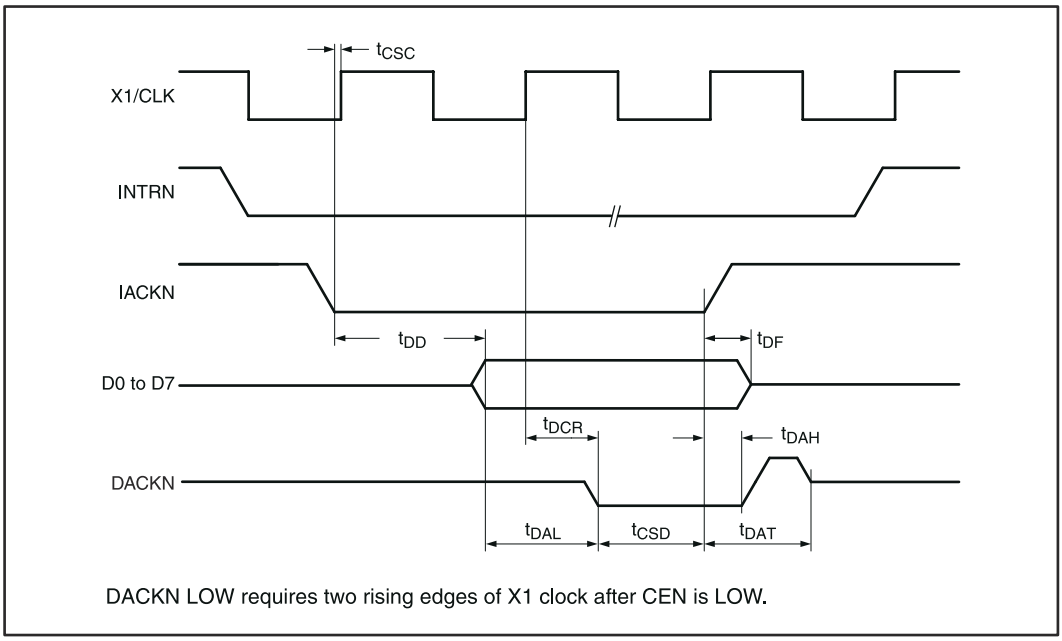
図 4-4. Bus Timing, Read Cycle (68xxx Mode)

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DACKN LOW requires two rising edges of X1 clock after CEN is LOW.

図 4-5. Bus Timing, Write Cycle (68xxx Mode)



DACKN LOW requires two rising edges of X1 clock after CEN is LOW.

図 4-6. Interrupt Cycle Timing (68xxx Mode)

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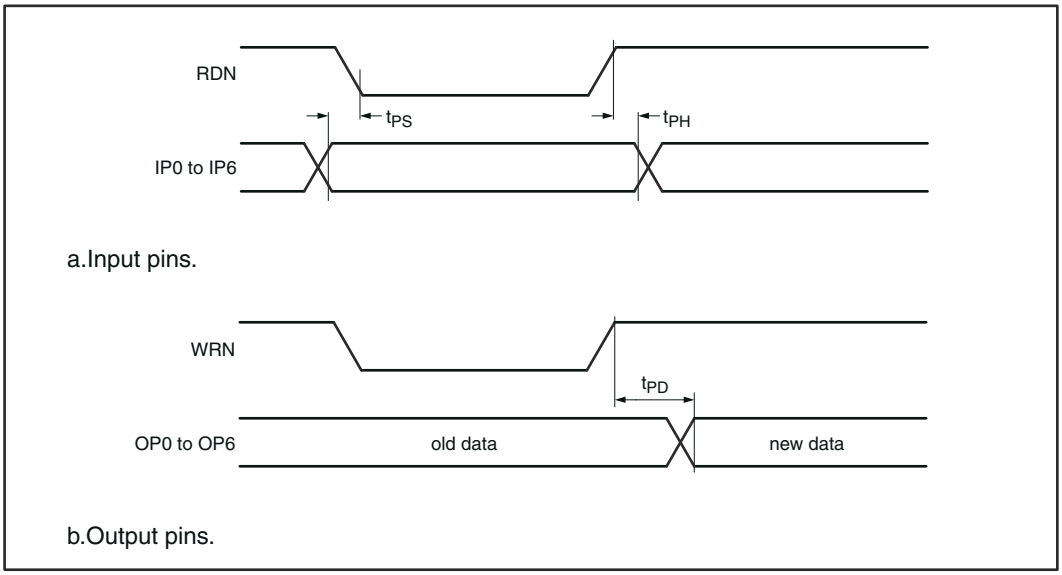
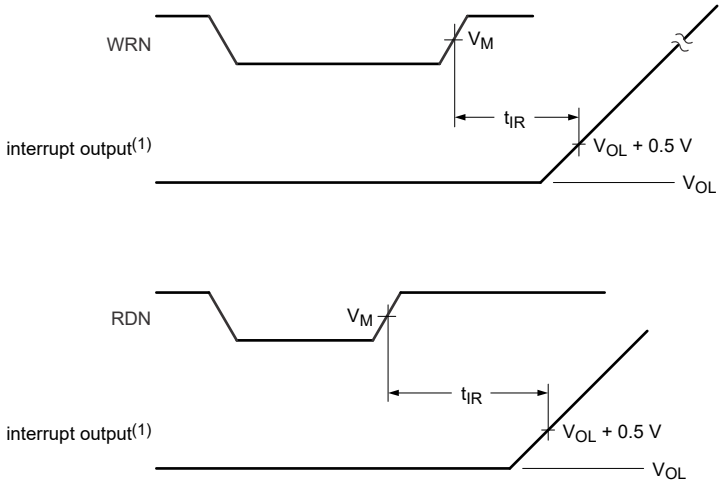


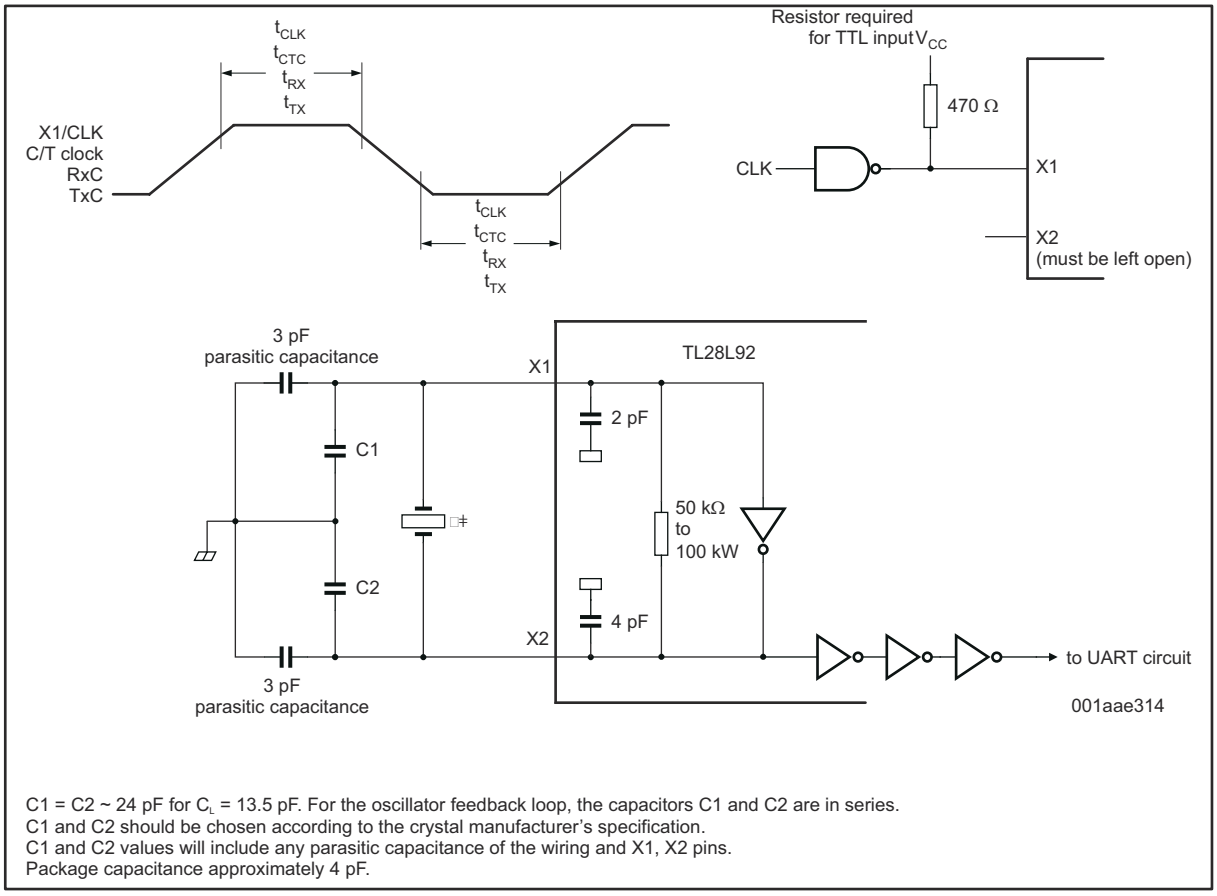
図 4-7. Port Timing



The test for open-drain outputs is intended to switch the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.2V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.
(1) IRQN or OP3toOP7 when used as interrupt outputs.

図 4-8. Interrupt Timing (80xxx Mode)

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C1 = C2 ~ 24 pF for C_L = 13.5 pF. For the oscillator feedback loop, the capacitors C1 and C2 are in series.
C1 and C2 should be chosen according to the crystal manufacturer's specification.
C1 and C2 values will include any parasitic capacitance of the wiring and X1, X2 pins.
Package capacitance approximately 4 pF.

図 4-9. Clock Timing

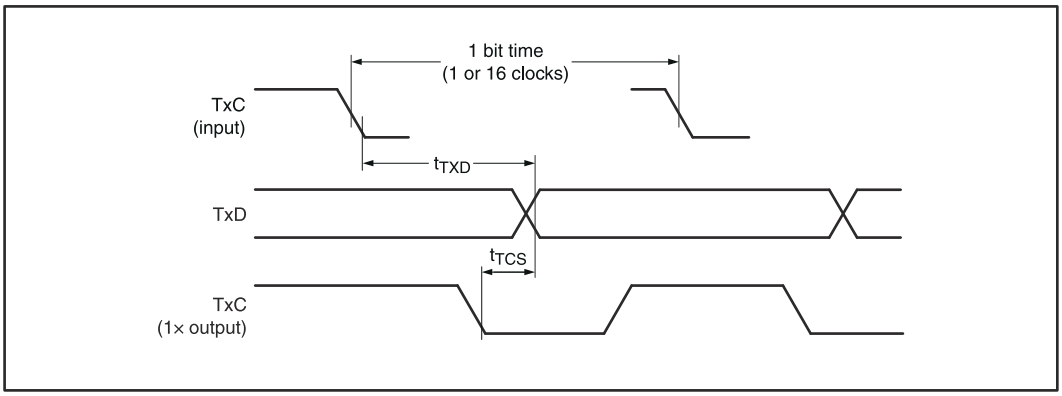


図 4-10. Transmitter External Clocks

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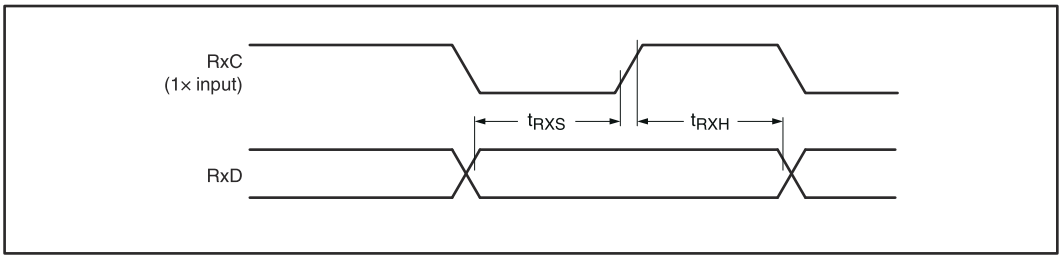
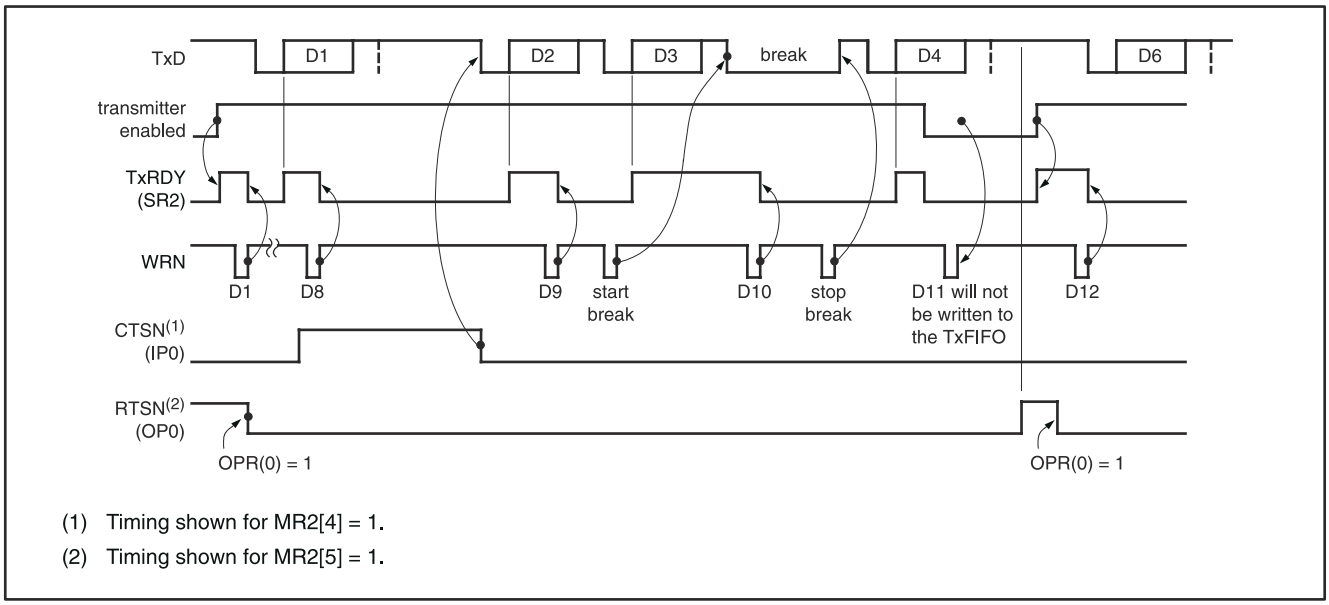


図 4-11. Receiver External Clocks



(1) Timing shown for MR2[4] = 1.
(2) Timing shown for MR2[5] = 1.

図 4-12. Transmitter Timing

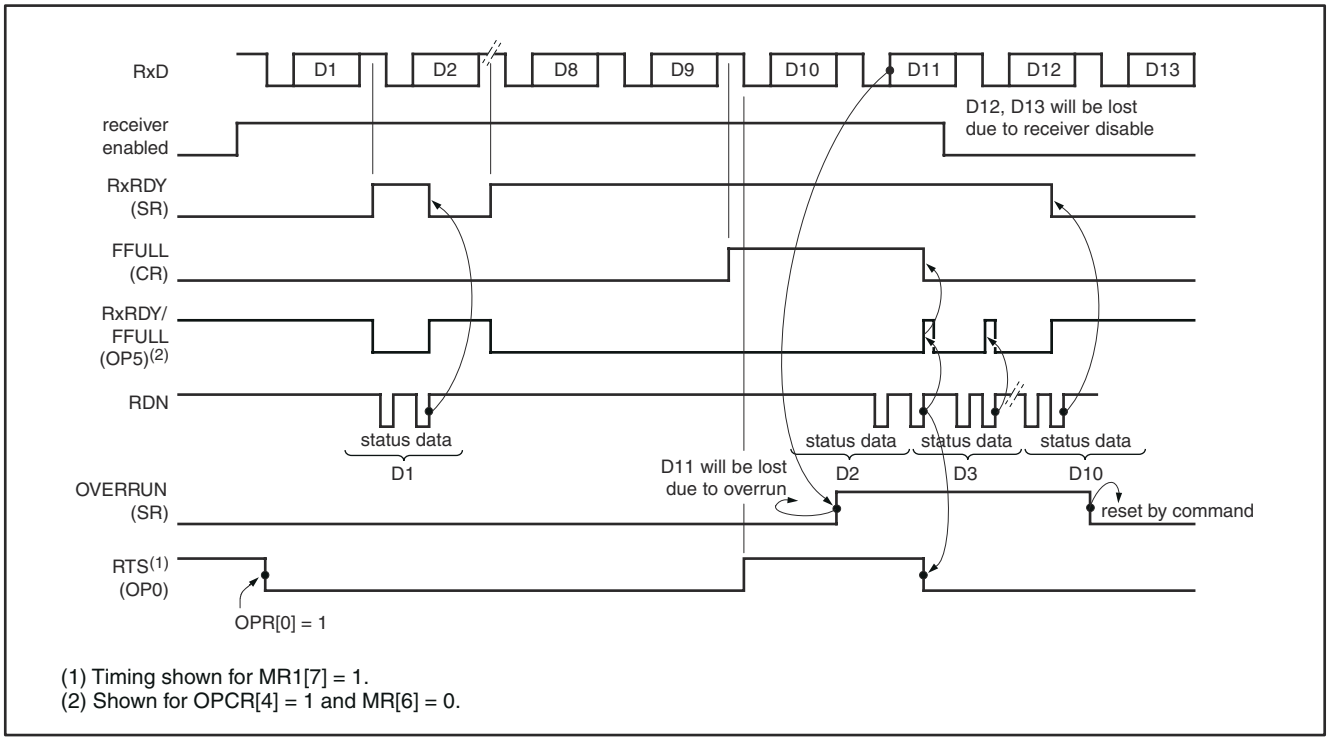


図 4-13. Receiver Timing

4.8 Test Information

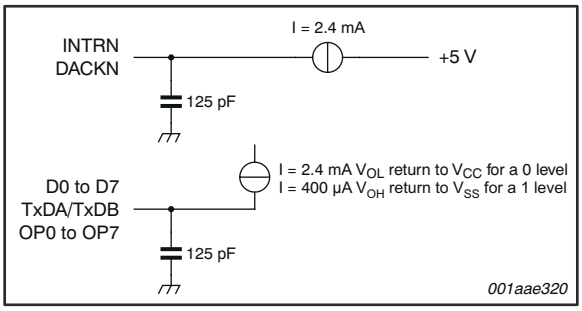


図 4-14. Test Conditions on Outputs

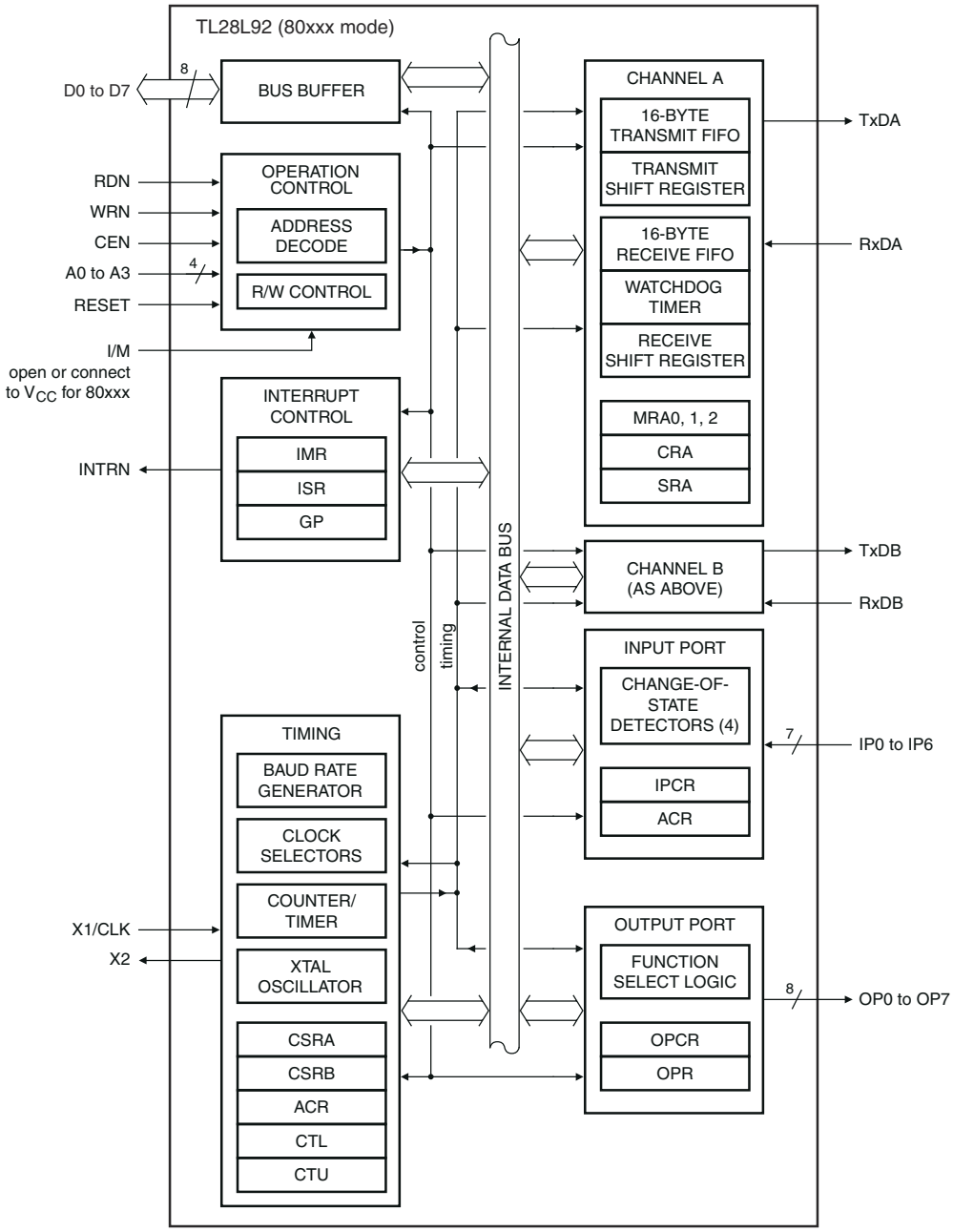
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5 Detailed Description

5.1 Overview

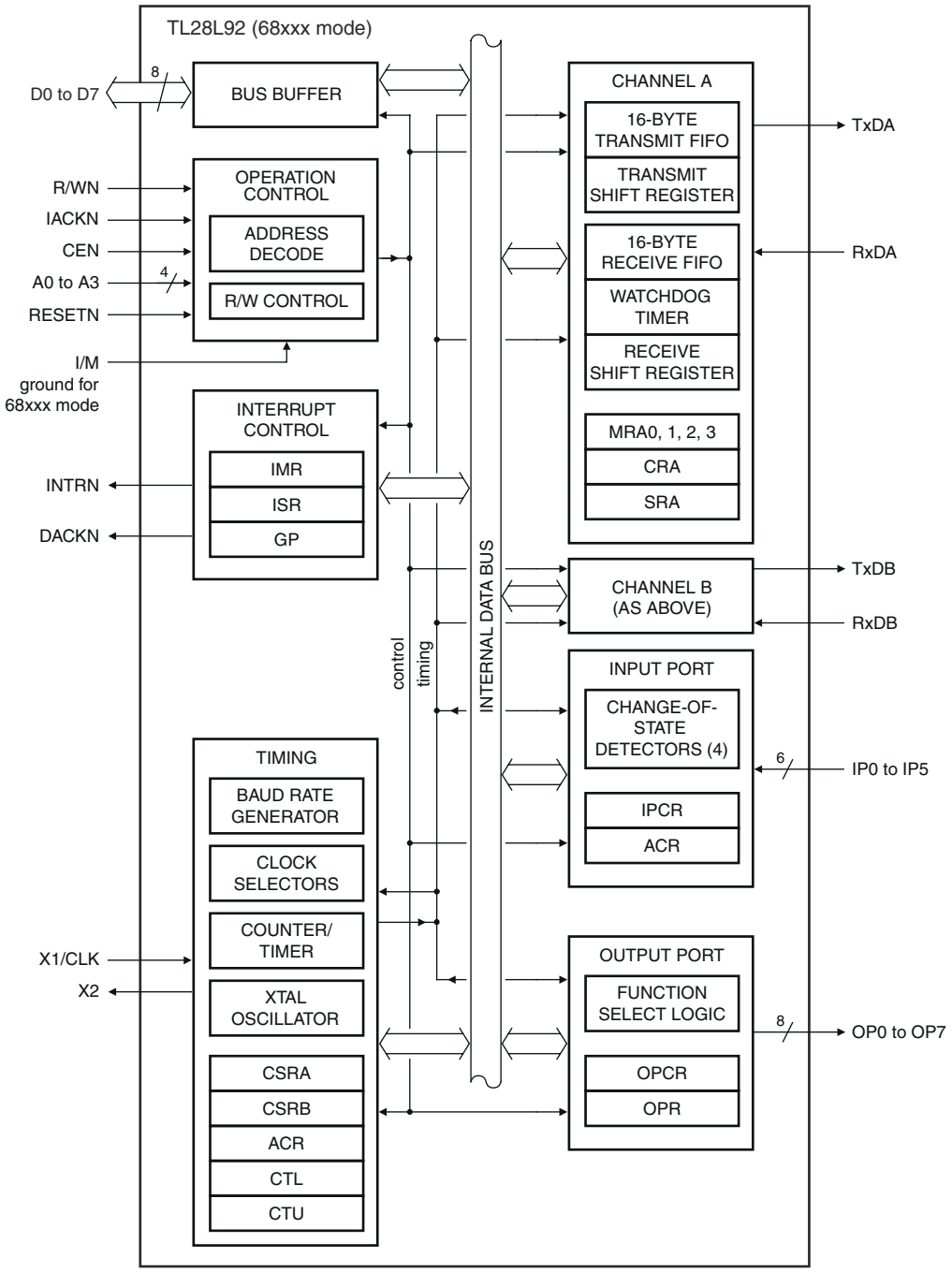
The TL28L92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. See 図 5-1 and 図 5-2 .

5.2 Functional Block Diagram



A. The data pins TxD and RxD are considered idle at the logic 1 (HIGH) level when inactive, or active when at the logic 0 (LOW) level. Comments about these levels when RS232 is referenced often refer to Mark and Space levels. Mark usually means inactive and Space means active. The voltage levels represented by the terms Mark and Space are often reversed from those above: Mark is low voltage, and Space is high voltage.

図 5-1. Block Diagram (80xxx Mode)



A. The data pins TxD and RxD are considered idle at the logic 1 (HIGH) level when inactive, or active when at the logic 0 (LOW) level. Comments about these levels when RS232 is referenced often refer to Mark and Space levels. Mark usually means inactive and Space means active. The voltage levels represented by the terms Mark and Space are often reversed from those above: Mark is low voltage, and Space is high voltage.

図 5-2. Block Diagram (68xxx Mode)

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5.3 Feature Description

5.3.1 Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

5.3.2 Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus.

5.3.3 Interrupt Control

A single active LOW interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3 to OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open-drain active LOW configuration. The OP pins may be used for DMA and modem control as well (see セクション 6.4).

5.3.4 FIFO Configuration

Each receiver and transmitter has a 16 byte FIFO. These FIFOs may be configured to operate at a fill capacity of either 8 bytes or 16 bytes. The 8 byte or 16 byte mode is controlled by the MR0A[3] bit. A logic 0 value for this bit sets the 8-bit mode (the default); a logic 1 sets the 16 byte mode. MR0A bit 3 sets the FIFO size for both channels.

The FIFO fill interrupt level automatically follow the programming of the MR0A[3] bit. See 表 6-22 and 表 6-23.

5.3.5 68xxx Mode

When the I/M pin is connected to GND (ground), the operation of the TL28L92 switches to the bus interface compatible with the Motorola bus interfaces. Several of the pins change their function as follows:

- IP6 becomes IACKN input
- RDN becomes DACKN
- WRN becomes R/WN

The interrupt vector is enabled and the interrupt vector is placed on the data bus when IACKN is asserted LOW. The interrupt vector register is located at address 0xC. The contents of this register are set to 0x0F on the application of RESETN.

The generation of DACKN uses two positive edges of the X1 clock as the DACKN delay from the falling edge of CEN. If the CEN is withdrawn before two edges of the X1 clock occur, the generation of DACKN is terminated. Systems not strictly requiring DACKN may use the 68xxx mode with the bus timing of the 80xxx mode greatly decreasing the bus cycle time.

5.3.6 Timing Circuits

5.3.6.1 Crystal Clock

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in 図 4-9. Nominal crystal rate is 3.6864 MHz. Rates up to 8 MHz may be used.

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5.3.6.2 Baud Rate Generator

The baud rate generator operates from the oscillator or external clock input at the X1 input and is capable of generating 28 commonly used data communications baud rates ranging from 50kBd to 38.4kBd. Programming bit 0 of MR0 to a logic 1 gives additional baud rates of 57.6kBd, 115.2kBd and 230.4kBd (500 kHz with X1 at 8MHz). Note that the MR0A[2:0] control this change and that the change applies to both channels. MR0B[2:0] are reserved.

The baud rates are based on an input frequency of 3.6864MHz. Changing the X1 frequency changes all baud rates by ratio of 3.6864MHz to the new frequency. All rates generated by the BRG is in the 16× mode. The clock outputs from the BRG are at 16× the actual baud rate.

The counter/timer can be used as a timer to produce a 16× clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal. The use of the counter/timer also requires the generation of a frequency 16× of the baud rate. See セクション 5.3.6.3.

5.3.6.3 Counter/Timer

The Counter/timer is a 16-bit programmable divider that operates in one of three modes: counter, timer and time-out. In the timer mode it generates a square wave. In the counter mode, it generates a time delay. In the time-out mode, it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the OP pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from logic 1 to logic 0. A register read address (see 表 6-1) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D(7:0) is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR[3] bit in the interrupt status register.

5.3.6.4 Timer Mode

In the timer mode, a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output is equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode, the ISR bit 3 (ISR[3]) is set each time the counter/timer transitions from logic 1 to logic 0 (HIGH-to-LOW). This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command.

注

The value of the divisor n is (1) Often the division results in a non-integer number; 26.3 for example. One may only program integer numbers to a digital divider. Therefore, 26 (0x1A) is chosen. If 26.7 is the result of the division, then 27 (0x1B) is chosen.

注

Reading of the CTU and CTL registers in the timer mode is not meaningful. When the C/T is used to generate, a baud rate and the C/T is selected through the CSR then the receivers and/or transmitter is operating in the 16× mode. Calculation for the number n to program the counter/timer upper and lower registers is shown in 式 1.

The value of the divisor n is:

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$$n = \frac{\text{counter/timer input clock}}{2 \times 16 \times (\text{desired baud rate})} \quad (1)$$

Often, the division results in a non-integer number; 26.3 for example. One may only program integer numbers to a digital divider. Therefore 26 (0x1A) would be chosen. If 26.7 is the result of the division, then 27 (0x1B) is chosen. This gives a baud rate error of 0.3/26.3 or 0.3/26.7 that yields a percentage error of 1.14% or 1.12% respectively, well within the ability of the asynchronous mode of operation. Higher input frequency to the counter reduces the error effect of the fractional division.

5.3.6.5 Counter Mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect. Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not stopped, a read of the C/T may result in changing data on the data bus.

5.3.6.6 Time-Out Mode

The time-out mode uses the received data stream to control the counter. The time-out mode forces the C/T into the timer mode. Each time a received character is transferred from the shift register to the Rx FIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU is not interrupted for the remaining characters in the Rx FIFO.

By programming the C/T such that it would time-out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time.

注

This is very similar to the watchdog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the Rx FIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing 0xA to CRA or CRB invokes the time-out mode for that channel. Writing 0xC to CRA or CRB will disable the time-out mode. Only one receiver should use this mode at a time. However, if both are on, the time-out occurs after both receivers have been inactive for the time-out period. The start of the C/T is on the logic OR of the two receivers.

The time-out mode disables the regular start counter or stop counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the Rx FIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], is set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the Set Time-out Mode On command, CRx = 0xA, will also clear the counter ready bit and stop the counter until the next character is received. The counter/timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands in セクション 5.3.7.3.

5.3.6.7 Time-Out Mode Caution

When operating in the special time-out mode, it is possible to generate what appears to be a false interrupt, that is, an interrupt without a cause. This can result when a time-out interrupt occurs. Then, before the interrupt is serviced, another character is received, that is, the data stream has started again. (The interrupt latency is

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longer than the pause in the data stream.) In this case, when a new character has been received, the counter/timer is restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR shows the Counter Ready bit not set. If nothing else is interrupting, this read of the ISR returns a 0x00 character. This action can present the appearance of a spurious interrupt.

5.3.6.8 Communications Channels A and B

Each communication channel of the TL28L92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (break received, framing and parity errors) are also FIFOed with each data character.

5.3.6.9 Input Port

The inputs to this unlatched 7-bit (6-bit for 68xxx mode) port can be read by the CPU by performing a read operation at address 0xD. A HIGH input results in a logic 1 while a LOW input results in a logic 0. D7 always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic, modem and DMA.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A HIGH-to-LOW or LOW-to-HIGH transition of these inputs, lasting longer than 25µs to 50µs, sets the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

The input port change of state detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25 µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, to specify that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the situation in which the change of state is just missed and the first change of state is not detected until 25µs later.

5.3.6.10 Output Port

The output ports are controlled from six places: the OPCR, OPR, MR, Command, SOPR and ROPR registers. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the set output port bits command and the reset output bits command. These commands are at 0xE and 0xF, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the set output port bits command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the reset output ports bits command would set OPR5 to zero and, hence, the pin OP5 to a one (V^{DD}).

These pins along with the IP pins and their change-of-state detectors are often used for modem and DMA control.

5.3.7 Operation

5.3.7.1 Transmitter

The TL28L92 is conditioned to transmit data when the transmitter is enabled through the command register. The TL28L92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPT bits is set in the status register. When a character is

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loaded to the transmit FIFO the TxEMPT bit is reset. The TxEMPT will not set until: 1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the Tx FIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the Tx FIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the Tx FIFO, the TxD output remains HIGH and the TxEMT bit in the Status Register (SR) is set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the Tx FIFO.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the Tx FIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the Tx FIFO when the transmitter is disabled.

When the transmitter is reset it stops sending data immediately.

The transmitter can be forced to send a break (a continuous LOW condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset. If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be LOW in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be HIGH, the transmitter will delay the transmission of any following characters until the CTS has returned to the LOW state. CTS going HIGH during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be end of message. See description of the MR2[5] bit for more detail. This feature may be used to automatically turn around a transceiver in simplex systems.

5.3.7.2 Receiver

The TL28L92 is conditioned to receive data when enabled through the command register. The receiver looks for a HIGH-to-LOW (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16× clock for 7 clocks to 1.2 clocks (16× clock mode) or at the next rising edge of the bit time clock (1× clock mode). If RxD is sampled HIGH, the start bit is invalid and the search for a valid start bit begins again. If RxD is still LOW, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the Rx FIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains LOW for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error and overrun error (if any) are strobed into the SR from the next byte to be read from the Rx FIFO. If a break condition is detected (RxD is LOW for the entire character including the stop bit), a character consisting of all zeros is loaded into the Rx FIFO and the received break bit in the SR is set to 1. The RxD input must return to HIGH for two (2) clock edges of the X1 crystal clock for the receiver to recognize the end of the break condition and begin the search for a start bit.

This will usually require a HIGH time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock.

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5.3.7.3 Transmitter Reset and Disable

Note the difference between transmitter disable and reset. A transmitter reset stops transmitter action immediately, clears the transmitter FIFO and returns the idle state. A transmitter disable withdraws the transmitter interrupts but allows the transmitter to continue operation until all bytes in its FIFO and shift register have been transmitted including the final stop bits. It then returns to its idle state.

5.3.7.4 Receiver FIFO

The Rx FIFO consists of a First-In-First-Out (FIFO) stack with a capacity of 8 or 16 characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all 8 or 16 stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the Rx FIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see Section 6.3.5) are popped thus emptying a FIFO position for new data.

A disabled receiver with data in its FIFO may generate an interrupt (see Section 6.3.5). Its status bits remain active and its watchdog, if enabled, will continue to operate.

5.3.7.5 Receiver Status Bits

In addition to the data word, three status bits (parity error, framing error and received break) are also appended to each data character in the FIFO. The overrun error, MR1[5], is not FIFOed.

Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logic OR of the status for all characters coming to the top of the FIFO since the last reset error from the command register was issued. In either mode reading the SR does not affect the FIFO. The FIFO is popped only when the Rx FIFO is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) is set upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output is negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output is reasserted (set LOW) automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

5.3.7.6 Receiver Reset and Disable

Receiver disable stops the receiver immediately. Data being assembled in the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected.

A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and realign the FIFO read/write pointers.

5.3.7.7 Watchdog

A watchdog timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the Rx FIFO which have not been read. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

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This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the Rx FIFO or a read of the Rx FIFO is executed.

5.3.7.8 Receiver Time-Out Mode

In addition to the watchdog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time-out intervals.

The time-out mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the Rx FIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The time-out mode is enabled by writing the appropriate command to the command register. Writing 0xA to CRA or CRB will invoke the time-out mode for that channel. Writing 0xC to CRA or CRB will disable the time-out mode. The time-out mode should only be used by one channel at once, since it uses the C/T. If, however, the time-out mode is enabled from both receivers, the time-out will occur only when both receivers have stopped receiving data for the time-out period. CTU and CTL must be loaded with a value greater than the normal receive character period. The time-out mode disables the regular start counter or stop counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the Rx FIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], is set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the set time-out mode on command, CRx = 0xA, will also clear the counter ready bit and stop the counter until the next character is received.

5.3.7.9 Time-Out Mode Caution

When operating in the special time-out mode, it is possible to generate what appears to be a false interrupt, i.e., an interrupt without a cause. This may result when a time-out interrupt occurs and then, before the interrupt is serviced, another character is received, i.e., the data stream has started again. (The interrupt latency is longer than the pause in the data stream.) In this case, when a new character has been receiver, the counter/timer is restarted by the receiver, thereby withdrawing its interrupt. If, at this time, the interrupt service begins for the previously seen interrupt, a read of the ISR will show the counter ready bit not set. If nothing else is interrupting, this read of the ISR will return a 0x00 character.

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6 Programming

6.1 Register Overview

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in 表 6-1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has three mode registers (MR0, MR1 and MR2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0x0 or 0x1 by MR control commands in the command register Miscellaneous Commands. Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0x0 or 0x1 via the miscellaneous commands of the command register. The pointer is set to 0x1 on reset for compatibility with previous TI UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to セクション 6.2 for register bit overview. The reserved registers at addresses 0x2 and 0xA should never be read during normal operation since they are reserved for internal diagnostics.

表 6-1. TL28L92 Register Addressing READ (RDN = 0), WRITE (WRN = 0)

BINARY ADDRESS				READ OPERATION (RDN = 0 and CEN = 0)	WRITE OPERATION (WRN = 0 and CEN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Interrupt vector (68xxx mode)	Interrupt vector (68xxx mode)
1	1	0	0	Miscellaneous register (Intel mode), IVR Motorola mode	Miscellaneous register (Intel mode), IVR Motorola mode
1	1	0	1	Input Port Register (IPR)	Output Port Configuration Register (OPCR)
1	1	1	0	Start counter command	Set Output Port Bits Command (SOPR)
1	1	1	1	Stop counter command	Reset Output Port Bits Command (ROPR)

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表 6-2. Registers for Channels A and B

REGISTER NAME	CHANNEL A REGISTER	CHANNEL B REGISTER	ACCESS
Mode	MRnA	MRnB	R/W
Status	SRA	SRB	R only
Clock	CSRA	CSRB	W only
Command	CRA	CRB	W only
Receiver FIFO	RxFIFOA	RxFIFOB	R only
Transmitter FIFO	TxFIFOA	TxFIFOB	W only

表 6-3. Registers Supporting Both Channels

REGISTER NAME	MNEMONIC	ACCESS
Input Port Change	IPCR	R
Auxiliary Control	ACR	W
Interrupt Status	ISR	R
Interrupt Mask	IMR	W
Counter/Timer Upper Value	CTU	R
Counter/Timer Lower Value	CTL	R
Counter/Timer Preset Upper	CTPU	W
Counter/Timer Preset Lower	CTPL	W
Input Port	IPR	R
Output Configuration	OPCR	W
Set Output Port	SOPR	W
Reset Output Port	ROPR	W
Interrupt Vector or GP	IVR/GP	R/W

6.2 Condensed Register Bit Formats

表 6-4. Mode Register 0 (MR0)

7	6	5	4	3	2	1	0
RxWATCHDOG	RxINT[2]	TxINT[1:0]		FIFOSIZE	BUADRATE EXTENDED II	TEST2	BAUDRATE EXTENDED1

表 6-5. Mode Register 1 (MR1)

7	6	5	4	3	2	1	0
RxRTS control	RxINT[1]	ERRORMODE	PARITYMODE		PARITYTYPE	bits per character	

表 6-6. Mode Register 2 (MR2)

7	6	5	4	3	2	1	0
channel mode		RTSN Control Tx	CTSN Enable Tx	stop bit length			

表 6-7. Clock Select Register (CSR)

7	6	5	4	3	2	1	0
receiver clock select code				transmitter clock select code			

表 6-8. Command Register (CR)

7	6	5	4	3	2	1	0
channel command code				disable Tx	enable Tx	disable Rx	enable Rx

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表 6-9. Channel Status Register (SR)

7	6	5	4	3	2	1	0
received break	framing error	parity error	overrun error	TxEMT	TxRDY	RxFULL	RxRDY

表 6-10. Interrupt Mask Register (Enables Interrupts) (IMR)

7	6	5	4	3	2	1	0
change input port	change break B	RxRDYB	TxRDTYB	counter ready	change break A	RxRDYA	TxRDYA

表 6-11. Interrupt Status Register (ISR)

7	6	5	4	3	2	1	0
input port change	change break B	RxRDYB FFULLB	TxRDTYB	counter ready	change break A	RxRDYA FFULLA	TxRDYA

表 6-12. Counter/Timer Preset Register, Upper (CTPU)

7	6	5	4	3	2	1	0
8 MSB of the BRG timer divisor							

表 6-13. Counter/Timer Preset Register, Lower (Enables Interrupts) (CTPL)

7	6	5	4	3	2	1	0
8 LSB of the BRG timer divisor							

表 6-14. Auxiliary Control Register and Change of State Control (ACR)

7	6	5	4	3	2	1	0
BRG set select	counter/timer mode and clock source select (see 表 6-51)			enable IP3 COS interrupt	enable IP2 COS interrupt	enable IP1 COS interrupt	enable IP0 COS interrupt

表 6-15. Input Port Change Register (IPCR)

7	6	5	4	3	2	1	0
delta IP3	delta IP2	delta IP1	delta IP0	state of IP3	state of IP2	state of IP1	state of IP0

表 6-16. Input Port Register (IPR)

7	6	5	4	3	2	1	0
state of IP7	state of IP6	state of IP5	state of IP4	state of IP3	state of IP2	state of IP1	state of IP0

表 6-17. Set Output Port Bits Register (SOPR)

7	6	5	4	3	2	1	0
set OP7	set OP6	set OP5	set OP4	set OP3	set OP2	set OP1	set OP0

表 6-18. Reset Output Port Bits Register (ROPR)

7	6	5	4	3	2	1	0
reset OP7	reset OP6	reset OP5	reset OP4	reset OP3	reset OP2	reset OP1	reset OP0

表 6-19. Output Port Configuration Register (OPCR)(1)

7	6	5	4	3	2	1	0
configure OP7	configure OP6	configure OP5	configure OP4	configure OP3	configure OP2	configure OP1	configure OP0

(1) OP1 and OP0 are the RTSN output and are controlled by the MR register

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6.3 Register Descriptions

6.3.1 Mode Registers

6.3.1.1 Mode Register 0 Channel A (MR0A)

表 6-20. Mode Register 0 Channel A (MR0A) (Address 0x0) Bit Allocation(1)

7	6	5	4	3	2	1	0
RxWATCHDOG	RxINT[2]	TxINT[1:0]		FIFOSIZE	BAUDRATE EXTENDED II	TEST2	BAUDRATE EXTENDED I

(1) MR0 is accessed by setting the MR pointer to logic 0 via the command register command B.

表 6-21. Mode Register 0 Channel A (MR0A) (Address 0x0) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	RxWATCHDOG	This bit controls the receiver watchdog timer. 0 = disable 1 = enable When enabled, the watchdog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1× clock. The watchdog timer is used to alert the control processor that data is in the Rx FIFO that has not been read. This situation will occur when the byte count of the last part of a message is not large enough to generate an interrupt. The watchdog timer presents itself as a receiver interrupt with the RxRDY bit set in SR and ISR.
6	RxINT[2]	Bit 2 of receiver FIFO interrupt level. This bit along with bit 6 of MR1 sets the fill level of the FIFO that generates the receiver interrupt. Note that this control is split between MR0 and MR1. This is for backward compatibility to the SC2692. For the receiver these bits control the number of FIFO positions filled when the receiver will attempt to interrupt. After the reset the receiver FIFO is empty. The default setting of these bits cause the receiver to attempt to interrupt when it has one or more bytes in it; see 表 6-22
5 and 4	TxINT[1:0]	Transmitter interrupt fill level. For the transmitter these bits control the number of FIFO positions empty when the receiver will attempt to interrupt; see 表 6-23. After the reset the transmit FIFO has 8 bytes empty. It will then attempt to interrupt as soon as the transmitter is enabled. The default setting (TxINT[1:0] = 00) condition the transmitter to attempt to interrupt only when it is completely empty. As soon as one byte is loaded, it is no longer empty and hence will withdraw its interrupt request.
3	FIFOSIZE	FIFO size for channel A and channel B. Selects the FIFO depth at 8-byte or 16-byte. 0 = 8 bytes 1 = 16 bytes
2	BAUDRATE EXTENDED I	Bits MR0[2:0] are used to select one of the six baud rate groups. See 表 6-32 for the group organization.
1	TEST2	000 = Normal mode
0	BAUDRATE EXTENDED II	001 = Extended mode I 100 = Extended mode II Other combinations of MR0[2:0] should not be used.

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表 6-22. Receiver FIFO Interrupt Fill Level(1)

RxINT[2:1] (BITS MR0[6] AND MR1[6])	INTERRUPT CONDITION
FIFOSIZE = 0 (8 bytes)	
00	1 or more bytes in FIFO (RxRDY)
01	3 or more bytes in FIFO
10	6 or more bytes in FIFO
11	8 bytes in FIFO (RxFULL)
FIFOSIZE = 1 (16 bytes)	
00	1 or more bytes in FIFO (RxRDY)
01	8 or more bytes in FIFO
10	12 or more bytes in FIFO
11	16 bytes in FIFO (RxFULL)

(1) Interrupt fill level must be set when the transmit and receive FIFOs are empty, otherwise the new level takes effect only after a read or a write to the FIFO.

表 6-23. Transmitter FIFO Interrupt Fill Level(1)

TxINT[2:1] (BITS MR0[6] AND MR1[6])	INTERRUPT CONDITION
FIFOSIZE = 0 (8 bytes)	
00	8 bytes empty (TxEMPTY)
01	4 or more bytes empty
10	6 or more bytes empty
11	1 or more bytes empty (TxRDY)
FIFOSIZE = 1 (16 bytes)	
00	16 bytes empty (TxEMPTY)
01	8 or more bytes empty
10	12 or more bytes empty
11	1 or more bytes empty (TxRDY)

(1) Interrupt fill level must be set when the transmit and receive FIFOs are empty, otherwise the new level takes effect only after a read or a write to the FIFO.

6.3.1.2 Mode Register 1 Channel A (MR1A)

表 6-24. Mode Register 1 Channel A (MR1A) (Address 0x0) Bit Allocation(1)

7	6	5	4	3	2	1	0
RxRTS control	RxINT[1]	ERRORMODE	PARITY MODE		PARITY TYPE	bits per character	

(1) MR1A is accessed when the channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

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表 6-25. Mode Register 1 Channel A (MR1A) (Address 0x0) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	RxRTS	Channel A receiver request to send control (flow control). This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. Proper automatic operation of flow control requires OPR[0] (channel A) or OPR[1] (channel B) to be set to logic 1. 0 = No RTS control 1 = RTS control RxRTS = 1 causes RTSAN to be negated (OP0 is driven to a logic 1 [V_{CC}]) upon receipt of a valid start bit if the channel A FIFO is full. This is the beginning of the reception of the 9th byte. If the FIFO is not read before the start of the 10th or 17th byte, an overrun condition will occur and the 10th or 17th or 17th byte is lost. However, the bit in OPR[0] is not reset and RTSAN is asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.
6	RxINT[1]	Bit 1 of the receiver interrupt control. See description of RxINT[2] in 表 6-22 and 表 6-23.
5	ERRORMODE	Channel A error mode select. 0 = character 1 = block This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for channel A. In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logic OR) of the status for all characters coming to the top of the FIFO since the last reset error command for channel A was issued.
4 and 3	PARITY MODE	Channel A parity mode select 00 = with parity 01 = force parity 10 = no parity 11 = multi-drop special mode
2	PARITY TYPE	Channel A parity type select 0 = even 1 = odd This bit selects the parity type (odd or even) if the with parity mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the force parity mode is programmed.
1:0	–	Channel A bits per character select. 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

6.3.1.3 Mode Register 2 Channel A (MR2A)

表 6-26. Mode Register 2 Channel A (MR2A) (Address 0x0) Bit Allocation(1)

7	6	5	4	3	2	1	0
channel mode		RTSN Control Tx	CTSN Enable Tx	stop bit length			

(1) MR2A is accessed when the channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

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表 6-27. Mode Register 2 Channel A (MR2A) (Address 0x0) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7 and 6	–	Channel A mode select. Each channel of the DUART can operate in one of the following four modes: 00 = Normal mode (default) 01 = Automatic echo mode 10 = Local loopback mode 11 = Remote loopback mode 表 6-28 gives a description of the channel modes. The user must exercise care when switching into and out of the various modes. The selected mode is activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of auto echo or remote loopback modes: if the deselection occurs just after the receiver has sampled the stop bit (indicated in auto echo by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in auto echo mode until the entire stop has been retransmitted.
5	–	Channel A transmitter request to send (RTS) control. 0 = No RTS control 1 = RTS control This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the channel A transmit shift register and in the Tx FIFO, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows (line turnaround): 1. Program auto-reset mode: MR2A[5] = 1 2. Enable transmitter 3. Assert RTSAN: OPR[0] = 1 4. Send message 5. Disable transmitter after the last character is loaded into the channel A Tx FIFO 6. The last character is transmitted and OPR[0] is reset one bit time after the last stop bit, causing RTSAN to be negated
4	–	Channel A transmitter clear to send (CTS) control. 0 = Input CTSAN(IP0) has no effect on the transmitter 1 = CTS control enabled If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (LOW), the character is transmitted. If it is negated (HIGH), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes LOW. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.
3 to 0	–	Stop bit length select. This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of $^{9}/_{16}$ to 1 and 1 –$^{9}/_{16}$ to 2 bits, in increments of $^{1}/_{16}$ bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1 –$^{1}/_{16}$ to 2 stop bits can be programmed in increments of $^{1}/_{16}$ bit. In all cases, the receiver only checks for a mark condition at the center of the stop bit position (one half-bit time after the last data bit, or after the parity bit if enabled is sampled). Refer to 表 6-29 for the values. If an external 1× clock is used for the transmitter: MR2A[3] = 0 selects one stop bit MR2A[3] = 1 selects two stop bits

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表 6-28. DUART Mode Description

MODE	DESCRIPTION
Normal	The transmitter and receiver operating independently.
Automatic echo	Places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode: 1. Received data is reclocked and retransmitted on the TxDA output 2. The receive clock is used for the transmitter 3. The receiver must be enabled, but the transmitter need not be enabled 4. The channel A TxRDY and TxEMT status bits are inactive 5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received 6. Character framing is checked, but the stop bits are retransmitted as received 7. A received break is echoed as received until the next valid start bit is detected 8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled
Local loopback	Selects local loopback diagnostic mode. In this mode: 1. The transmitter output is internally connected to the receiver input 2. The transmit clock is used for the receiver 3. The TxDA output is held HIGH 4. The RxDA input is ignored 5. The transmitter must be enabled, but the receiver need not be enabled 6. CPU to transmitter and receiver communications continue normally
Remote loopback	Selects remote loopback diagnostic mode. In this mode: 1. Received data is reclocked and retransmitted on the TxDA output 2. The receive clock is used for the transmitter 3. Received data is not sent to the local CPU, and the error status conditions are inactive 4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received 5. The receiver must be enabled 6. Character framing is not checked, and the stop bits are retransmitted as received 7. A received break is echoed as received until the next valid start bit is detected

表 6-29. Stop Bit Length

MR2A[3:0] (HEXADECIMAL)	STOP BIT LENGTH(1)
0	0.563
1	0.625
2	0.688
3	0.750
4	0.813
5	0.875
6	0.938
7	1.000
8	1.563
9	1.653
A	1.688
B	1.750
C	1.813
D	1.875
E	1.938

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表 6-29. Stop Bit Length (続き)

MR2A[3:0] (HEXADECIMAL)	STOP BIT LENGTH(1)
F	2.000

(1) Add 0.5 to values shown for 0 to 7 if channel is programmed for 5 bit per character.

6.3.1.4 Mode Register 0 Channel B (MR0B)

MR0B (address 0x8) is accessed when the channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a set pointer command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except the FIFO size bit and that all control actions apply to the channel B receiver, transmitter, the corresponding inputs and outputs. MR0B[2:0] are reserved.

6.3.1.5 Mode Register 1 Channel B (MR1B)

MR1B (address 0x8) is accessed when the channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

6.3.1.6 Mode Register 2 Channel B (MR2B)

MR2B (address 0x8) is accessed when the channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

6.3.2 Clock Select Registers

表 6-30. Clock Select Register Channel A (CSRA) (Address 0x1) and Clock Select Register Channel B (CSRB) (Address 0x9) Bit Allocation

7	6	5	4	3	2	1	0
receiver clock select code				transmitter clock select code			

6.3.2.1 Clock Select Register Channel A (CSRA)

表 6-31. Clock Select Register Channel A (CSRA) (Address 0x1) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7 to 4	–	Receiver clock select. The baud rate clock for the channel A receiver is as shown in 表 6-32, except as follows: 1110 = IP4 – 16× 1111 = IP4 – 1× The receiver clock is always a 16× clock except for CSRA[7:4] = 1111
3 to 0	–	Transmitter clock select. The baud rate clock for the channel A transmitter is as shown in 表 6-32, except as follows: 1110 = IP3 – 16× 1111 = IP3 – 1× The transmitter clock is always a 16× clock except for CSRA[3:0] = 1111

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表 6-32. Baud Rate (Based on a 3.6864 MHz Crystal Clock)(1)

CSR[7:4]	MR0[0] = 0 (NORMAL MODE)		MR0[0] = 1 (EXTENDED MODE I)		MR0[2] = 1 (EXTENDED MODE II)	
CSR[3:0]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	300	450	4,800	7,200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	134.5	1,076	1,076
0011	200	150	1200	900	19.200	14.400
0100	300	300	1800	1800	28.800	28.800
0101	600	600	3600	3600	57.600	57.600
0110	1,200	1,200	7,200	7,200	115,200	115,200
0111	1,050	2,000	1,050	2,000	1,050	2,000
1000	2,400	2,400	14,400	14,400	57,600	57,600
1001	4,800	4,800	28,800	28,800	4,800	4,800
1010	7,200	1,800	7,200	1,800	57,600	14,400
1011	9,600	9,600	57,600	57,600	9,600	9,600
1100	38,400	19,200	230,400	115,200	38,400	19,200
1101	Timer	Timer	Timer	Timer	Timer	Timer

(1) See 表 6-33 for bit rate characteristics.

表 6-33. Bit Rate Generator Characteristics(1) (2)

NORMAL RATE (BAUD)	ACTUAL 16× CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4 0	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19200	307.2	0
38400	614.4	0

(1) Crystal or clock = 3.6864 MHz.
(2) Duty cycle of 16× clock is 50% ± 1%.

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6.3.2.2 Clock Select Register Channel B (CSRB)

表 6-34. Clock Select Register Channel B (CSRB) (Address 0x1) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7 to 4	–	Receiver clock select. The baud rate clock for the channel B receiver is as shown in 表 6-32, except as follows: 1110 = IP4 – 16× 1111 = IP4 – 1× The receiver clock is always a 16× clock except for CSRB[7:4] = 1111
3 to 0	–	Transmitter clock select. The baud rate clock for the channel B transmitter is as shown in 表 6-32, except as follows: 1110 = IP3 – 16× 1111 = IP3 – 1× The transmitter clock is always a 16× clock except for CSRB[3:0] = 1111

6.3.3 Command Registers

表 6-35. Command Register Channel A (CRA) (Address 0x2) and Command Register Channel B (CRB) (Address 0xA) Bit Allocation

7	6	5	4	3	2	1	0
channel command code				disable Tx	enable Tx	disable Rx	enable Rx

6.3.3.1 Command Register Channel A (CRA)

CRA is a register used to supply commands to channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

表 6-36. Command Register Channel A (CRA) (Address 0x2) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7 to 4	–	Miscellaneous commands. Execution of the commands in the upper four bits of this register must be separated by 3 X1 clock edges. Other reads or writes (including writes to the lower four bits) may be inserted to achieve this separation. A description of miscellaneous commands is given in 表 6-37.
3	–	Disable channel A transmitter. This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the Tx FIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state
2	–	Enable channel A transmitter. Enables operation of the channel A transmitter. The TxRDY and TxEMT status bits is asserted if the transmitter is idle
1	–	Disable channel A receiver. This command terminates operation of the receiver immediately-a character being received is lost. The command has no effect on the receiver status bits or any other control registers.
0	–	Enable channel A receiver. Enables operation of the channel A receiver. If not in the special wake-up mode, this also forces the receiver into the search for start-bit state

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表 6-37. Miscellaneous Commands

COMMAND	DESCRIPTION
0000	No command.
0001	Reset MR pointer. Causes the channel A MR pointer to point to MR1.
0010	Reset receiver. Resets the channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011	Reset transmitter. Resets the channel A transmitter as if a hardware reset had been applied.
0100	Reset error status. Clears the channel A received break, parity error, and overrun error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101	Reset channel A break change interrupt. Causes the channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110	Start break. Forces the TxDA output LOW (spacing). If the transmitter is empty the start of the break condition is delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the Tx FIFO, the start of the break is delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111	Stop break. The TxDA line will go HIGH (marking) within two bit times. TxDA will remain HIGH for one bit time before the next character, if any, is transmitted.
1000	Assert RTSN. Causes the RTSN output to be asserted (LOW).
1001	Negate RTSN. Causes the RTSN output to be negated (HIGH).
1010	Set time-out mode on. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the Rx FIFO. The C/T is placed in the counter mode, the start counter or stop counter commands are disabled, the counter is stopped, and the counter ready bit, ISR[3], is reset. (see also watchdog timer description in the receiver セクション 5.3.7.7.)
1011	Set MR pointer to 0x0.
1100	Disable time-out mode. This command returns control of the C/T to the regular start counter or stop counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the time-out mode, a stop counter command should be issued to force a reset of the ISR[3] bit.
1101	Not used.
1110	Power-down mode on. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable Power-down mode (1111) requires a X1/CLK. While in the Power-down mode, do not issue any commands to the CR except the disable Power-down mode command. The contents of all registers is saved while in this mode. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into Power-down mode. This command is in CRA only.
1111	Disable Power-down mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only. For maximum power reduction input pins should be at V_{SS} or V_{DD}.

6.3.3.2 Command Register Channel B (CRB)

CRB is a register used to supply commands to channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of miscellaneous commands 0xE and 0xF which are used for Power-down mode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

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6.3.4 Status Registers

6.3.4.1 Status Register Channel A (SRA)

表 6-38. Status Register Channel A (SRA) (Address 0x1) Bit Allocation

7	6	5	4	3	2	1	0
received break(1)	framing error(1)	parity error(1)	overrun error	TxEMTA	TxRDYA	RxFULLA	RxRDYA

(1) These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode they are discarded when the corresponding data character is read from the FIFO. In block error mode, the error-reset command (command 0x4 or receiver reset) must used to clear block error conditions.

表 6-39. Status Register Channel A (SRA) (Address 0x1) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	Channel A received break. 0 = no 1 = yes This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time two successive edges of the internal or external 1× clock. This will usually require a HIGH time of one X1 clock period or 3 X1 edges since the clock of the controller is not synchronous to the X1 clock. When this bit is set, the channel A change in break bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected. This bit is reset by command 0x4 (0100) written to the command register or by receiver reset.
6	–	Channel A framing error. 0 = no 1 = yes This bit, when set, indicates that a stop bit was not detected (not a logic 1) when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.
5	–	Channel A parity error. 0 = no 1 = yes This bit is set when the with parity or force parity mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multi-drop mode the parity error bit stores the receive A/D (Address/Data) bit.
4	–	Channel A overrun error. 0 = no 1 = yes This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.
3	TxEMTA	Channel A transmitter empty. 0 = no 1 = yes This bit is set when the transmitter under runs, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the under run condition.

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表 6-39. Status Register Channel A (SRA) (Address 0x1) Bit Description (続き)

BIT(S)	SYMBOL	DESCRIPTION
2	TxRDYA	Channel A transmitter ready. 0 = no 1 = yes This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the transmitter is first enabled. Characters loaded to the Tx FIFO while this bit is logic 0 is lost. This bit has different meaning from ISR[0].
1	FFULLA	Channel A FIFO full. 0 = no 1 = yes This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight (or 16) FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1[6] is programmed to a logic 1
0	RxRDYA	Channel A receiver ready. 0 = no 1 = yes This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO – the Rx FIFO becomes empty.

6.3.4.2 Status Register Channel B (SRB)

表 6-40. Status Register Channel B (SRB) (Address 0x9) Bit Allocation

7	6	5	4	3	2	1	0
received break(1)	framing error(1)	parity error(1)	overrun error	TxEMTB	TxRDYB	RxFULLB	RxRDYB

(1) These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode they are discarded when the corresponding data character is read from the FIFO. In block error mode, the error-reset command (command 0x4 or receiver reset) must used to clear block error conditions.

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the channel B receiver and transmitter and the corresponding inputs and outputs.

6.3.5 Output Configuration Control Register (OPCR)

This register controls the signal presented by the OP[7:2] pins. The signal presented by the OP[1:0] pins is controlled by the Rx, Tx, and the command register. The default condition of the OP pins is to drive the complement of the data in the OPR[7:0] register.

When OP[7:2] pins drive DMA or interrupt type signals, they switch to open-drain configuration. Otherwise, they drive strong logic 0 or logic 1 levels

表 6-41. Output Configuration Control Register (OPCR) (Address 0xD) Bit Allocation

7	6	5	4	3	2	1	0
configure OP7	configure OP6	configure OP5	configure OP4	configure OP3	configure OP2	configure OP1	configure OP0

表 6-42. Output Configuration Control Register (OPCR) (Address 0xD) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	OP7 output select 0 = The complement of OPR[7] 1 = The channel B transmitter interrupt output which is the complement of ISR[4]. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

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表 6-42. Output Configuration Control Register (OPCR) (Address 0xD) Bit Description (続き)

BIT(S)	SYMBOL	DESCRIPTION
6	–	OP6 output select 0 = The complement of OPR[6] 1 = The channel A transmitter interrupt output which is the complement of ISR[0]. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.
5	–	OP5 output select 0 = The complement of OPR[5] 1 = The channel B receiver interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.
4	–	OP4 output select 0 = The complement of OPR[4] 1 = The channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.
3 and 2	–	OP3 output select 00 = The complement of OPR[3] 01 = The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains HIGH until terminal count is reached, at which time it goes LOW. The output returns to the HIGH state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR. 10 = The 1× clock for the channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1× clock is output. 11 = The 1× clock for the channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1× clock is output.
1 and 0	–	OP2 output select 00 = The complement of OPR[2] 01 = The 16× clock for the channel A transmitter. This is the clock selected by CSRA[3:0], and is a 1× clock if CSRA[3:0] = 1111. 10 = The 1× clock for the channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1× clock is output. 11 = The 1× clock for the channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1× clock is output.

6.3.6 Set Output Port Bits Register (SOPR)

Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect. This allows software to set individual bits without keeping a copy of the OPR bit configuration.

表 6-43. Set Output Port Bits Register (SOPR) (Address 0xE) Bit Allocation

7	6	5	4	3	2	1	0
set OP7	set OP6	set OP5	set OP4	set OP3	set OP2	set OP1	set OP0

表 6-44. Set Output Port Bits Register (SOPR) (Address 0xE) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	OPR7 1 = set bit 0 = no change
6	–	OPR6 1 = set bit 0 = no change
5	–	OPR5 1 = set bit 0 = no change
4	–	OPR4 1 = set bit 0 = no change
3	–	OPR3 1 = set bit 0 = no change

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表 6-44. Set Output Port Bits Register (SOPR) (Address 0xE) Bit Description (続き)

BIT(S)	SYMBOL	DESCRIPTION
2	–	OPR2 1 = set bit 0 = no change
1	–	OPR1 1 = set bit 0 = no change
0	–	OPR0 1 = set bit 0 = no change

6.3.7 Reset Output Port Bits Register (ROPR)

Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect. This allows software to reset individual bits without keeping a copy of the OPR bit configuration.

表 6-45. Reset Output Port Bits Register (ROPR) (Address 0xF) Bit Allocation

7	6	5	4	3	2	1	0
reset OP7	reset OP6	reset OP5	reset OP4	reset OP3	reset OP2	reset OP1	reset OP0

表 6-46. Reset Output Port Bits Register (ROPR) (Address 0xF) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	OPR7 1 = reset bit 0 = no change
6	–	OPR6 1 = reset bit 0 = no change
5	–	OPR5 1 = reset bit 0 = no change
4	–	OPR4 1 = reset bit 0 = no change
3	–	OPR3 1 = reset bit 0 = no change
2	–	OPR2 1 = reset bit 0 = no change
1	–	OPR1 1 = reset bit 0 = no change
0	–	OPR0 1 = reset bit 0 = no change

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6.3.8 Output Port Register (OPR)

The output pins (OP pins) drive the complement of the data in this register as controlled by SOPR and ROPR.

表 6-47. Output Port Bits Register (OPR) (No Address) Bit Allocation

7	6	5	4	3	2	1	0
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0

表 6-48. Output Port Bits Register (OPR) (Address 0xF) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	pin OP7 0 = pin HIGH 1 = pin LOW
6	–	pin OP6 0 = pin HIGH 1 = pin LOW
5	–	pin OP5 0 = pin HIGH 1 = pin LOW
4	–	pin OP4 0 = pin HIGH 1 = pin LOW
3	–	pin OP3 0 = pin HIGH 1 = pin LOW
2	–	pin OP2 0 = pin HIGH 1 = pin LOW
1	–	pin OP1 0 = pin HIGH 1 = pin LOW
0	–	pin OP0 0 = pin HIGH 1 = pin LOW

6.3.9 Auxiliary Control Register (ACR)

表 6-49. Auxiliary Control Register (ACR) (Address 0x4) Bit Allocation

7	6	5	4	3	2	1	0
BRG set select	counter/timer mode and clock source select			enable IP3 COS interrupt	enable IP2 COS interrupt	enable IP1 COS interrupt	enable IP0 COS interrupt

表 6-50. Auxiliary Control Register (ACR) (Address 0x4) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	Baud rate generator set select. This bit selects one of two sets of baud rates to be generated by the BRG (see 表 6-32). The selected set of rates is available for use by the channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in 表 6-33.
6 to 4	–	Counter/timer mode and clock source select. This field selects the operating mode of the counter/timer and its clock source as shown in 表 6-51.
3 to 0	–	IP3, IP2, IP1 and IP0 change-of-state interrupt enable. 0 = off 1 = enabled This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR [7]) to be set. If a bit is in the enabled state the setting of the corresponding bit in the IPCR will also result in the setting of ISR [7], which results in the generation of an interrupt output if IMR [7] = 1. If a bit is in the off state, the setting of that bit in the IPCR has no effect on ISR [7].

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表 6-51. ACR[6:4] Field Definition(1)

ACR[6:4]	MODE	CLOCK SOURCE
000	Counter	External IP2
001	Counter	TxCA – 1× clock of channel A transmitter
010	Counter	TxCB – 1× clock of channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

(1) The timer mode generates a square wave.

6.3.10 Input Port Change Register (IPCR)

表 6-52. Input Port Change Register (IPCR) (Address 0x4) Bit Allocation

7	6	5	4	3	2	1	0
ΔIP3	ΔIP2	ΔIP1	ΔIP0	state of IP3	state of IP2	state of IP1	state of IP0

表 6-53. Input Port Change Register (IPCR) (Address 0x4) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7 to 4	–	IP3, IP2, IP1 and IP0 change of state. 0 = no change 1 = change These bits are set when a change of state, as defined in セクション 5.3.6.9, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.
3 to 0	–	IP3, IP2, IP1 and IP0 state. 0 = LOW 1 = HIGH These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

6.3.11 Interrupt Status Register (ISR)

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a logic 1 and the corresponding bit in the IMR is also a logic 1, the INTRN output is asserted (LOW). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR. The true status is provided regardless of the contents of the IMR. The contents of this register are initialized to 0x0 when the DUART is reset.

表 6-54. Interrupt Status Register (ISR) (Address 0x5) Bit Allocation

7	6	5	4	3	2	1	0
change input port	change break B	RxRDYB	TxRDYB	counter ready	change break A	RxRDYA	TxRDYA

表 6-55. Interrupt Status Register (ISR) (Address 0x5) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	Input port change status. 0 = not active 1 = active This bit is a logic 1 when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

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表 6-55. Interrupt Status Register (ISR) (Address 0x5) Bit Description (続き)

BIT(S)	SYMBOL	DESCRIPTION
6	–	Channel B change in break. 0 = not active 1 = active This bit, when set, indicates that the channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B reset break change interrupt command.
5	RxRDYB	RxB interrupt. 0 = not active 1 = active This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers or the watchdog timer has timed-out. This bit has a different meaning than the receiver ready/full bit in the status register.
4	TxRDYB	TxB interrupt. 0 = not active 1 = active This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the TxRDY bit in the status register.
3	–	Counter ready. 0 = not active 1 = active In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.
2	–	Channel A change in break. 0 = not active 1 = active This bit, when set, indicates that the channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel A reset break change interrupt command.
1	RxRDYA	RxA interrupt. 0 = not active 1 = active This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers or the watchdog timer has timed-out. This bit has a different meaning than the receiver ready/full bit in the status register.
0	TxRDYA	TxA interrupt. 0 = not active 1 = active This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the TxRDY bit in the status register.

6.3.12 Interrupt Mask Register (IMR)

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a logic 1 and the corresponding bit in the IMR is also a logic 1 the INTRN output is asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3 to OP7 or the reading of the ISR.

表 6-56. Interrupt Mask Register (IMR) (Address 0x5) Bit Allocation

7	6	5	4	3	2	1	0
input port change	change break B	RxRDYB FFULLB	TxRDYB	counter ready	change break A	RxRDYA FFULLA	TxRDYA

表 6-57. Interrupt Mask Register (IMR) (Address 0x5) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7	–	Input port change. 0 = not enabled 1 = enabled

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表 6-57. Interrupt Mask Register (IMR) (Address 0x5) Bit Description (続き)

BIT(S)	SYMBOL	DESCRIPTION
6	–	Channel B change in break. 0 = not enabled 1 = enabled
5	RxRDYB FFULLB	RxB interrupt. 0 = not enabled 1 = enabled
4	TxRDYB	TxB interrupt. 0 = not enabled 1 = enabled
3	–	Counter ready. 0 = not enabled 1 = enabled
2	–	Channel A change in break. 0 = not enabled 1 = enabled
1	RxRDYA FFULLA	RxA interrupt. 0 = not enabled 1 = enabled
0	TxRDYA	TxA interrupt. 0 = not enabled 1 = enabled

6.3.13 Interrupt Vector Register (IVR; 68xxx Mode) or General Purpose Register (GP; 80xxx Mode)

This register stores the Interrupt Vector. It is initialized to 0x0F on hardware reset and is usually changed from this value during initialization of the TL28L92. The contents of this register is placed on the data bus when IACKN is asserted LOW or a read of address 0xC is performed.

When not operating in the 68xxx mode, this register may be used as a general purpose one byte storage register. A convenient use could be to store a shadow of the contents of another TL28L92 register (IMR, for example).

表 6-58. Interrupt Vector Register (IVR; 68xxx Mode) or General Purpose Register (GP; 80xxx Mode) (Address 0xc) Bit Allocation

7	6	5	4	3	2	1	0
interrupt vector (68xxx mode) or one byte storage (80xxx mode)							

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6.3.14 Counter and Timer Registers

表 6-59. Counter and Timer Preset Upper (CTPU) (Address 0x6) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7:0	–	The upper eight (8) bits for the 16-bit counter/timer preset register

表 6-60. Counter and Timer Preset Lower (CTPL) (Address 0x7) Bit Description

BIT(S)	SYMBOL	DESCRIPTION
7:0	–	The lower eight (8) bits for the 16-bit counter/timer preset register

The CTPU and CTPL hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTPU/CTPL registers is 0x0002. Note that these registers are write only and cannot be read by the CPU.

In the timer mode, the C/T generates a square wave whose period is twice the value (in C/T clock periods) of the CTPU and CTPL. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTPU and CTPL for a particular 1× data clock is:

$$n = \frac{\textit{counter/timer clock frequency}}{2 \times 16 \times \textit{(desired baud rate)}} \tag{2}$$

Often, this division results in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14 %; well within the ability asynchronous mode of operation.

The C/T dose not run until it receives an initial start counter command (read at address A3 to A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3 to A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTPU and CTPL. If the value in CTPU and CTPL is changed, the current half-period will not be affected, but subsequent half periods is affected.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3 to A0 = 1111). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output. In the counter mode, the value C/T loaded into CTPU and CTPL by the CPU is counted down to 0. Counting begins upon receipt of a start counter command. Upon reaching terminal count 0x0000, the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains HIGH until terminal count is reached, at which time it goes LOW. The output returns to the HIGH state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTPU and CTPL at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTPU and CTPL.

When the C/T clock divided by 16 is selected, the maximum divisor becomes 1,048,575.

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6.4 Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register. The OPCR register controls the source of the data for the output ports OP2 to OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register.

The content of the OPR register is controlled by the Set Output Port bits command and the Reset Output Port bits command. These commands are at 0xE and 0xF, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a logic 1 in bit location 5 of the data word used with the Set Output Port bits command will result in OPR5 being set to one. The OP5 would then be set to logic 0 (V_{SS}). Similarly, a logic 1 in bit position 5 of the data word associated with the Reset Output Ports bits command would set OPR5 to logic 0 and, hence, the pin OP5 to a logic 1 (V_{DD}).

6.5 CTS, RTS, CTS Enable Tx Signals

Clear To Send (CTS) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active LOW; thus, it is called CTSAN for TxA and CTSBN for TxB. RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active LOW and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output is usually connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire.

MR2[4] is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven HIGH, the transmitter stops sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that is connected to the transmitter CTS input. The receiver is set RTS HIGH when the receiver FIFO is full AND the start bit of the 9th or 17th character is sensed. Transmission then stops with 9 or 17 valid characters in the receiver. When MR2[4] is set to one, CTSN must be at zero for the transmitter to operate. If MR2[4] is set to zero, the IP pin has no effect on the operation of the transmitter. MR1[7] is the bit that allows the receiver to control OP0. The value of the pin is set when OP0 (or OP1) is controlled by the receiver.

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7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

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7.2 サポート・リソース

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7.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2009) to Revision C (April 2024)	Page
• ドキュメントをデータ マニュアルからデータシート フォーマットに変更	1
• 次の「特長」リストから項目を削除:「SC28L92 ピン互換」、「マルチドロップ モード ...」、「自動ウェークアップ モード ...」および「電源をオンにして SC26C92 をエミュレート」	1
• データシート全体にわたって SC26C92 への参照を削除	1
• Deleted the RGZ package from the *Pin Configurations and Functions*	3
• Deleted the Wake-Up Mode Timing image from the *Timing Diagrams*	14
• Deleted the *Multi-Drop Mode (9-Bit or Wake-Up)* section	29
• Deleted "11 = multi-drop special mode" from bit 4 in 表 6-25	34
• Deleted multi-drop text from bit 2 in 表 6-25	34
• Deleted multi-drop text from bit 1 in 表 6-36	40
• Deleted multi-drop text from bit 5 in 表 6-39	42

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Changes from Revision A (October 2008) to Revision B (August 2009)	Page
• Changes made to pin names in 図 3-2	3

Changes from Revision * (August 2008) to Revision A (October 2008)	Page
• ドキュメントのステータスを:製品プレビューから:「量産データ」に変更	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL28L92FR	Obsolete	Production	QFP (FR) | 44	-	-	Call TI	Call TI	0 to 70	TL28L92
TL28L92FR.B	Obsolete	Production	QFP (FR) | 44	-	-	Call TI	Call TI	0 to 70	TL28L92
TL28L92IFR	Obsolete	Production	QFP (FR) | 44	-	-	Call TI	Call TI	-40 to 85	TL28L92I
TL28L92IFR.B	Obsolete	Production	QFP (FR) | 44	-	-	Call TI	Call TI	-40 to 85	TL28L92I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

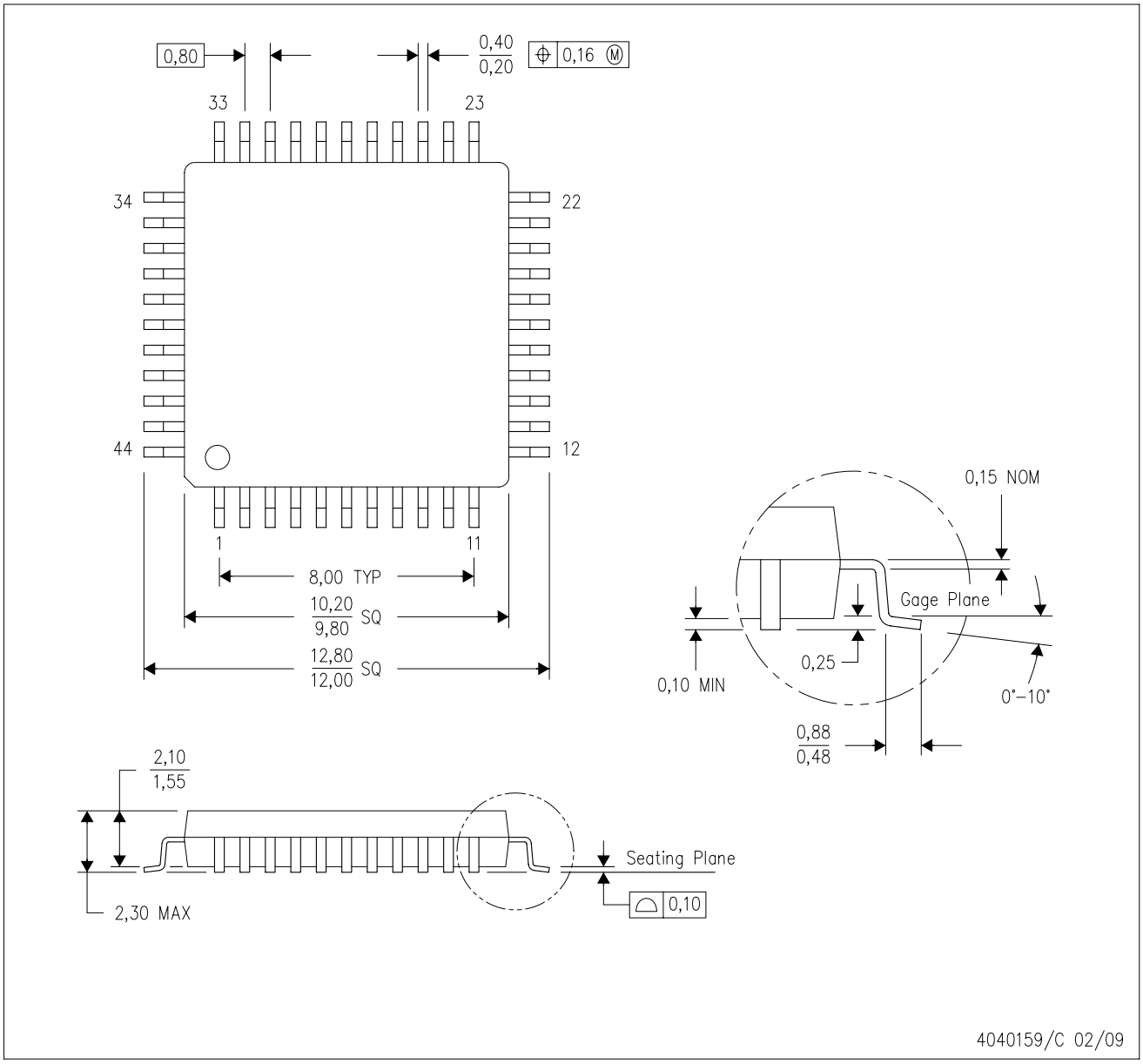
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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FR (S–PQFP–G44) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

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