TLC2272M-MIL 高度なLinCMOSレール・ツー・レール・オペアンプ

1 特長

- 出力スイングに両方の電源レールを含む
- 低ノイズ: f = 1kHz時に9nV/√Hz (標準値)
- 低い入力バイアス電流: 1pA (標準値)
- 単一電源と分割電源での動作を完全に規定
- 同相入力電圧範囲に負のレールを含む
- 高いゲイン帯域幅: 2.2MHz (標準値)
- 高いスルー・レート: 3.6V/μs (標準値)
- 低い入力オフセット電圧: T_A = 25℃時に2.5mV (最大値)
- マクロモデル内蔵
- TLC272およびTLC274の性能強化版
- Q-Temp車載用で利用可能

2 アプリケーション

- 白物家電(冷蔵庫、洗濯機)
- ハンドヘルド監視システム
- 構成制御と印刷のサポート
- トランスデューサ・インターフェイス
- バッテリ駆動のアプリケーション

3 概要

TLC2272M-MILデバイスは、テキサス・インスツルメンツ製のデュアル・オペアンプです。このデバイスはレール・ツー・レールの出力性能があり、単一および分割電源アプリケーションでダイナミック・レンジが増大します。TLC2272M-MILデバイスは2MHzの帯域幅と3V/μsのスルー・レートを実現しており、高速アプリケーションに適しています。このデバイスは既存のCMOSオペアンプと同等のAC性能を備えながら、ノイズ、入力オフセット電圧、消費電力の点でCMOSオペアンプより優れています。TLC2272M-MILデバイスのノイズ電圧は9nV/√Hzで、競合ソリューションの半分です。

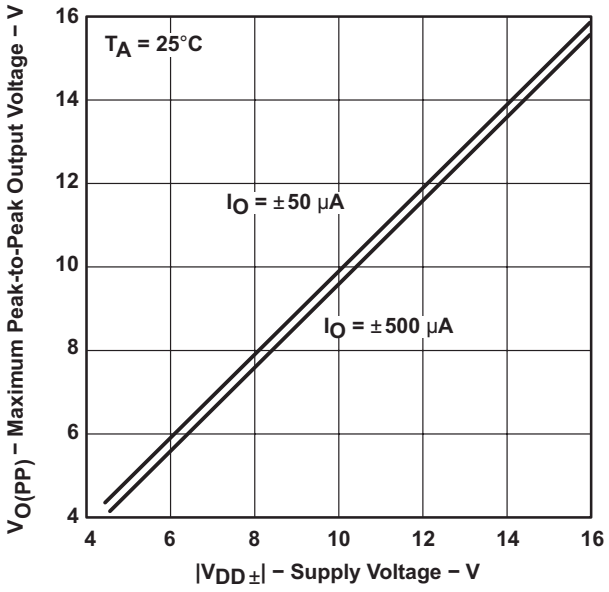
TLC2272M-MILデバイスは入力インピーダンスが高く、ノイズが低いため、圧電性トランスデューサなど高インピーダンスのソース用の小信号コンディショニングに最適です。Micropowerの消費電力レベルであるため、ハンドヘルドの監視機器やリモート・センシング・アプリケーションで適切に動作します。さらに、単一または分割電源でレール・ツー・レール出力が可能なため、このデバイスはA/Dコンバータ(ADC)と接続するための優れた選択肢です。高精度のアプリケーション向けには、最大入力オフセット電圧950μVのTLC2272AM-MILデバイスが利用可能です。このデバイスは5Vおよび±5Vで完全に動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLC2272M-MIL	SOIC (8)	3.91mm×4.90mm
	CDIP (8)	6.67mm×9.60mm
	LCCC (20)	8.89mm×8.89mm
	CFP (10)	6.35mm×6.35mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

最大ピーク・ツー・ピーク出力電圧と電源電圧との関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 概要（続き） ... 3
6 **Pin Configuration and Functions** ... 4
7 **Specifications** ... 6
7.1 Absolute Maximum Ratings ... 6
7.2 ESD Ratings ... 6
7.3 Recommended Operating Conditions ... 6
7.4 Thermal Information ... 6
7.5 TLC2272M-MIL Electrical Characteristics V_{DD} = 5 V 7
7.6 TLC2272M-MIL Electrical Characteristics V_{DD}± = ±5 V ... 9
7.7 Typical Characteristics ... 11
8 **Detailed Description** ... 21
8.1 Overview ... 21
8.2 Functional Block Diagram ... 21
8.3 Feature Description ... 21
8.4 Device Functional Modes ... 21
9 **Application and Implementation** ... 22
9.1 Application Information ... 22
9.2 Typical Application ... 23
10 **Power Supply Recommendations** ... 25
11 **Layout** ... 26
11.1 Layout Guidelines ... 26
11.2 Layout Example ... 26
12 デバイスおよびドキュメントのサポート ... 27
12.1 ドキュメントの更新通知を受け取る方法 ... 27
12.2 コミュニティ・リソース ... 27
12.3 商標 ... 27
12.4 静電気放電に関する注意事項 ... 27
12.5 Glossary ... 27
13 メカニカル、パッケージ、および注文情報 ... 27

4 改訂履歴

日付	改訂内容	注
2017年6月	*	初版

Copyright © 2017, Texas Instruments Incorporated

5 概要（続き）

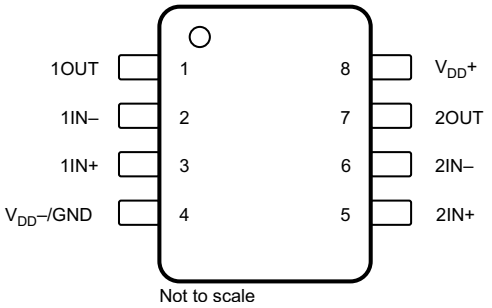
TLC2272M-MILデバイスは、標準設計におけるTLC272のアップグレードとしても優れており、出力ダイナミック・レンジの増大、ノイズ電圧の低下、入力オフセット電圧の低下を実現できます。これらの拡張機能セットから、広範なアプリケーションで使用可能です。高い出力駆動能力と、広い入力電圧範囲を必要とするアプリケーション向けには、TLV2432およびTLV2442デバイスを参照してください。

設計で必要なアンプが1つだけの場合は、TLV2211、TLV2221、TLV2231ファミリを参照してください。これらのデバイスは単一のレール・ツー・レール・オペアンプで、SOT-23パッケージで供給されます。サイズが小さく、消費電力が低いため、高密度のバッテリ駆動機器に最適です。

Copyright © 2017, Texas Instruments Incorporated

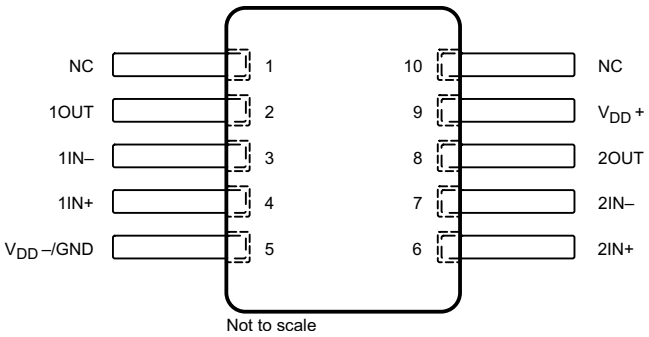
6 Pin Configuration and Functions

D or JG Package
8-Pin SOIC or CDIP
Top View



Not to scale

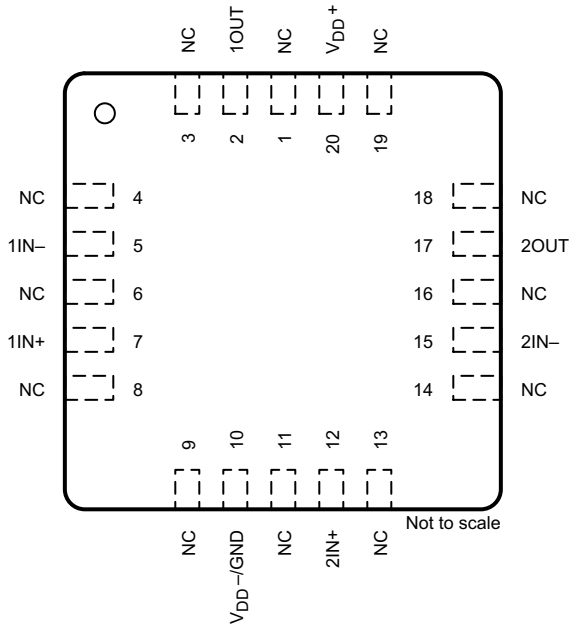
U Package
10-Pin CFP
Top View



Not to scale

NC – No internal connection

FK Package
20-Pin LCCC
Top View



Not to scale

NC – No internal connection

Copyright © 2017, Texas Instruments Incorporated

Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	D or JG	FK	U		
1IN+	3	7	4	I	Non-inverting input, Channel 1
1IN–	2	5	3	I	Inverting input, Channel 1
1OUT	1	2	2	O	Output, Channel 1
2IN+	5	12	6	I	Non-inverting input, Channel 2
2IN–	6	15	7	I	Inverting input, Channel 2
2OUT	7	17	8	O	Output, Channel 2
V_{DD}+	8	20	9	—	Positive (highest) supply
V_{DD}–	—	—	—	—	Negative (lowest) supply
V_{DD}–/GND	4	10	5	—	Negative (lowest) supply
NC	—	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	1, 10	—	No connection

Copyright © 2017, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}+(2)		8	V
V_{DD}–(2)	–8		V
Differential input voltage, V_{ID}(3)		±16	V
Input voltage, V_I (any input)(2)	V_{DD}– – 0.3	V_{DD}+	V
Input current, I_I (any input)		±5	mA
Output current, I_O		±50	mA
Total current into V_{DD}+		±50	mA
Total current out of V_{DD}–		±50	mA
Duration of short-circuit current at (or below) 25°C(4)	Unlimited		
Operating ambient temperature range, T_A	–55	125	
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD}+ and V_{DD}–.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD}– – 0.3 V.
(4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	Devices in D packages	±2000	V
	Charged-device model (CDM), per AEC Q100-011	Devices in D packages	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}±	Supply voltage	±2.2	±8	V
V_I	Input voltage	V_{DD}–	V_{DD}+ – 1.5	V
V_{IC}	Common-mode input voltage	V_{DD}–	V_{DD}+ – 1.5	V
T_A	Operating ambient temperature	–55	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLC2272M-MIL				UNIT
		D (SOIC)	JG (CDIP)	FK (LCCC)	U (CFP)	
		8-PIN		20-PIN	10-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	115.6		—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)(3)	61.8		18	121.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9		—	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3		—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.4		—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—		—	8.68	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

Copyright © 2017, Texas Instruments Incorporated

7.5 TLC2272M-MIL Electrical Characteristics V_{DD} = 5 V

at specified ambient temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	T_A = 25°C			300	2500	µV
			T_A = –55°C to 125°C				3000	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(1)	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	T_A = 25°C			0.5	60	pA
			T_A = –55°C to 125°C				800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	T_A = 25°C			1	60	pA
			T_A = –55°C to 125°C				800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\|V_{IO}\|$ ≤ 5 mV	T_A = 25°C		–0.3	2.5	4	V
			T_A = –55°C to 125°C		0	2.5	3.5	
V_{OH}	High-level output voltage	I_{OH} = –20 µA				4.99		V
		I_{OH} = –200 µA	T_A = 25°C		4.85	4.93		
			T_A = –55°C to 125°C		4.85			
		I_{OH} = –1 mA	T_A = 25°C		4.25	4.65		
			T_A = –55°C to 125°C		4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA			0.01		V
			I_{OL} = 500 µA	T_A = 25°C		0.09	0.15	
				T_A = –55°C to 125°C			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				T_A = –55°C to 125°C			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ(2)	T_A = 25°C		10	35		V/mV
			T_A = –55°C to 125°C		10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 1 MΩ(2)				175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	T_A = 25°C		70	75		dB
			T_A = –55°C to 125°C		70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load	T_A = 25°C		80	95		dB
			T_A = –55°C to 125°C		80			
I_{DD}	Supply currrent	V_O = 2.5 V, no load	T_A = 25°C			2.2	3	mA
			T_A = –55°C to 125°C				3	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ(2), C_L = 100 pF(2)	T_A = 25°C		2.3	3.6		V/µs
			T_A = –55°C to 125°C		1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ(2)	A_V = 1			0.0013%		
			A_V = 10			0.004%		
			A_V = 100			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ(2), C_L = 100 pF(2)				2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ(2), C_L = 100 pF(2)				1		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ(2), Step = 0.5 V to 2.5 V, C_L = 100 pF(2)	To 0.1%			1.5		µs
			To 0.01%			2.6		

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 0 V.

Copyright © 2017, Texas Instruments Incorporated

TLC2272M-MIL Electrical Characteristics V_{DD} = 5 V (continued)

at specified ambient temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
φ_m	Phase margin at unity gain	R_L = 10 kΩ(2), C_L = 100 pF(2)		50		°
	Gain margin	R_L = 10 kΩ(2), C_L = 100 pF(2)		10		dB

Copyright © 2017, Texas Instruments Incorporated

7.6 TLC2272M-MIL Electrical Characteristics V_{DD}± = ±5 V

at specified ambient temperature, V_{DD}± = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		300	2500	µV
				T_A = –55°C to 125°C			3000	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(1)	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		0.5	60	pA
				T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		1	60	pA
				T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\lvert V_{IO} \rvert$ ≤ 5 mV		T_A = 25°C	–5.3	0	4	V
				T_A = –55°C to 125°C	–5	0	3.5	
V_{OM}+	Maximum positive peak output voltage	I_O = –20 µA				4.99		V
		I_O = –200 µA		T_A = 25°C	4.85	4.93		
				T_A = –55°C to 125°C	4.85			
		I_O = –1 mA		T_A = 25°C	4.25	4.65		
				T_A = –55°C to 125°C	4.25			
V_{OM}–	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 µA			–4.99		V
			I_O = 500 µA	T_A = 25°C	–4.85	–4.91		
				T_A = –55°C to 125°C	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				T_A = –55°C to 125°C	–3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V; R_L = 10 kΩ		T_A = 25°C	20	50		V/mV
				T_A = –55°C to 125°C	20			
		V_O = ±4 V; R_L = 1 MΩ				300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				T_A = –55°C to 125°C	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				T_A = –55°C to 125°C	80			
I_{DD}	Supply currrent	V_O = 0 V, no load		T_A = 25°C		2.4	3	mA
				T_A = –55°C to 125°C			3	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		T_A = 25°C	2.3	3.6		V/µs
				T_A = –55°C to 125°C	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ		A_V = 1		0.0011%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF				2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF				0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF		To 0.1%		1.5		µs
				To 0.01%		3.2		
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF				52		°

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

Copyright © 2017, Texas Instruments Incorporated

TLC2272M-MIL Electrical Characteristics V_{DD}± = ±5 V (continued)

at specified ambient temperature, V_{DD}± = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain margin	R_L = 10 kΩ, C_L = 100 pF		10		dB

Copyright © 2017, Texas Instruments Incorporated

7.7 Typical Characteristics

Table 1. Table of Graphs

			FIGURE (1)
V_{IO}	Input offset voltage	Distribution	1, 2
		vs Common-mode voltage	3, 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5, 6 (2)
I_{IB} / I_{IO}	Input bias and input offset current	vs ambient temperature	7 (2)
V_I	Input voltage	vs Supply voltage	8
		vs ambient temperature	9 (2)
V_{OH}	High-level output voltage	vs High-level output current	10 (2)
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12 (2)
V_{OM+}	Maximum positive peak output voltage	vs Output current	13 (2)
V_{OM-}	Maximum negative peak output voltage	vs Output current	14 (2)
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15
I_{OS}	Short-circuit output current	vs Supply voltage	16
		vs ambient temperature	17 (2)
V_O	Output voltage	vs Differential input voltage	18, 19
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	20
	Large-signal differential voltage amplification and phase margin	vs Frequency	21, 22
	Large-signal differential voltage amplification	vs ambient temperature	23 (2), 24 (2)
z_0	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency	27
		vs ambient temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	29, 30
		vs ambient temperature	31 (2)
I_{DD}	Supply current	vs Supply voltage	32 (2), (2)
		vs ambient temperature	33 (2), (2)
SR	Slew rate	vs Load Capacitance	34
		vs ambient temperature	35 (2)
V_O	Inverting large-signal pulse response		36, 37
	Voltage-follower large-signal pulse response		38, 39
	Inverting small-signal pulse response		40, 41
	Voltage-follower small-signal pulse response		42, 43
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage over a 10-second period		46
	Integrated noise voltage	vs Frequency	47
THD+N	Total harmonic distortion + noise	vs Frequency	48
	Gain-bandwidth product	vs Supply voltage	49
		vs ambient temperature	50 (2)
φ_m	Phase margin	vs Load capacitance	51
	Gain margin	vs Load capacitance	52

(1) For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.
(2) Data at high and low temperatures are applicable only within the rated operating ambient temperature range of the device.

Copyright © 2017, Texas Instruments Incorporated

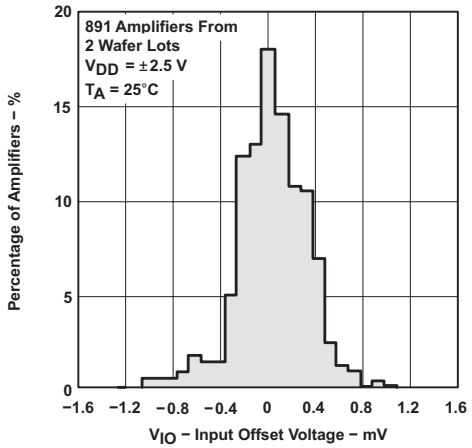


Figure 1. Distribution of Input Offset Voltage

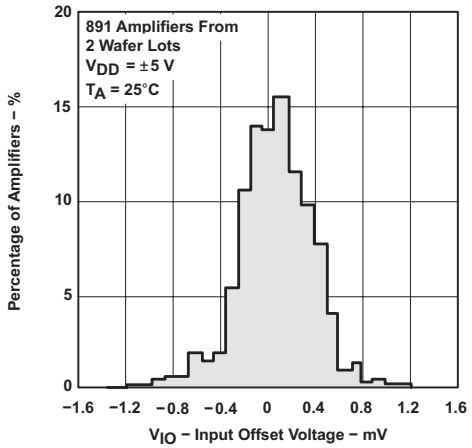


Figure 2. Distribution of Input Offset Voltage

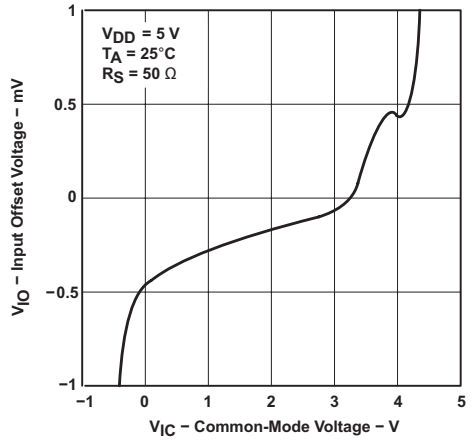


Figure 3. Input Offset Voltage vs Common-Mode Voltage

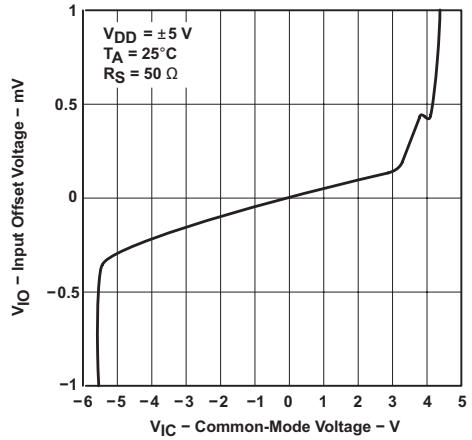


Figure 4. Input Offset Voltage vs Common-Mode Voltage

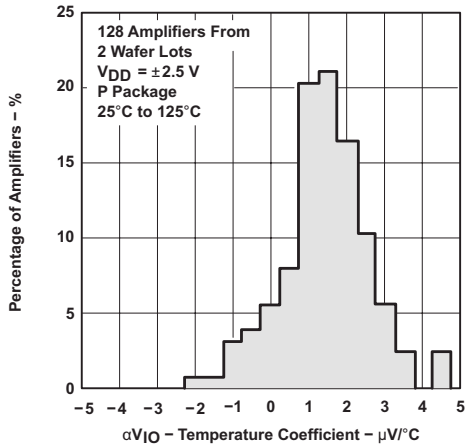


Figure 5. Distribution of Amplifiers vs Input Offset Voltage Temperature Coefficient

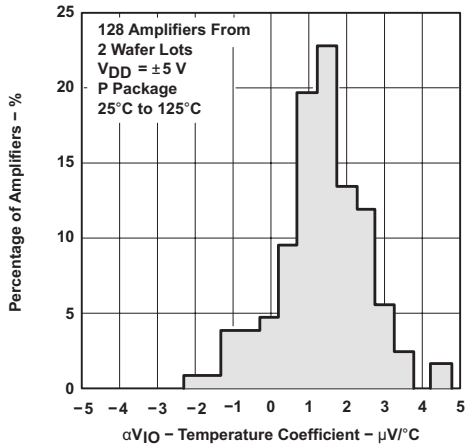


Figure 6. Distribution of Amplifiers vs Input Offset Voltage Temperature Coefficient

Copyright © 2017, Texas Instruments Incorporated

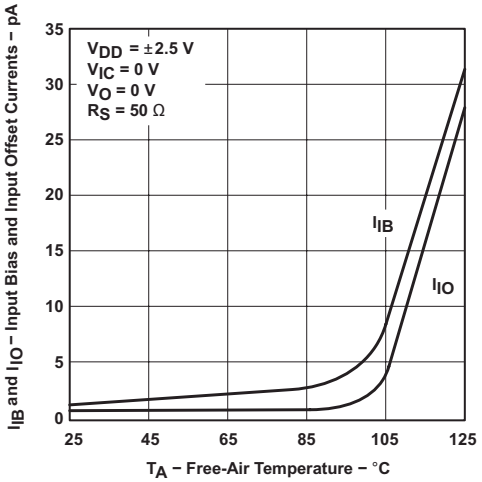


Figure 7. Input Bias and Input Offset Current vs Ambient Temperature

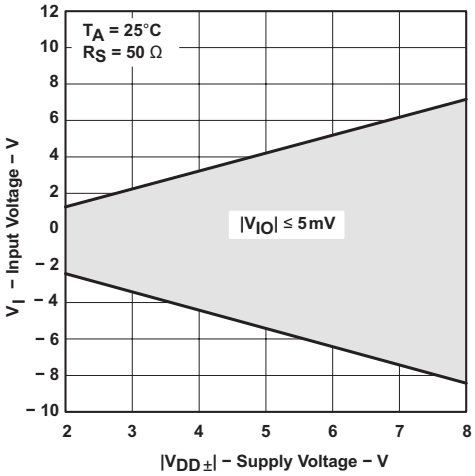


Figure 8. Input Voltage vs Supply Voltage

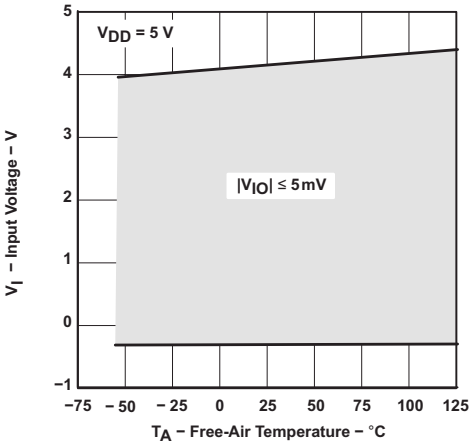


Figure 9. Input Voltage vs Ambient Temperature

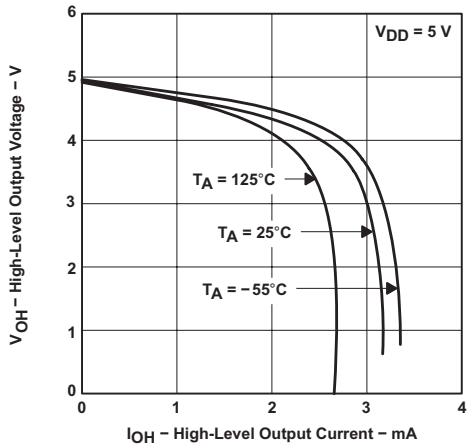


Figure 10. High-Level Output Voltage vs High-Level Output Current

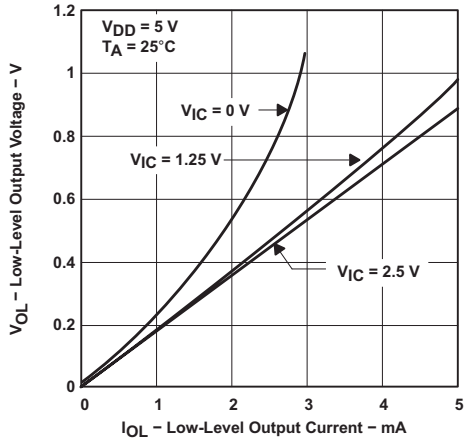


Figure 11. Low-Level Output Voltage vs Low-Level Output Current

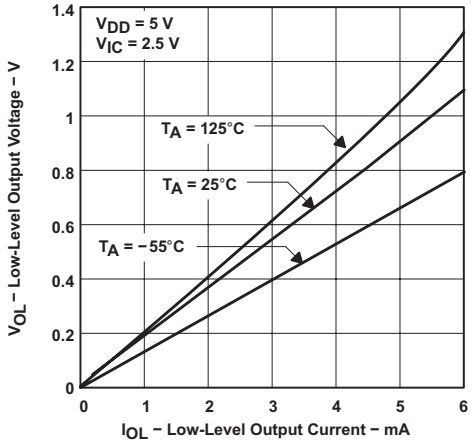


Figure 12. Low-Level Output Voltage vs Low-Level Output Current

Copyright © 2017, Texas Instruments Incorporated

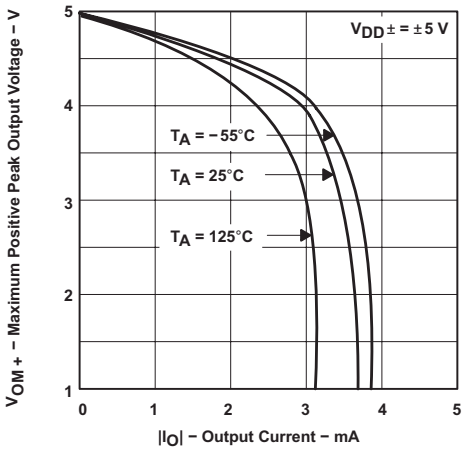


Figure 13. Maximum Positive Peak Output Voltage vs Output Current

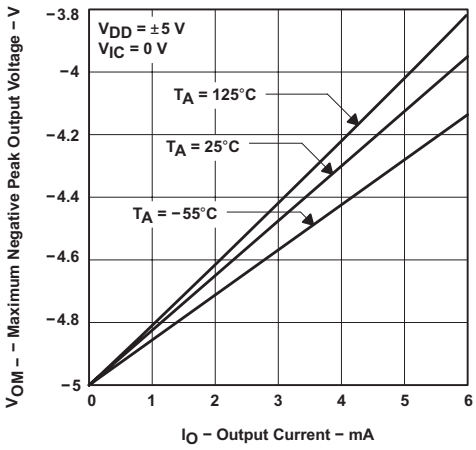


Figure 14. Maximum Negative Peak Output Voltage vs Output Current

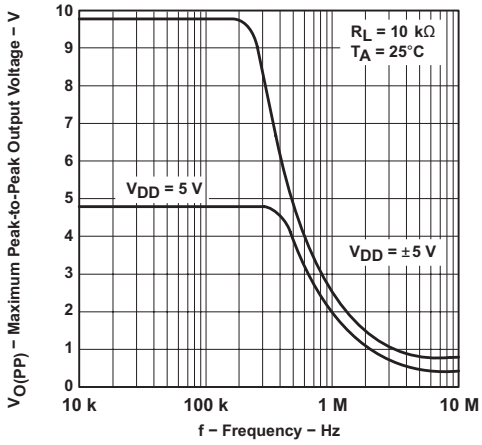


Figure 15. Maximum Peak-to-Peak Output Voltage vs Frequency

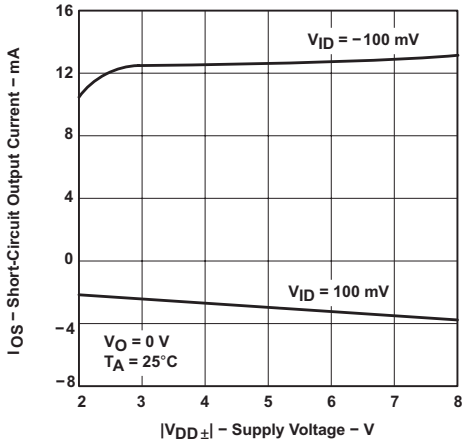


Figure 16. Short-Circuit Output Current vs Supply Voltage

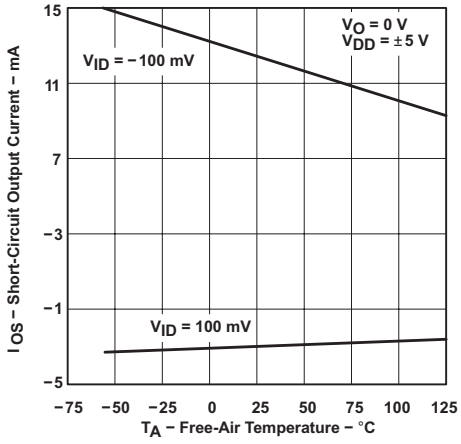


Figure 17. Short-Circuit Output Current vs Ambient Temperature

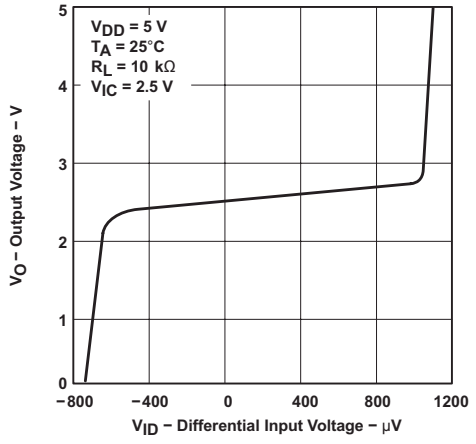


Figure 18. Output Voltage vs Differential Input Voltage

Copyright © 2017, Texas Instruments Incorporated

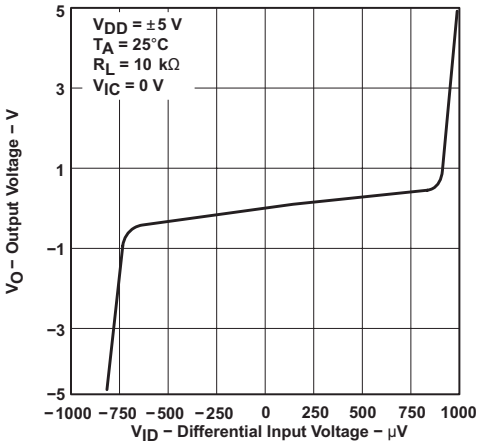


Figure 19. Output Voltage vs Differential Input Voltage

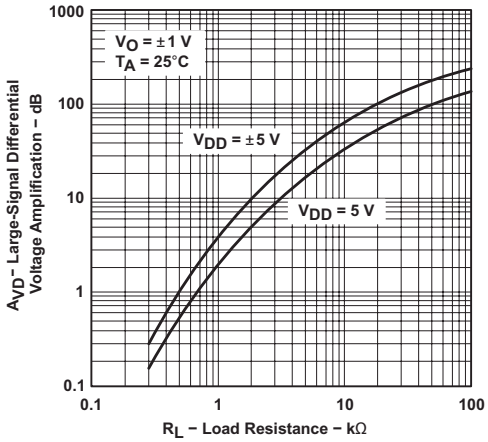


Figure 20. Large-Signal Differential Voltage Amplification vs Load Resistance

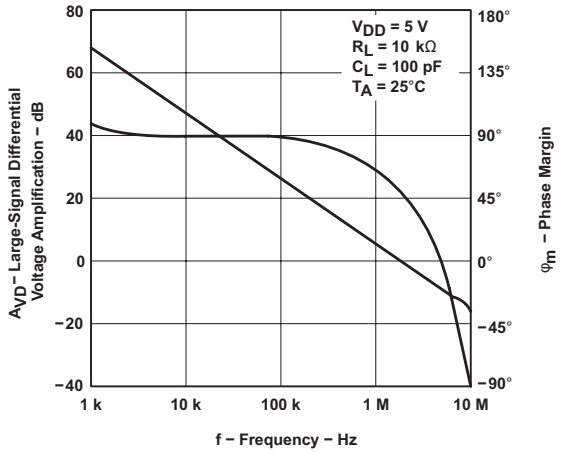


Figure 21. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

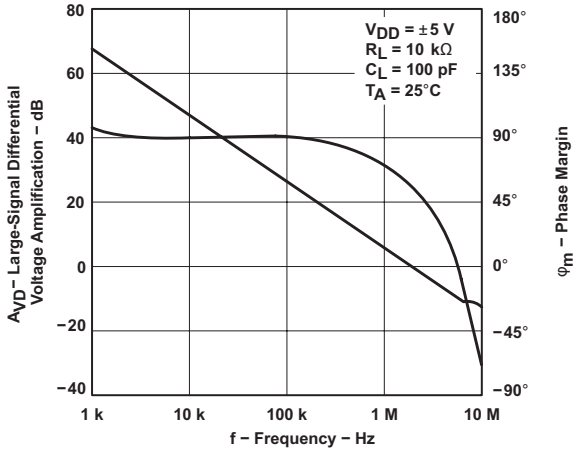


Figure 22. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

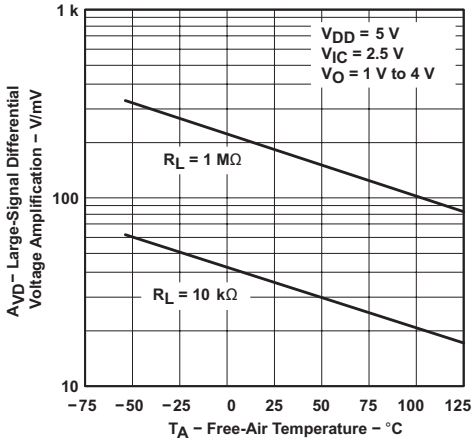


Figure 23. Large-Signal Differential Voltage Amplification vs Ambient Temperature

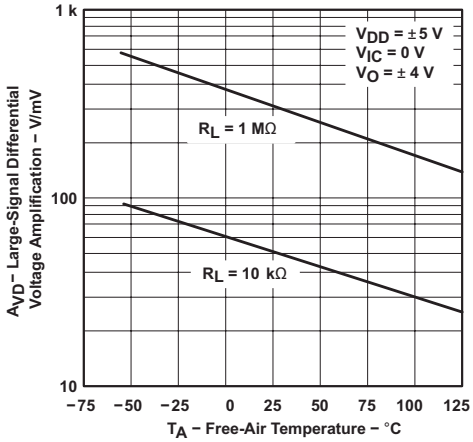


Figure 24. Large-Signal Differential Voltage Amplification vs Ambient Temperature

Copyright © 2017, Texas Instruments Incorporated

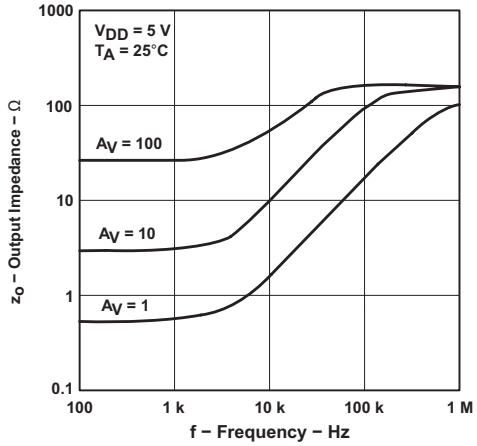


Figure 25. Output Impedance vs Frequency

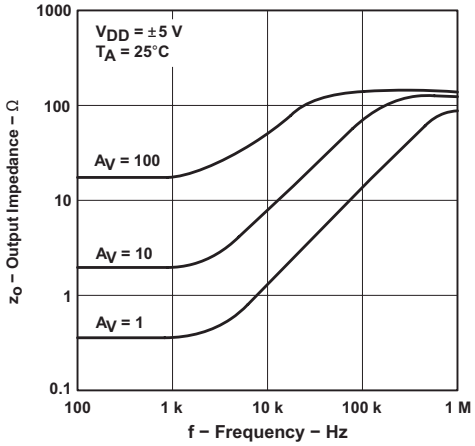


Figure 26. Output Impedance vs Frequency

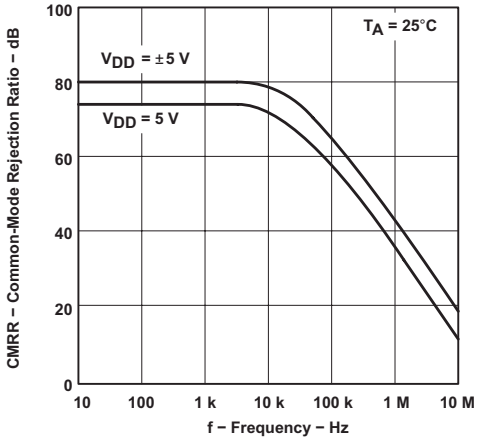


Figure 27. Common-Mode Rejection Ratio vs Frequency

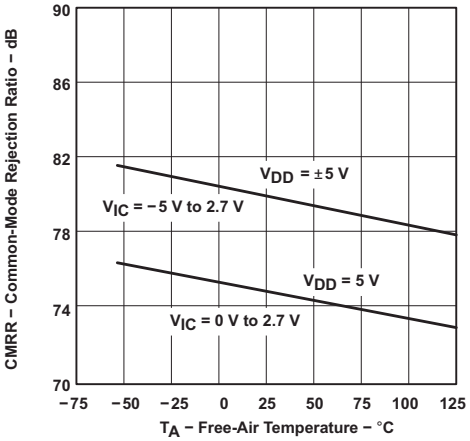


Figure 28. Common-Mode Rejection Ratio vs Ambient Temperature

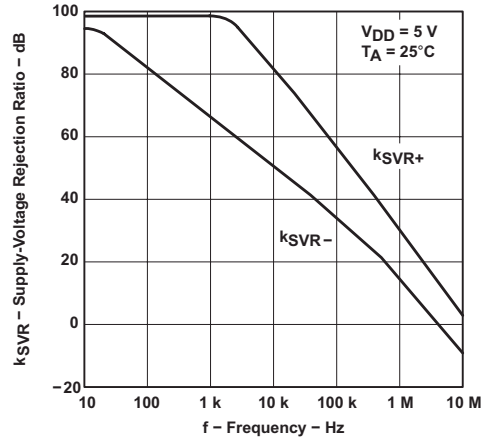


Figure 29. Supply-Voltage Rejection Ratio vs Frequency

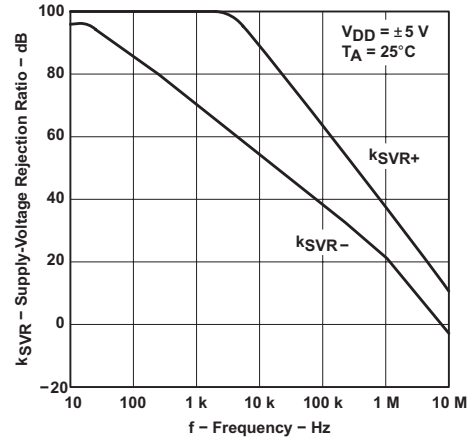


Figure 30. Supply-Voltage Rejection Ratio vs Frequency

Copyright © 2017, Texas Instruments Incorporated

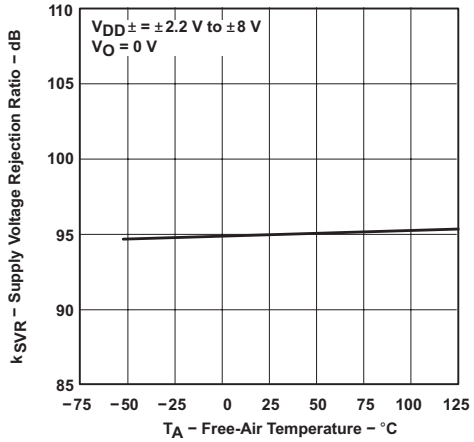


Figure 31. Supply-Voltage Rejection Ratio vs Ambient Temperature

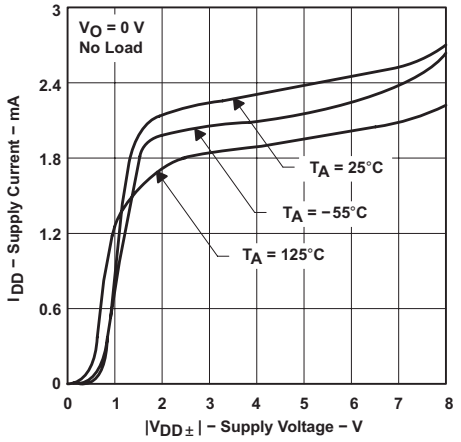


Figure 32. Supply Current vs Supply Voltage

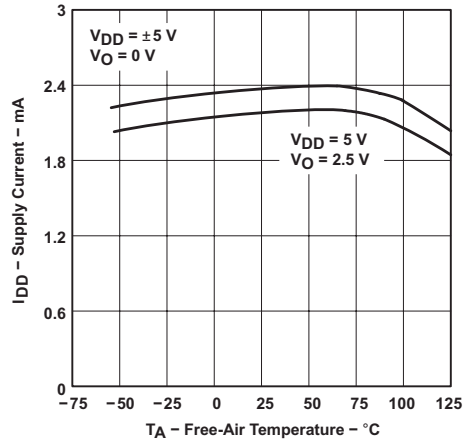


Figure 33. Supply Current vs Ambient Temperature

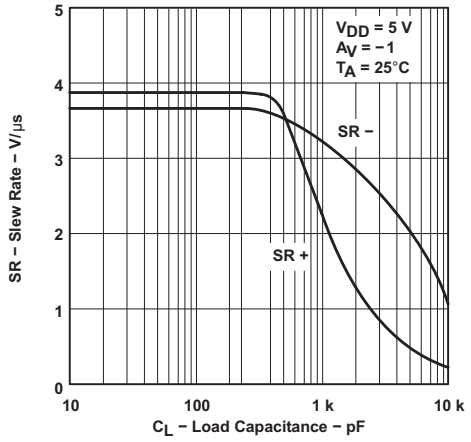


Figure 34. Slew Rate vs Load Capacitance

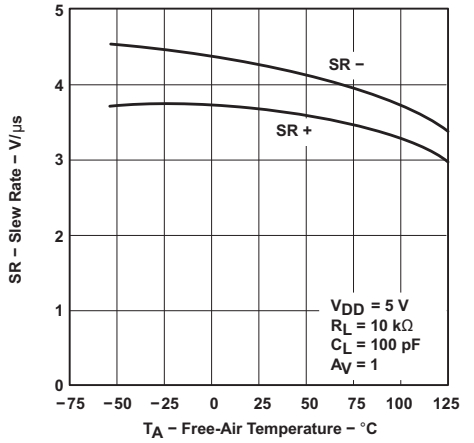


Figure 35. Slew Rate vs Ambient Temperature

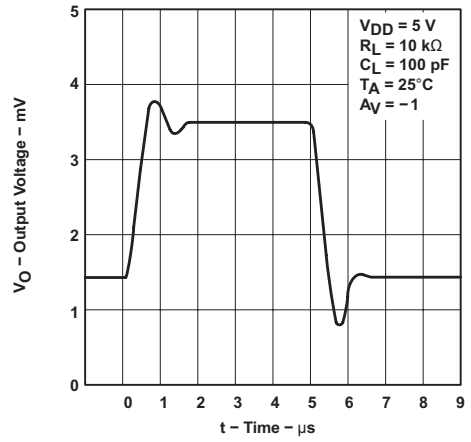


Figure 36. Inverting Large-Signal Pulse Response

Copyright © 2017, Texas Instruments Incorporated

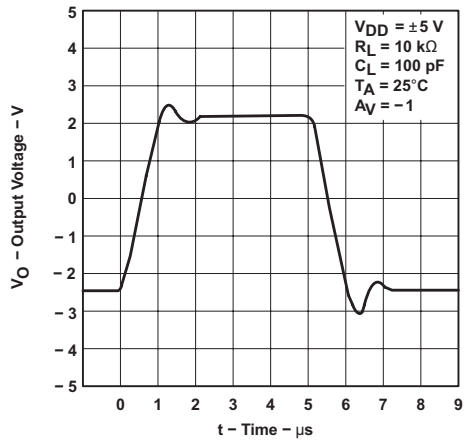


Figure 37. Inverting Large-Signal Pulse Response

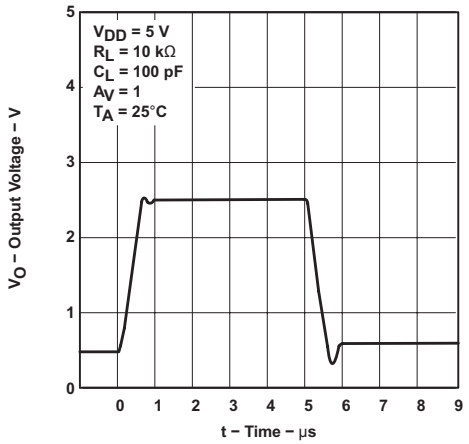


Figure 38. Voltage-Follower Large-Signal Pulse Response

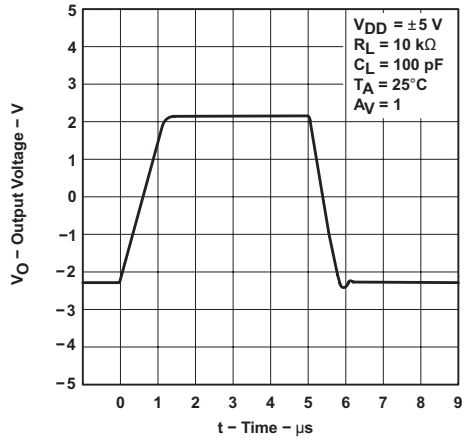


Figure 39. Voltage-Follower Large-Signal Pulse Response

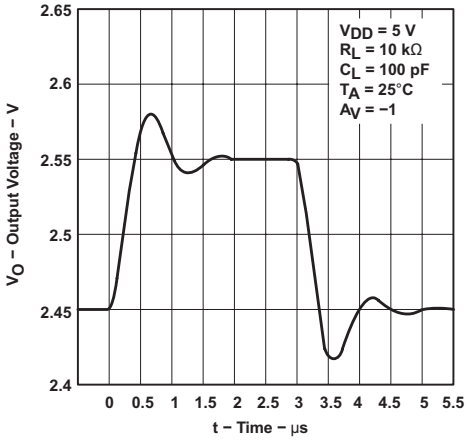


Figure 40. Inverting Small-Signal Pulse Response

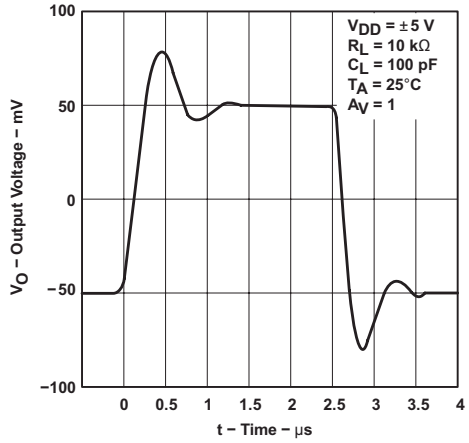


Figure 41. Inverting Small-Signal Pulse Response

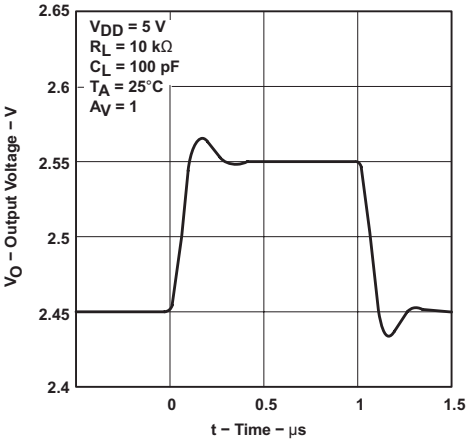


Figure 42. Voltage-Follower Small-Signal Pulse Response

Copyright © 2017, Texas Instruments Incorporated

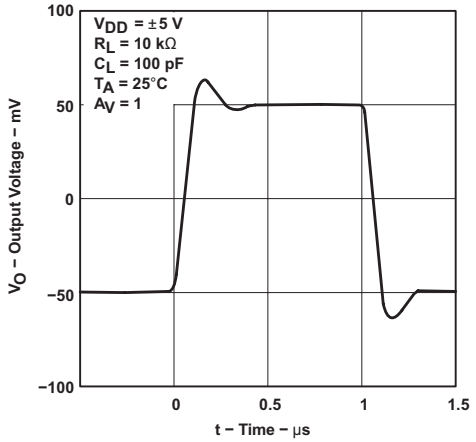


Figure 43. Voltage-Follower Small-Signal Pulse Response

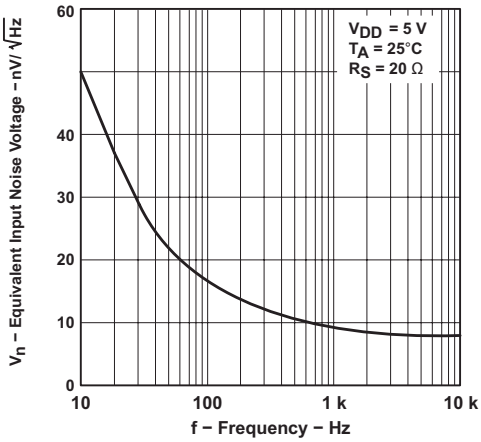


Figure 44. Equivalent Input Noise Voltage vs Frequency

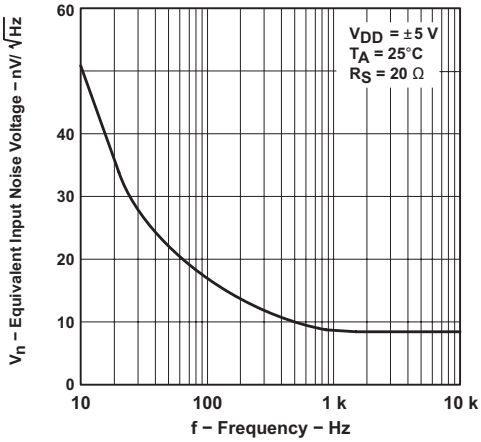


Figure 45. Equivalent Input Noise Voltage vs Frequency

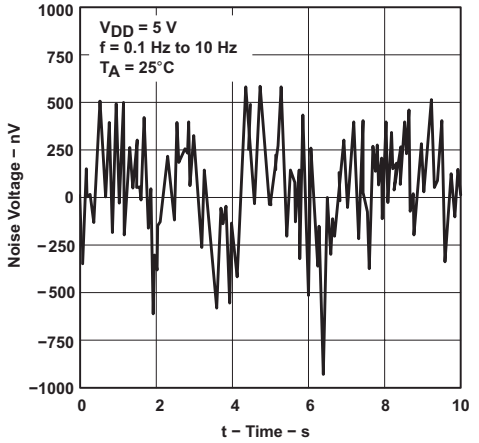


Figure 46. Noise Voltage Over a 10-Second Period

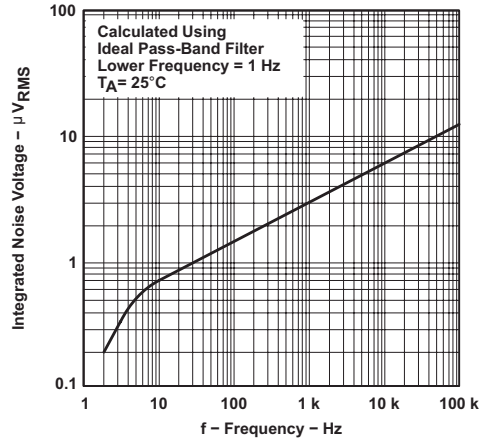


Figure 47. Integrated Noise Voltage vs Frequency

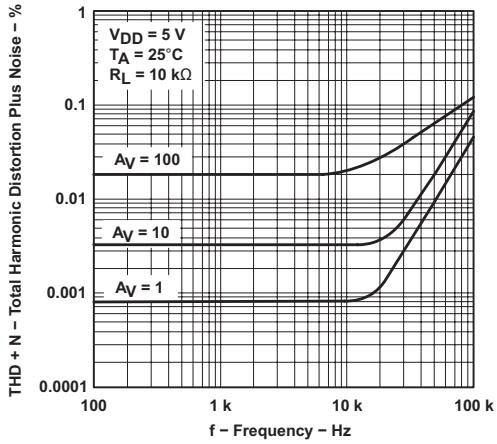


Figure 48. Total Harmonic Distortion + Noise vs Frequency

Copyright © 2017, Texas Instruments Incorporated

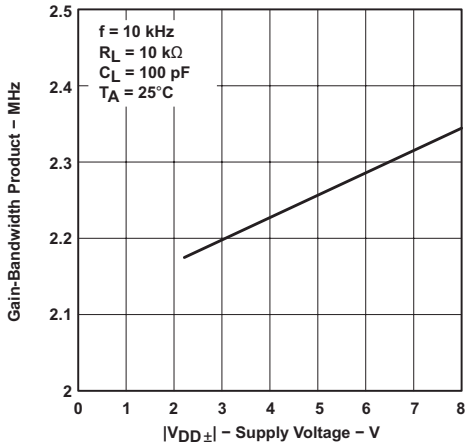


Figure 49. Gain-Bandwidth Product vs Supply Voltage

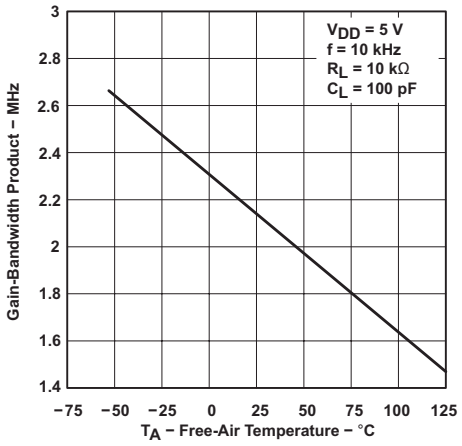


Figure 50. Gain-Bandwidth Product vs Ambient Temperature

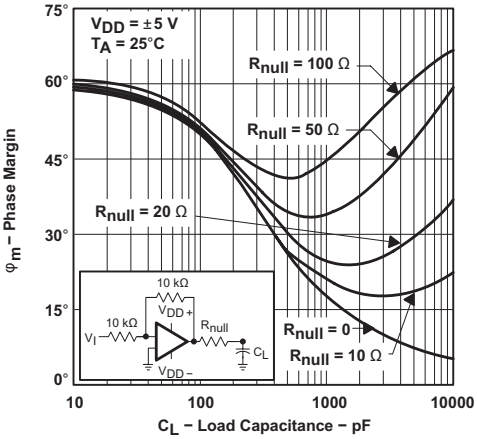


Figure 51. Phase Margin vs Load Capacitance

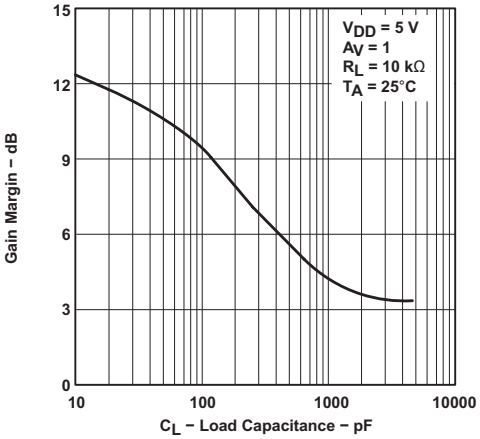


Figure 52. Gain Margin vs Load Capacitance

Copyright © 2017, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The TLC2272M-MIL device is a rail-to-rail output operational amplifier. The device operates from a 4.4-V to 16-V single supply or ±2.2-V to ±8-V dual supply, is unity-gain stable, and is suitable for a wide range of general-purpose applications.

8.2 Functional Block Diagram

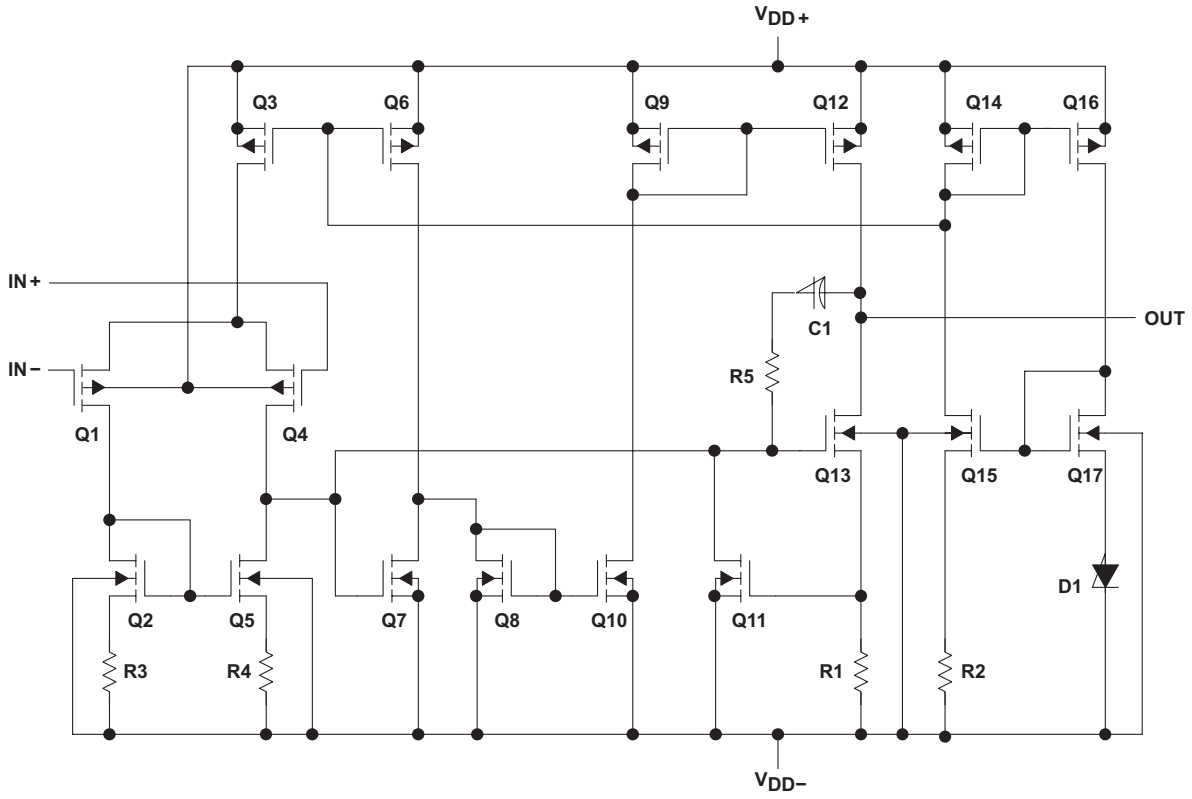


Table 2. Device Component Count(1)

COMPONENT	COUNT
Transistors	38
Resistors	26
Diodes	9
Capacitors	3

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

8.3 Feature Description

The TLC2272M-MIL device features 2-MHz bandwidth and voltage noise of 9 nV/$\sqrt{\text{Hz}}$ with performance rated from 4.4 V to 16 V across a temperature range of –55°C to 125°C). LinMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

8.4 Device Functional Modes

The TLC2272M-MIL device is powered on when the supply is connected. The device may operate with single or dual supply, depending on the application. The device is in its full-performance mode once the supply is above the recommended value.

Copyright © 2017, Texas Instruments Incorporated

9 Application and Implementation

NOTE

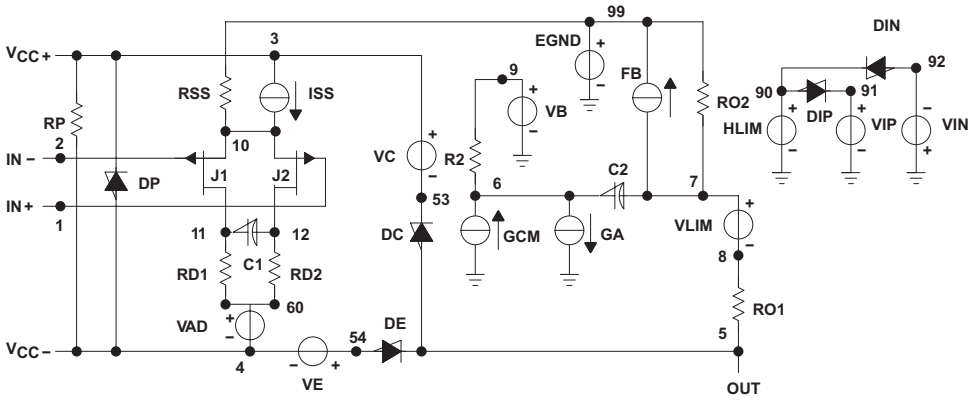
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts™, the model generation software used with MicroSim PSpice™. The Boyle macromodel (1) and subcircuit in Figure 53 were generated using the TLC2272M-MIL typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLC227x 1 2 3 4 5
C1      11      12      1214E−12
C2      6       7       760.00E−12
DC      5       53      53DX
DE      54      5       5DX
DLP     90      91      91DX
DLN     92      90      90DX
DP      4       3       3DX
EGND    99      0       0POLY (2) (3,0) (4,) 0 .5 .5
FB      99      0       0POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 −1E6 1E6 1E6 −1E6
GA      6       0       011 12 377.0E−6
GCM 0 6 10 99 134E−9
ISS     3       10      10DC 216.OE−6
HLIM    90      0       0VLIM 1K
J1      11      1       210 JX
J2      12      10      110 JX
R2      6       9       9100.OE3
RD1     60      11      112.653E3
RD2     60      12      122.653E3
R01     8       5       550
R02     7       99      9950
RP      3       2       44.310E3
RSS     10      99      99925.9E3
VAD     60      4       −.5
VB      9       0       0DC 0
VC 3 53 DC .78
VE      54      4       4DC .78
VLIM    7       8       8DC 0
VLP     91      0       0DC 1.9
VLN     0       92      92DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 53. Boyle Macromodel and Subcircuit

(1) *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

Copyright © 2017, Texas Instruments Incorporated

9.2 Typical Application

9.2.1 High-Side Current Monitor

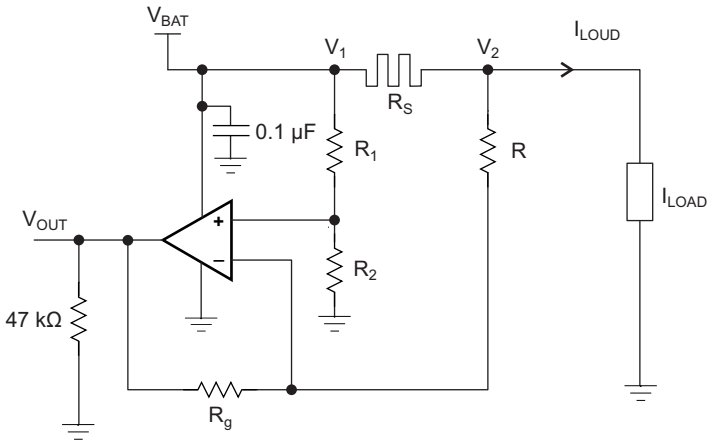


Figure 54. Equivalent Schematic (Each Amplifier)

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER		VALUE
V_{BAT}	Battery voltage	12 V
R_{SENSE}	Sense resistor	0.1 Ω
I_{LOAD}	Load current	0 A to 10 A
	Operational amplifier	Set in differential configuration with gain = 10

9.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

9.2.1.2.1 Differential Amplifier Equations

Equation 1 and Equation 2 are used to calculate V_{OUT}.

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times\frac{V_1+V_2}{2}+\frac{1+\frac{1}{2}\left(\frac{R_1}{R_2}+\frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}(V_1-V_2)\right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times V_{BAT}+\frac{1+\frac{1}{2}\left(\frac{R_1}{R_2}+\frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}\times R_S\times I_{Load}\right) \quad (2)$$

In an ideal case $R_1 = R$ and $R_2 = R_g$, and V_{OUT} can then be calculated using Equation 3:

$$V_{OUT} = \frac{R_g}{R}\times R_S\times I_{Load} \quad (3)$$

Copyright © 2017, Texas Instruments Incorporated

However, as the resistors have tolerances, they cannot be perfectly matched.

$R_1 = R \pm \Delta R_1$

$R_2 = R_2 \pm \Delta R_2$

$R = R \pm \Delta R$

$R_g = R_g \pm \Delta R_g$

$$Tol = \frac{DR}{R} \tag{4}$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by Equation 5.

$$V_{OUT} = \pm (4\ Tol)\frac{R_g}{R + R_g} \times V_{BAT} + \left(1 \pm 2\ Tol\left(1 + \frac{2R}{R + R_g}\right)\right)\frac{R_g}{R} \times R_S \times I_{LOAD}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1%

(5)

If the resistors are perfectly matched, then Tol = 0 and V_{OUT} is calculated using Equation 6.

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \tag{6}$$

The highest error is from the common mode, as shown in Equation 7.

$$4\ (Tol)\frac{R_g}{R + R_g} \times V_{BAT} \tag{7}$$

Gain of 10, R_g / R = 10, and Tol = 1%:

Common mode error = ((4 × 0.01) / 1.1) × 12 V = 0.436 V

Gain of 10 and Tol = 0.1%:

Common mode error = 43.6 mV

The resistors were chosen from 2% batches.

R_1 and R 12 kΩ

R_2 and R_g 120 kΩ

Ideal Gain = 120 / 12 = 10

The measured value of the resistors:

R_1 = 11.835 kΩ

R = 11.85 kΩ

R_2 = 117.92 kΩ

R_g = 118.07 kΩ

Copyright © 2017, Texas Instruments Incorporated

9.2.1.3 Application Curves

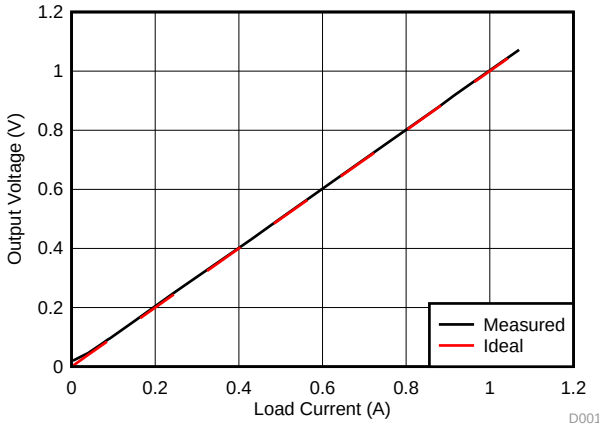


Figure 55. Output Voltage Measured vs Ideal (0 to 1 A)

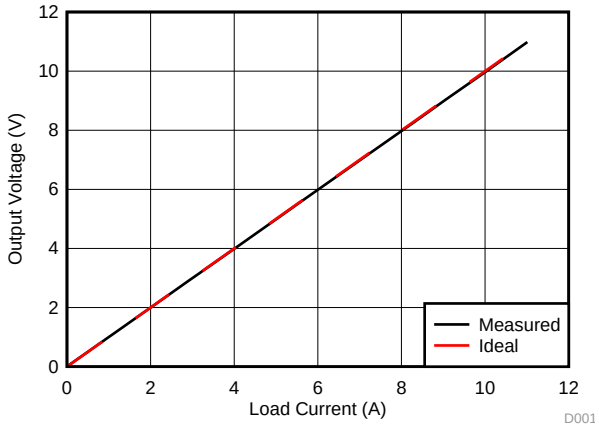


Figure 56. Output Voltage Measured vs Ideal (0 to 10 A)

10 Power Supply Recommendations

Supply voltage for a single supply is from 4.4 V to 16 V, and from ±2.2 V to ±8 V for a dual supply. In the high-side sensing application, the supply is connected to a 12-V battery.

Copyright © 2017, Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

The TLC2272M-MIL device is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-μF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

11.2 Layout Example

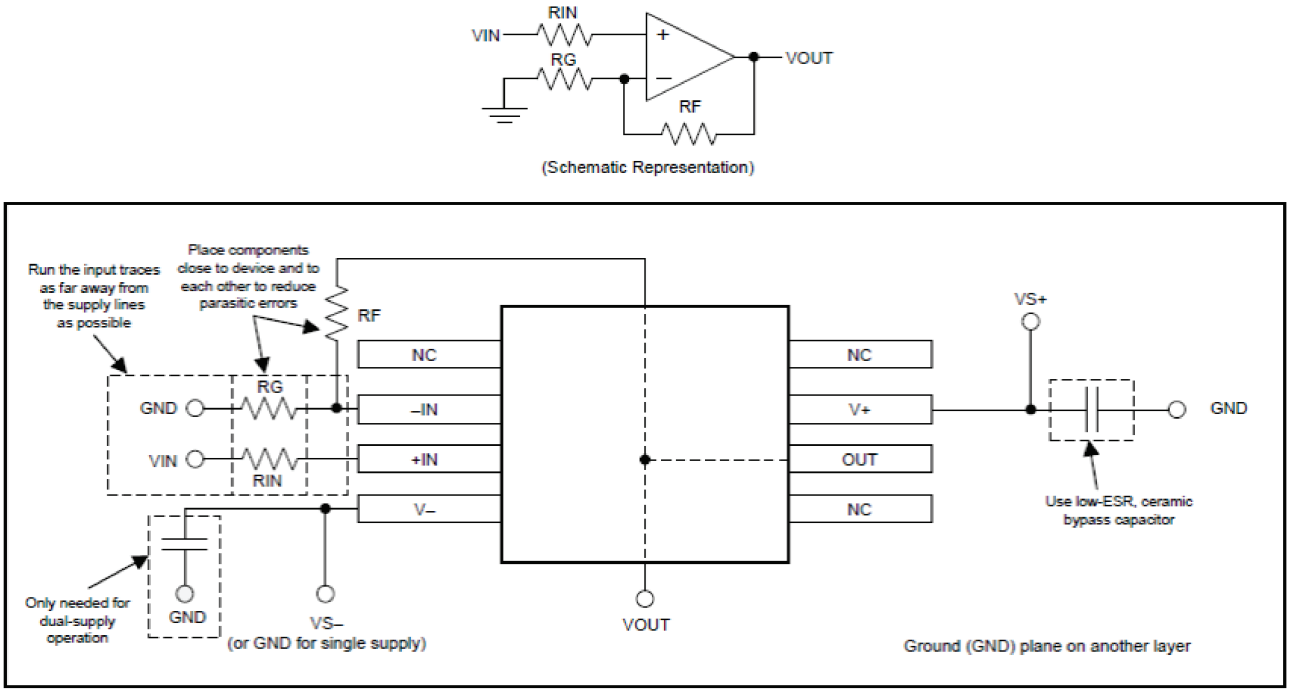


Figure 57. Layout Example

Copyright © 2017, Texas Instruments Incorporated

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.3 商標

E2E is a trademark of Texas Instruments.
MicroSim Parts, PSpice are trademarks of MicroSim.
All other trademarks are the property of their respective owners.

12.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9555201NXD	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2272M
5962-9555201NXDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2272M
5962-9555201NXDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2272M
5962-9555201Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9555201Q2A TLC2272 MFKB
5962-9555201QHA	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555201QHA TLC2272M
5962-9555201QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555201QPA TLC2272M
TLC2272MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9555201Q2A TLC2272 MFKB
TLC2272MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9555201Q2A TLC2272 MFKB
TLC2272MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC2272MJG
TLC2272MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC2272MJG
TLC2272MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555201QPA TLC2272M
TLC2272MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555201QPA TLC2272M
TLC2272MUB	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555201QHA TLC2272M
TLC2272MUB.A	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555201QHA TLC2272M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

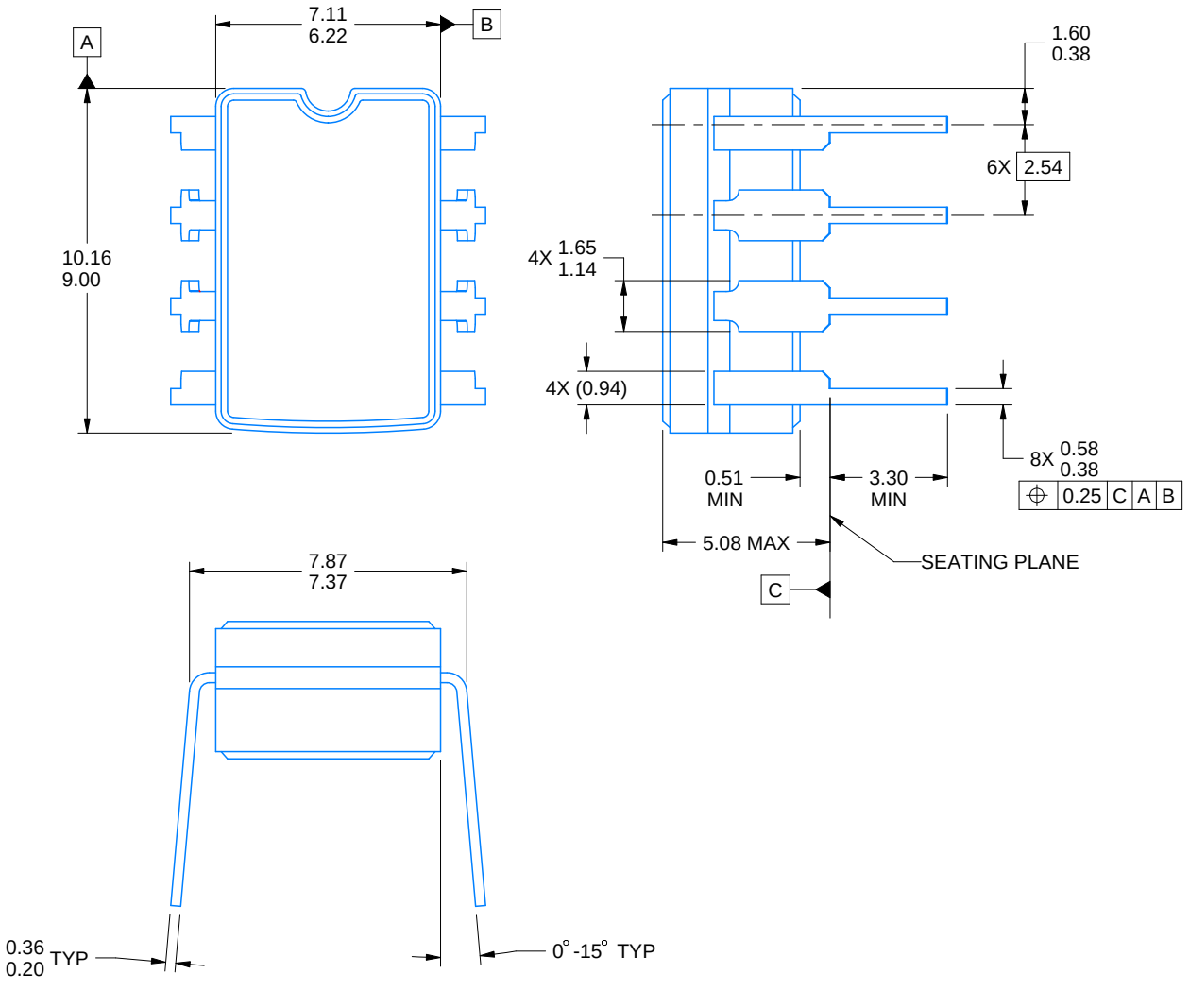
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

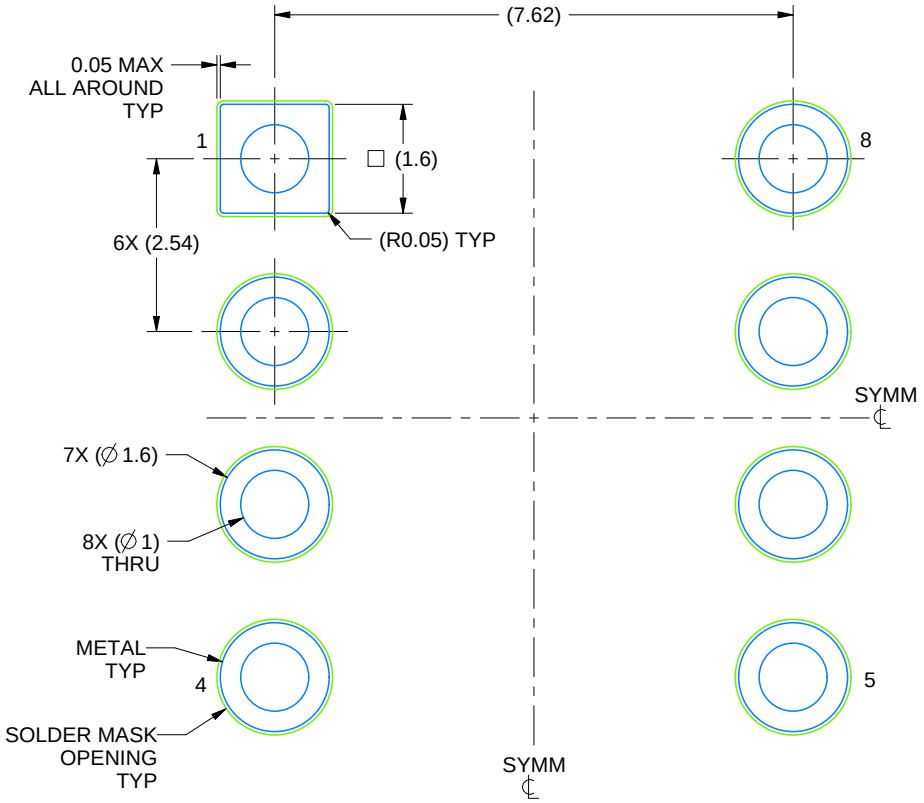
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

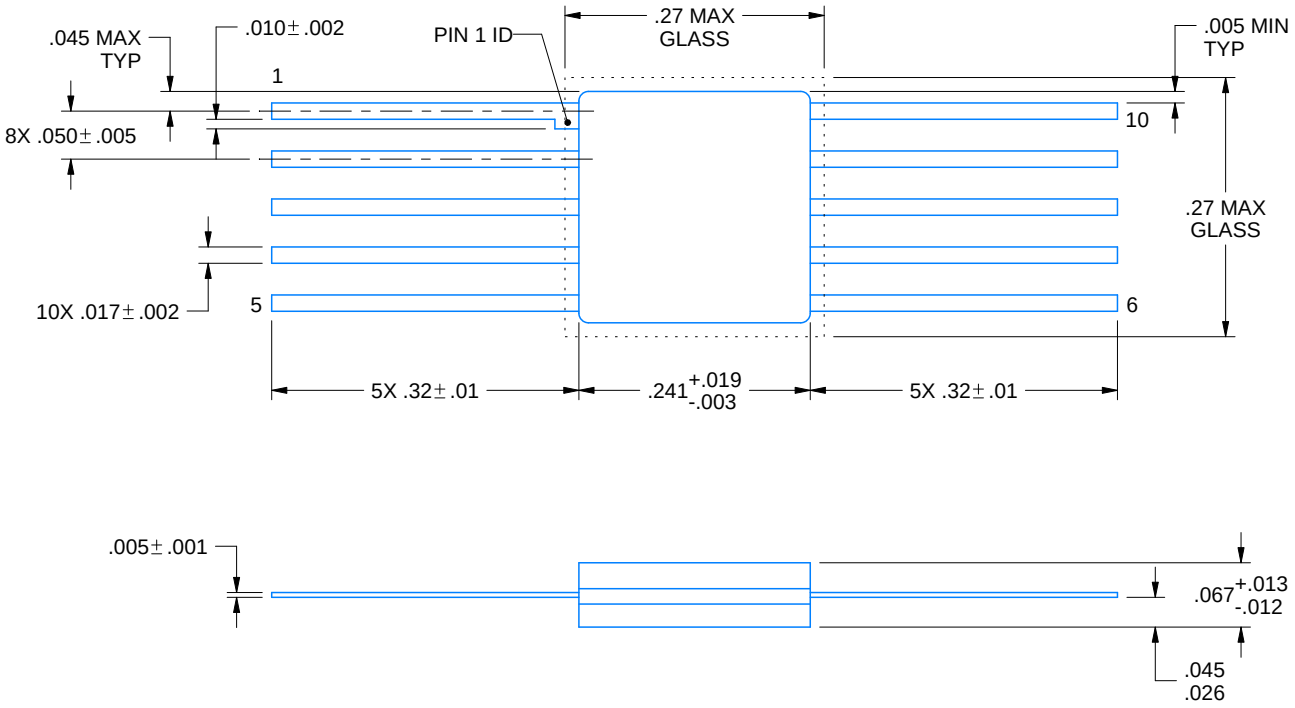
U0010A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

GENERIC PACKAGE VIEW

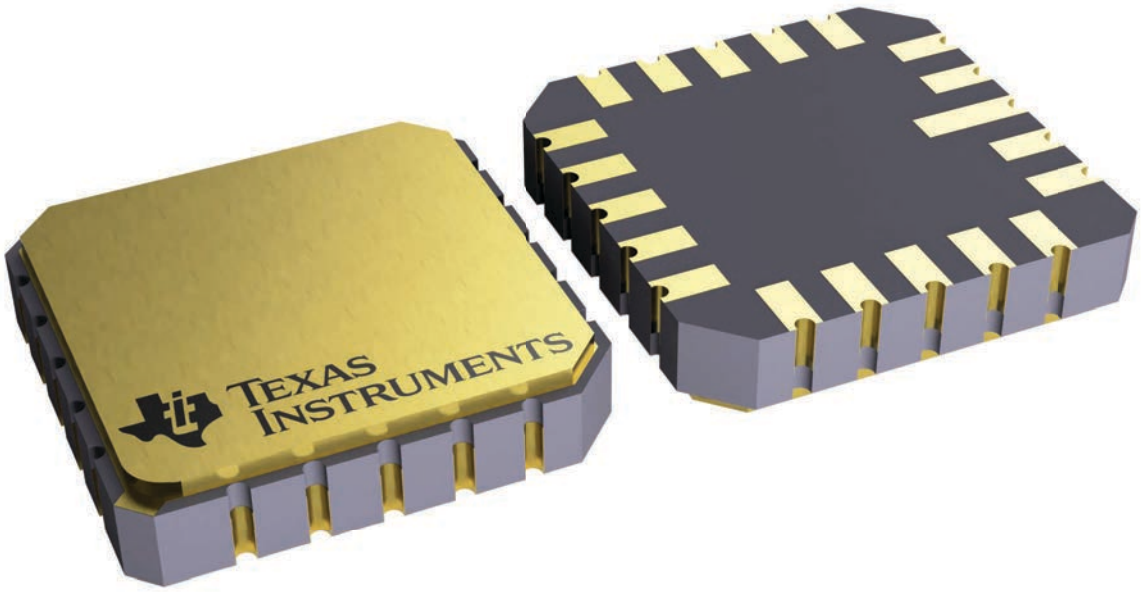
FK 20

LCCC - 2.03 mm max height

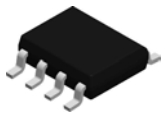
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

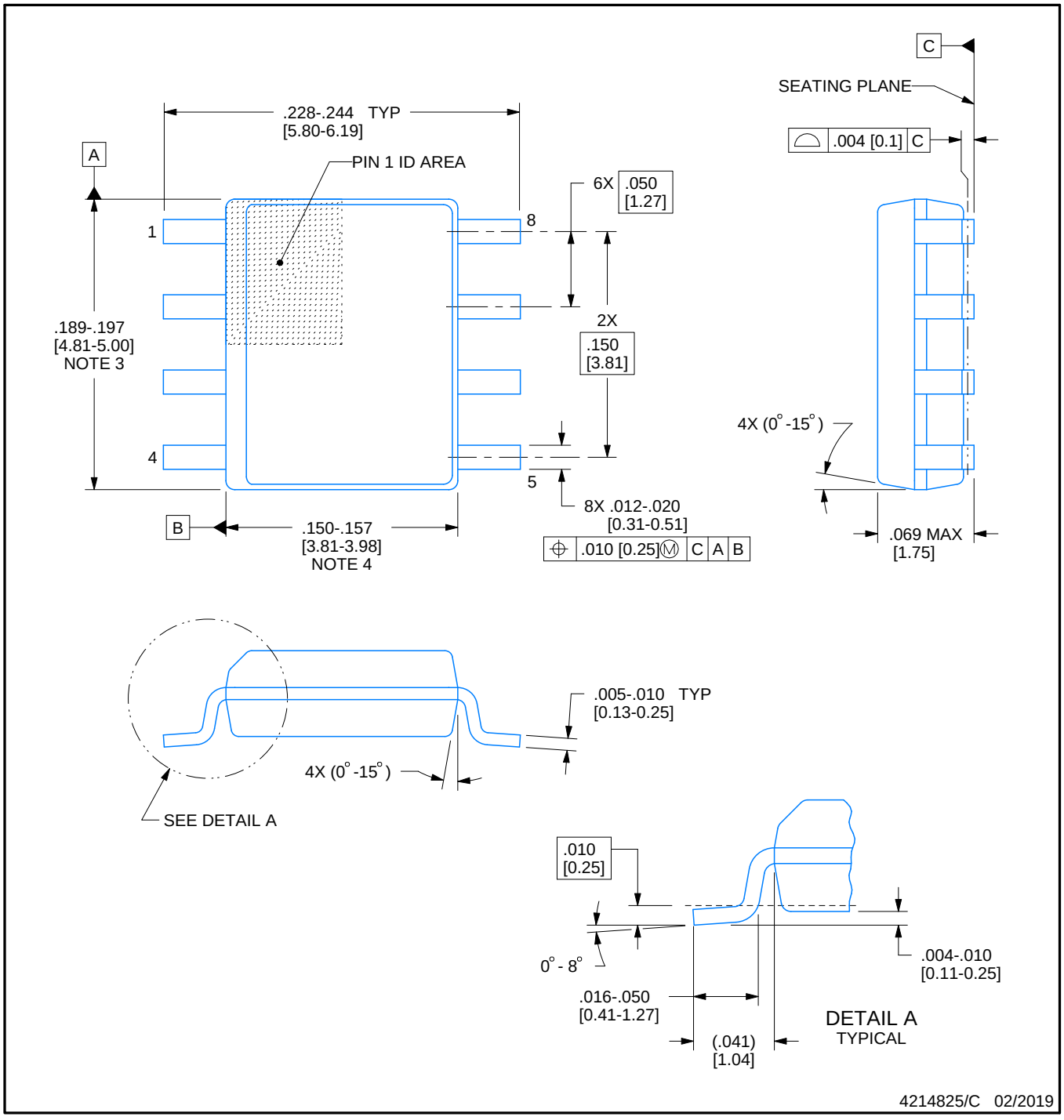


PACKAGE OUTLINE

D0008A

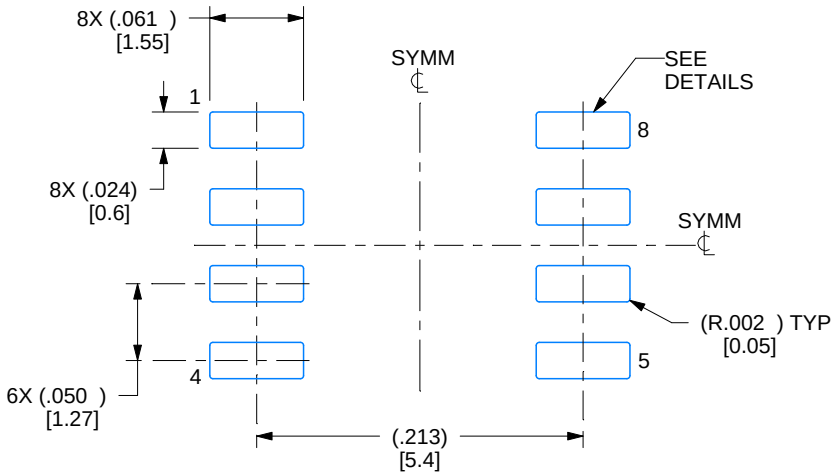
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

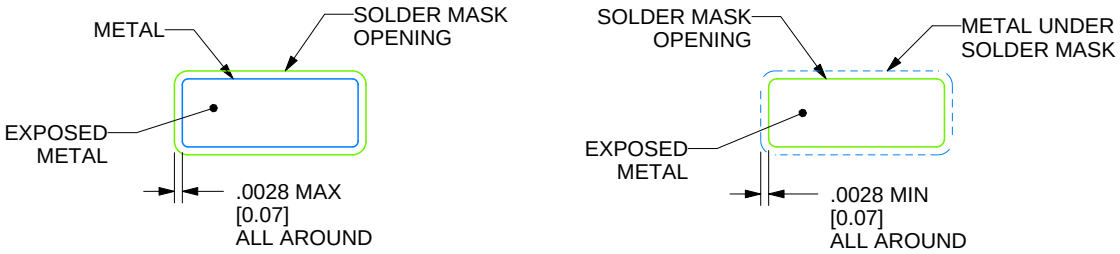


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

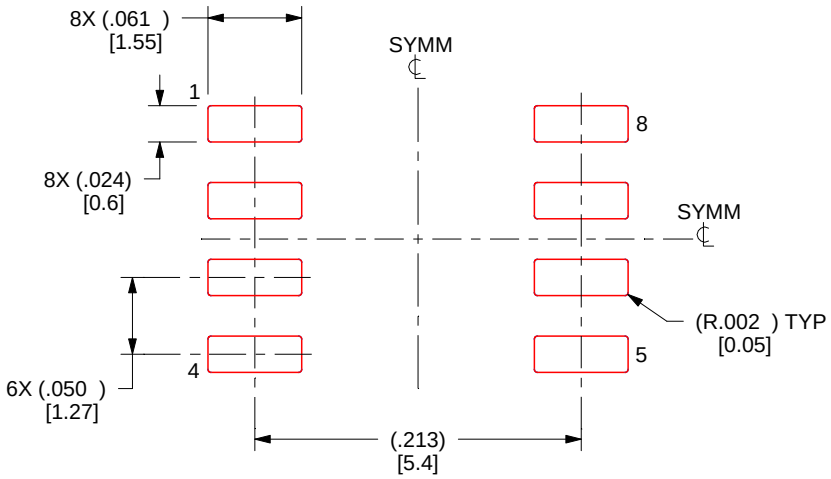
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月