TLC3702-EP デュアル マイクロパワー LinCMOS 電圧コンパレータ

1 特長

- 管理されたベースライン
  - 1 つのアセンブリ / テスト拠点と 1 つの製造拠点
- 拡張温度範囲:-55℃～125℃
- プッシュプル CMOS 出力はプルアップ抵抗なしで容量性負荷を駆動、I_O = ±8mA
- 超低消費電力:5V において 100μW (標準値)
- 高速応答時間:t_{PLH} = 2.7μs (標準値、5mV オーバードライブ時)
- 単一電源動作:4V ～ 16V
- オンチップ ESD 保護

2 概要

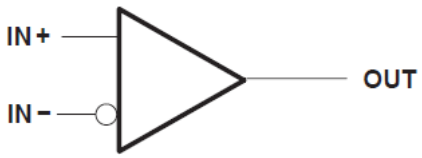
TLC3702-EP は 2 つの独立したマイクロパワー電圧コンパレータで構成されており、単一電源で動作し、最新の HCMOS ロジック システムと互換性があります。これらのチップは LM339 と機能的に類似していますが、同じ応答時間に対して消費電力が 1/20 となります。プッシュプル CMOS 出力段は、消費電力の大きいプルアップ抵抗を使用せずに容量性負荷を直接駆動し、規定の応答時間を達成します。プルアップ抵抗を排除することで、消費電力が低減されるだけでなく、基板面積と部品コストを節約できます。また、出力段は TTL 要件と完全に互換性があります。

テキサス インスツルメンツの LinCMOS プロセスは、標準的な CMOS プロセスに対して高品質のアナログ性能を実現します。LinCMOS プロセスでは、速度を犠牲にせず低消費電力、高い入力インピーダンス、低バイアス電流という標準的な CMOS の利点に加えて、大きな差動入力電圧で非常に安定した入力オフセット電圧を実現しています。この特性は、信頼性の高い CMOS コンパレータを構築するように設計されています。

製品情報

T_A	パッケージ (1)	発注用製品型番 (2)	上面のマーキング
-55℃ ～ 125℃	SOP– D	TLC3702MDREP	3702ME

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



シンボル (各コンパレータ)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 概要 ... 1
Pin Configuration and Functions ... 2
3 Specifications ... 3
3.1 Absolute Maximum Ratings ... 3
3.2 Recommended Operating Conditions ... 3
3.3 Electrical Characteristics ... 4
3.4 Switching Characteristics ... 4
3.5 Typical Characteristics ... 6
4 Detailed Description ... 8
4.1 Overview ... 8
4.2 Functional Block Diagrams ... 8
4.3 Feature Description ... 8
4.4 Device Functional Modes ... 8
5 Application and Implementation ... 12
5.1 Application Information ... 12
5.2 Typical Applications ... 13
5.3 Power Supply Recommendations ... 14
5.4 Layout ... 15
6 Device and Documentation Support ... 16
6.1 Documentation Support ... 16
6.2 ドキュメントの更新通知を受け取る方法 ... 16
6.3 サポート・リソース ... 16
6.4 Trademarks ... 16
6.5 静電気放電に関する注意事項 ... 16
6.6 用語集 ... 16
7 Revision History ... 16
8 Mechanical, Packaging, and Orderable Information ... 16

Pin Configuration and Functions

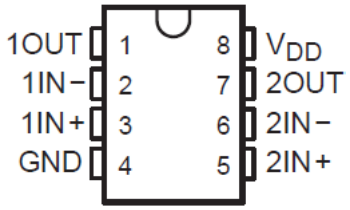


図 3-1. D Package (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply

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3 Specifications

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range(2)	-0.3	18	V
V_{ID}	Differential input voltage(3)		$\pm V_{DD}$	V
V_I	Input voltage range	-0.3	V_{DD}	V
V_O	Output voltage range	-0.3	V_{DD}	V
I_I	Input current		±5	mA
I_O	Output current (each output)		±20	mA
	Total supply current into V_{DD}		40	mA
	Total current out of GND		40	mA
T_A	Operating free-air temperature range	-55	125	℃
	Storage temperature range	-65	150	℃
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260	℃

(1) Stresses beyond those listed under “absolute maximum ratings” can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN−.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4	5	16	V
V_{IC}	Common-mode input voltage	0		V_{DD}− 1.5	V
T_A	Operating free-air temperature	−55		125	°C

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3.3 Electrical Characteristics

at specified operating free-air temperature, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5V to 10V, V_{IC} = V_{ICR}min, See [2]		25°C		1.2	15 5	mV
				−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} − 1			V
				−55°C to 125°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				125°C		83		
				−55°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5V to 10V		25°C		85		dB
				125°C		85		
				−55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1V,	I_{OH} = − 4mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1V,	I_{OH} = − 4mA	25°C		210	300	mV
				125°C			500	
I_{OH}	Short-circuit current (Sourcing)			25°C	15	30		mA
I_{OL}	Short-circuit current (Sinking)			25°C	15	30		mA
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		18	40	µA
				−55°C to 125°C			90	

(1) All characteristics are measured with zero common-mode voltage unless otherwise noted.
(2) The offset voltage limits given are the maximum values required to drive the output up to 4.5V or down to 0.3V.

3.4 Switching Characteristics

V_{DD} = 5V , T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output[1]	f = 10kHz, C_L = 50pF	Overdrive = 2mV		4.5		µs
			Overdrive = 5mV		2.7		
			Overdrive = 10mV		1.9		
			Overdrive = 20mV		1.4		
			Overdrive = 40mV		1.1		

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3.4 Switching Characteristics (続き)

V_{DD} = 5V , T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output(1)	V_I = 1.4V step at IN+			1.1		µs
		f = 10kHz, C_L = 50pF	Overdrive = 2mV		4		
			Overdrive = 5mV		2.3		
			Overdrive = 10mV		1.5		
			Overdrive = 20mV		0.95		
			Overdrive = 40mV		0.65		
		V_I = 1.4V step at IN+			0.15		
t_f	Fall time	f = 10kHz, C_L = 50pF	Overdrive = 50mV		50		ns
t_r	Rise time	f = 10kHz, C_L = 50pF	Overdrive = 50mV		125		ns

(1) Simultaneous switching of inputs causes degradation in output response.

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3.5 Typical Characteristics

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

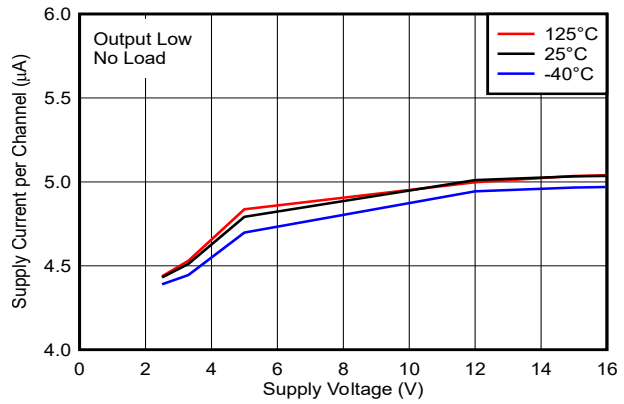


図 3-1. Supply Current per Channel vs. Supply Voltage, Output Low

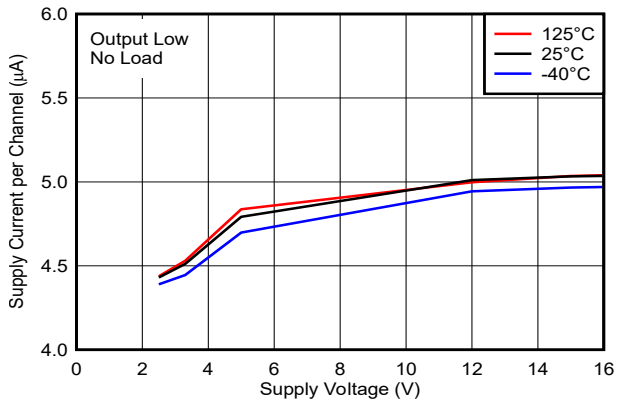


図 3-2. Supply Current per Channel vs. Supply Voltage, Output High

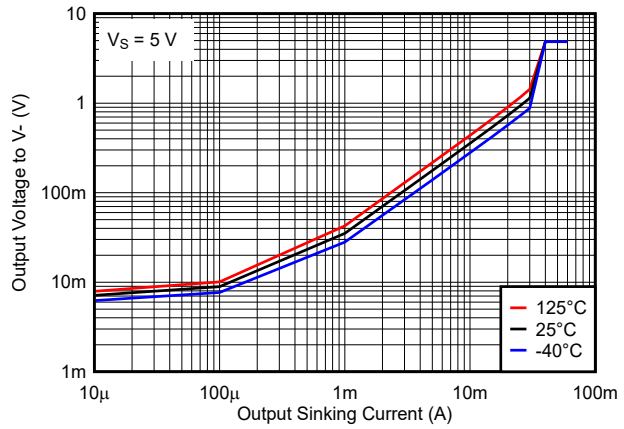


図 3-3. Output Voltage vs. Output Sinking Current, 5V

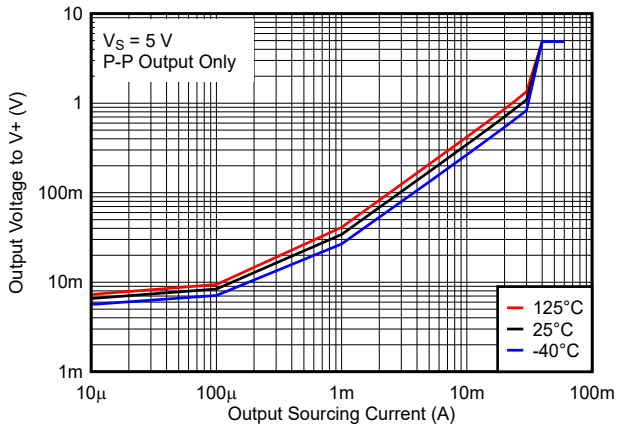


図 3-4. Output Voltage vs. Output Sourcing Current, 5V

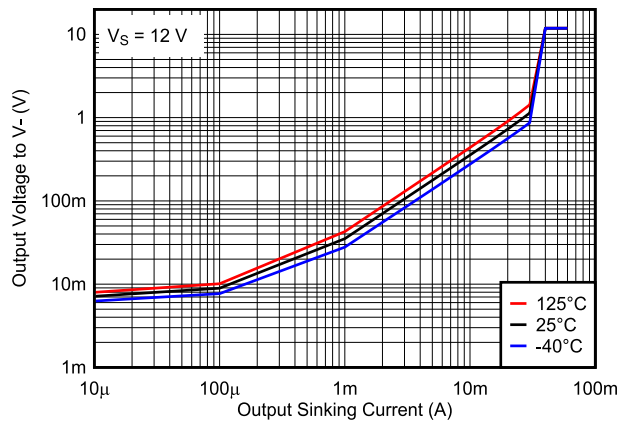


図 3-5. Output Voltage vs. Output Sinking Current, 12V

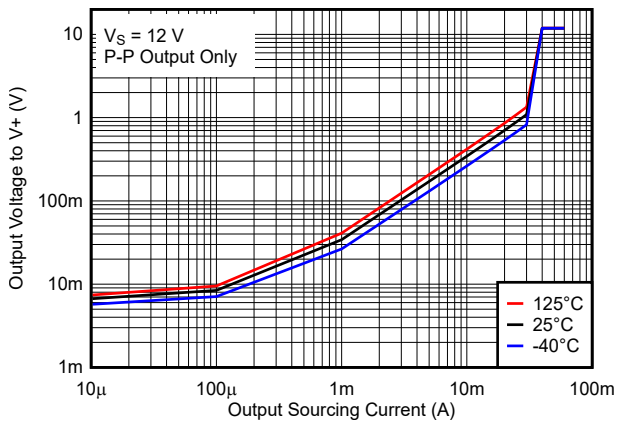


図 3-6. Output Voltage vs. Output Sourcing Current, 12V

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3.5 Typical Characteristics (continued)

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

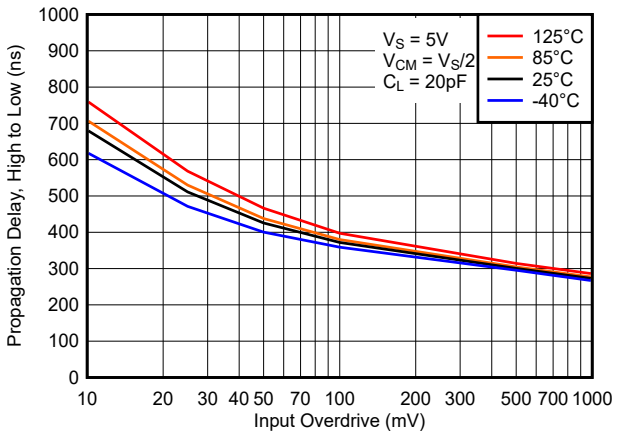


図 3-7. Propagation Delay, High to Low, 5V

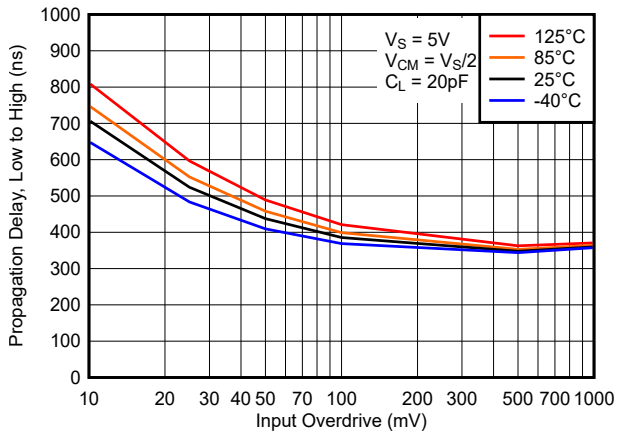


図 3-8. Propagation Delay, Low to High, 5V

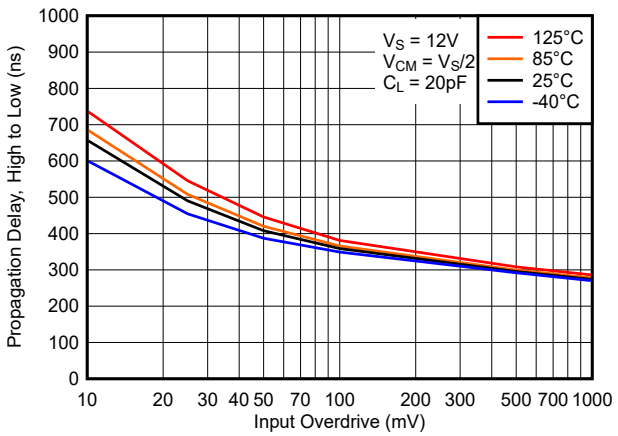


図 3-9. Propagation Delay, High to Low, 12V

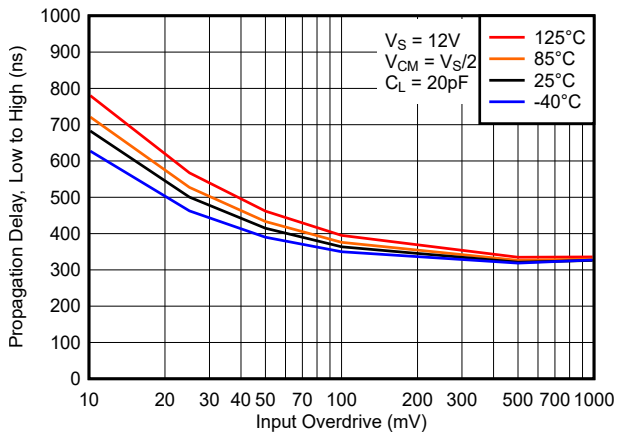


図 3-10. Propagation Delay, Low to High, 12V

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4 Detailed Description

4.1 Overview

The TLC3702-EP device is a micro-power comparator with push-pull output. Operating down to 4V while only consuming only 5µA per channel, the TLC3702-EP is excellent for power conscious applications.

4.2 Functional Block Diagrams

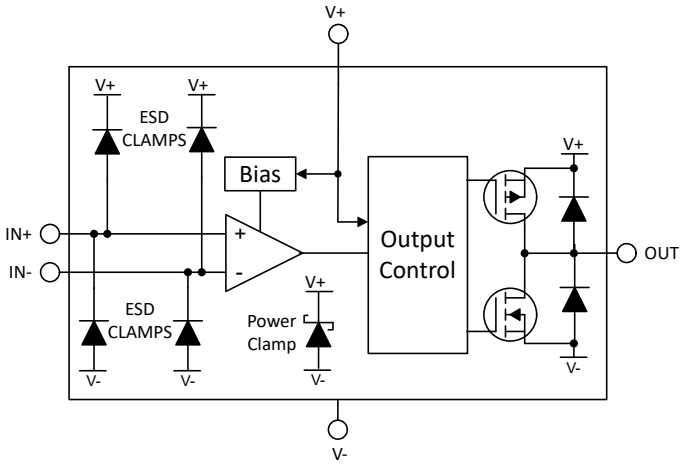


図 4-1. Block Diagram

4.3 Feature Description

The TLC3702-EP comparator consists of a CMOS differential pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The output consists of a push-pull output stage capable of sinking current with a negative differntial input voltage and sourcing current with a positive differential input.

4.4 Device Functional Modes

4.4.1 Input

The TLC3702-EP input voltage range extends from V- to 1.5V below V+ over the full temperature range. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

4.4.2 ESD Protection

The TLC3702-EP input and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and V+, and a "lower" ESD clamp between the I/O pins and V-. The inputs or output must not exceed the supply rails by more than 300mV. TI does not recommend applying signals to the inputs with no supply voltage.

When the inputs are connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limitng the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

4.4.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the

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specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage.

4.4.4 Push-Pull Output

The TLC3702-EP features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail (V+ when output "low" or V- when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

4.4.5 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in 図 4-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

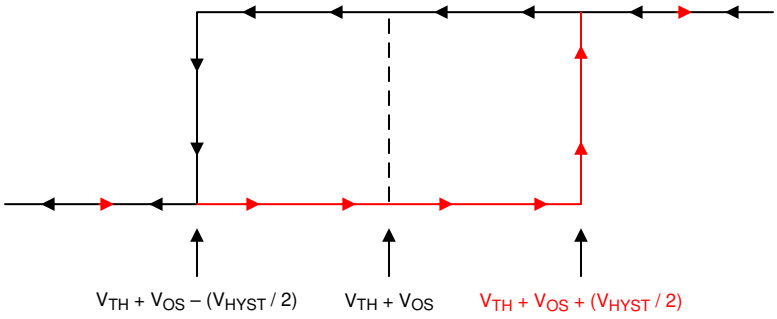


図 4-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

4.4.5.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown below.

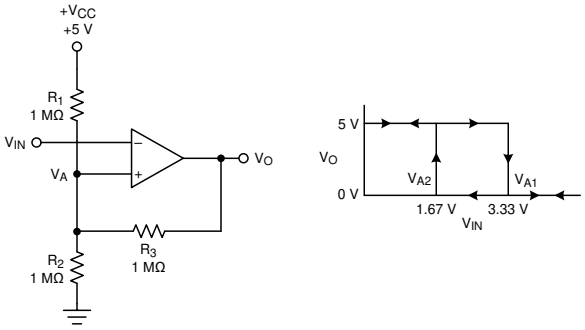


図 4-3. Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

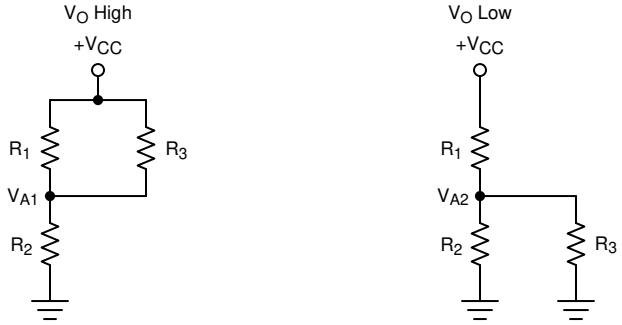


図 4-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown above on the left.

The equation below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown above on the right.

Use the equation below to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

4.4.5.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in 図 4-5.

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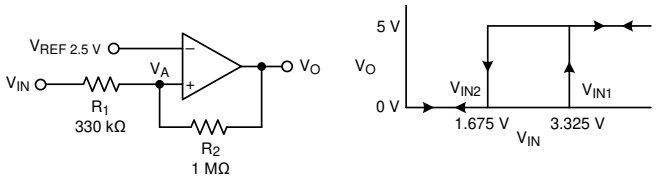


図 4-5. Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 図 4-6.

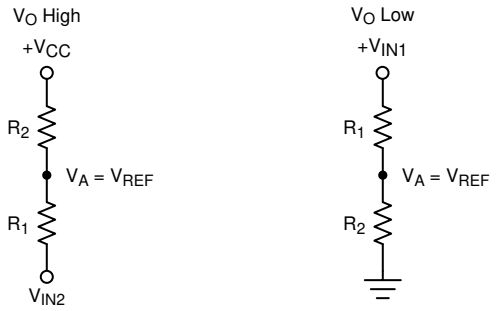


図 4-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use 式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use 式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

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5 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

5.1 Application Information

5.1.1 Basic Comparator Definitions

5.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the 図 5-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). 表 5-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 5-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

5.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in 図 5-1 and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive (V_{OD}) and underdrive (V_{UD}) voltage levels (see section below).

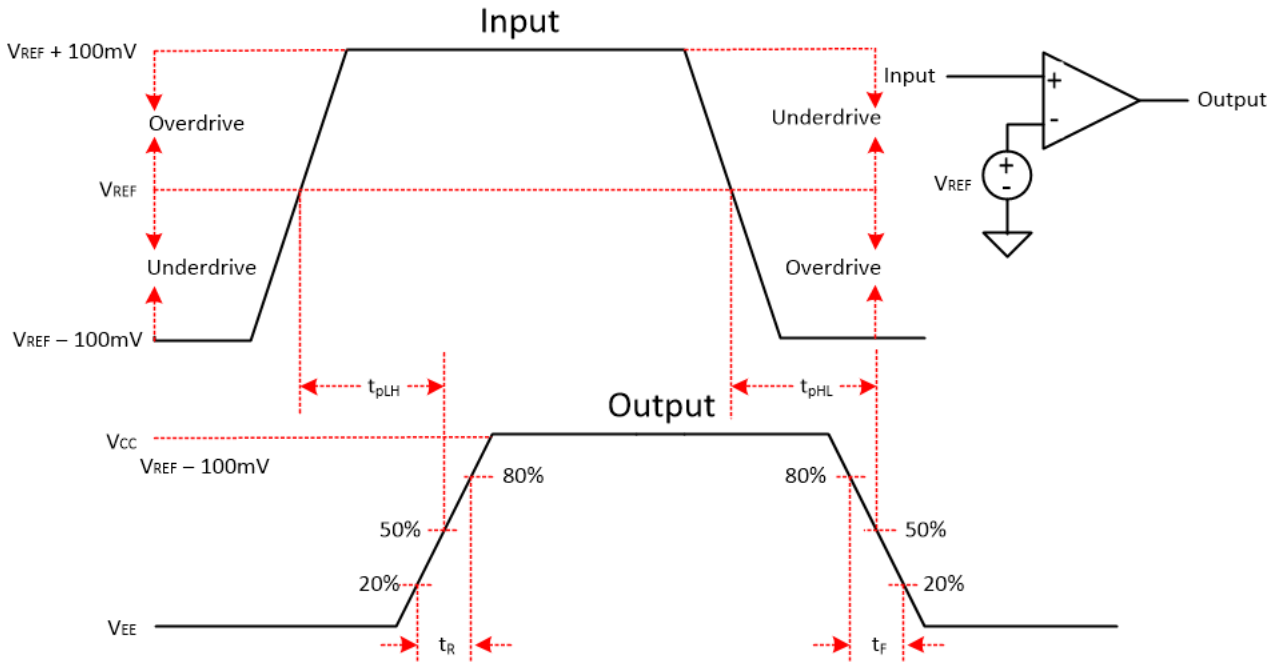


図 5-1. Comparator Timing Diagram

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5.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the 図 5-1 example. Similarly, underdrive voltage, V_{UD}, is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay (t_p). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes propagation delay to increase. This is particularly important in applications where rail-to-rail input swings are present at the comparator inputs. The result can be skewed propagation delay (difference between tp_{LH} and tp_{HL}). As a low power comparator, do not use this comparator family if variation in propagation delay is critical.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

5.2 Typical Applications

5.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. The figure below shows a simple window comparator circuit monitoring a 24V PLC power supply.

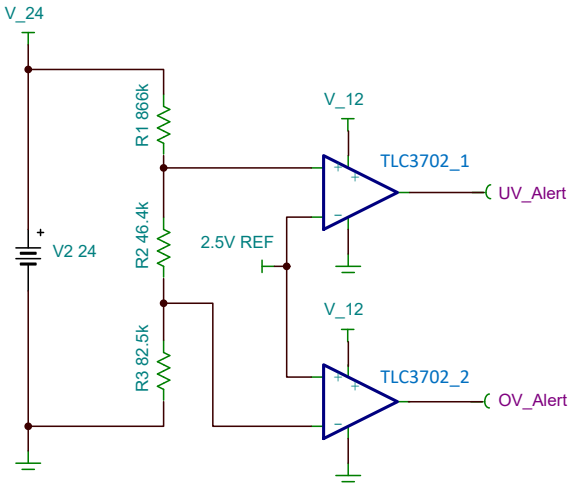


図 5-2. Window Comparator

5.2.1.1 設計要件

この設計については、以下の設計要件に従ってください。

- 24V 電源が 19.2V を下回る場合の UV_Alert (論理低出力)
- 24V 電源が 30V を上回る場合の OV_Alert (論理低出力)
- 抵抗ストリングで消費される電流は、30µA です
- コンパレータは、5V 電源で動作します
- 2.5V の外部参照を使用します

5.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC3702-EP is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV_Alert and UV_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

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The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from 2.5V / 30uA which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from (2.5V /19.2uA) - R3 which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kohms. Please note that standard 1% resistor values were selected for the circuit

The respective comparator outputs (OV_Alert and UV_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

5.2.1.3 Application Curve

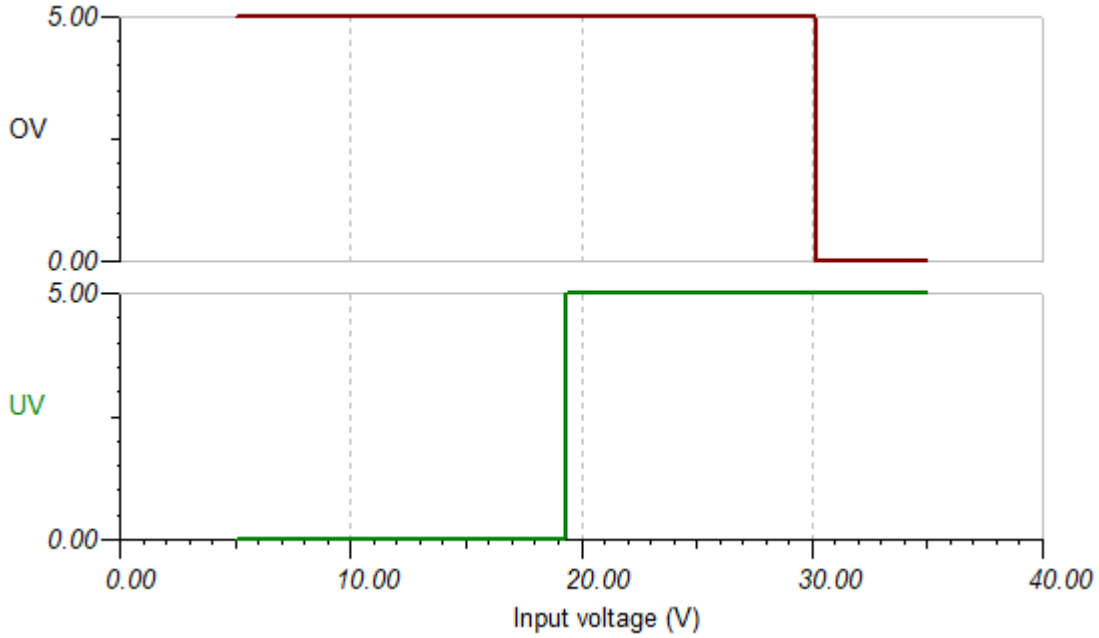


図 5-3. Window Comparator Results

5.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between V+ pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the output swings "low" (V_{OL}) to V- potential and not GND.

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5.4 Layout

5.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V+ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V+ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (≤100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

5.4.2 Layout Example

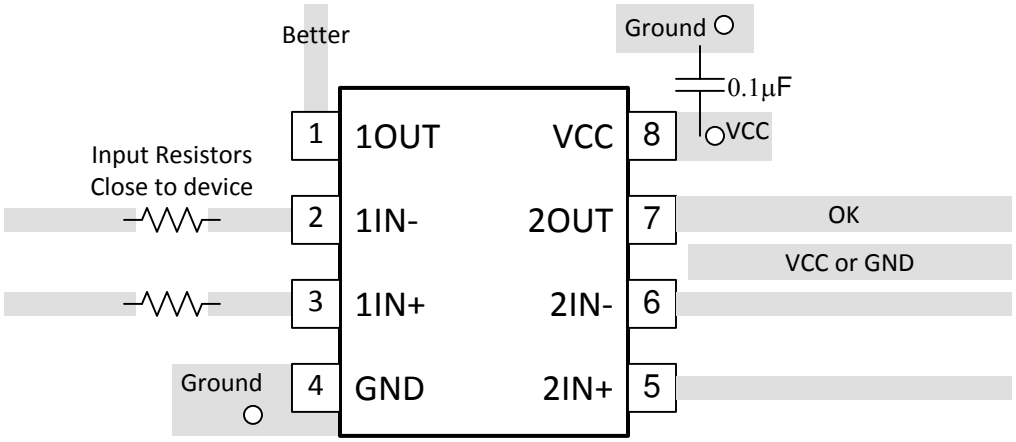


図 5-4. Dual Layout Example

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

6.2 ドキュメントの更新通知を受け取る方法

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6.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

7 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (March 2025) to Revision B (June 2025)	Page
• 「特長」を更新	1

Changes from Revision * (July 2002) to Revision A (March 2025)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 新しいダイを反映するようにデータシート全体を更新 - 最小および最大仕様への変更なし	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC3702MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3702ME
TLC3702MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3702ME
V62/03643-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3702ME

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLC3702-EP :

- Catalog : TLC3702

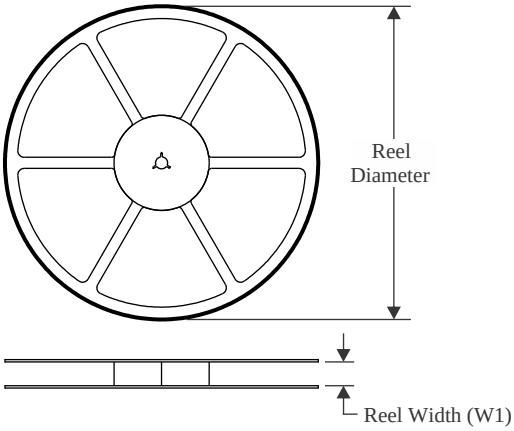
- Automotive : TLC3702-Q1
- Military : TLC3702M

NOTE: Qualified Version Definitions:

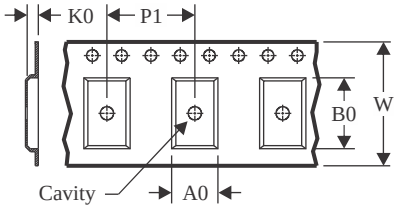
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

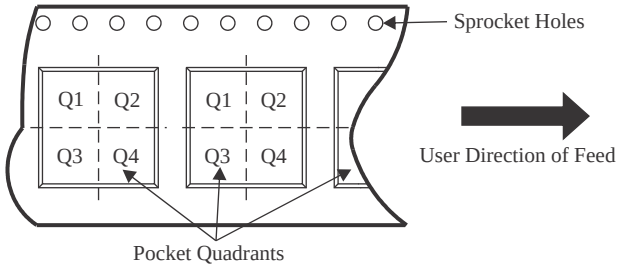


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

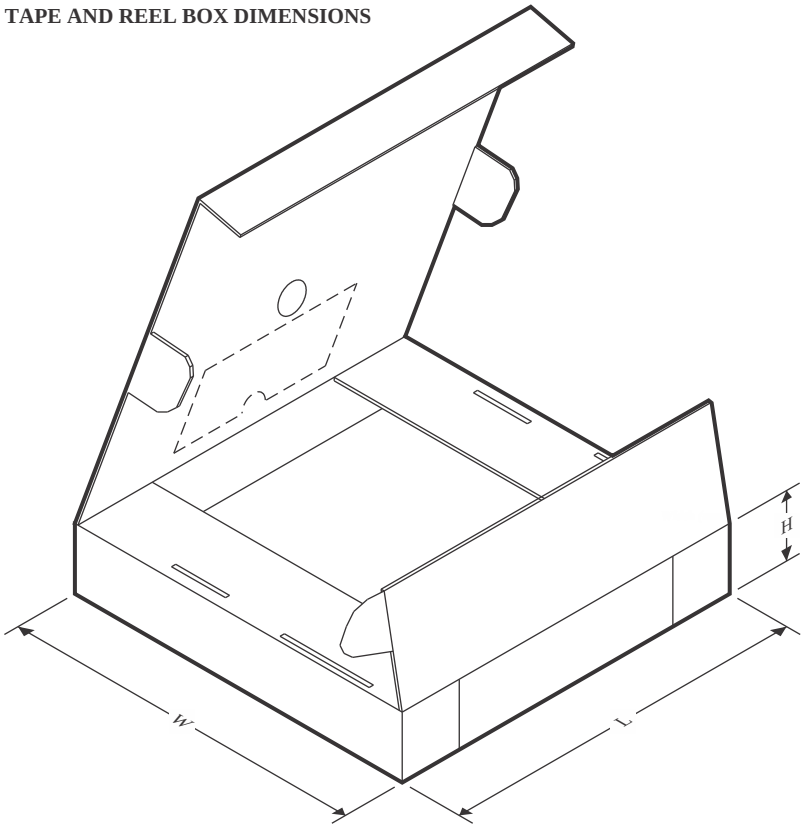
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

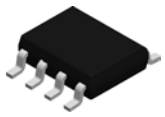
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3702MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3702MDREP	SOIC	D	8	2500	353.0	353.0	32.0

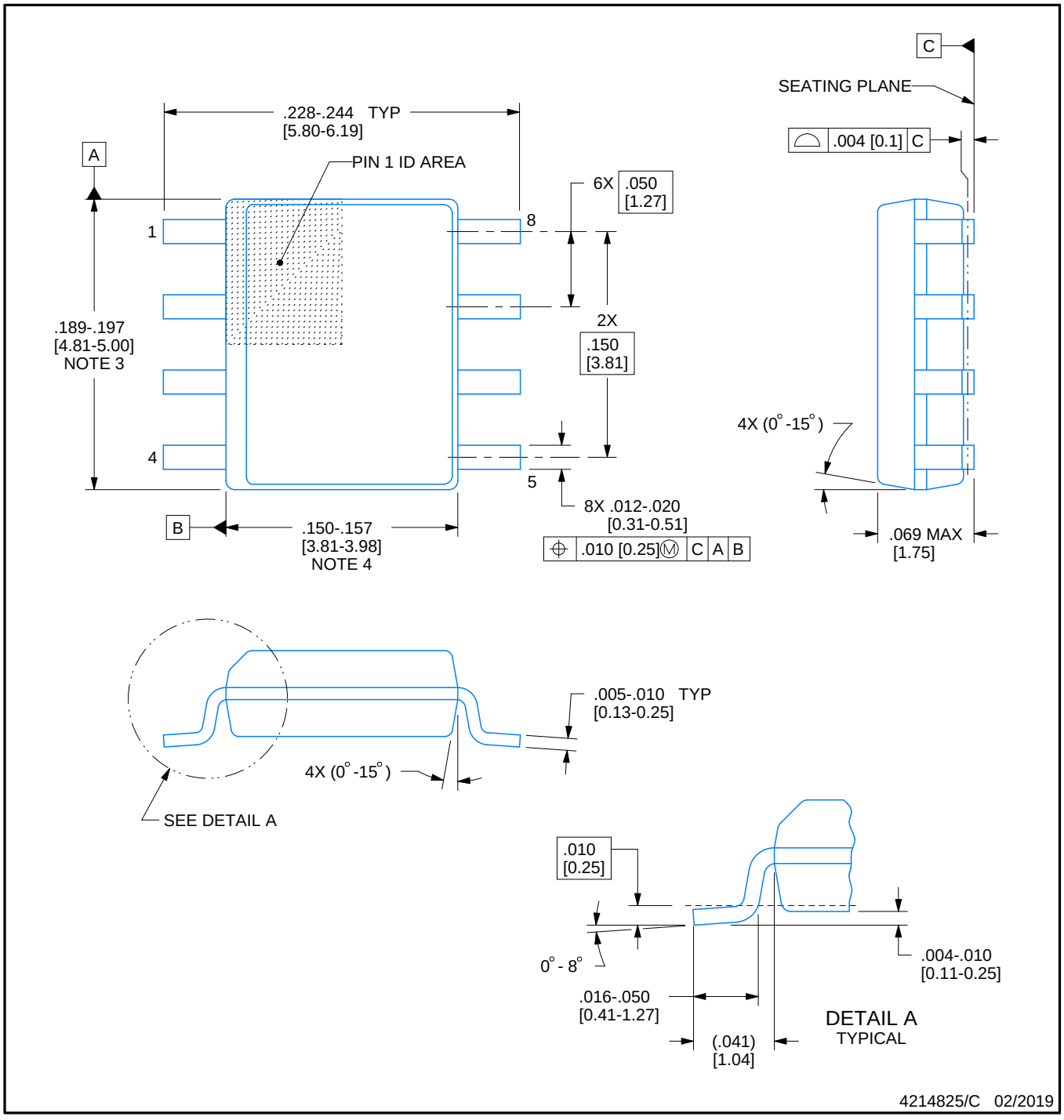


PACKAGE OUTLINE

D0008A

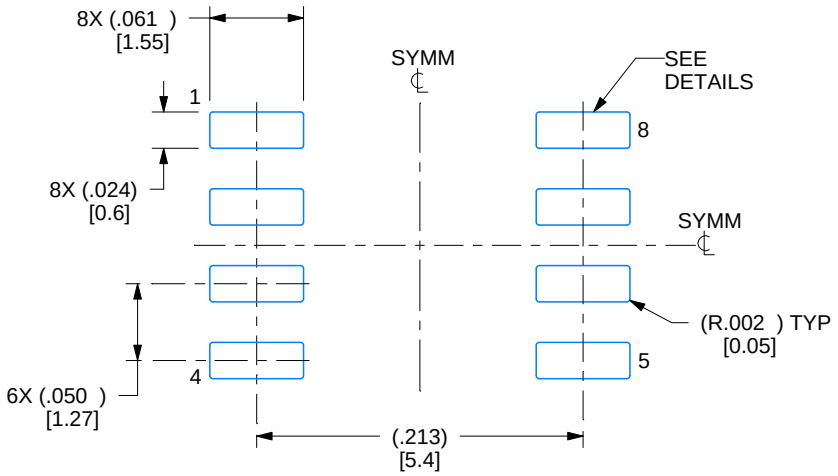
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

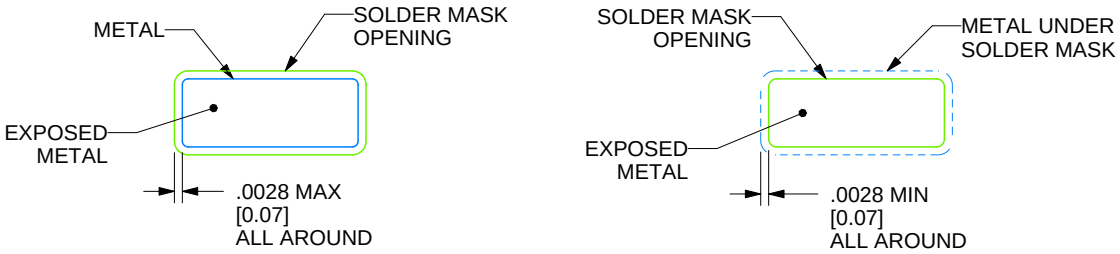


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

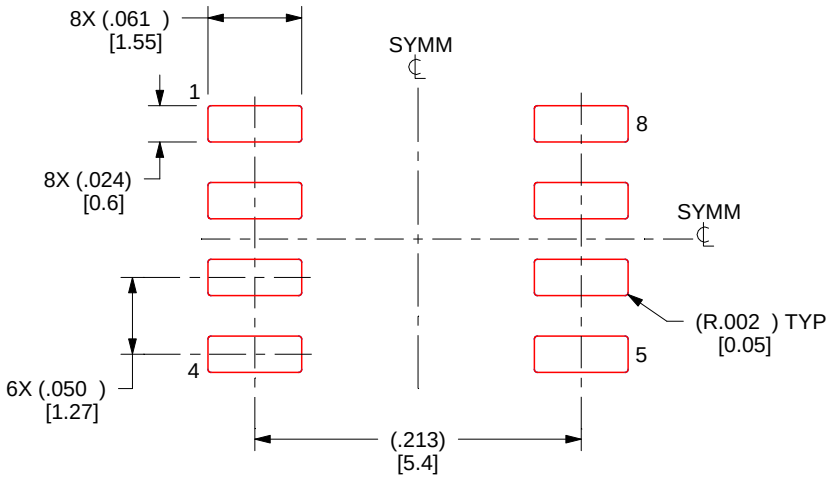
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月