



TLC694x 16チャンネル、32/48多重化、16ビットのES-PWM定電流LEDドライバ

1 特長

- 電源電圧範囲
 - V_{CC} 電圧範囲: 3V~5.5V
 - V_{LED} 電圧範囲: $V_{CC} + 0.3V$ (最大値)
- 16の定電流シンク・チャンネル
 - 0.3mA~25mA ($3V \leq V_{CC} \leq 5.5V$)
 - チャンネル電流偏差: $\pm 1\%$ (標準値)
 - デバイス電流偏差: $\pm 1\%$ (標準値)
 - 低いニー電圧: 10mAで0.3V(標準値)
- 7ビット (128ステップ) のグローバル輝度制御(BC)
- 16ビット (65,536ステップ) の拡張スペクトラムPWMグレイスケール制御
- 内蔵メモリによりTLC6946で32、TLC6948で48の多重化をサポート
- LED表示性能の強化
 - 低グレイスケールの均一性向上
 - 低グレイスケールの結合問題の解消
 - ゴーストの除去とキャタピラ問題の解消
- 高速のシリアル・データ・インターフェイス
 - データ・シフト・クロック: 33MHz(最大値)
 - グレイスケール制御クロック: 33MHz(最大値)
 - デュアル・エッジのグレイスケール制御をサポート
- 診断および保護
 - LEDオープン検出(LOD)
 - IREF抵抗短絡保護(ISP)
 - サーマル・シャットダウン(TSD)
- スマート・パワーセービング・モード

2 アプリケーション

- モノクロ、マルチカラー、フルカラーのLEDディスプレイ
- 高リフレッシュ・レートのLEDビデオ・ディスプレイ
- 高密度、小ピッチのLEDマトリクス・ディスプレイ

3 概要

高密度、小ピッチのLEDパネル・アプリケーションでは、高いマルチプレクシング、高いPWM分解能、高いリフレッシュ・レートを実現するため、マルチチャンネルLEDドライバの性能への要求が増大しています。表示品質の厳格な要件を満たすため、LEDドライバには、各種のLEDマトリクス・アプリケーション・シナリオで発生する様々な問題を解決する能力が必要になります。

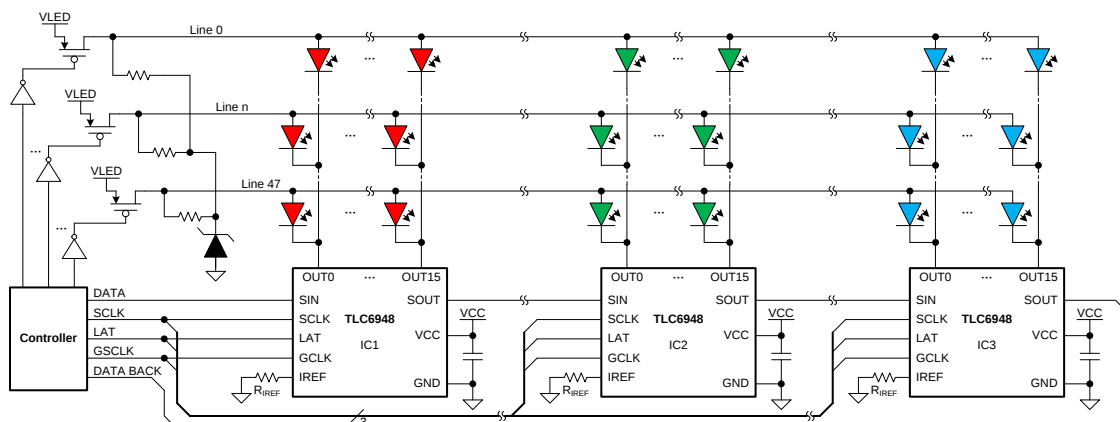
TLC694xデバイスは、16チャンネル、定電流シンクのLEDドライバです。各チャンネルは、それぞれ独立に65,536ステップでPWMグレイスケール制御を調整できます。16チャンネルすべての最大定電流の値を単一の外付け抵抗によって設定でき、0.3mA~25mAの範囲で128ステップのグローバルな輝度制御が可能です。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TLC6946	SSOP (24)	8.65mm×3.90mm
	VQFN (24)	4.00mm×4.00mm
TLC6948	SSOP (24)	8.65mm×3.90mm
	VQFN (24)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図、TLC6948で48多重化



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4 改訂履歴

2018年6月発行のものから更新

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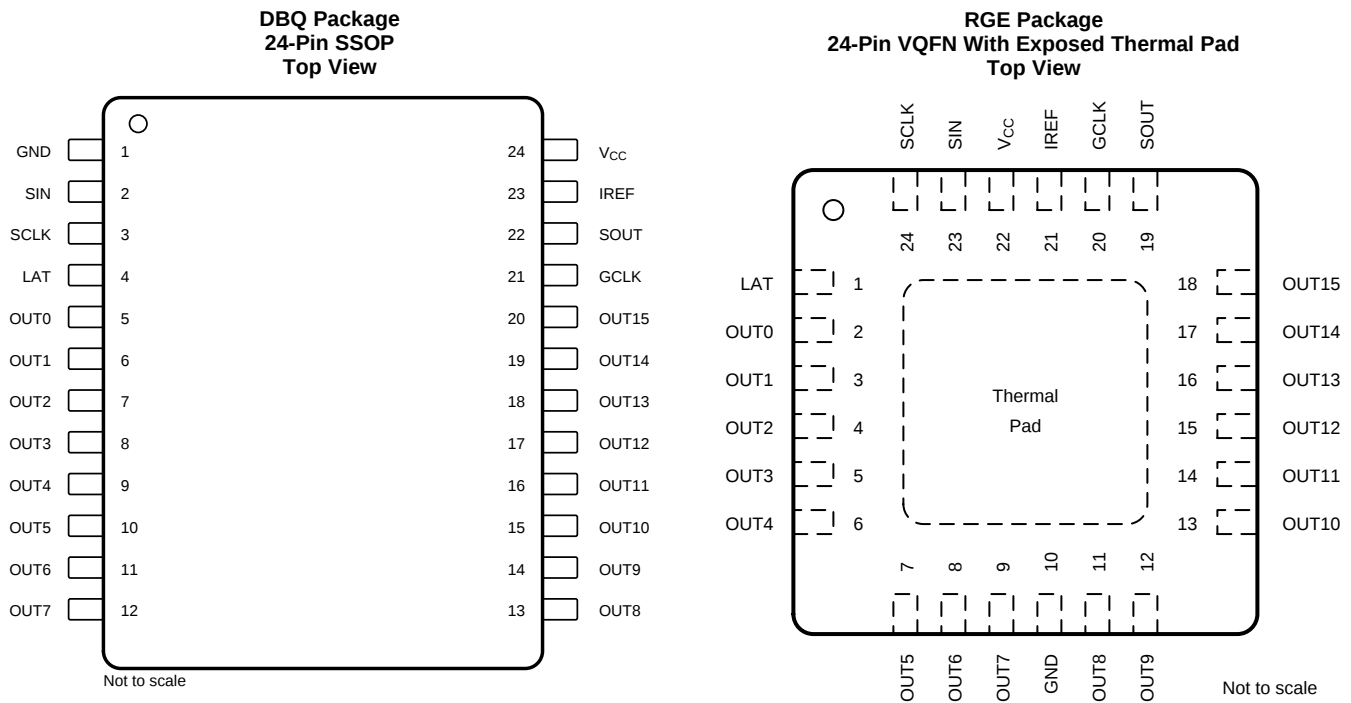
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5 概要（続き）

TLC694xデバイスには、小ピッチのLEDディスプレイ・アプリケーションで発生する、低グレイスケールの不均一、結合、ゴースト、キャタピラなど各種の表示上の問題を解決するため、拡張回路が内蔵されています。

TLC694xデバイスにはLEDオープン検出機能が搭載されており、エラー検出結果はシリアル・データ・インターフェイス・ポートから読み出せます。サーマル・シャットダウンおよびIREF抵抗短絡保護により、システムの高い信頼性が確保されます。また、TLC694xデバイスにはスマート・パワーセービング・モードがあり、すべての出力がオフのときは、合計消費電流が1mA（標準値）に設定されます。

6 Pin Configuration and Functions



Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	DBQ	RGE		
GCLK	21	20	I	Grayscale (GS) pulse-width modulation (PWM) reference-clock-signal input pin. In the default operating mode, each GCLK rising edge increments the GS counter for PWM control. GCLK supports dual-edge operation.
GND	1	10	—	Power-ground reference
IREF	23	21	I	Pin for setting the maximum constant-current value. Connecting an external resistor between IREF and GND sets the maximum current for each constant-current output channel. When this pin is connected directly to GND, all outputs are forced off. The external resistor should be placed close to the device.
LAT	4	1	I	Data latch pin. The falling edge of LAT latches the data from the common shift register into the GS data memory or the function control register.

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBQ	RGE		
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant current. A different voltage can be applied to each output.
OUT1	6	3	O	
OUT2	7	4	O	
OUT3	8	5	O	
OUT4	9	6	O	
OUT5	10	7	O	
OUT6	11	8	O	
OUT7	12	9	O	
OUT8	13	11	O	
OUT9	14	12	O	
OUT10	15	13	O	
OUT11	16	14	O	
OUT12	17	15	O	
OUT13	18	16	O	
OUT14	19	17	O	
OUT15	20	18	O	
SCLK	3	24	I	Clock-signal input pin. Serial data present on SIN are shifted to the LSB of the internal 16-bit common shift register on the SCLK rising edge. All data in the shift register are shifted toward the MSB of the internal 16-bit common shift register on each SCLK rising edge.
SIN	2	23	I	Serial-data input pin of the internal 16-bit common shift register. When SIN is high, the LSB of the internal 16-bit common shift register is set to 1 on the SCLK input rising edge. When SIN is low, the LSB of the internal 16-bit common shift register is set to 0 on the SCLK input rising edge.
SOUT	22	19	O	Serial data output pin of the internal 16-bit common shift register. The MSB of the internal 16-bit common shift register appears on SOUT.
V _{CC}	24	22	I	Power supply pin
Thermal pad	—	—	—	Internally connected to GND in the RGE package only. The thermal pad and the GND pin must be connected together on the board.

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
Voltage	V _{CC}	−0.3	6	V
	GCLK, IREF, LAT, SCLK, SIN, SOUT	−0.3	V _{CC} + 0.3	V
	OUT0 to OUT15	−0.3	V _{CC} + 0.3	V
Current	OUT0 to OUT15	0	27	mA
Operating junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±7000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	Supply voltage	3		5.5	V
V _{OUTn}	Voltage applied to OUT0 to OUT15	Voltage applied to OUT0 to OUT15	0		V _{CC}	V
V _{IH}	High-level input voltage	GCLK, LAT, SCLK, SIN	0.7 × V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage	GCLK, LAT, SCLK, SIN	0		0.3 × V _{CC}	V
I _{OH}	High-level output current	SOUT			−2	mA
I _{OL}	Low-level output current	SOUT			2	mA
I _{OLC, max}	Maximum constant-output sink current	OUT0 to OUT15	0.3		25	mA
f _{SCLK}	Data-shift clock frequency	SCLK			33	MHz
f _{GCLK}	Grayscale control clock frequency	GCLK			33	MHz
f _{GCLK,B}	Grayscale control clock frequency for dual-edge operation	GCLK			25	MHz
t _{w(H0)}	Pulse width duration	SCLK	10			ns
t _{w(L0)}	Pulse width duration	SCLK	10			ns
t _{w(H1)}	Pulse width duration	GCLK	10			ns
t _{w(L1)}	Pulse width duration	GCLK	10			ns
t _{w(H2)}	Pulse width duration	GCLK (for dual-edge operation)	18			ns
t _{w(L2)}	Pulse width duration	GCLK (for dual-edge operation)	18			ns
t _{SU(0)}	Setup time	SIN to SCLK↑	2			ns
t _{SU(1)}	Setup time	LAT↑ to SCLK↑	5			ns
t _{SU(2)}	Setup time	LAT↓ to SCLK↑	5			ns
t _{SU(3)}	Setup time	LAT↓ to SCLK↑, read data from SOUT	50			ns
t _{SU(4)}	Setup time	LAT↓ (WRTGS) to LAT↓ (WRTGS)	1.5			μs

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{SU(5)}$	Setup time	LAT ↓ (WRTGS) to LAT ↓ (VSYNC)	1.5			μs
$t_{SU(6)}$	Setup time	LAT ↓ (VSYNC) to GCLK ↑	2.5			μs
$t_{SU(7)}$	Setup time	LAT ↓ (VSYNC) to LAT ↓ (WRTGS)	2.5			μs
$t_{SU(8)}$	Setup time	Last LAT (non-0 GS data latched) ↓ to the first GCLK ↑ of next frame (wake up from power-save mode)	50			μs
t_{LSW}	Line switching time	Last GCLK ↓ to the first GCLK ↑ of next line	1			μs
$t_{h(0)}$	Hold time	SCLK ↑ to SIN	2			ns
$t_{h(1)}$	Hold time	SCLK ↑ to LAT ↑	2			ns
$t_{h(2)}$	Hold time	SCLK ↑ to LAT ↓	10			ns
T_A	Operating ambient temperature	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLC6946		UNIT
		DBQ (SSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.2	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	34.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.4	15.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.2	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41	15.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	5	°C/W

(1) For more information about traditional and new thermalmetrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

$V_{CC} = 3\text{ V}$ to 5.5 V and $T_A = -40^\circ\text{C}$ to 85°C ; typical values are at $V_{CC} = V_{LED} = 3.5\text{ V}$, $T_A = 25^\circ\text{C}$, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = −2 mA at SOUT	V _{CC} − 0.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA at SOUT			0.4	V
V _{IREF}	Reference voltage	BC = 00h, R _{IREF} = 10.7 kΩ (I _{OUTn} = 0.3-mA target)	0.8			V
V _(LOD)	LED open-detection threshold	All OUTn = on, LODVTH = 00b	0.12	0.2	0.28	V
		All OUTn = on, LODVTH = 01b	0.42	0.5	0.58	V
		All OUTn = on, LODVTH = 10b	0.82	0.9	0.98	V
		All OUTn = on, LODVTH = 11b	1.12	1.2	1.28	V
V _(KNEE)	Knee voltage (OUT0 to OUT15)	All OUTn = on, BC = 36h, R _{IREF} = 1.27 kΩ (I _{OUTn} = 10-mA target)	0.3			V
ΔIOLC0	Constant-current error (channel-to-channel) ⁽¹⁾	All OUTn = on, BC = 00h, V _{OUTn} = 1 V, R _{IREF} = 10.7 kΩ (I _{OUTn} = 0.3-mA target), T _A = 25°C, includes the V _{IREF} tolerance	±1%		±3.5%	

(1) The deviation of each output from average of all channels constant current. The deviation is calculated by the formula.

$$\Delta(\%) = \left[\frac{I_{OUTn}}{I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15}} - 1 \right] \times 100$$

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Electrical Characteristics (continued)

$V_{CC} = 3\text{ V}$ to 5.5 V and $T_A = -40^\circ\text{C}$ to 85°C ; typical values are at $V_{CC} = V_{LED} = 3.5\text{ V}$, $T_A = 25^\circ\text{C}$, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC1}	Constant-current error (device-to-device) ⁽²⁾	All OUTn = on, BC = 00h, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 10.7\text{ k}\Omega$ ($I_{OUTn} = 0.3\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 2\%$	
ΔI_{OLC2}	Constant-current error (channel-to-channel) ⁽¹⁾	All OUTn = on, BC = 2Ah, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 10.7\text{ k}\Omega$ ($I_{OUTn} = 1\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 3\%$	
ΔI_{OLC3}	Constant-current error (device-to-device) ⁽²⁾	All OUTn = on, BC = 2Ah, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 10.7\text{ k}\Omega$ ($I_{OUTn} = 1\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 2.5\%$	
ΔI_{OLC4}	Constant-current error (channel-to-channel) ⁽¹⁾	All OUTn = on, BC = 36h, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 1.27\text{ k}\Omega$ ($I_{OUTn} = 10\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 2.5\%$	
ΔI_{OLC5}	Constant-current error (device-to-device) ⁽²⁾	All OUTn = on, BC = 36h, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 1.27\text{ k}\Omega$ ($I_{OUTn} = 10\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 2.5\%$	
ΔI_{OLC6}	Constant-current error (channel-to-channel) ⁽¹⁾	All OUTn = on, BC = 7Eh, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 1.02\text{ k}\Omega$ ($I_{OUTn} = 25\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 2\%$	
ΔI_{OLC7}	Constant-current error (device-to-device) ⁽²⁾	All OUTn = on, BC = 7Eh, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 1.02\text{ k}\Omega$ ($I_{OUTn} = 25\text{-mA}$ target), $T_A = 25^\circ\text{C}$, includes the V_{IREF} tolerance		$\pm 1\%$	$\pm 2\%$	
ΔI_{OLC8}	Line regulation ⁽³⁾	All OUTn = on, $V_{CC} = 3\text{ V}$ to 5.5 V , $V_{OUTn} = 1\text{ V}$		± 1	± 2	%/V
ΔI_{OLC9}	Load regulation ⁽⁴⁾	All OUTn = on, $V_{OUTn} = 1\text{ V}$ to 3 V		± 1	± 2	%/V
$V_{IL(ISP)}$	IREF resistor short-protection enter threshold		0.15	0.195		V
$V_{IH(ISP)}$	IREF resistor short-protection release threshold			0.325	0.4	V
$T_{(TSD)}$	Thermal shutdown threshold ⁽⁵⁾			170		$^\circ\text{C}$
$T_{(HYS)}$	Thermal shutdown hysteresis ⁽⁵⁾			15		$^\circ\text{C}$
I_I	SCLK or SIN Input current	$V_I = V_{CC}$ or GND at SCLK or SIN	-1		1	μA

(2) The deviation of the average of constant current from the ideal constant current value.

$$\Delta(\%) = \left[\frac{\frac{I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15}}{16} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right] \times 100$$

, Ideal current is calculated by the

$$\text{Ideal Output (mA)} = \text{Gain} \times \left(\frac{V_{IREF}}{R_{IREF(\Omega)}} \right) \times \left(\frac{1}{8} + \frac{BC}{144} \right)$$

following equation

(3) Line regulation is calculated by the following equation

$$\Delta(\%V) = \left[\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{V}) - (I_{OUTn} \text{ at } V_{CC} = 3\text{V})}{(I_{OUTn} \text{ at } V_{CC} = 3\text{V})} \right] \times \frac{100}{5.5\text{V} - 3\text{V}}$$

(4) Load regulation is calculated by the following equation

$$\Delta(\%V) = \left[\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{V})} \right] \times \frac{100}{3\text{V} - 1\text{V}}$$

(5) Specified by design

Electrical Characteristics (continued)

$V_{CC} = 3\text{ V}$ to 5.5 V and $T_A = -40^\circ\text{C}$ to 85°C ; typical values are at $V_{CC} = V_{LED} = 3.5\text{ V}$, $T_A = 25^\circ\text{C}$, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CC(0)}	Supply current ⁽⁵⁾	GCLK = LAT = SCLK = SIN = GND, GS _n = 0000h, BC = 00h, PCHG_EN = 0, V _{OUTn} = V _{CC} , R _{IREF} = open	3	4.5	6	mA
I _{CC(1)}		GCLK = LAT = SCLK = SIN = GND, GS _n = 0000h, BC = 36h, PCHG_EN = 0, V _{OUTn} is floating, R _{IREF} = 1.27 kΩ (I _{OUTn} = 10-mA target)	4	6.5	8	mA
I _{CC(2)}		GCLK = LAT = SCLK = SIN = GND, GS _n = 0000h, BC = 7Eh, PCHG_EN = 0, V _{OUTn} is floating, R _{IREF} = 1.27 kΩ (I _{OUTn} = 20-mA target)	4	7.5	9	mA
I _{CC(3)}		LAT = SCLK = SIN = GND, GCLK = 33 MHz, GS _n = FFFFh, BC = 36h, PCHG_EN = 0, V _{OUTn} = 1 V, R _{IREF} = 1.27 kΩ (I _{OUTn} = 10-mA target)	4.7	7	10	mA
I _{CC(4)}		LAT = SCLK = SIN = GND, GCLK = 33 MHz, GS _n = FFFFh, BC = 7Eh, PCHG_EN = 0, V _{OUTn} = 1 V, R _{IREF} = 1.27 kΩ (I _{OUTn} = 20-mA target)	4.7	7.7	10	mA
I _{CC(6)}		In power-save mode, PCHG_EN = 0, R _{IREF} = 1.60 kΩ		1	1.5	mA
R _{DW}	Pulldown resistor	LAT	250	480	750	kΩ
		GCLK	250	480	750	

7.6 Switching Characteristics

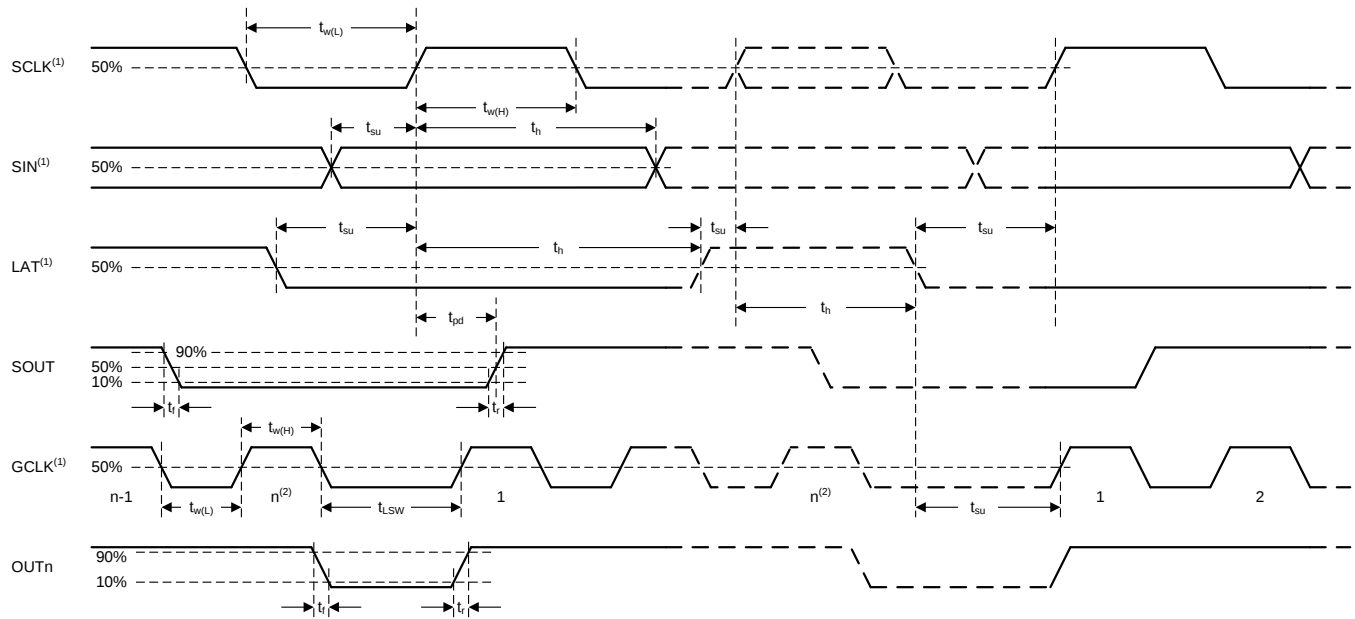
$V_{CC} = 3\text{ V}$ to 5.5 V and $T_A = -40^\circ\text{C}$ to 85°C ; Typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{LED} = 5\text{ V}$, over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(0)}$	SOUT		2		ns
$t_{r(1)}$	Rise time ⁽¹⁾ OUT _n , BC = 7Eh, V _{OUTn} = 1 V, R _{IREF} = 1.02 k Ω (I _{OUTn} = 25-mA target), $T_A = 25^\circ\text{C}$, $R_L = 160\ \Omega$		20		ns
$t_{f(0)}$	SOUT		2		ns
$t_{f(1)}$	Fall time ⁽¹⁾ OUT _n , BC = 7Eh, V _{OUTn} = 1 V, R _{IREF} = 1.02 k Ω (I _{OUTn} = 25-mA target), $T_A = 25^\circ\text{C}$, $R_L = 160\ \Omega$		15		ns
$t_{pd(0)}$	Propagation delay ⁽¹⁾ SCLK $\uparrow$ to SOUT $\uparrow\downarrow$, SEL_TD0 = 00b		5		ns
	SCLK $\uparrow$ to SOUT $\uparrow\downarrow$, SEL_TD0 = 01b		10		ns
	SCLK $\uparrow$ to SOUT $\uparrow\downarrow$, SEL_TD0 = 10b		20		ns
	SCLK $\downarrow$ to SOUT $\uparrow\downarrow$, SEL_TD0 = 11b		5		ns
$t_{pd(1)}$	LAT $\downarrow$ to SOUT, read LOD information		25	50	ns

(1) Specified by design

TLC6946, TLC6948

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- (1) Pulse rise and fall times are 1 ns–3 ns
 (2) The last GCLK of each display segment in the sub period

图 1. Timing Diagram

7.7 Typical Characteristics

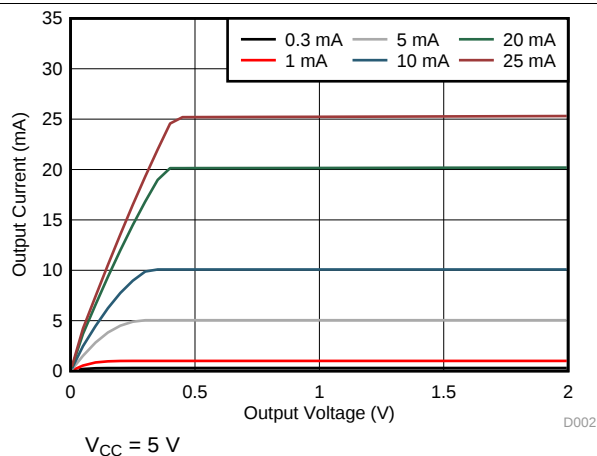


Figure 2. Channel Sink Current vs OUTn Voltage

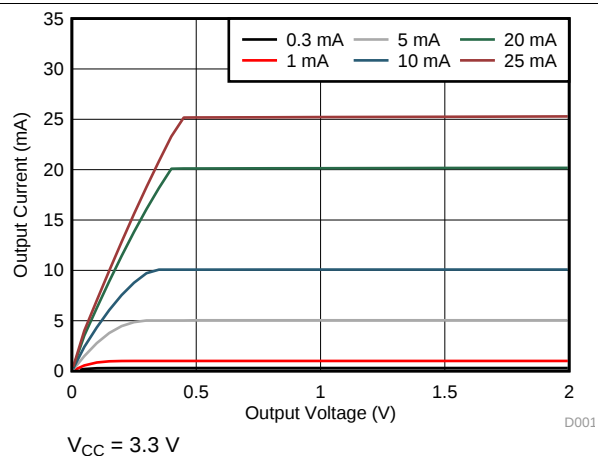


Figure 3. Channel Sink Current vs OUTn Voltage

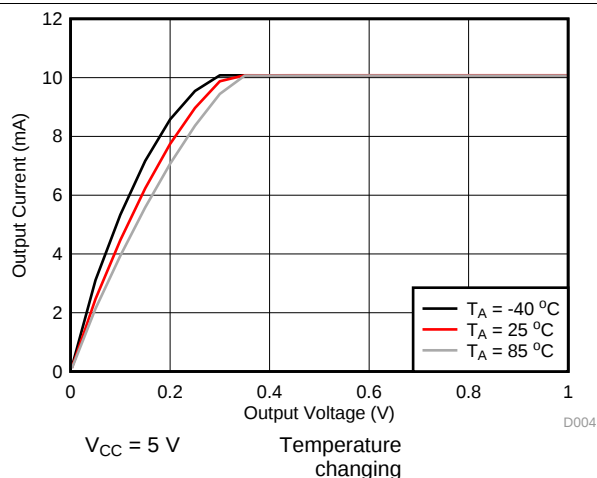


Figure 4. Channel Sink Current vs OUTn Voltage

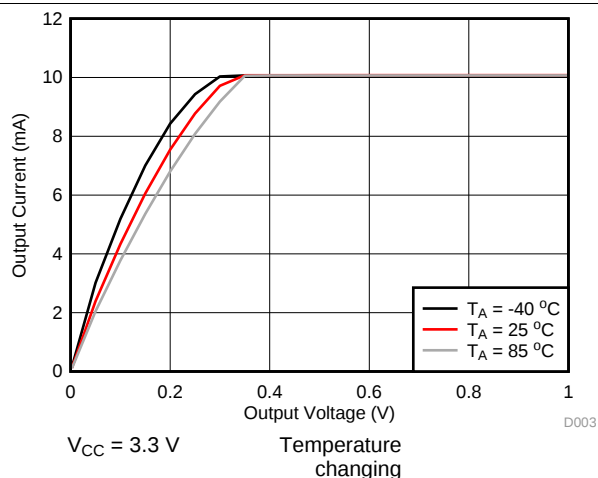


Figure 5. Channel Sink Current vs OUTn Current

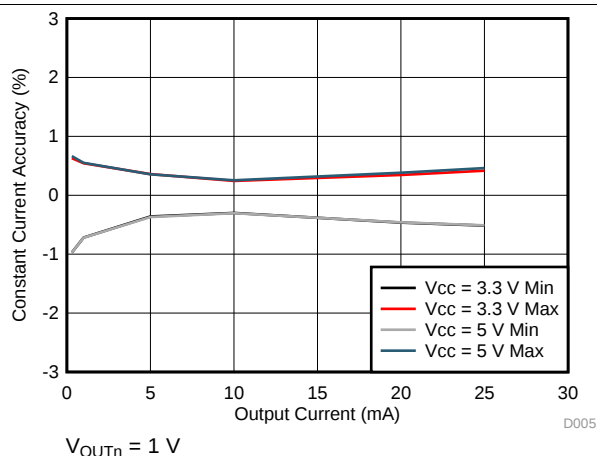


Figure 6. Channel to Channel Accuracy vs OUTn Current

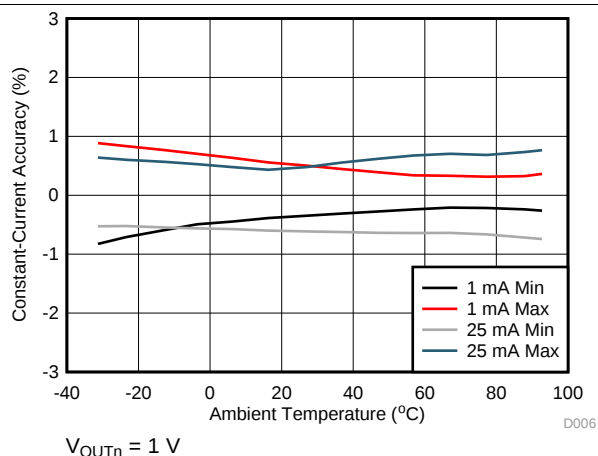


Figure 7. Channel to Channel Accuracy vs Temperature

Typical Characteristics (continued)

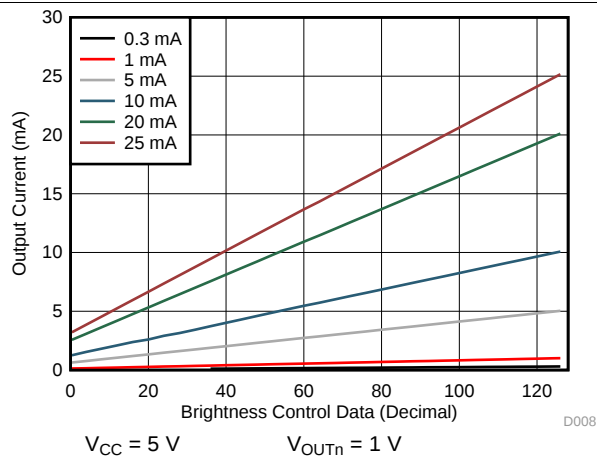


FIG 8. Channel Sink Current vs Brightness Control (BC)

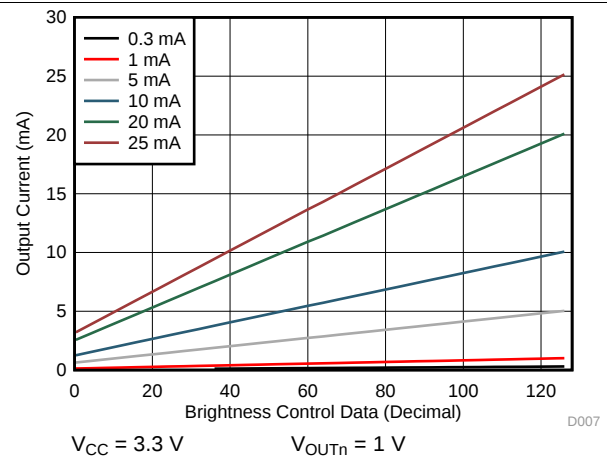


FIG 9. Channel Sink Current vs Brightness Control (BC)

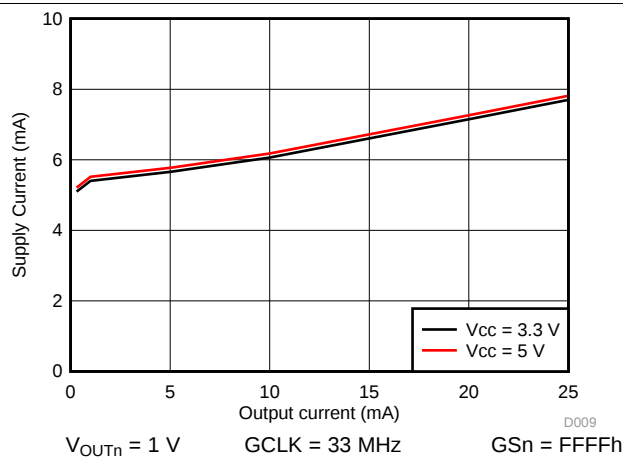


FIG 10. Supply Current (I_{CC}) vs Channel Sink Current

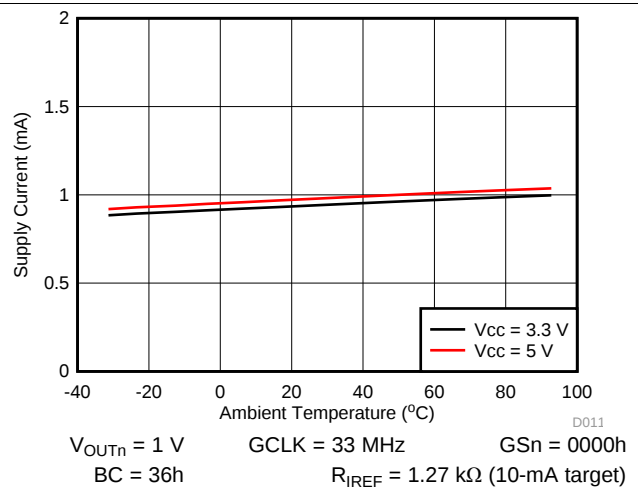
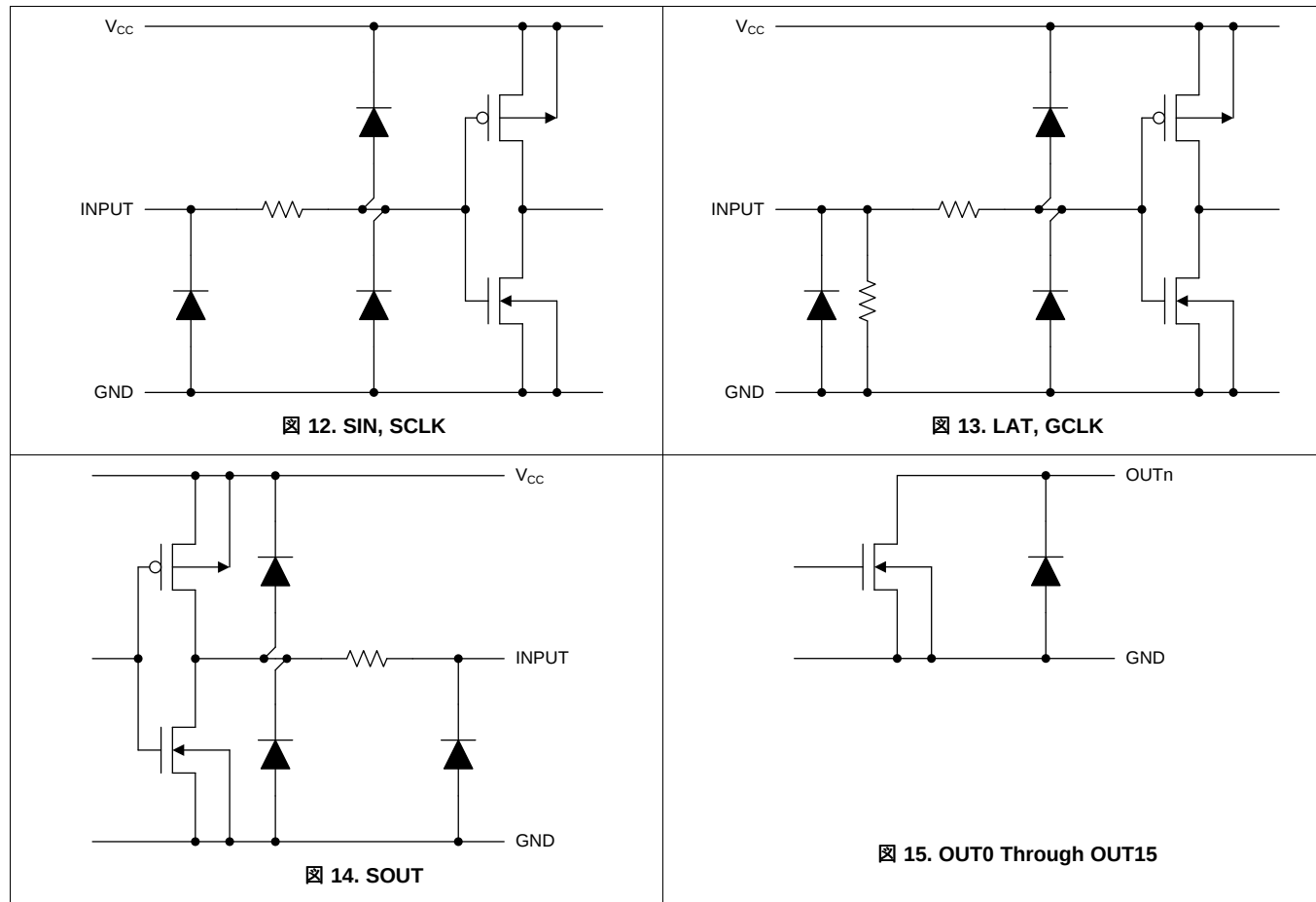


FIG 11. Supply Current (I_{CC}) in Power-Save Mode vs Temperature

8 Parameter Measurement Information

8.1 Pin Equivalent Input and Output Schematic Diagrams



9 Detailed Description

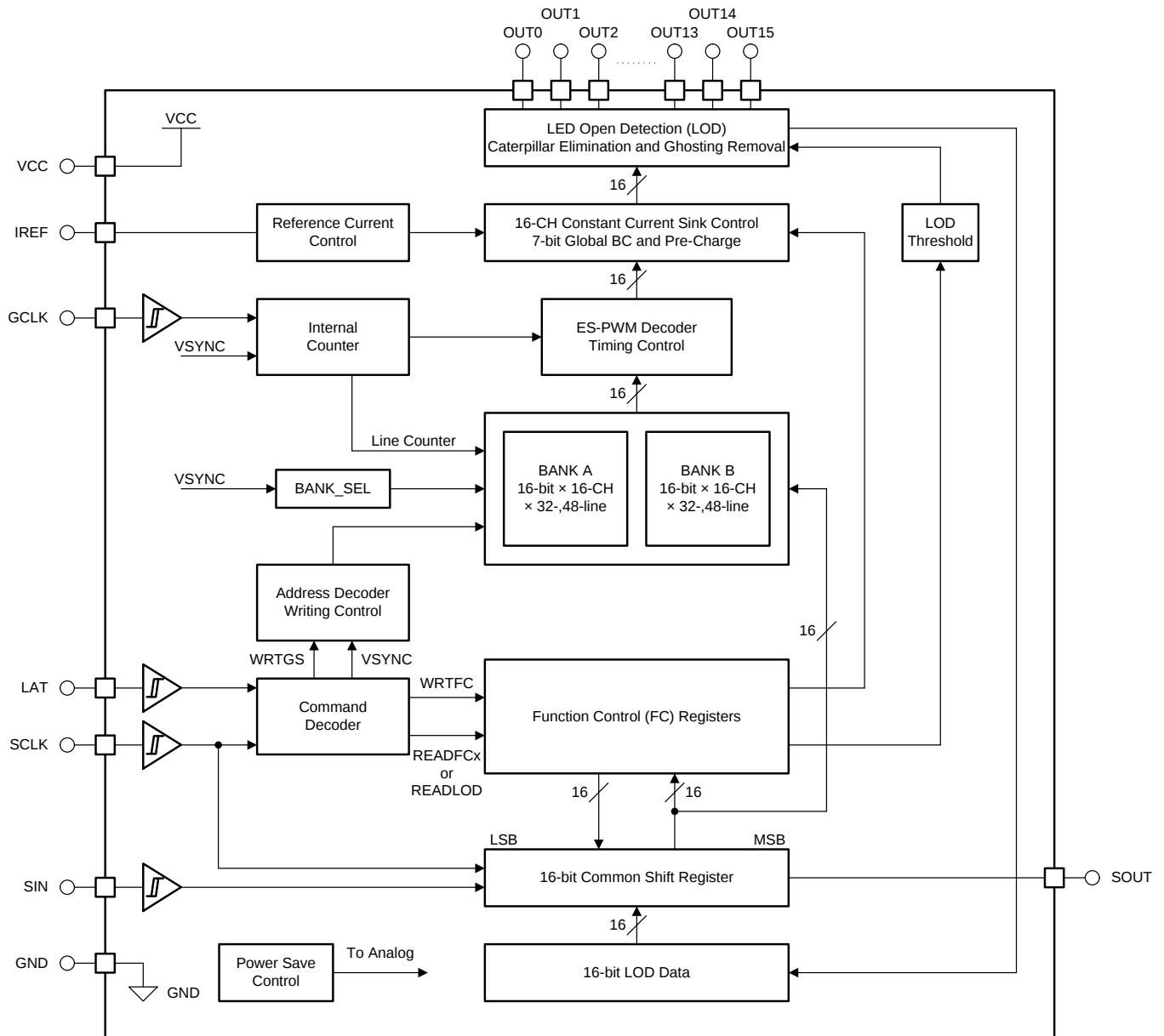
9.1 Overview

The TLC694x device is a 16-channel constant-current-sink LED driver supporting 1- to 32-, 48-multiplexing. Each channel has an individually adjustable 65,536-step pulse-width modulation (PWM) grayscale (GS) control. The TLC6946 device implements 16-Kbit display memory and the TLC6948 device implements 24-Kbit display memory to increase the visual refresh rate and to decrease the grayscale data-writing frequency.

The TLC694x device supports current from 0.3 mA to 25 mA for each channel, with typical 1% channel-to-channel current deviation and typical 1% device-to-device current deviation. The maximum current value of all 16 channels is set by an external IREF resistor and can be adjusted by the 128-step global brightness control (BC). The device also implements low-grayscale enhancement technology to solve the coupling issue and improve the display quality in low-grayscale conditions. These features make the TLC694x device a candidate for high-density-multiplexing LED-matrix-display and LED-panel applications.

The TLC694x device integrates enhanced circuits to solve the various display issues in fine-pitch LED display applications: the low-grayscale uniformity issue, coupling issue, ghosting issue, and caterpillar issue. The TLC694x device features an LED-open detection function, and the error detection results can be read via a serial data-interface port. Thermal shutdown and I_{REF} -resistor short protection ensure a higher system reliability. The TLC694x device also has a smart power-save mode that sets the total current consumption to 1 mA (typical) when all outputs are off.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Built-In 16Kb Display Memory (SRAM)

The TLC6946 device integrates 16K bits of SRAM to support 1- to 32-multiplexing and the TLC6948 device integrates 24K bits of SRAM to support 1- to 48-multiplexing. SRAM is divided into two BANKs: BANK A and BANK B. While BANK A is displaying, BANK B is ready to receive the data of the next frame. While BANK B is displaying, BANK A is ready to receive the data of next frame.

9.3.2 GCLK Dual-Edge Operation

The TLC694x device uses the rising edge or both edges of GCLK. The selection is made by setting the GCLK_EDGE bit in the function control register. By default, the TLC6946 device uses the GCLK rising edge, and the maximum input GCLK frequency is 33 MHz. By setting GCLK_EDGE = 1, the TLC694x device operates at both GCLK edges (rising and falling), and the maximum internal GCLK frequency is 50 MHz with external 25MHz input.

9.3.3 Programmable Constant-Sink Channel Current

9.3.3.1 Global Brightness Control (BC)

The TLC694x device is able to adjust the output current of all constant-current outputs simultaneously. This function is called global brightness control (BC). The global BC for all outputs is programmed with a 7-bit word, thus all output currents can be adjusted in 128 steps from 12.5% to 100.69% for a given current-programming resistor, R_{IREF} (See 表 1). BC data can be set through the serial interface. When the BC data changes, the output current also changes immediately. When the device is powered on, the BC data in the function control register is set to 36h as the default value.

表 1. Global BC Data vs Constant-Current Ratio and Set Current Value

BC DATA			GAIN	RATIO OF GAIN / GAIN_MAX (AT MAX BC)	I_{OUT} (mA) (I_{OLCmax} = 25 mA, TYP)	I_{OUT} (mA) (I_{OLCmax} = 2.4 mA, TYP)
BINARY	DECIMAL	HEX				
000 0000	0	00	4	12.5%	3.13	0.3
000 0001	1	01	4.22	13.19%	3.3	0.32
000 0010	2	02	4.44	13.88%	3.47	0.33
...	...	...	...	...	...	...
011 0101	53	35	15.78	49.31%	12.33	1.18
011 0110 (Default)	54 (Default)	36 (Default)	16	50%	12.5	1.2
011 0111	55	37	16.22	50.69%	12.67	1.22
...	...	...	...	...	...	...
111 1101	125	7D	31.78	99.31%	24.83	2.38
111 1110	126	7E	32	100%	25	2.4
111 1111	127	7F	32.22	100.69%	25.17	2.42

9.3.3.2 Select R_{IREF} for a Given BC

The maximum current per channel, I_{OLCmax} , is determined by resistor R_{IREF} , placed between the IREF and GND pins. The voltage on IREF is typically 0.8 V. R_{IREF} can be calculated by 式 1.

$$R_{IREF} (k\Omega) = \frac{V_{IREF} (V)}{I_{OLCmax} (mA)} \times \text{Gain} = \frac{V_{IREF} (V)}{I_{OLCmax} (mA)} \times 32 \times \left(\frac{1}{8} + \frac{BC}{144} \right)$$

where

- V_{IREF} is the internal reference voltage on I_{REF} (0.8 V)
- I_{OLCmax} is the maximum current for each channel
- Gain is the current gain at BC = 7E (See 表 1)

(1)

R_{IREF} must be between 1.02 k Ω and 10.7 k Ω in order to hold the channel sink current I_{OLC} between 25 mA (typical) and 0.3 mA (typical). Otherwise, the output may be unstable.

表 2. Maximum Constant Current vs External Resistor R_{IREF}

I_{OLCmax} (mA)	R_{IREF} (k Ω , typical)
25	1.02
20	1.28
15	1.71
10	2.56
5	5.12
2.4	10.7

9.3.4 Grayscale (GS) Function (PWM Control)

The TLC694x device can adjust the brightness of each output channel using a pulse-width-modulation (PWM) control scheme. The architecture of 16 bits per channel results in 65536 brightness steps, from 0% up to 100% brightness. The on-time (t_{OUT_ON}) of each output (OUTn) can be calculated by 式 2.

$$t_{OUT_ON} = t_{GCLK} \times GS_n$$

where GS_n is the grayscale of channel OUTn (2)

The TLC694x device implements an enhanced spectrum (ES) PWM control. The ES-PWM control can be selected with two different modes: 8-bit MSB + 8-bit LSB (8+8) mode, and 9-bit MSB + 7-bit LSB (9+7) mode. See [TLC6946 Technical Reference Manual](#) for more details.

9.3.5 Serial Data Interface

The TLC6948 has a flexible serial interface that can be connected to microcontrollers or digital signal processors in various ways. Only three pins are needed to input data into the device. More than two TLC6948s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. The SOUT pin can also be connected to the controller to read back data from the TLC6948 device.

9.3.6 LED-Open Detection (LOD)

The LED-open detection (LOD) function detects faults caused by an open circuit in any LED string or a short from OUTn to ground with low impedance. It does this by comparing the OUTn voltage to the LOD-detection threshold-voltage level set by LODVTH in the function control register. If the OUTn voltage is lower than the programmed voltage, the corresponding output LOD bit is set to 1 to indicate an open LED. Otherwise, the output of that LOD bit is 0. LOD data output by the detection circuit are valid only during the on period of that OUTn output channel.

9.3.7 Caterpillar Removal

The TLC694x device implements an internal circuit that can eliminate the caterpillar issue caused by an open LED. The caterpillar effect is a common issue for LED panels. The caterpillar removal function is enabled by setting LODRM_EN to 1 (default value after device powered on) in the function control register. When this function is enabled, the device automatically detects the open LED, and the corresponding channel does not turn on until device reset.

9.3.8 Precharge FET

The TLC694x internal precharge FET can prevent ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current from parasitic capacitance on OUTn through the LED when the supply voltage switches from one common line to the next common line. To prevent this unwanted charging current, the TLC694x device uses an internal FET to pull up OUTn during the common-line switching period. As a result, no charging current flows through LED and ghosting is eliminated.

9.3.9 Thermal Shutdown

The thermal shutdown (TSD) function turns off all device constant-current outputs when the junction temperature (T_J) exceeds 170°C (typical). It resumes normal operation when T_J falls below 155°C (typical).

9.3.10 IREF Resistor Short Protection (ISP)

The IREF resistor short protection (ISP) function prevents unwanted large currents from flowing through the constant-current output when the IREF resistor is shorted accidentally. The TLC694x device turns off all output channels when the IREF pin voltage is lower than 0.19 V (typical). When the IREF pin voltage goes higher than 0.325 V (typical), the TLC694x device resumes normal operation.

9.4 Device Functional Modes

9.4.1 Normal Operating Mode

The TLC694x device is fully functional when V_{CC} reaches 3 V and is below 5.5 V. After power on, all OUTn of the TLC694x device are turned off. All the internal counters and function control registers are initialized. Write the proper grayscale data and function control data to enable normal device operation.

9.4.2 Power-Save Mode (PSM)

The power-save mode (PSM) is enabled by setting PSM_EN to 1 in the function control register.

When powered on, the default value of this bit is 0. When this function is enabled, if all the GS data received for the next frame are 0, then device enters power-save mode during the display of the next frame. When the device is in power-save mode, it resumes normal mode when it detects non-zero GS data input. In power-save mode, part of analog circuits are not operational; the device total current consumption, I_{CC} , is 1 mA(typical).

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLC6948 device is a 16-channel constant-current sink LED driver supporting 1- to 48-multiplexing. Each channel has an individually adjustable 65,536-step pulse-width-modulation (PWM) grayscale (GS) control. The TLC6948 device implements 24 Kbits of display memory to increase the visual refresh rate and to decrease the grayscale data writing frequency. This integrated memory makes TLC6948 a potential for high-density, fine-pitch LED matrix applications.

10.2 Typical Application

The TLC6948 is typically connected in series to drive the LED matrix with only a few controller ports. [Figure 16](#) shows a typical application diagram with TLC6948 devices connected in cascade for an LED matrix.

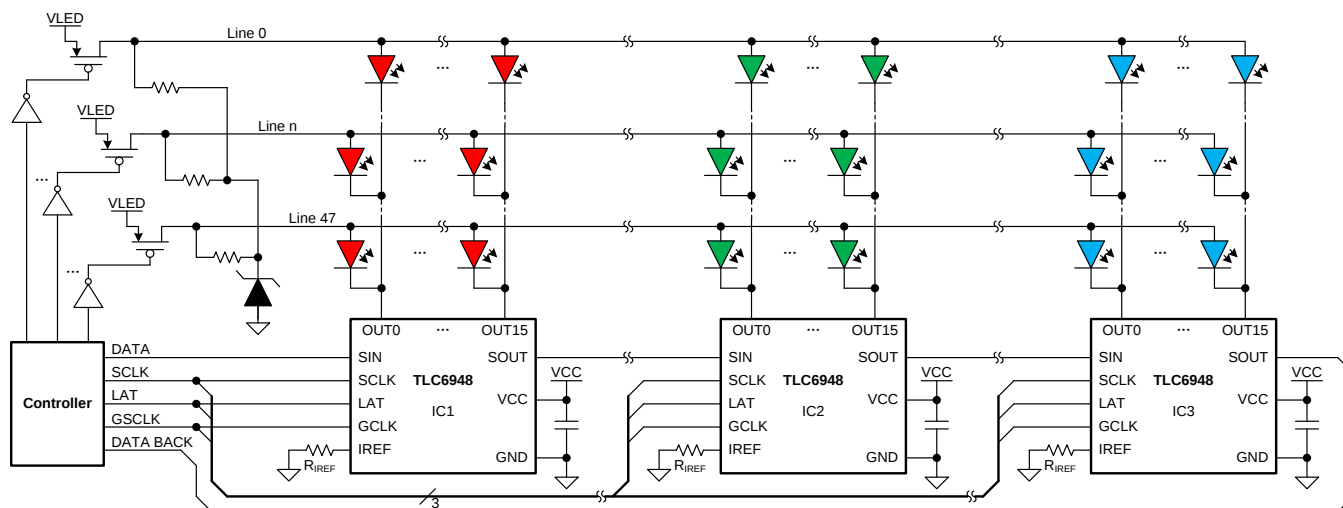


Figure 16. Cascading Three TLC6948 Devices

10.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC} and V_{LED} voltage	3 V to 5.5 V
SIN, SCLK, LAT, and GCLK voltage range	Low level = GND, high level = V_{CC}
The maximum LED forward voltage, $V_{(F)}$	Red LED 2V, green and blue LED 3V
The maximum current for each color LED, I_{OLCmax}	Red LED 10mA, green LED 6mA, blue LED 4mA.

10.2.2 Detailed Design Procedures

10.2.2.1 Power Supply Voltage

The LED power supply voltage V_{LED} must be higher than $V_{(F)} + V_{(KNEE)}$. The device power supply voltage, V_{CC} should be equal or higher than V_{LED} . One example value is $V_{LED} = V_{CC} = 3.8\text{ V}$. See [TLC6946 Technical Reference Manual](#) for more details.

10.2.2.2 Channel Current and Brightness Control

See [Global Brightness Control \(BC\)](#) and [Select \$R_{IREF}\$ for a Given BC](#). Select the reference-current-setting resistor R_{IREF} to set the maximum channel current for each color LED. Select the BC data for the best white balance of the red, green, and blue LED lamp. See [TLC6946 Technical Reference Manual](#) for more details.

10.2.2.3 SCLK and GCLK Frequency

SCLK is the serial data shift-in clock signal; and GCLK is the PWM-control reference-clock signal. 式 3 shows the minimum frequency requirement for GCLK and SCLK. See [TLC6946 Technical Reference Manual](#) for more details.

$$f_{GCLK} = m \times n \times f_{VR}$$

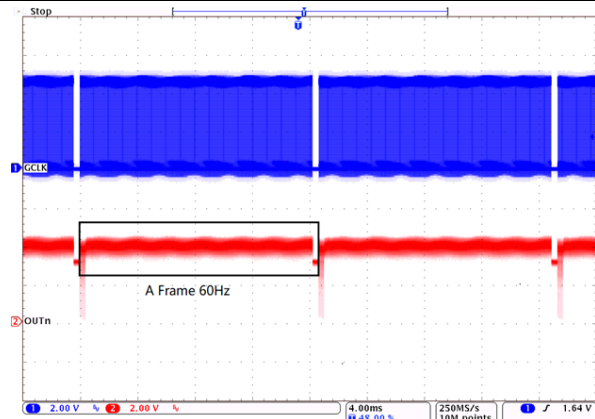
$$f_{SCLK} = N \times n \times 256 \times f_{FPS}$$

where

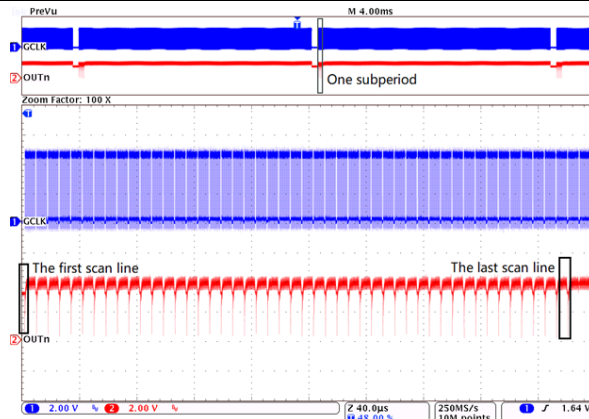
- f_{GCLK} is the minimum GCLK frequency for single-edge operating mode
- f_{SCLK} is the minimum SCLK frequency
- m is the GCLK number of each sub-period, determined by the PWM mode selected
- f_{VR} is the visual refresh rate of the entire cascading series
- N is the number of cascaded TLC6948 devices
- n is the number of scan lines
- f_{FPS} is the frame rate

(3)

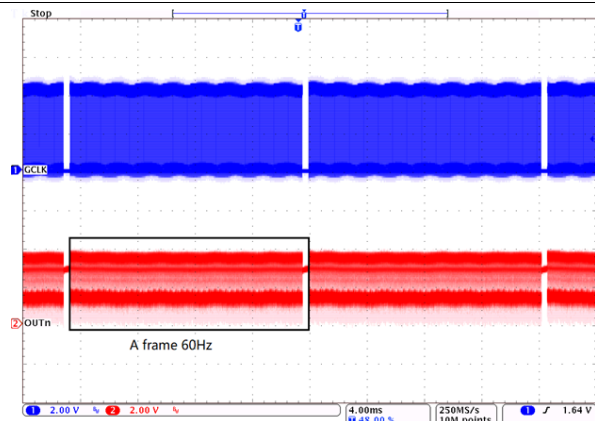
10.2.3 Application Curves



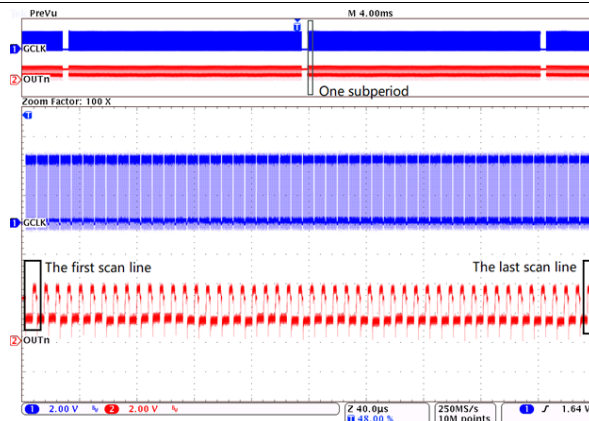
17. OUTn Waveform for ES-PWM Mode (GSn = 0001h)



18. OUTn Waveform for ES-PWM Mode Zooming in One Sub-period (GSn = 0001h)



19. OUTn Waveform for ES-PWM Mode (GSn = FFFFh)



20. OUTn Waveform for ES-PWM Mode Zooming in One Sub-period (GSn = FFFFh)

11 Power Supply Recommendations

Decouple the V_{CC} power supply voltage by placing a 0.1- μ F ceramic capacitor close to the V_{CC} pin and GND plane. Depending on panel size, several equally distributed electrolytic capacitors must be placed on the board for a well-regulated LED supply voltage V_{LED} . V_{LED} voltage ripple must be less than 5% of its nominal value.

12 Layout

12.1 Layout Guidelines

Place the decoupling capacitor near the V_{CC} pin and GND plane.

Place the current-programming resistor, R_{IREF} , close to the IREF pin and the GND pin.

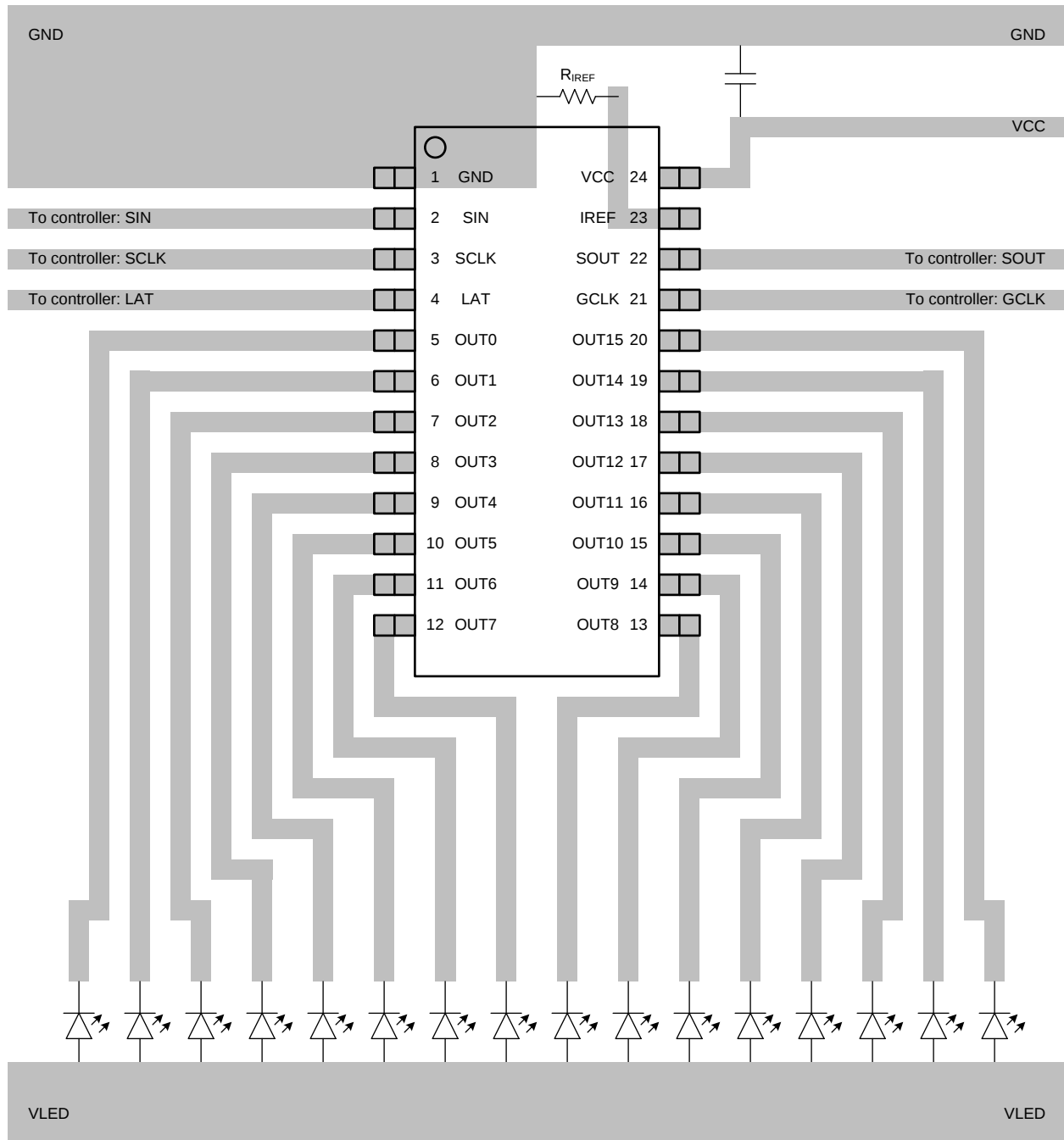
Make the GND trace as wide as possible for large GND currents.

Routing between the LED cathode and the device OUTn pin must be as short and straight as possible to reduce wire inductance.

The thermal pad (QFN package) must be connected to the GND plane. Because the thermal pad is used as a power ground pin internally, there is a large current flow through this pad when all channels turn on. Furthermore, connect the thermal pad to a heat sink layer by thermal vias to reduce device temperature. One suggested thermal via pattern is shown in [Layout Examples](#). For more information about suggested thermal via pattern and via size, see [PowerPAD Thermally Enhanced Package](#).

MOSFETs must be placed in the middle of the board, which should be laid out as symmetrically as possible.

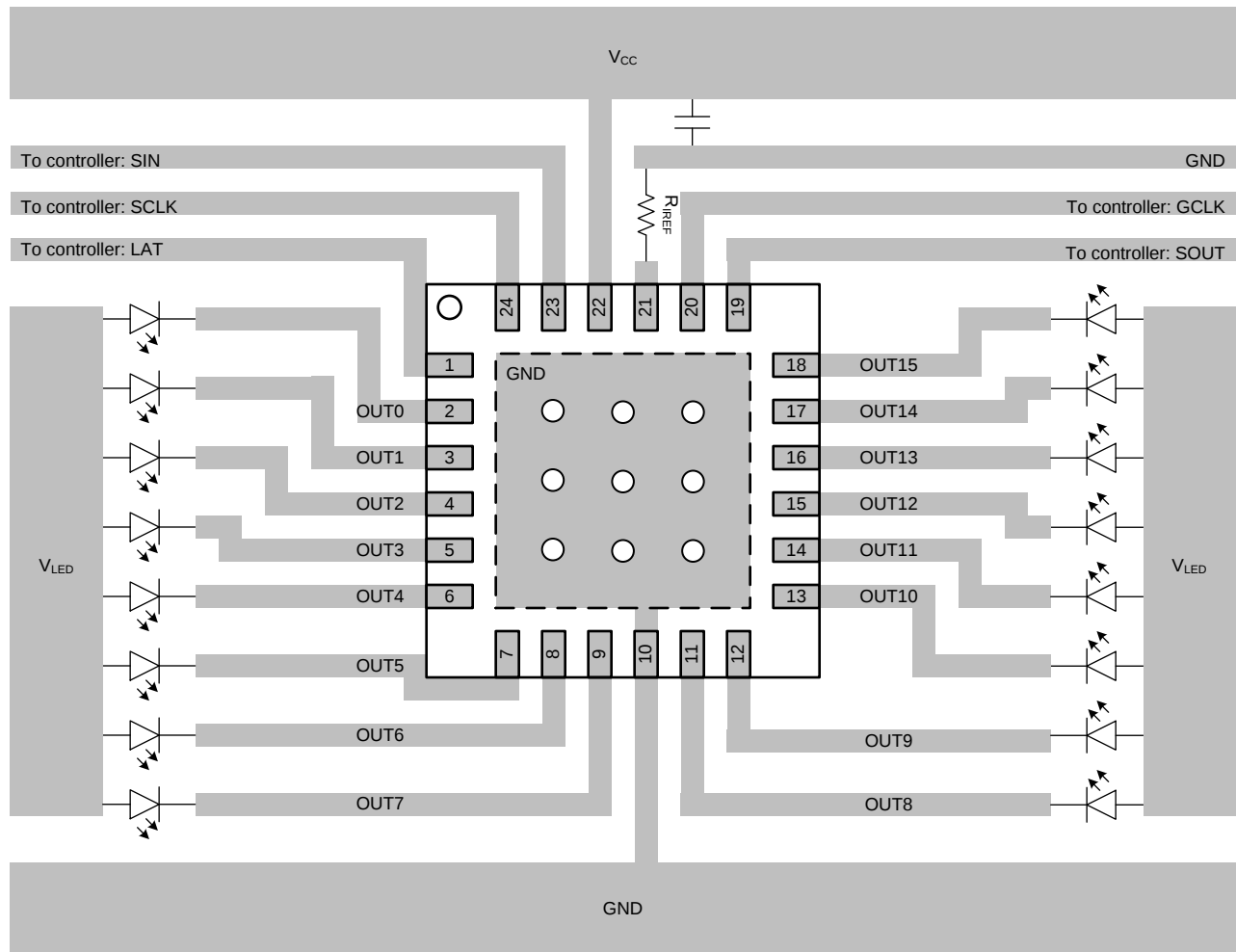
12.2 Layout Examples



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21. SSOP-24 Package Layout Example

Layout Examples (continued)



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22. VQFN-24 Package Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください。

- 『[TLC694x 16チャンネルLEDドライバ・テクニカル・リファレンス・マニュアル](#)』
- 『[半導体およびICパッケージの熱指標](#)』

13.2 関連リンク

表 4 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLC6946	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLC6948	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

13.5 商標

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13.6 静電気放電に関する注意事項



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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC6946DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6946
TLC6946DBQR.A	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6946
TLC6946RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TLC 6946
TLC6946RGER.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TLC 6946
TLC6948DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6948
TLC6948DBQR.A	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6948
TLC6948RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TLC 6948
TLC6948RGER.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TLC 6948

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6946DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC6946RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC6948DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC6948RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

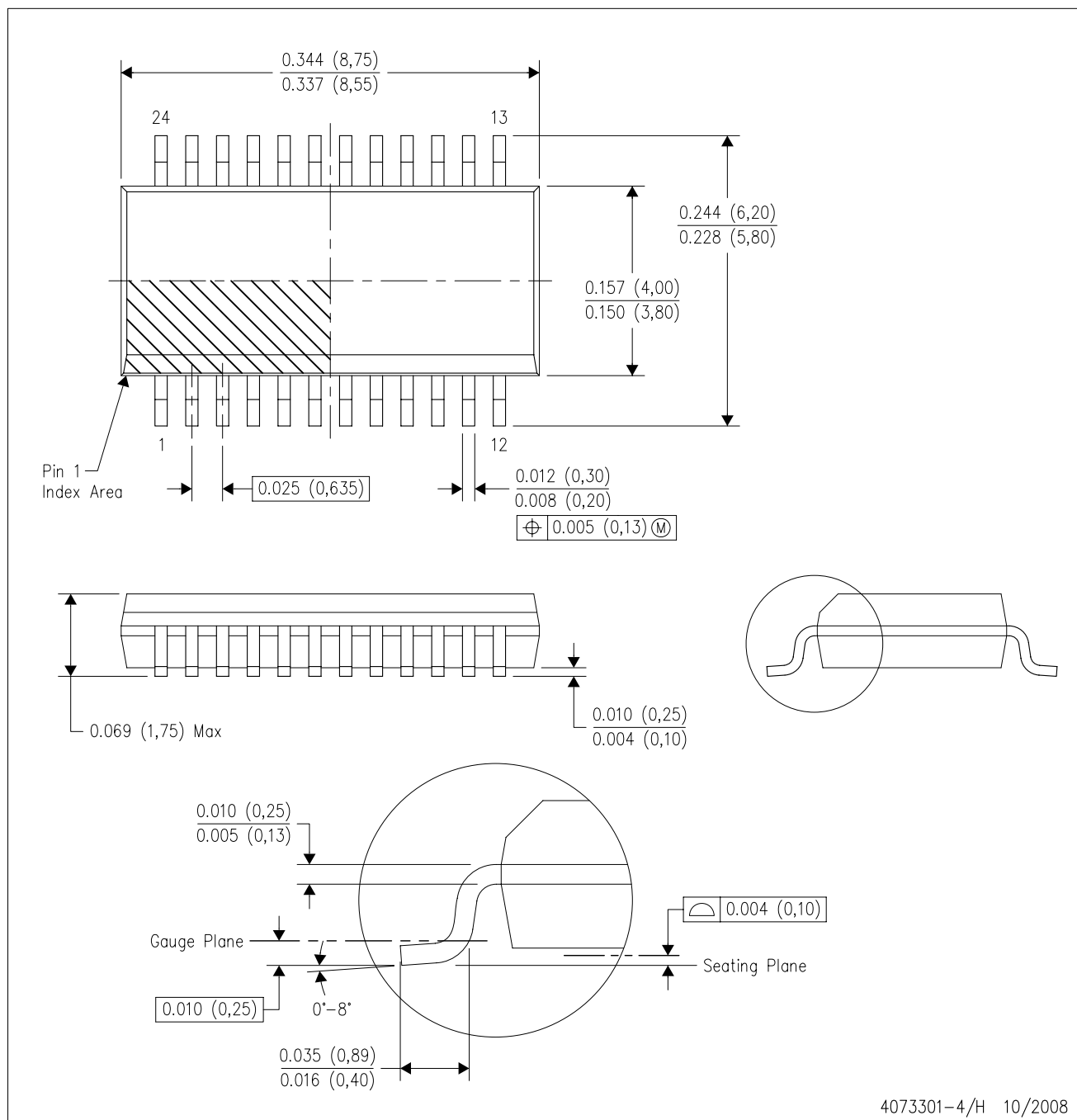


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6946DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
TLC6946RGER	VQFN	RGE	24	3000	360.0	360.0	36.0
TLC6948DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
TLC6948RGER	VQFN	RGE	24	3000	360.0	360.0	36.0

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



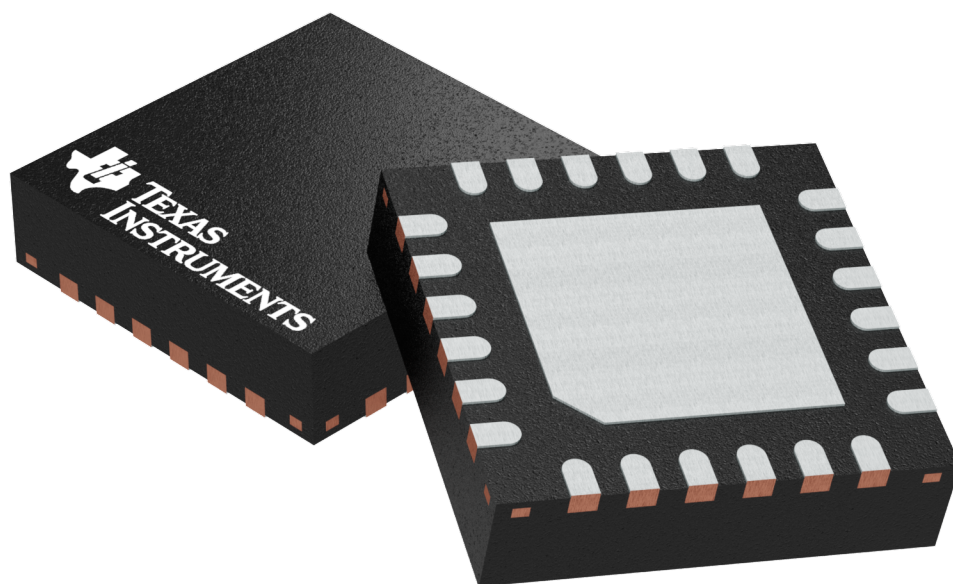
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

RGE 24

GENERIC PACKAGE VIEW

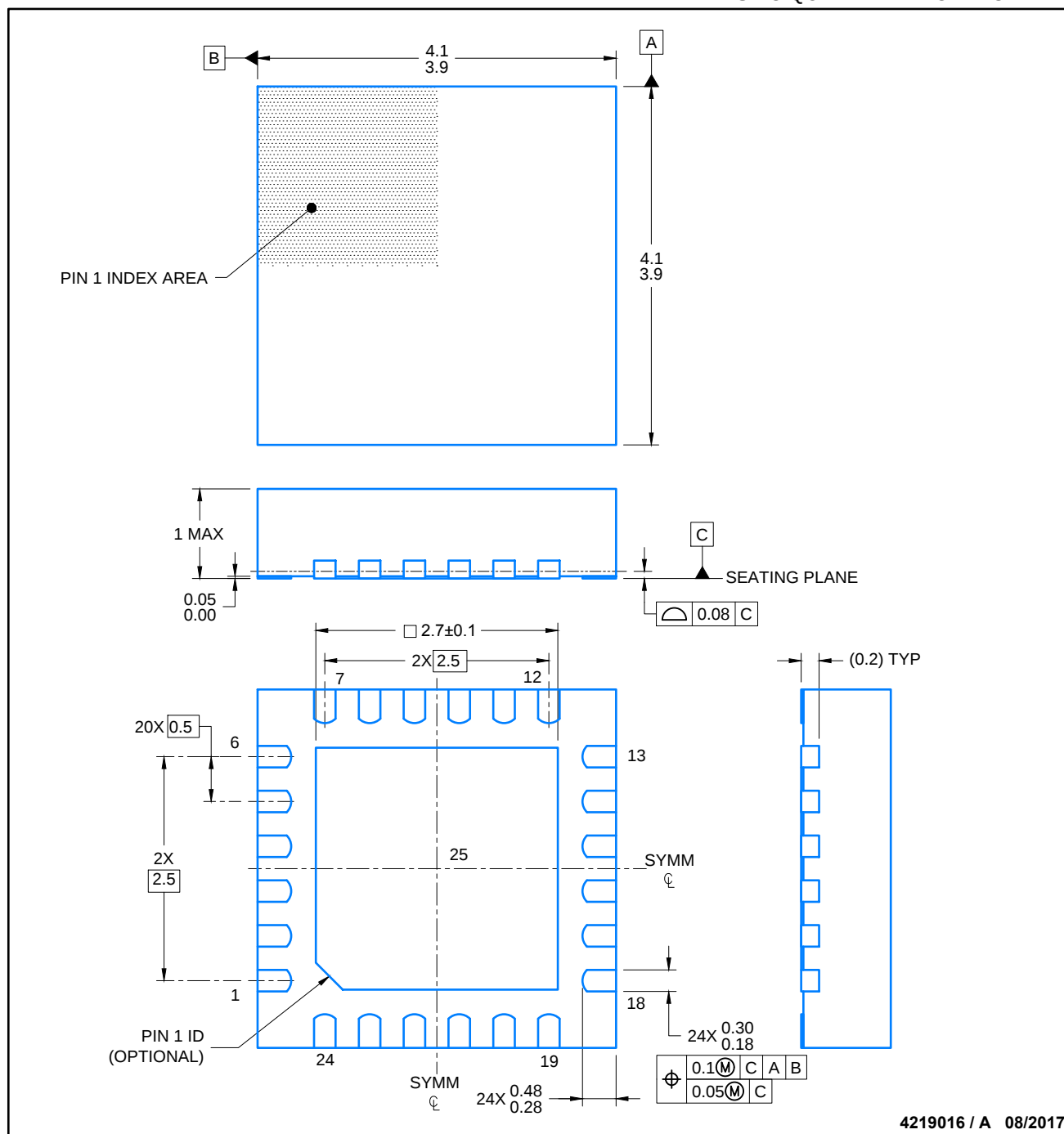
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



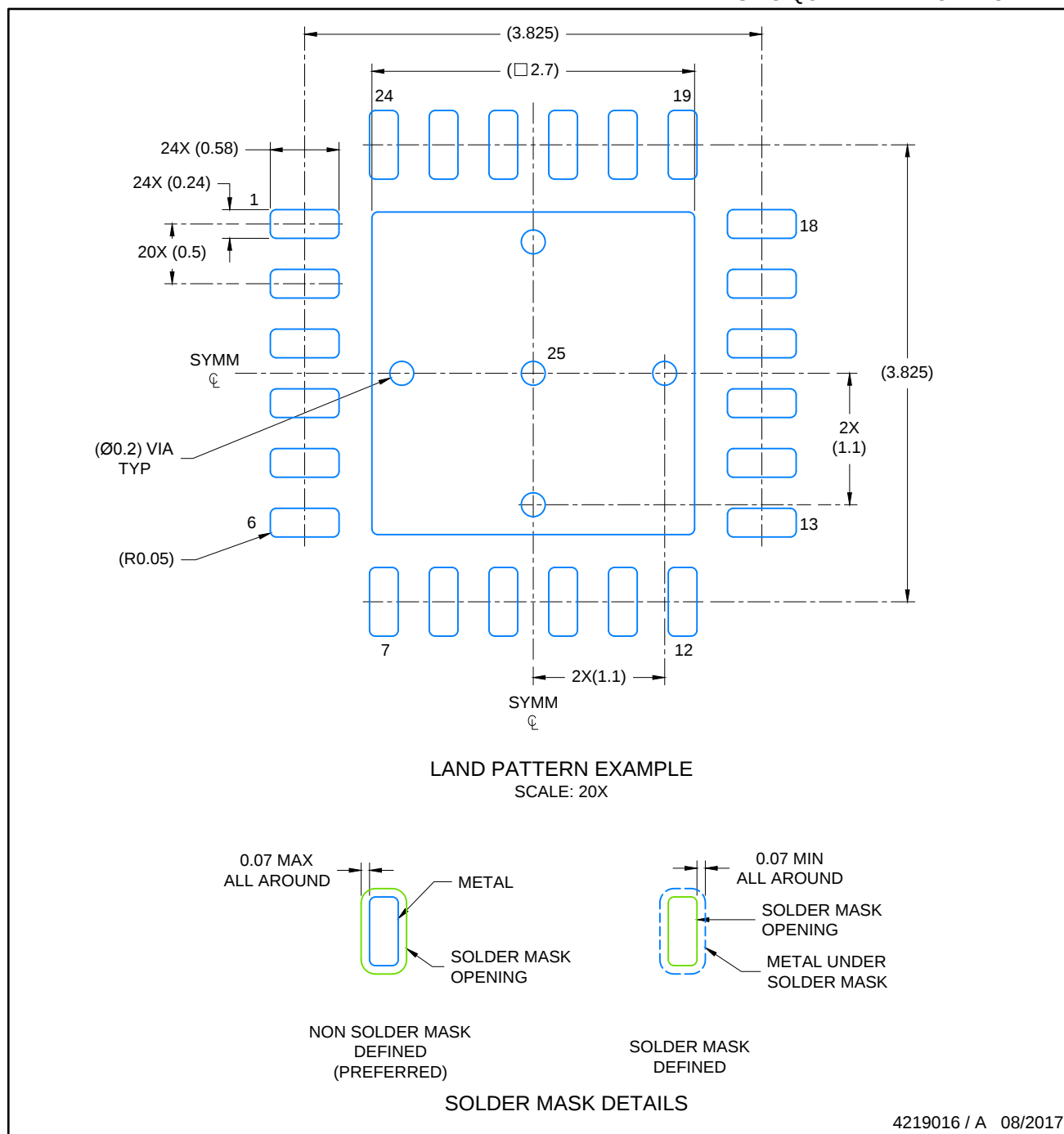
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



NOTES:

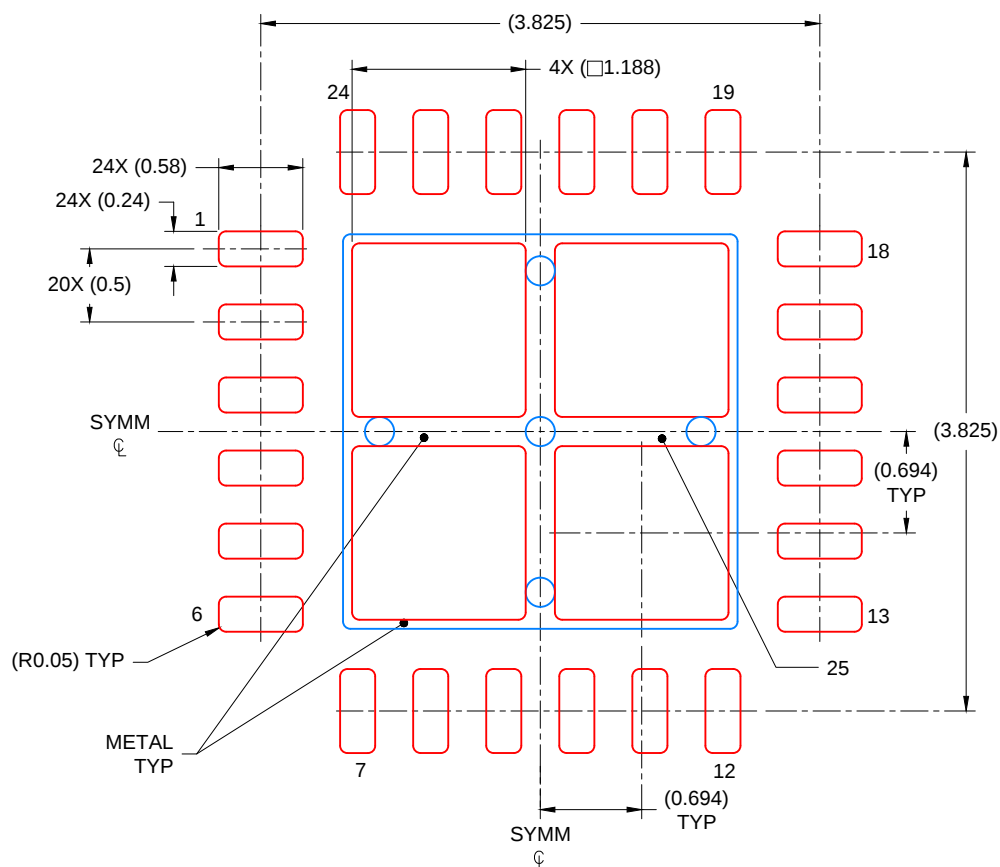
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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