TLIN1029-Q1 ドミナント状態タイムアウト機能を備えた LIN (Local Interconnect Network) トランシーバ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - 温度グレード 1:-40℃～125℃、T_A
  - デバイス HBM 認定レベル:±8kV
  - デバイス CDM 認定レベル:±1.5kV
- LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2 A、および ISO/DIS 17987-4.2 に準拠 (「SLLA490」を参照)
- LIN 用の SAE J2602 推奨プラクティスに準拠 (「SLLA490」を参照)
- ISO 9141 (K ライン) をサポート
- 12V アプリケーションをサポート
- 最高 20kbps の LIN 送信データ・レート
- 広い動作範囲
  - 4V～36V の電源電圧
  - ±45V の LIN バス・フォルト保護
- スリープ・モード:超低消費電流で、以下に示すウェークアップ・イベントに対応
  - LIN バス
  - EN 経由のローカル・ウェークアップ
- 電源オンおよびオフ時のグリッチ・フリー動作
- 保護機能:
  - V_{SUP} の低電圧保護
  - TXD ドミナント・タイムアウト保護 (DTO)
  - サーマル・シャットダウン保護機能
  - 電源なしノードまたはグランド切断に対するシステム・レベルのフェイルセーフ
- SOIC (8) パッケージと自動光学検査 (AOI) 性能を向上させたリードレス VSON (8) パッケージで供給

2 アプリケーション

- ボディ・エレクトロニクス / 照明
- インフォテインメントとクラスタ
- ハイブリッド電気自動車およびパワー・トレイン・システム
- パッシブ型安全運転支援システム
- 家電製品

3 概要

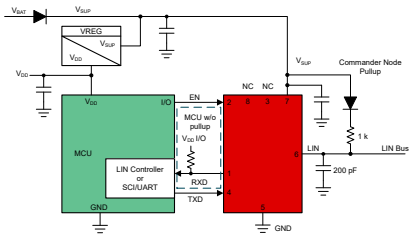
TLIN1029-Q1 は、ウェークアップおよび保護機能を内蔵し、LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2A、および ISO/DIS 17987-4.2 標準に準拠したローカル相互接続ネットワーク (LIN) 物理層トランシーバです。LIN は、データ・レートが最高 20kbps の車内ネットワークとして一般的に使用されている単線式双方向バスです。TLIN1029-Q1 は、幅広い動作電圧に対応し、追加のバス・フォルト保護機能を備えた 12V アプリケーションをサポートするように設計されています。

LIN レシーバは、高速インライン・プログラミング用に最大 100kbps のデータ・レートをサポートしています。TLIN1029-Q1 は、電磁放射 (EME) を低減する電流制限波形整形ドライバを使用して、TXD 入力のデータ・ストリームを LIN バス信号に変換します。このレシーバは、データ・ストリームをロジック・レベル信号に変換し、オープン・ドレインの RXD ピンを経由してマイクロプロセッサに送信します。LIN バスや EN ピンによってウェークアップできるスリープ・モードを使用すれば、非常に低い消費電流を実現できます。

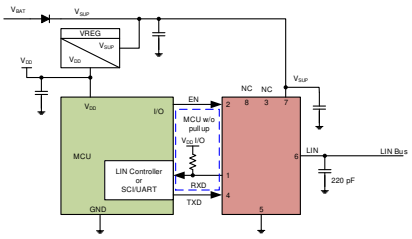
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLIN1029-Q1	SOIC (D) (8)	4.90mm × 3.91mm
	VSON (DRB) (8)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図、コマンダ・モード



概略回路図、レスポンダ・モード

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (May 2020) to Revision F (May 2022) — **Page**

- 旧式の用語を使っている場合、すべてコマンダおよびレスポンダに変更 ... 1

Changes from Revision D (March 2020) to Revision E (May 2020) — **Page**

- 「概要」のリストに「SLLA490 を参照」を追加 ... 1
- Added : See errata TLIN1029-Q1 and TLIN2029-Q1 Duty Cycle Over V_{SUP} ... 8

Changes from Revision C (July 2019) to Revision D (March 2020) — **Page**

- 概略回路図 (コマンダ・モード) の 200pF のコンデンサを 220pF に変更 ... 1
- 概略回路図 (レスポンダ・モード) の 200pF のコンデンサを 220pF に変更 ... 1
- Changed V_{LIN} from MIN = –58, MAX = 58 To: MIN = –60, MAX = 60 in the Absolute Maximum Ratings ... 5
- Changed C_{LINPIN} from MAX = 45 pF To: MAX = 25 pF and added V_{SUP} = 14 V for Test Condition in Electrical Characteristics ... 6
- Changed text From: "... a 200 pF capacitor" To: "... a 220 pF capacitor" For Pin 6 (LIN) in the *Layout Guidelines* ... 29

Changes from Revision B (February 2018) to Revision C (July 2019) — **Page**

- 製品情報の SOIC パッケージの本体サイズを 4.90mm x 6.00mm から 4.90mm x 3.91mm に変更 ... 1
- 概略回路図 (コマンダ・モード) の 220pF のコンデンサを 200pF に変更 ... 1
- 概略回路図 (レスポンダ・モード) の 220pF のコンデンサを 200pF に変更 ... 1
- Changed V_{LOGIC} absolute maximum rating MAX from 5.5 V to 6 V ... 5
- Changed the title of 図 10-2 To: Recessive to Dominant Propagation ... 28
- Changed the title of 図 10-3 To: Dominant to Recessive Propagation ... 28
- Changed text From: "... a 220 pF capacitor" To: "... a 200 pF capacitor" For Pin 6 (LIN) in the *Layout Guidelines* ... 29

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Changes from Revision A (December 2017) to Revision B (February 2018) **Page**

- データシート全体にわたって次のように変更:「Complaint to LIN 2.0」を「Compliant to LIN 2.0 (LIN 2.0 に準拠)」に、「特長」および「概要」で変更 1
- Changed From: "complaint to LIN 2.0..." To: "compliant to LIN 2.0..." in the *Overview* section 21

Changes from Revision * (October 2017) to Revision A (December 2017) **Page**

- デバイス・ステータスを「*事前情報*」から「*量産データ*」に変更 1

5 概要 (続き)

抵抗、静電放電 (ESD) 保護、フォルト保護機能を内蔵しているため、アプリケーションの基板面積を削減できます。

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6 Pin Configuration and Functions

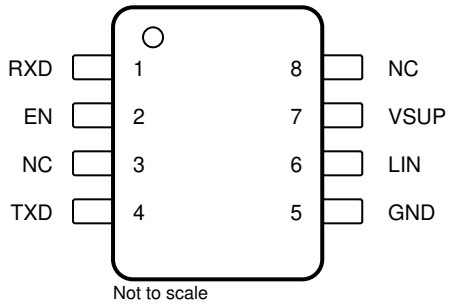


図 6-1. D Package, 8-Pin (SOIC)
(Top View)

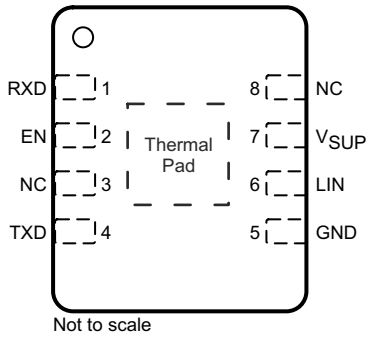


図 6-2. DRB Package, 8-Pin (VSON)
Top View

表 6-1. Pin Functions

PIN		Type	DESCRIPTION
Name	No.		
RXD	1	DO	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	DI	Enable input - High puts the device in normal operation mode and low puts the device in sleep mode
NC	3	–	Not connected
TXD	4	DI	TXD input interface to control state of LIN output - Internally pulled to ground
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V_{SUP}	7	HV Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
NC	8	–	Not connected
Thermal Pad		-	No electrical connection. Can be connected to the PCB to improve thermal coupling (DRB package only)

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7 Specifications

7.1 Absolute Maximum Ratings

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)(1)

Symbol	Parameter	MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987 Param 10)	–0.3	45	V
V_{LIN}	LIN bus input voltage (ISO/DIS 17987 Param 82)	–45	45	V
V_{LOGIC}	Logic pin voltage (RXD, TXD, EN)	–0.3	6	V
T_A	Ambient temperature range	–40	125	°C
T_J	Junction temperature range	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

ESD Ratings				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) TXD, RXD, EN Pins, per AEC Q100-002(1)		±4000	V
		Human body model (HBM) LIN and V_{SUP} Pin, per AEC Q100-002(2)		±8000	
		Charged device model (CDM), per AEC Q100-011	All terminals	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) LIN bus is stressed with respect to GND.

7.3 ESD Ratings - IEC

ESD and Surge Protection Ratings			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 per IEC 62228-3 Contact discharge	±8000	V
$V_{(ESD)}$	Powered ESD Performance, per SAEJ2962-1(1)	contact discharge	±8000	V
		air-gap discharge	±25000	
ISO 7637-2 and IEC 62215-3 transients according to IBEE LIN EMC test specifications(2) (LIN and V_{SUP})		Pulse 1	–100	V
		Pulse 2	75	V
		Pulse 3a	–150	V
		Pulse 3b	100	V

(1) SAEJ2962-1 Testing performed at 3rd party EMC test facility, test report available upon request.
(2) ISO 7637 is a system level transient test. Different system level configurations may lead to diffrent results.

7.4 Thermal Information

THERMAL METRIC(1)		TLIN1029D D (SOIC) 8-PINS	TLIN1029DRB DRB (VSON) 8-PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	115.5	48.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	58.7	55.5	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	58.9	22.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.1	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.2	22.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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7.5 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4		36	V
V_{LIN}	LIN Bus input voltage	0		36	V
V_{LOGIC}	Logic Pin Voltage (RXD, TXD, EN)	0		5.25	V
TSD	Thermal shutdown temperature	165			°C
$TSD_{(HYS)}$	Thermal shutdown hysteresis		15		°C

7.6 Electrical Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range. See 図 8-1 and 図 8-2	4		36	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10)	Normal and Standby Modes: ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50 % duty cycle and 18V swing. See 図 8-1 and 図 8-2	4		36	V
		Sleep Mode	4		36	V
UV_{SUP}	Under voltage V_{SUP} threshold	Min is falling edge and Max is rising edge	2.9		3.85	V
UV_{HYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.2		V
I_{SUP}	Supply current	Normal Mode: EN = high, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF (See 図 8-7)		1	5	mA
		Standby Mode: EN = low, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF (See 図 8-7)		1	2.1	mA
I_{SUP}	Supply current	Normal Mode: EN = high, bus recessive (LIN = V_{SUP})		300	650	µA
		Standby Mode: EN = low, bus recessive (LIN = V_{SUP})		10	30	µA
		Sleep Mode: 4.0 V < V_{SUP} ≤ 14 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating		8	12	µA
		Sleep Mode: 14 V < V_{SUP} ≤ 36 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating			20	µA
TSD	Thermal shutdown		165			℃
$TSD_{(HYS)}$	Thermal shutdown hysteresis			15		℃
RXD OUTPUT PIN (OPEN DRAIN)						
V_{OL}	Output low voltage	R_{PU} = 2.4 kΩ			0.6	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{ILG}	Leakage current, high-level	LIN = V_{SUP}, RXD = 5 V	–5	0	5	µA
TXD INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{ILG}	Low level input leakage current	TXD = low	–5	0	5	µA
R_{TXD}	Internal pull-down resistor value		125	350	800	kΩ
LIN PIN						

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7.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	HIGH level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 7 V to 36 V(1)	0.85			V_{SUP}
		LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 4 V ≤ V_{SUP} < 7 V(1)	3			V
V_{OL}	LOW level output voltage	LIN dominant, TXD = low, V_{SUP} = 7 V to 36 V(1)			0.2	V_{SUP}
		LIN dominant, TXD = low, V_{SUP} = 4 V ≤ V_{SUP} < 7 V(1)			1.2	V
$V_{SUP_NON_OP}$	VSUP where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open LIN = 4 V to 45 V	–0.3		45	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 18 V, R_{MEAS} = 440 Ω, V_{SUP} = 18 V, V_{BUSdom} < 4.518 V See 図 8-6	40	90	200	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	LIN = 0 V, V_{SUP} = 12 V Driver off/ recessive 図 8-7	–1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN > V_{SUP}, 4 V ≤ V_{SUP} ≤ 36 V Driver off; 図 8-8			20	µA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN = V_{SUP}, Driver off; 図 8-8	–5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 18 V, LIN = 0 V; 図 8-9	–1		1	mA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	LIN = 18 V, V_{SUP} = GND; 図 8-10			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up) See 図 8-4, 図 8-3			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive See 図 8-4, 図 8-3	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2 See 図 8-4, 図 8-3	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)	V_{HYS} = (V_{IL} - V_{IH}) See 図 8-4, 図 8-3			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path	By design and characterization	0.4	0.7	1	V
R_{PU-LIN}	Internal pull-up resistor to V_{SUP}	Normal and standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 14 V, LIN = GND	–2		–20	µA
C_{LINPIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF
EN INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
V_{IT}	Hysteresis voltage	By design and characterization		50	500	mV
I_{ILG}	Low level input current	EN = low	–5	0	5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ

(1) LIN driver bus load conditions (C_{LIN}, R_{LIN}): No external load

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7.7 Switching Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)(1)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7.4 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)	0.396			
$D1_{12V}$	Duty Cycle 1(2)	$TH_{REC(MAX)}$ = 0.625 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7.4 V to 9.4 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)	0.368			
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 9.4 V to 18 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4 V to 7.4 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)			0.581	
$D2_{12V}$	Duty Cycle 2(2)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7.4 V to 9.4 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)			0.67	
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 9.4 V to 18 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)	0.417			
$D3_{12V}$	Duty Cycle 3	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 4.6 V to 7.4 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)			0.59	
$D4_{12V}$	Duty Cycle 4(2)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 7.4 V to 9.4 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)			0.6	
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 7.4 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See 図 8-11, 図 8-12)			0.59	

(1) Duty cycles: LIN driver bus load conditions (C_{LIN}, R_{LIN}): Load1 = 1 nF, 1 kΩ; Load2 = 10 nF, 500 Ω, Load3 = 6.8 nF, 660 Ω. Duty cycles 3 and 4 are defined for 10.4-kbps operation. The TLIN1029 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification

(2) See errata TLIN1029-Q1 and TLIN2029-Q1 Duty Cycle Over VSUP

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7.8 Timing Requirements

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rx_pdr}, t_{rx_pdf}	Receiver rising and falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See 図 8-13 and 図 8-14)			6	µs
t_{rx_sym}	Symmetry of receiver propagation delay time	Rising edge with respect to falling edge, (trx_sym = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See 図 8-13 and 図 8-14)	–2		2	µs
t_{LINBUS}	LIN wakeup time (Minimum dominant time on LIN bus for wakeup)	See 図 8-17, 図 9-2, and 図 9-3	25	65	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See 図 9-3	8	25	50	µs
t_{DST}	Dominant state time out		20	45	80	ms
t_{MODE_CHANGE}	Mode change delay time	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin (See 図 8-15 and 図 9-4)	2		15	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid (See 図 8-15)			35	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

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7.9 Typical Characteristics

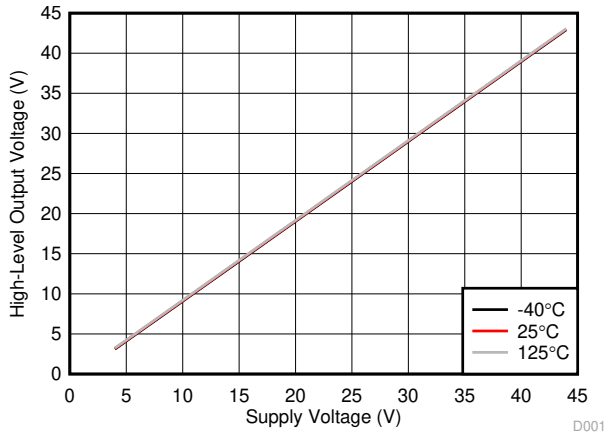


図 7-1. V_{OH} vs V_{SUP} and Temperature

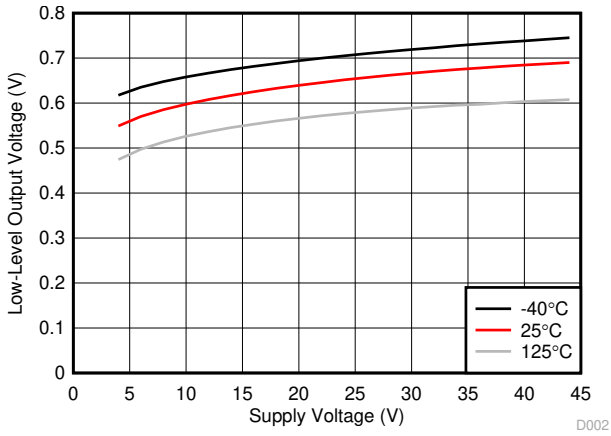


図 7-2. V_{OL} vs V_{SUP} and Temperature

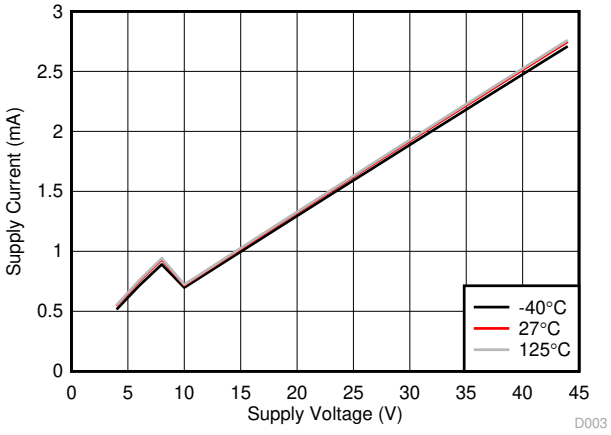


図 7-3. Dominant I_{SUP} vs V_{SUP} and Temperature

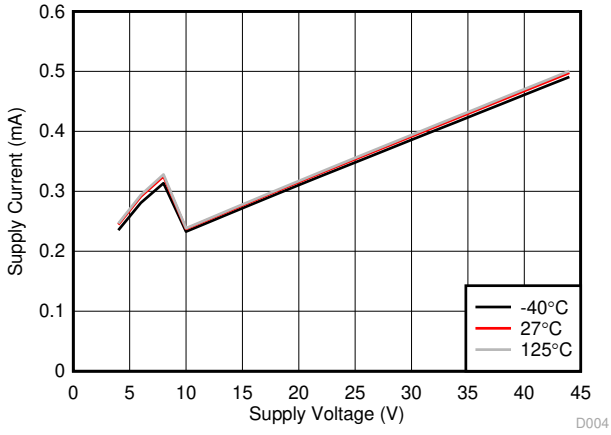


図 7-4. Recessive I_{SUP} vs V_{SUP} and Temperature

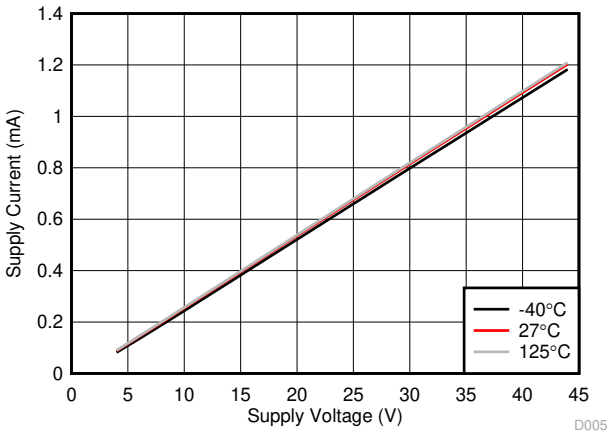


図 7-5. Standby Dominant I_{SUP} vs V_{SUP} and Temperature

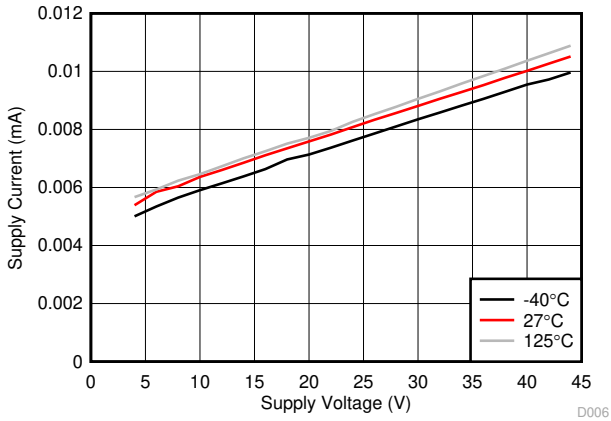


図 7-6. Standby Recessive I_{SUP} vs V_{SUP} and Temperature

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7.9 Typical Characteristics (continued)

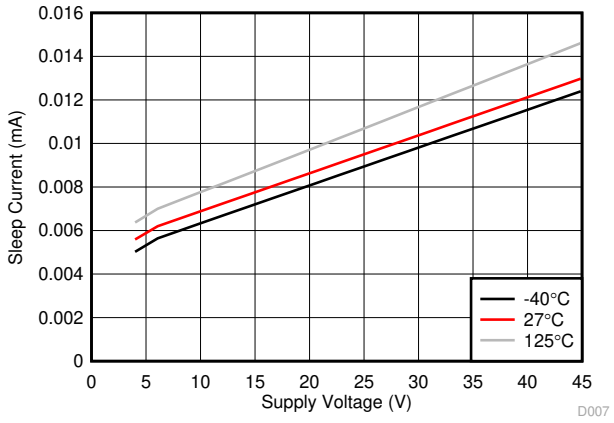


図 7-7. Sleep Current vs V_{SUP} and Temperature

8 Parameter Measurement Information

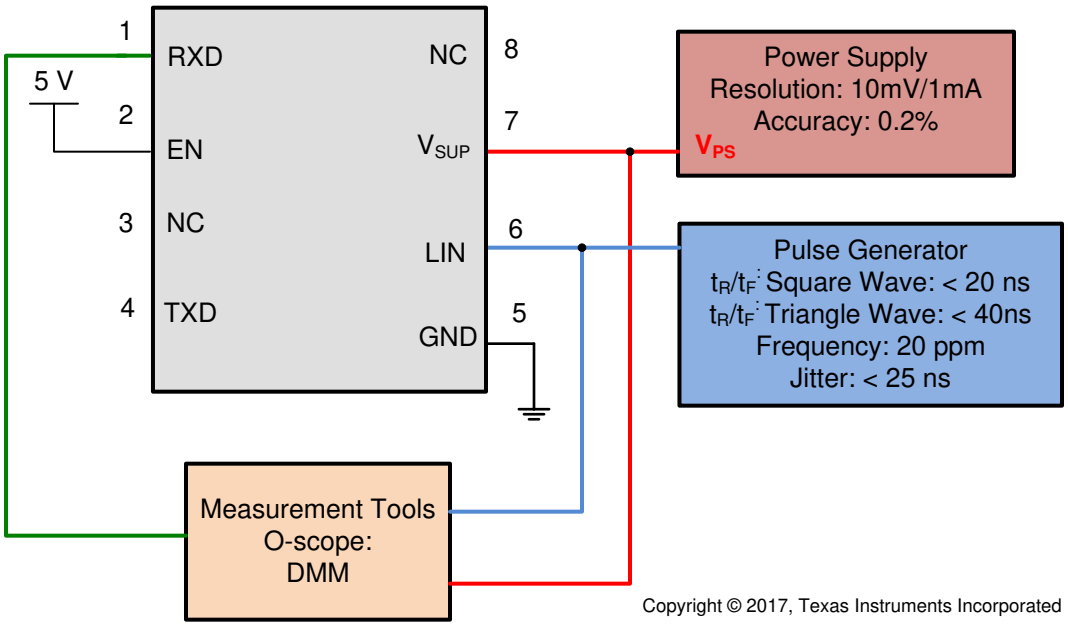


図 8-1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

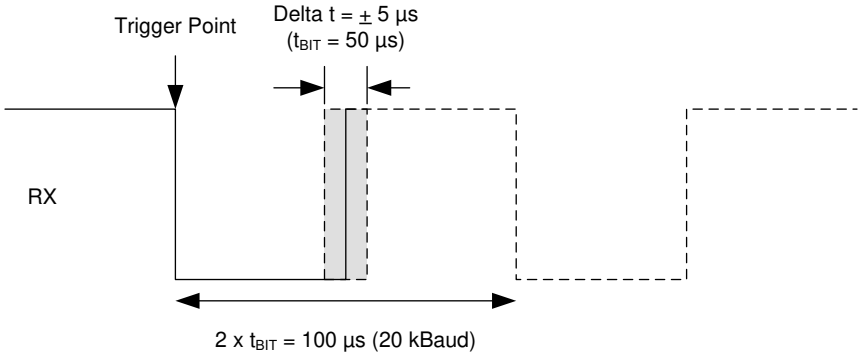


図 8-2. RX Response: Operating Voltage Range

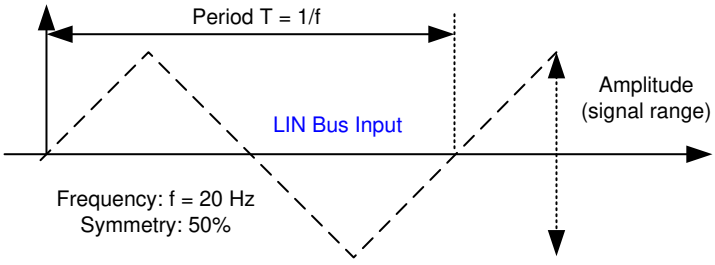


図 8-3. LIN Bus Input Signal

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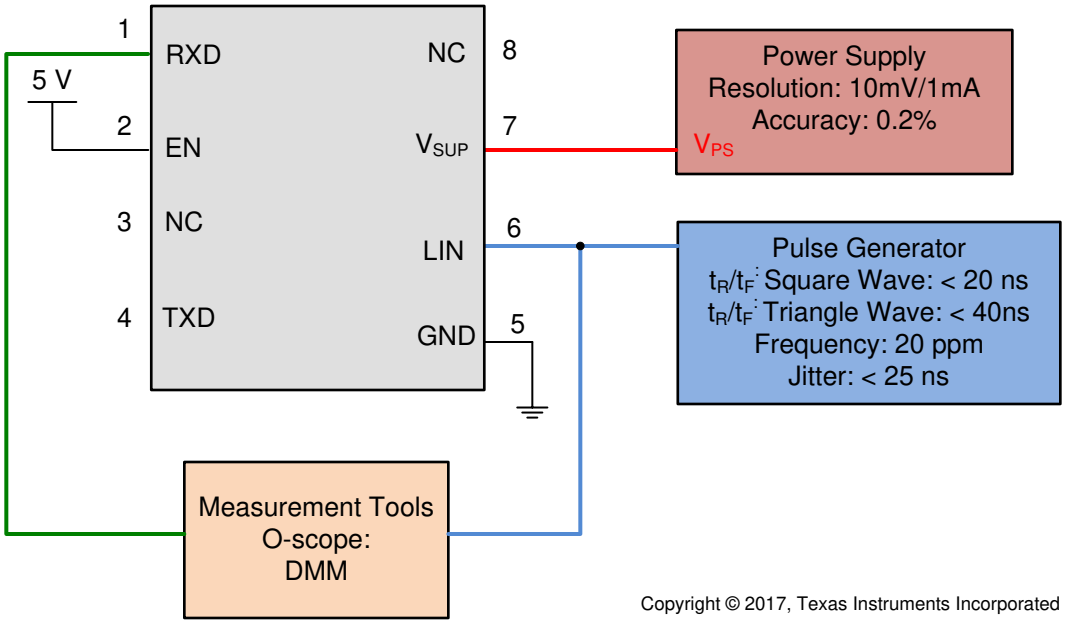


図 8-4. LIN Receiver Test with RX access Param 17, 18, 19, 20

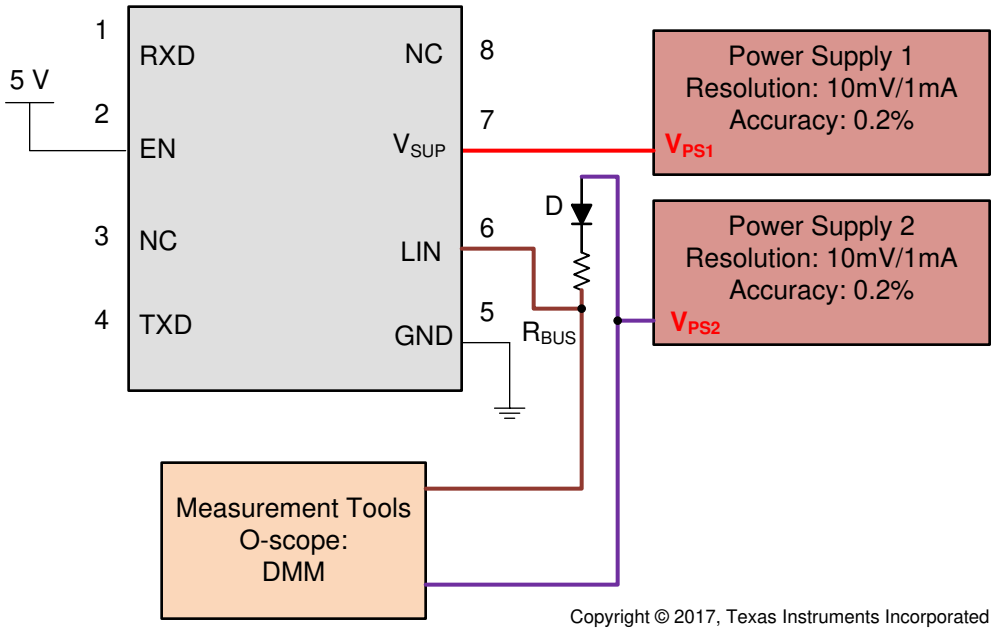
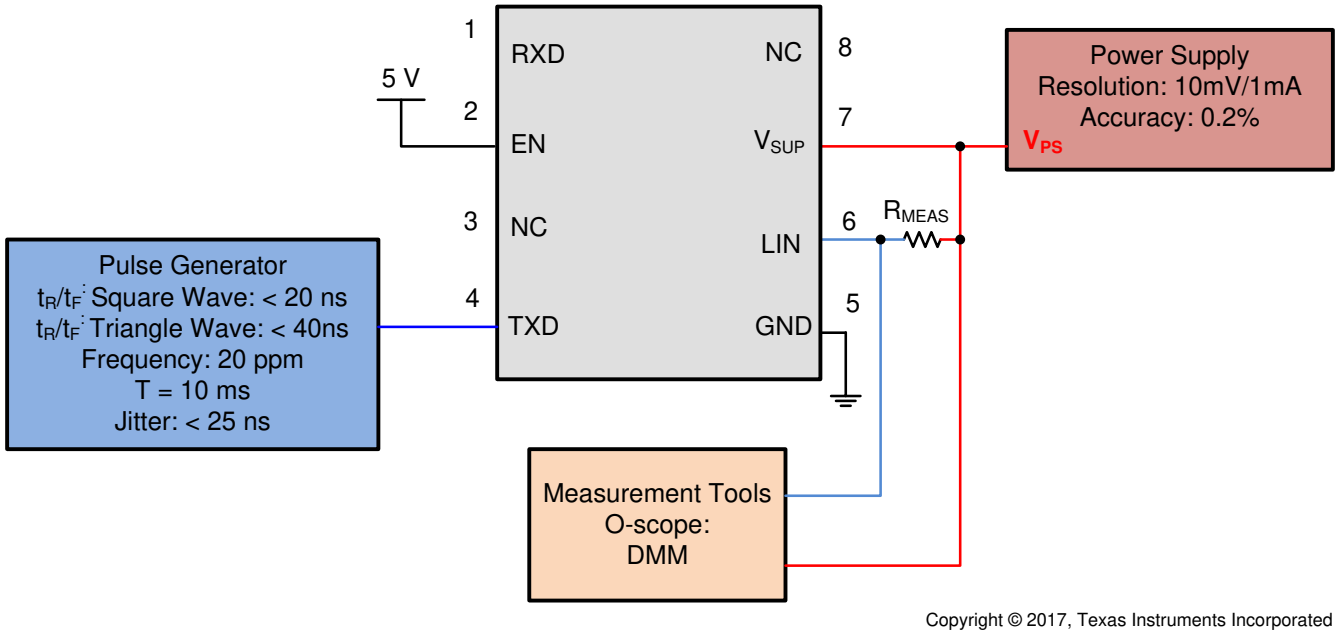
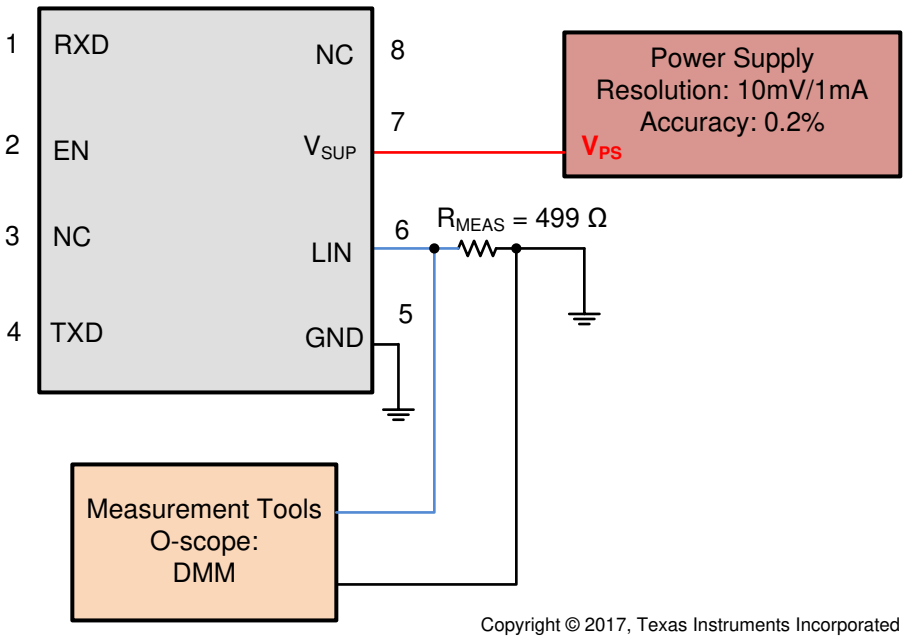


図 8-5. $V_{SUP_NON_OP}$ Param 11



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図 8-6. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on) Param 12



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図 8-7. Test Circuit for $I_{BUS_PAS_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13

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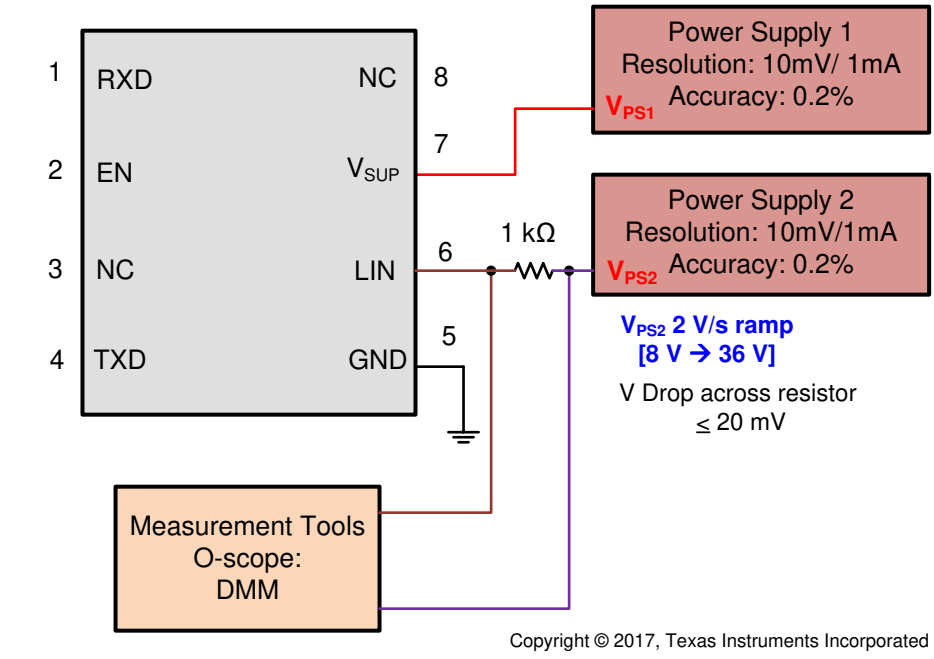


図 8-8. Test Circuit for $I_{BUS_PAS_rec}$ Param 14

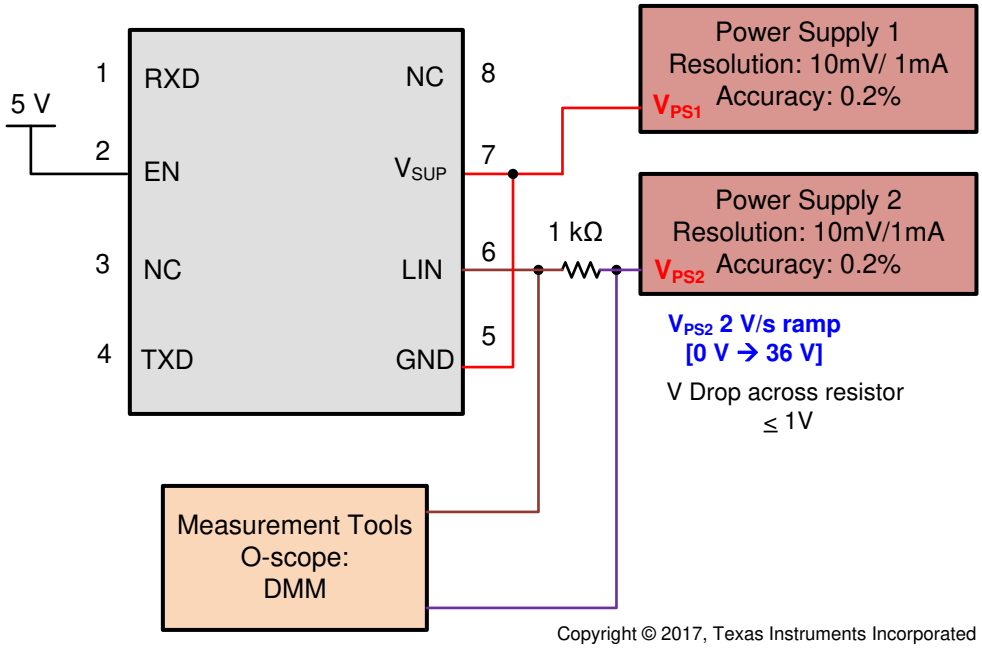


図 8-9. Test Circuit for $I_{BUS_NO_GND}$ Loss of GND

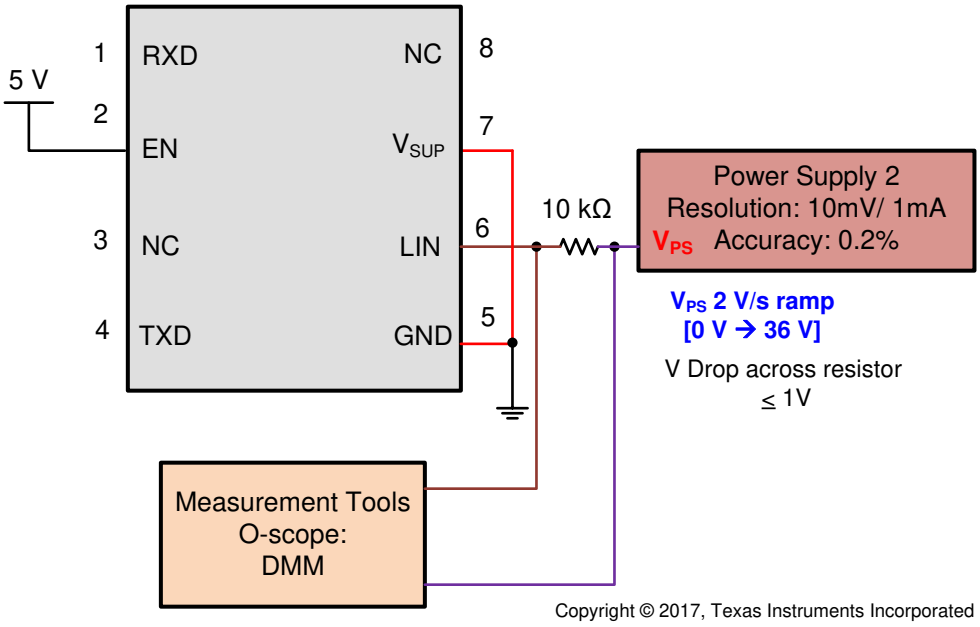


図 8-10. Test Circuit for $I_{BUS_NO_BAT}$ Loss of Battery

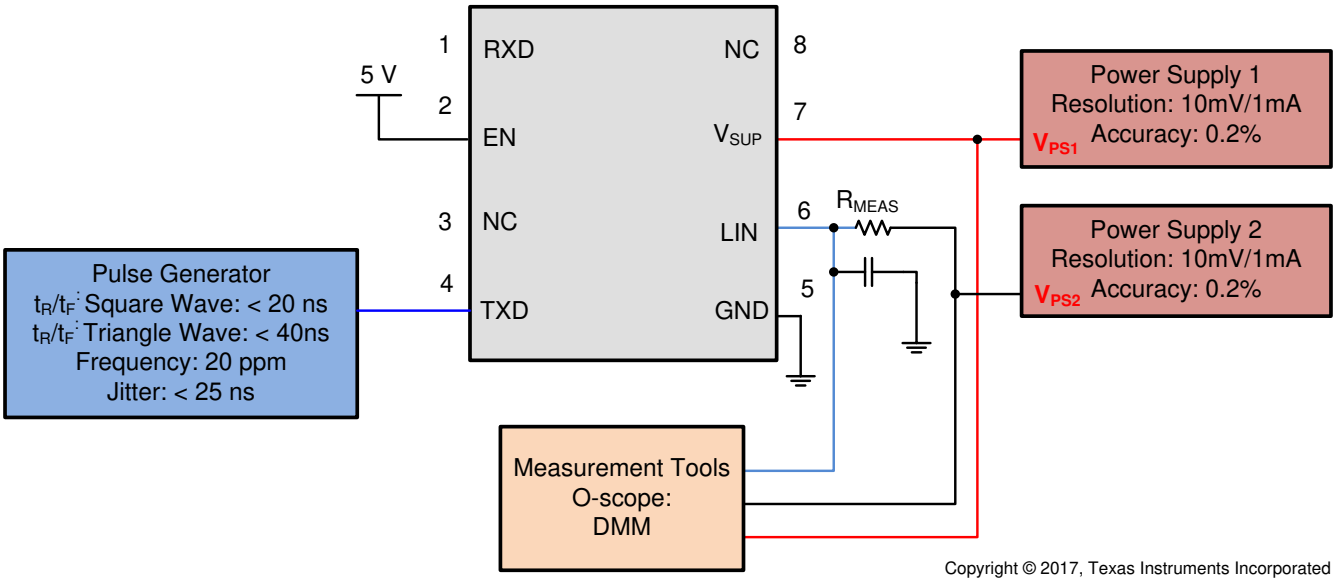


図 8-11. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

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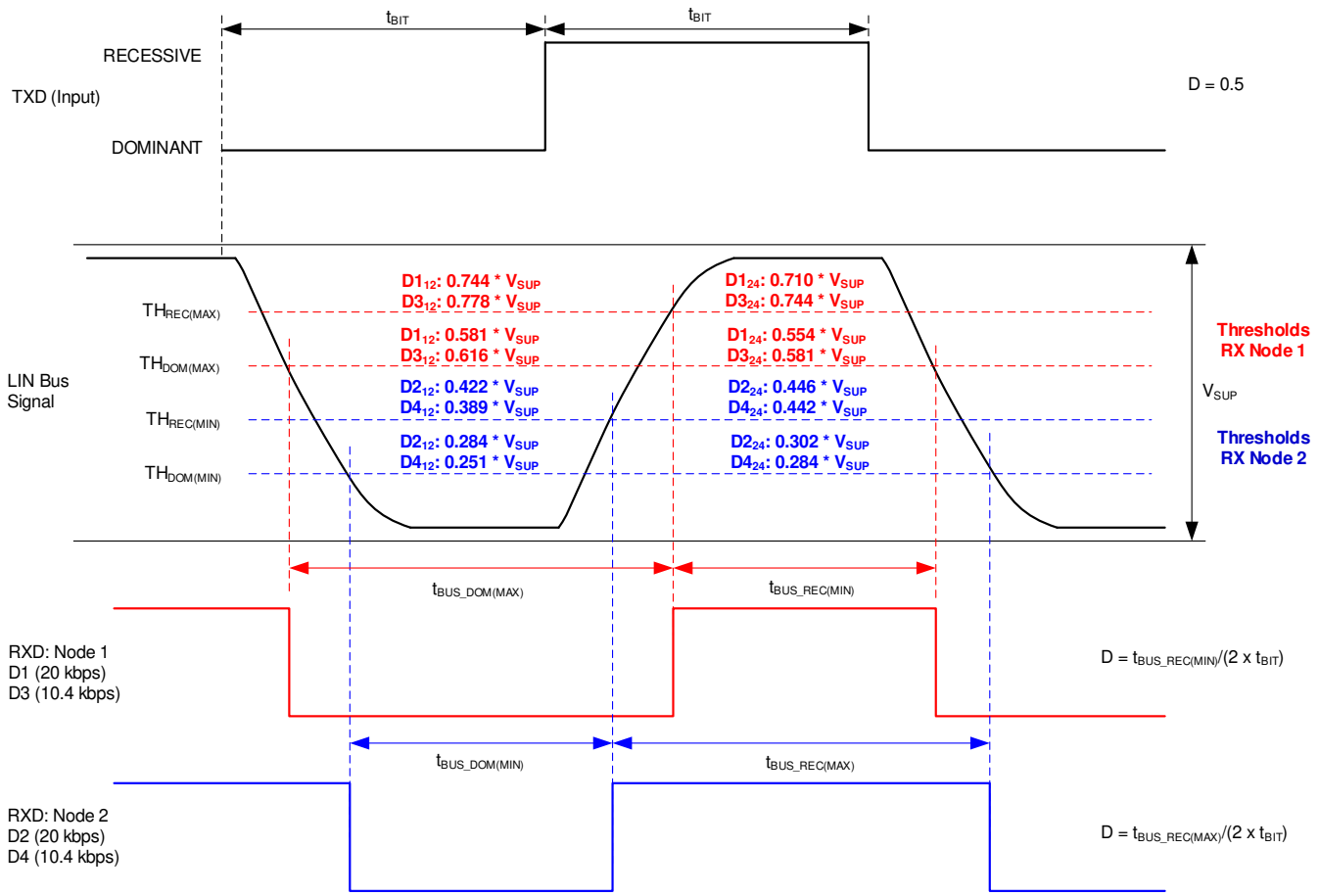


図 8-12. Definition of Bus Timing Parameters

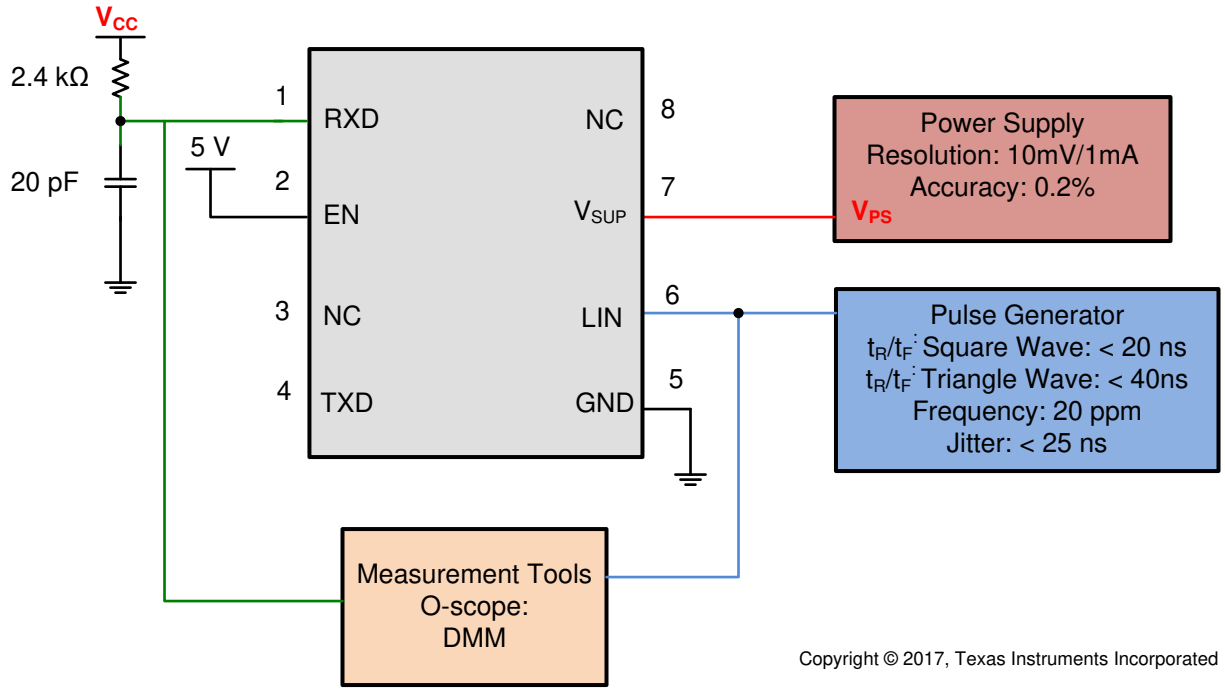
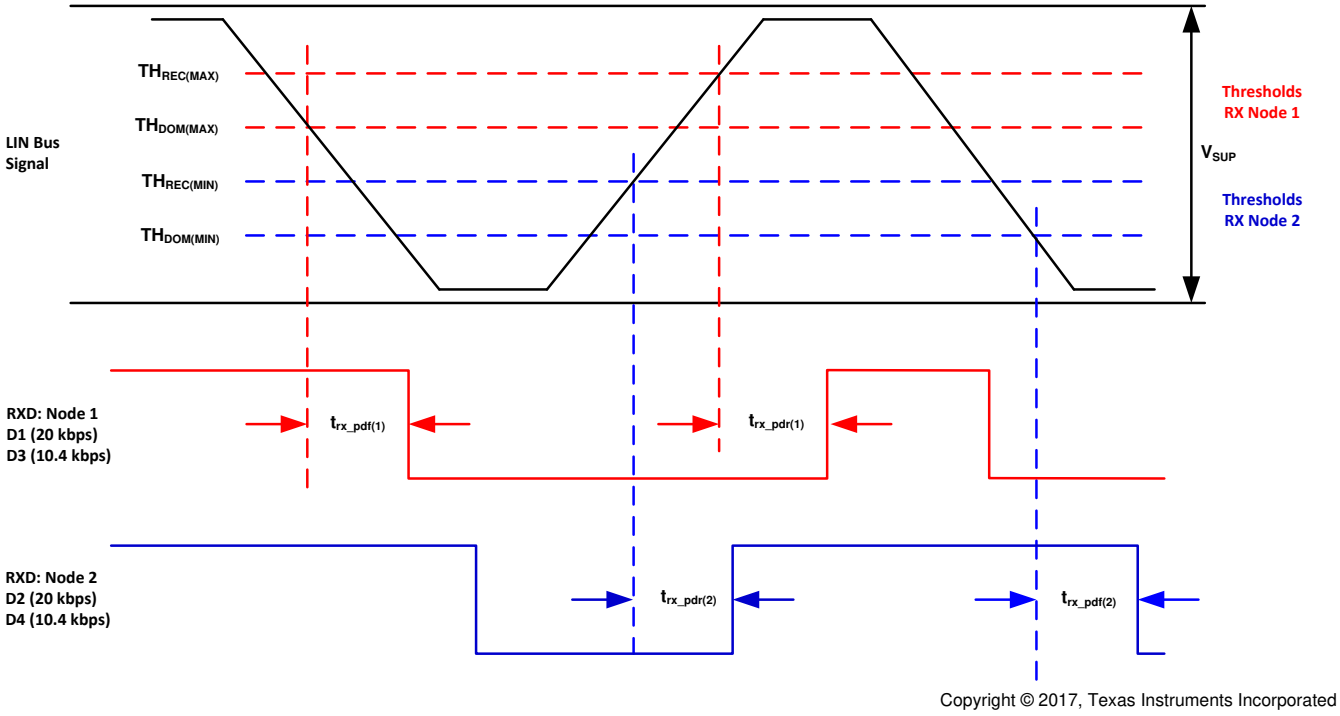


図 8-13. Propagation Delay Test Circuit; Param 31, 32



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図 8-14. Propagation Delay

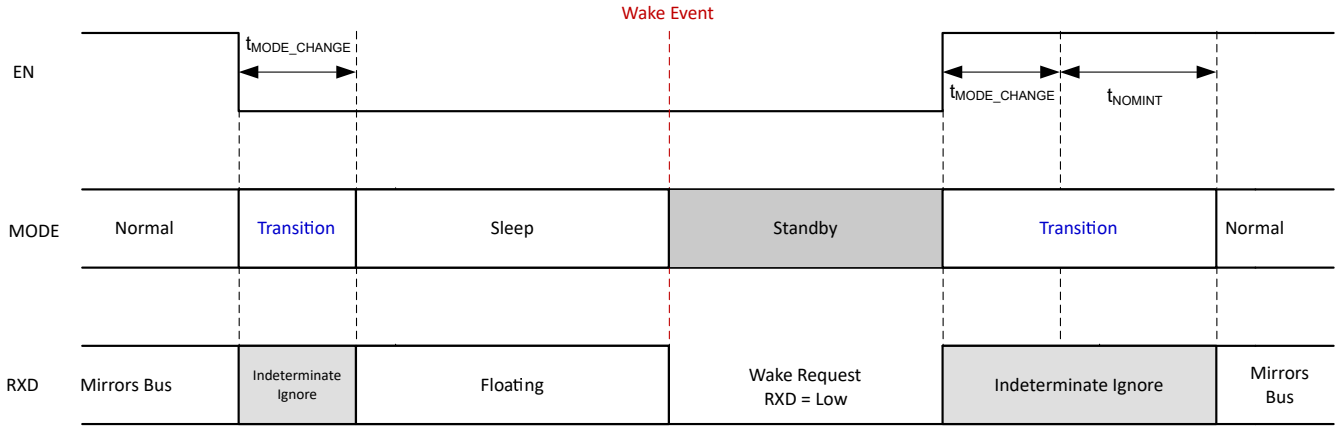


図 8-15. Mode Transitions

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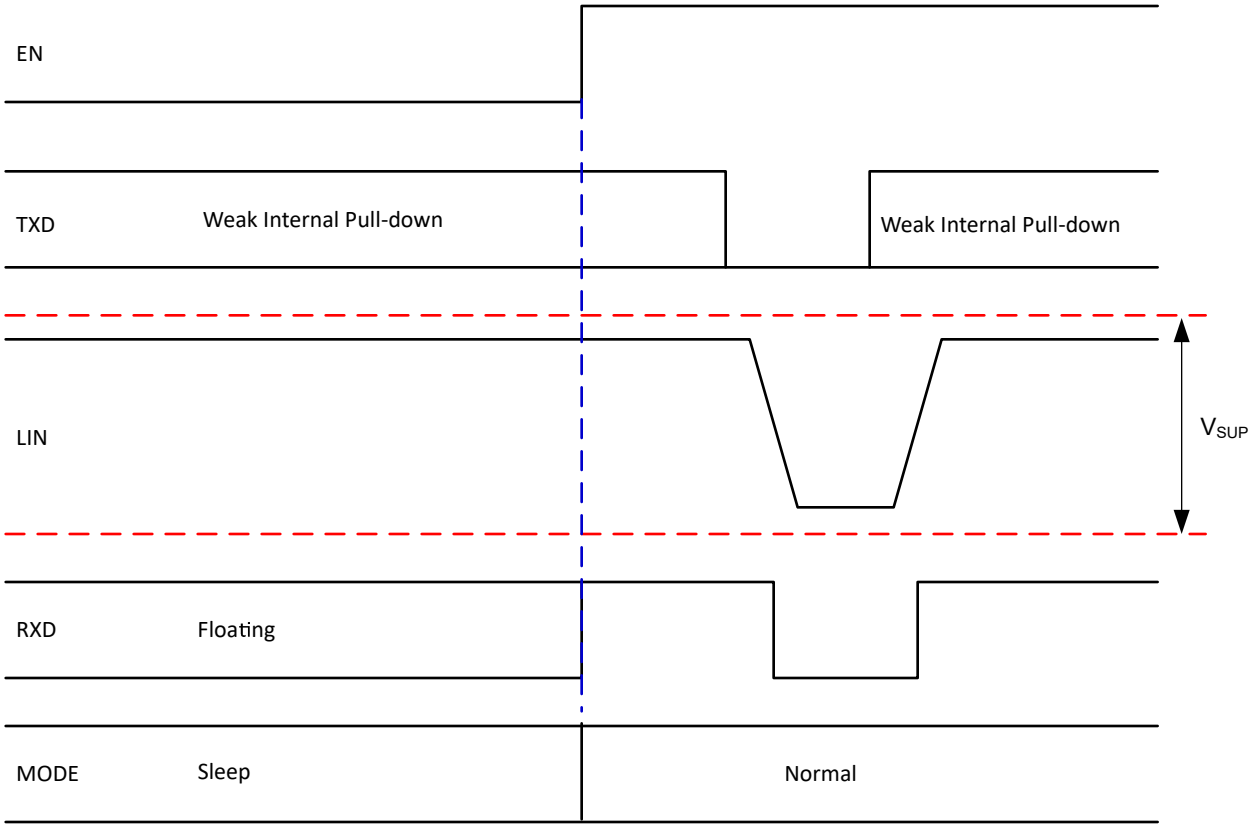


図 8-16. Wake-up Through EN

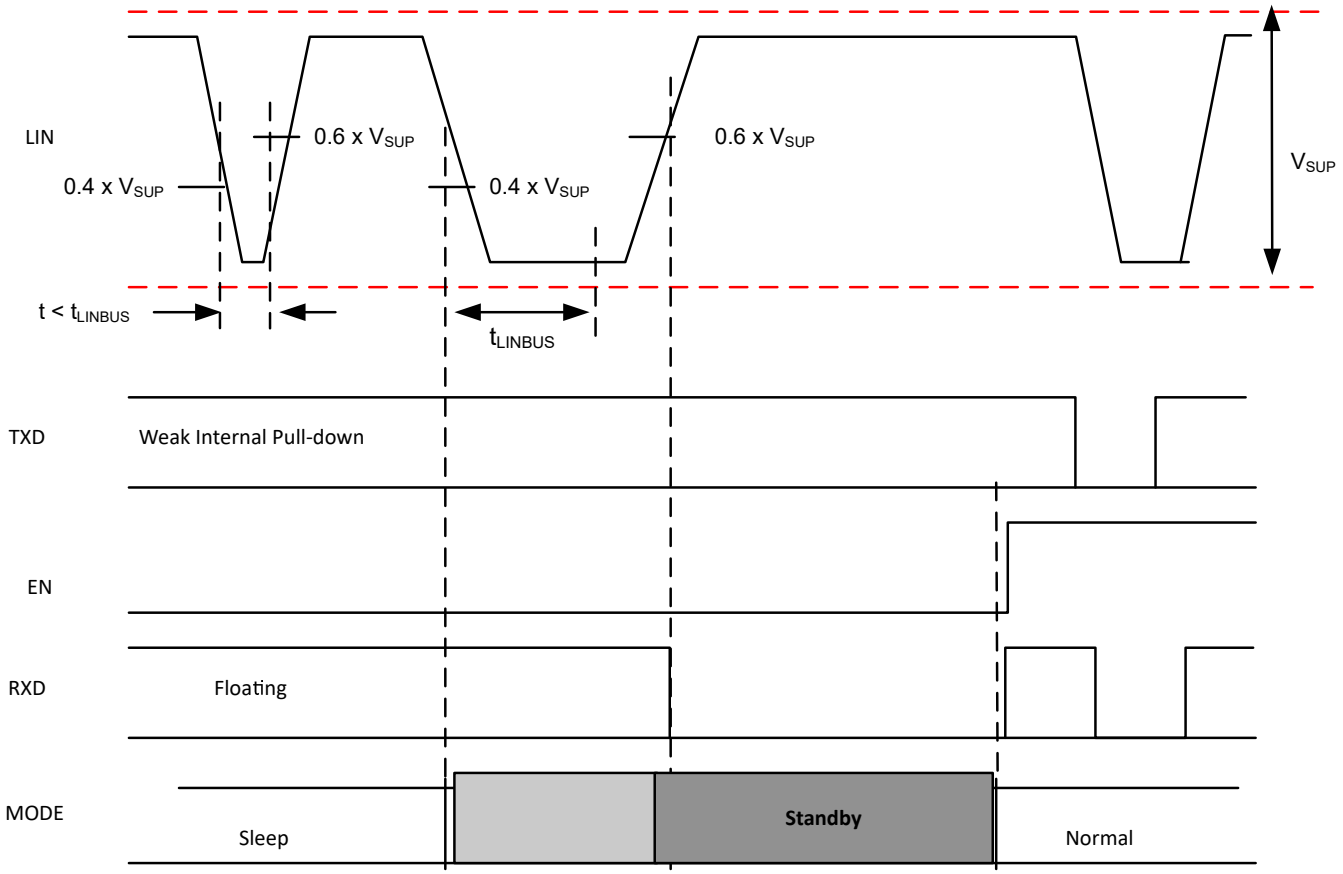
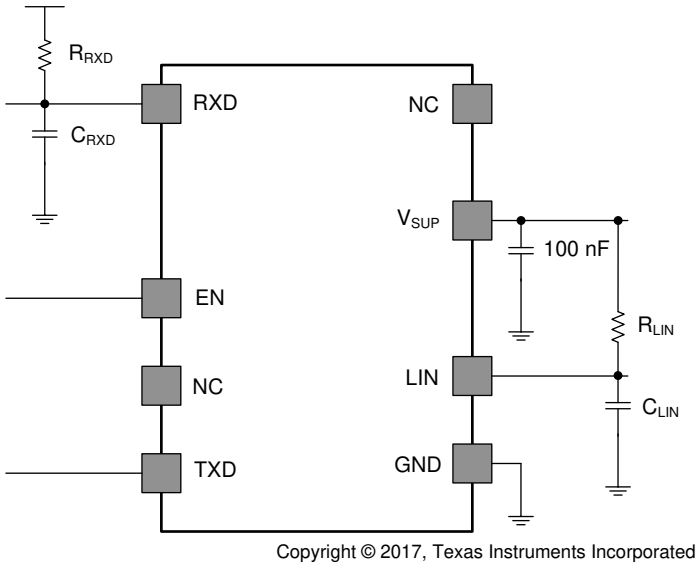


図 8-17. Wake-up through LIN



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図 8-18. Test Circuit for AC Characteristics

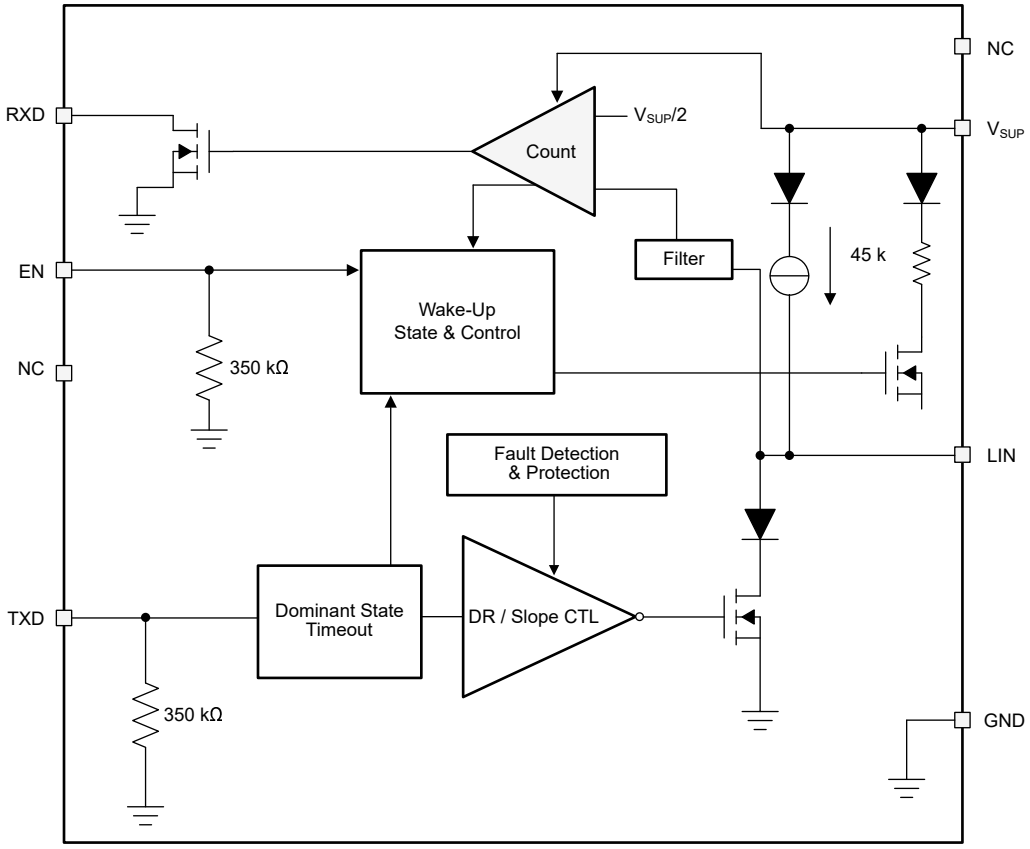
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9 Detailed Description

9.1 Overview

The TLIN1029-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, compatible with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 standards, with integrated wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low speed in-vehicle networks using data rates from 2.4 kbps to 20 kbps. The TLIN1029-Q1 LIN receiver works up to 100 kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN1029-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for responder mode applications. Commander mode applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification. The TLIN1029-Q1 provides many protection features such as immunity to ESD and high bus standoff voltage. The device also provides two methods to wake up: EN pin and from the LIN bus.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 45 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shut-down condition, the

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transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder mode applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a commander mode node application.

9.3.1.2 LIN Receiver Characteristics

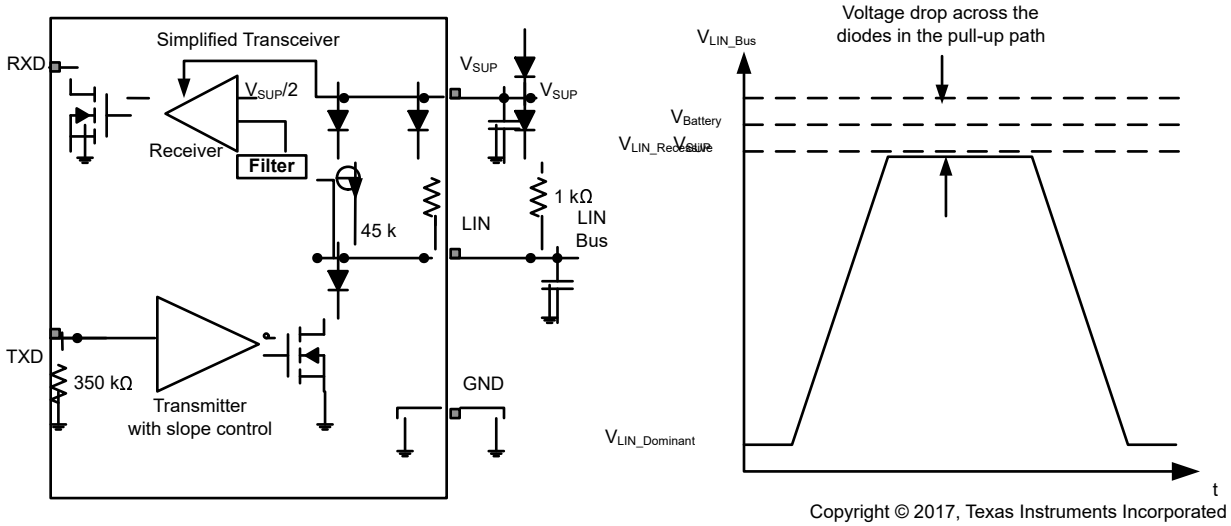
The receiver's characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1029-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder mode applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for com mode applications as per the LIN specification.

図 9-1 shows a commander node configuration and how the voltage levels are defined



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図 9-1. Commander Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the MCU's LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near $V_{Battery}$). See 図 9-1. The TXD input structure is compatible with microcontrollers with 3.3 V and 5 V I/O. TXD has an internal pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer.

9.3.3 RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake-up request from the LIN bus.

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9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (図 9-1). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage, as well as ensuring the input and output voltages are within their appropriate thresholds. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake-up. EN has an internal pull-down resistor to ensure the device remains in low-power mode even if EN floats.

9.3.7 Protection Features

The TLIN1029-Q1 has several protection features, described below.

9.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

9.3.9 Bus Stuck Dominant System Fault: False Wake-Up Lockout

The TLIN1029-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current consumption. 図 9-2 and 図 9-3 show the behavior of this protection.

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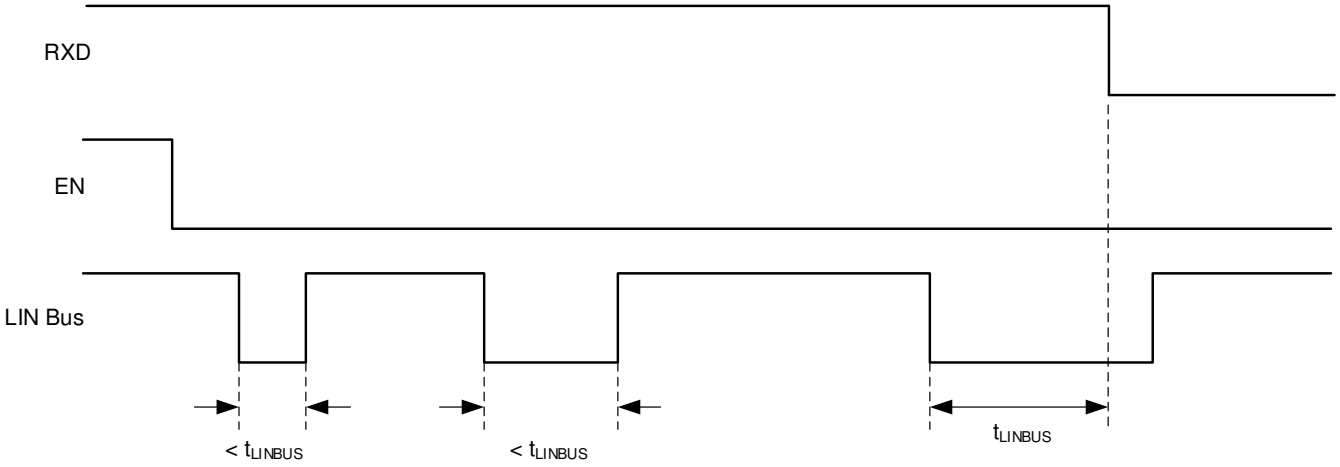


図 9-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake-Up

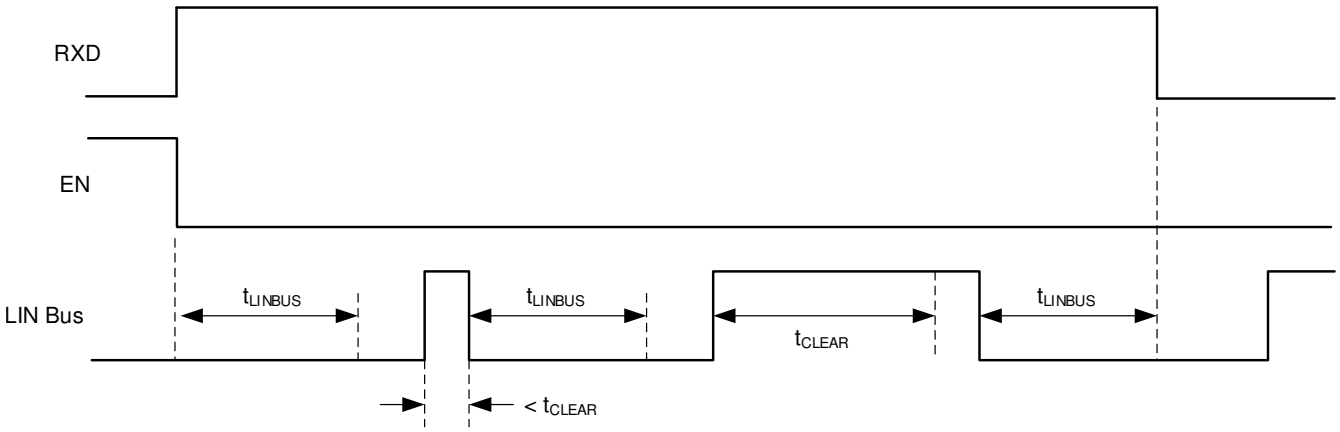


図 9-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake-Up

9.3.10 Thermal Shutdown

The LIN transmitter is protected by current limiting circuitry; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over-temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

9.3.11 Under Voltage on V_{SUP}

The TLIN1029-Q1 contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.12 Unpowered Device and LIN Bus

In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The TLIN1029-Q1 has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

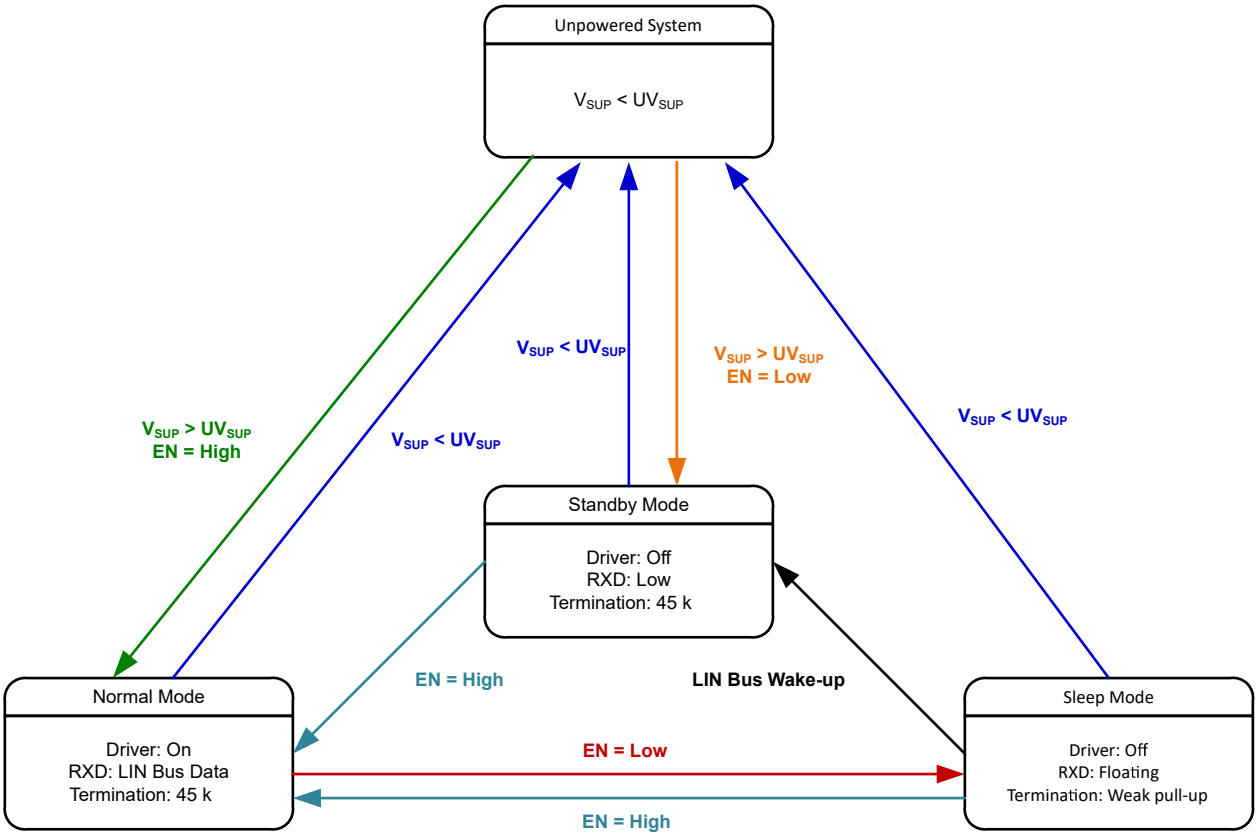
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9.4 Device Functional Modes

The TLIN1029-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. 図 9-4 graphically shows the relationship while 表 9-1 shows the state of pins.

表 9-1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak current pull-up	Off	
Standby	Low	Low	45 kΩ (typical)	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	45 kΩ (typical)	On	LIN transmission up to 20 kbps



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図 9-4. Operating State Diagram

9.4.1 Normal Mode

If the EN pin is high at power up the device will power up in normal mode. If the EN pin is low, it will power up in standby mode. The EN pin controls the mode of the device. In normal operational mode the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN1029-Q1 is in sleep or standby mode for > t_{MODE_CHANGE} plus t_{NOMINT}.

9.4.2 Sleep Mode

Sleep mode is the power saving mode for the TLIN1029-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with extremely low current consumption in this mode, the TLIN1029-Q1 can still wake up from LIN bus through a wake-up signal or if EN is set high for ≥ t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake-up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake-up receiver are active.

9.4.3 Standby Mode

This mode is entered whenever a wake-up event occurs through LIN bus while the device is in sleep mode. The LIN bus responder mode termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See *セクション 10.2.2.2* for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode, the device returns to normal mode. The normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

9.4.4 Wake-Up Events

There are two ways to wake up from sleep mode:

- Remote wake-up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake-up event, eliminating false wake-ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake-up through EN being set high for longer than t_{MODE_CHANGE}.

9.4.4.1 Wake-Up Request (RXD)

When the TLIN1029-Q1 encounters a wake-up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin is releases the wake-up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.4.2 Mode Transitions

When the TLIN1029-Q1 is transitioning from normal to sleep or standby modes the device needs the time t_{MODE_CHANGE} to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs t_{MODE_CHANGE} plus t_{NOMINT}.

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10 Application and Implementation

Note

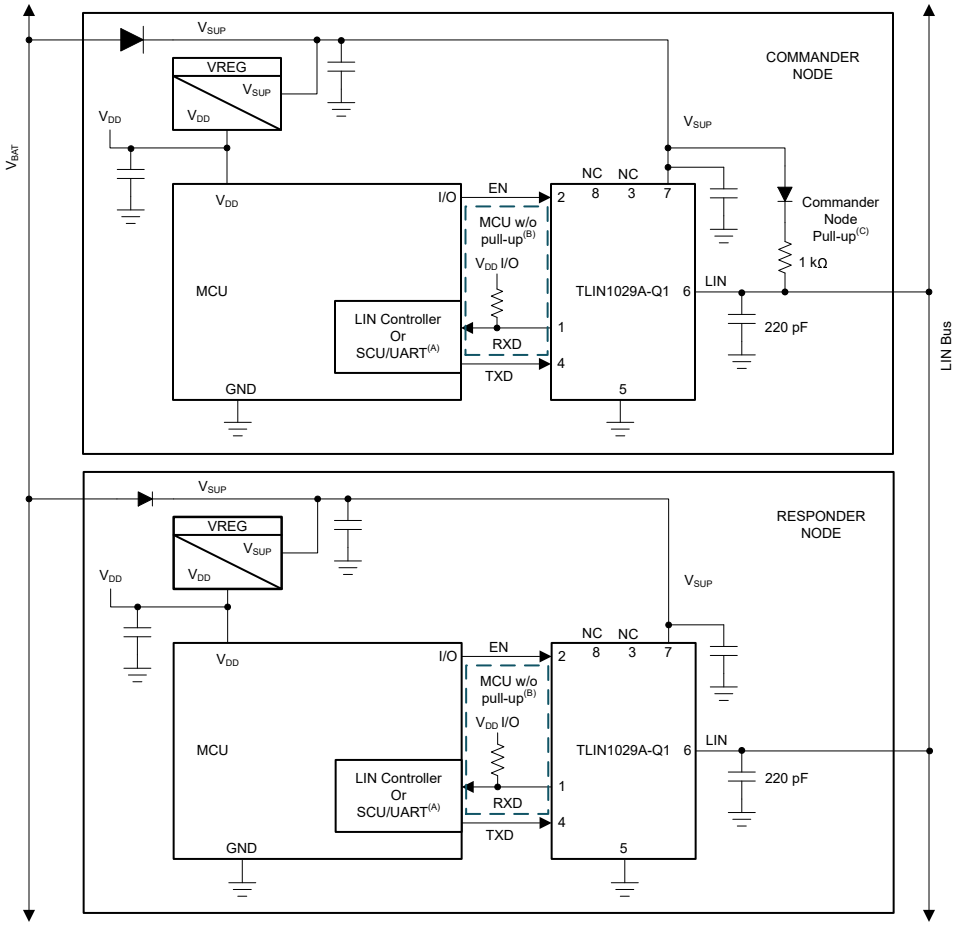
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLIN1029-Q1 can be used as both a responder node device and a commander node device in a LIN network. The device comes with the ability to support both remote wake-up request and local wake-up request.

10.2 Typical Application

The device integrates a 45 kΩ pull-up resistor and series diode for responder node applications. For commander applications an external 1 kΩ pull-up resistor with series blocking diode can be used. 図 10-1 shows the device being used in both commander mode and responder mode applications.



A. If RXD on MCU on LIN responder node has internal pull-up, no external pull-up resistor is needed.
B. If RXD on MCU on LIN responder node does not have an internal pull-up, requires external pull-up resistor.
C. Commander node applications require and external 1 kΩ pull-up resistor and serial diode.
D. Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥ 10 µF.

図 10-1. Typical LIN Bus

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN1029-Q1 to be used with 3.3- V and 5-V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The select external pull-up resistor value should be between 1 kΩ to 10 kΩ, depending on supply used (See I_{OL} in electrical characteristics). The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN1029-Q1 in systems which are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE}. This is shown in 図 8-15

10.2.2.2 Standby Mode Application Note

If the TLIN1029-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low and would signal to the software that the TLIN1029-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

10.2.2.2.1 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for a commander node and responder node applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.3 Application Curves

The below figures show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant stated under lightly loaded conditions.

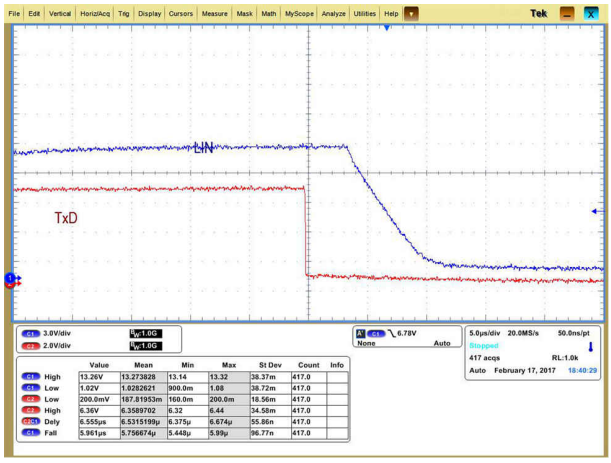


図 10-2. Recessive to Dominant Propagation

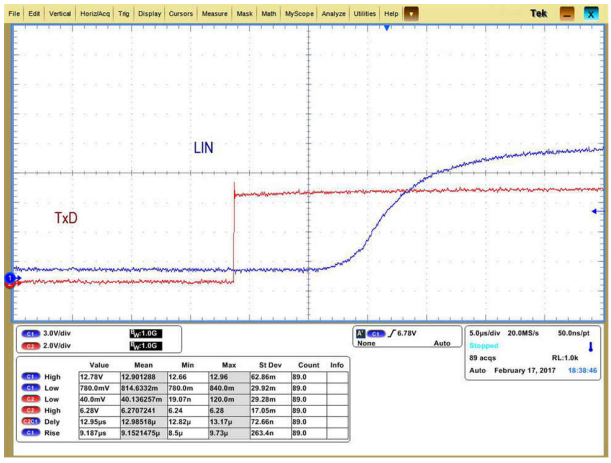


図 10-3. Dominant to Recessive Propagation

11 Power Supply Recommendations

The TLIN1029-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4 V to 36 V. A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible. It is good practice for some applications with noisier supplies to include 1 µF and 10 µF decoupling capacitor, as well.

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12 Layout

In order for your PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1 (RXD):** The pin is an open-drain output and requires an external pull-up resistor in the range of 1 kΩ to 10 kΩ to function properly. Note that the minimum value will depend on the VIO supply used. See I_{OL} in electrical specifications. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low-power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (NC):** Not Connected.
- **Pin 4 (TXD):** The TXD pin is used to transmit the input signal from the microcontroller. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For responder mode applications, a 220 pF capacitor to ground is implemented. For commander mode applications, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See 図 10-1.
- **Pin 7 (VSUP):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 8 (NC):** Not Connected.

Note

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

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12.2 Layout Example

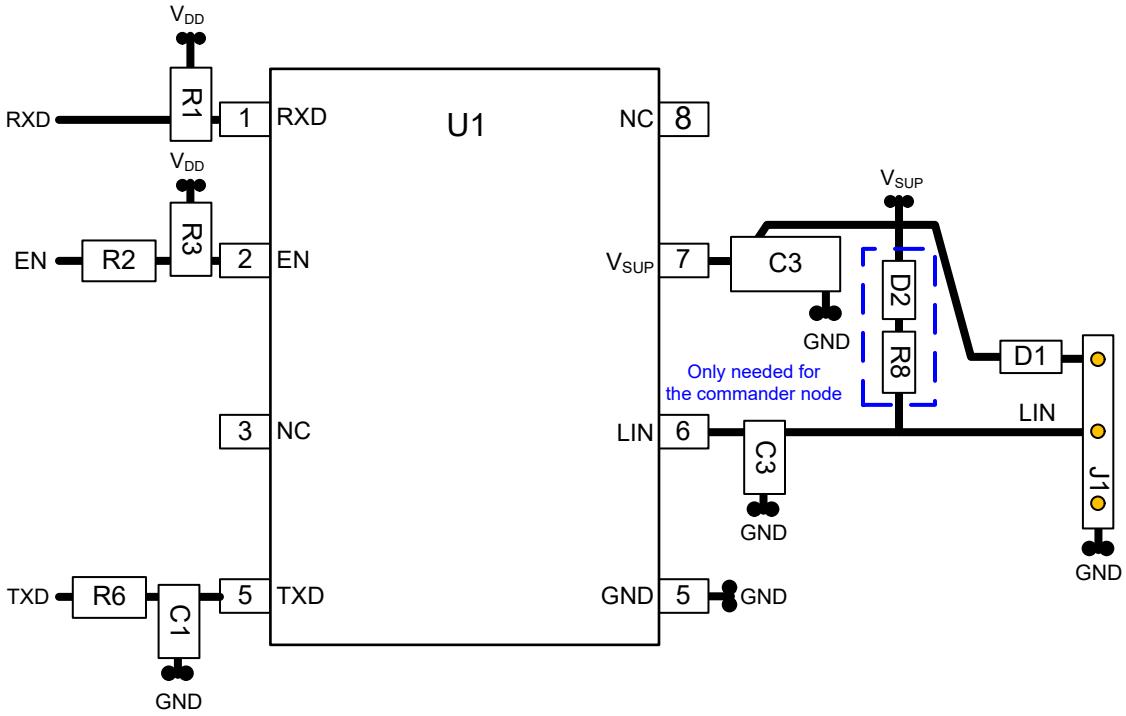


図 12-1. Layout Example

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

TLIN1029-Q1 and TLIN2029-Q1 Duty Cycle Over V_{SUP}

For related documentation see the following:

- LIN Standards:
  - ISO/DIS 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
  - ISO/DIS 17987-4: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
  - SAEJ2602-1: LIN Network for Vehicle Applications
  - LIN Specifications LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A
- EMC requirements:
  - SAEJ2962-1: Communication Transceivers Qualification Requirements - LIN
  - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
  - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
  - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
  - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
  - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
  - IEC 61000-4-2
  - IEC 61967-4
  - CISPR25
- Conformance Test requirements:
  - ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
  - SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test
-

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN1029DQ1	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TL029
TLIN1029DQ1.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL029
TLIN1029DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TL029
TLIN1029DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029
TLIN1029DRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TL029
TLIN1029DRBTQ1.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029
TLIN1029DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TL029
TLIN1029DRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL029
TLIN1029MDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TL029
TLIN1029MDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

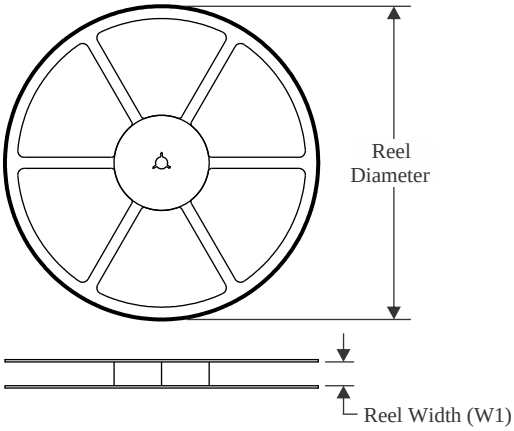
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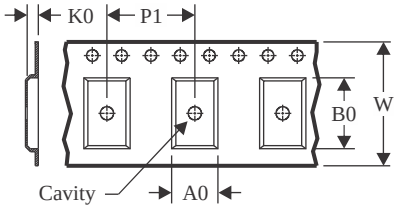
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

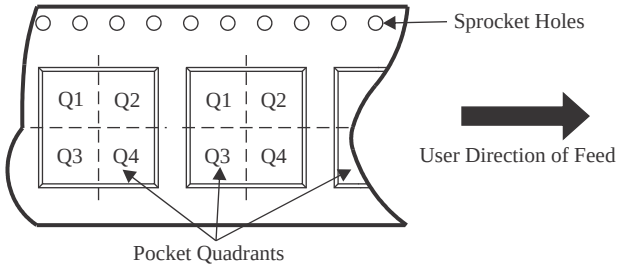


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

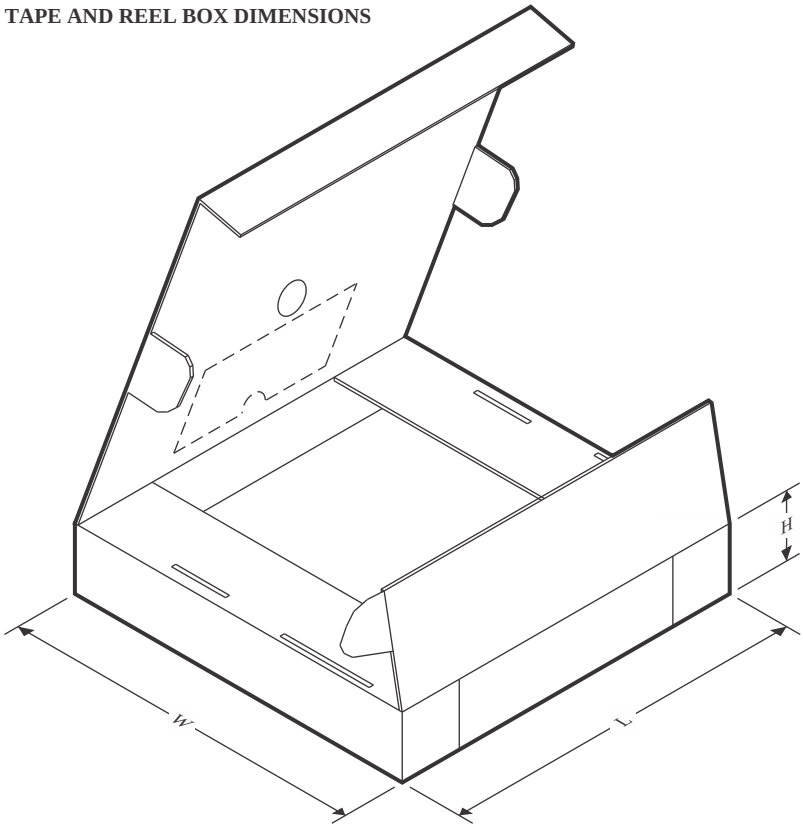
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN1029DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLIN1029DRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLIN1029DRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TLIN1029MDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
TLIN1029MDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1

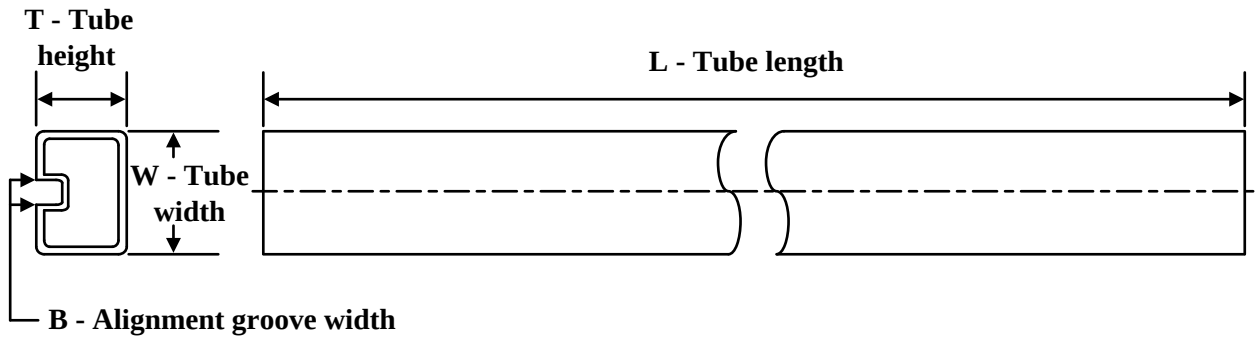
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN1029DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN1029DRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TLIN1029DRBTQ1	SON	DRB	8	250	213.0	191.0	35.0
TLIN1029MDRBRQ1	SON	DRB	8	3000	367.0	367.0	38.0
TLIN1029MDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLIN1029DQ1	D	SOIC	8	75	507	8	3940	4.32
TLIN1029DQ1	D	SOIC	8	75	507	8	3940	4.32
TLIN1029DQ1	D	SOIC	8	75	517	7.87	635	4.25
TLIN1029DQ1.A	D	SOIC	8	75	507	8	3940	4.32
TLIN1029DQ1.A	D	SOIC	8	75	517	7.87	635	4.25
TLIN1029DQ1.A	D	SOIC	8	75	507	8	3940	4.32

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

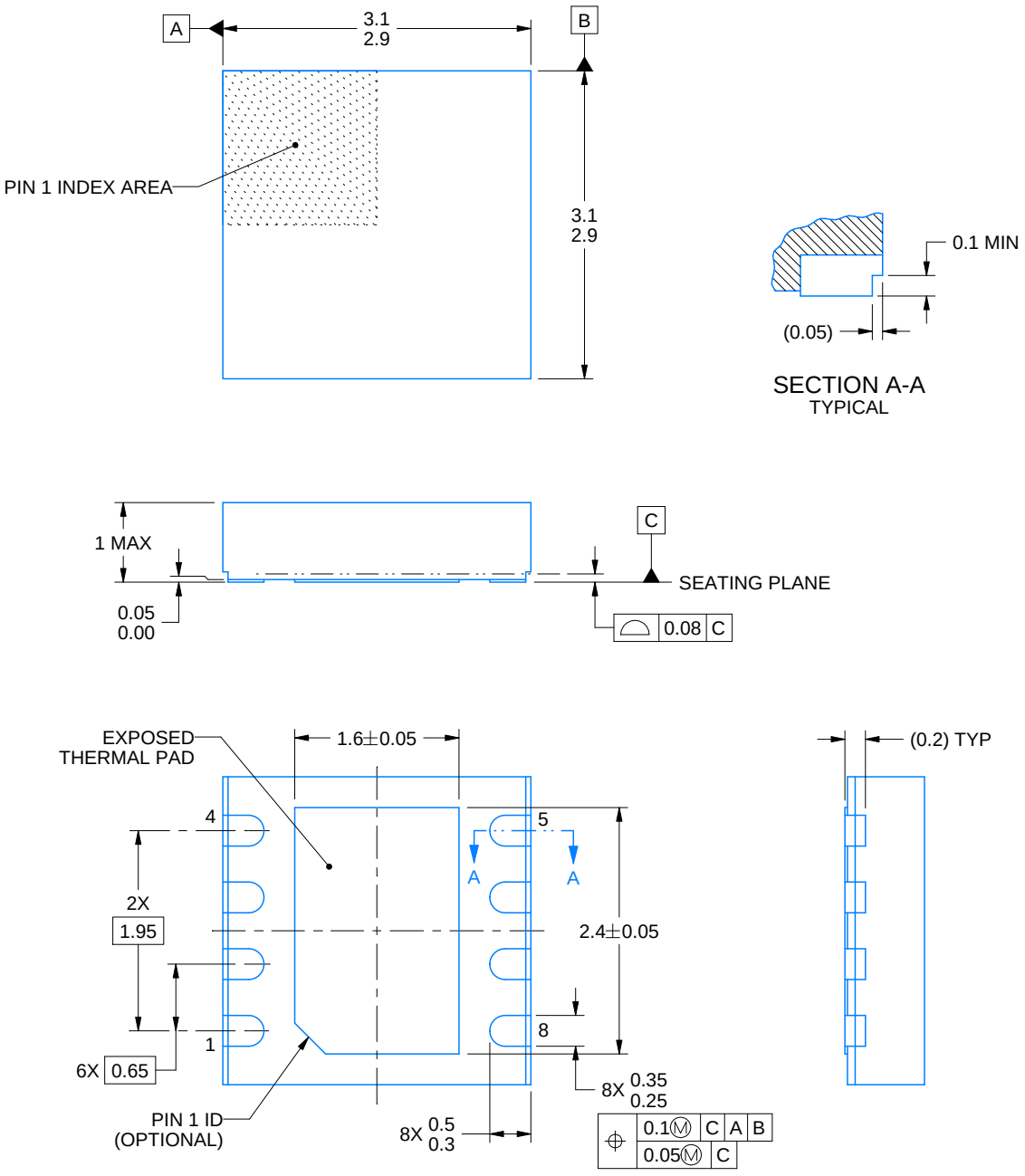
4203482/L

DRB0008F

PACKAGE OUTLINE

VSON - 1 mm max height

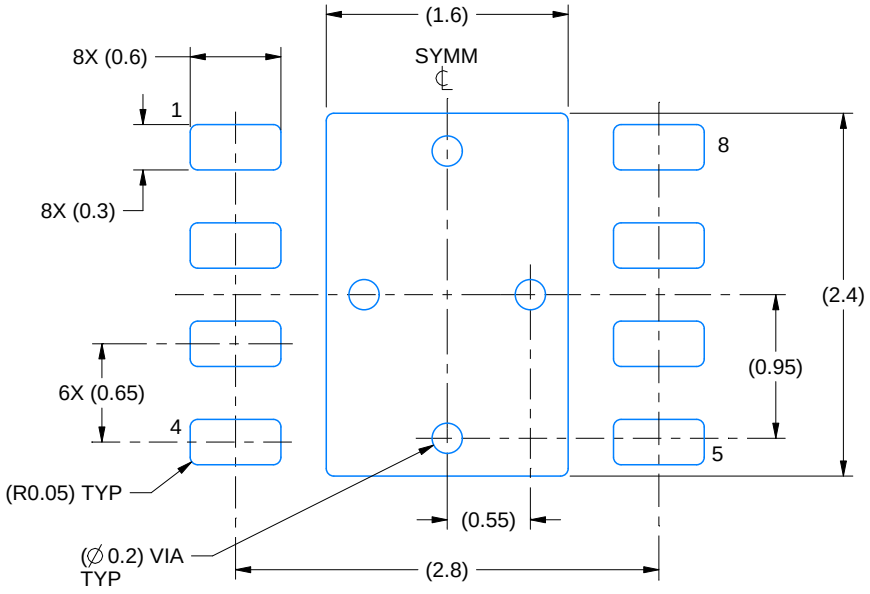
PLASTIC SMALL OUTLINE - NO LEAD



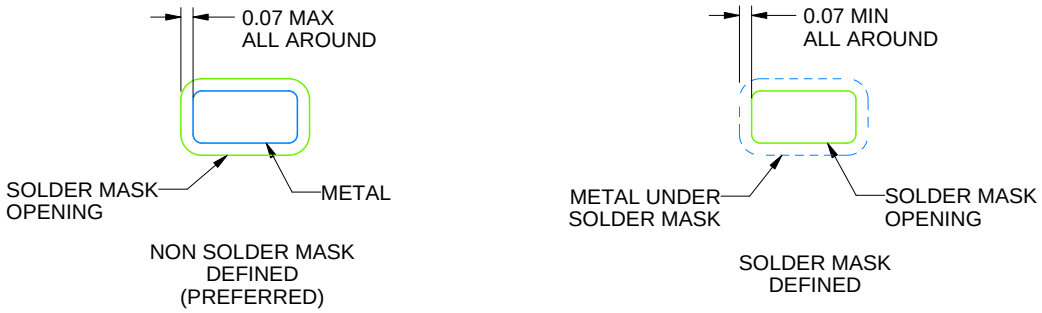
4222121/C 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

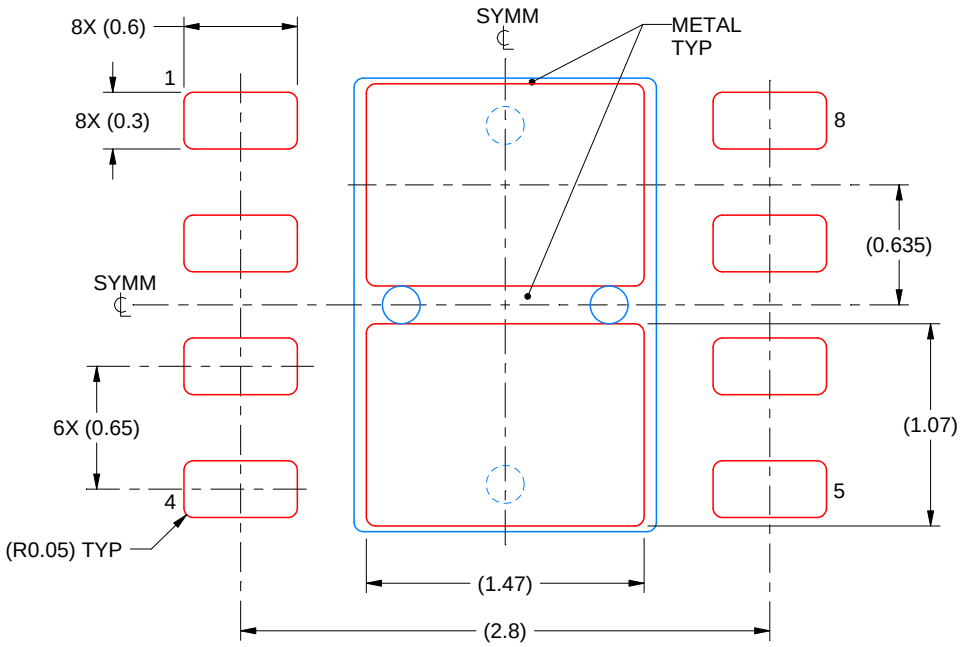


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

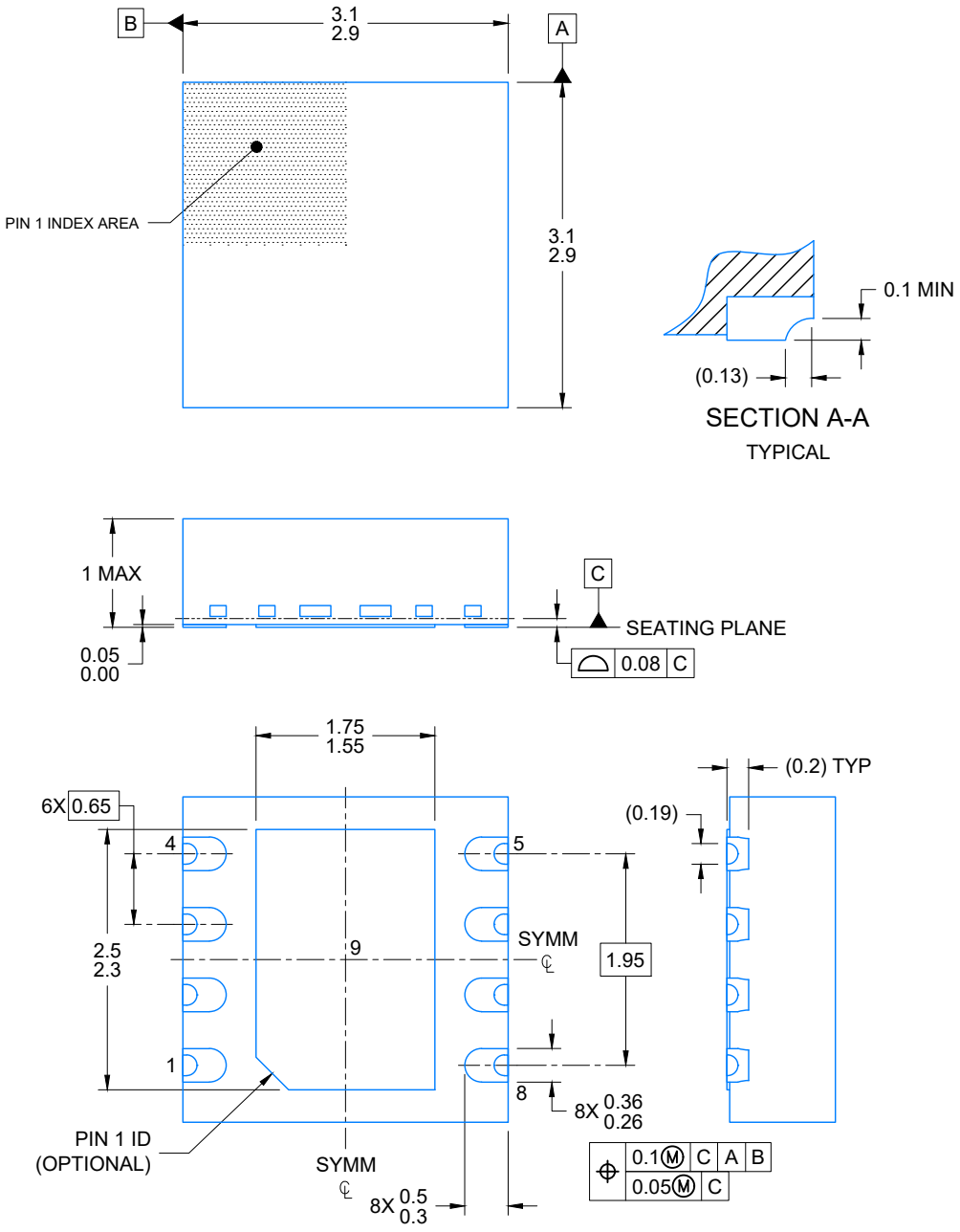
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRB0008J

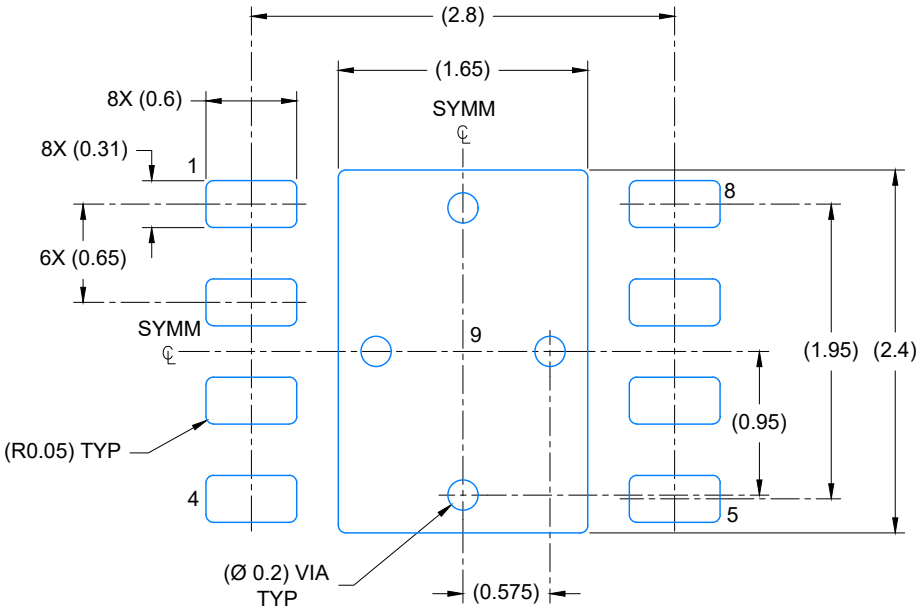
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

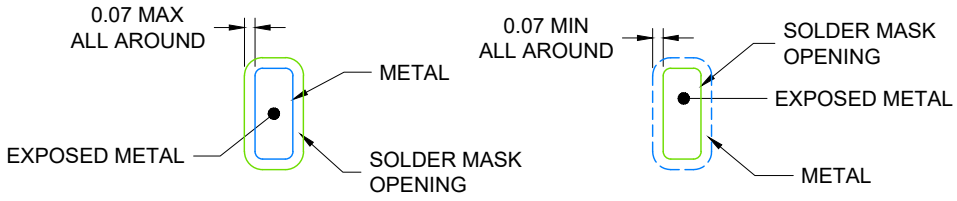


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

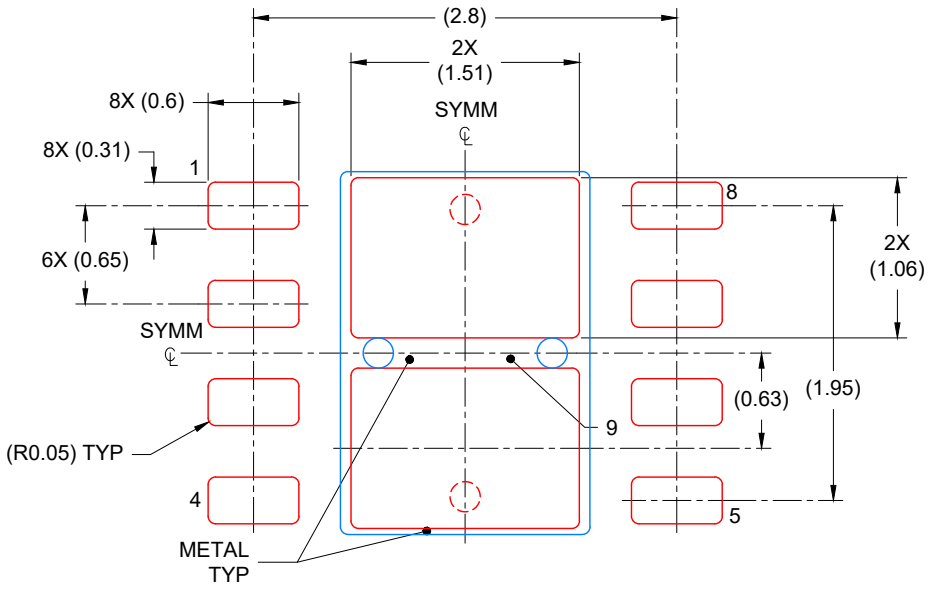
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

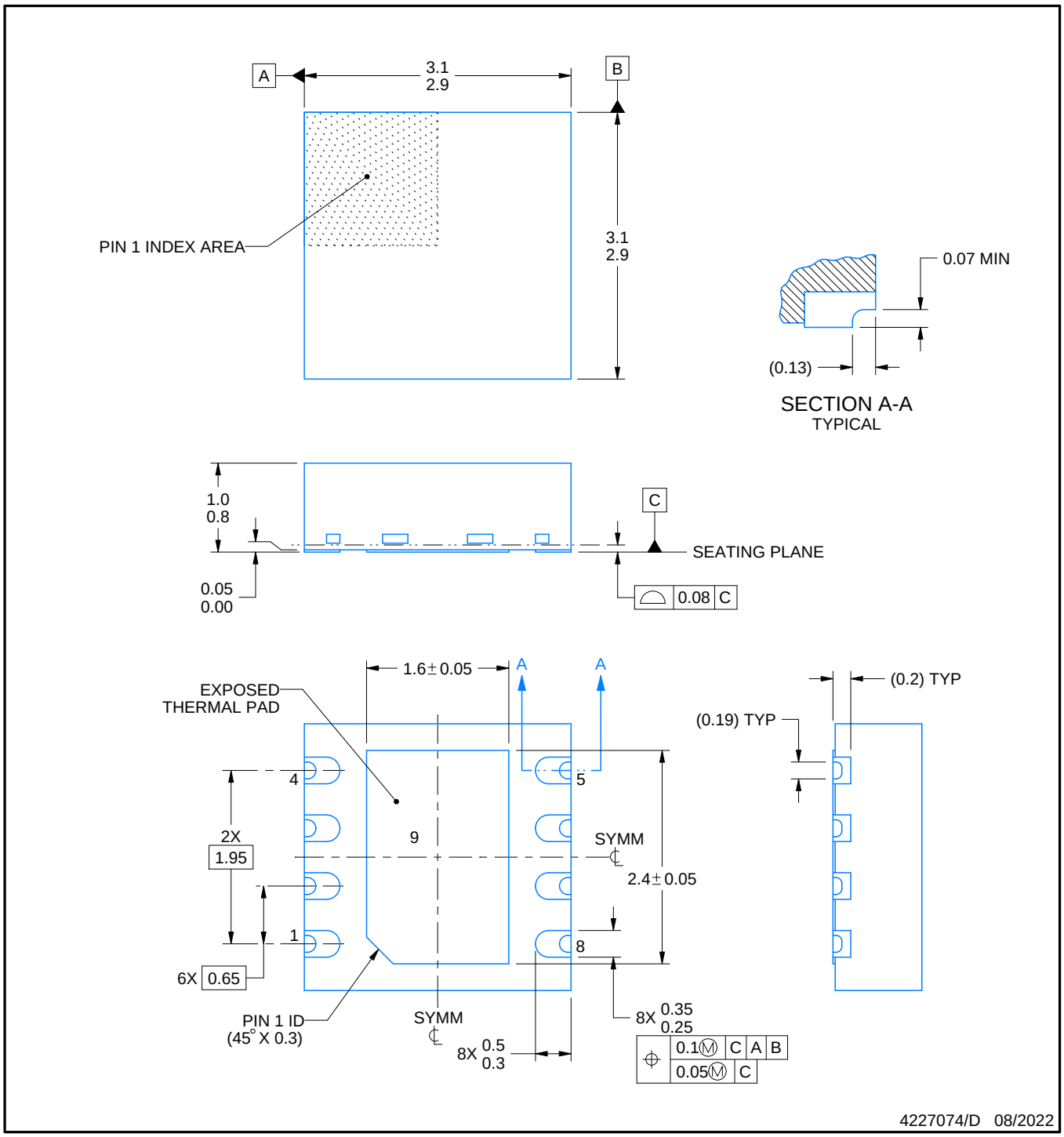
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRB0008K

PACKAGE OUTLINE

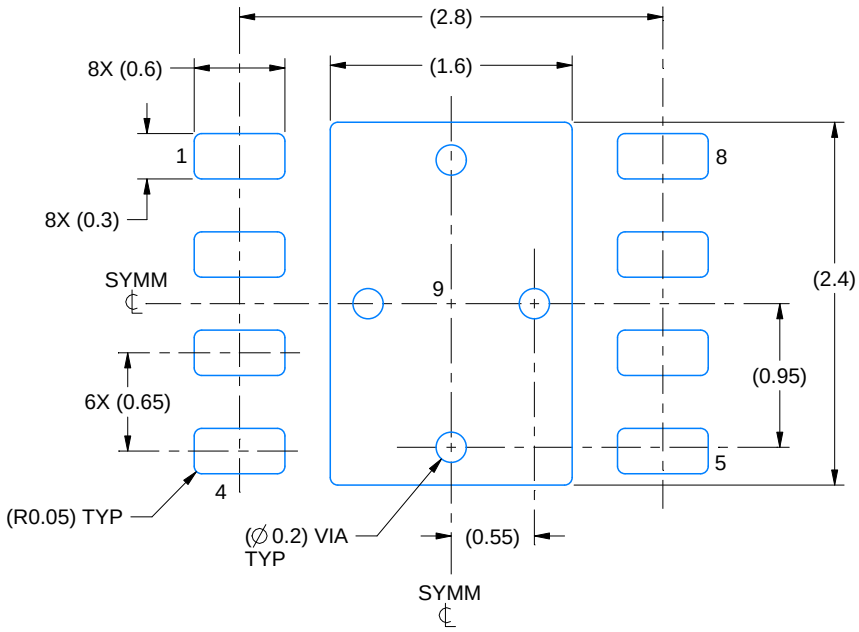
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

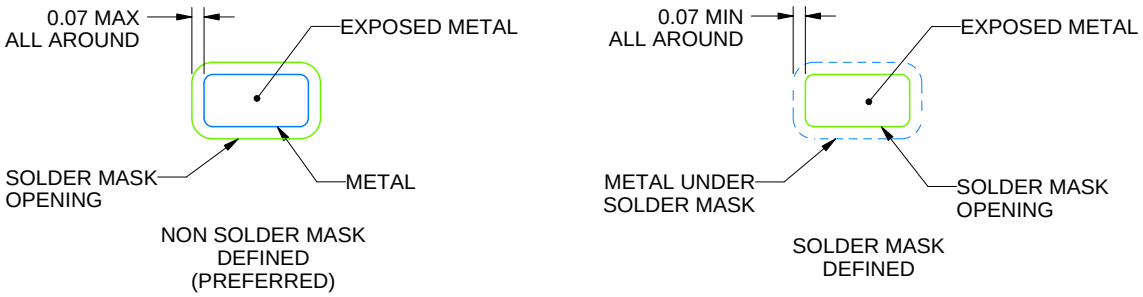


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

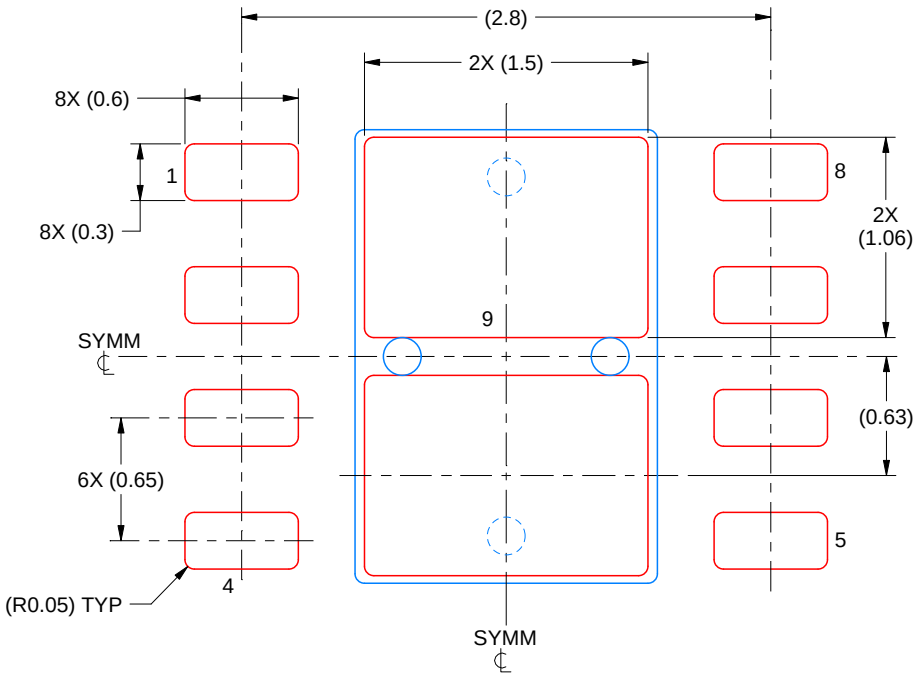


SOLDER MASK DETAILS

4227074/D 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



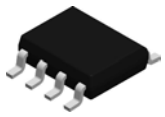
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4227074/D 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

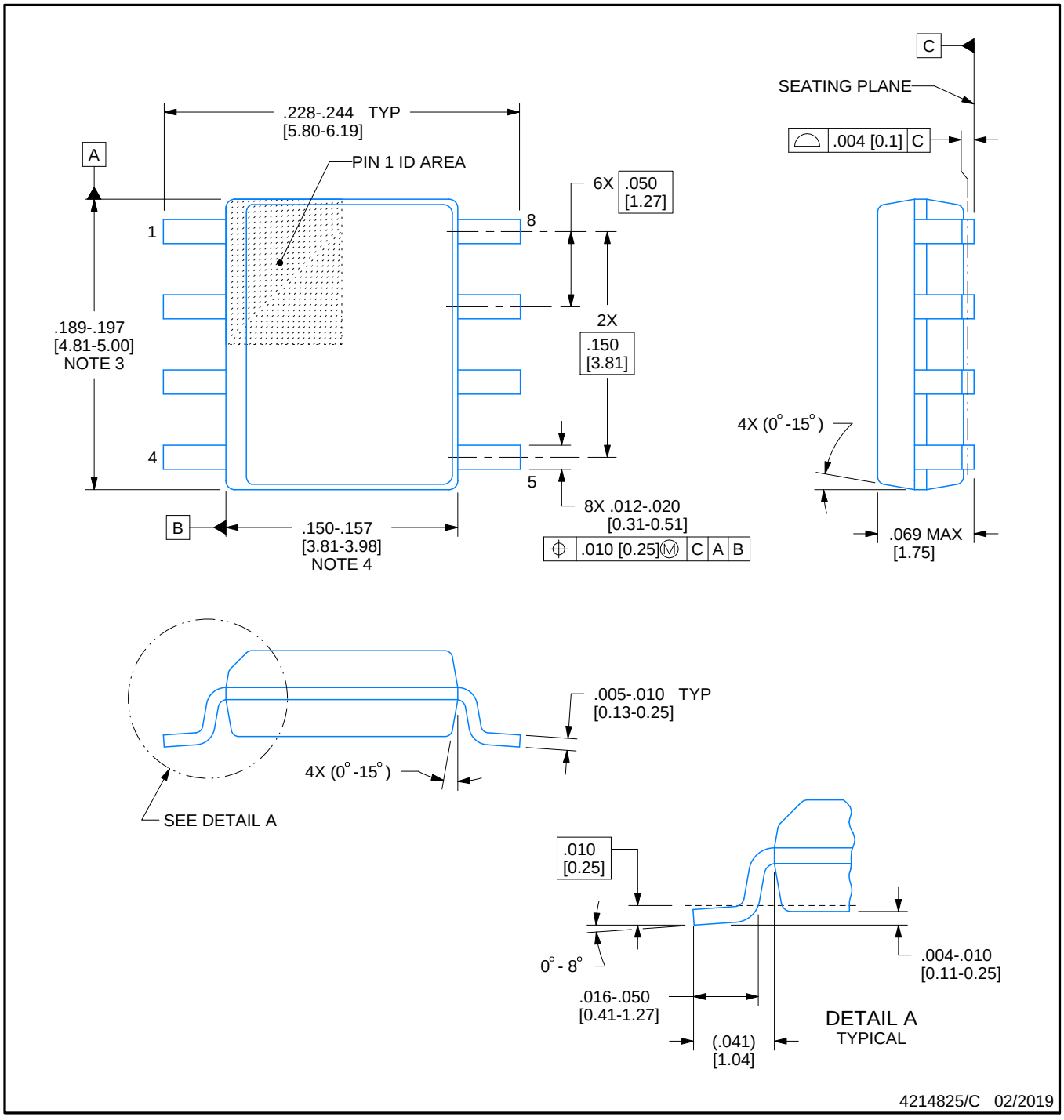


PACKAGE OUTLINE

D0008A

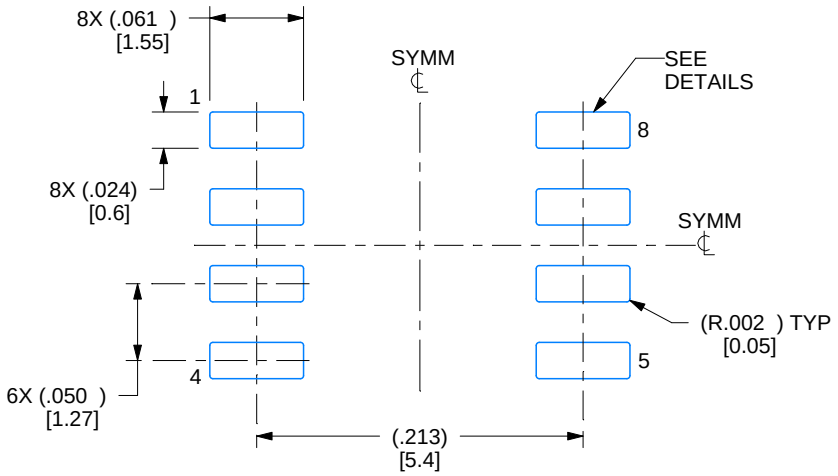
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

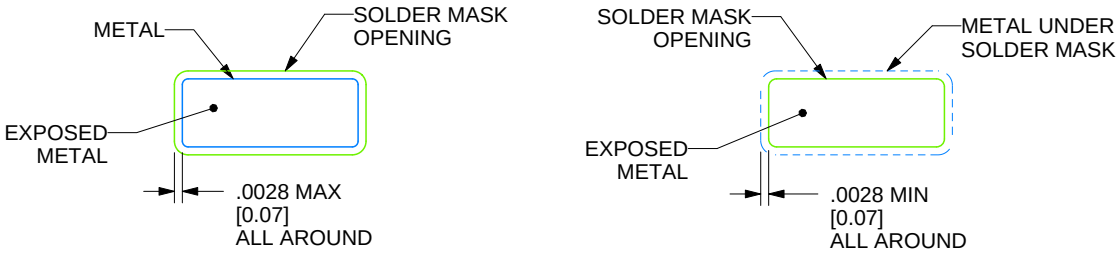


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

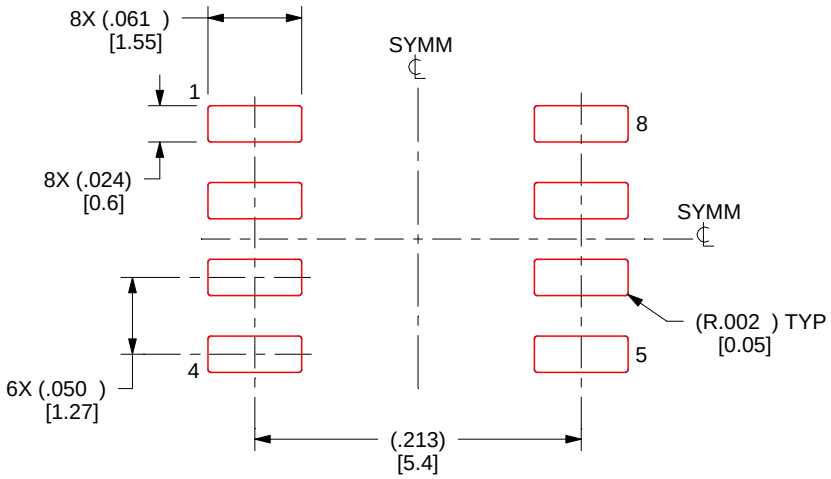
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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