TEXAS INSTRUMENTS
TLIN1039-Q1
JAJSMR1 – AUGUST 2021

TLIN1039-Q1 ローカル相互接続ネットワーク (LIN) トランシーバ、ドミナント状態タイムアウト対応

1 特長

- 車載アプリケーション用に AEC-Q100 (グレード 1) 認定済み
- LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2A、ISO/DIS 17987–4 電気的物理層 (EPL) 仕様に準拠
- SAE J2602-1 に準拠した車載用途向け LIN ネットワーク
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 12V アプリケーションをサポート
- 広い動作時電源電圧範囲:4.5V～36V
- 最高 20kbps の LIN 送信データ・レート
- 最高 100kbps の LIN 受信データ・レート
- スリープ・モード:超低消費電流で、次のウェイクアップ・イベントに対応
  - LIN バス
  - EN 経由のローカル・ウェイクアップ
- 45kΩ の LIN プルアップ抵抗を内蔵
- 電源オン / オフ時の LIN バスと RXD 出力のグリッチを防止
- 保護機能:
  - LIN バスの障害耐性:±45V
  - V_{SUP} の低電圧保護
  - TXD ドミナント・タイムアウト保護 (DTO)
  - サーマル・シャットダウン保護機能
  - 電源なしノードまたはグランド切断に対するシステム・レベルのフェイルセーフ
- 接合部温度範囲:-40℃～150℃
- 小フットプリントの SOT-23 パッケージで供給

2 アプリケーション

- ボディ・エレクトロニクス / 照明
- インフォテインメントとクラスタ
- ハイブリッド電気自動車およびパワー・トレイン・システム
- パッシブ型安全運転支援システム
- 家電製品

3 概要

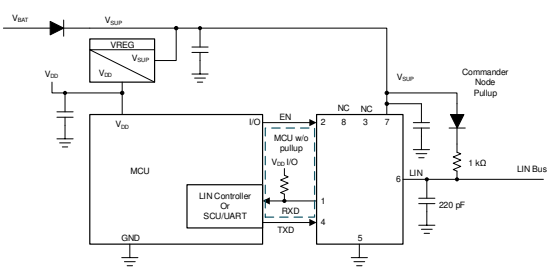
TLIN1039-Q1 は、ウェイクアップおよび保護機能を内蔵し、LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2A、および ISO/DIS 17987-4 標準に準拠したローカル相互接続ネットワーク (LIN) 物理層トランシーバです。LIN は、車載ネットワークで一般的に使用されている単線式双方向バスです。TLIN1039-Q1 は、幅広い動作電圧に対応し、かつ追加のバス・フォルト保護機能を備えた 12V アプリケーションをサポートするように設計されています。

TLIN1039-Q1 のトランスミッタは最大 20kbps のデータ・レートをサポートしています。TLIN1039-Q1 レシーバは、高速インライン・プログラミング用に最大 100kbps のデータ・レートをサポートしています。TLIN1039-Q1 は、電磁気放射 (EME) を低減する電流制限波形整形ドライバを使用して、TXD 入力のデータ・ストリームを LIN バス信号に変換します。本レシーバは、データ・ストリームを論理レベル信号に変換し、オープン・ドレインの RXD ピンを経由してマイクロプロセッサに送信します。スリープ・モードから LIN バスやピンによるウェイクアップが可能なため、非常に低い消費電流を実現できます。

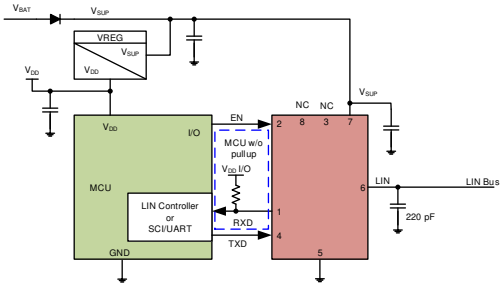
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TLIN1039-Q1	SOT-23 (8) (DDF)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図、コマンダ・モード



概略回路図、レスポンダ・モード

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2021	*	Initial release.

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5 概要 (続き)

TLIN1039-Q1 には LIN レスポンダ・ノード・アプリケーション用の抵抗、ESD 保護、フォルト保護が内蔵されているため、アプリケーションの外付け部品数を減らせます。このデバイスでは、グランドのシフトまたは電源電圧の切断が発生しても、電流が LIN 経由で電源入力に逆流することはありません。本デバイスは、低電圧検出、サーマル・シャットダウン保護、グランド喪失保護機能も内蔵しています。

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6 Pin Configuration and Functions

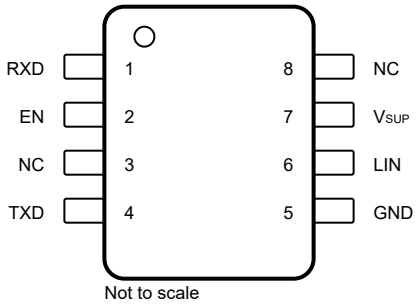


図 6-1. DDF Package, 8-Pin (SOT), Top View

表 6-1. Pin Functions

PIN		Type	DESCRIPTION
Name	No.		
RXD	1	DO	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	DI	Enable input - High puts the device in normal operation mode and low puts the device in sleep mode; integrated pull-down
NC	3	–	Not connected
TXD	4	DI	TXD input interface to control state of LIN output; integrated pull-down
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V_{SUP}	7	HV Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
NC	8	–	Not connected

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7 Specifications

7.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO 17987)	–0.3	45	V
V_{LIN}	LIN Bus input voltage (ISO 17987)	–45	45	V
V_{LOGIC_INPUT}	Logic input voltage (TXD, EN)	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage (RXD)	–0.3	6	V
I_O	Digital pin output current		8	mA
T_J	Junction Temp	–55	165	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM) classification level 3B: V_{SUP} with respect to ground		±8000	V
		Human body model (HBM) classification level 3B: LIN with respect to ground		±10000	V
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±4000	V
V_{ESD}	Electrostatic discharge	Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings - IEC Specification

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	LIN, V_{SUP} terminal to GND(1)	IEC 62228-2 per ISO 10605 Contact discharge R = 330 Ω, C = 150 pF (IEC 61000-4-2)	±8000	V
		LIN terminal to GND(1)	IEC 62228-2 per ISO 10605 Indirect contact discharge R = 330 Ω, C = 150 pF (IEC 61000-4-2)	±8000	
V_{TRAN}	Non-synchronous transient injection	LIN, V_{SUP} terminal to GND(1)	IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 1	-100	V
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 2	75	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3a	-150	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3b	150	
	Direct capacitor coupling	LIN terminal to GND(2)	SAE J2962-1 per ISO 7637-3 DCC - Slow transient pulse	±30	

(1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Results given here are specific to the SAE J2962-1 Communication Transceivers Qualification Requirements - LIN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.

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7.4 Thermal Information

THERMAL METRIC(1)		TLIN1039-Q1 DDF(SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	4.5		36	V
V_{LIN}	LIN Bus input voltage	0		36	V
V_{LOGIC}	Logic Pin Voltage	0		5.25	V
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

7.6 Power Supply Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
V_{SUP}	Operational supply voltage ISO 17987 Param 10	Device is operational beyond the LIN defined nominal supply voltage range See 図 8-1 and 図 8-2	4.5		36	V
	Nominal supply voltage ISO 17987 Param 10	Normal and standby modes(1) See 図 8-1 and 図 8-2	4.5		36	V
		Sleep mode	4.5		36	V
I_{SUP}	Supply current Bus dominant	Normal mode EN = High, R_{LIN} ≥ 500 Ω, C_{LIN} ≤ 10 nF		1.2	6.5	mA
		Standby mode EN = 0 V, R_{LIN} ≥ 500 Ω, C_{LIN} ≤ 10 nF		1	1.7	mA
	Supply current Bus recessive	Normal mode EN = High		300	700	µA
		Standby mode EN = 0 V		20	30	µA
	Supply current Sleep mode	4.5 V < V_{SUP} ≤ 14 V, EN = 0 V, TXD and RXD floating		9	14	µA
		14 V < V_{SUP} ≤ 36 V, EN = 0 V, TXD and RXD floating			22	µA
$UV_{SUP(R)}$	Under voltage V_{SUP} threshold	Ramp up		4.15	4.45	V
$UV_{SUP(F)}$	Under voltage V_{SUP} threshold	Ramp down	3.5	4		V
UV_{HYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.13		V

(1) Ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50% duty cycle and 36 V swing.

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7.7 Electrical Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OL}	Low-level voltage	Based upon external pull-up to V_{CC} (4)			0.6	V
I_{OL}	Low-level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5		5	µA
TXD Input Terminal						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
I_{LKG}	Low-level input leakage current	TXD = 0 V	–5		5	µA
R_{TXD}	Internal pull-down resistor value		125	350	800	kΩ
EN Input Terminal						
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{IH}	High-level input voltage		2		5.25	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low-level input current	EN = 0 V	–5		5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIN Terminal						
V_{OH}	LIN recessive high-level output voltage(3)	TXD = V_{CC}, I_O = 0 mA 7 V ≤ V_{SUP} ≤ 36 V	0.85			V_{SUP}
V_{OH}	LIN recessive high-level output voltage(3)	TXD = V_{CC}, I_O = 0 mA 4.5 V ≤ V_{SUP} < 7 V	3			V
V_{OH}	LIN recessive high-level output voltage(1) (2)	TXD = V_{CC}, I_O = 0 mA 7 V ≤ V_{SUP} ≤ 18 V	0.8			V_{SUP}
V_{OL}	LIN dominant low-level output voltage(3)	TXD = 0 V 7 V ≤ V_{SUP} ≤ 36 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(3)	TXD = 0 V 4.5 V ≤ V_{SUP} < 7 V			1.2	V
V_{OL}	LIN dominant low-level output voltage(1) (2)	TXD = 0 V 7 V ≤ V_{SUP} ≤ 18 V			0.2	V_{SUP}
V_{BUSdom}	Low-level input voltage ISO 17987 Param 17	LIN dominant (including LIN dominant for wake up) See 図 8-3 and 図 8-4			0.4	V_{SUP}
V_{BUSrec}	High-level input voltage ISO 17987 Param 18	LIN recessive See 図 8-3 and 図 8-4	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage threshold(1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltage threshold(1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.4		0.53	V_{SUP}
$V_{SUP_NON_OP}$	V_{SUP} where impact of recessive LIN bus < 5%(3)	TXD & RXD open 4.5 V ≤ LIN ≤ 45 V	–0.3		42	V
V_{BUS_CNT}	Receiver center threshold	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2 See 図 8-3 and 図 8-4	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO 17987)	V_{HYS} = V_{BUSrec} - V_{BUSdom} See 図 8-3 and 図 8-4			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	V_{HYS} = V_{IH} - V_{IL} See 図 8-3 and 図 8-4	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I_{SERIAL_DIODE} = 10 µA	0.4	0.7	1.0	V
$I_{BUS(LIM)}$	Limiting current ISO 17987 Param 12	TXD = 0 V, V_{LIN} = 18 V V_{SUP} = 18 V	40	90	200	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant	Driver off/recessive, LIN = 0 V V_{SUP} = 12 V See 図 8-6	–1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive	Driver off/recessive, LIN ≥ V_{SUP} 4.5 V ≤ V_{SUP} ≤ 36 V See 図 8-7			20	µA

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7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive	Driver off/recessive, LIN = V_{SUP} See 図 8-7	–5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground	GND_{Device} = V_{SUP} = 18 V R_{Meas} = 1 kΩ 0 V < V_{LIN} < 18 V	–1		1	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground (5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{COMMANDER}$ = 1 kΩ, C_L = 1 nF $R_{RESPONDER}$ = 20 kΩ, C_L = 1 nF LIN = dominant	–1		1	mA
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground (5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{COMMANDER}$ = 1 kΩ, C_L = 1 nF $R_{RESPONDER}$ = 20 kΩ, C_L = 1 nF LIN = recessive	–100		100	µA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply	V_{SUP} = GND 0 V ≤ V_{LIN} ≤ 18 V			5	µA
I_{RSLEEP}	Pull-up current source to V_{SUP} sleep mode	V_{SUP} = 14 V, LIN = GND	–20		–1.5	µA
R_{PU}	Pull-up resistor to V_{SUP}	Normal and standby modes	20	45	60	kΩ
C_{LIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF
Duty Cycle Characteristics						
D1	Duty Cycle 1(3) ISO 17987 Param 27	$TH_{REC(MAX)}$ = 0.744 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11	0.396			
D1	Duty Cycle 1 (3) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11	0.396			
D1	Duty cycle 1(1) (2) (6)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11	0.396			
D2	Duty Cycle 2(3) ISO 17987 Param 28	$TH_{REC(MIN)}$ = 0.422 x V_{SUP} $TH_{DOM(MIN)}$ = 0.284 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11			0.581	
D2	Duty cycle 2(3) (6)	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11			0.581	
D2	Duty cycle 2(1) (2) (6)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11			0.581	
D3	Duty Cycle 3(3) ISO 17987 Param 29	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11	0.417			
D3	Duty Cycle 3(3) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP} $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11	0.417			

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7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D3	Duty cycle 3(1) (2) (6)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11	0.417			
D4	Duty Cycle 4(3) ISO 17987 Param 30	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11			0.59	
D4	Duty Cycle 4(3) (6)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11			0.59	
D4	Duty cycle 4(1) (2) (6)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) See 図 8-10 and 図 8-11			0.59	
$D1_{LB}$	Duty cycle 1 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 52 µs	0.396			
$D2_{LB}$	Duty cycle 2 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 52 µs			0.581	
$D3_{LB}$	Duty cycle 3 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs	0.396			
D_{4LB}	Duty cycle 4 at low battery(1) (2) (6)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 96 µs			0.581	
$T_{r\text{-}d\ max_D1}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{REC(MAX)_D1}$ - $t_{DOM(MIN)_D1}$			10.8	µs
$T_{d\text{-}r\ max_D2}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{DOM(MAX)_D2}$ - $t_{REC(MIN)_D2}$			8.4	µs
$T_{r\text{-}d\ max_D3}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{REC(MAX)_D3}$ - $t_{DOM(MIN)_D3}$			15.9	µs
$T_{d\text{-}r\ max_D4}$	Transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{DOM(MAX)_D4}$ - $t_{REC(MIN)_D4}$			17.28	µs
$T_{r\text{-}d\ max_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (6) Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{REC(MAX)_low}$ - $t_{DOM(MIN)_low}$			10.8	µs
$T_{d\text{-}r\ max_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (6) Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{DOM(MAX)_low}$ - $t_{REC(MIN)_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(6) Specified by design

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7.8 AC Switching Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdr}	Receiver rising propagation delay time ISO 17987 Param 31	5.5 V ≤ VSUP , R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See 図 8-12 and 図 8-13			5	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				5	µs
t_{rx_pdr}	Receiver rising propagation delay time ISO 17987 Param 31	4.5 V ≤ VSUP < 5.5 V, R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See 図 8-12 and 図 8-13			6	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				6	µs
t_{rx_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time ISO 17987 Param 32	Rising edge with respect to falling edge $t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}$ R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See 図 8-12 and 図 8-13	–2		2	µs
t_{LINBUS}	Minimum dominant time on LIN bus for wake-up	See 図 8-16, 図 9-2 and 図 9-3	25	65	150	µs
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See 図 9-3	8	25	50	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin See 図 9-4 and 図 8-14	2		15	µs
t_{NOMINT}	Normal mode initialization time(1)	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby to normal mode. See 図 8-14			45	µs
t_{PWR}	Power-up time	Time it takes for valid data on RXD upon power-up			1.5	ms
t_{TXD_DTO}	Dominant state time out		20	50	80	ms

(1) The transition time from sleep mode to normal mode includes both t_{MODE_CHANGE} and t_{NOMINT}.

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7.9 Typical Characteristics

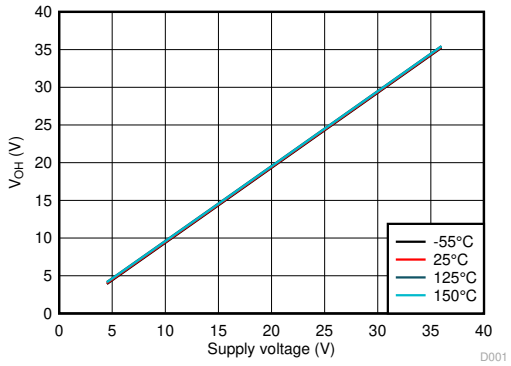


図 7-1. V_{OH} vs V_{SUP} and Temperature

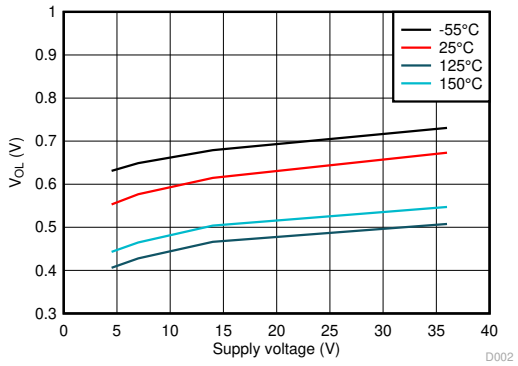


図 7-2. V_{OL} vs V_{SUP} and Temperature

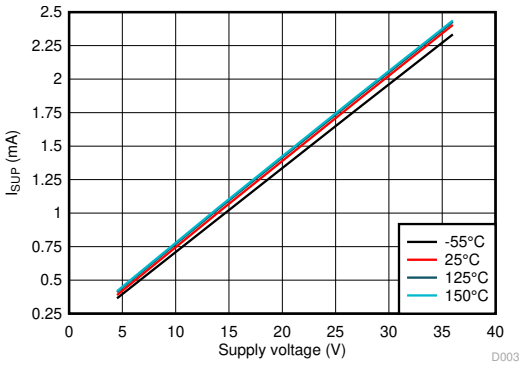


図 7-3. I_{SUP} Dominant vs V_{SUP} and Temperature

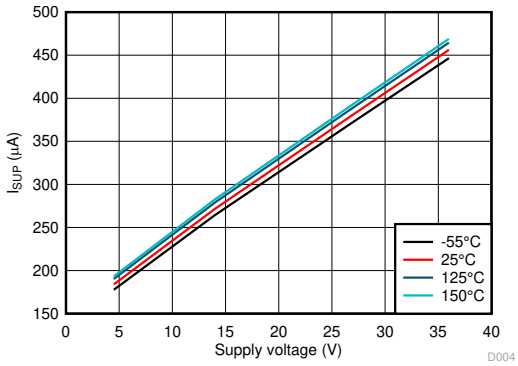


図 7-4. I_{SUP} Recessive vs V_{SUP} and Temperature

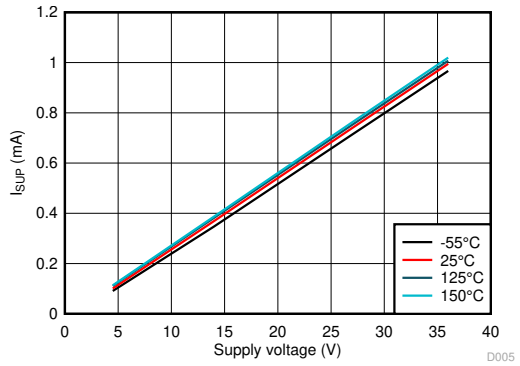


図 7-5. Standby Mode I_{SUP} Dominant vs V_{SUP} and Temperature

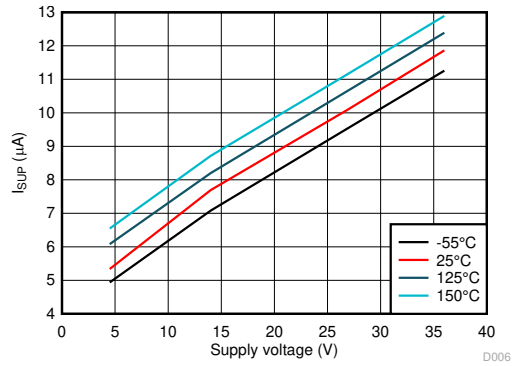


図 7-6. Standby Mode I_{SUP} Recessive vs V_{SUP} and Temperature

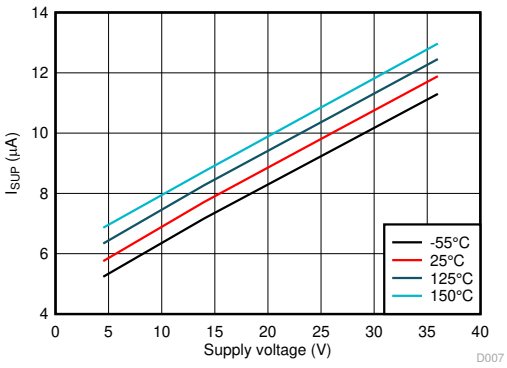


図 7-7. Sleep Mode I_{SUP} vs V_{SUP} and Temperature

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8 Parameter Measurement Information

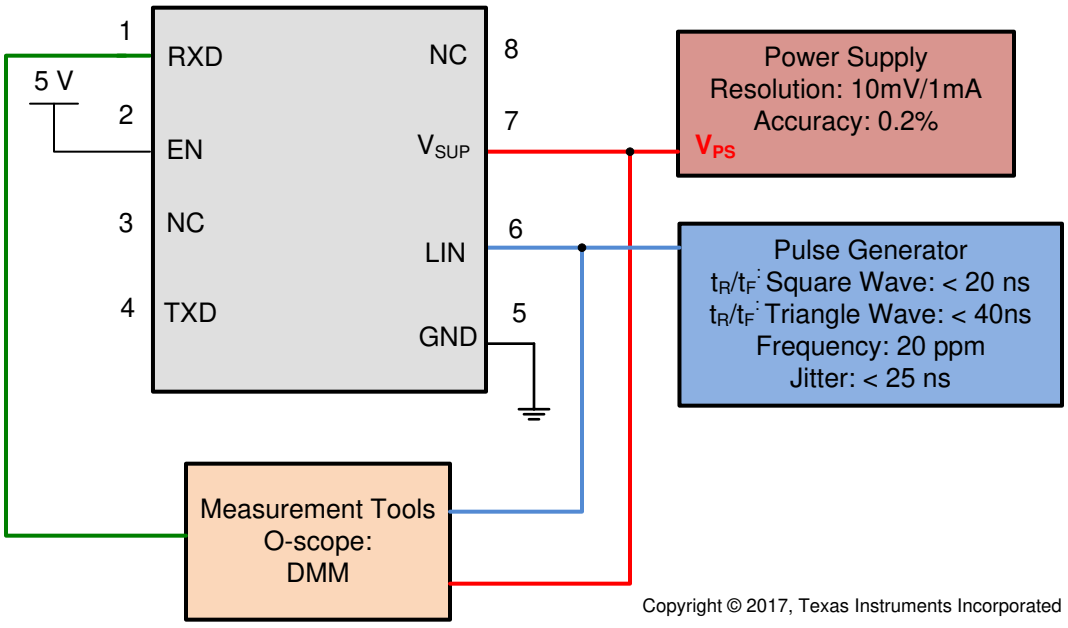


図 8-1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

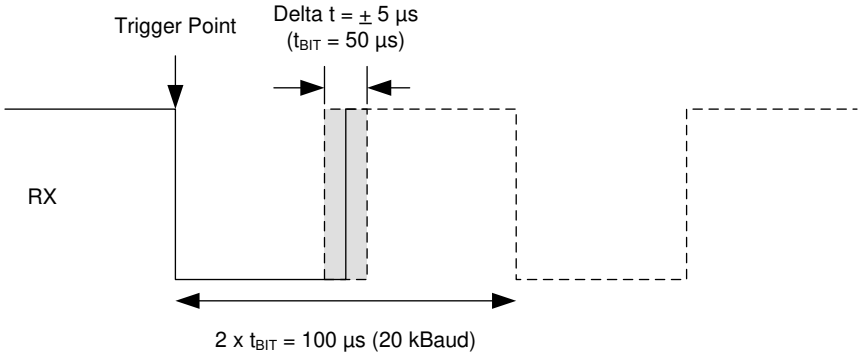


図 8-2. RX Response: Operating Voltage Range

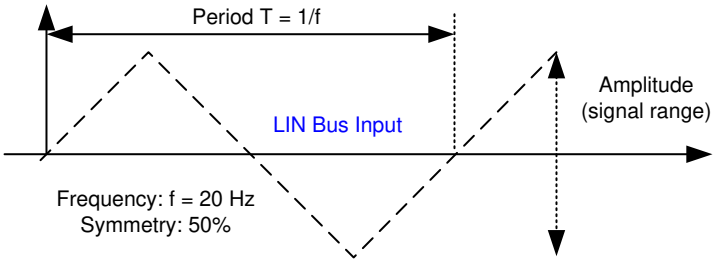


図 8-3. LIN Bus Input Signal

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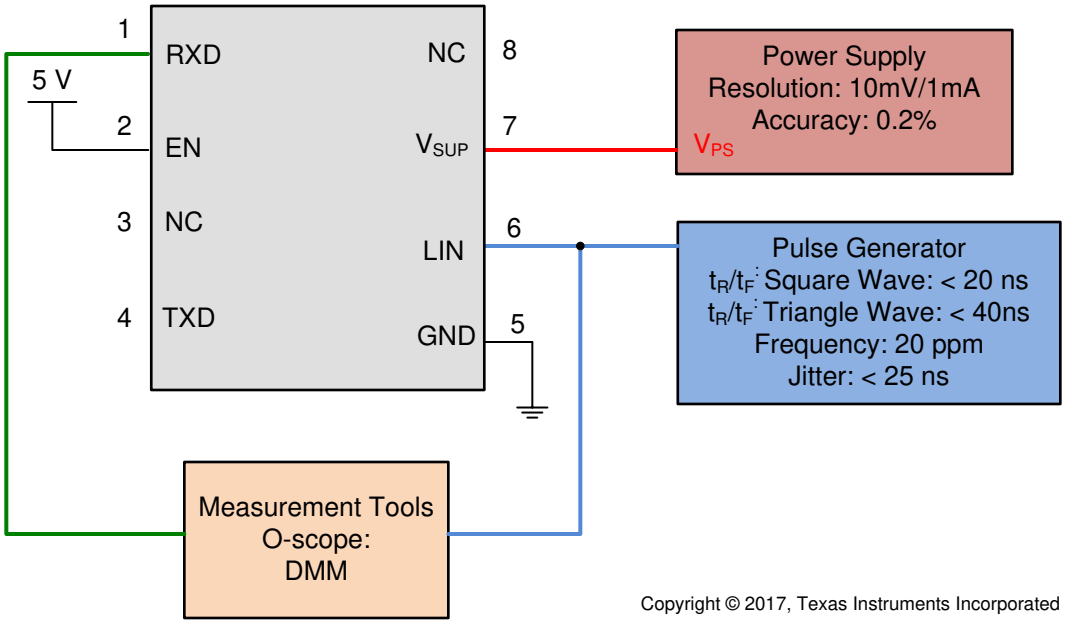


図 8-4. LIN Receiver Test with RX access Param 17, 18, 19, 20

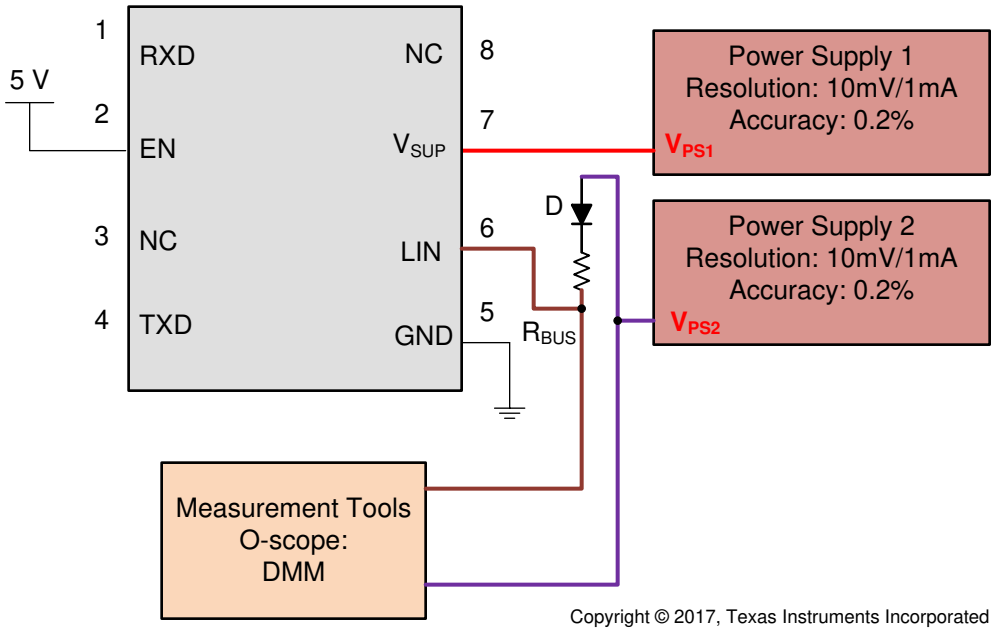
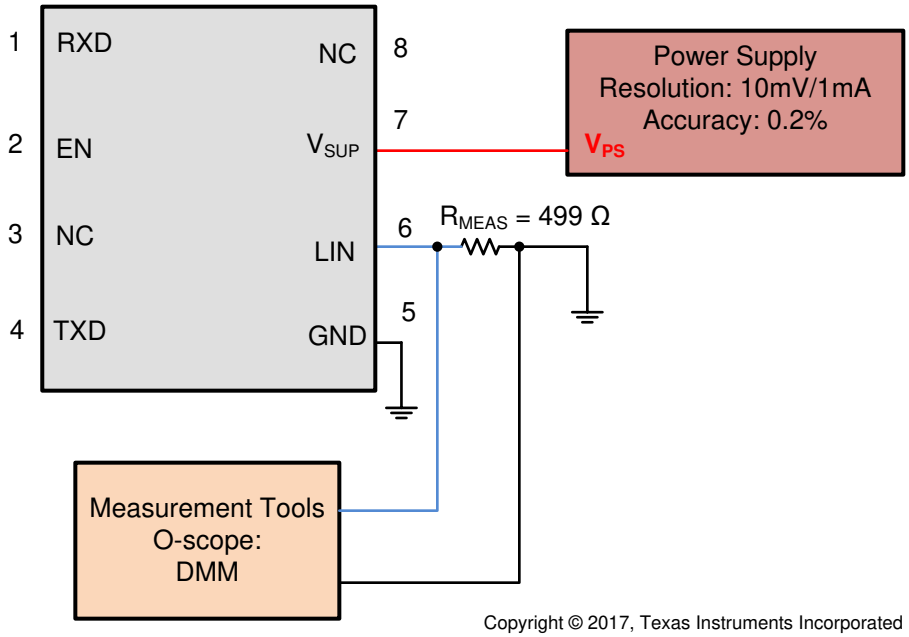
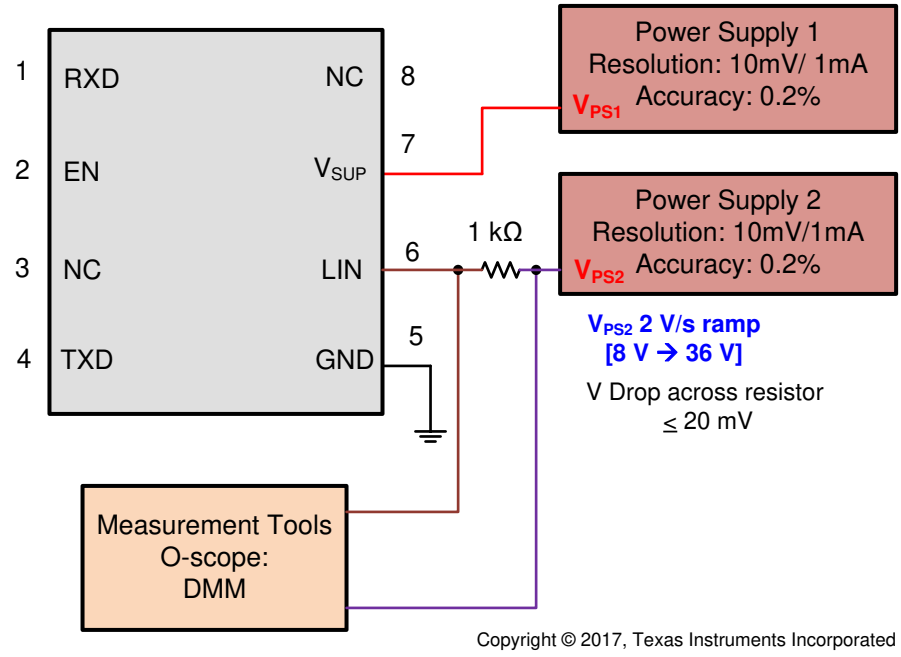


図 8-5. $V_{SUP_NON_OP}$ Param 11



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図 8-6. Test Circuit for $I_{BUS_PAS_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13



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図 8-7. Test Circuit for $I_{BUS_PAS_rec}$ Param 14

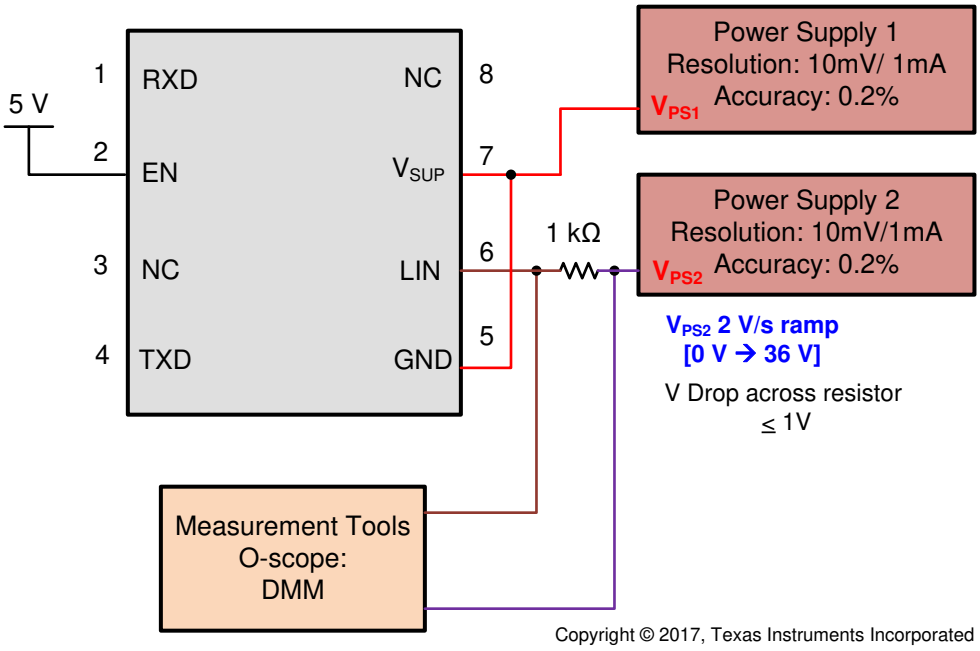


図 8-8. Test Circuit for $I_{BUS_NO_GND}$ Loss of GND

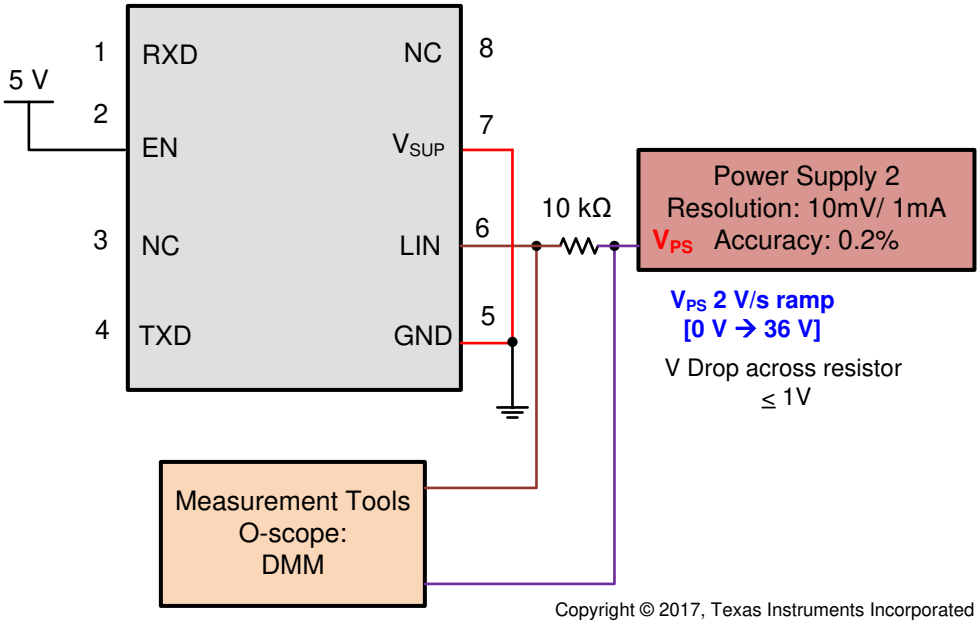
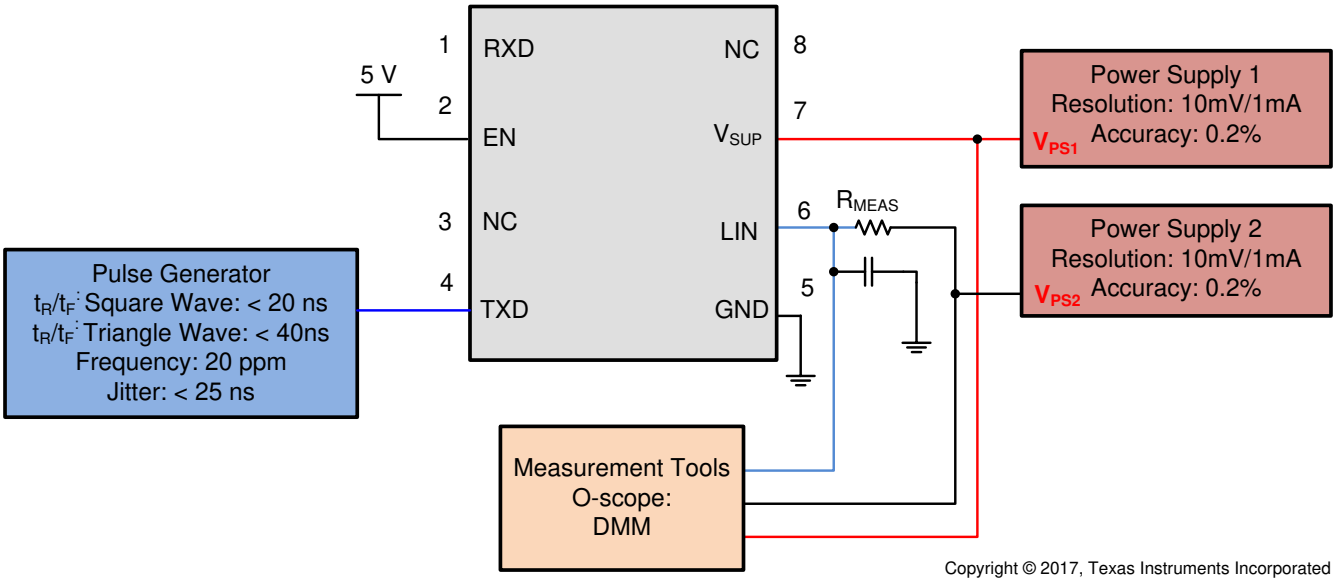


図 8-9. Test Circuit for $I_{BUS_NO_BAT}$ Loss of Battery



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図 8-10. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

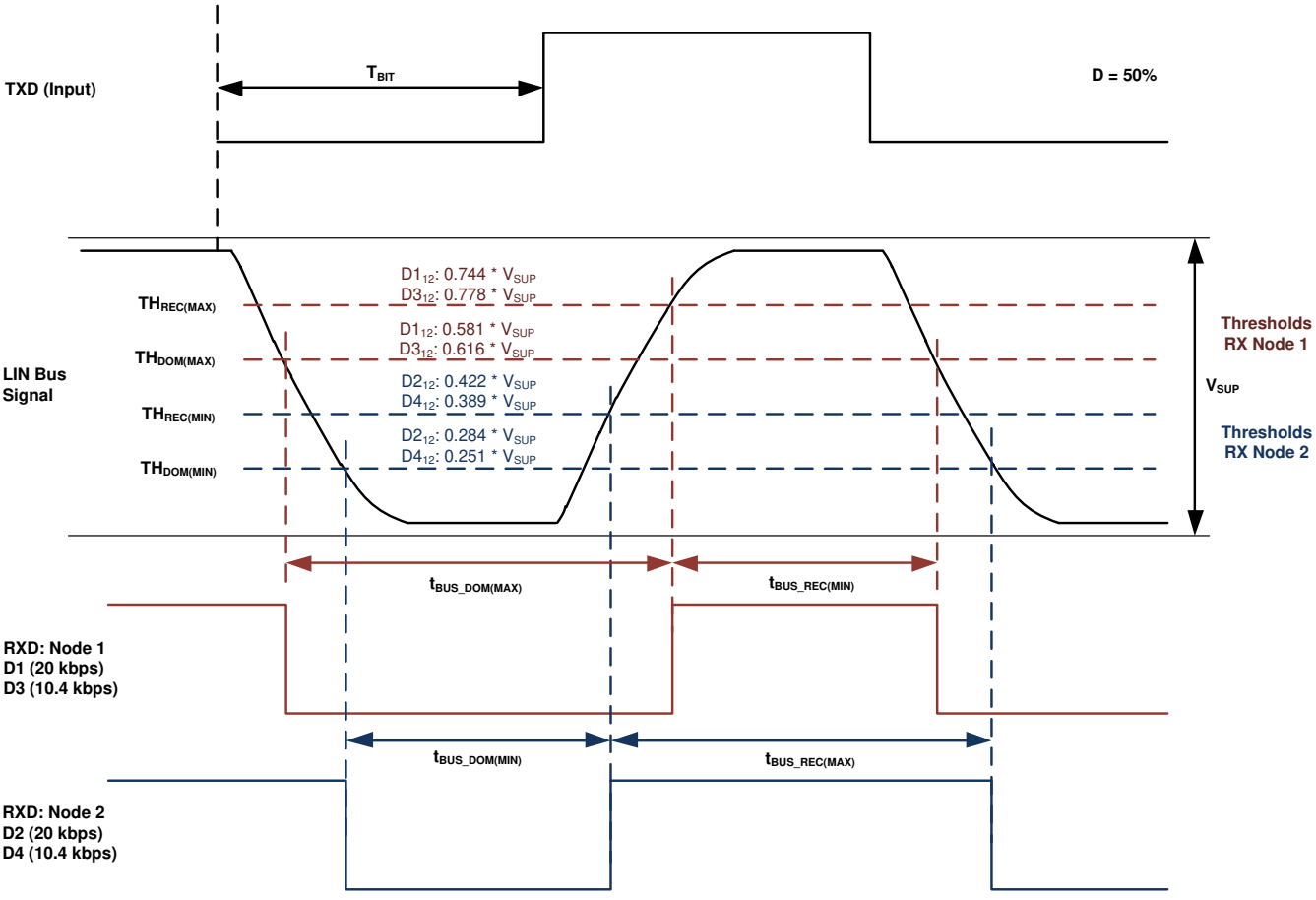


図 8-11. Definition of Bus Timing Parameters

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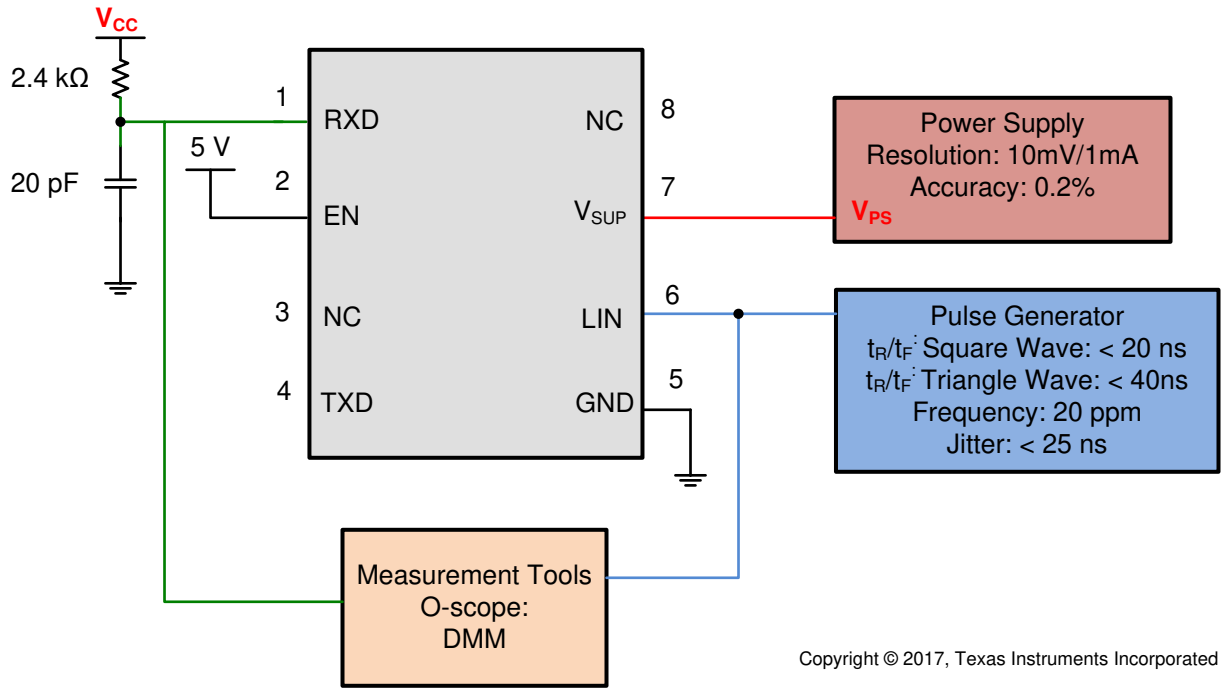


図 8-12. Propagation Delay Test Circuit; Param 31, 32

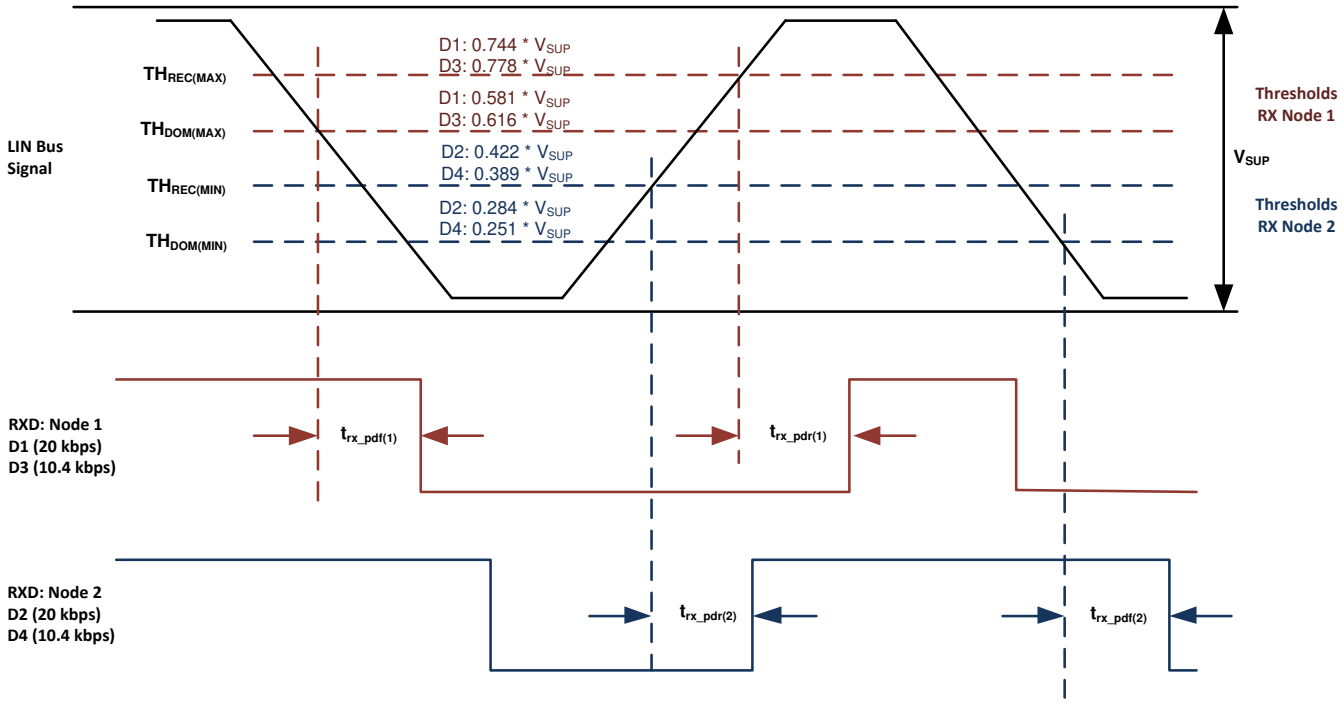


図 8-13. Propagation Delay

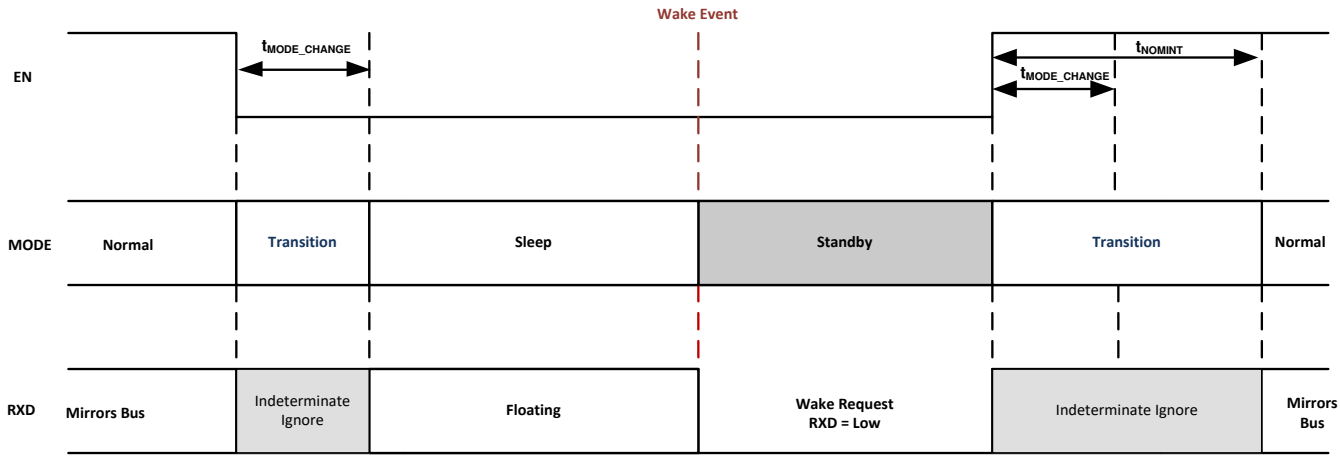


図 8-14. Mode Transitions

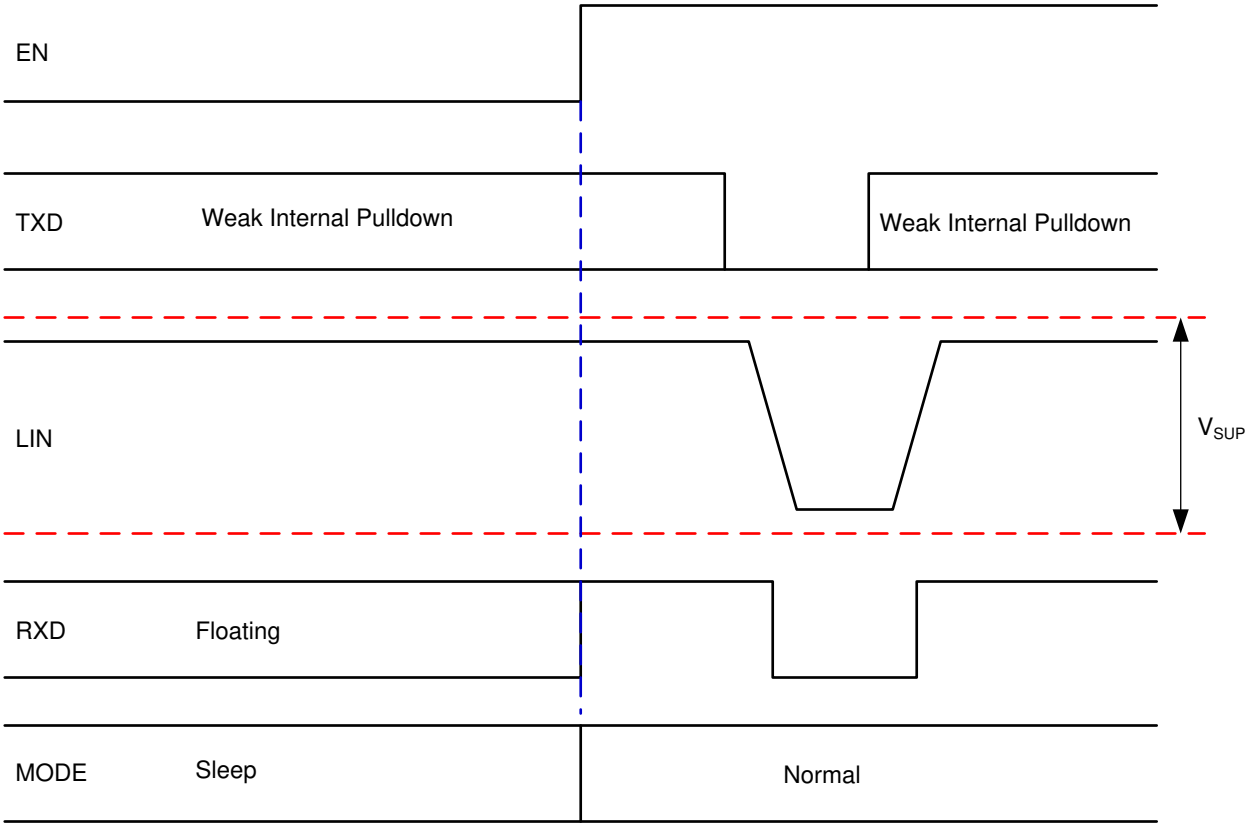


図 8-15. Wakeup Through EN

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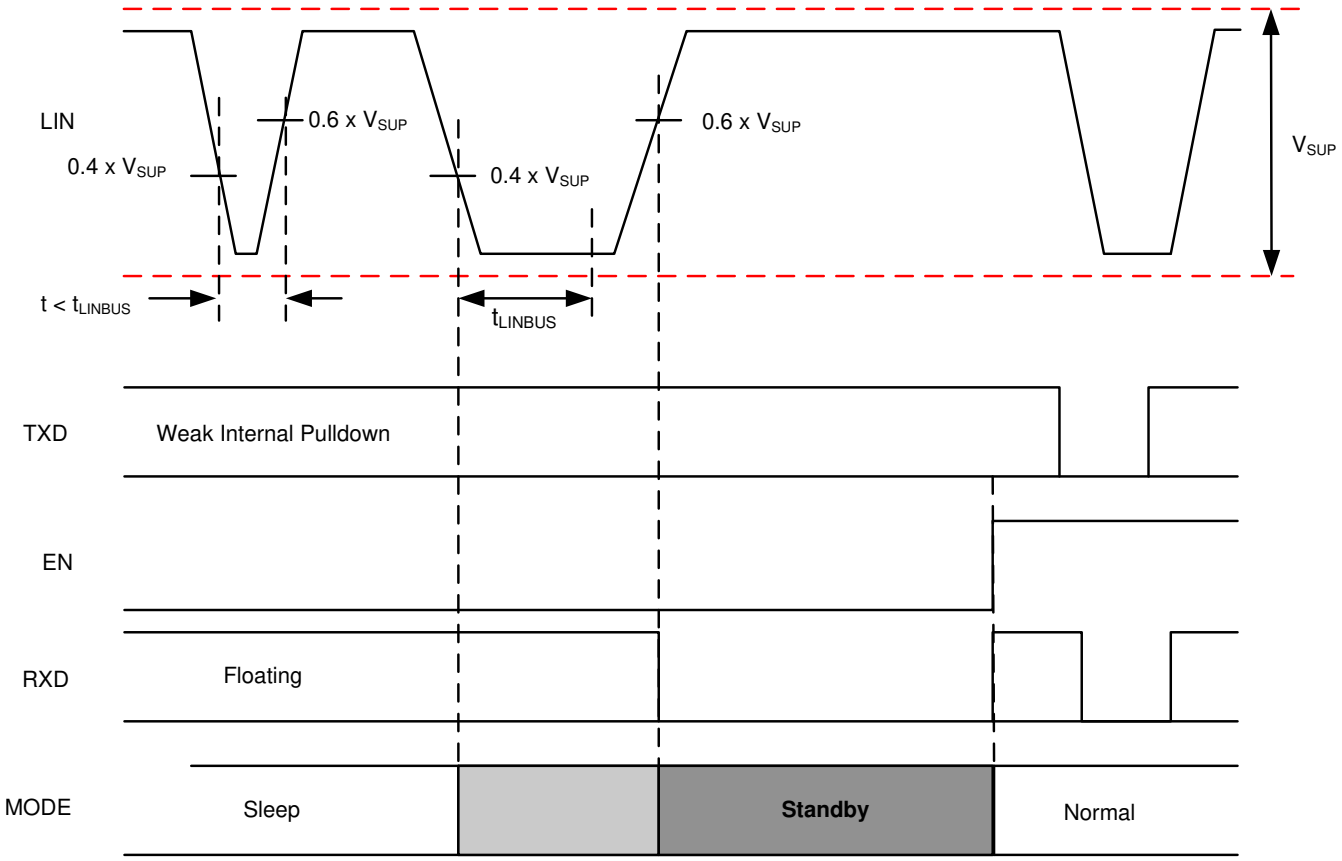


図 8-16. Wakeup through LIN

9 Detailed Description

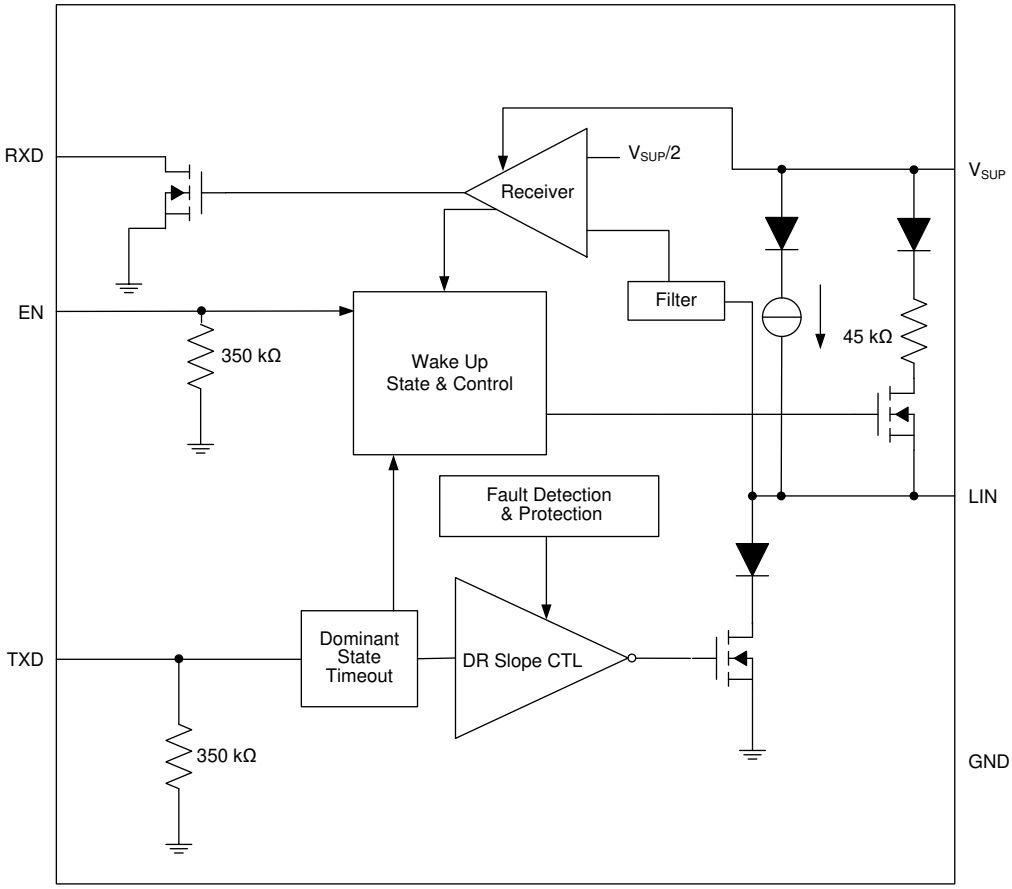
9.1 Overview

The TLIN1039-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 standards, with integrated wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low speed in-vehicle networks. The device transmitter supports data rates from 2.4 kbps to 20 kbps and the receiver works up to 100 kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN1039-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification.

The device is designed to support 12-V applications with a wide input voltage operating range and also supports low-power sleep mode. The device also provides two methods to wake up: EN pin and from the LIN bus.

The TLIN1039-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input. The device also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 45 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a commander node application per the LIN specification.

9.3.1.2 LIN Receiver Characteristics

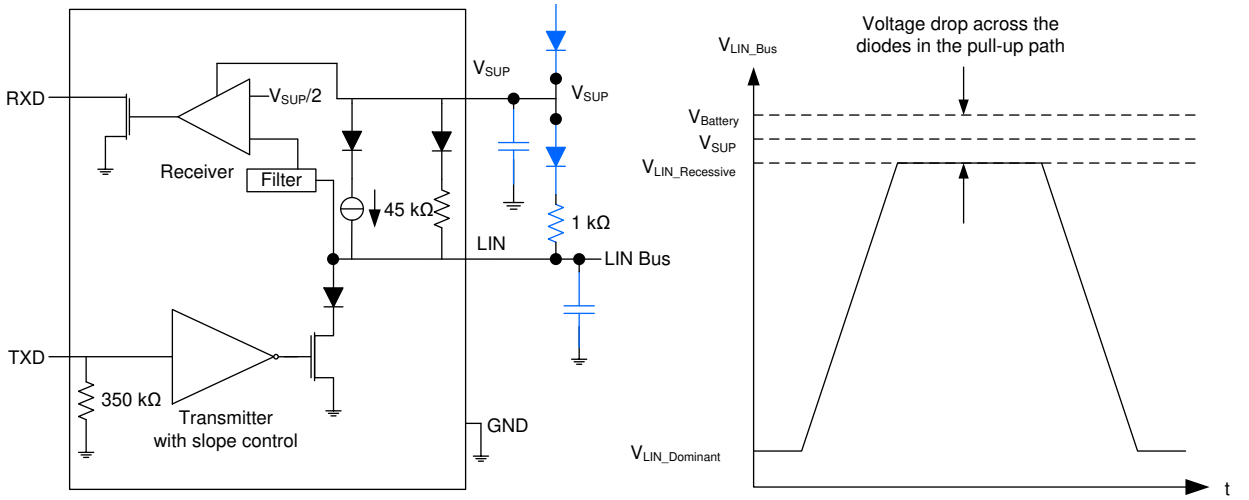
The receiver characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAE J2602 specifications. This allows the TLIN1039-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

図 9-1 shows a commander node configuration, and how the voltage levels are defined.



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図 9-1. Commander Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the MCU LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near $V_{Battery}$). See 図 9-1. The TXD input structure is compatible with microcontrollers with 3.3 V and 5 V I/O and integrates a weak pull-down resistor.

9.3.3 RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake-up request from the LIN bus.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (図 9-1). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage, as well as ensuring the input and output voltages are within their appropriate thresholds. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high, the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. After LIN bus wake-up is received, the device can enter normal mode only by making EN = high. EN has an internal pull-down resistor to make sure the device remains in low-power mode even if EN floats.

9.3.7 Protection Features

The TLIN1039-Q1 has several protection features such as:

9.3.8 TXD Dominant Timeout (DTO)

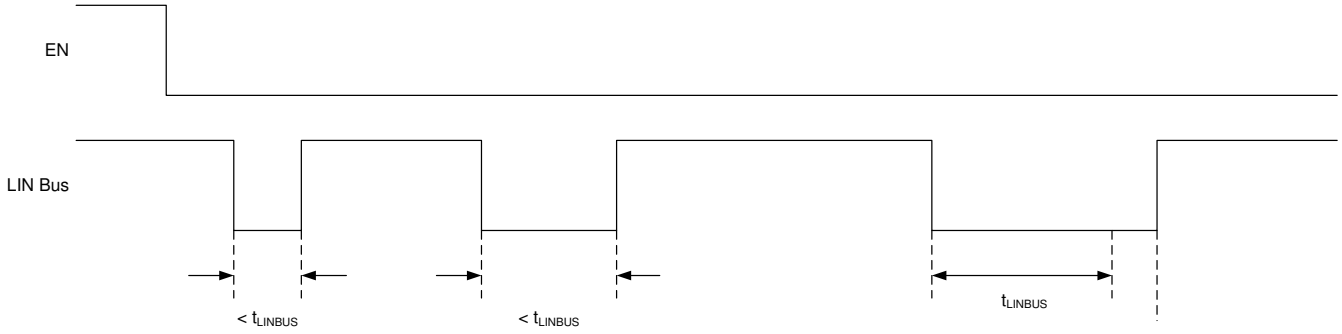
While the LIN driver is active, TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout constant of the circuit, t_{TXD_DTO}, expires the LIN driver is disabled releasing the bus line to the recessive level. This keeps the bus free for communication between other nodes on the network. The LIN driver is re-activated on the next dominant to recessive transition on the TXD terminal, thus clearing the dominant timeout. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, and the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

The TXD pin has an internal pull-down to make sure the transceiver fails to a known state if TXD is disconnected. If EN pin is high at power-up the TLIN1039-Q1 enters normal mode. With the internal TXD connected low, the DTO timer starts. To avoid a t_{TXD_DTO} fault, a recessive signal should be put onto the TXD pin before the t_{TXD_DTO} timer expires, or the transceiver should be into sleep mode by connecting EN pin low.

9.3.9 Bus Stuck Dominant System Fault: False Wake-Up Lockout

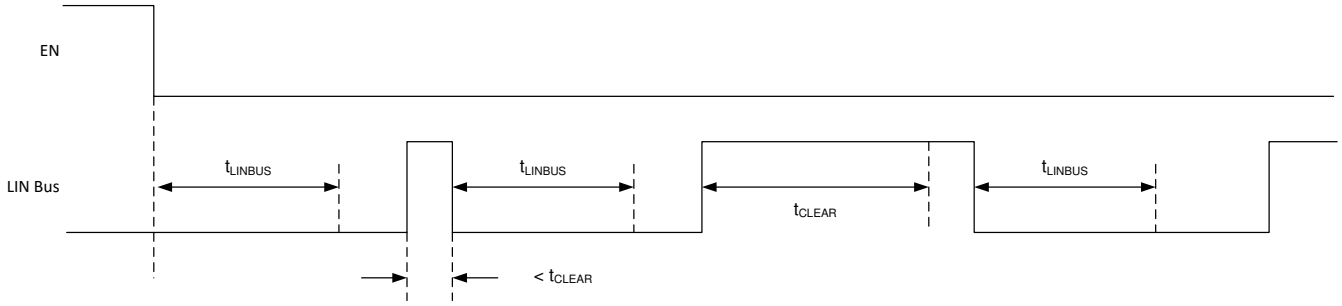
The TLIN1039-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus "clears" the bus stuck dominant, preventing excessive current consumption. 図 9-2 and 図 9-3 show the behavior of this protection.

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図 9-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake-up



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図 9-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake-up

9.3.10 Thermal Shutdown

The LIN transmitter is protected by current limiting circuitry. If the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over-temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remains in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

9.3.11 Under Voltage on V_{SUP}

The TLIN1039-Q1 contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.12 Unpowered Transceiver

In automotive applications, some LIN nodes in a system can be unpowered, ignition supplied, while others in the network remains powered by the battery. The TLIN1039-Q1 has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

9.4 Functional Modes

The TLIN1039-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. 図 9-4 graphically shows the relationship while 表 9-1 shows the state of pins

表 9-1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak current pull-up	Off	
Standby	Low	Low	45 kΩ	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	45 kΩ	On	LIN transmission up to 20 kbps

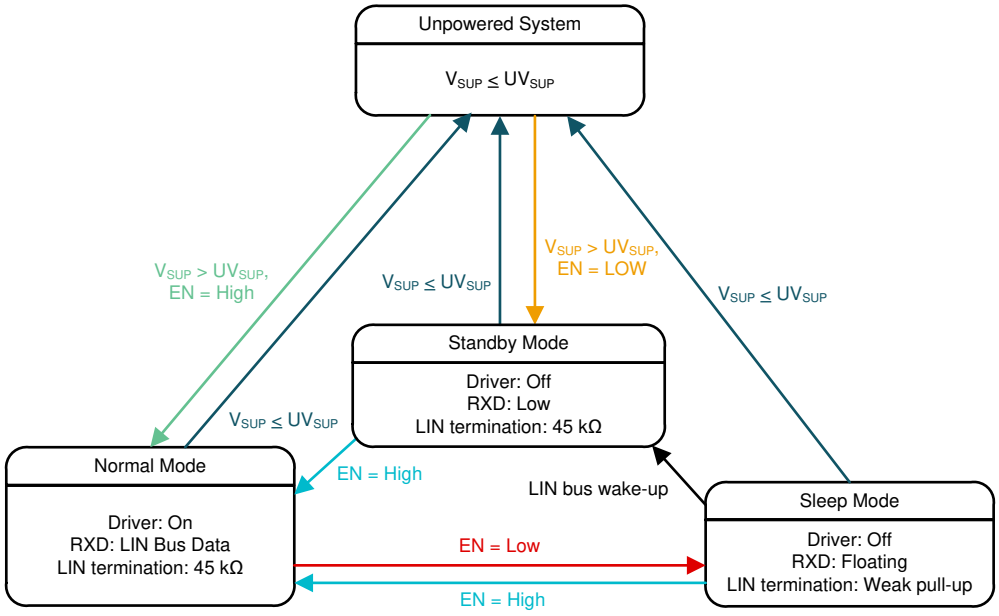


図 9-4. Operating State Diagram

9.4.1 Normal Mode

If the EN pin is high at power-up, the device will power-up in normal mode. If the EN pin is low, it will power-up in standby mode. The EN pin controls the mode of the device. In normal operational mode the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN1039-Q1 is in sleep or standby mode for > t_{NOMINT}.

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9.4.2 Sleep Mode

Sleep mode is the power saving mode for the TLIN1039-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with extremely low current consumption in this mode, the TLIN1039-Q1 can still wake-up from LIN bus through a wake-up signal or if EN is set high for ≥ t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake-up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake-up receiver are active.

9.4.3 Standby Mode

This mode is entered whenever a wake-up event occurs through LIN bus while the device is in sleep mode. The LIN bus responder mode termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See *Standby Mode Application Note* for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode, the device returns to normal mode. The normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

9.4.4 Wake-Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After the t_{LINBUS} filter time has been met, a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake-up event, eliminating false wake-ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake-up through EN being set high for longer than t_{MODE_CHANGE}.

9.4.4.1 Wake-Up Request (RXD)

When the TLIN1039-Q1 encounters a wake-up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake-up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.4.2 Mode Transitions

When the TLIN1039-Q1 is transitioning from normal to sleep or standby modes the device needs the time t_{MODE_CHANGE} to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs t_{NOMINT}.

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10 Application and Implementation

Note

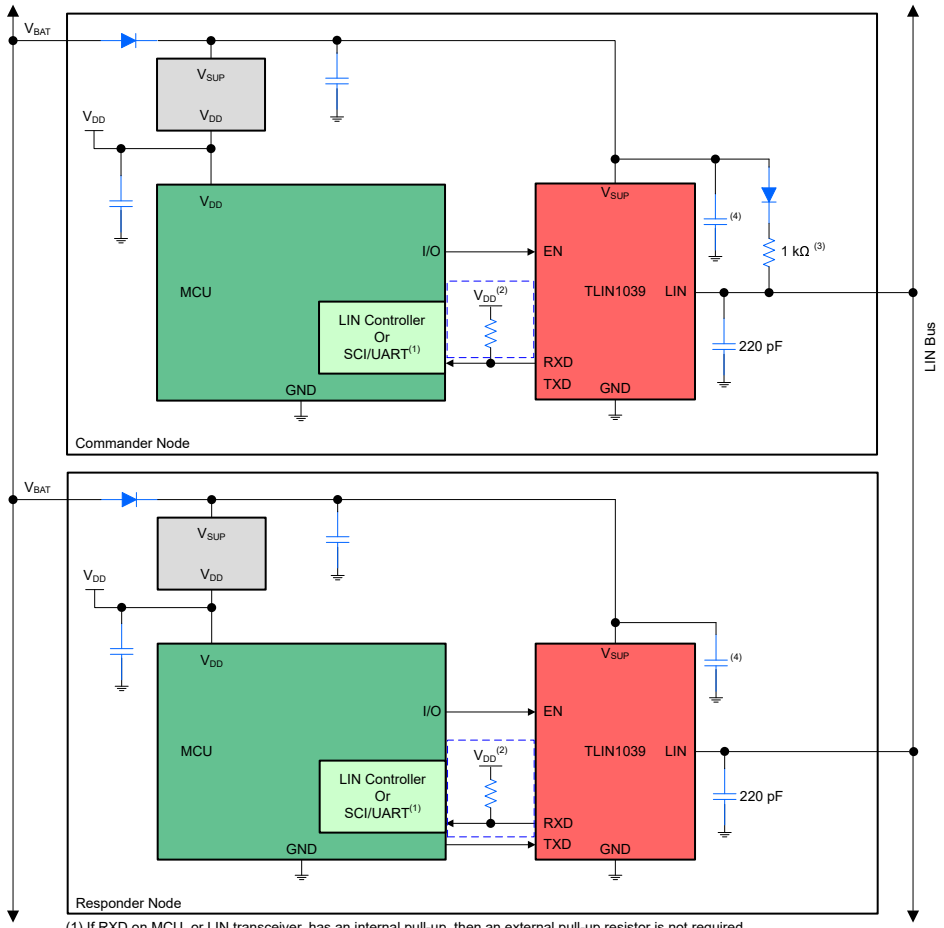
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10.1 Application Information

The TLIN1039-Q1 can be used as both a responder node device and a commander node device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

10.2 Typical Application

The device integrates a 45 kΩ pull-up resistor and series diode for responder node applications. For commander applications an external 1 kΩ pull-up resistor with series blocking diode can be used. 図 10-1 shows the device being used in both commander node and responder node applications.



(1) If RXD on MCU, or LIN transceiver, has an internal pull-up, then an external pull-up resistor is not required.
(2) If RXD on MCU, or LIN transceiver, does not have an internal pull-up, then an external pull-up resistor is required.
(3) Commander node applications require an external 1 kΩ pull-up resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

図 10-1. Typical LIN Bus

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN1039-Q1 to be used with 3.3 V and 5 V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The external pull-up resistor value should be between 1

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kΩ to 10 kΩ, depending on supply used (See I_{OL} in electrical characteristics). The V_{SUP} pin of the device should be decoupled with a 100 nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN1039-Q1 in systems which are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin, for indication of wake-up request, until t_{MODE_CHANGE} has been met. This is shown in 図 8-14

10.2.2.2 Standby Mode Application Note

If the TLIN1039-Q1 detects an under voltage on V_{SUP}, the RXD pin transitions low and signals to the software that the TLIN1039-Q1 is in standby mode. The transceiver should be returned to sleep mode for the lowest power state.

10.2.3 Application Curves

図 10-2 and 図 10-3 show the propagation delay from the TXD pin to the LIN pin for the dominant to recessive and recessive to dominant edges. The device was configured as a commander node with an external pull-up resistor (1 kΩ) and 680 pF bus capacitance.

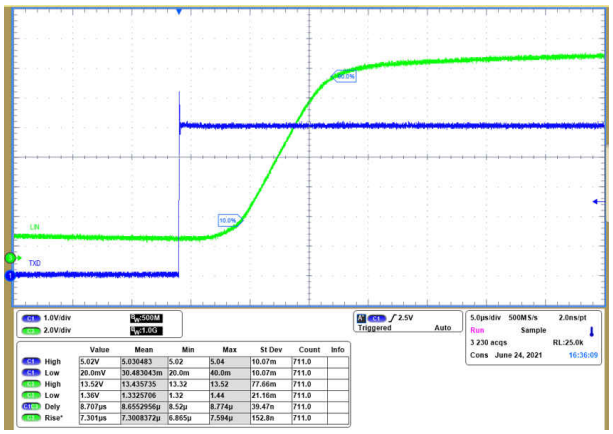


図 10-2. Dominant to Recessive Propagation Delay

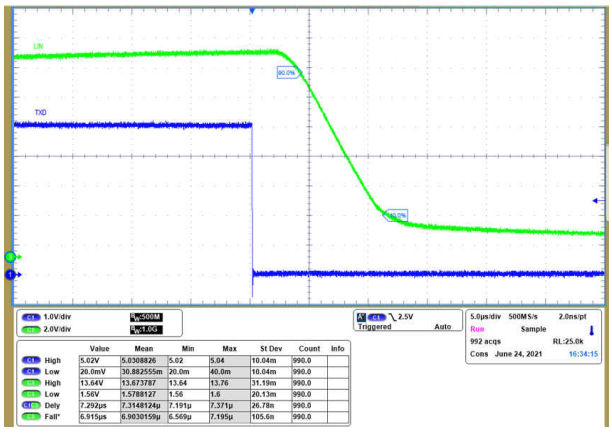


図 10-3. Recessive to Dominant Propagation Delay

11 Power Supply Recommendations

The was designed to operate directly from a car battery, or any other DC supply ranging from 4.5 V to 36 V. The V_{SUP} pin of the transceiver should be decoupled with a 100-nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

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12 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1 (RXD):** The pin is an open-drain output and requires an external pull-up resistor in the range of 1 kΩ to 10 kΩ to function properly. Note that the minimum value depends on the logic supply used. See I_{OL} in electrical specifications. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low-power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (NC):** Not Connected.
- **Pin 4 (TXD):** The TXD pin is used to transmit the input signal from the microcontroller. To prevent an over-voltage on this pin, a series resistor can be placed to limit the input current to the device. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For responder mode applications a 220 pF capacitor to ground is implemented. For commander mode applications, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See Typical LIN Bus.
- **Pin 7 (V_{SUP}):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 8 (NC):** Not Connected.

Note

All ground and power connections should be made as short as possible, and use at least two vias to minimize the total loop inductance.

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12.2 Layout Example

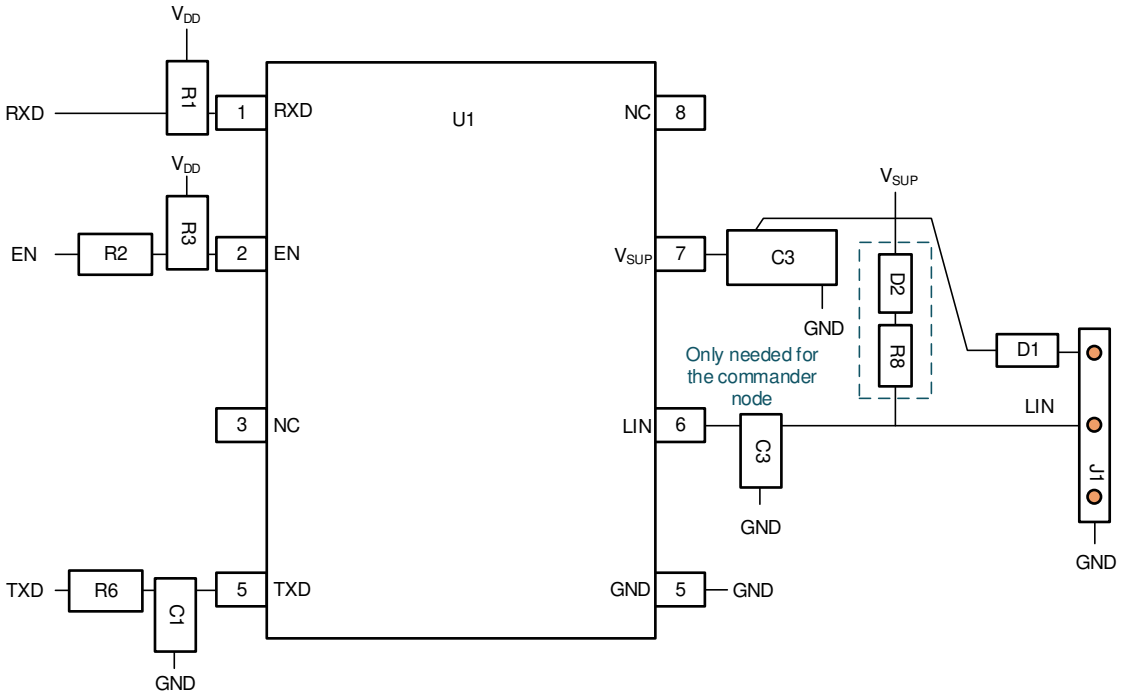


図 12-1. Layout Example

13 Device and Documentation Support

13.1 Related Documentation

For related documentation see the following:

- LIN Standards:
  - ISO/DIS 17987-1.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
  - ISO/DIS 17987-4.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
  - SAE J2602-1: LIN Network for Vehicle Applications
  - LIN Specifications LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A
- EMC requirements:
  - SAE J2962-1: Communication Transceivers Qualification Requirements - LIN
  - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
  - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
  - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
  - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
  - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
  - IEC 61000-4-2
  - IEC 61967-4
  - CISPR25
- Conformance Test requirements:
  - ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
  - SAE J2602-2: LIN Network for Vehicle Applications Conformance Test

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13.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated transceiver. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN1039DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JIF
TLIN1039DDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JIF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

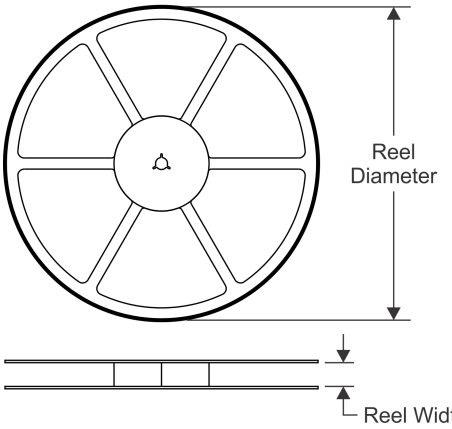
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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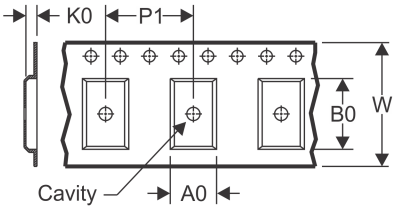
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

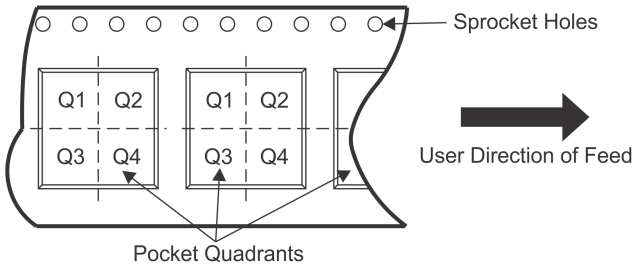


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

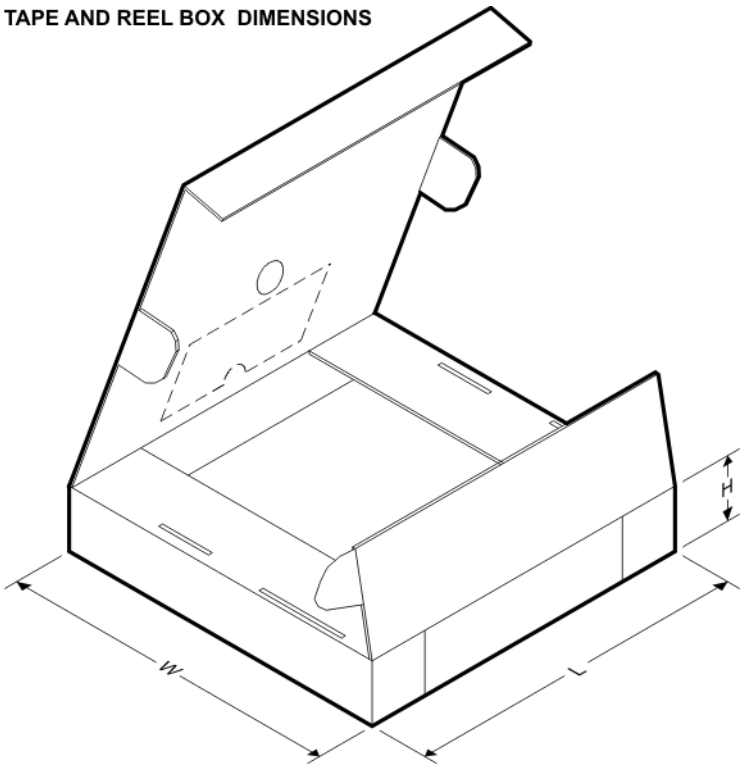
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN1039DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

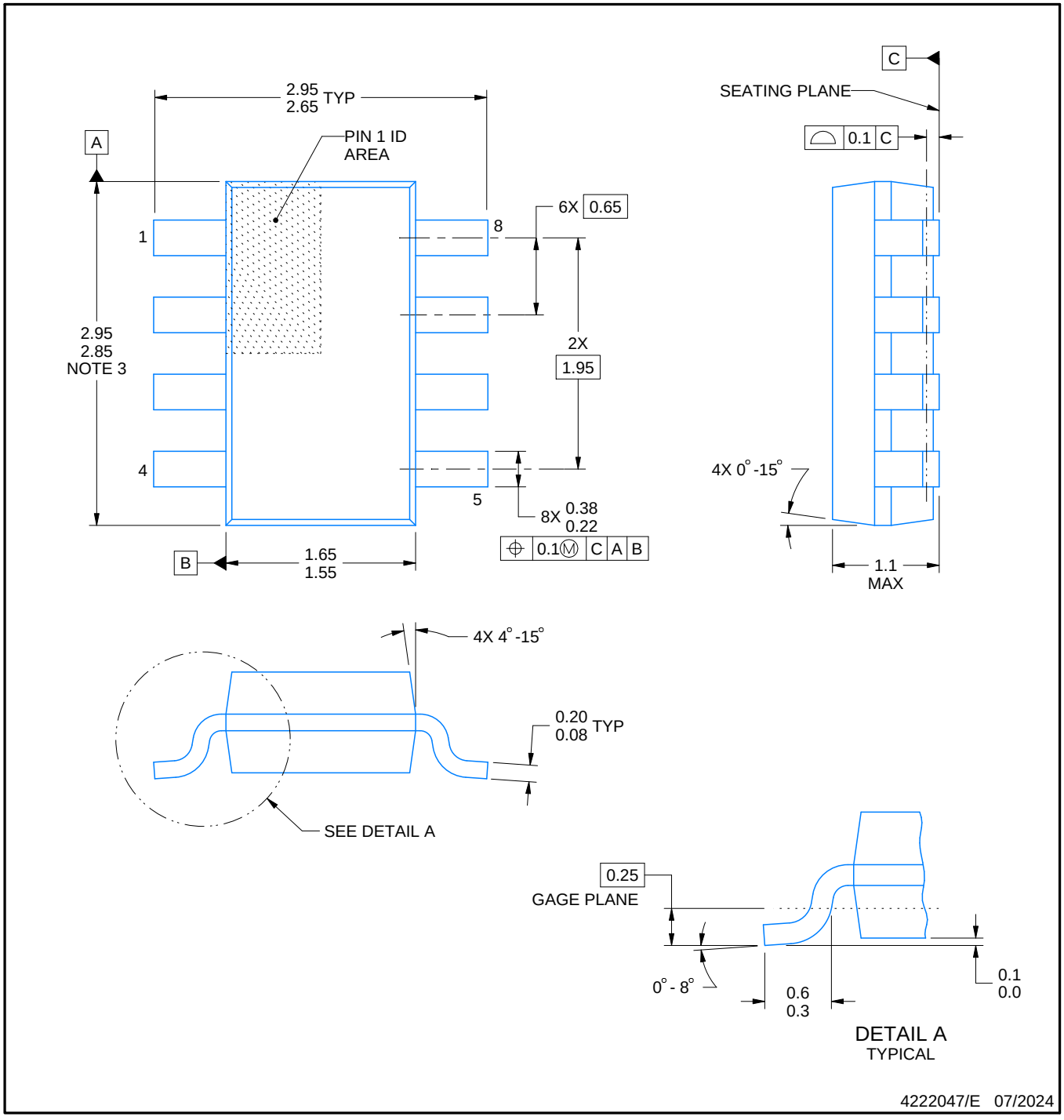
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN1039DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

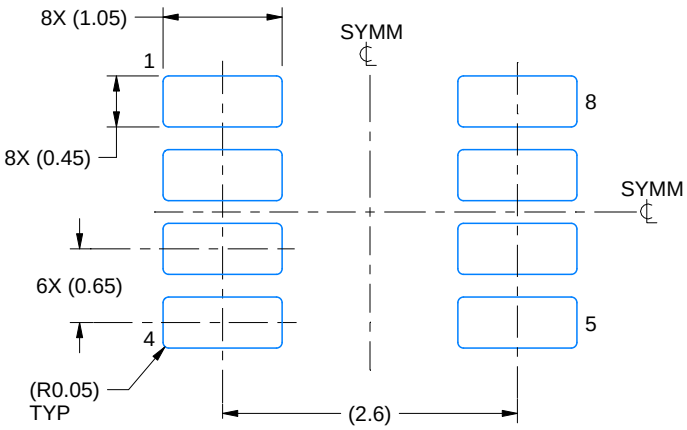
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

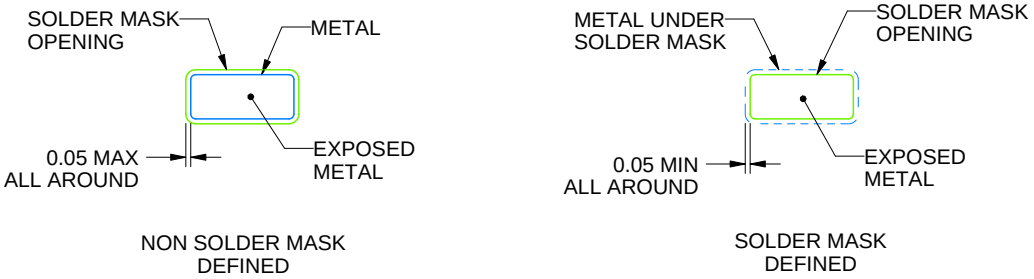


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

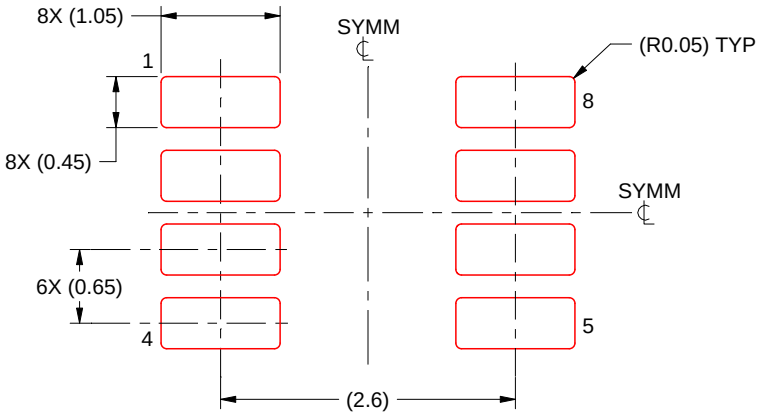
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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