TLV1117LV 正側固定電圧出力の 1A 低ドロップアウト・レギュレータ

1 特長

- 標準精度:1.5%
- 低 I_Q:100μA 以下
  - 標準の 1117 デバイスに比べて 1/500 の低い値
- V_{IN}:2V～5.5V
  - V_{IN} の絶対最大定格:6V
- 出力電流が 0mA 時でも安定動作
- 低いドロップアウト:V_{OUT} = 3.3V で 1A 出力時に 455mV
- 高 PSRR:1kHz 時に 65dB
- 最小電流制限規定値:1.1A
- コスト効率の優れたセラミック・コンデンサ使用時に安定動作:
  - ESR 0Ω に対応
- 温度範囲:-40℃～+125℃
- サーマル・シャットダウン機能と過電流保護機能
- アップグレードされた機能を持つドロップイン代替品については、TLV761 を参照してください
- SOT-223 パッケージで供給
  - 利用可能な電圧オプションの詳細なリストについては、このドキュメントの最後にある「メカニカル、パッケージ、および注文情報」セクションを参照してください。

2 アプリケーション

- セット・トップ・ボックス
- テレビ、モニタ
- PC 周辺機器、ノートブック、マザーボード
- モデム、その他の通信製品
- スイッチング電源のポスト・レギュレーション

3 概要

TLV1117LV 低ドロップアウト (LDO) リニア・レギュレータは、一般的な TLV1117 電圧レギュレータの低入力電圧版です。

TLV1117LV は非常に低消費電力のデバイスで、従来の 1117 電圧レギュレータと比べて静止時に消費する電流は 1/500 です。この設計のため本デバイスは、非常に低いスタンバイ電流を必要とするアプリケーションに適しています。また、TLV1117LV LDO は、負荷電流が 0mA の状態で安定します。最小の負荷要件はないため、通常動作時に 1A という大きな負荷電流に対応するだけでなく、スタンバイ時の非常に小さい負荷に対して、レギュレータから電力を供給する必要があるアプリケーション用としても、有効な選択肢となります。TLV1117LV はライン過渡特性と負荷過渡特性が優れており、その結果、要求される負荷電流が 1mA 未満から 500 mA を超える範囲で変化するような場合でも、出力電圧振幅のアンダーシュートやオーバーシュートは非常に小さく抑えられます。

高精度のバンドギャップとエラー・アンプにより、1.5% の精度を実現しています。本デバイスの電源電圧変動除去比 (PSRR) は非常に高いので、スイッチング・レギュレータの後段に配置するポスト・レギュレーションにも使用できます。他の有用な特徴としては、低出力ノイズ、低ドロップアウト電圧などが挙げられます。

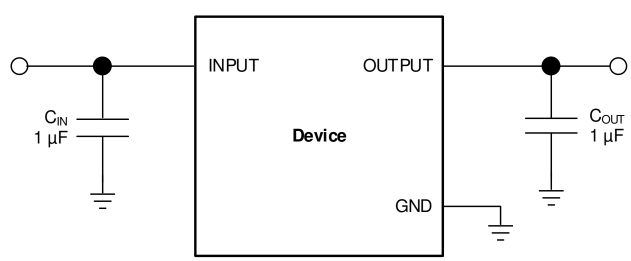
また、等価直列抵抗 (ESR) 0Ω のコンデンサでも安定するよう内部的に補償されています。これらの主な長所が、コスト効率の優れた小型のセラミック・コンデンサの使用を可能にしています。必要に応じて、コスト効率が優れていて、バイアス電圧が高く温度ディレーティングが大きいタイプのコンデンサを使用することもできます。

TLV1117LV は SOT-223 パッケージで供給されます。

パッケージ情報

部品番号	パッケージ[1]	本体サイズ (公称)
TLV1117LV	DCY (SOT-223、4)	6.50mm × 3.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (January 2015) to Revision C (January 2023)	Page
• 「特長」セクションにドロップイン代替に関する箇条書きを追加	1

Changes from Revision A (September 2011) to Revision B (January 2015)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 表紙の図を差し替え	1
• Deleted *Dissipation Ratings* table	4

5 Pin Configuration and Functions

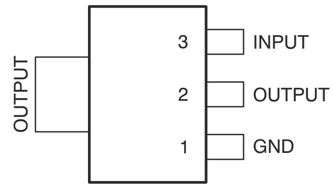


図 5-1. DCY Package, 4 Pins (SOT-223) (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	3	I	Input pin. See the *Input and Output Capacitor Requirements* section for more details.
OUT	2, Tab	O	Regulated output voltage pin. See the *Input and Output Capacitor Requirements* section for more details.
GND	1	—	Ground pin.

6 Specifications

6.1 Absolute Maximum Ratings

at T_J = 25°C (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{OUT}	–0.3	6	V
Current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
V_{OUT}	Output voltage	0		5.5	V
I_{OUT}	Output current	0		1	A

6.4 Thermal Information

THERMAL METRIC(1)		TLV1117LV DCY (SOT-223) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-board thermal resistance	12	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

at $V_{IN} = V_{OUT(nom)} + 1.5$ V; I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2		5.5	V
V_{OUT}	DC output accuracy	V_{OUT} > 2 V	–1.5%		1.5%	
		1.5 V ≤ V_{OUT} < 2 V	–2%		2%	
		1.2 V ≤ V_{OUT} < 1.5 V	–40		40	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 1 A		1	35	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} < 3.3 V, I_{OUT} = 200 mA		115		mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} < 3.3 V, I_{OUT} = 500 mA		285		mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} < 3.3 V, I_{OUT} = 800 mA		455		mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} < 3.3 V, I_{OUT} = 1 A		570	800	mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} ≥ 3.3 V, I_{OUT} = 200 mA		90		mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} ≥ 3.3 V, I_{OUT} = 500 mA		230		mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} ≥ 3.3 V, I_{OUT} = 800 mA		365		mV
		V_{IN} = 0.98 × $V_{OUT(nom)}$, V_{OUT} ≥ 3.3 V, I_{OUT} = 1 A		455	700	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	1.1			A
I_Q	Quiescent current	I_{OUT} = 0 mA		50	100	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA, f = 100 Hz		65		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 2.8 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA		60		μV_{RMS}
t_{STR}	Start-up time(2)	C_{OUT} = 1.0 µF, I_{OUT} = 1 A		100		µs
UVLO	Undervoltage lockout	V_{IN} rising		1.95		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		°C
T_J	Operating junction temperature		–40		125	°C

(1) V_{DO} is measured for devices with $V_{OUT(nom)}$ = 2.5 V so that V_{IN} = 2.45 V.
(2) Start-up time = time from when V_{IN} asserts to when output is sustained at a value greater than or equal to 0.98 × $V_{OUT(nom)}$.

6.6 Typical Characteristics

at $V_{IN} = V_{OUT(nom)} + 1.5\ V$, $I_{OUT} = 10\ mA$, $C_{OUT} = 1.0\ \mu F$, and $T_A = 25°C$ (unless otherwise noted)

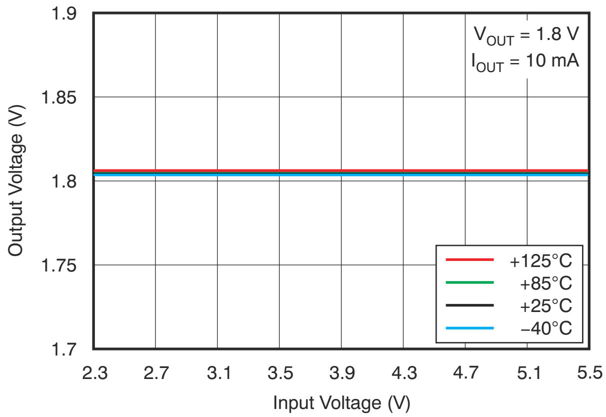


図 6-1. Line Regulation

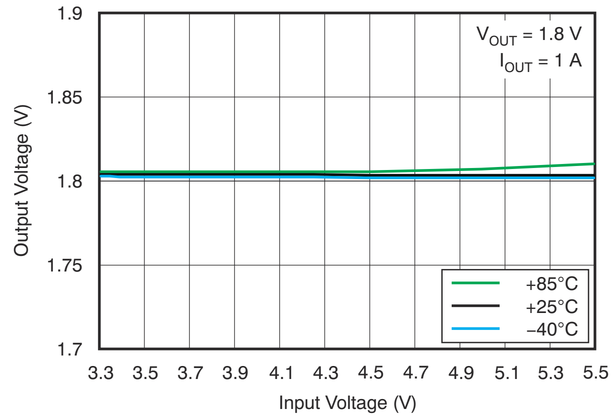


図 6-2. Line Regulation

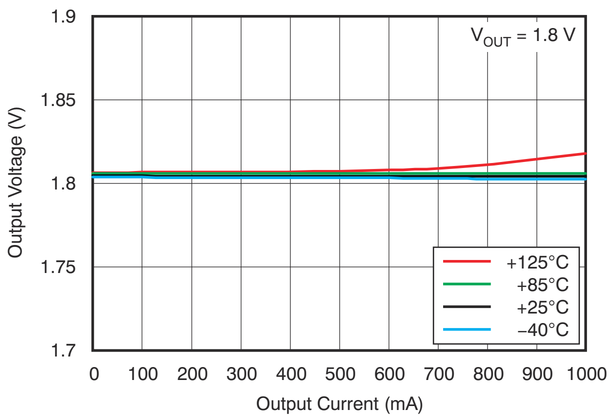


図 6-3. Load Regulation

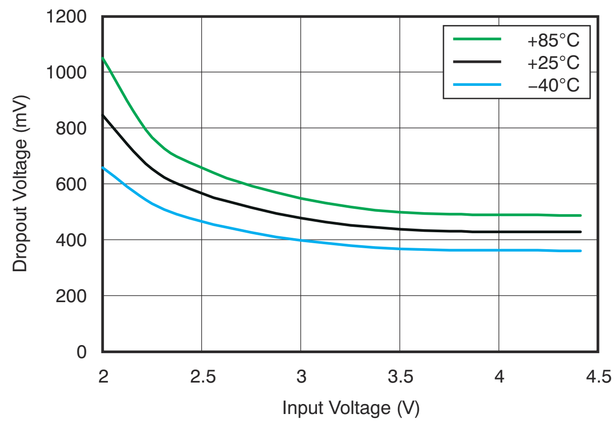


図 6-4. Dropout Voltage vs Input Voltage

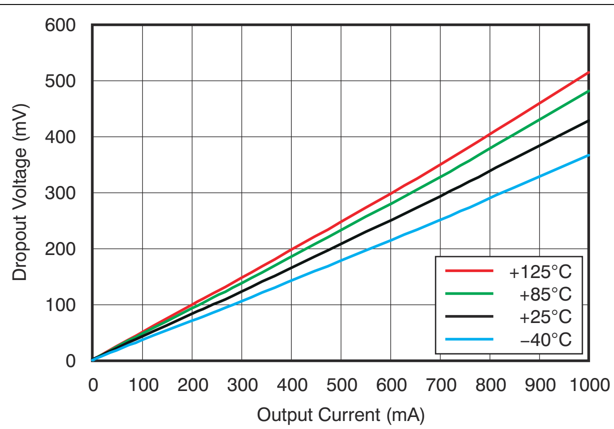


図 6-5. Dropout Voltage vs Output Current

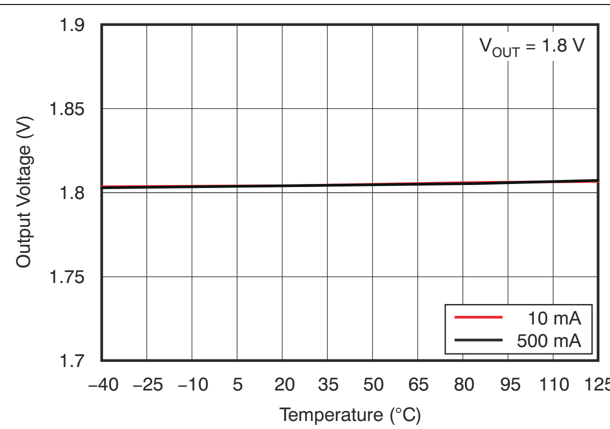


図 6-6. Output Voltage vs Temperature

6.6 Typical Characteristics (continued)

at $V_{IN} = V_{OUT(nom)}$ + 1.5 V, I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C (unless otherwise noted)

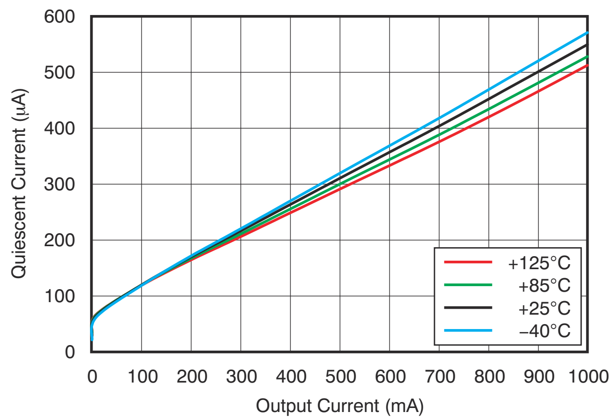


図 6-7. Quiescent Current vs Load

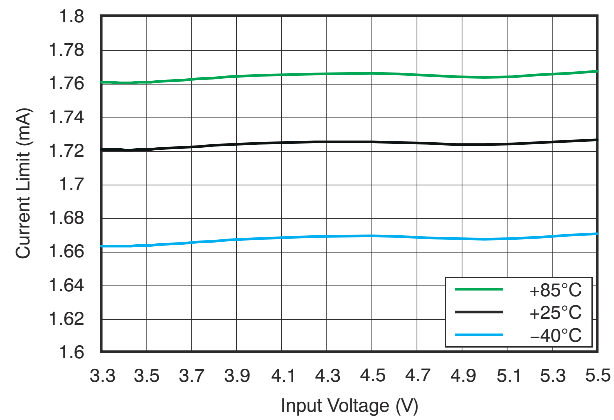


図 6-8. Current Limit vs Input Voltage

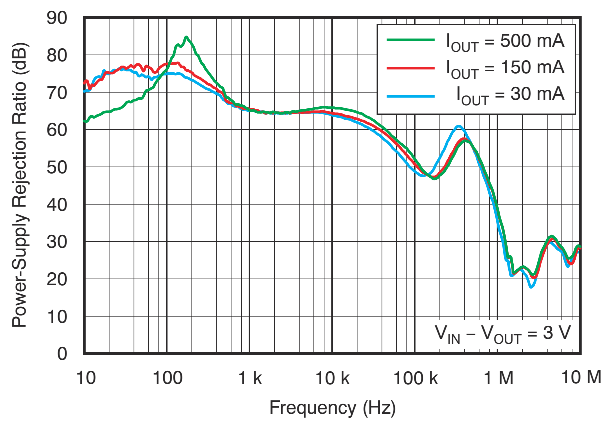


図 6-9. Power-Supply Rejection Ratio vs Frequency

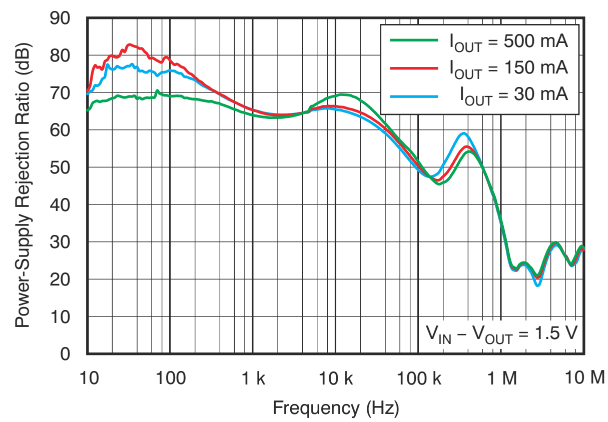


図 6-10. Power-Supply Rejection Ratio vs Frequency

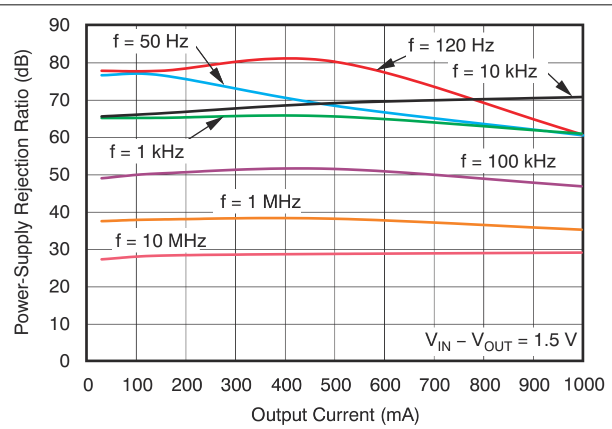


図 6-11. Power-Supply Rejection Ratio vs Output Current

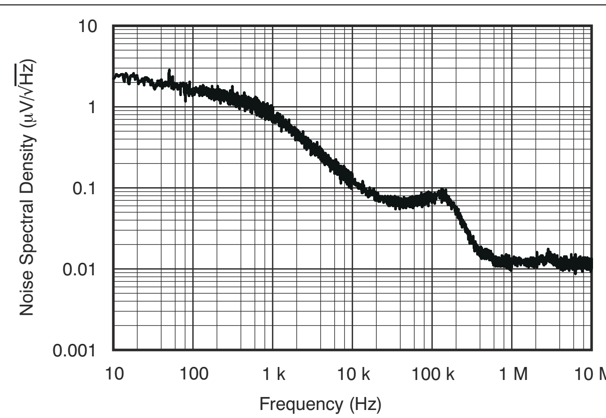
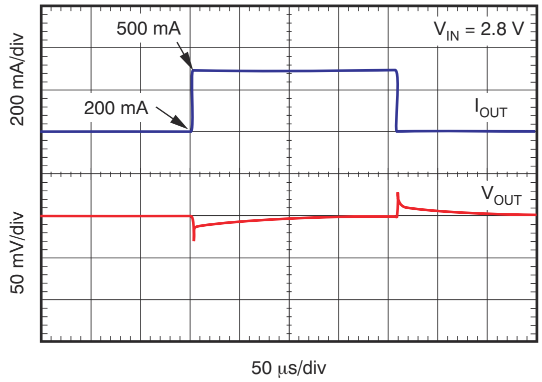


図 6-12. Spectral Noise Density vs Frequency

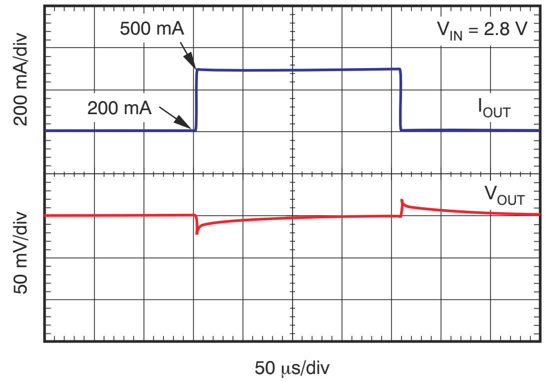
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(nom)}$ + 1.5 V, I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C (unless otherwise noted)



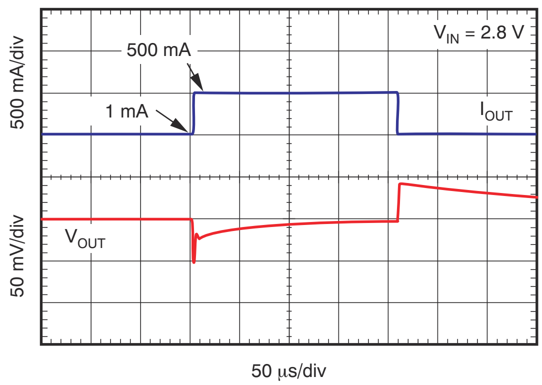
C_{OUT} = 1 µF

図 6-13. Load Transient Response 200 mA to 500 mA



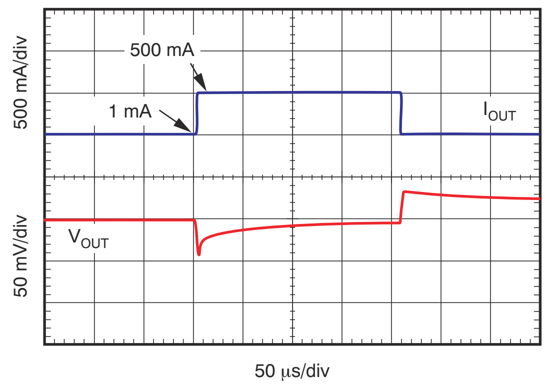
C_{OUT} = 10 µF

図 6-14. Load Transient Response 200 mA to 500 mA



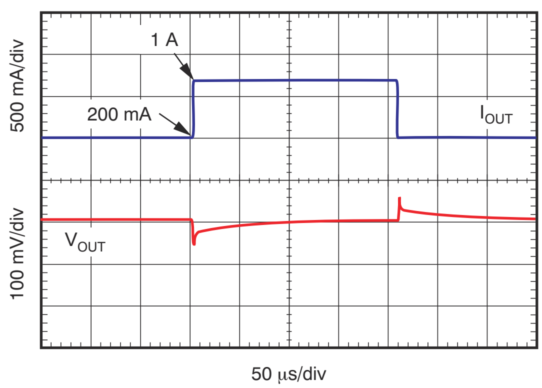
C_{OUT} = 1 µF

図 6-15. Load Transient Response 1 mA to 500 mA



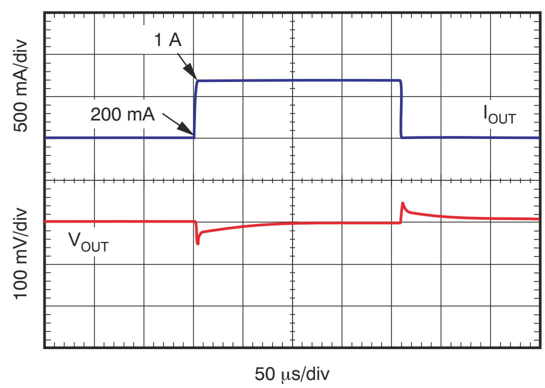
C_{OUT} = 10 µF

図 6-16. Load Transient Response 1 mA to 500 mA



C_{OUT} = 1 µF

図 6-17. Load Transient Response 200 mA to 1 A

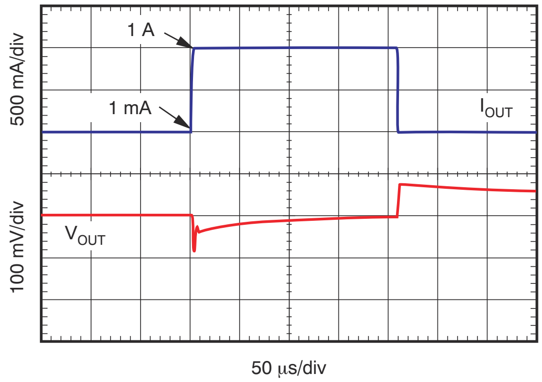


C_{OUT} = 10 µF

図 6-18. Load Transient Response 200 mA to 1 A

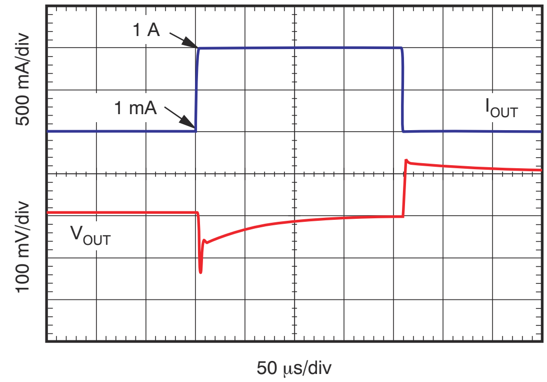
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(nom)}$ + 1.5 V, I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C (unless otherwise noted)



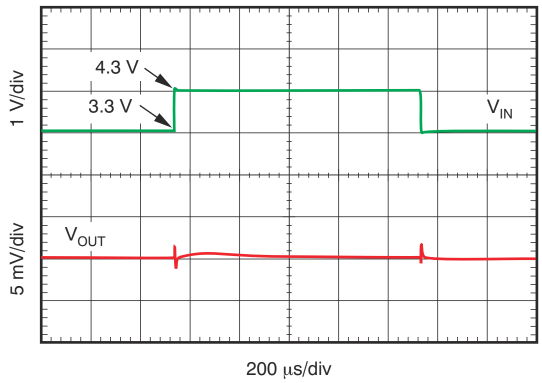
C_{OUT} = 1 µF

図 6-19. Load Transient Response 1 mA to 1 A



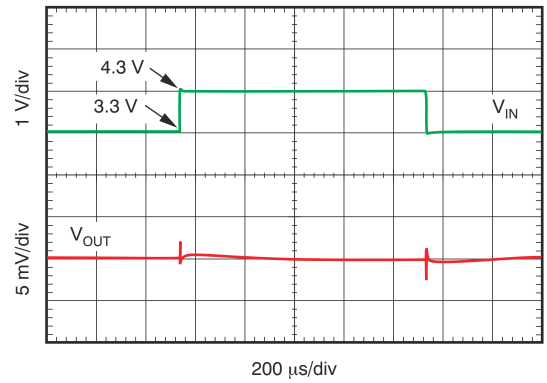
C_{OUT} = 10 µF

図 6-20. Load Transient Response 1 mA to 1 A



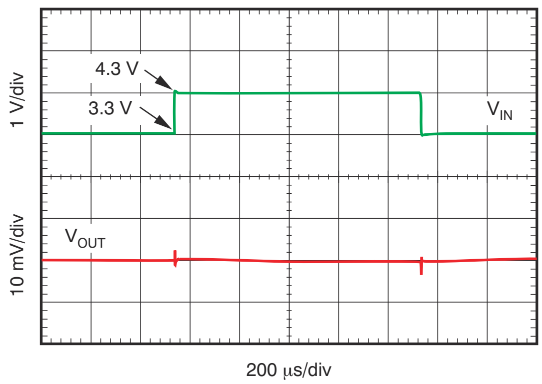
V_{OUT} = 1.8 V, I_{OUT} = 10 mA

図 6-21. Line Transient Response



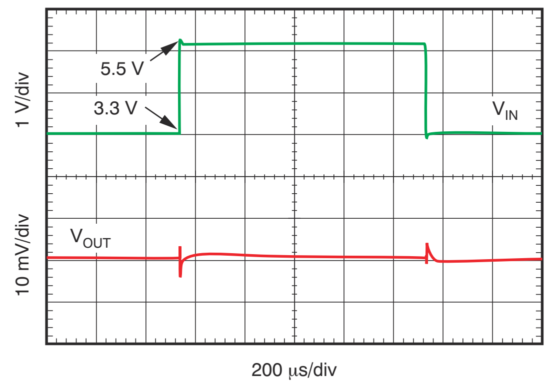
V_{OUT} = 1.8 V, I_{OUT} = 500 mA

図 6-22. Line Transient Response



V_{OUT} = 1.8 V, I_{OUT} = 1 A

図 6-23. Line Transient Response

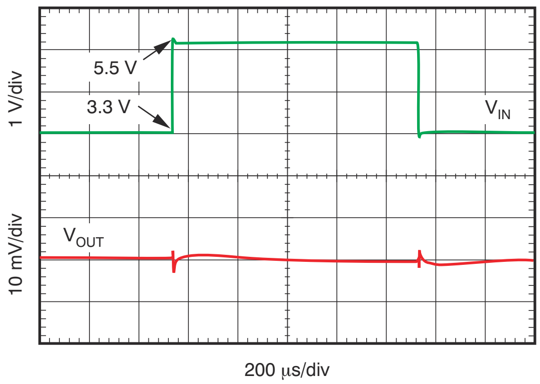


V_{OUT} = 1.8 V, I_{OUT} = 10 mA

図 6-24. Line Transient Response

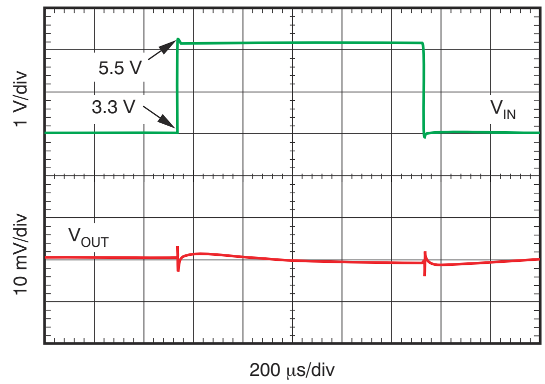
6.6 Typical Characteristics (continued)

at $V_{IN} = V_{OUT(nom)}$ + 1.5 V, I_{OUT} = 10 mA, C_{OUT} = 1.0 µF, and T_A = 25°C (unless otherwise noted)



V_{OUT} = 1.8 V, I_{OUT} = 500 mA

図 6-25. Line Transient Response



V_{OUT} = 1.8 V, I_{OUT} = 1 A

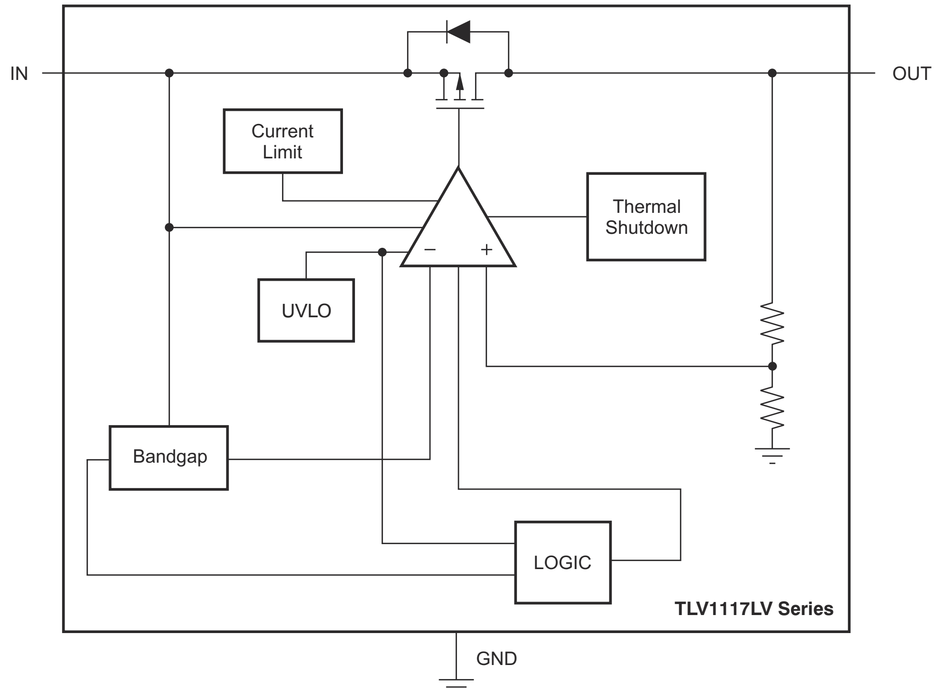
図 6-26. Line Transient Response

7 Detailed Description

7.1 Overview

The TLV1117LV is a low quiescent current, high PSRR LDO capable of handling up to 1 A of load current. This device features an integrated current limit, thermal shutdown, band-gap reference, and undervoltage lockout (UVLO) circuit blocks.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TLV1117LV internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and can be calculated by the formula: $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Protection* section for more details.

The PMOS pass transistor in the TLV1117LV has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.2 Dropout Voltage

The TLV1117LV uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass transistor. V_{DO} scales approximately with output current because the PMOS transistor behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when $(V_{IN} – V_{OUT})$ approaches dropout.

7.3.3 Undervoltage Lockout

The TLV1117LV uses an undervoltage lockout (UVLO) circuit to keep the output shut off until internal circuitry is operating properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage
- The output current is less than the current limit
- The device die temperature is lower than the thermal shutdown temperature

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

表 7-1 shows the conditions that lead to the different modes of operation.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV1117LV is a low quiescent current linear regulator designed for high current applications. Unlike typical high current linear regulators, the TLV1117LV consumes significantly less quiescent current. This device delivers excellent line and load transient performance. The device is low noise, and exhibits a very good PSRR. As a result, this device is designed for high current applications that require very sensitive power-supply rails.

This regulators offer both current limit and thermal protection. The operating junction temperature range of the device is –40°C to +125°C.

8.2 Typical Application

図 8-1 shows a typical application circuit.

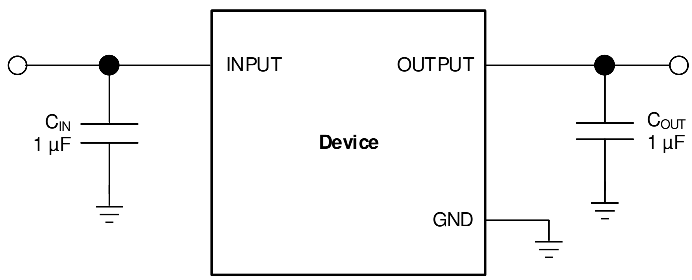


図 8-1. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5 V to 3.3 V
Output voltage	1.8 V
Output current	500 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

For stability, 1.0-µF ceramic capacitors are required at the output. Higher-valued capacitors improve transient performance. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. Unlike traditional linear regulators that need a minimum ESR for stability, the TLV1117LV is specified to be stable with no ESR. Therefore, cost-effective ceramic capacitors can be used with this device. Effective output capacitance that takes bias, temperature, and aging effects into consideration must be greater than 0.5 µF to ensure stability of the device.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1.0-µF, low-ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated, or if the device is not located physically close to the power source. If source impedance is greater than 2 Ω, a 0.1-µF input capacitor can also be necessary to ensure stability.

8.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude.

8.2.3 Application Curves

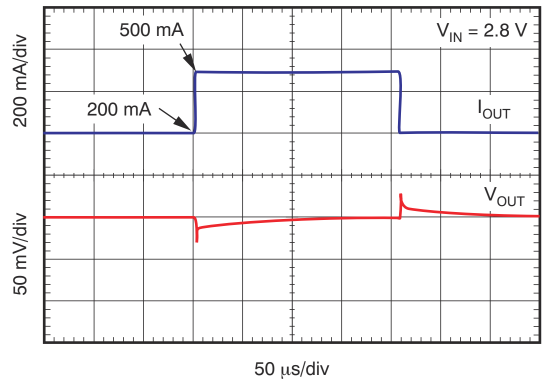


図 8-2. Load Transient Response 200 mA to 500 mA, C_{OUT} = 1 µF

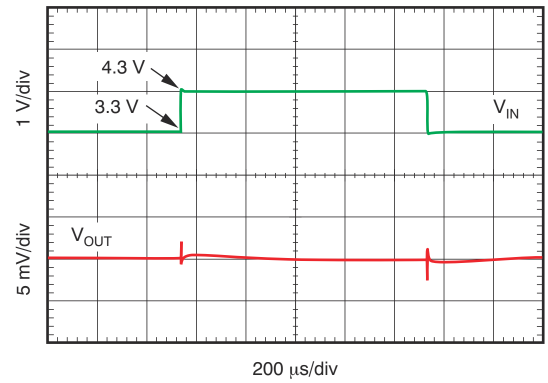


図 8-3. Line Transient Response V_{OUT} = 1.8 V, I_{OUT} = 500 mA

8.3 Best Design Practices

Place input and output capacitors as close to the device as possible.

Use a ceramic output capacitor.

Do not use an electrolytic output capacitor.

Do not exceed the device absolute maximum ratings.

8.4 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the TLV1117LV. Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during start-up or load transient events.

8.5 Layout

8.5.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve characteristic AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. Higher value ESR capacitors can degrade PSRR performance.

8.5.1.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV1117LV is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TLV1117LV into thermal shutdown degrades device reliability.

8.5.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in 式 1:

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \tag{1}$$

8.5.2 Layout Example

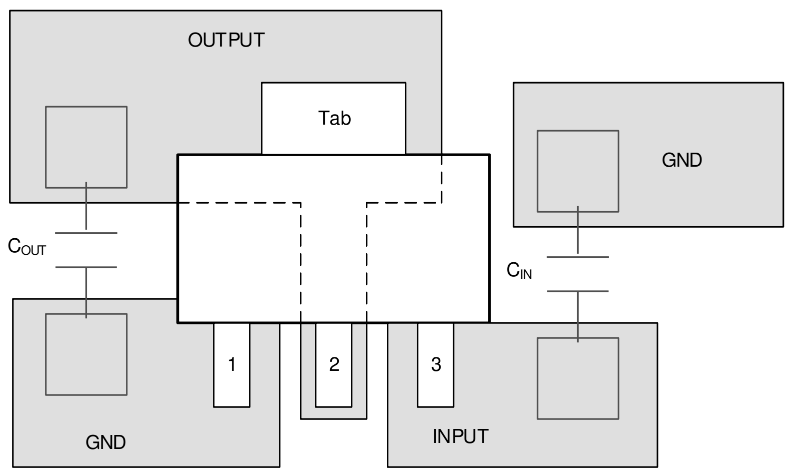


図 8-4. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV1117LV. The TLV1117LV33EVM-714 evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV1117LV is available through the product folders under *Tools & Software*.

9.1.2 Device Nomenclature

表 9-1. Available Options(1)

PRODUCT	V_{OUT}
TLV1117LV**xxyyyz**	**xx** is the nominal output voltage (for example 33 = 3.3 V). **yyy** is the package designator. **z** is the package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV1117LVxxEVM-714 Evaluation Module* user's guide

9.3 ドキュメントの更新通知を受け取る方法

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1117LV12DCYR	NRND	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SI
TLV1117LV12DCYR.B	NRND	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SI
TLV1117LV15DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VR
TLV1117LV15DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VR
TLV1117LV15DCYT	Obsolete	Production	SOT-223 (DCY) | 4	-	-	Call TI	Call TI	-40 to 125	VR
TLV1117LV18DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH
TLV1117LV18DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH
TLV1117LV18DCYT	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH
TLV1117LV18DCYT.B	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SH
TLV1117LV25DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VS
TLV1117LV25DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VS
TLV1117LV25DCYT	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VS
TLV1117LV25DCYT.B	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VS
TLV1117LV28DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VT
TLV1117LV28DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VT
TLV1117LV28DCYT	Obsolete	Production	SOT-223 (DCY) | 4	-	-	Call TI	Call TI	-40 to 125	VT
TLV1117LV30DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VU
TLV1117LV30DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VU
TLV1117LV30DCYT	Obsolete	Production	SOT-223 (DCY) | 4	-	-	Call TI	Call TI	-40 to 125	VU
TLV1117LV33DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TJ
TLV1117LV33DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TJ
TLV1117LV33DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[(4)] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[(5)] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[(6)] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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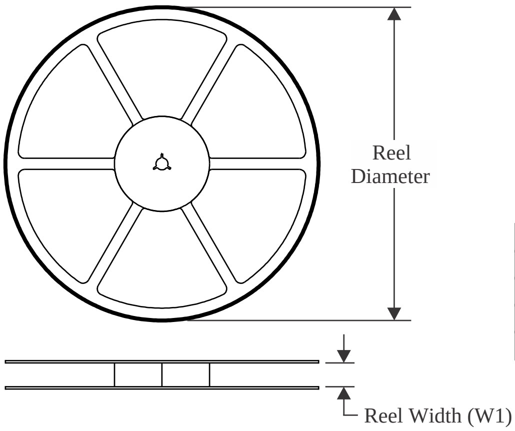
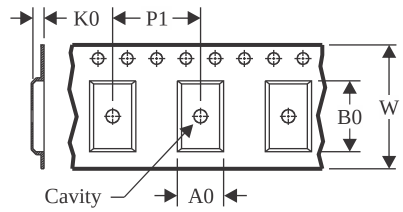
TAPE AND REEL INFORMATION

REEL DIMENSIONS

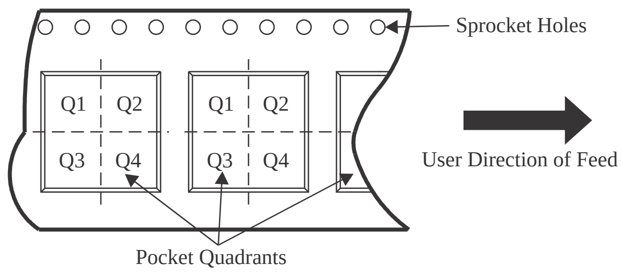


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

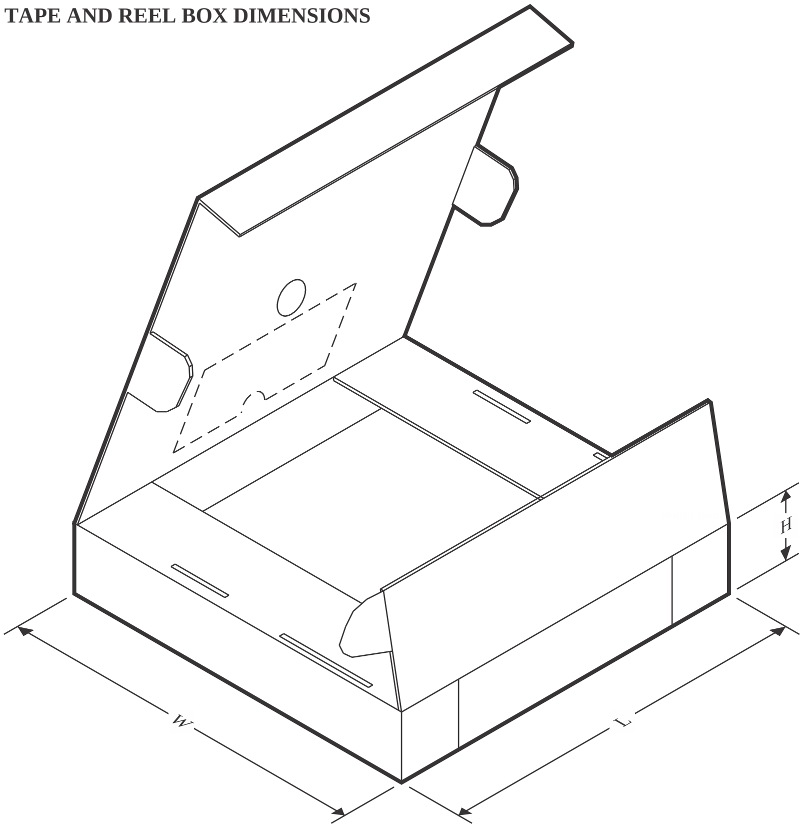
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117LV12DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV15DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV18DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV18DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV25DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV25DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV28DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV30DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117LV33DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

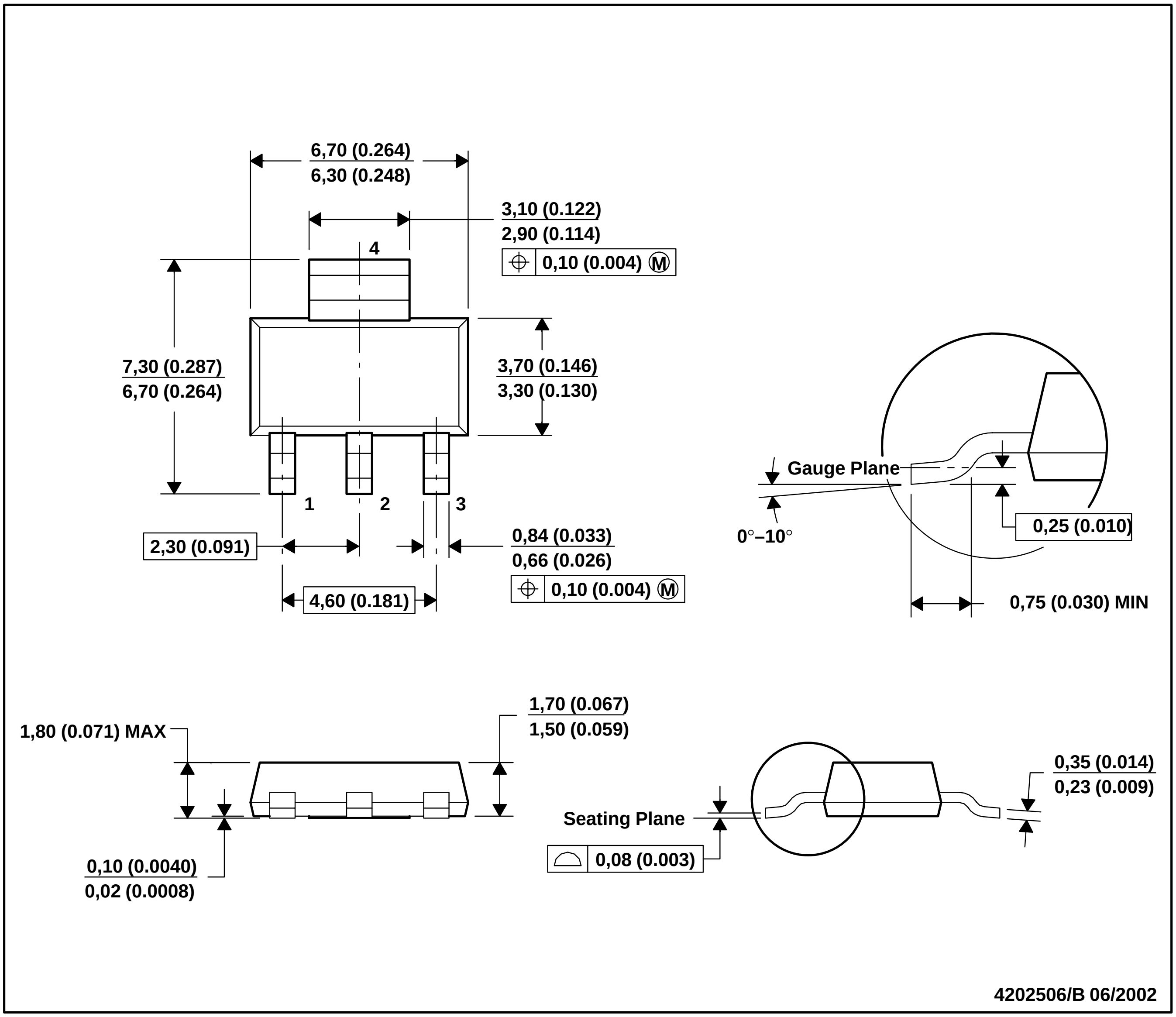
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

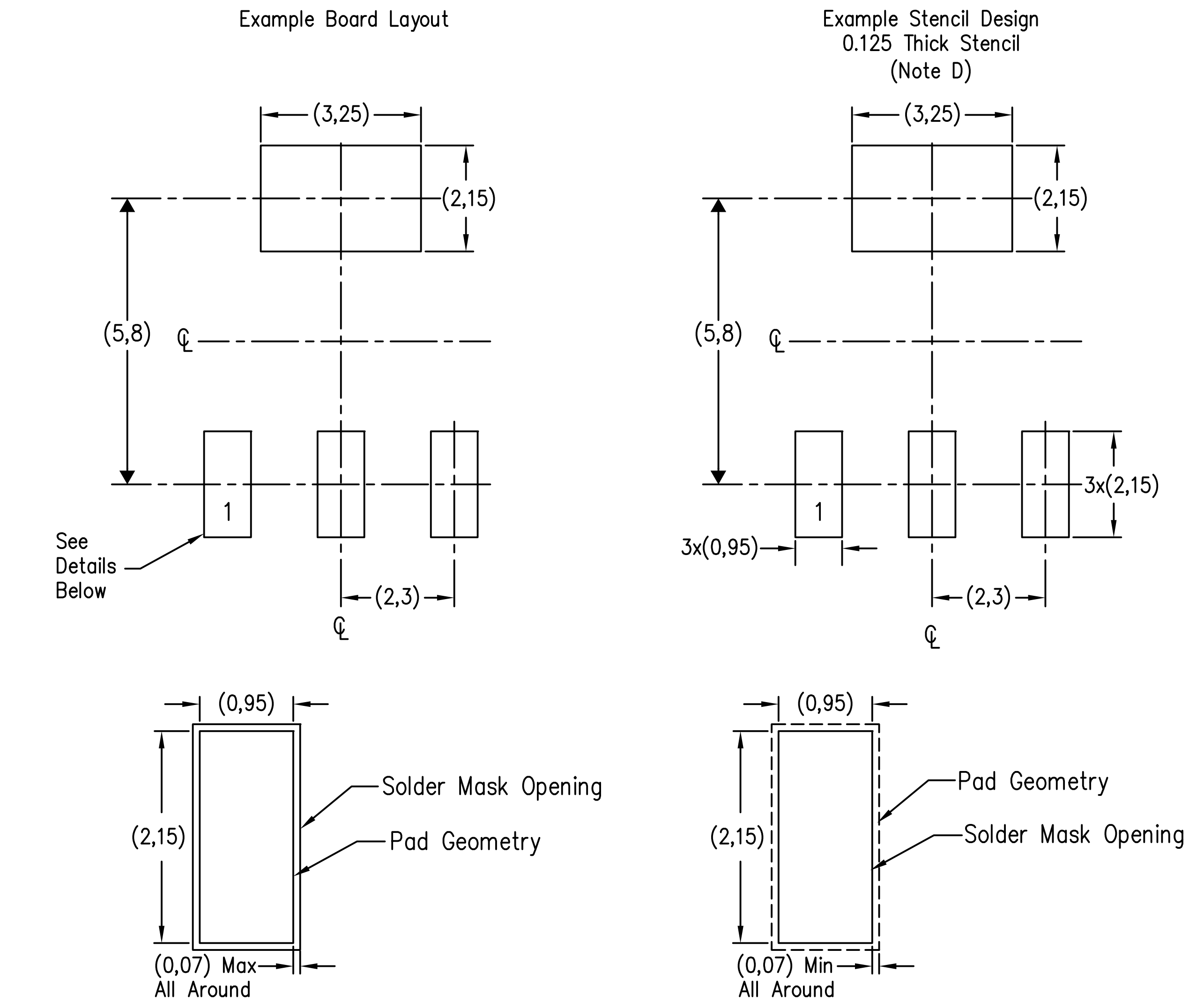
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117LV12DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV15DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV18DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV18DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV25DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV25DCYT	SOT-223	DCY	4	250	340.0	340.0	38.0
TLV1117LV28DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV30DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117LV33DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



Example, non–solder mask defined pad.
(Preferred)

Example, solder mask defined pad.

4210278/C 07/13

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

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