TLV183x および TLV184x 40V 高速コンパレータ ファミリ

1 特長

- 幅広い電源電圧範囲:2.7V～40V
- 伝搬遅延時間:65ns
- 低い消費電流:75µA (チャネルあたり)
- レール ツー レール入力
- 低い入力オフセット電圧:500µV
- 既知の起動条件を提供するパワーオン リセット (POR)
- プッシュプル出力オプション (TLV183x)
- オープン ドレイン出力オプション (TLV184x)
- 分割電源オプション (TLV187x)
- 温度範囲:-40℃～+125℃

2 アプリケーション

- モーター ドライブ
- 電化製品
- グリッド インフラ
- ファクトリ オートメーション / 制御
- トラクション インバータ

3 概要

TLV183x および TLV184x は、最大 40V の動作電圧に対応する高速コンパレータです。このコンパレータは、プッシュプルおよびオープン ドレイン出力オプションを持つレール ツー レール入力を提供します。これらの特長と 65ns の伝搬遅延の組み合わせにより、このファミリは高速の電流検出および電圧保護のアプリケーションに最適です。

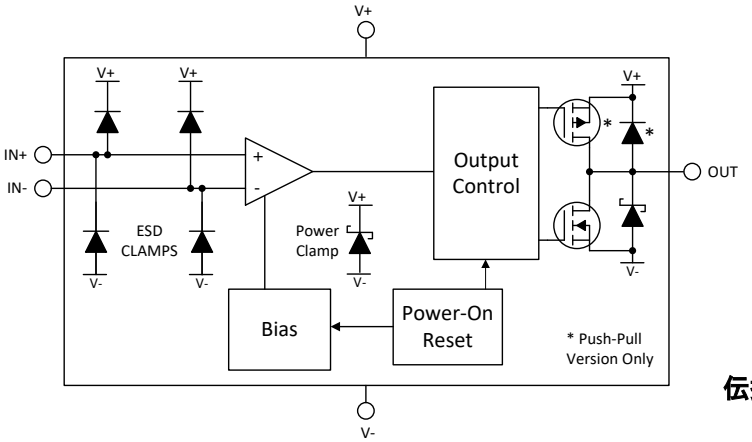
すべてのデバイスにはパワーオン リセット (POR) 機能があり、最小電源電圧に達するまで出力が既知の状態になることを保証します。この電圧に達すると、出力が入力に応答するため、システムの電源オンおよび電源オフ時に誤った出力が発生するのを防止できます。

コンパレータにはプッシュプル出力段があり、立ち上がりと立ち下がりの出力応答に対称性が求められるアプリケーション向けに設計されています。TLV184x コンパレータにはオープン ドレイン出力段があるため、レベル遷移に適しています。

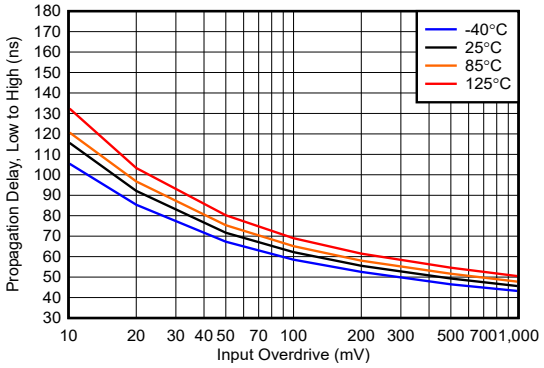
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TLV1831、TLV1841	SC-70 (5)	2.00mm × 2.00mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV1832、TLV1842	VSSOP (8)	3.00mm × 3.00mm
	TSSOP (8)	3.00mm × 4.40mm
	WSON (8)	2.00mm × 2.00mm
TLV1834、TLV1844	SOT-23 (14) (プレビュー)	4.20mm × 2.00mm
	WQFN (16) (プレビュー)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図



伝搬遅延 (Low から High) と入力オーバードライブ、12V の関係

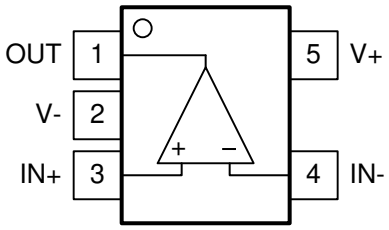
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4 Pin Configuration and Functions

Pin Configuration: TLV1831 and TLV1841



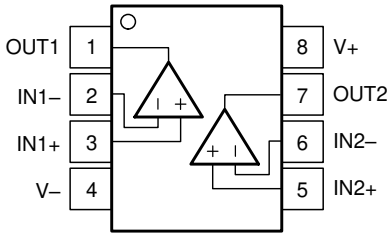
DBV, DCK Packages
SOT-23-5, SC-70-5
Top View
(Standard "north west" pinout)

表 4-1. Pin Functions: TLV1831 and TLV1841

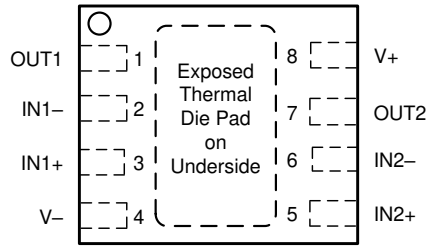
PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage

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Pin Configurations: TLV1832 and TLV1842



DGK, PW Packages
8-Pin VSSOP, TSSOP
Top View



NOTE: Connect exposed thermal pad directly to V- pin.

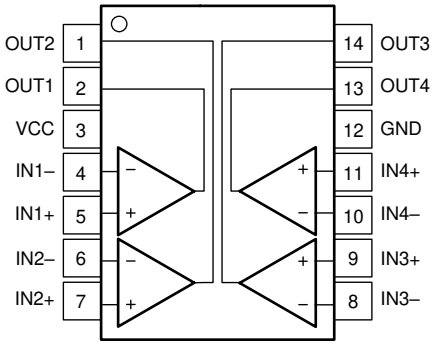
DSG Package
8-Pad WSON With Exposed Thermal Pad,
Top View

表 4-2. Pin Functions: TLV1832 and TLV1842

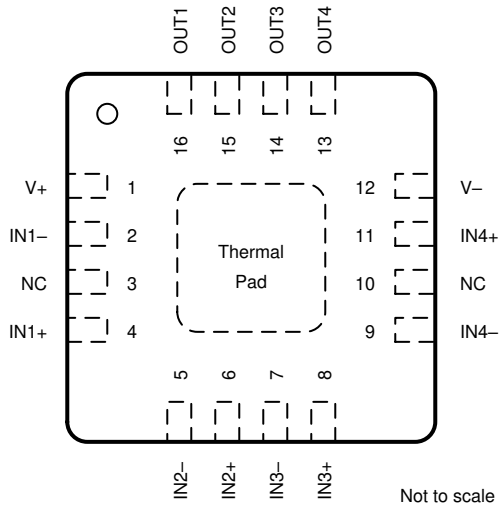
PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative supply voltage
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply voltage

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Pin Configuration and Functions: TLV1834 and TLV1844



DYY Package
14-Pin SOT-23
Top View



NOTE: Connect exposed thermal pad directly to V- pin.

RTE Package,
16-Pad WQFN With Exposed Thermal Pad
Top View

表 4-3. Pin Functions: TLV1834 and TLV1844

PIN			I/O	DESCRIPTION
NAME	SOT-23	WQFN		
OUT2	1	15	O	Output pin of the comparator 2
OUT1	2	16	O	Output pin of the comparator 1
V+	3	1	-	Positive supply voltage
IN1-	4	2	I	Inverting input pin of the comparator 1
IN1+	5	4	I	Noninverting input pin of the comparator 1
IN2-	6	5	I	Inverting input pin of the comparator 2
IN2+	7	6	I	Noninverting input pin of the comparator 2
IN3-	8	7	I	Inverting input pin of the comparator 3
IN3+	9	8	I	Noninverting input pin of the comparator 3
IN4-	10	9	I	Inverting input pin of the comparator 4
IN4+	11	11	I	Noninverting input pin of the comparator 4
V-	12	12	-	Negative supply voltage
OUT4	13	13	O	Output pin of the comparator 4
OUT3	14	14	O	Output pin of the comparator 3
NC	-	3	-	No internal connection - leave floating or GND
NC	-	10	-	No internal connection - leave floating or GND
Thermal Pad	-	PAD	-	Connect directly to V- pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	42	V
Input pins (IN+, IN–) from (V–)(2)	–0.3	(V+) + 0.3	V
Current into input pins (IN+, IN–)	–10	10	mA
Output (OUT) (Open-Drain) from (V–)(3)	–0.3	42	V
Output (OUT) (Push-Pull) from (V–)	–0.3	(V+) + 0.3	V
Output short circuit current(4)	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V–) and (V+). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as the voltage is within the –0.3V to 42V range
(4) Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		TLV183x/4x					UNIT
		DCK (SC-70)	DBV (SOT-23)	PW (TSSOP)	DSG (WSON)	DGK (VSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	216.4	183.6	157.6	110.3	151.5	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	167.9	81.1	65.7	92.8	61.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	98.1	50.4	96.5	71.0	86.1	°C/W
y_{JT}	Junction-to-top characterization parameter	75.7	18.4	8.1	5.7	5.0	°C/W
y_{JB}	Junction-to-board characterization parameter	97.1	50.0	95.2	70.8	84.8	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	62.0	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		2.7	40	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Output voltage for open drain		–0.2	40	V
Ambient temperature, T_A		–40	125	°C

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5.5 Electrical Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 12V, V_{CM} = VS/2 at TA = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C	–2.5	±0.3	2.5	mV
		T_A = –40°C to +125°C	–3.0		3.0	mV
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±1.2		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator, TLV18x1 Only	No Load, Output High T_A = 25°C TLV1831, TLV1841		75	100	µA
		No Load, Output High T_A = –40°C to +125°C TLV1831, TLV1841			105	µA
		No Load, Output Low T_A = 25°C TLV1831, TLV1841		100	135	µA
		No Load, Output Low T_A = –40°C to +125°C TLV1831, TLV1841			140	µA
I_Q	Quiescent current per comparator	No Load, Output High T_A = 25°C		75	95	µA
		No Load, Output High T_A = –40°C to +125°C			100	µA
		No Load, Output Low T_A = 25°C		95	130	µA
		No Load, Output Low T_A = –40°C to +125°C			135	µA
V_{POR}				1.9		V
INPUT BIAS CURRENT						
I_B	Input bias current (1)			500		pA
I_B	Input bias current (1) (2)	T_A = –40°C to +125°C	-5		5	nA
I_{OS}	Input offset current			10		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential			5		pF
C_{IC}	Input Capacitance, Common Mode			5		pF
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 2.7V to 40V T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA T_A = –40°C to +125°C			400	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	I_{SOURCE} = 4mA T_A = –40°C to +125°C			400	mV
I_{LKG}	Open-drain output leakage current	V_{ID} = +0.1V, V_{PULLUP} = (V+) T_A = –40°C to +125°C		3	70	nA
I_{OL}	Short-circuit current	Sinking T_A = –40°C to +125°C		30		mA
I_{OH}	Short-circuit current	Sourcing T_A = –40°C to +125°C		30		mA

(1) Please see figure for I_{BIAS} vs V_{ID} performance curve
(2) This parameter is verified by design and/or characterization and is not tested in production.

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5.6 Switching Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 12V, V_{CM} = VS/2, C_L = 15pF at TA = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output						
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 10mV, V_{UD} = 100mV V_{PU} = 5V and R_{PU} = 10k (open-drain output only)		110		ns
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 100mV, V_{UD} = 100mV V_{PU} = 5V and R_{PU} = 10k (open-drain output only)		65		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull output	V_{OD} = 10mV, V_{UD} = 100mV		110		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull output	V_{OD} = 100mV, V_{UD} = 100mV		65		ns
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	V_{OD} = 100mV, V_{UD} = 100mV		5		ns
T_{FALL}	Output Fall Time, 80% to 20%	V_{OD} = 100mV, V_{UD} = 100mV		5		ns
F_{TOGGLE}	Toggle Frequency	V_{ID} = 200mV		7.5		MHz
POWER ON TIME						
P_{ON}	Power on-time			80		µs

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5.7 Typical Characteristics

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

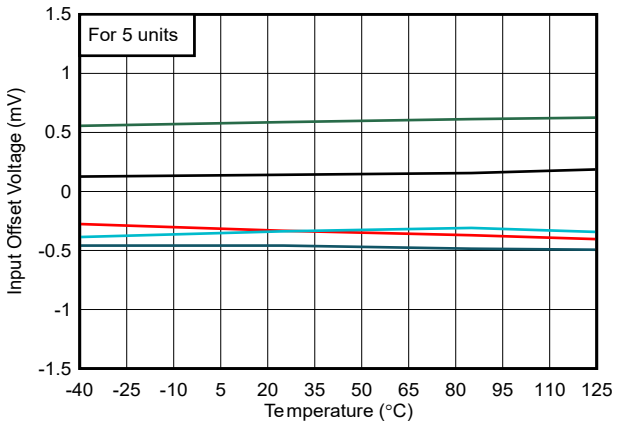


図 5-1. Offset vs. Temperature

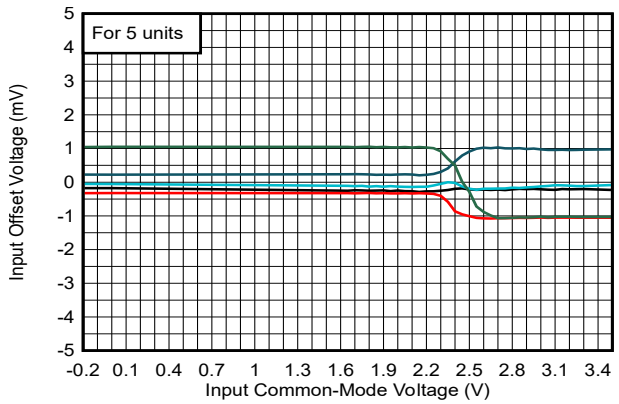


図 5-2. Offset vs. Common-Mode, 3.3V

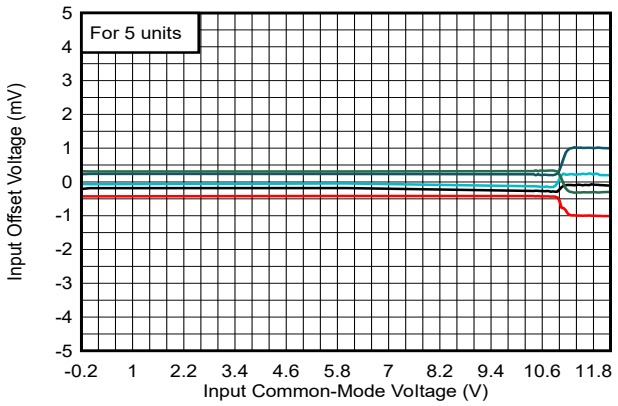


図 5-3. Offset Voltage vs. Common-Mode, 12V

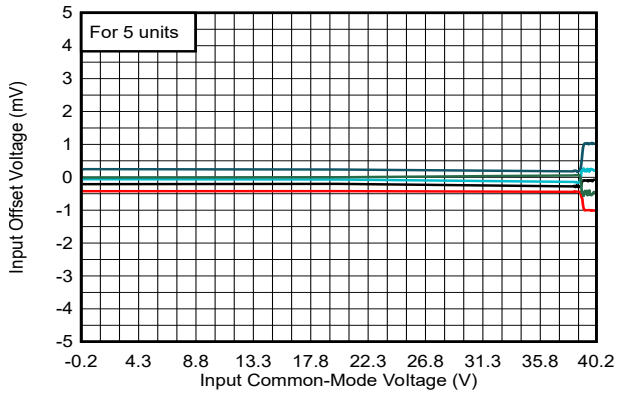


図 5-4. Offset Voltage vs. Common-Mode, 40V

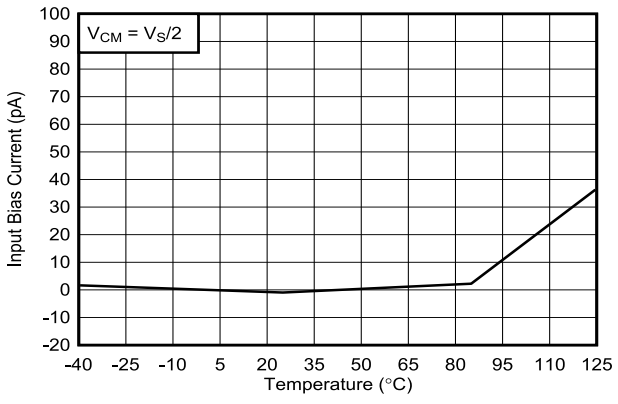


図 5-5. Bias Current vs. Temperature, 3.3V

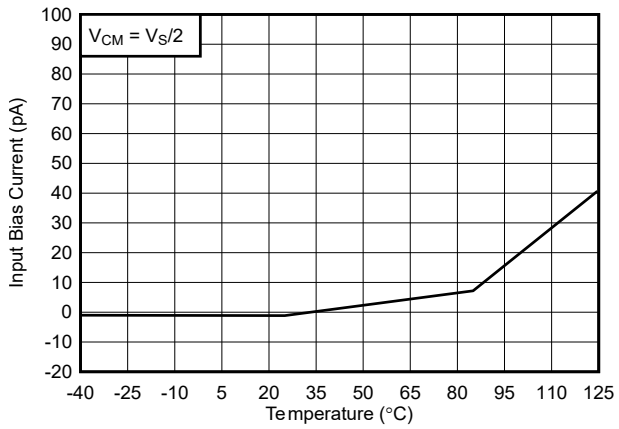


図 5-6. Bias Current vs. Temperature, 40V

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5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

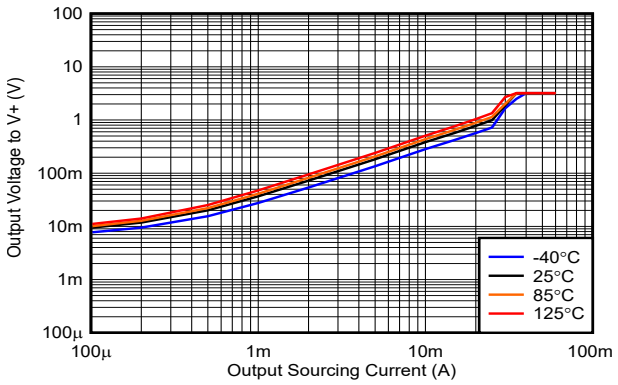


図 5-7. Output Voltage vs. Sourcing Current, 3.3V, Push-Pull only

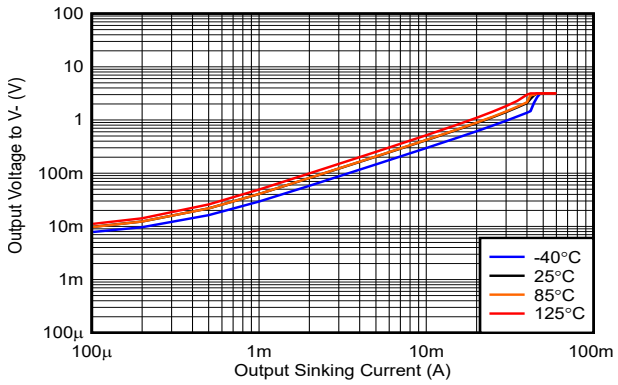


図 5-8. Output Voltage vs. Sinking Current, 3.3V

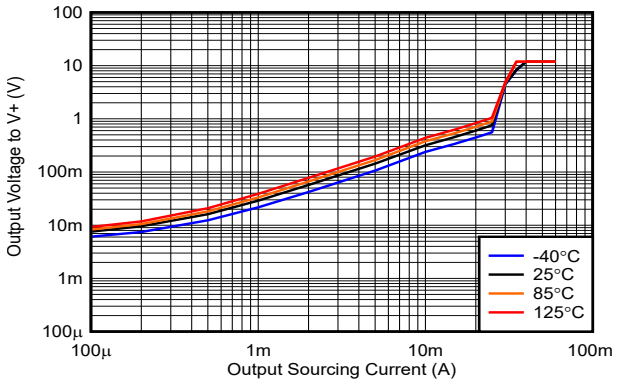


図 5-9. Output Voltage vs. Sourcing Current, 12V, Push-Pull only

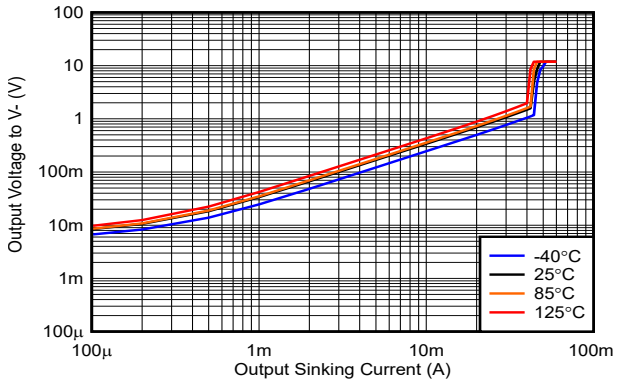


図 5-10. Output Voltage vs. Sinking Current, 12V

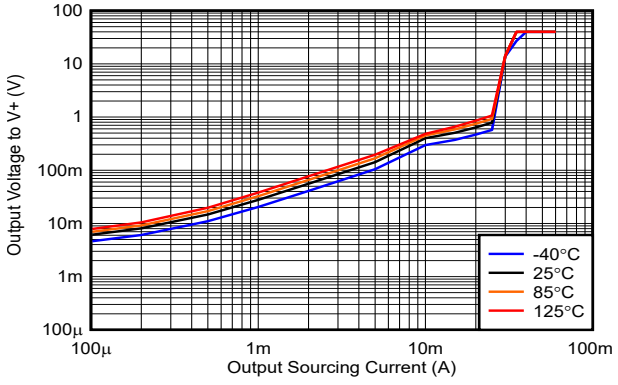


図 5-11. Output Voltage vs. Sourcing Current, 40V, Push-Pull only

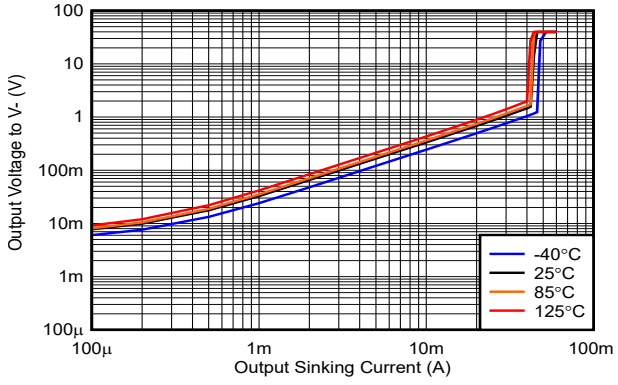


図 5-12. Output Voltage vs. Sinking Current, 40V

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5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

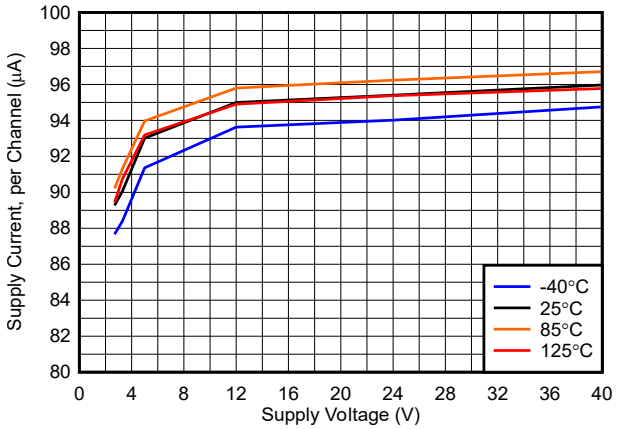


図 5-13. Supply Current vs. Supply Voltage, Output Low, No Load

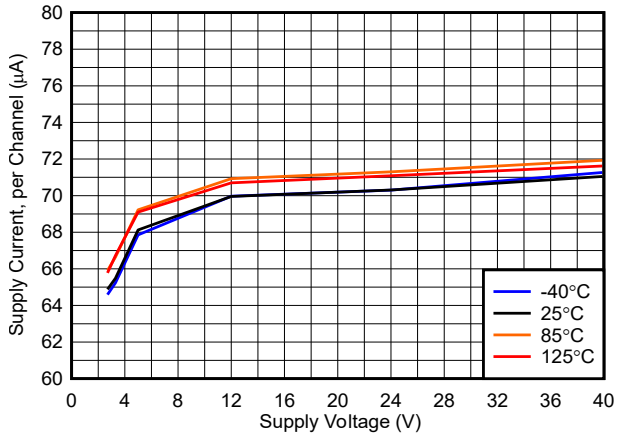


図 5-14. Supply Current vs. Supply Voltage, Output High, No Load

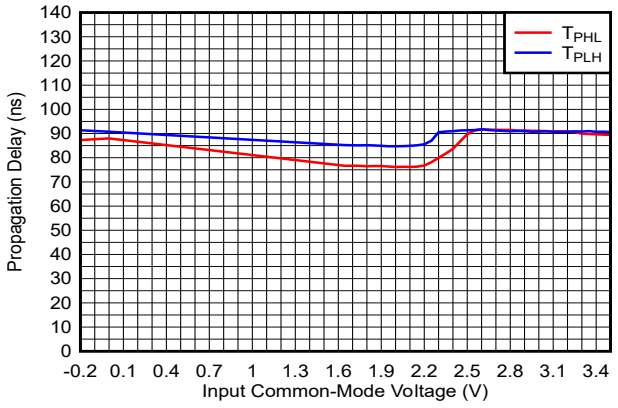


図 5-15. Propagation Delay vs. Common-Mode, 3.3V

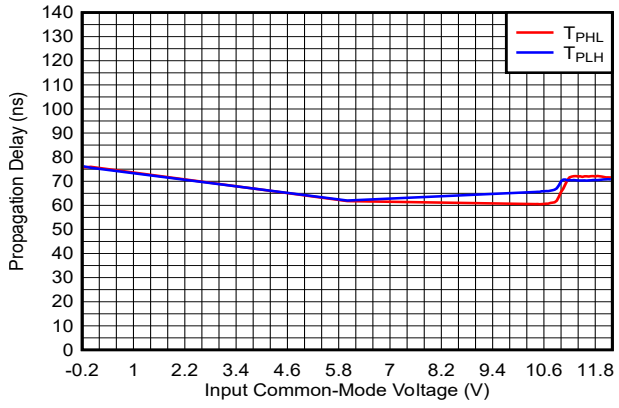


図 5-16. Propagation Delay vs. Common-Mode, 12V

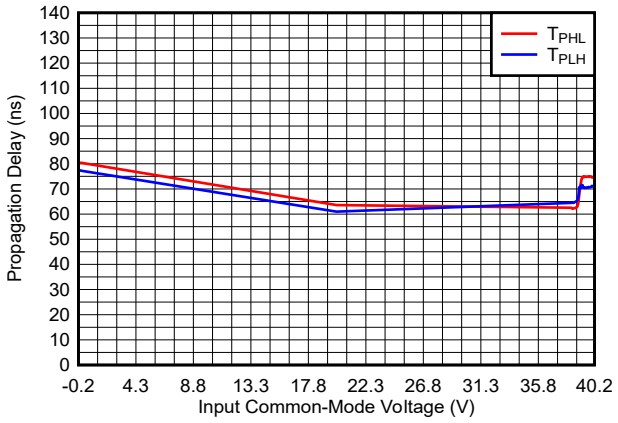


図 5-17. Propagation Delay vs. Common-Mode, 40V

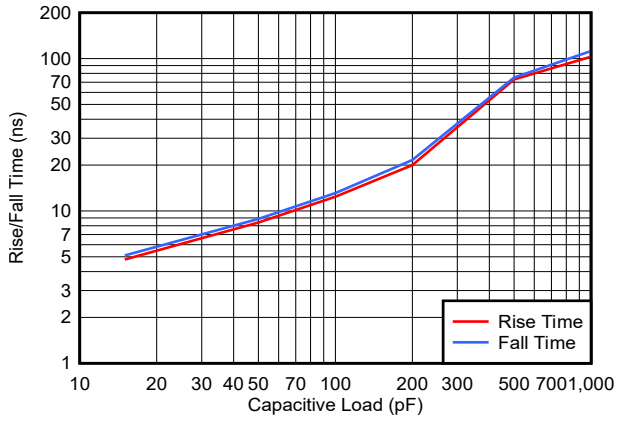


図 5-18. Rise/Fall Time vs. Capacitive Load, 12V

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5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

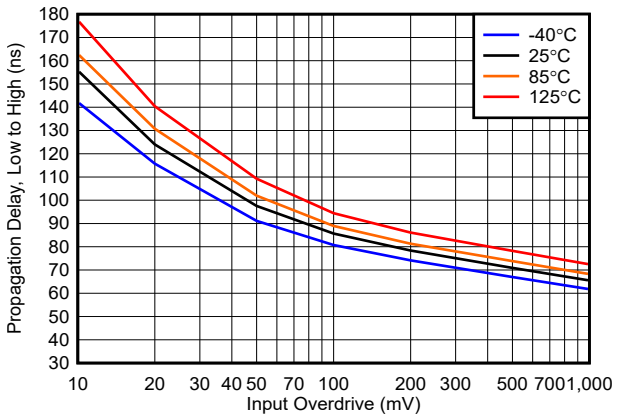


図 5-19. Propagation Delay, (Low to High) vs. Input Overdrive, 3.3V

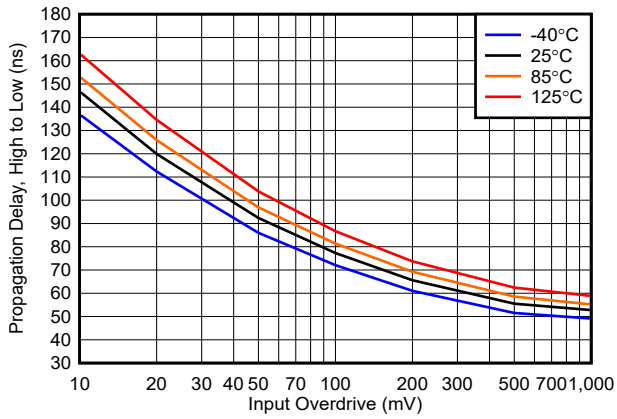


図 5-20. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V

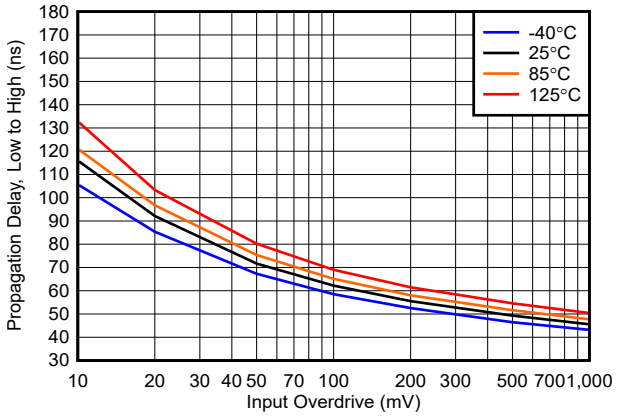


図 5-21. Propagation Delay, (Low to High) vs. Input Overdrive, 12V

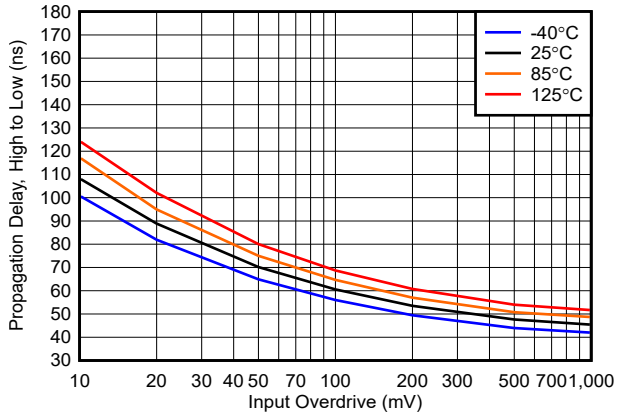


図 5-22. Propagation Delay, (High to Low) vs. Input Overdrive, 12V

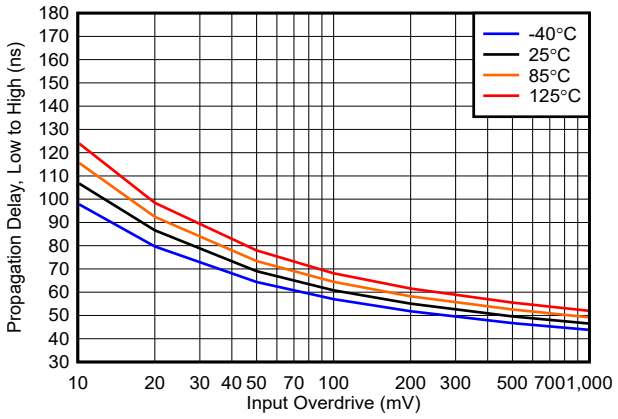


図 5-23. Propagation Delay, (Low to High) vs. Input Overdrive, 40V

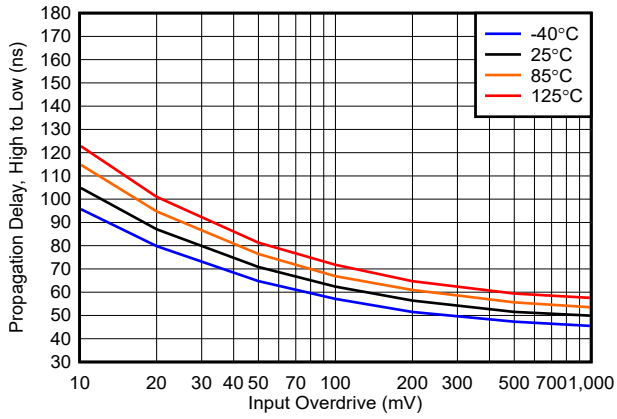


図 5-24. Propagation Delay, (High to Low) vs. Input Overdrive, 40V

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5.7 Typical Characteristics (continued)

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

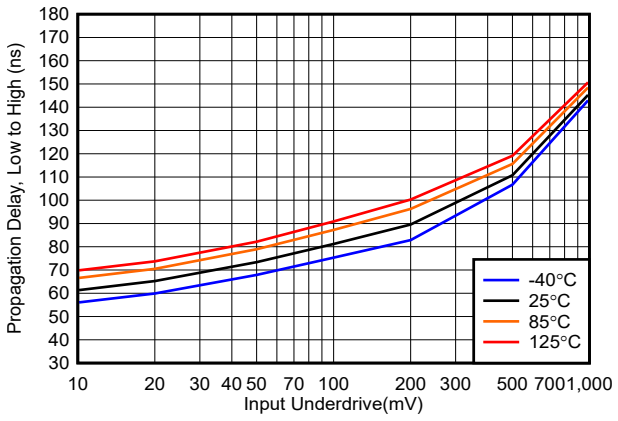


図 5-25. Propagation Delay, (Low to High) vs. Input Underdrive, 3.3V

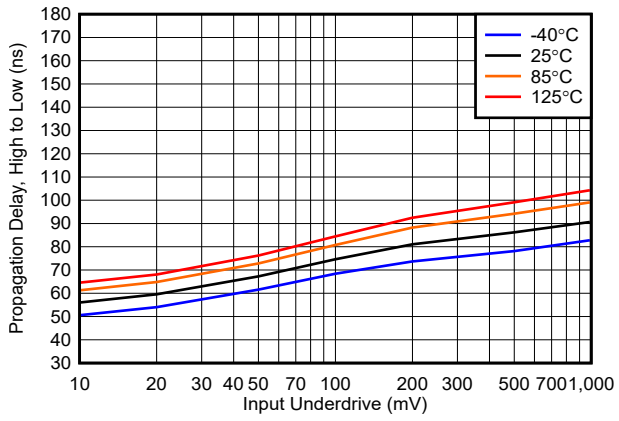


図 5-26. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V

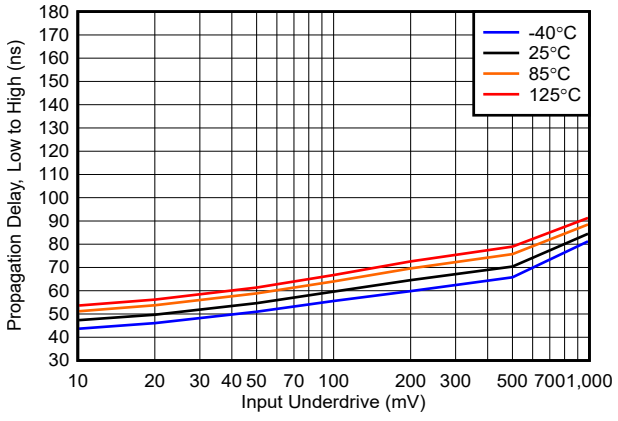


図 5-27. Propagation Delay, (Low to High) vs. Input Underdrive, 12V

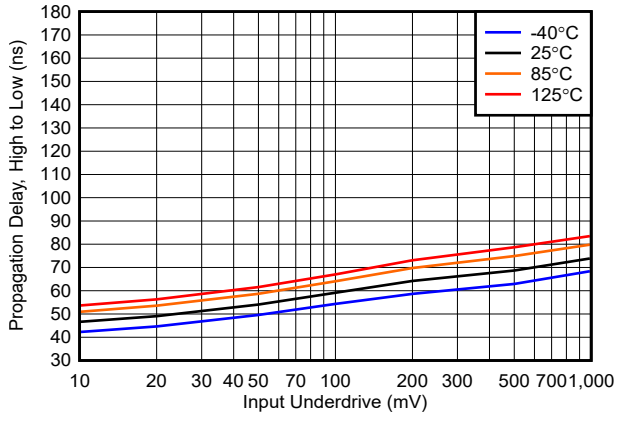


図 5-28. Propagation Delay, (High to Low) vs. Input Underdrive, 12V

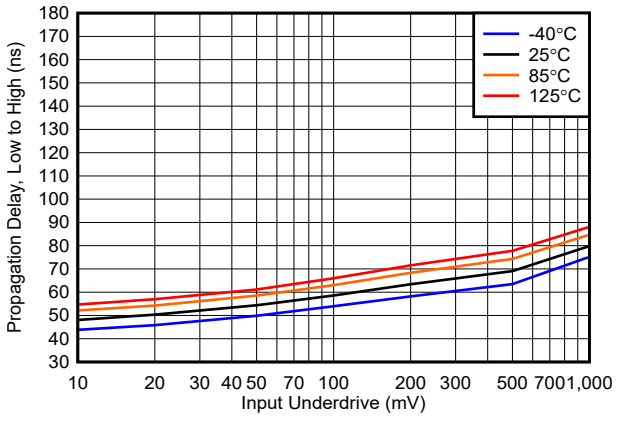


図 5-29. Propagation Delay, (Low to High) vs. Input Underdrive, 40V

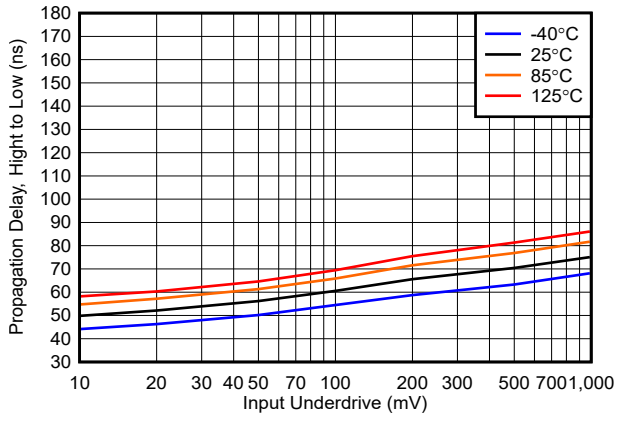


図 5-30. Propagation Delay, (High to Low) vs. Input Underdrive, 40V

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6 Detailed Description

6.1 Overview

The TLV183x and TLV184x devices are 40V high-speed comparators with push-pull and open-drain output options. Operating down to 2.7V while only consuming only 75µA per channel, the TLV183x and TLV184x are designed for voltage and current sensing applications in high voltage industrial and automotive systems. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down.

6.2 Functional Block Diagrams

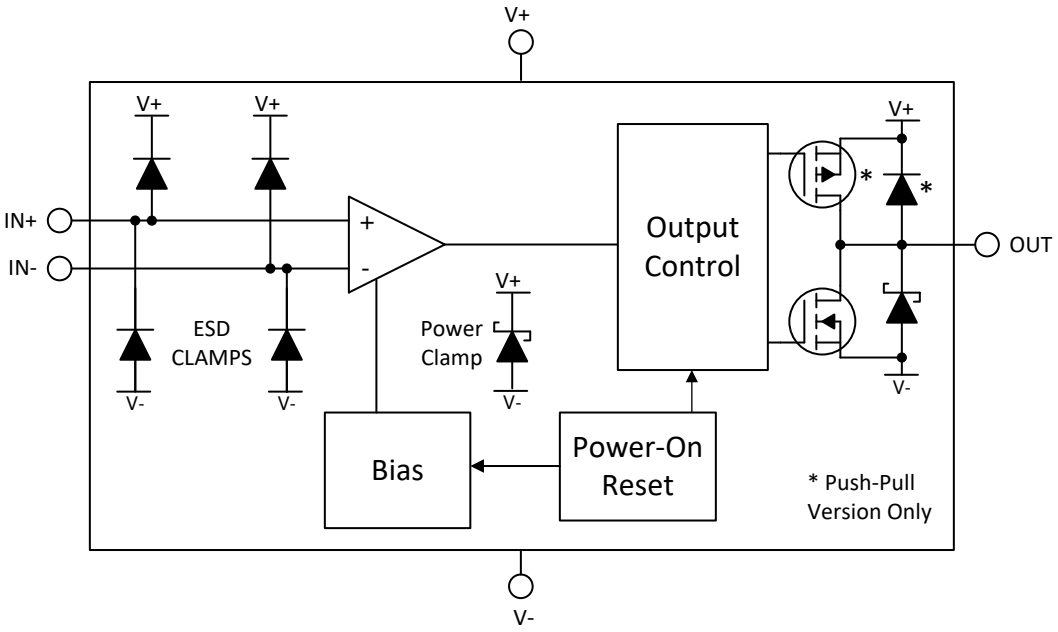


図 6-1. Block Diagram

6.3 Feature Description

The TLV183x (push-pull output) and TLV184x (open-drain output) devices are high speed comparators with a typical propagation delay of 65ns and are capable of operating at voltages up to 40V. These comparators are well-suited for high-voltage systems where short-circuit current and over voltage protection is essential for internal components. These comparators also feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails combined with a maximum 2.5mV input offset and Power-on Reset (POR) for known start-up conditions.

6.4 Device Functional Modes

6.4.1 Inputs

6.4.1.1 Rail-to-Rail Input

The input voltage range extends from 200mV below (V-) to 200mV above (V+), maximizing input dynamic range. The input stage has ESD clamps to the (V+) supply line and therefore the input voltages must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor must be used to limit the current to less than 1mA.

Likewise, unlike high-speed amplifiers, the comparator inputs do not have clamping diodes between them. This allows for applications where the input differential voltage can match the supply voltage (V+). However, when the input differential voltage increases to 2V, bias current increases to the nA range occur. This is a result of internal circuitry intended to minimize propagation delay increases due to large input underdrive amplitudes.

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6.4.1.2 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

6.4.2 Outputs

6.4.2.1 TLV183x Push-Pull Output

The TLV183x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for an external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.2.2 TLV184x Open-Drain Output

The TLV184x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage up to 40V, independent of the comparator supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA to optimize V_{OL} logic levels. Lower pull-up resistor values help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1MΩ) create an exponential rising edge due to the output RC time constant and increase the risetime.

Directly shorting the output to (V+) can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limitng resistor is recommended to limit the power dissipation.

Unused open drain outputs must be left floating, or can be tied to the (V-) pin if floating pins are not desired.

6.4.3 ESD Protection

6.4.3.1 Inputs

The rail-to-rail input does have an ESD clamp to (V+) and (V-) and therefore the input voltage must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor must be used to limit the current to less than 1mA.

Similarly, if the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. Limit the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

6.4.3.2 Outputs

The TLV183x push-pull output ESD protection contains a conventional ESD clamp between the output and (V+), and a ESD clamp between the output and (V-). The output must not exceed the supply rails by more than 200mV.

The TLV184x open-drain output ESD protection consists of an ESD clamping circuit to (V-) only to allow the output to be pulled above (V+) to a maximum of 40V. There is no ESD clamp diode between the output and (V+) on the open-drain output.

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6.4.4 Power-On Reset (POR)

The TLV183x and TLV184x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 80µs after the V_{POR} of 1.9V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For both TLV183x and TLV184x devices, the POR circuit keeps the output high impedance (Hi-Z) during the POR period (P_{on}).

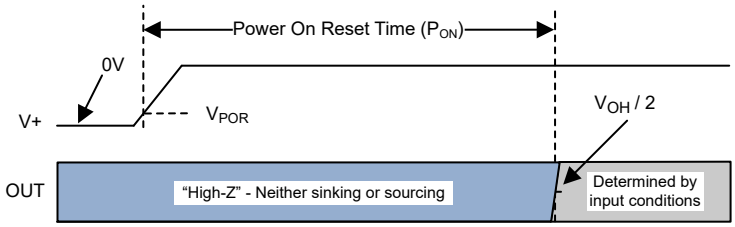


図 6-2. Power-On Reset Timing Diagram

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7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the 図 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). 表 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in 図 7-1 and is measured from the mid-point of the input to the midpoint of the output.

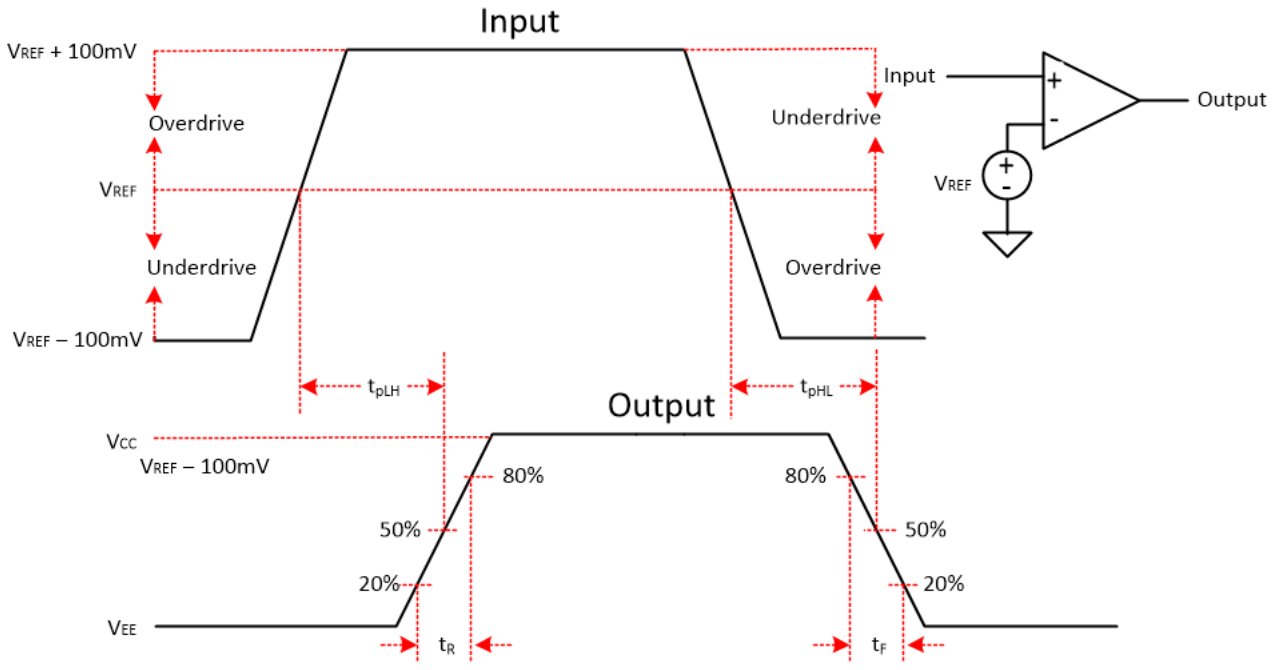


図 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the 図 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration can produce a noisy chatter output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

External hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown in 図 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

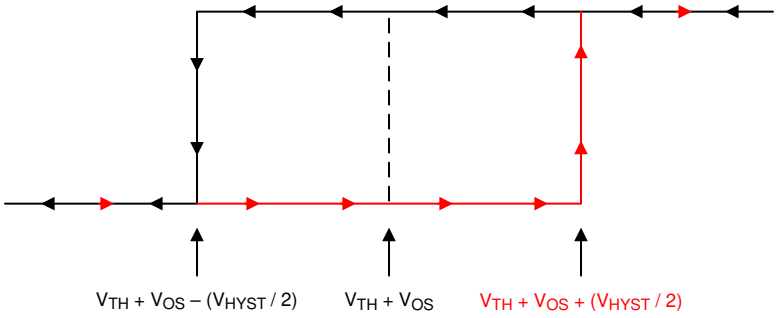


図 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 図 7-3.

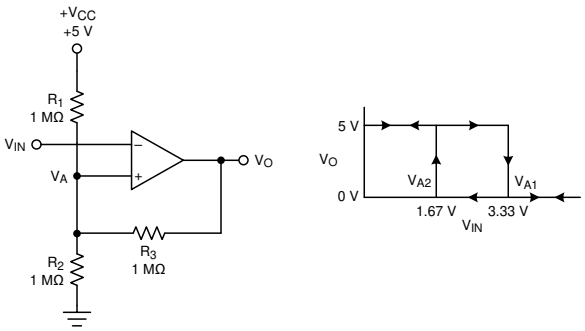


図 7-3. TLV183x in an Inverting Configuration With Hysteresis

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The equivalent resistor networks when the output is high and low are shown in 図 7-3.

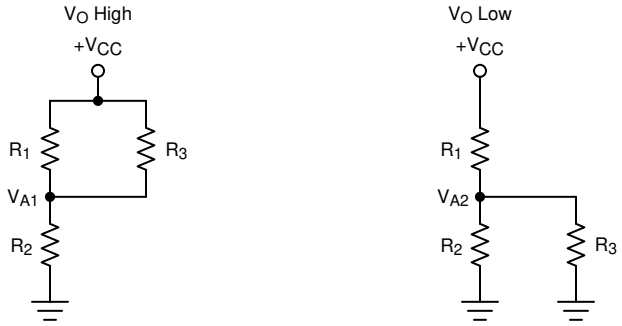


図 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in 図 7-4.

式 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in 式 2.

Use 式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in 図 7-5,

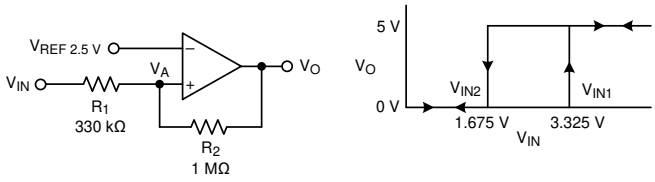


図 7-5. TLV183x in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 図 7-6.

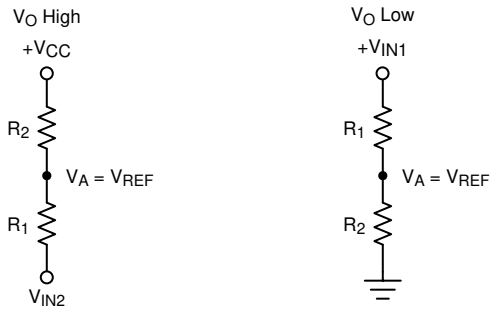


図 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF},, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use 式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use 式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.1.2.3 Inverting and Non-Inverting Hysteresis Using Open-Drain Output

Using an open drain output device, such as the TLV184x is possible, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 図 7-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV184x if the outputs are directly connected together.

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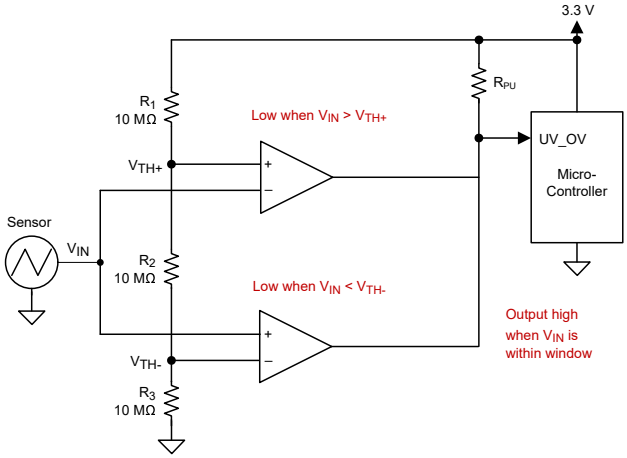


図 7-7. Window Comparator

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 7-7. Connect V+ to a 3.3V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs is low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in 図 7-8.

7.2.1.3 Application Curve

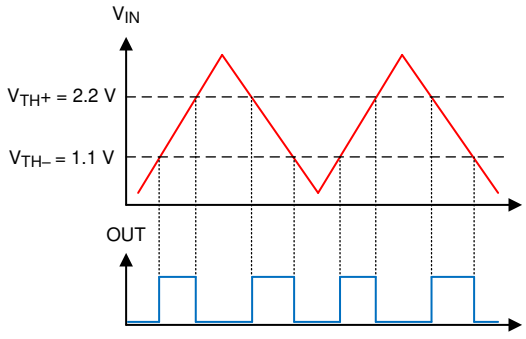


図 7-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.2.2 Square Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV183x) is recommended for best symmetry.

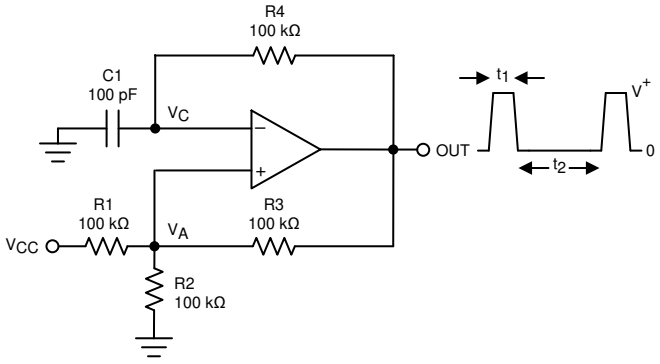


図 7-9. Square-Wave Oscillator

7.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help to reduce BOM cost and board space. TI recommends that R4 be over several kilo-ohms to minimize loading of the output.

7.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

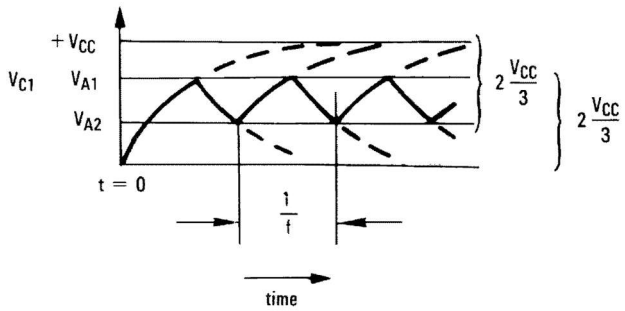


図 7-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Square-Wave Oscillator as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increasing until equal to the noninverting input. The value of V_A at the point is calculated below.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated below.

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$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until reaching V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by R_4C_1 × ln 2 for each trip. Therefore, the total time duration is calculated as 2 R_4C_1 × ln 2.

The oscillation frequency can be obtained below.

$$f = 1/(2\ R4 \times C1 \times In2) \quad (9)$$

7.2.2.3 Application Performance Plots

The Square-Wave Oscillator Output Waveform shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 10k\Omega$
- C_1 =100pF, C_L = 20pF
- V+ = 5V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10pF

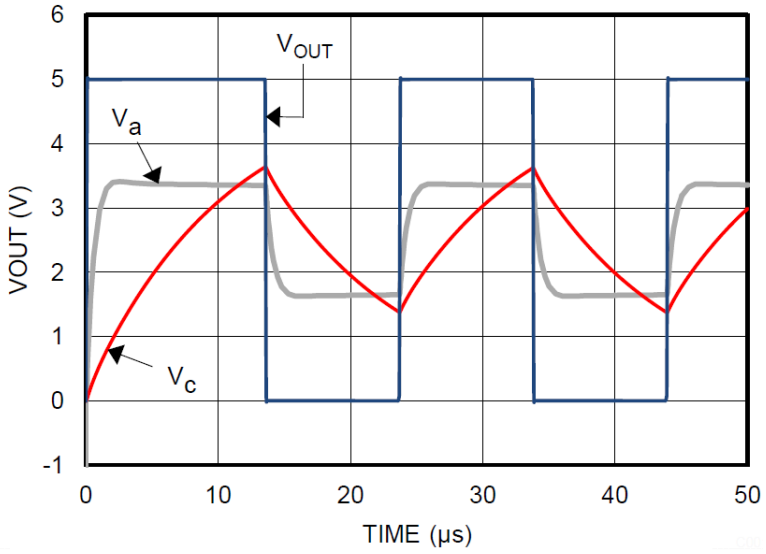


図 7-11. Square-Wave Oscillator Output Waveform

7.3 Power Supply Recommendations

Due to fast output edges, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can impact the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) & (V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

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7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. As shown in the figure below, input and output traces can be run in parallel as long as there is a (V+) or GND trace between output to reduce coupling. A "better" way to reduce coupling is to have the traces ran further away from each other.

When series resistance is added to inputs, place the resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

7.4.2 Layout Example

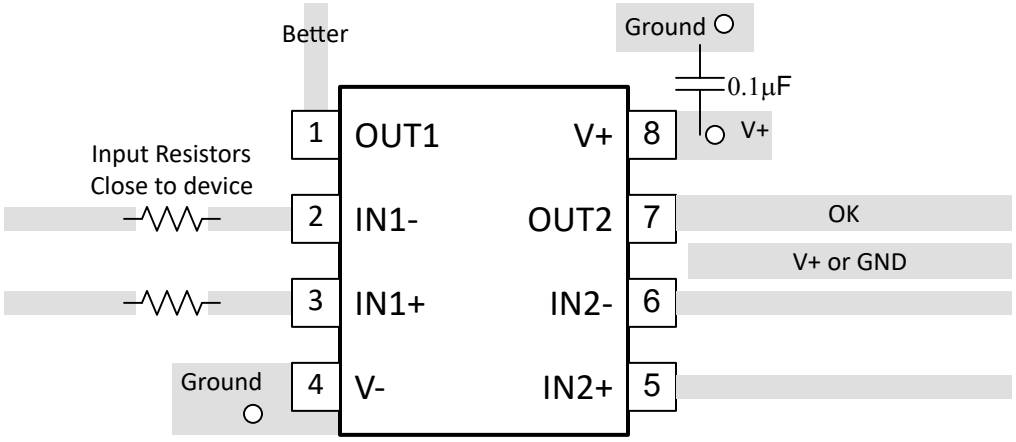


図 7-12. Dual Layout Example

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2024) to Revision B (February 2025)	Page
• WSON パッケージ オプションをリリース	1

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Changes from Revision * (May 2024) to Revision A (November 2024) **Page**

- ドキュメント全体を通して静止電流と入力オフセット電圧の仕様を更新.....1
- データシート全体を通して TLV1831_41_32_42-Q1 を量産にリリース.....1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1831DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1831
TLV1831DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	See TLV1831DBVR	1831
TLV1831DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1TL
TLV1831DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	See TLV1831DCKR	1TL
TLV1832DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	T32D
TLV1832DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TLV1832DGKR	T32D
TLV1832DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	T32C
TLV1832PWR	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1832
TLV1832PWR.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TLV1832PWR	TL1832
TLV1841DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1841
TLV1841DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	See TLV1841DBVR	1841
TLV1841DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1TM
TLV1841DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	See TLV1841DCKR	1TM
TLV1842DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42D
TLV1842DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42D
TLV1842DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42C
TLV1842PWR	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1842
TLV1842PWR.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1842

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV1831, TLV1832, TLV1841, TLV1842 :

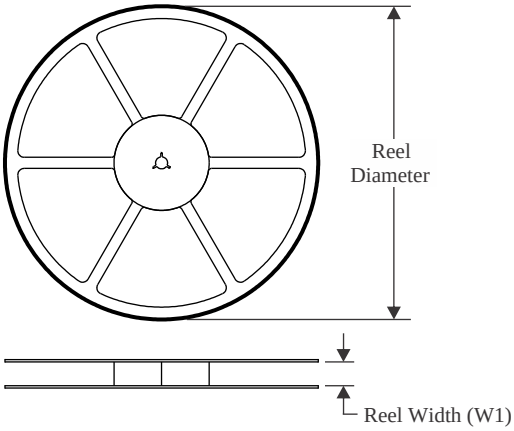
- Automotive : TLV1831-Q1, TLV1832-Q1, TLV1841-Q1, TLV1842-Q1

NOTE: Qualified Version Definitions:

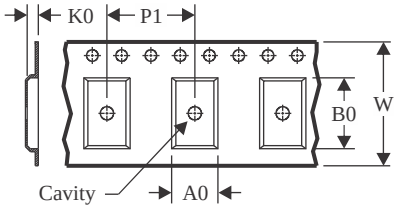
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

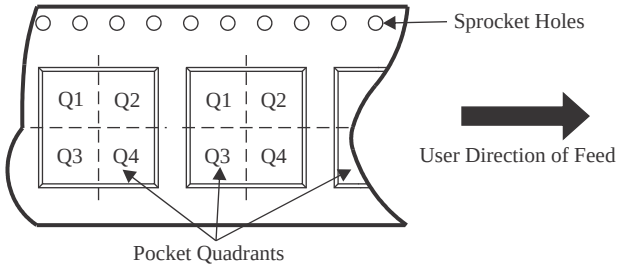


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

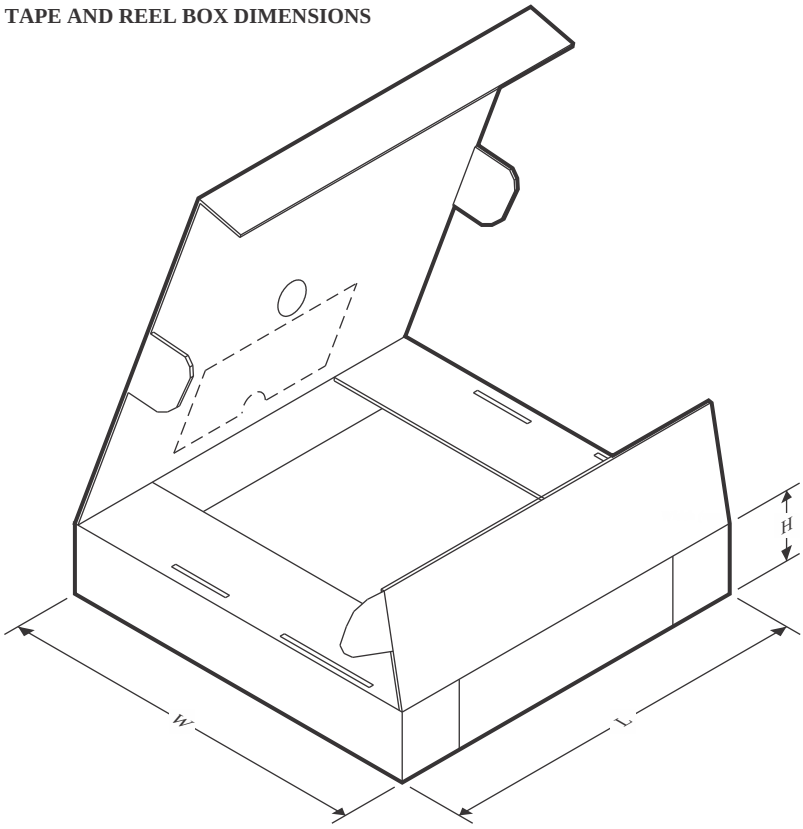
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1831DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1831DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV1832DGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1832DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV1832PWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV1841DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1841DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV1842DGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1842DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV1842PWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

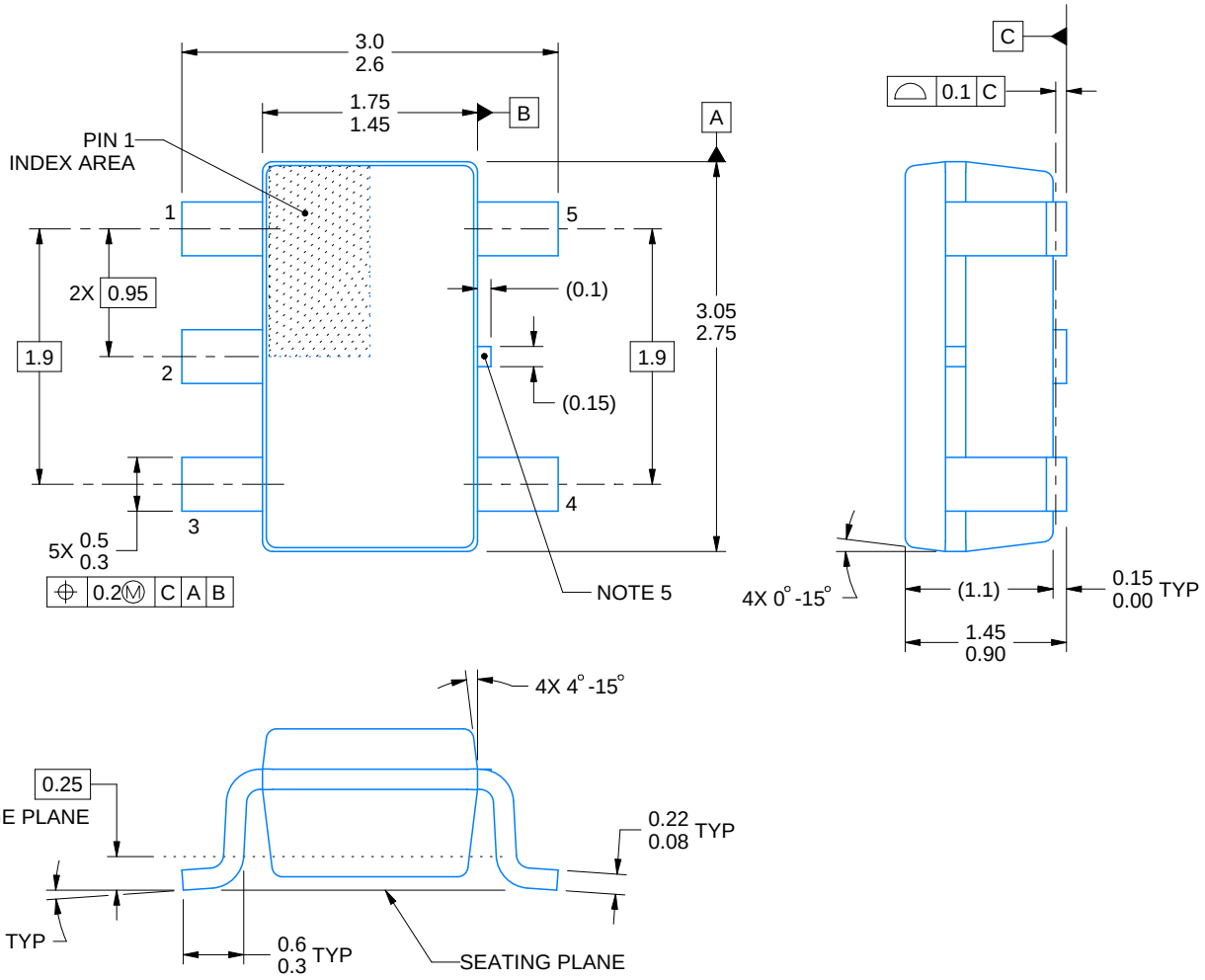
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1831DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1831DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV1832DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1832DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV1832PWR	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV1841DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1841DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV1842DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1842DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV1842PWR	TSSOP	PW	8	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

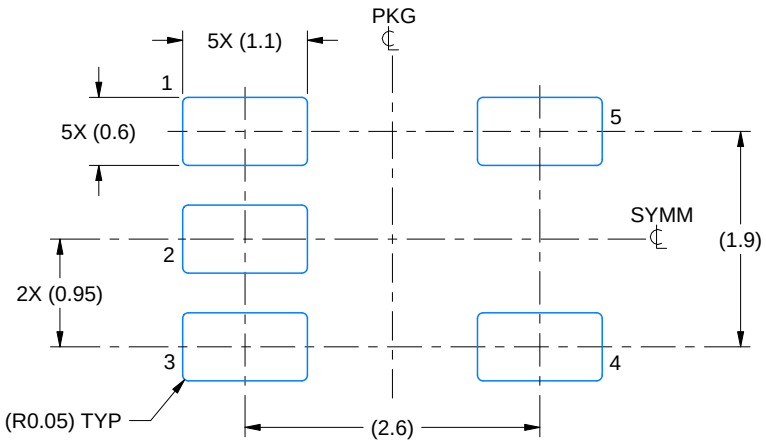
SMALL OUTLINE TRANSISTOR



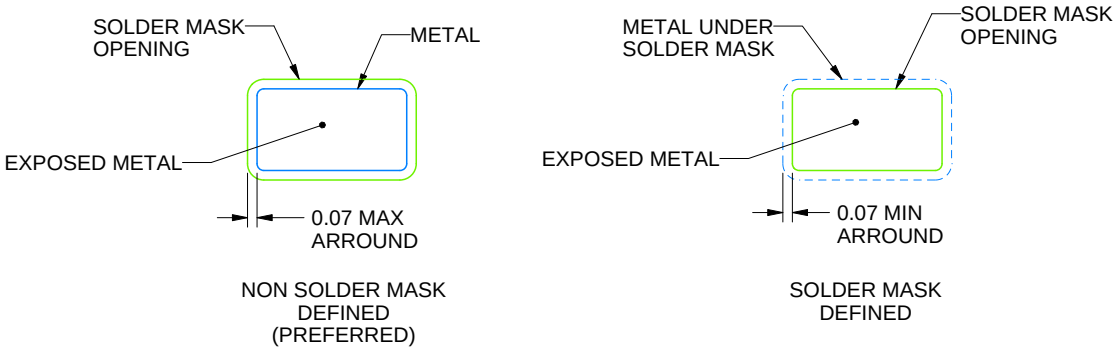
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

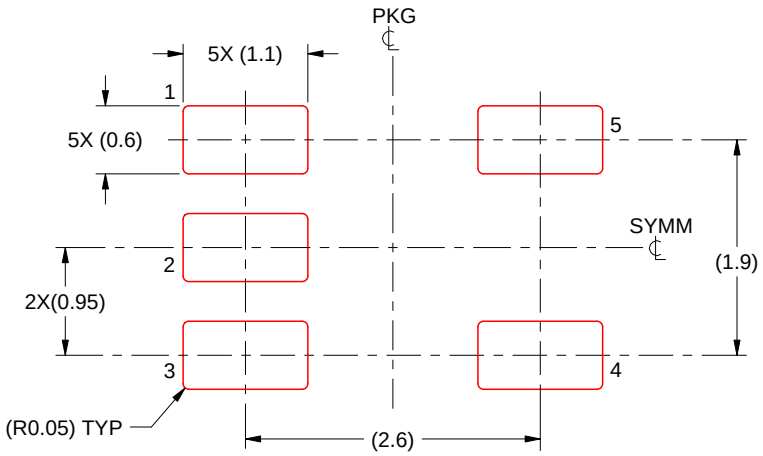


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

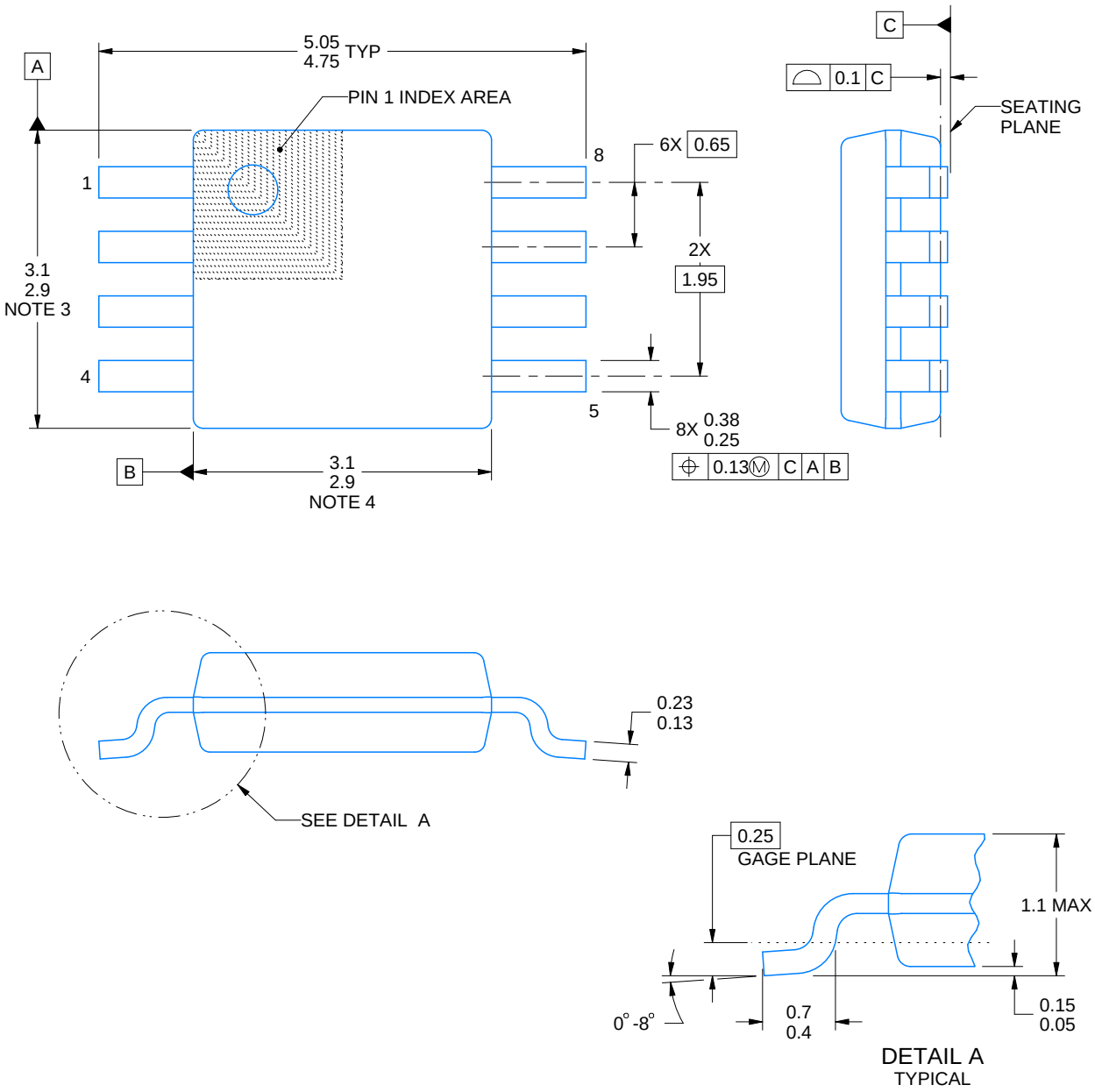
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

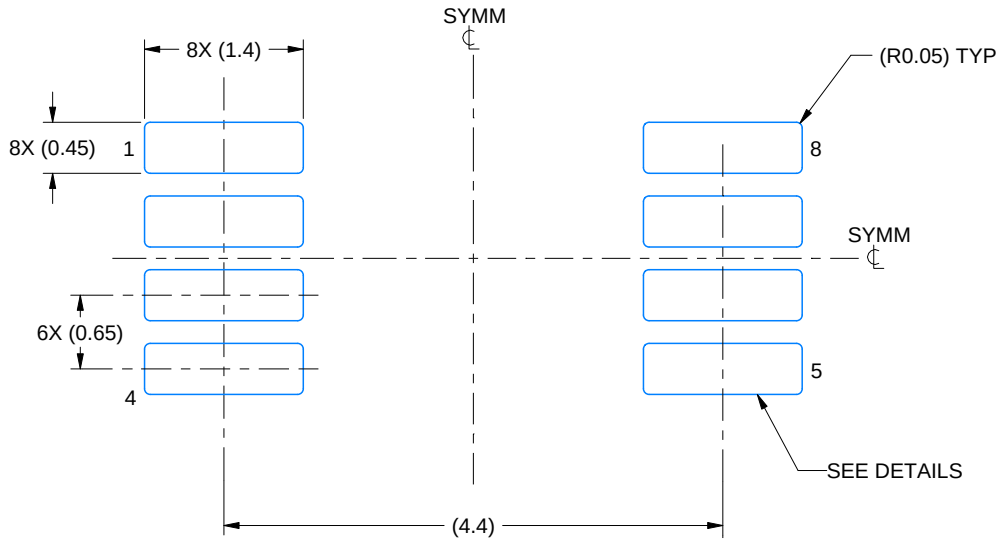
SMALL OUTLINE PACKAGE



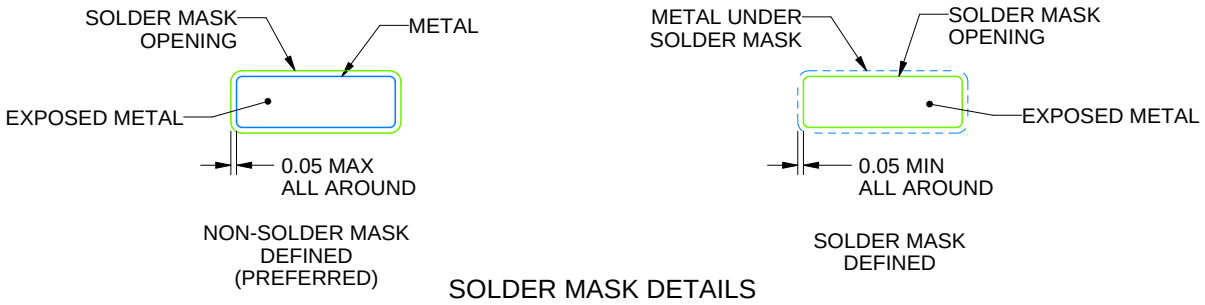
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

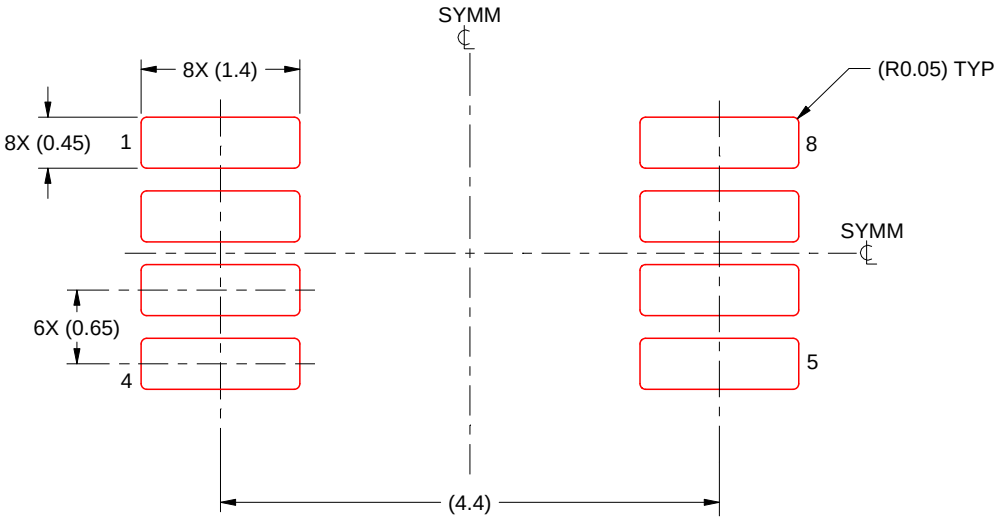


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

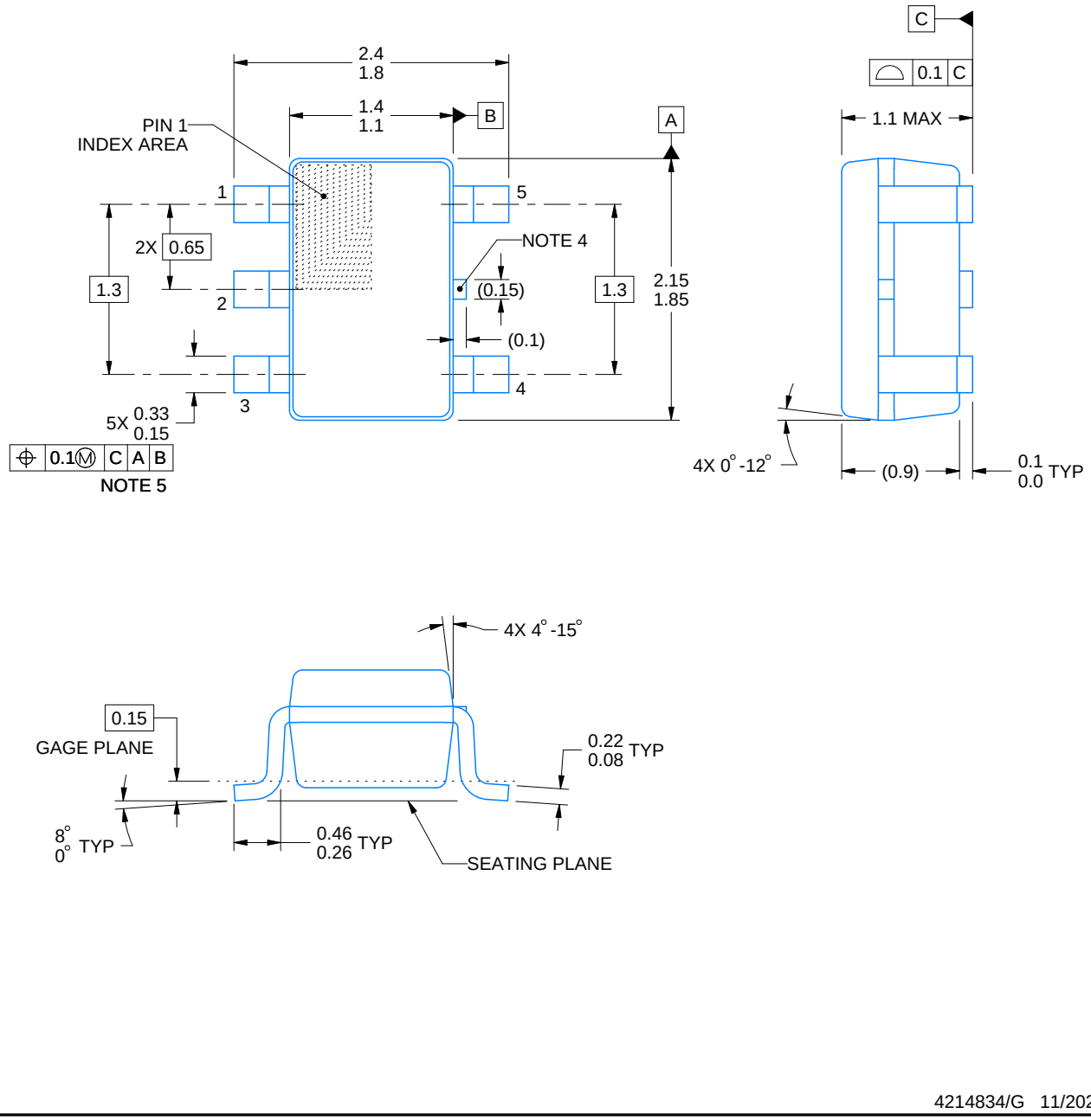
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

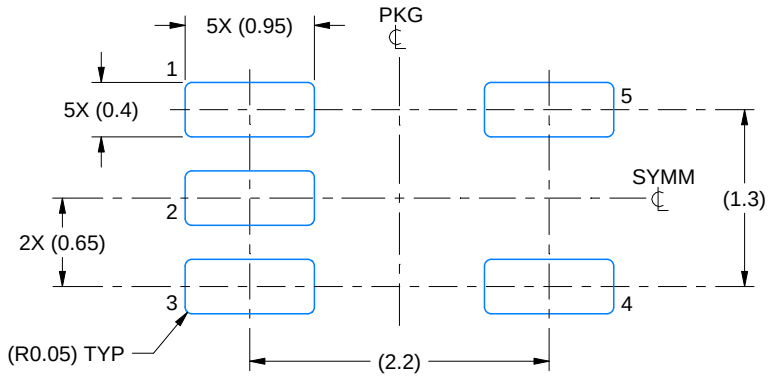
SMALL OUTLINE TRANSISTOR



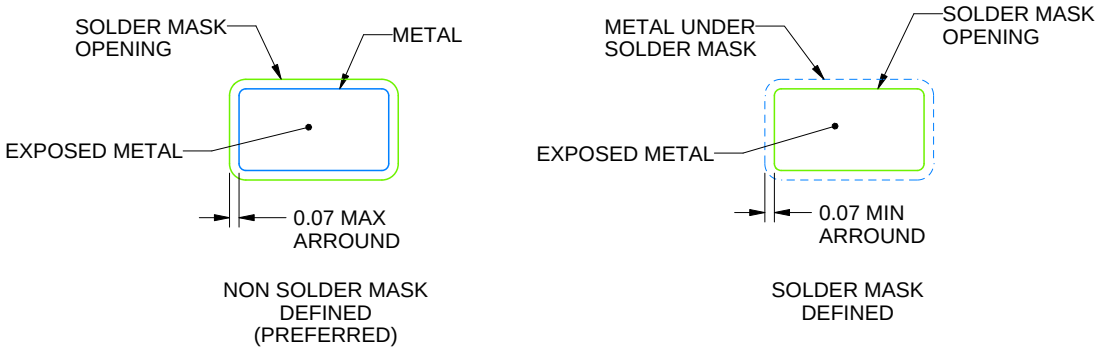
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

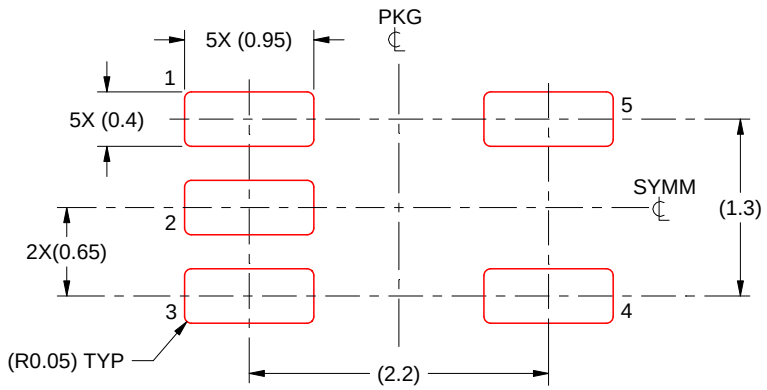


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

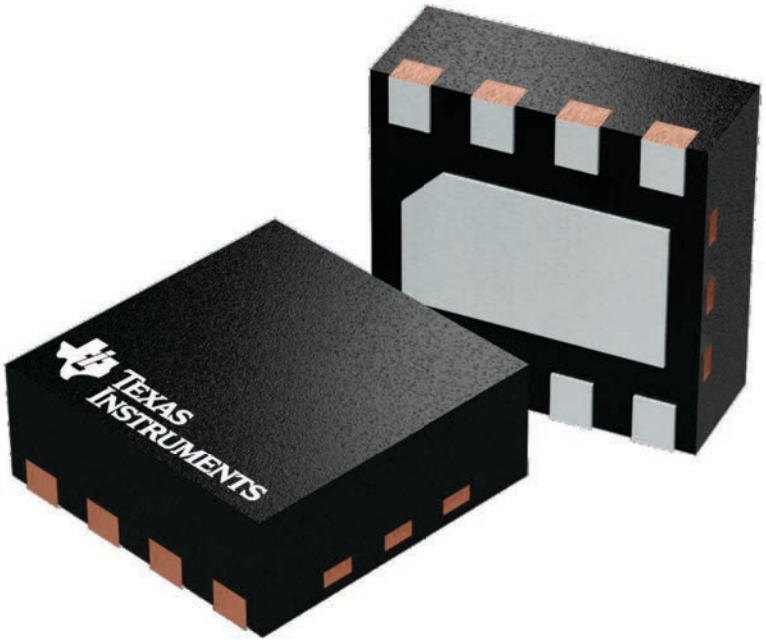
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



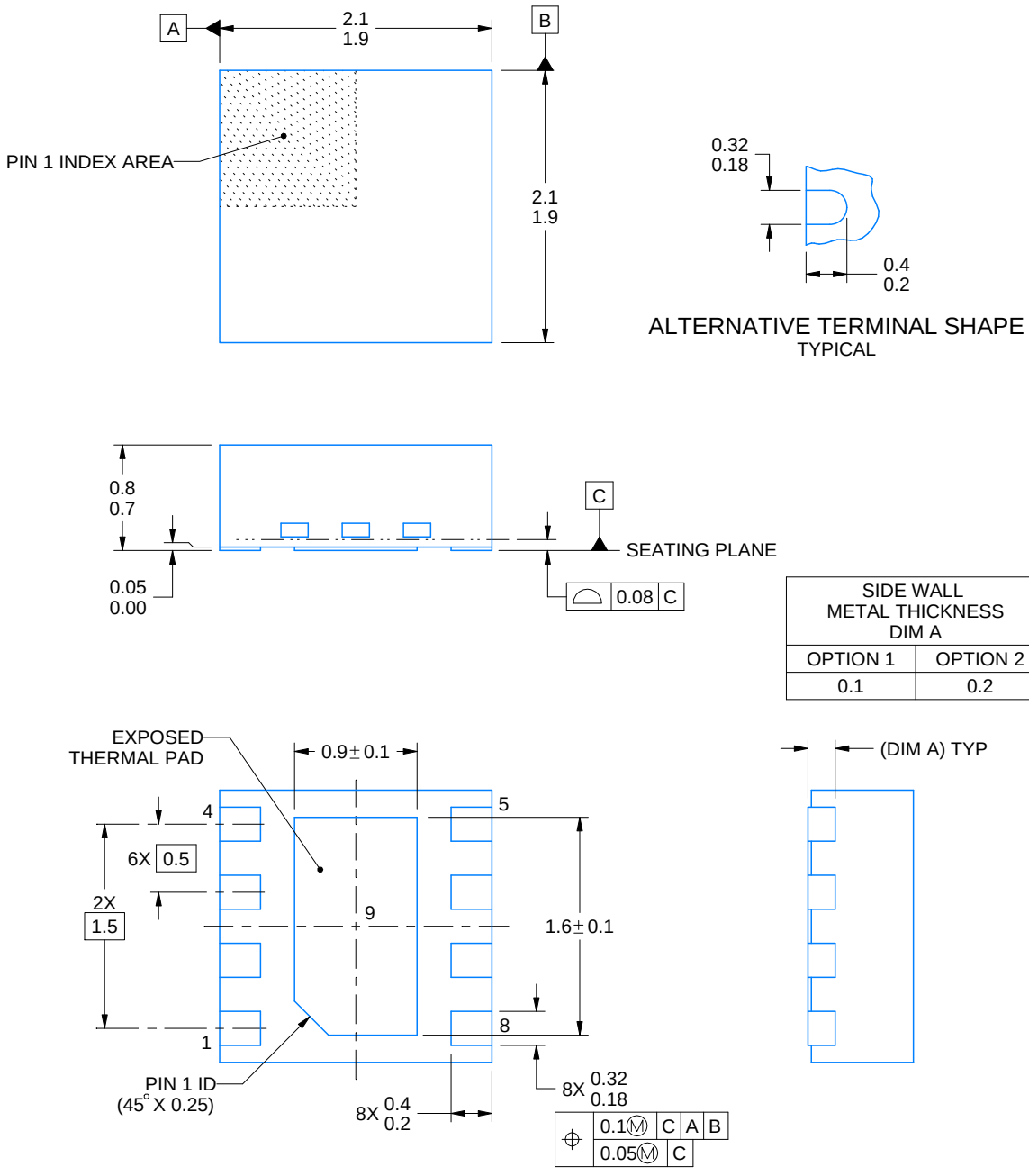
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

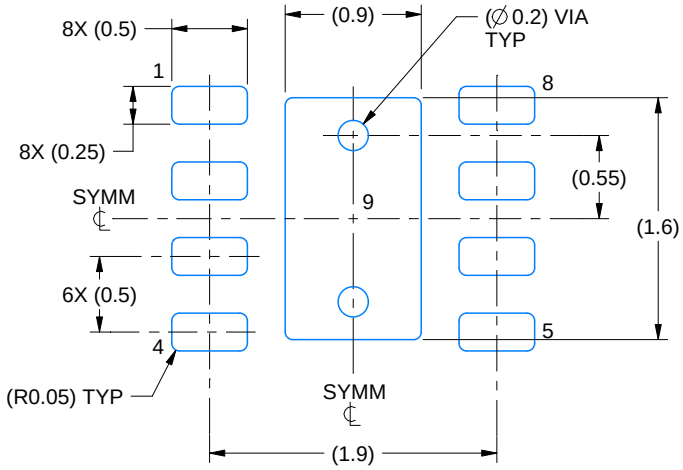
PLASTIC SMALL OUTLINE - NO LEAD



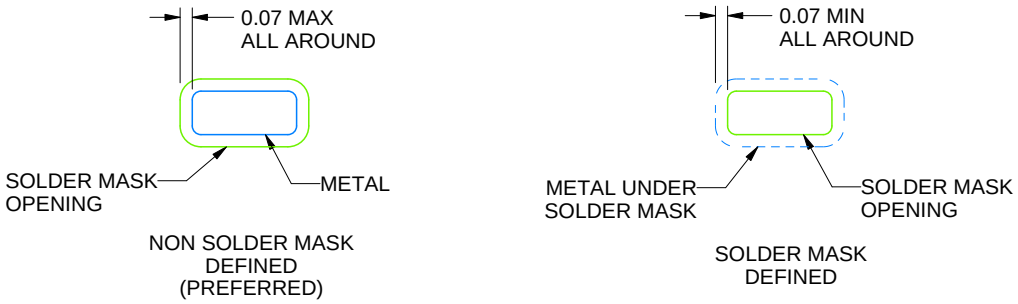
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

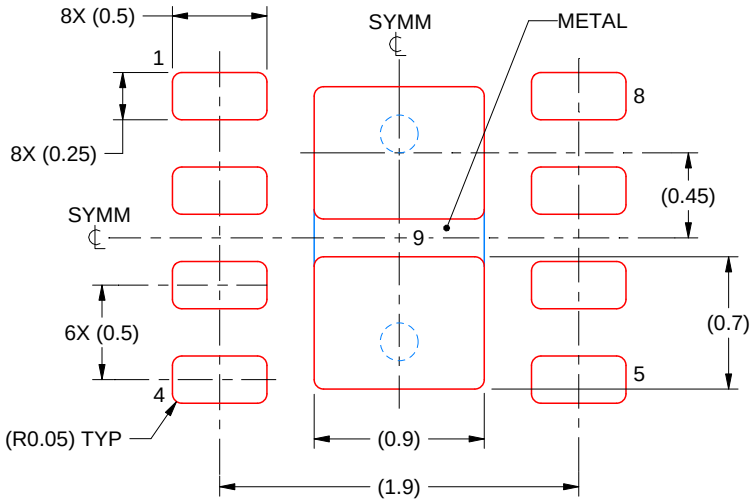


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

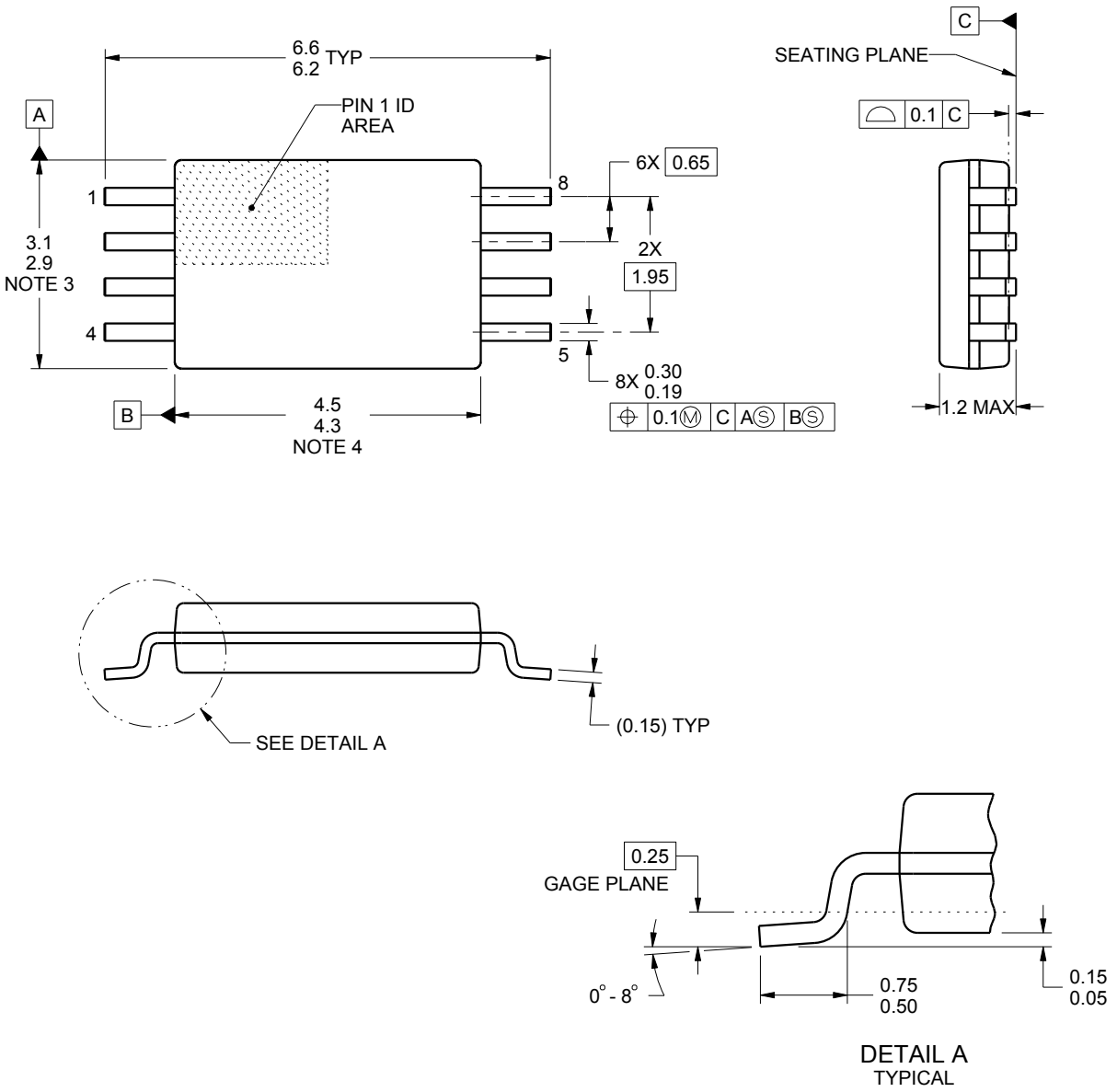
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

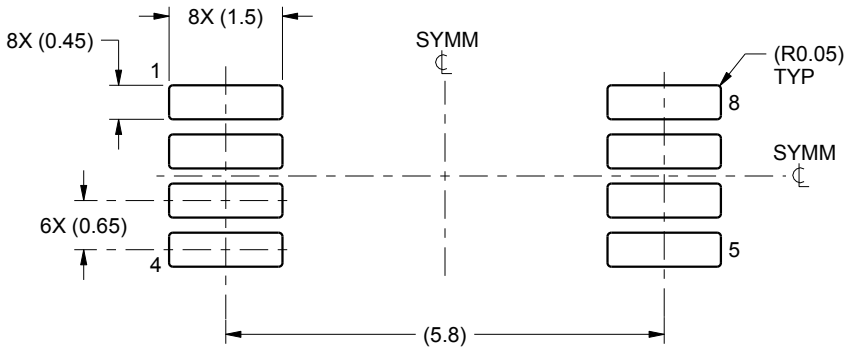
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

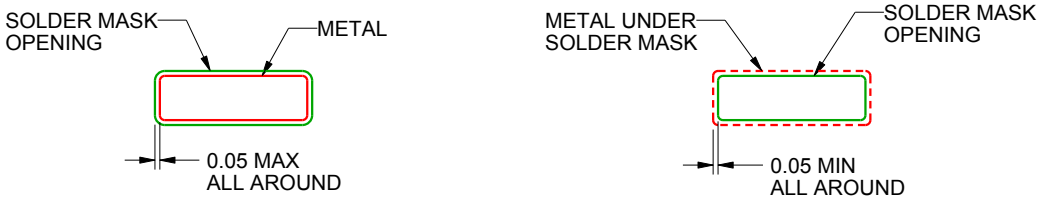


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

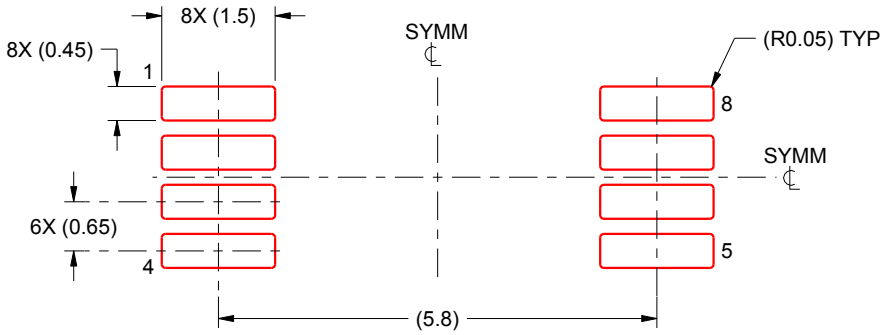


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月