



TLVx379

コスト最適化された低電圧、4 μ A、レール・ツー・レールI/Oオペアンプ

1 特長

- コスト最適化された高精度のアンプ
- microPower: 4 μ A (標準値)
- 低いオフセット電圧: 0.8mV (標準値)
- レール・ツー・レール入出力
- ユニティ・ゲイン安定
- 広い電源電圧範囲: 1.8V~5.5V
- microSizeパッケージ
 - 5ピンSC70
 - 5ピンSOT-23
 - 8ピンSOIC
 - 14ピンTSSOP

2 アプリケーション

- 外付けバッテリー
- 太陽光インバータ
- 低電力のモータ制御
- バッテリー駆動計測器
- ポータブル・デバイス
- 医療機器
- ハンドヘルド・テスト機器

3 概要

TLV379ファミリのシングル、デュアル、クワッド・オペアンプは、コスト最適化された世代の低電圧microPowerアンプです。これらのアンプは最低1.8V (± 0.9 V)の電源電圧で動作し、チャンネルごとに静止電流4 μ Aと非常に消費電流が低いため、消費電力の制約が厳しいアプリケーションに最適です。さらに、レール・ツー・レールの入出力能力があるため、TLV379ファミリは事実上あらゆる単一電源のアプリケーションに使用可能です。

TLV379 (シングル)は、5ピンのSC70およびSOT23と、8ピンのSOICパッケージで供給されます。TLV2379 (デュアル)は、8ピンのSOICパッケージで供給されます。

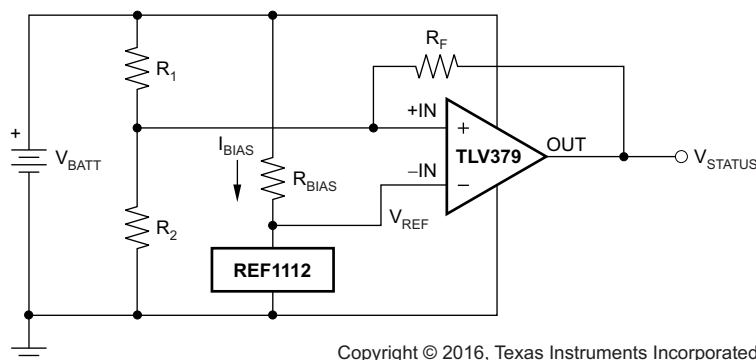
TLV4379 (クワッド)は、14ピンのTSSOPパッケージで供給されます。どのバージョンも、-40 $^{\circ}$ C~+125 $^{\circ}$ Cで動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TLV379	SC70 (5)	2.00mm×1.25mm
	SOT-23 (5)	2.90mm×1.60mm
	SOIC (8)	4.90mm×3.91mm
TLV2379	SOIC (8)	4.90mm×3.91mm
TLV4379	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

バッテリー監視アプリケーションでのTLV379の使用



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

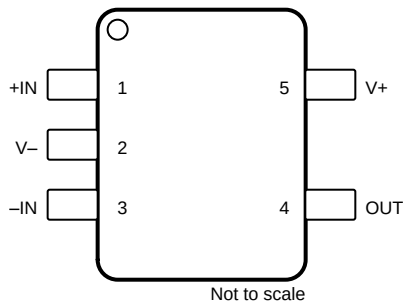
Revision A (September 2016) から Revision B に変更	Page
• Added underscores to pin names in Pin Functions tables to match connection diagrams	4
2016年4月発行のものから更新	Page
• Changed DBV pinout	3

5 Device Comparison Table

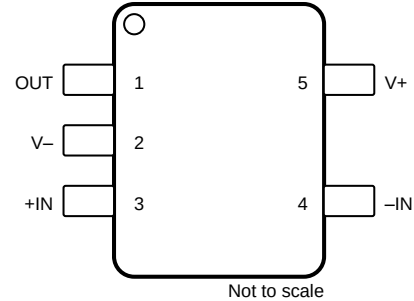
FEATURES	PRODUCT
1 μ A, 70 kHz, 2-mV V_{OS} , 1.8-V to 5.5-V supply	OPAx349
1 μ A, 5.5 kHz, 390- μ V V_{OS} , 2.5-V to 16-V supply	TLV240x
1 μ A, 5.5 kHz, 0.6-mV V_{OS} , 2.5-V to 12-V supply	TLV224x
7 μ A, 160 kHz, 0.5-mV V_{OS} , 2.7-V to 16-V supply	TLV27Lx
7 μ A, 160 kHz, 0.5-mV V_{OS} , 2.7-V to 16-V supply	TLV238x
20 μ A, 350 kHz, 2-mV V_{OS} , 2.3-V to 5.5-V supply	OPAx347
20 μ A, 500 kHz, 550- μ V V_{OS} , 1.8-V to 3.6-V supply	TLV276x
45 μ A, 1 MHz, 1-mV V_{OS} , 2.1-V to 5.5-V supply	OPAx348

6 Pin Configuration and Functions

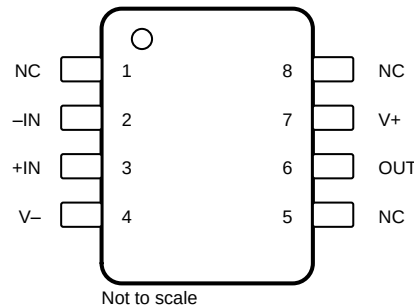
**TLV379: DCK Package
5-Pin SC70
Top View**



**TLV379: DBV Package
5-Pin SOT23
Top View**



**TLV379: D Package
8-Pin SOIC
Top View**

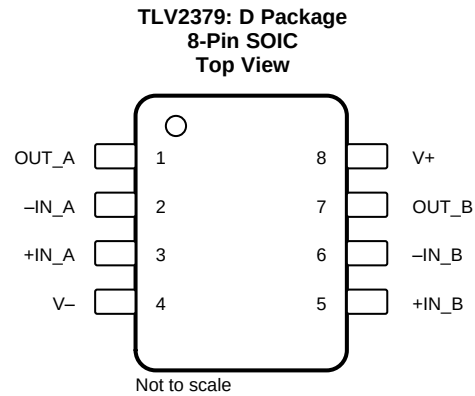


Pin Functions: TLV379

NAME	NO.			I/O	DESCRIPTION
	DCK	DBV	D		
-IN	3	4	2	I	Negative (inverting) input
+IN	1	3	3	I	Positive (noninverting) input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V-	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

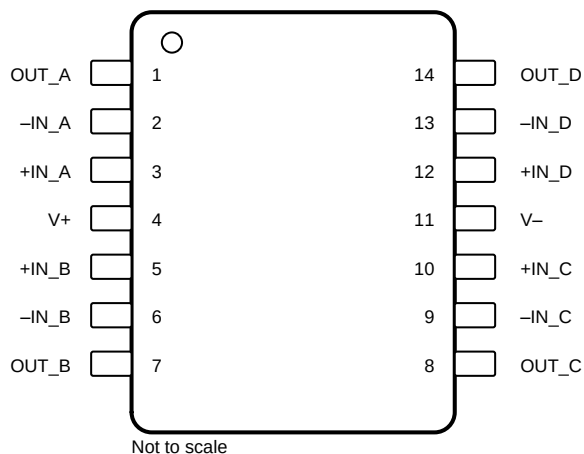
TLV379, TLV2379, TLV4379

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Pin Functions: TLV2379

NAME	NO.	I/O	DESCRIPTION
-IN_A	2	I	Inverting input, channel A
+IN_A	3	I	Noninverting input, channel A
-IN_B	6	I	Inverting input, channel B
+IN_B	5	I	Noninverting input, channel B
OUT_A	1	O	Output, channel A
OUT_B	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

**TLV4379: PW Package
14-Pin TSSOP
Top View**



Pin Functions: TLV4379

NAME	NO.	I/O	DESCRIPTION
-IN_A	2	I	Inverting input, channel A
+IN_A	3	I	Noninverting input, channel A
-IN_B	6	I	Inverting input, channel B
+IN_B	5	I	Noninverting input, channel B
-IN_C	9	I	Inverting input, channel C
+IN_C	10	I	Noninverting input, channel C
-IN_D	13	I	Inverting input, channel D
+IN_D	12	I	Noninverting input, channel D
OUT_A	1	O	Output, channel A
OUT_B	7	O	Output, channel B
OUT_C	8	O	Output, channel C
OUT_D	14	O	Output, channel D
V-	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, $V_S = (V+) - (V-)$		7	V
	Signal input pin ⁽²⁾	$(V-) - 0.5$	$(V+) + 0.5$	
Current	Signal input pin ⁽²⁾		±10	mA
	Output short-circuit ⁽³⁾		Continuous	
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S Supply voltage	Single supply	1.8		5.5	V
	Dual supply	±0.9		±2.75	
T_A Operating temperature		–40		125	°C

7.4 Thermal Information: TLV379

THERMAL METRIC ⁽¹⁾		TLV379			UNIT
		DCK (SC70)	DBV (SOT23)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.2	220.8	130.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.7	148.3	77.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.0	48.2	71.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.3	28.6	30.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.2	47.3	70.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information: TLV2379

THERMAL METRIC ⁽¹⁾		TLV2379	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Thermal Information: TLV4379

THERMAL METRIC ⁽¹⁾		TLV4379	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	52.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 Electrical Characteristics: $V_S = 1.8\text{ V to }5.5\text{ V}$

at $T_A = 25^\circ\text{C}$, $R_L = 25\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} < (V+) - 1\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5 V		0.8	2.5	mV
dV _{OS} /dT	V _{OS} drift	T _A = −40°C to +125°C		3		μV/°C
PSRR	Power-supply rejection ratio		92	104		dB
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range		(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio ⁽¹⁾	(V−) < V _{CM} < (V+) − 1 V	85	100		dB
		T _A = −40°C to +125°C, (V−) < V _{CM} < (V+) − 1 V	62			
INPUT BIAS CURRENT						
I _{IB}	Input bias current	V _S = 5 V, V _{CM} ≤ V _S / 2		±5		pA
I _{IO}	Input offset current	V _S = 5 V		±5		pA
INPUT IMPEDANCE						
	Differential			10 ¹³ 3		Ω pF
	Common-mode			10 ¹³ 6		Ω pF
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.8		μV _{PP}
e _n	Input voltage noise density	f = 1 kHz		83		nV/√Hz
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 5 V, R _L = 5 kΩ, 500 mV < V _O < (V+) − 500 mV	90	110		dB
OUTPUT						
	Voltage output swing from rail	R _L = 5 kΩ		25	50	mV
		T _A = −40°C to +125°C, R _L = 5 kΩ			75	
I _{SC}	Short-circuit current			±5		mA
C _{LOAD}	Capacitive load drive		See Capacitive Load and Stability section			
R _{OUT}	Closed-loop output impedance	G = 1, f = 1 kHz, I _O = 0		10		Ω
R _O	Open-loop output impedance	f = 100 kHz, I _O = 0		28		kΩ
FREQUENCY RESPONSE (C _{LOAD} = 30 pF)						
GBW	Gain bandwidth product			90		kHz
SR	Slew rate	G = 1		0.03		V/μs
	Overload recovery time	V _{IN} × Gain > V _S		25		μs
t _{ON}	Turn-on time			1		ms
POWER SUPPLY						
V _S	Specified, operating voltage range		1.8		5.5	V
I _Q	Quiescent current per amplifier	V _S = 5 V, T _A = −40°C to +125°C		4	12	μA
TEMPERATURE						
T _A	Specified, operating range		−40		125	°C
T _{stg}	Storage range		−65		150	°C

(1) See typical characteristic graph, *Common-Mode Rejection Ratio vs Frequency* ([Figure 2](#)).

7.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 25\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

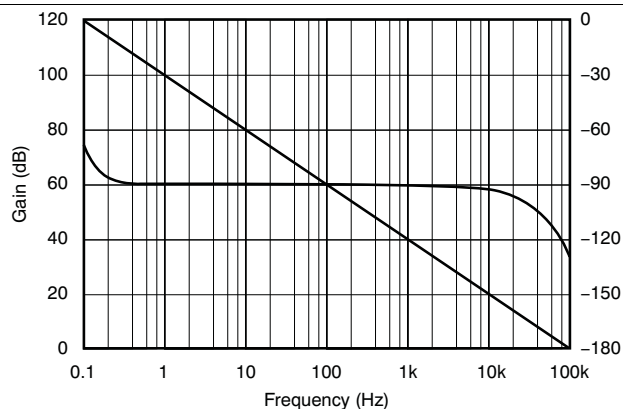


Figure 1. Open-Loop Gain and Phase vs Frequency

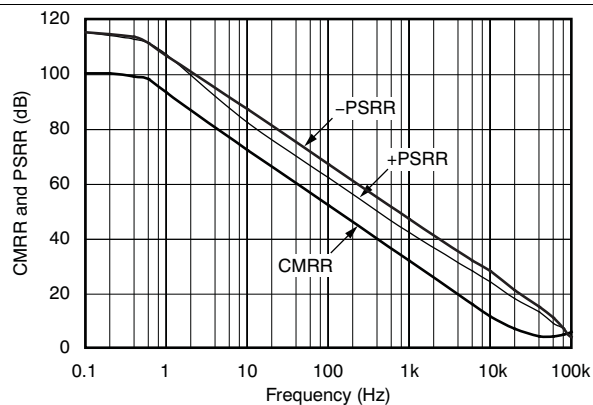


Figure 2. Common-Mode and Power-Supply Rejection Ratio vs Frequency

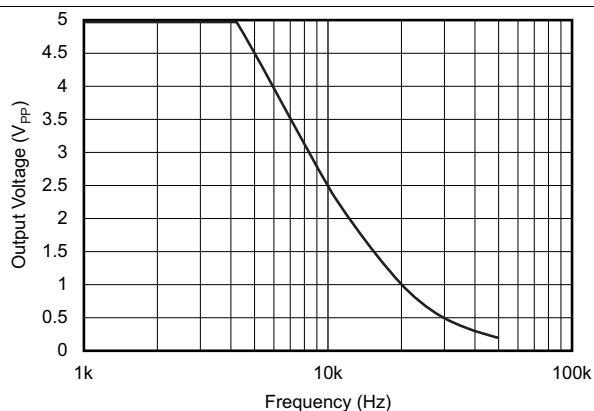


Figure 3. Maximum Output Voltage vs Frequency

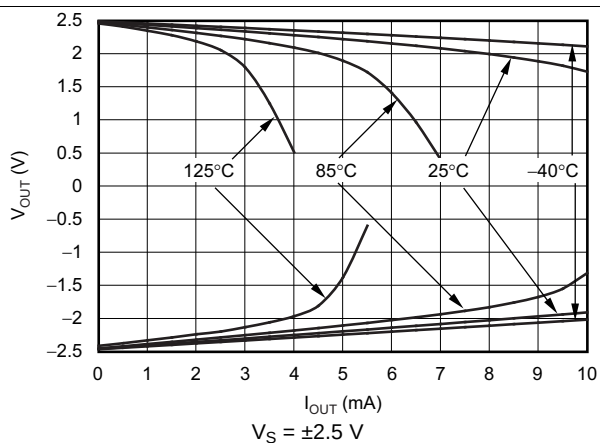


Figure 4. Output Voltage vs Output Current

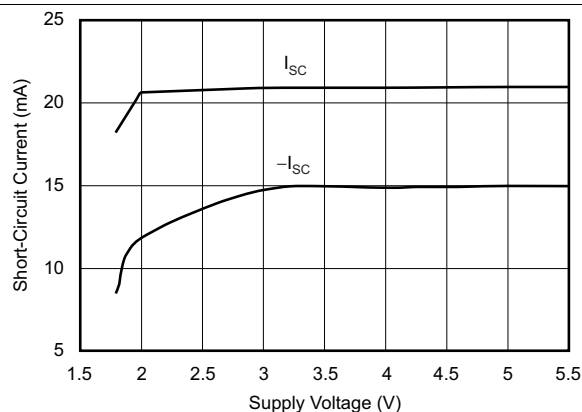


Figure 5. Short-Circuit Current vs Supply Voltage

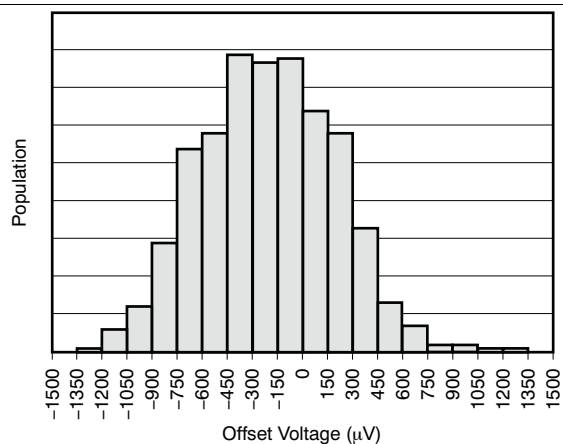


Figure 6. Offset Voltage Production Distribution

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 25\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

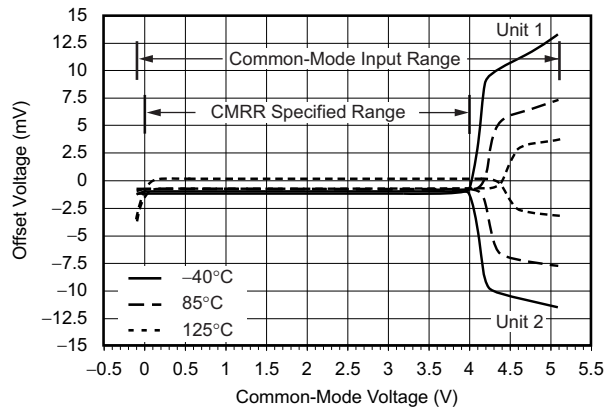


Figure 7. Offset Voltage vs Common-Mode Voltage and Temperature

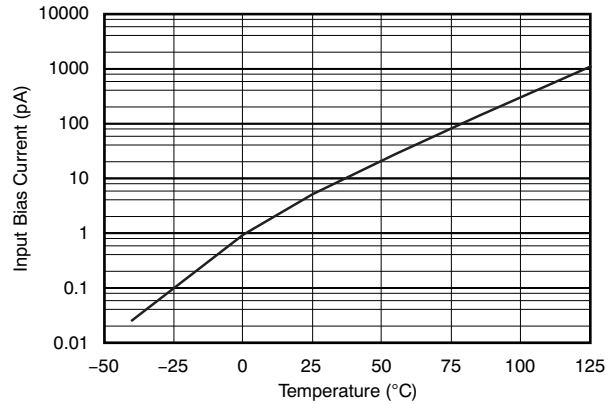


Figure 8. Input Bias Current vs Temperature

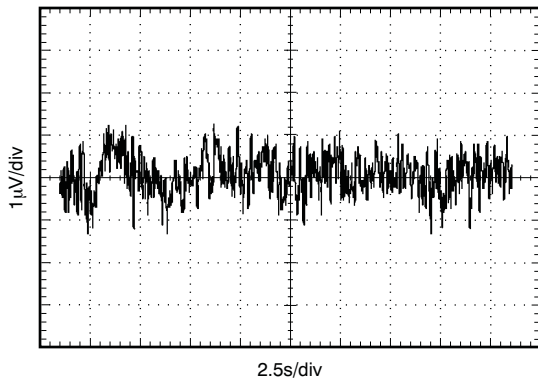


Figure 9. 0.1-Hz to 10-Hz Noise

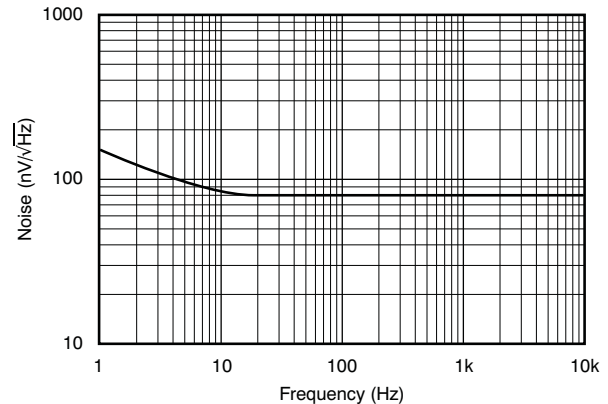


Figure 10. Noise vs Frequency

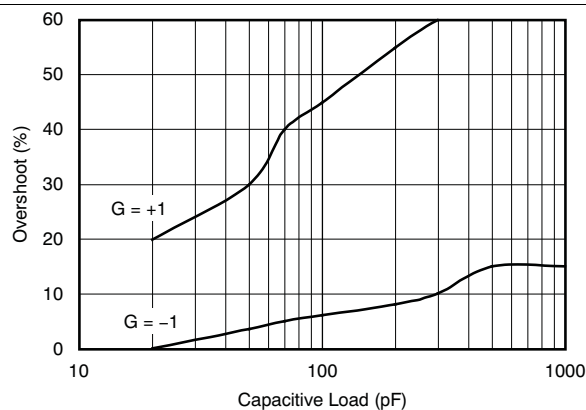


Figure 11. Small-Signal Overshoot vs Capacitive Load

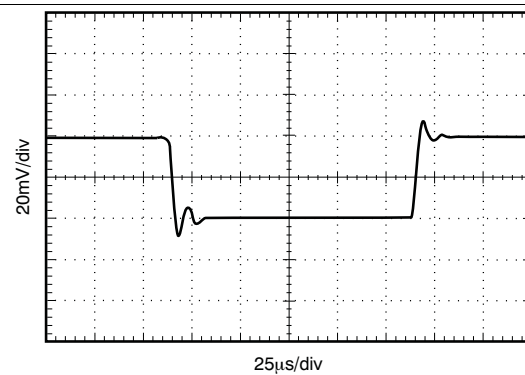


Figure 12. Small-Signal Step Response

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and $R_L = 25\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

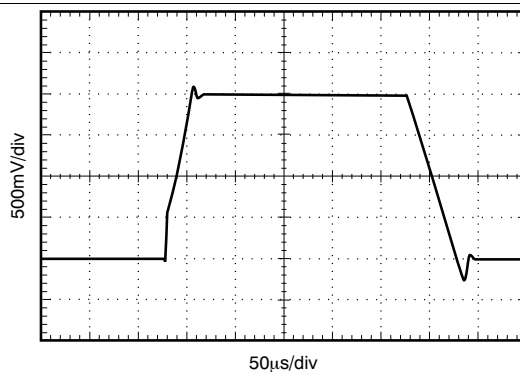


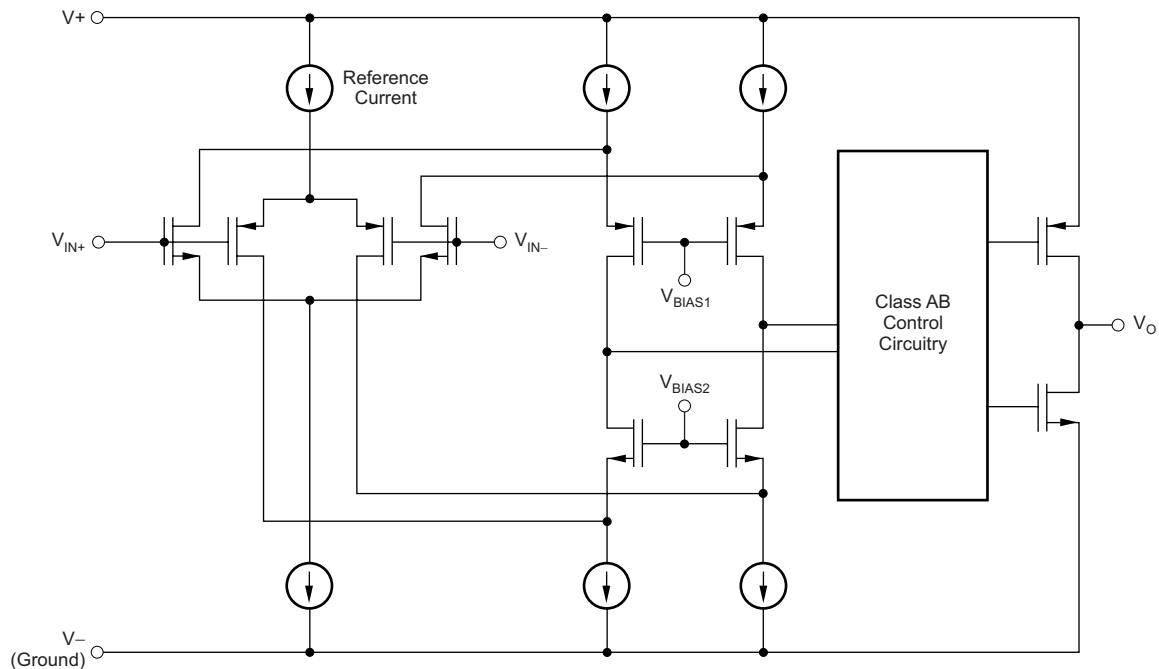
Figure 13. Large-Signal Step Response

8 Detailed Description

8.1 Overview

The TLV379 devices are a family of micropower, low-voltage, rail-to-rail input and output operational amplifiers designed for battery-powered applications. This family of amplifiers features impressive bandwidth (90 kHz), low bias current (5 pA), low noise (83 nV/√Hz), and consumes very low quiescent current of only 12 μA (maximum) per channel.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

The TLV379 series is fully specified and tested from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V). Parameters that vary with supply voltage are illustrated in the [Typical Characteristics](#) section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV379 family typically extends 100 mV beyond each supply rail. This rail-to-rail input is achieved using a complementary input stage. CMRR is specified from the negative rail to 1 V below the positive rail. Between $(V+) - 1$ V and $(V+) + 0.1$ V, the amplifier operates with higher offset voltage because of the transition region of the input stage. See the typical characteristic graph, *Offset Voltage vs Common-Mode Voltage vs Temperature* ([Figure 7](#)).

Feature Description (continued)

8.3.3 Rail-to-Rail Output

Designed as a micropower, low-noise operational amplifier, the TLV379 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 25 k Ω , the output typically swings to within 5 mV of either supply rail, regardless of the power-supply voltage applied.

8.3.4 Capacitive Load and Stability

Follower configurations with load capacitance in excess of 30 pF can produce extra overshoot (see the typical characteristic graph, *Small-Signal Overshoot vs Capacitive Load*, Figure 11) and ringing in the output signal. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20 Ω) resistor, R_S , in series with the output as shown in Figure 14. This resistor significantly reduces ringing and maintains direct current (dc) performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio of R_S / R_L and is generally negligible.

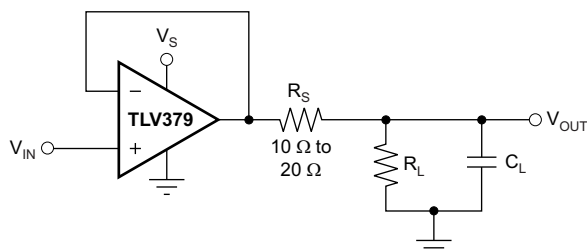


Figure 14. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the operational amplifier (op amp) input and the gain-setting resistors. Best performance is achieved by using smaller-value resistors. However, when large-value resistors cannot be avoided, a small (4 pF to 6 pF) capacitor (C_{FB}) can be inserted in the feedback, as shown in Figure 15. This configuration significantly reduces overshoot by compensating the effect of capacitance (C_{IN}) that includes the amplifier input capacitance (3 pF) and printed circuit board (PCB) parasitic capacitance.

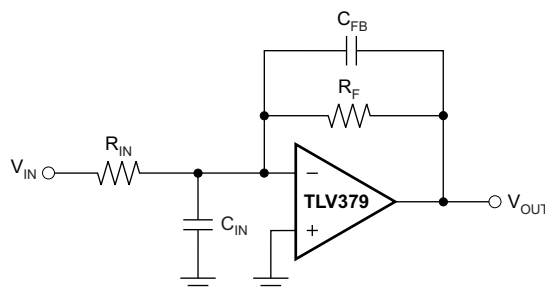


Figure 15. Improving Stability for Large R_F and R_{IN}

8.4 Device Functional Modes

The TLV379 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (± 0.9 V) and 5.5 V (± 2.75 V).

9 Application and Implementation

NOTE

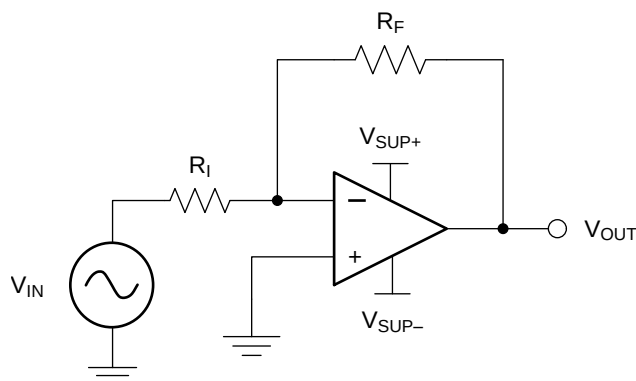
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing for ultra-low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors can react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in [Figure 16](#). An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F .



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Figure 16. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ± 0.5 V (1 V) to ± 1.8 V (3.6 V). Setting the supply at ± 2.5 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Typical Application (continued)

When the desired gain is determined, choose a value for R_1 or R_F . Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of kilohms) draw the smallest current but generate the highest noise. Very small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 k Ω for R_1 , meaning 36 k Ω is used for R_F . These values are determined by [Equation 3](#):

$$A_V = -\frac{R_F}{R_1} \quad (3)$$

9.2.3 Application Curve

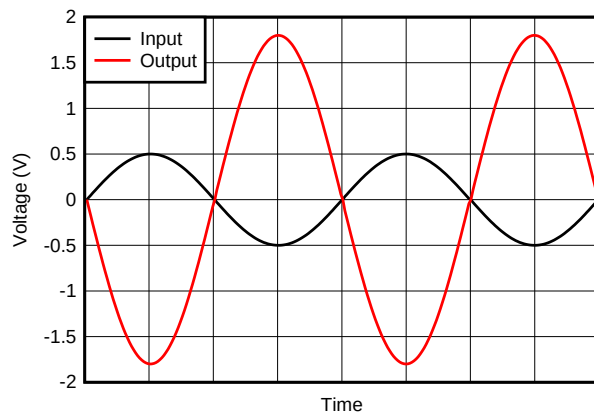


Figure 17. Inverting Amplifier Input and Output

9.3 System Examples

[Figure 18](#) shows the basic configuration for a bridge amplifier using the TLV379.

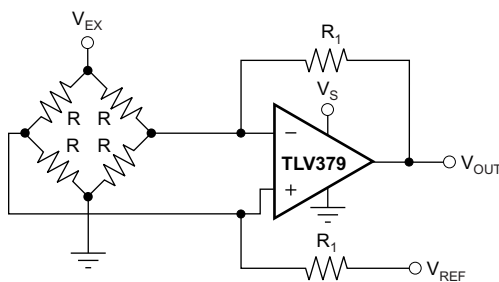


Figure 18. Single Op Amp Bridge Amplifier

System Examples (continued)

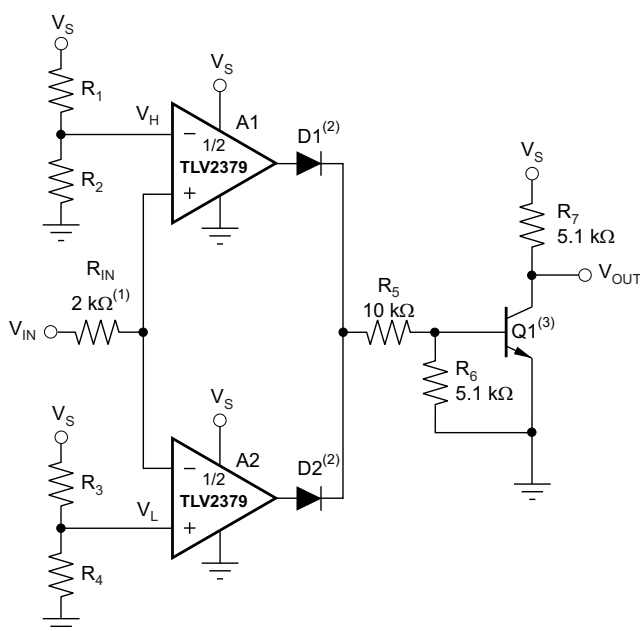
Figure 19 shows the TLV2379 used as a window comparator. The threshold limits are set by V_H and V_L , with $V_H > V_L$. When $V_{IN} < V_H$, the output of A1 is low. When $V_{IN} > V_L$, the output of A2 is low. Therefore, both op amp outputs are at 0 V as long as V_{IN} is between V_H and V_L . This architecture results in no current flowing through either diode, Q1 in cutoff, with the base voltage at 0 V, and V_{OUT} forced high.

If V_{IN} falls below V_L , the output of A2 is high, current flows through D2, and V_{OUT} is low. Likewise, if V_{IN} rises above V_H , the output of A1 is high, current flows through D1, and V_{OUT} is low.

The window comparator threshold voltages are set using Equation 4 and Equation 5.

$$V_H = \frac{R_2}{R_1 + R_2} \times V_S \quad (4)$$

$$V_L = \frac{R_4}{R_3 + R_4} \times V_S \quad (5)$$



- (1) R_{IN} protects A1 and A2 from possible excess current flow.
- (2) IN4446 or equivalent diodes.
- (3) 2N2222 or equivalent NPN transistor.

Figure 19. TLV2379 as a Window Comparator

10 Power Supply Recommendations

The TLV379 family is specified for operation from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the [Layout Guidelines](#) section.

10.1 Input and ESD Protection

The TLV379 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#) table. [Figure 20](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input that must be kept to a minimum in noise-sensitive applications.

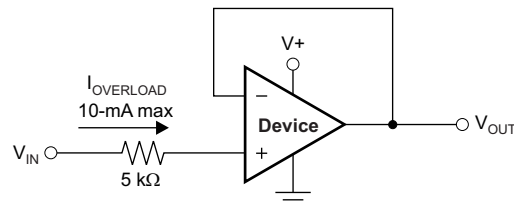


Figure 20. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V_+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close as possible to the device. Keep R_F and R_G close to the inverting input in order to minimize parasitic capacitance, as shown in [Figure 21](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

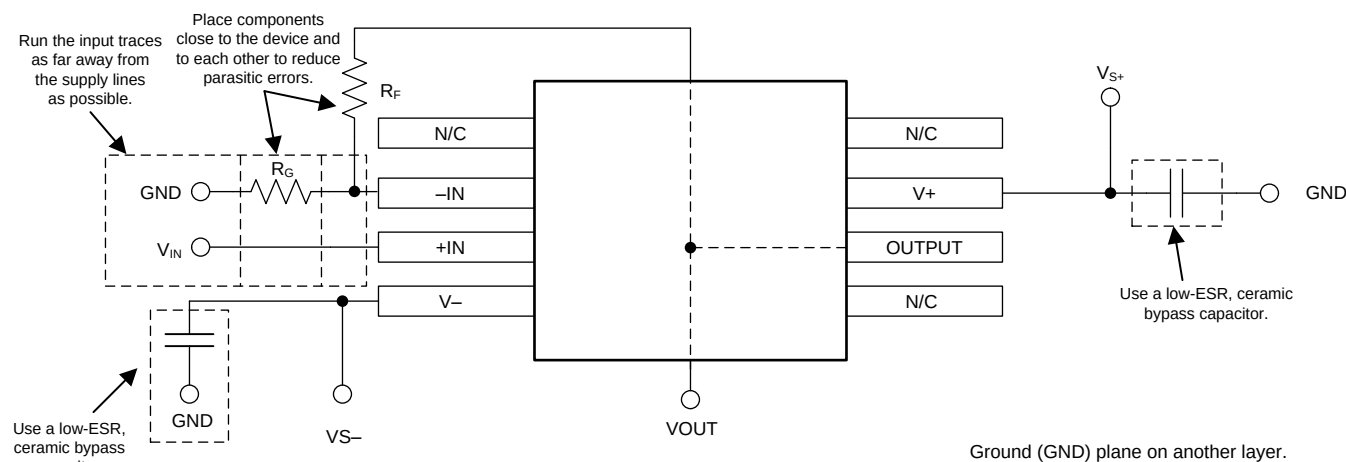


Figure 21. Operational Amplifier Board Layout for Noninverting Configuration

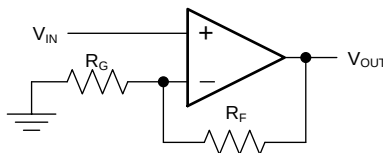


Figure 22. Schematic Representation of [Figure 21](#)

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- 『オペアンプのEMI除去率』(SBOA128)
- 『基板のレイアウト技法』(SLOA089)
- 『QFN/SONのPCB実装』(SLUA271)
- 『クワッド・フラットパック・リード端子なしロジック・パッケージ』(SCBA017)

12.2 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV379	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2379	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV4379	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2379IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2379
TLV2379IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2379
TLV379IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	12N
TLV379IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12N
TLV379IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	12N
TLV379IDBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12N
TLV379IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU POST- PLAT AG SPOT	Level-2-260C-1 YEAR	-40 to 125	12O
TLV379IDCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12O
TLV379IDCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12O
TLV379IDCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12O
TLV379IDCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU POST- PLAT AG SPOT	Level-2-260C-1 YEAR	-40 to 125	12O
TLV379IDCKT.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12O
TLV379IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 379
TLV379IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 379
TLV4379IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	TLV4379
TLV4379IPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4379

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

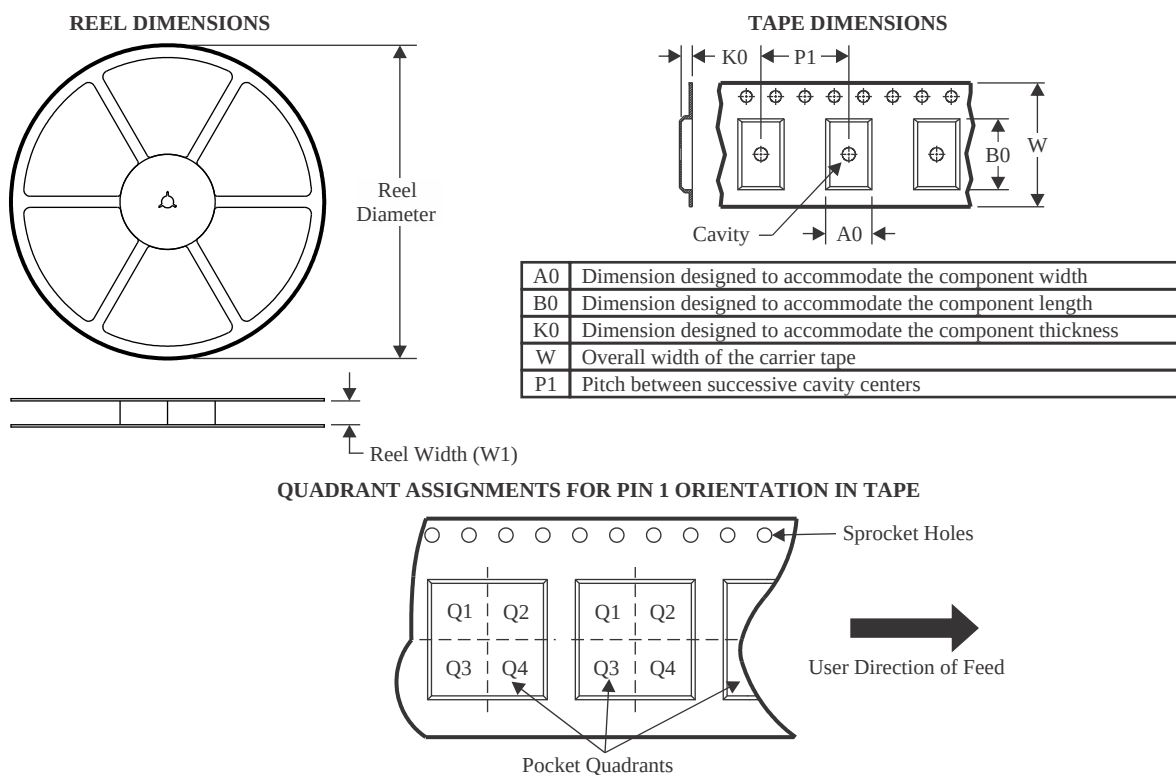
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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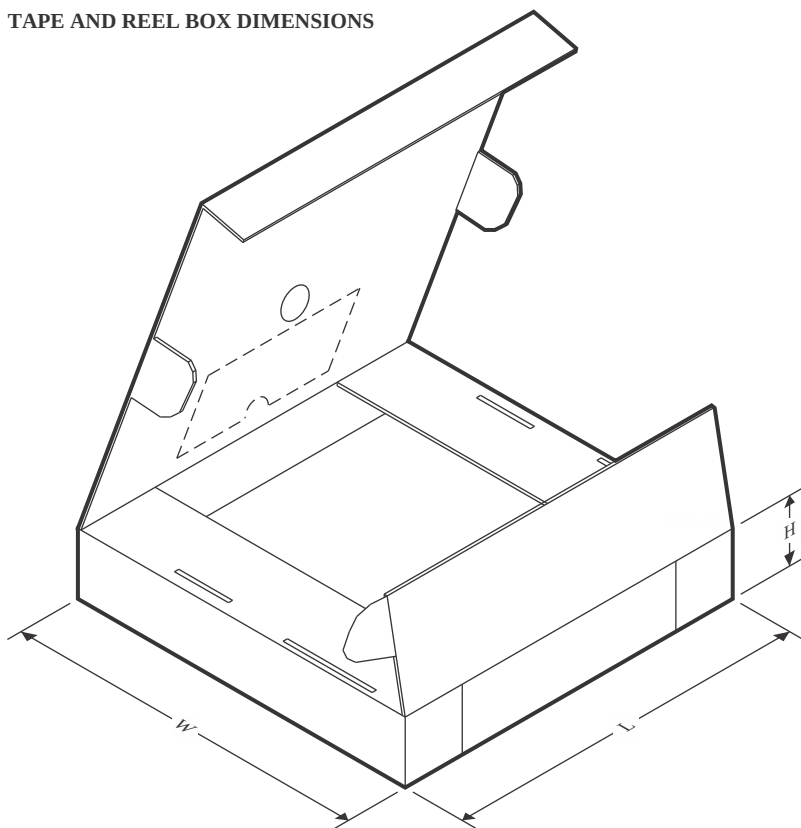
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2379IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV379IDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV379IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV379IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV379IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV379IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV379IDCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV379IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV379IDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV379IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4379IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV4379IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

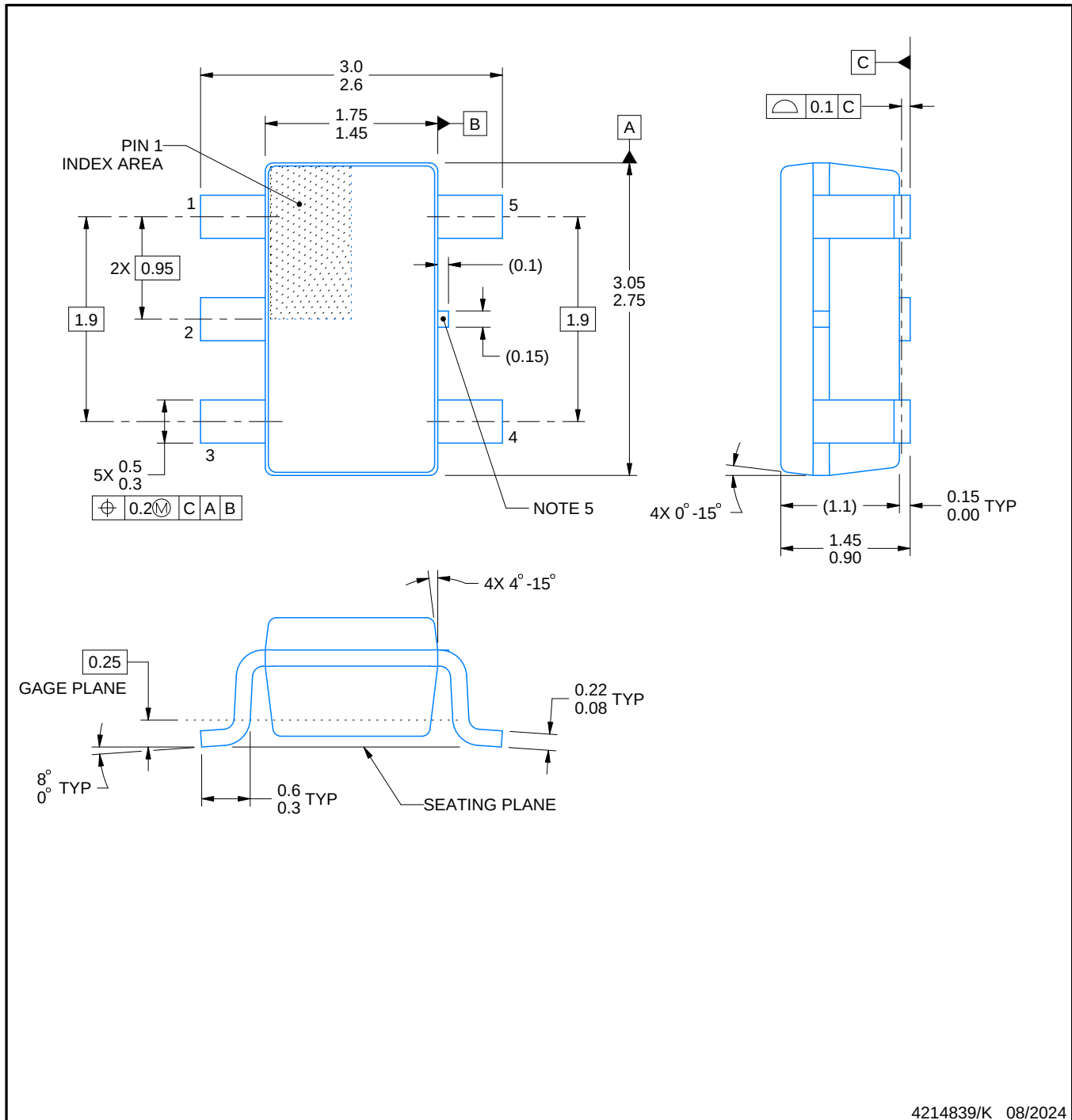


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2379IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV379IDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV379IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV379IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV379IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV379IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV379IDCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
TLV379IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV379IDCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV379IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV4379IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV4379IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

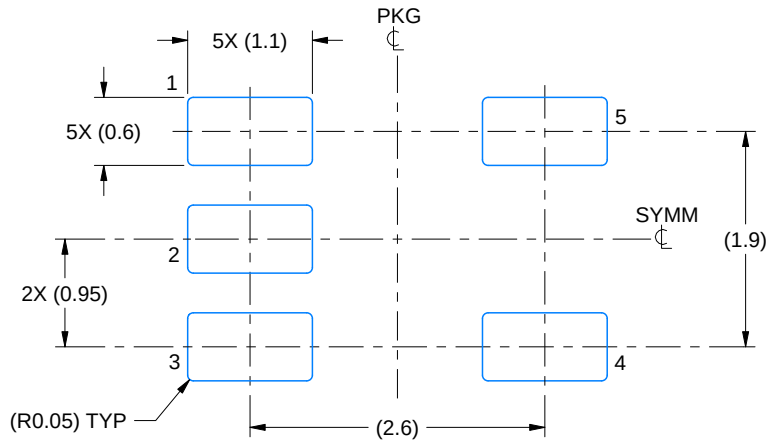
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

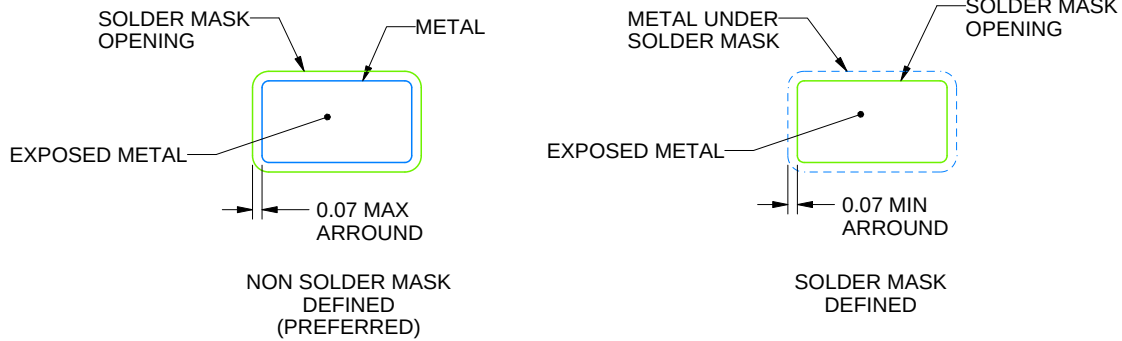
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

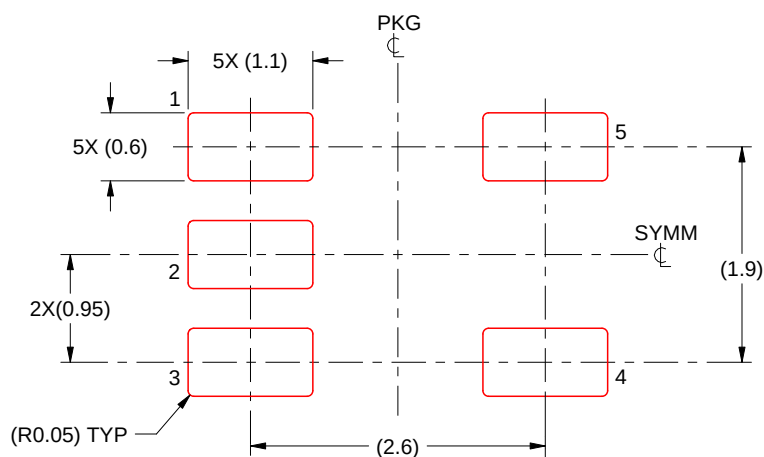
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

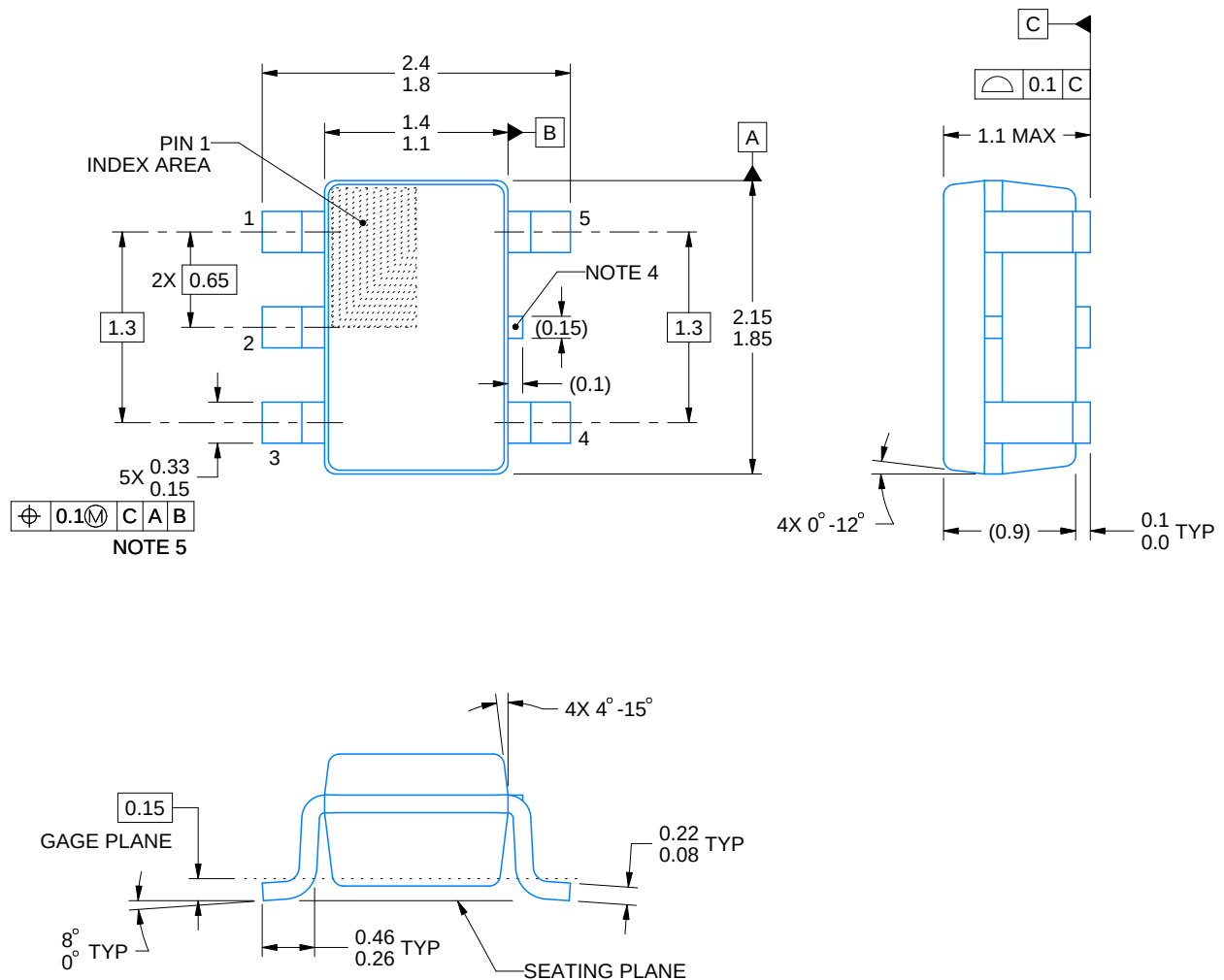
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK0005A

PACKAGE OUTLINE

SOT - 1.1 max height

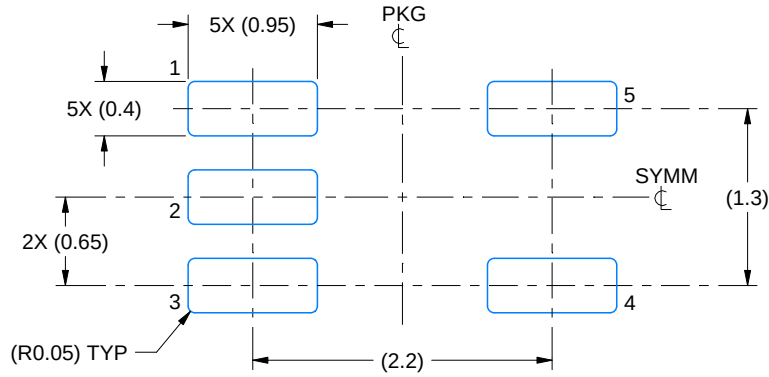
SMALL OUTLINE TRANSISTOR



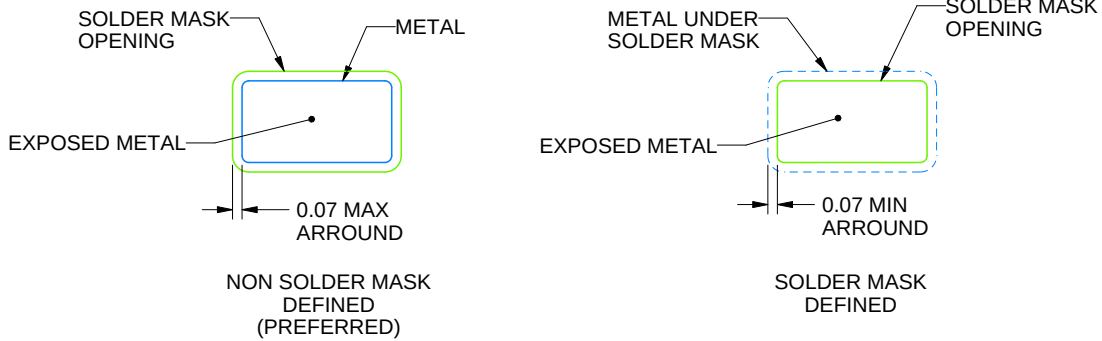
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

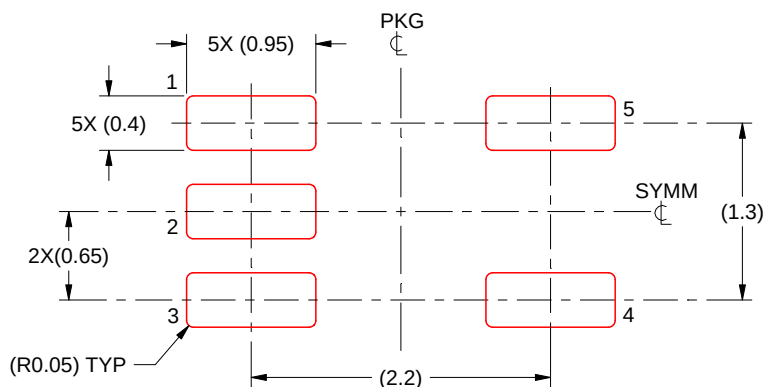


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214834/G 11/2024

NOTES: (continued)

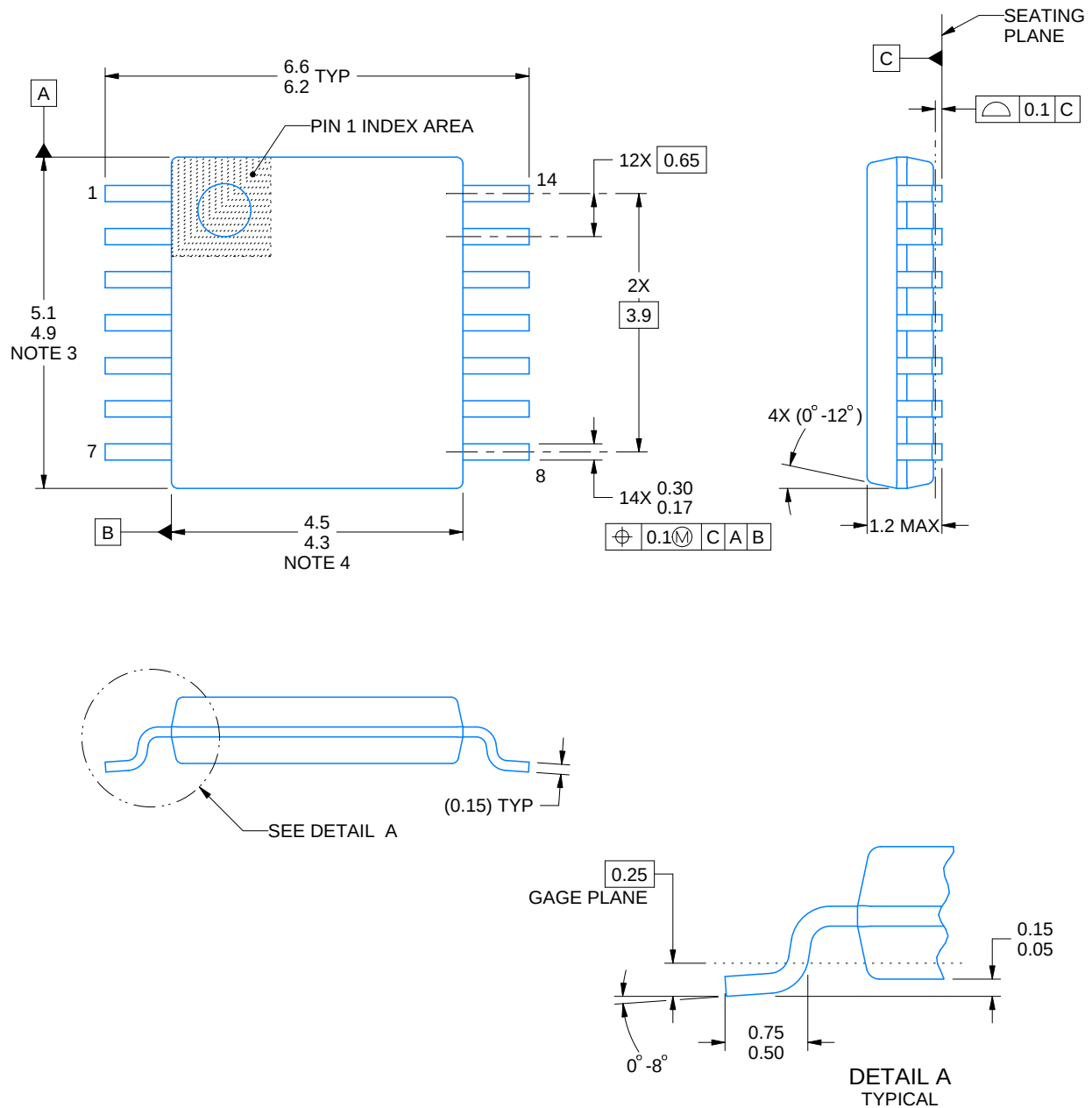
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

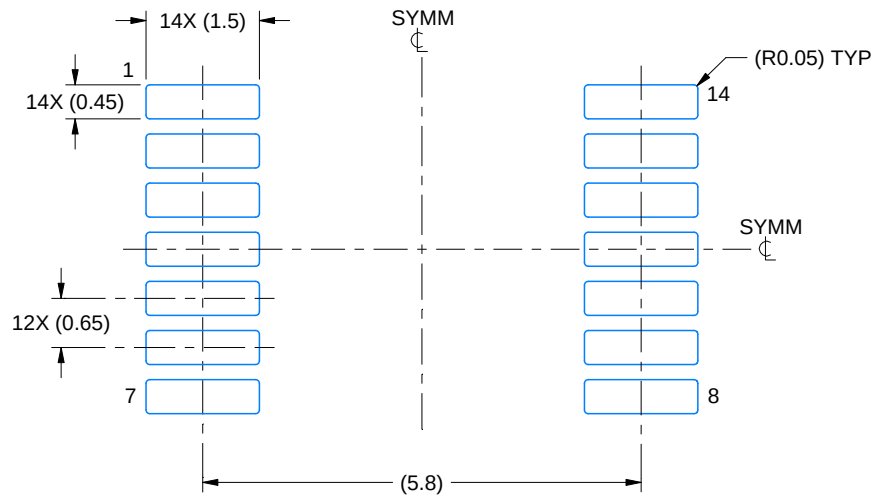
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

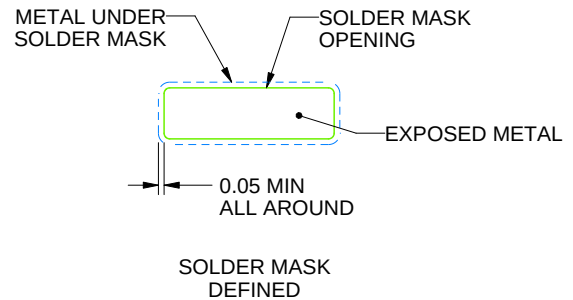
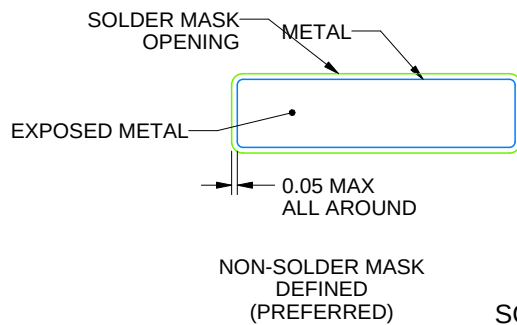
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

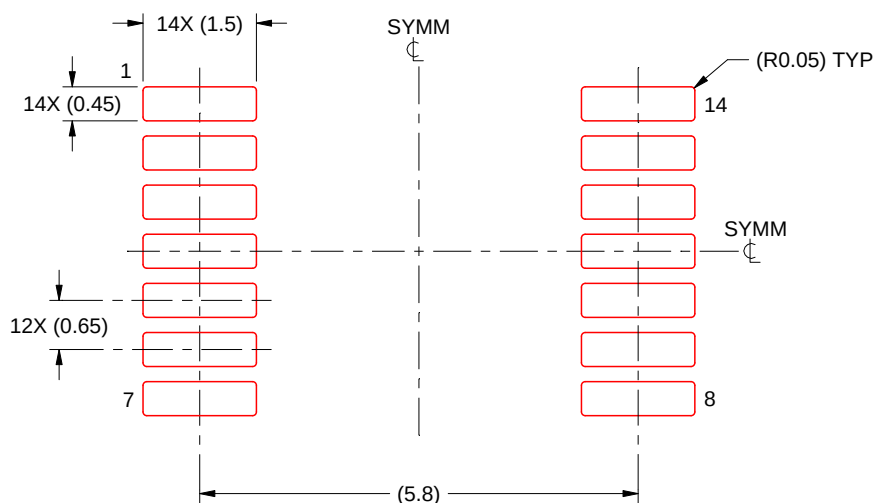
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

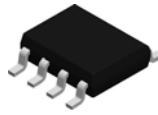


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

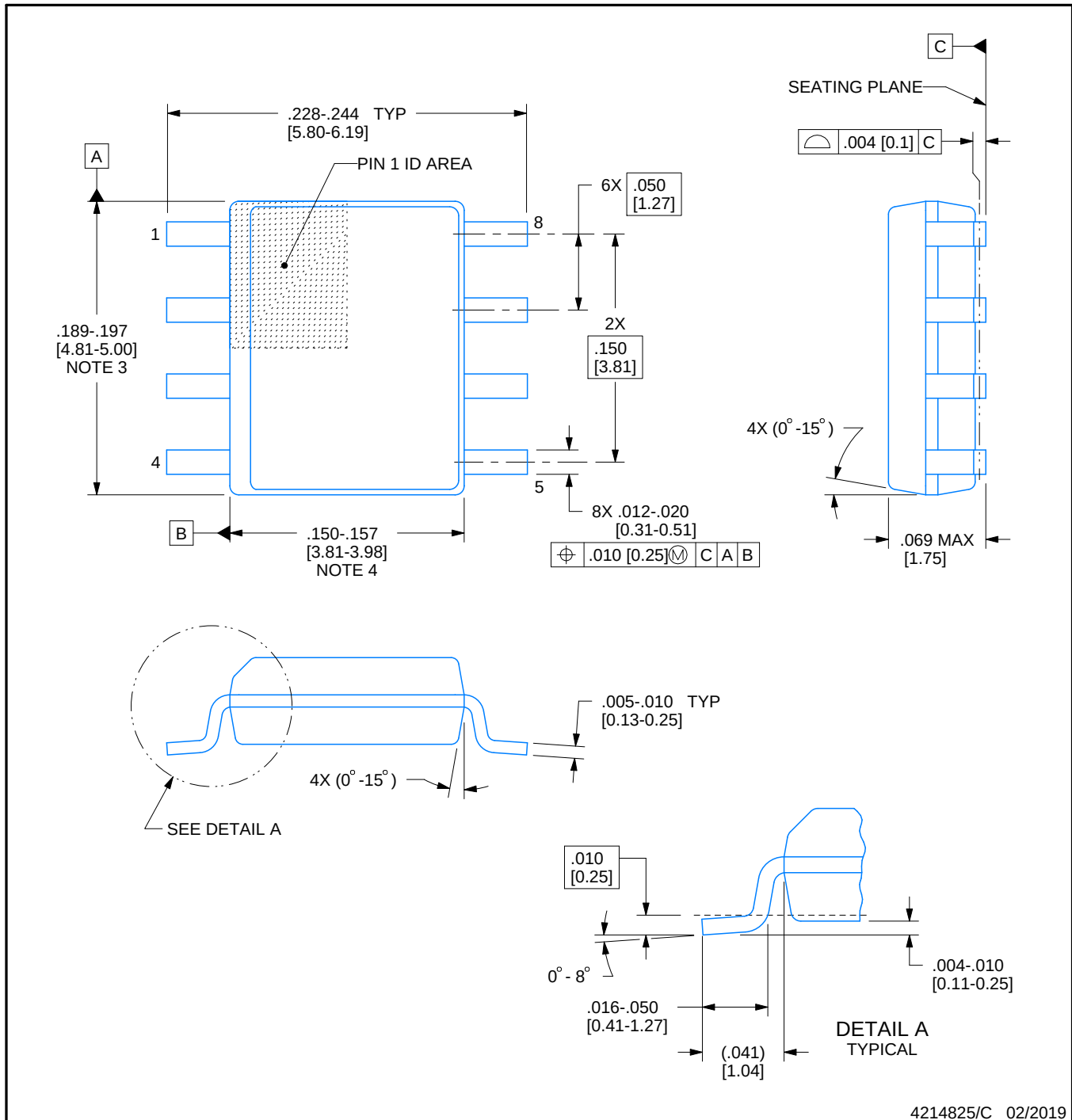
4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

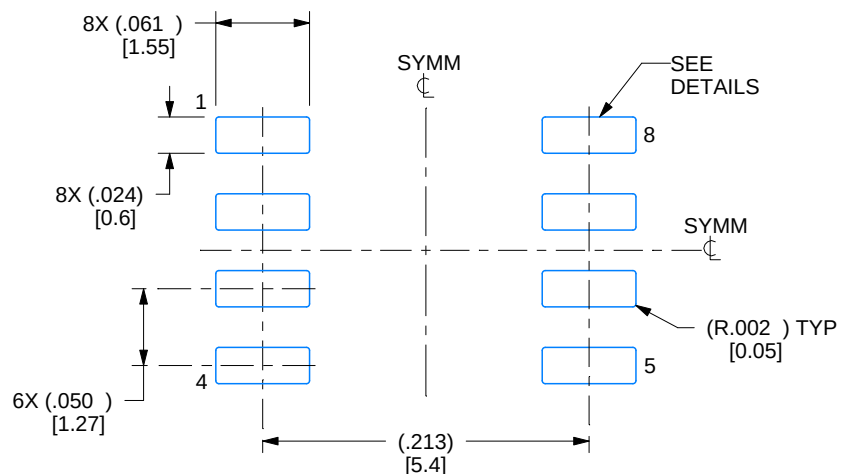
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

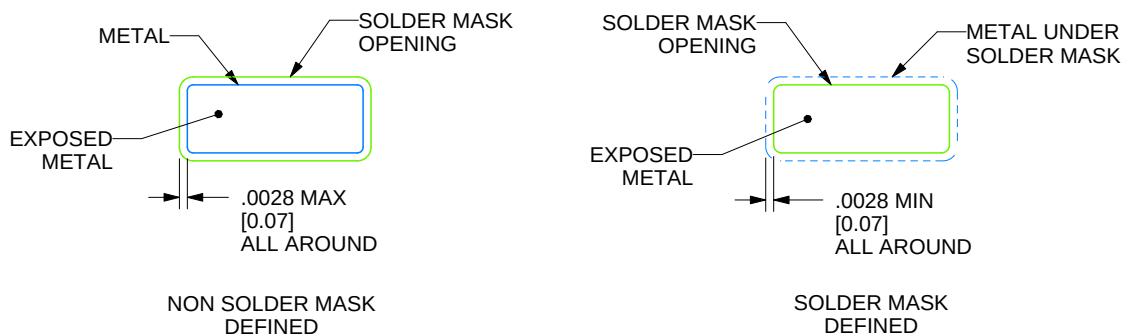
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

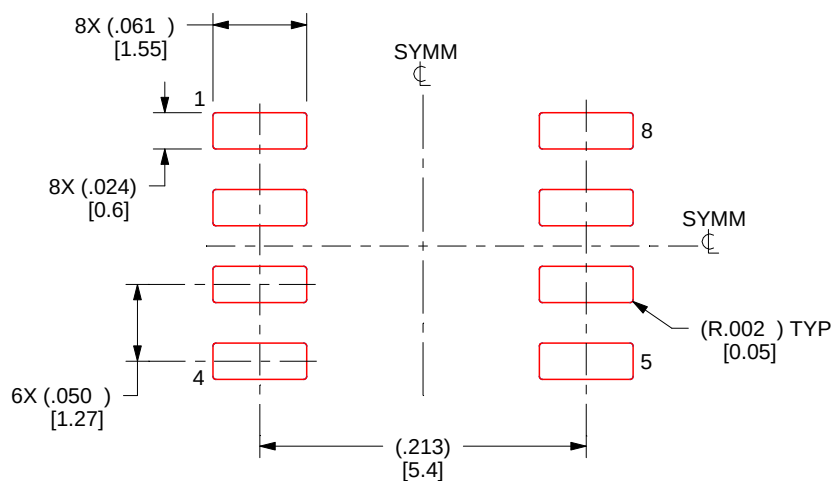
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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