TLVx172 低コストシステム用の 36V、単一電源、低消費電力オペアンプ

1 特長

- 電源電圧範囲: 4.5V～36V、±2.25V～±18V
- 低ノイズ: 9nV/√Hz
- 低いオフセット・ドリフト: ±1µV/℃(標準値)
- EMI強化
- 入力範囲は負の電源電圧にも対応
- レール・ツー・レール出力
- ゲイン帯域幅: 10MHz
- スルーレート: 10V/µs
- 低い静止電流: アンプごとに1.6mA
- 高い同相除去: 116dB (標準値)
- 低い入力バイアス電流: 10pA

2 アプリケーション

- TFT-LCD駆動回路
- タッチ・スクリーン・ディスプレイ
- ワイヤレスLAN
- 携帯機器
- A/Dコンバータ(ADC)バッファ
- アクティブ・フィルタ
- ライン・ドライバまたはライン・レシーバ
- 超音波
- 貨幣計数機
- トランスデューサ・アンプ

3 概要

TLVx172 ファミリの電磁気干渉 (EMI) 対策された 36V、単一電源、低ノイズ・オペアンプは、THD+N が 1kHz において 0.0002% で、4.5V (± 2.25V) から 36V (± 18V) までの電源で動作できます。このような特長に加え、TLVx172 は低ノイズで電源電圧除去比 (PSRR) も非常に高いことから、HEV/EV 自動車およびパワー・トレイン、医療機器などのアプリケーションで、マイクロボルト・レベルの信号を増幅するのに適しています。TLVx172 デバイスはオフセットおよびドリフトが小さく、10MHz の広い帯域幅を持ち、スルーレートは 10V/µs、温度範囲全体にわたって静止電流がわずか 2.3mA (最大値) です。

ほとんどのオペアンプは1つの電源電圧でのみ動作が規定されているのに対して、TLVx172 デバイスは 4.5V～36V の範囲で規定されており、電源レールの範囲外の入力信号でも位相反転を起こすことはありません。TLVx172 デバイスは、最大 300pF の容量性負荷で安定して動作します。通常の動作時に、入力は負のレールより 100mV下、および正のレールから2V以内で動作できます。なお、完全なレール・ツー・レール入力で、正のレールを100mV超えて動作しますが、正のレールから2V以内では性能が低下します。

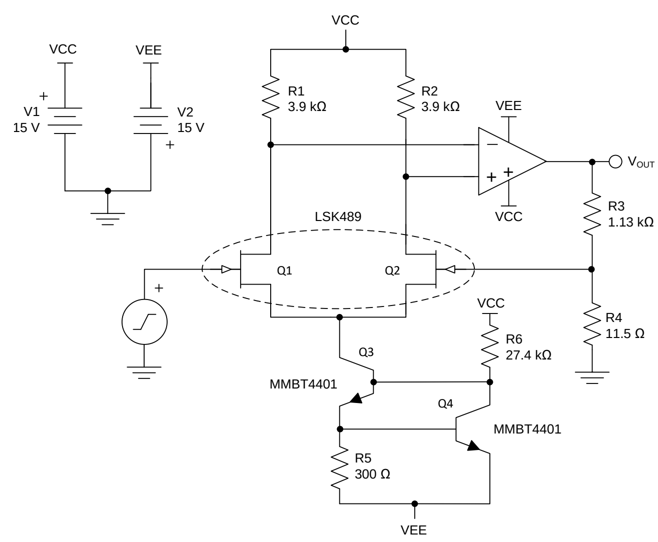
TLVx172 オペアンプは、-40°C～+125°C での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV172	SOIC (8)	4.90mm×3.91mm
	SC70 (5)	2.00mm×1.25mm
	SOT-23 (5)	2.90mm×1.60mm
TLV2172	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm
TLV4172	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



English Data Sheet: SBOS784

目次

4 改訂履歴

Revision B (September 2018) から **Revision C** に変更 — **Page**

- データシートのタイトルを「TLV2172 ...36V、単一電源、低消費電力...」から「TLVx172 ...36V、単一電源、低消費電力..」に変更 .. 1

Revision A (May 2018) から **Revision B** に変更 — **Page**

- Deleted the *Device Family Comparison* table ... 3
- Added the 5-pin SC70 and SOT-23, and the 8-pin SOIC pinout diagrams to the data sheet ... 4
- Added TLV172 Pin Functions table to the data sheet ... 4
- Added 14-pin SOIC and TSSOP pinout diagram to the data sheet ... 6

2016年11月発行のものから更新 — **Page**

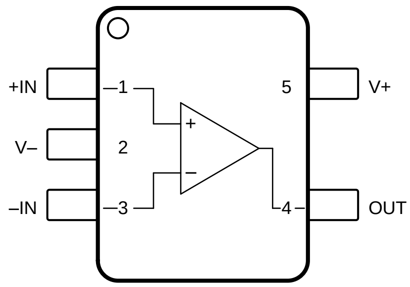
- Updated supply voltage values in *Absolute Maximum Ratings* table ... 7

5 Device Comparison Table

DEVICE	PACKAGE
TLV172 (single)	SC70-5, SOT-23-5, SOIC-8
TLV2172 (dual)	SOIC-8, VSSOP-8
TLV4172 (quad)	SOIC-14, TSSOP-14

6 Pin Configuration and Functions

TLV172 DCK Package
5-Pin SC70
Top View



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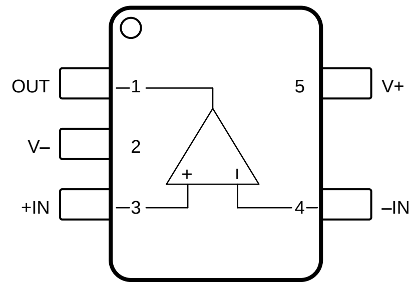
TLV172 DBV Package
5-Pin SOT-23
Top View



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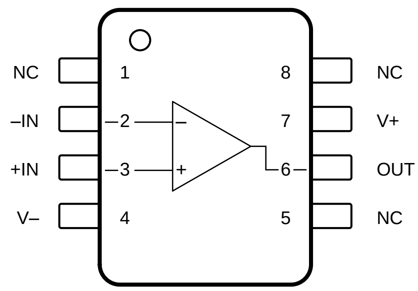
TLV172 D Package
8-Pin SOIC
Top View



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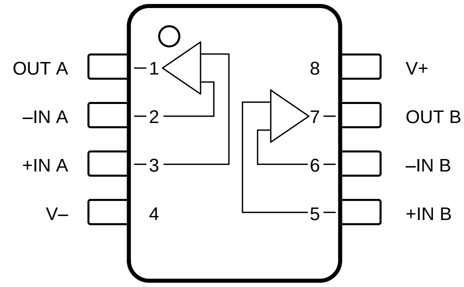
NC- no internal connection

Pin Functions: TLV172

PIN				I/O	DESCRIPTION
NAME	SC70	SOT-23	SOIC		
–IN	3	4	2	I	Negative (inverting) input
+IN	1	3	3	I	Positive (noninverting) input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V–	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

TLV2172 D and DGK Packages
8-Pin SOIC and VSSOP
Top View



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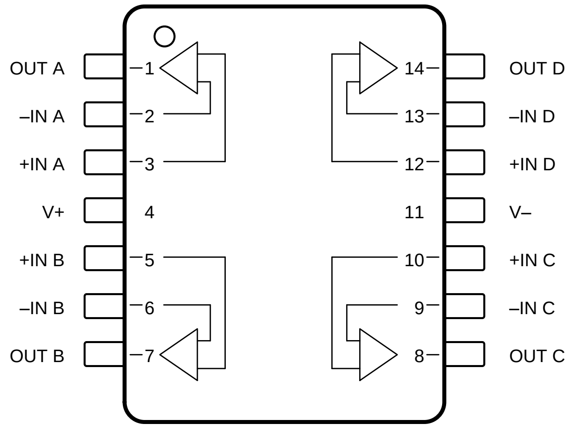
Pin Functions: TLV2172

PIN			I/O	DESCRIPTION
NAME	SOIC (D)	VSSOP (DGK)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

TLV4172 D and PW Packages
14-Pin SOIC and TSSOP
Top View



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Pin Functions: TLV4172

PIN			I/O	DESCRIPTION
NAME	SOIC (D)	TSSOP (PW)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	9	9	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Voltage	Supply voltage, [(V+) – (V−)]			40	V
	Single-supply voltage			40	
	Signal input pin[2]	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential[3]	–0.5	0.5	
Current	Signal input pin		–10	10	mA
	Output short-circuit[4]		Continuous		
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
(3) See the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, (V+) – (V–)	Single-supply	4.5		36	V
	Dual-supply	±2.25		±18	
Specified temperature		–40		125	°C

7.4 Thermal Information: TLV172

THERMAL METRIC(1)		TLV172			UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.5	227.9	285.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.6	115.7	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	65.9	78.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.0	10.7	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.6	65.3	77.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: TLV2172

THERMAL METRIC(1)		TLV2172		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: TLV4172

THERMAL METRIC(1)		TLV4172		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.7	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	54.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	T_A = 25°C			0.5	1.7	mV
		T_A = –40°C to +125°C				2	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, T_A = –40°C to +125°C		100	120		dB
	Channel separation, dc				5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±10		pA
I_{OS}	Input offset current	T_A = 25°C			±2		pA
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.5		$µV_{PP}$
e_n	Input voltage noise density	f = 100 Hz			14		$nV/\sqrt{Hz}$
		f = 1 kHz			9		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz			1.6		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range (1)			(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		94	116		dB
INPUT IMPEDANCE							
	Differential				100 || 4		MΩ || pF
	Common-mode				6 || 4		10^{13} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, T_A = –40°C to +125°C		97	115		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +125°C			107		
FREQUENCY RESPONSE							
GBP	Gain bandwidth product				10		MHz
SR	Slew rate	G = +1			10		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step			2		µs
		To 0.01% (12-bit), V_S = ±18 V, G = +1, 10-V step			3.2		
	Overload recovery time	V_{IN} × gain > V_S			200		ns
THD+N	Total harmonic distortion + noise	V_S = 36 V, G = +1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.0002%		
OUTPUT							
V_O	Voltage output swing from rail	V_S = ±18 V, R_L = 10 kΩ	T_A = 25°C		70		mV
			T_A = –40°C to +125°C		95		
		V_S = ±18 V, R_L = 2 kΩ	T_A = 25°C		330	400	
			T_A = –40°C to +125°C		470	530	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A			60		Ω
POWER SUPPLY							
V_S	Specified voltage range			4.5		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = –40°C to +125°C			1.6	2.3	mA

(1) The input range can be extended beyond (V+) – 2 V up to V+. See the *Typical Characteristics* and *Application and Implementation* sections for additional information.

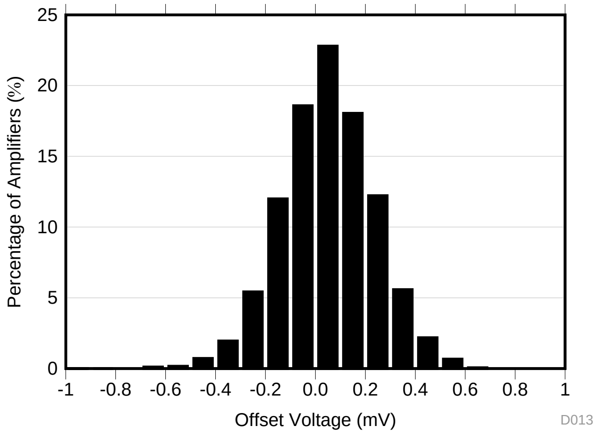
7.8 Typical Characteristics

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

表 1. Characteristic Performance Measurements

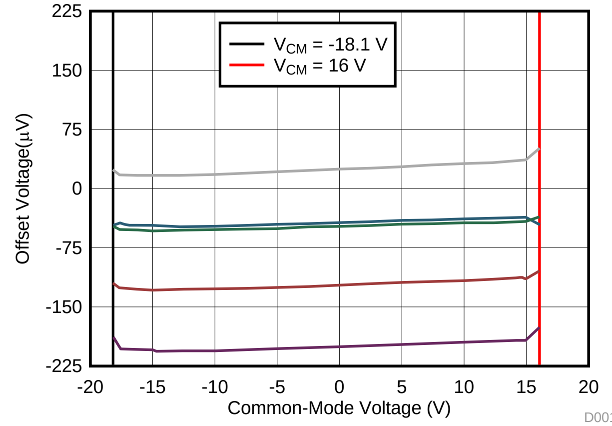
DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage vs Common-Mode Voltage	図 2
Offset Voltage vs Common-Mode Voltage (Upper Stage)	図 3
Input Bias Current vs Temperature	図 4
Output Voltage Swing vs Output Current (Maximum Supply)	図 5
CMRR and PSRR vs Frequency (Referred-to-Input)	図 6
0.1-Hz to 10-Hz Noise	図 7
Input Voltage Noise Spectral Density vs Frequency	図 8
Quiescent Current vs Supply Voltage	図 9
Open-Loop Gain and Phase vs Frequency	図 10
Closed-Loop Gain vs Frequency	図 11
Open-Loop Output Impedance vs Frequency	図 12
Small-Signal Overshoot vs Capacitive Load	図 13, 図 14
No Phase Reversal	図 15
Small-Signal Step Response (10 mV)	図 16, 図 17
Large-Signal Step Response	図 18, 図 19
Large-Signal Settling Time	図 20, 図 21
Short-Circuit Current vs Temperature	図 22
Maximum Output Voltage vs Frequency	図 23
EMIRR IN+ vs Frequency	図 24

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



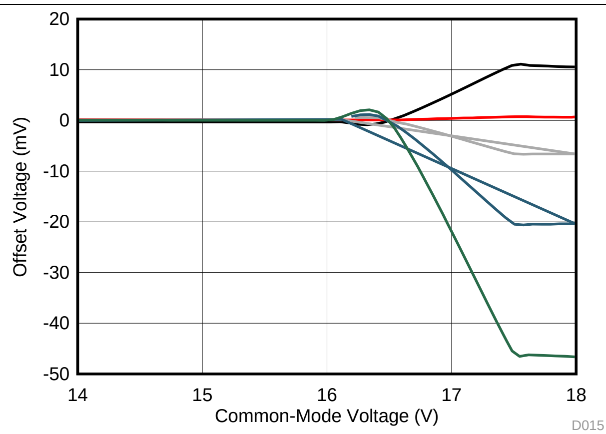
Distribution taken from 5185 amplifiers

図 1. Offset Voltage Production Distribution Histogram



5 typical units shown, V_S = ±18 V

図 2. Offset Voltage vs Common-Mode Voltage



5 typical units shown, V_S = ±18 V

図 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)

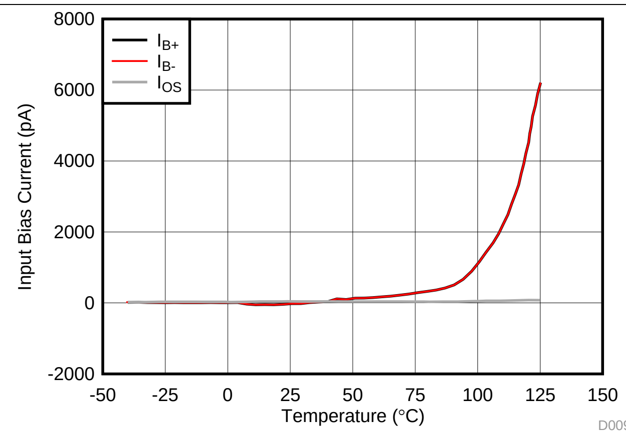


図 4. Input Bias Current vs Temperature

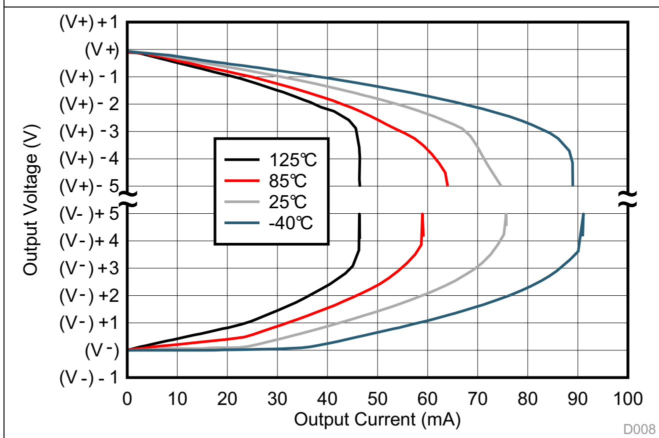


図 5. Output Voltage Swing vs Output Current (Maximum Supply)

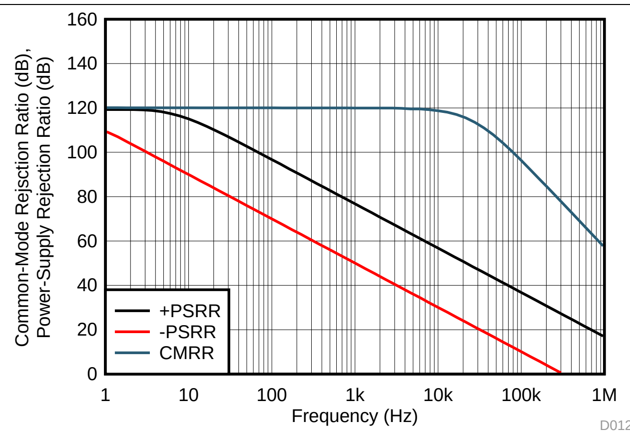


図 6. CMRR and PSRR vs Frequency (Referred-to-Input)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

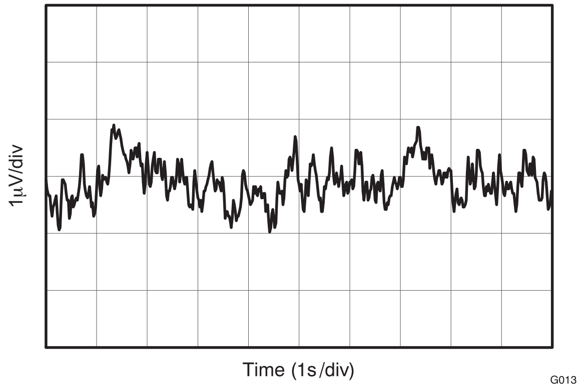


図 7. 0.1-Hz to 10-Hz Noise

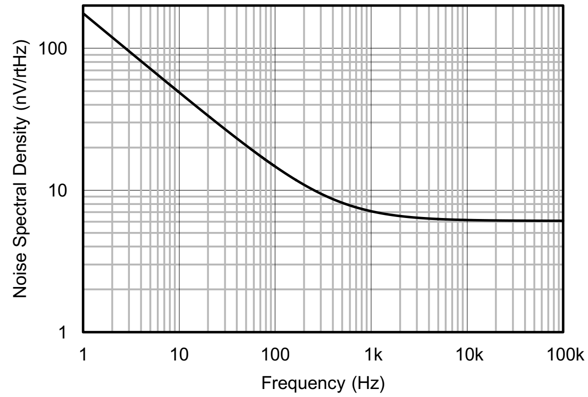


図 8. Input Voltage Noise Spectral Density vs Frequency

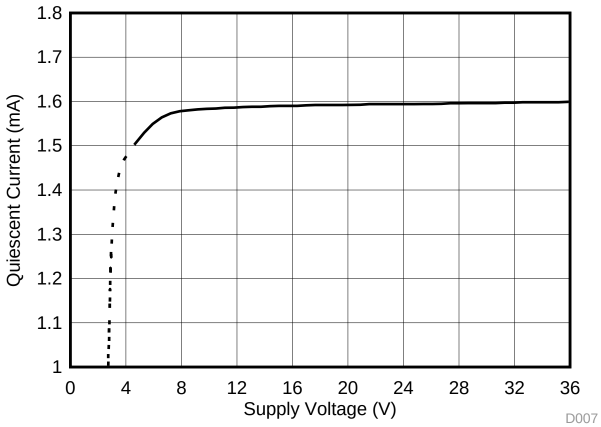


図 9. Quiescent Current vs Supply Voltage

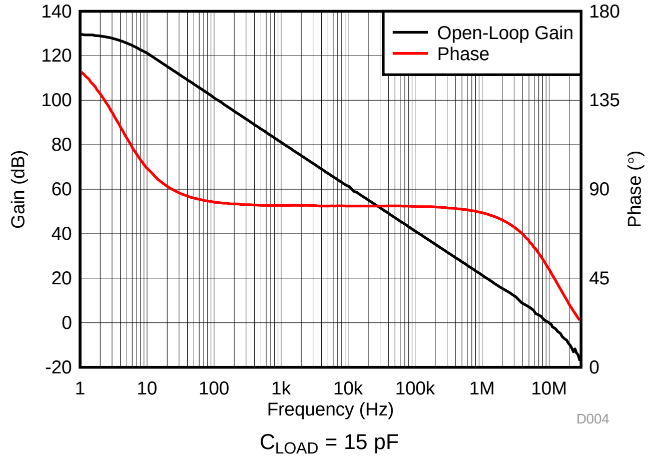


図 10. Open-Loop Gain and Phase vs Frequency

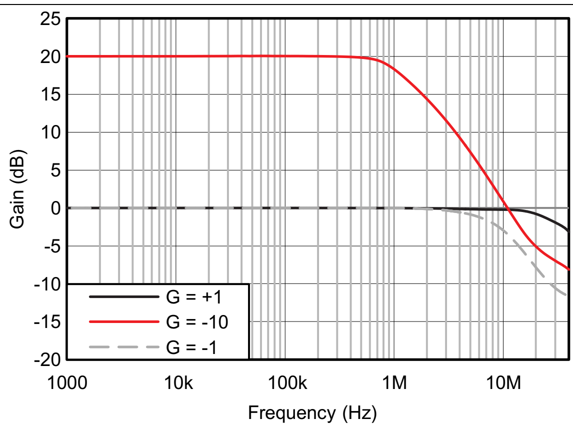


図 11. Closed-Loop Gain vs Frequency

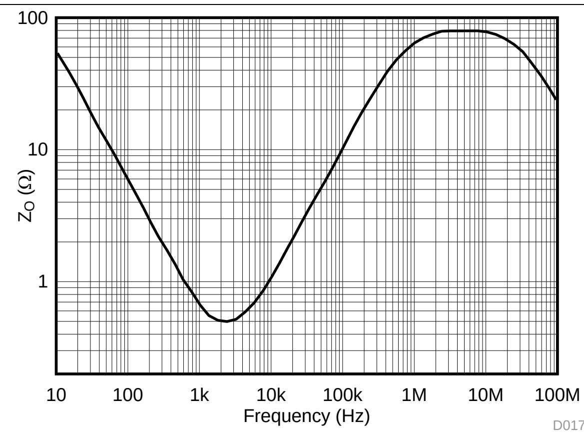
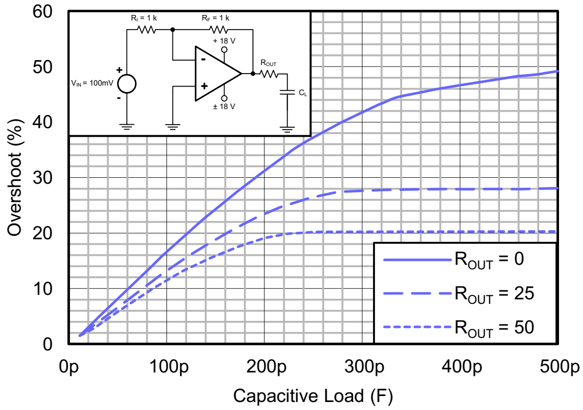


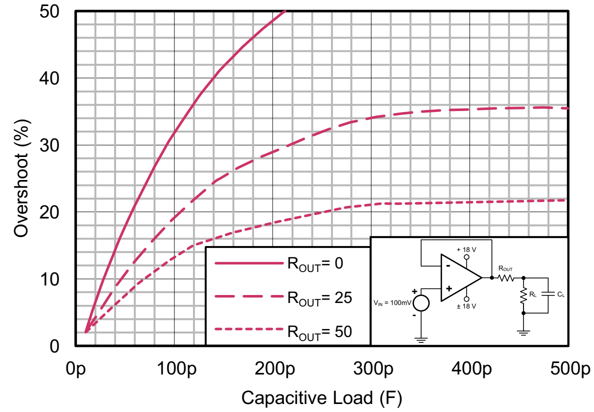
図 12. Open-Loop Output Impedance vs Frequency

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



100-mV output step, G = –1

図 13. Small-Signal Overshoot vs Capacitive Load



100-mV output step, G = 1

図 14. Small-Signal Overshoot vs Capacitive Load

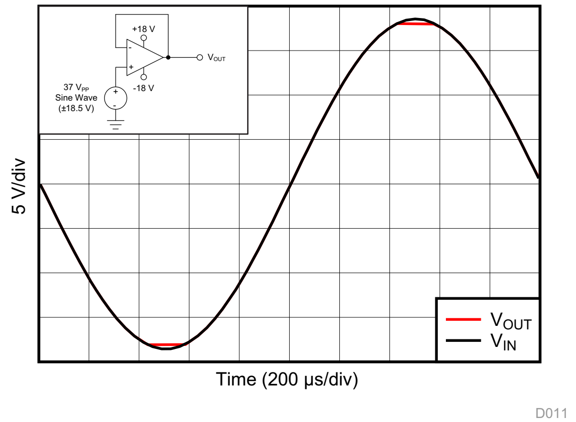
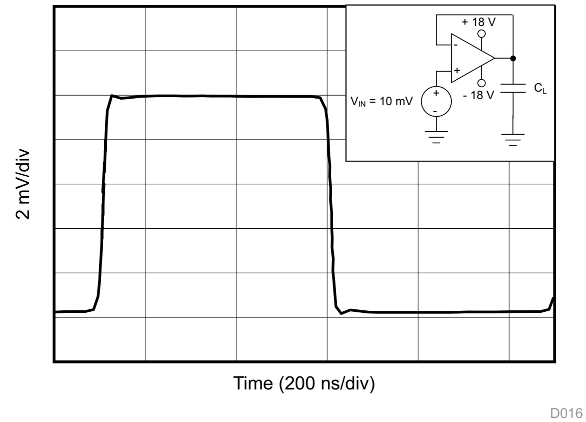
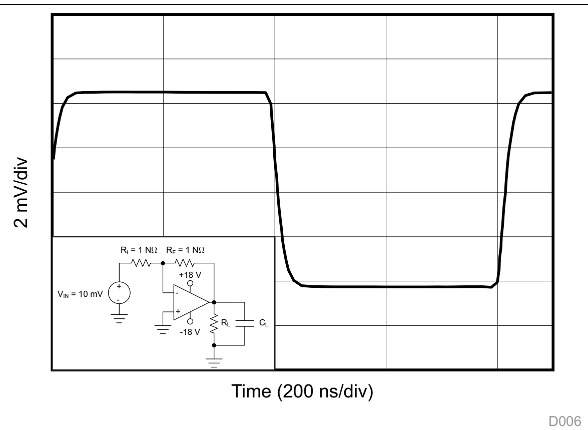


図 15. No Phase Reversal



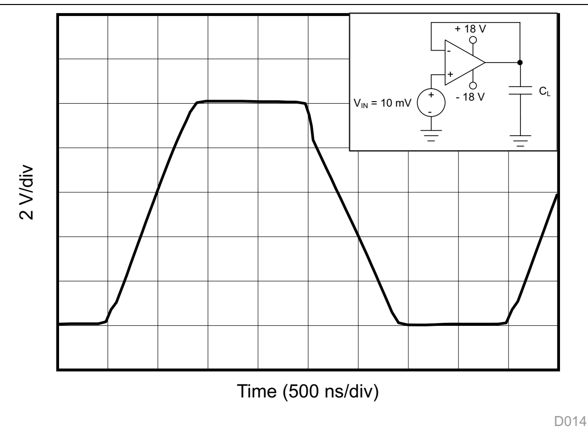
C_L = 10 pF 10-mV step

図 16. Small-Signal Step Response



R_L = 1 kΩ C_L = 10 pF 10-mV step

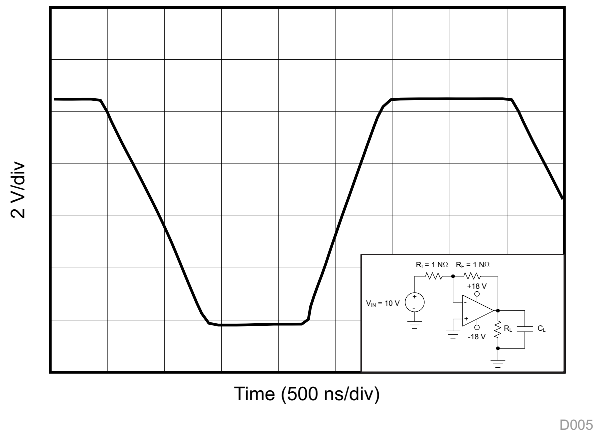
図 17. Small-Signal Step Response



C_L = 10 pF

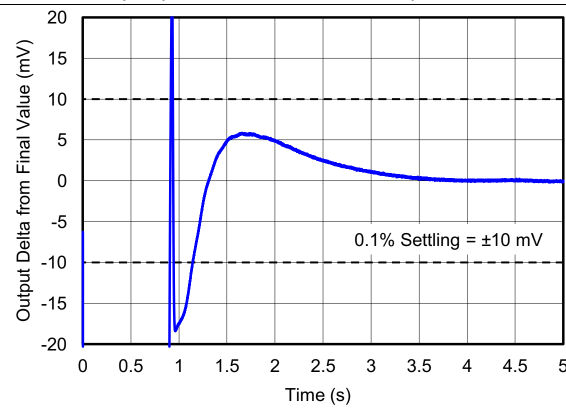
図 18. Large-Signal Step Response

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



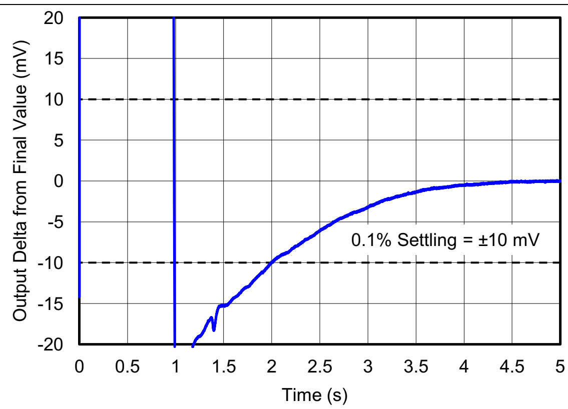
R_L = 1 kΩ　　C_L = 10 pF

図 19. Large-Signal Step Response



10-V positive step　　G = 1　　C_L = 10 pF

図 20. Large-Signal Settling Time



10-V negative step　　G = 1　　C_L = 10 pF

図 21. Large-Signal Settling Time

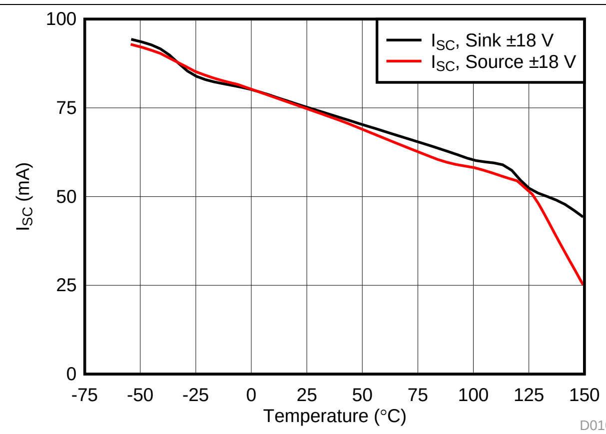


図 22. Short-Circuit Current vs Temperature

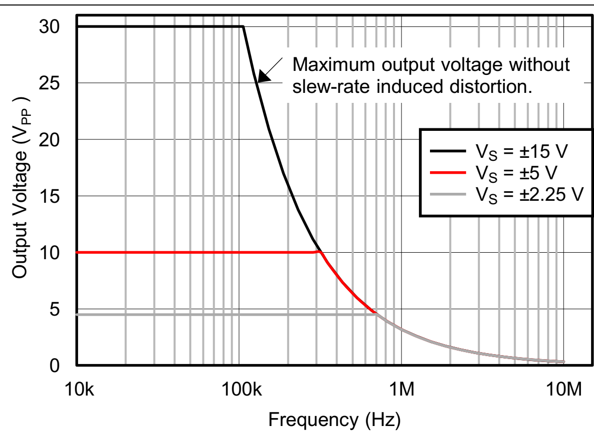
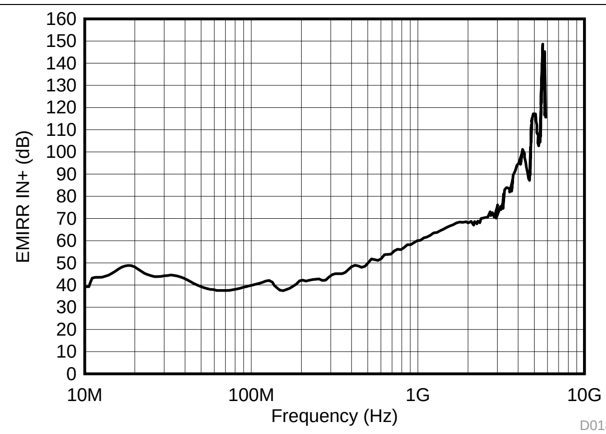


図 23. Maximum Output Voltage vs Frequency



P_{RF} = –10 dBm　　V_{SUPPLY} = ±18 V　　V_{CM} = 0 V

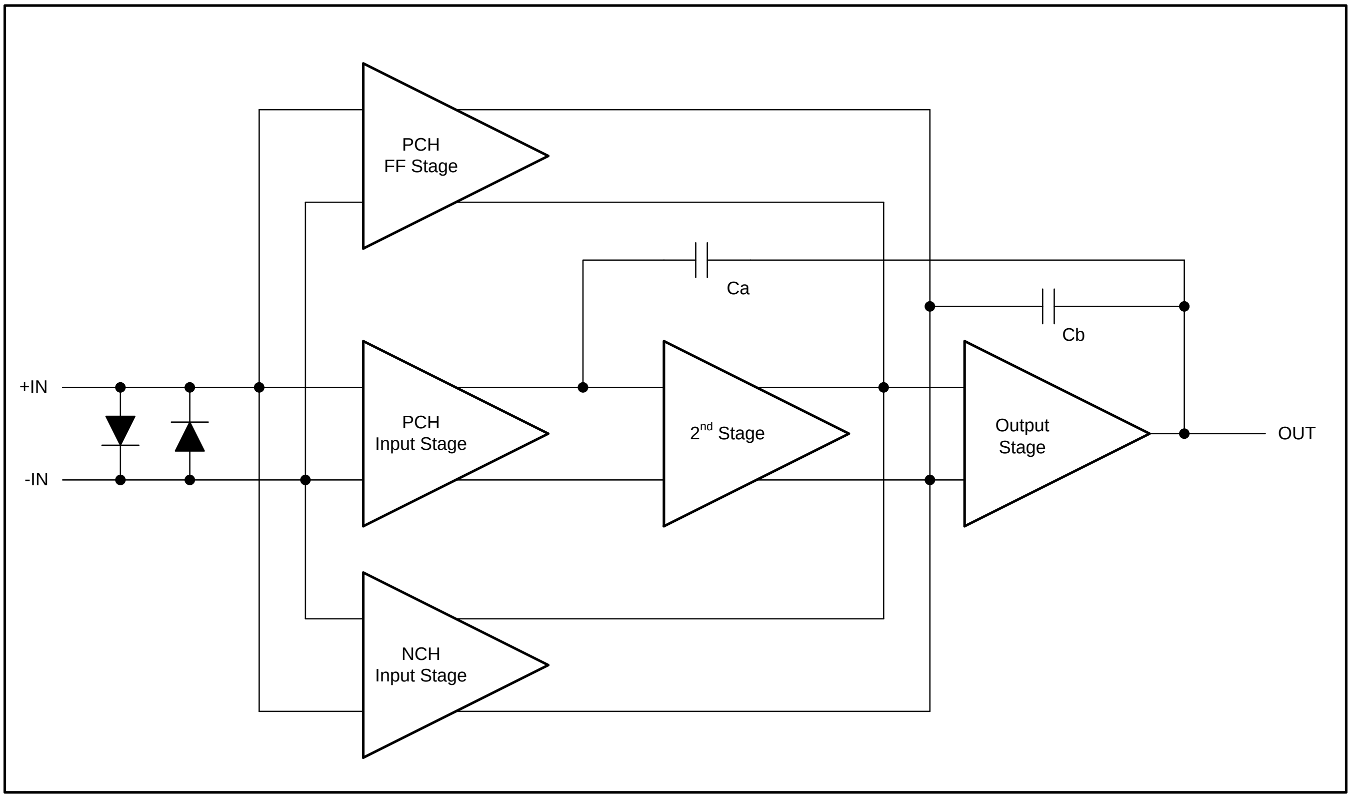
図 24. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The TLVx172 operational amplifier provides high overall performance, making these devices designed for many general-purpose applications. The excellent offset drift of only 1 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The TLVx172 amplifier is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

8.3.2 Phase-Reversal Protection

The TLVx172 device has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx172 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 図 25.

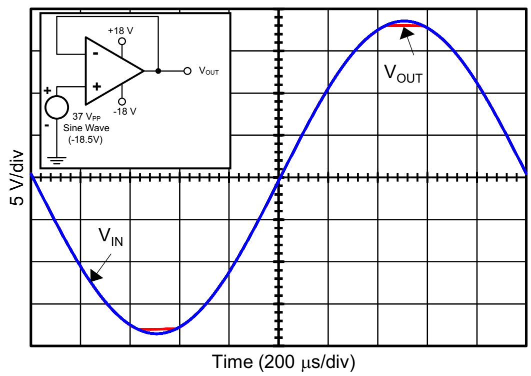


図 25. No Phase Reversal

8.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 図 26 shows the ESD circuits contained in the TLVx172 (indicated by the dashed box). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)

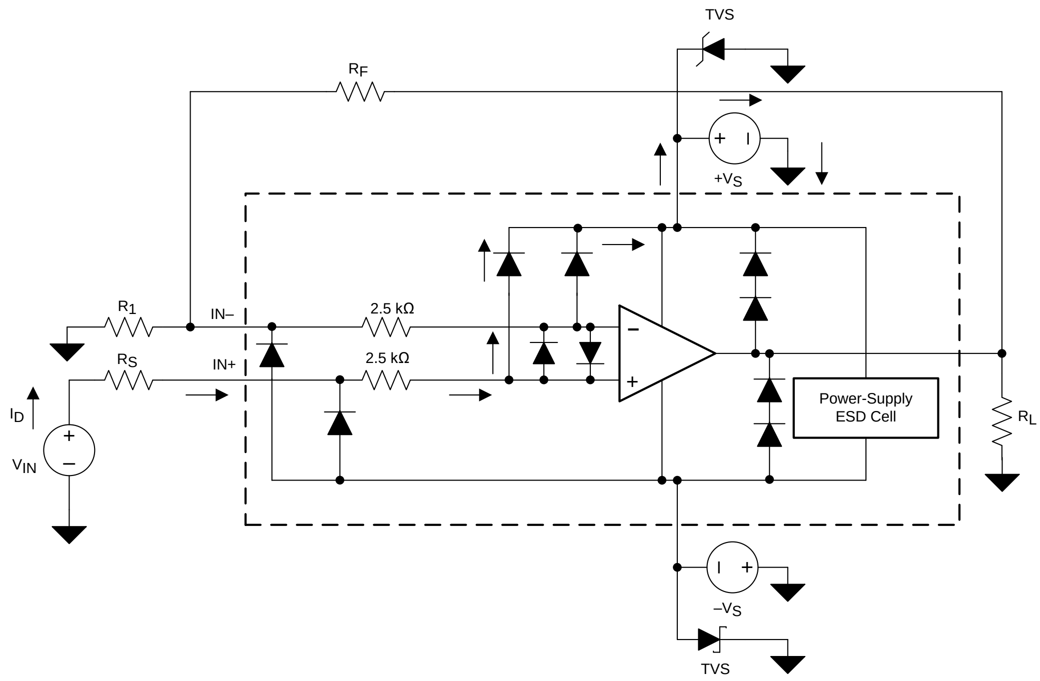


図 26. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLVx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as shown in 図 26, the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 26 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, then one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

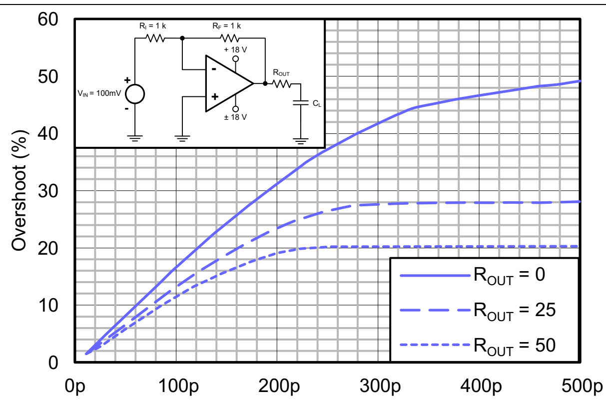
Feature Description (continued)

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 図 26. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The input pins of the TLVx172 are protected from excessive differential voltage with back-to-back diodes; see 図 26. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, then limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the TLVx172. 図 26 shows an example configuration that implements a current-limiting feedback resistor.

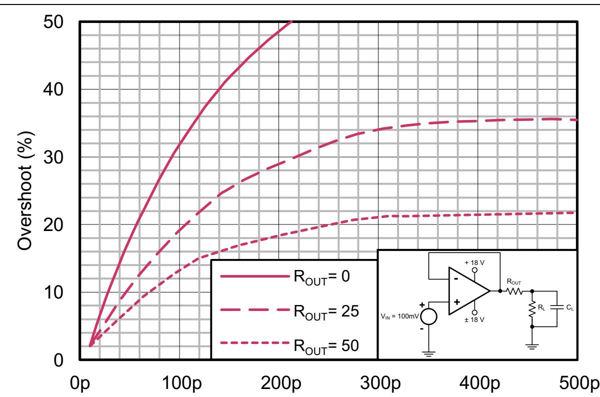
8.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLVx172 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 図 27 and 図 28 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. See the *Feedback Plots Define Op Amp AC Performance* application note for details of analysis techniques and application circuits.



100-mV output step, G = –1

図 27. Small-Signal Overshoot vs Capacitive Load



100-mV output step, G = 1

図 28. Small-Signal Overshoot vs Capacitive Load

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx172 device extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. 表 2 lists the typical performances in this range.

表 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
Offset voltage vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/µs

8.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, which is a result from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. As a result, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx172 is approximately 2 µs.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLVx172 operational amplifier provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Follow the additional recommendations in the *Layout Guidelines* section to achieve the maximum performance from this device. Many applications introduce capacitive loading to the output of the amplifier (which potentially causes instability). To stabilize the amplifier, add an isolation resistor between the amplifier output and the capacitive load. *Typical Application* section shows the process for selecting a resistor.

9.2 Typical Application

This circuit can drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an operational amplifier. R_{ISO} modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin.

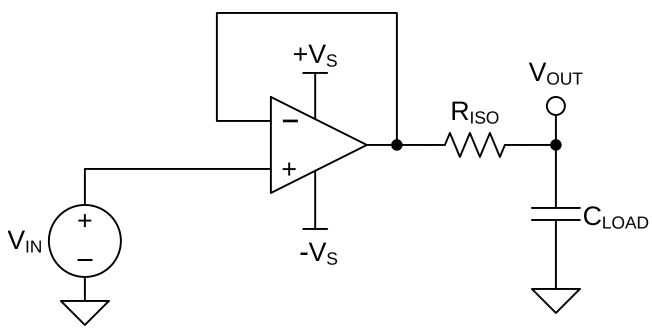


図 29. Unity-Gain Buffer With R_{ISO} Stability Compensation

9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

9.2.2 Detailed Design Procedure

図 29 shows a unity-gain buffer driving a capacitive load. 式 1 shows the transfer function for the circuit in 図 29. 図 29 does not show the open-loop output resistance of the operational amplifier (R_o).

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 式 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. The R_{ISO} and C_{LOAD} components determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} so that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB per decade. 図 30 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (continued)

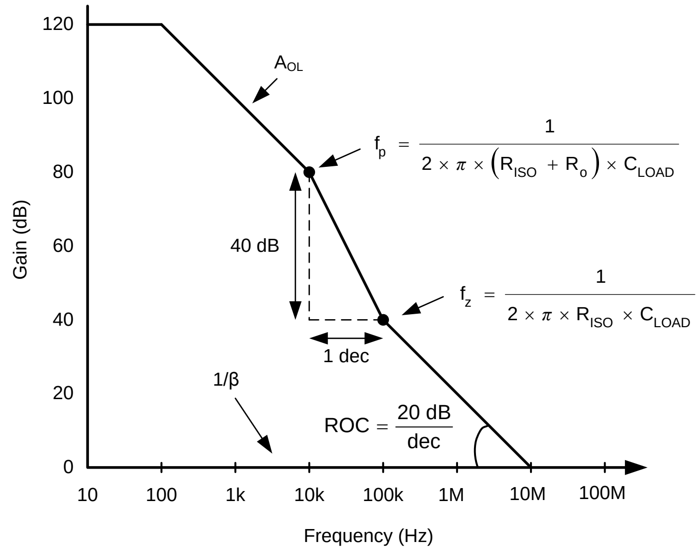


図 30. Unity-Gain Amplifier With R_{ISO} Compensation

Typically, ROC stability analysis is simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can replace the TLVx172, see the *Capacitive Load Drive Solution Using an Isolation Resistor* precision design.

表 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.3 Application Curve

The values of R_{ISO} that yield phase margins of 45º and 60º for various capacitive loads are determined using the described methodology. 図 31 shows the results.

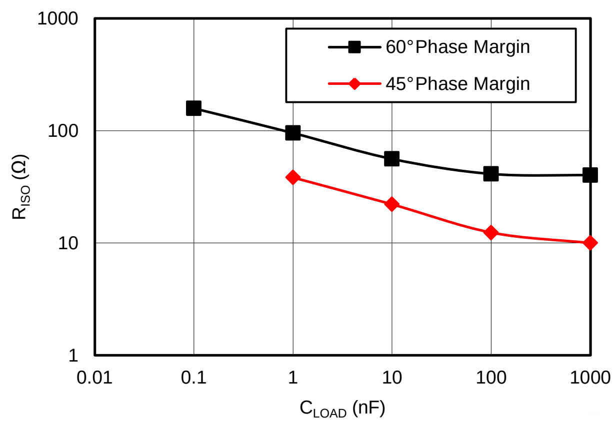


図 31. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

10 Power Supply Recommendations

The TLVx172 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

> **注意**
>
> Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 33, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

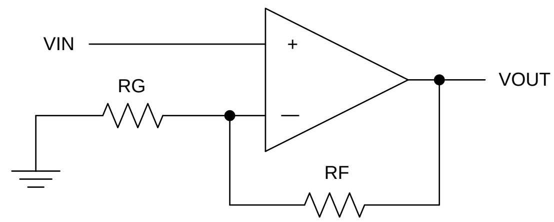


図 32. Schematic Representation

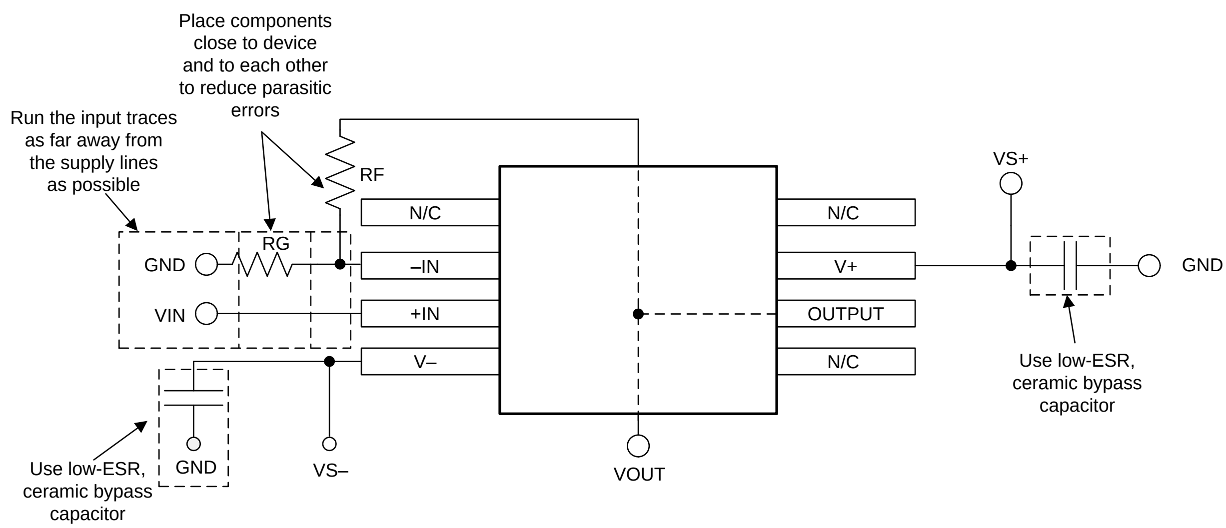


図 33. Operational Amplifier Board Layout for a Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.1.2 開発サポート

12.1.2.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA-TI™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。 TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TI™には従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TI™はAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

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12.1.2.2 DIPアダプタ評価モジュール

DIPアダプタ評価基板ツールを使用すると、小さな表面実装デバイスのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV (SOT23-6、SOT23-5、およびSOT23-3)、DCK (SC70-6およびSC70-5)、およびDRL (SOT563-6)のTIパッケージに対応しています。DIPアダプタ評価基板は、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

12.1.2.3 ユニバーサル・オペアンプ評価基板

ユニバーサル・オペアンプ評価基板は一連の汎用のブランクアウト回路基板で、各種のデバイス・パッケージ・タイプ向け回路のプロトタイプ作成を容易にします。この評価基板基板は、多くの異なる回路を簡単かつ迅速に構築できるように設計されています。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、VSSOP、TSSOP、およびSOT23のパッケージがすべてサポートされています。

注

これらの基板には部品が搭載されていないため、ユーザーが独自のデバイスを実装する必要があります。ユニバーサル・オペアンプ評価基板を注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

12.1.2.4 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果が含まれています。TI Precision Designsは、www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

12.1.2.5 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH® Filter Designerにより、TIのオペアンプと、TIのベンダ・パートナーの受動部品を選択して、最適化されたフィルタを設計できます。

デバイス・サポート (continued)

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、完全な多段アクティブ・フィルタ・ソリューションの設計、最適化、シミュレーションを、わずか数分で実行できます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『フィードバック・プロットによるオペアンプAC性能の定義』*
- *『オペアンプのEMI除去率』*
- *『トランスインピーダンス・アンプの直感的な補正』*
- *『高速オペアンプのノイズ解析』*

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV2172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV4172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

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12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ *TIのE2E（Engineer-to-Engineer）コミュニティ。*エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.6 商標

TINA-TI, E2E are trademarks of Texas Instruments.
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12.7 静電気放電に関する注意事項

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12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV172IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	18VV	Samples
TLV172IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	18VV	Samples
TLV172IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15W	Samples
TLV172IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	15W	Samples
TLV172IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV172	Samples
TLV2172IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14P6	Samples
TLV2172IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14P6	Samples
TLV2172IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL2172	Samples
TLV4172IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLV4172	Samples
TLV4172IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2172 :

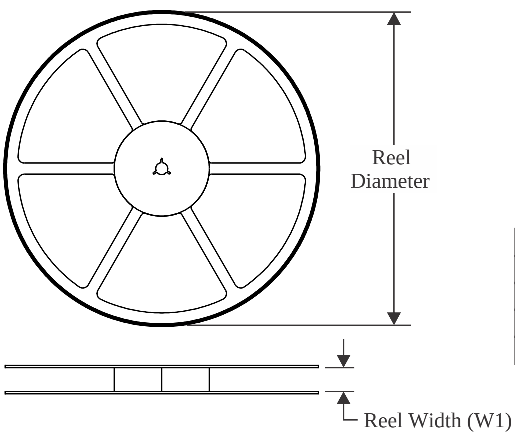
- Automotive : TLV2172-Q1

NOTE: Qualified Version Definitions:

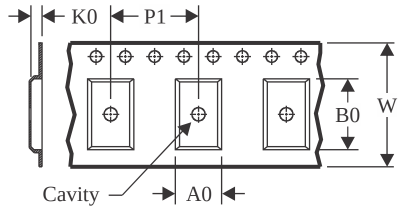
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

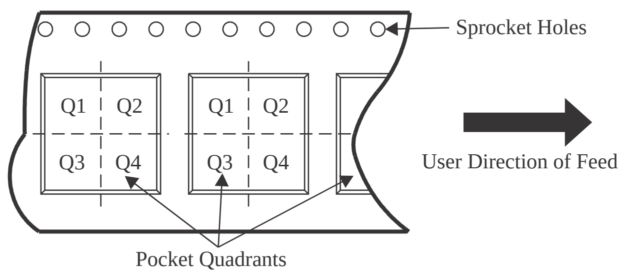


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

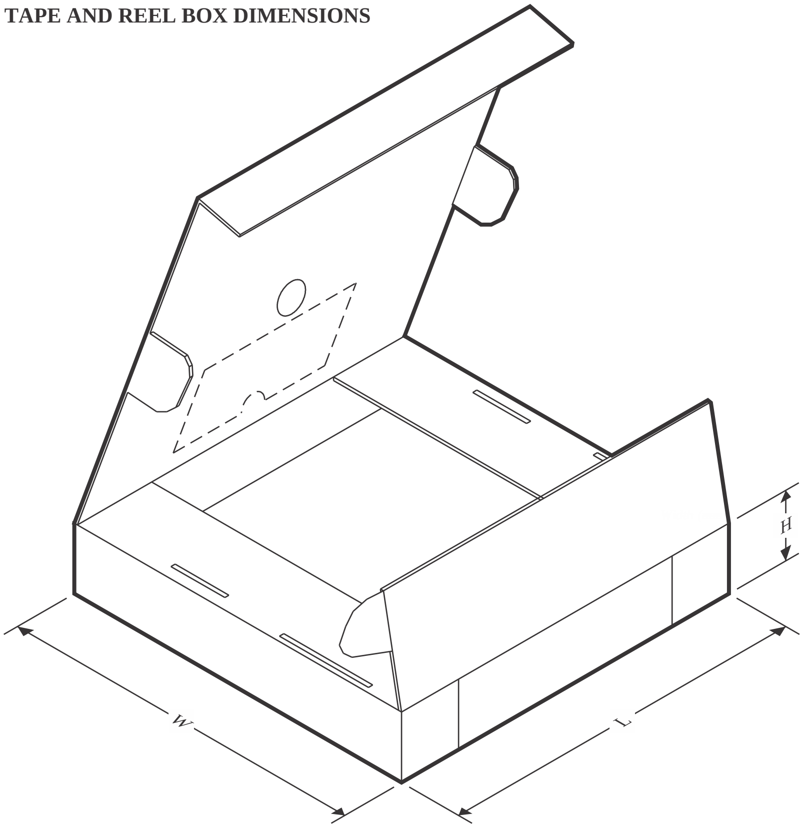
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV172IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV172IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV172IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV172IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2172IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2172IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4172IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4172IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

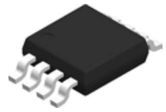
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

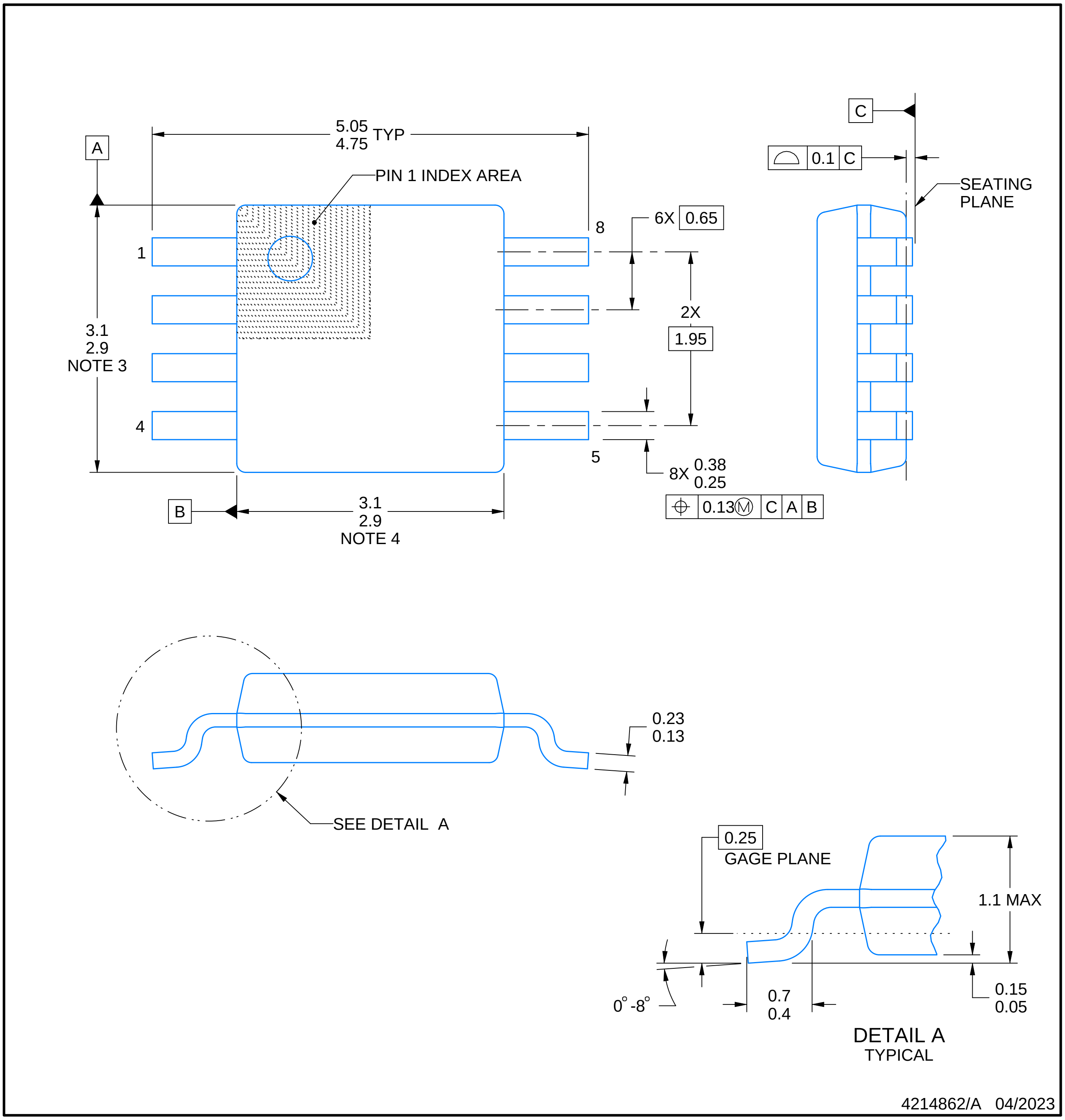
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV172IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV172IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV172IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV172IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV172IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV2172IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
TLV2172IDGKT	VSSOP	DGK	8	250	356.0	356.0	35.0
TLV2172IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV4172IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV4172IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

DGK0008A



VSSOP - 1.1 mm max height

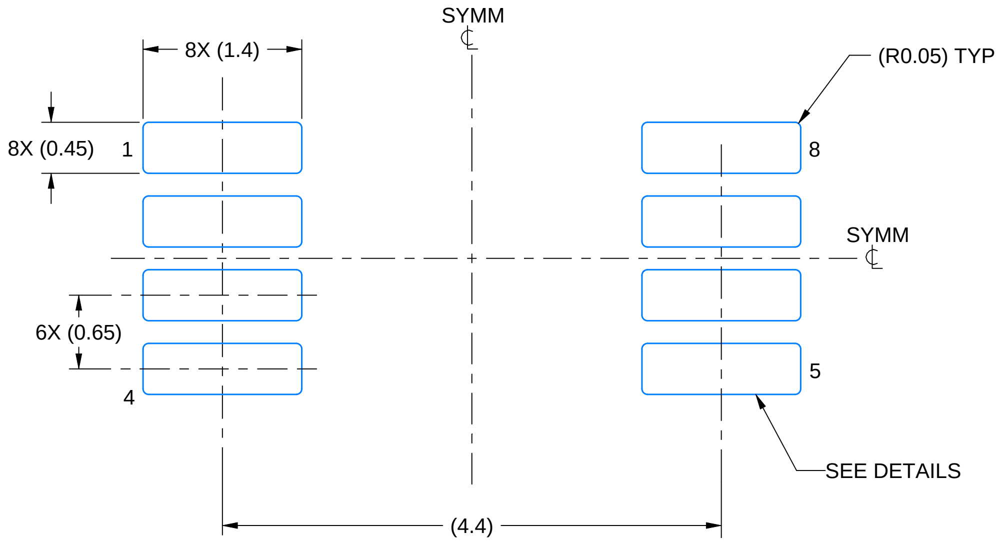
SMALL OUTLINE PACKAGE



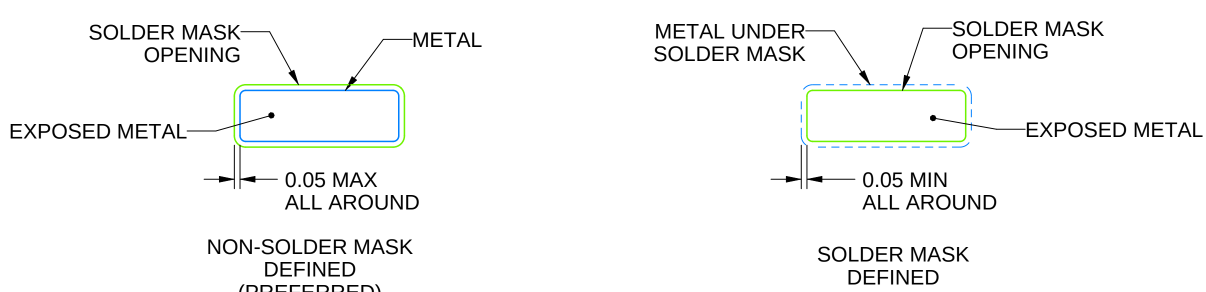
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

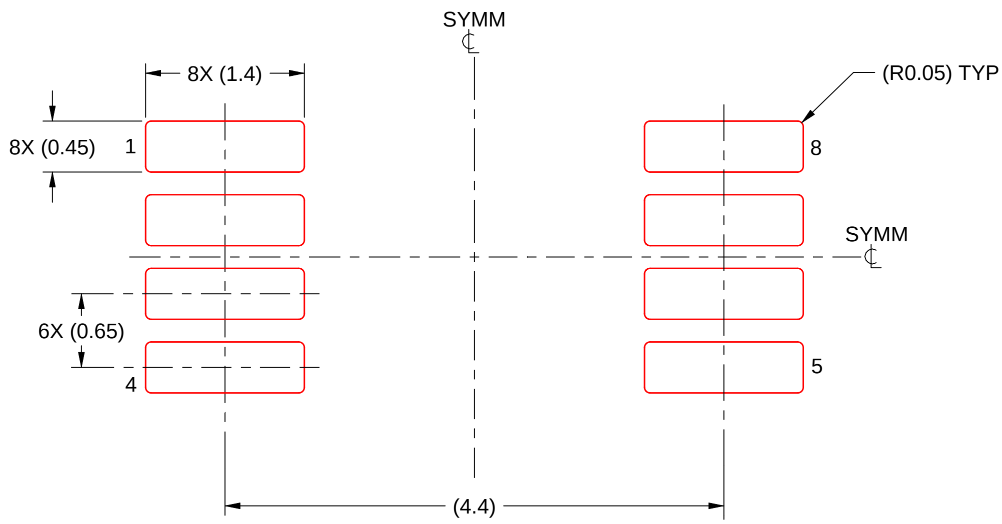


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

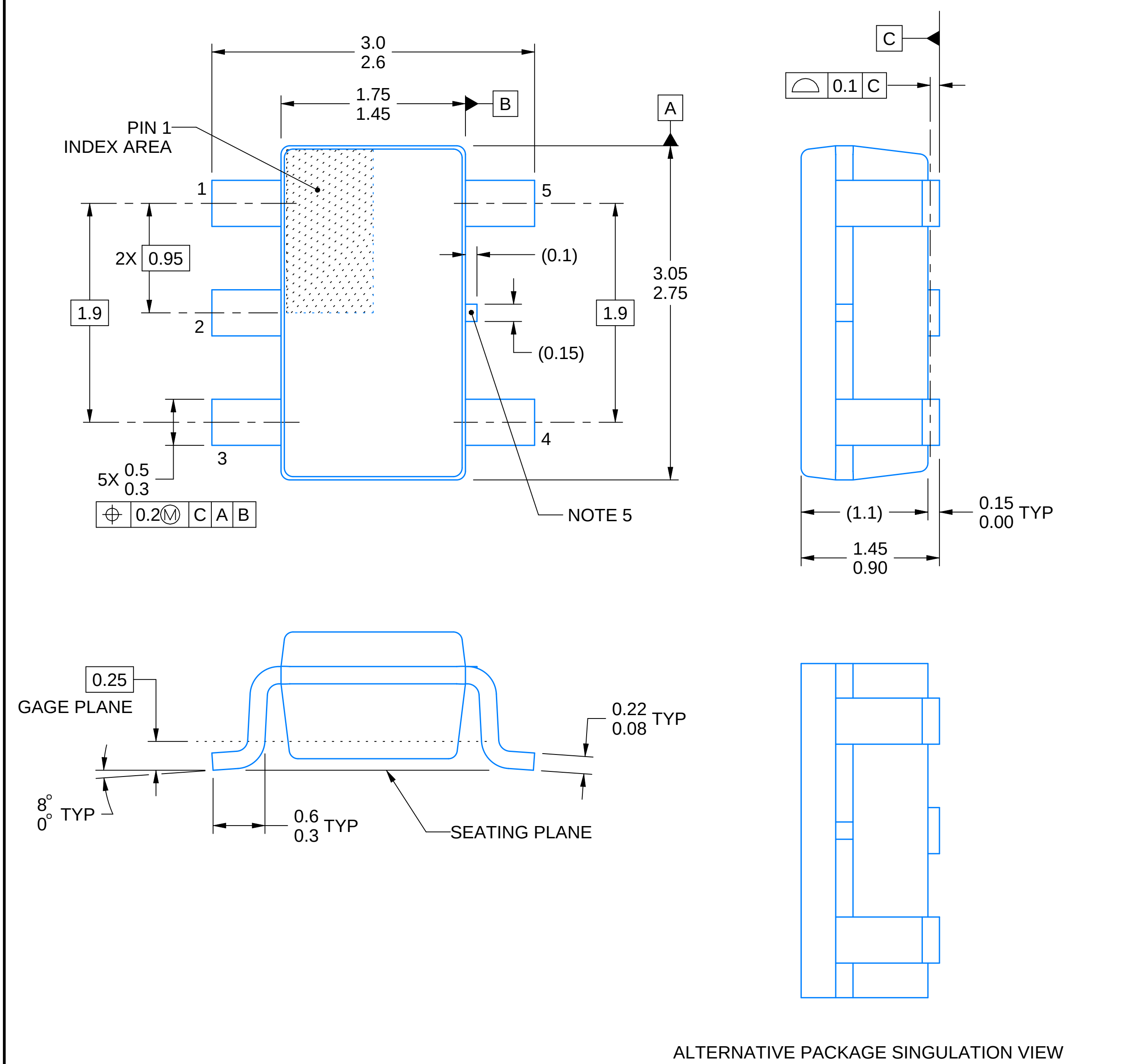


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

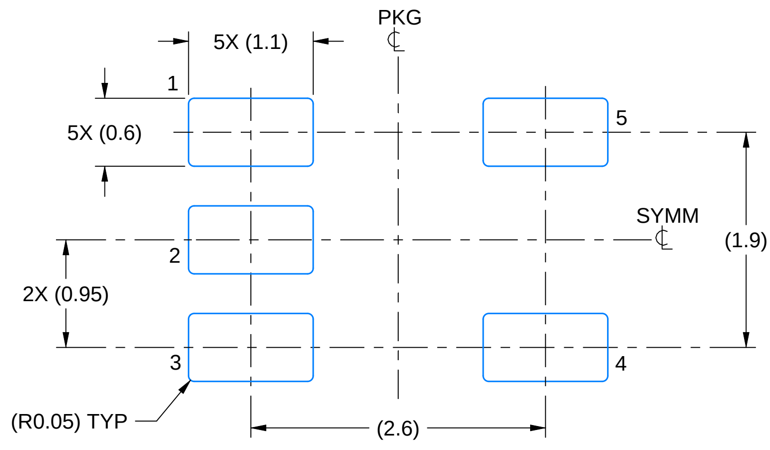
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



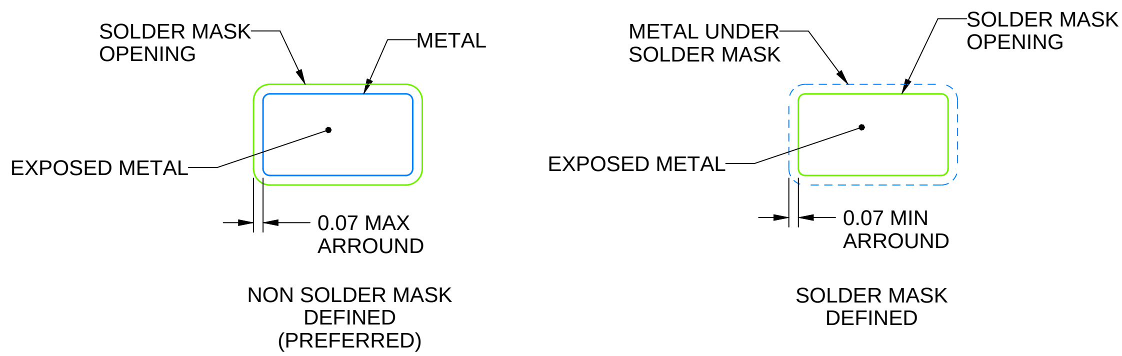
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

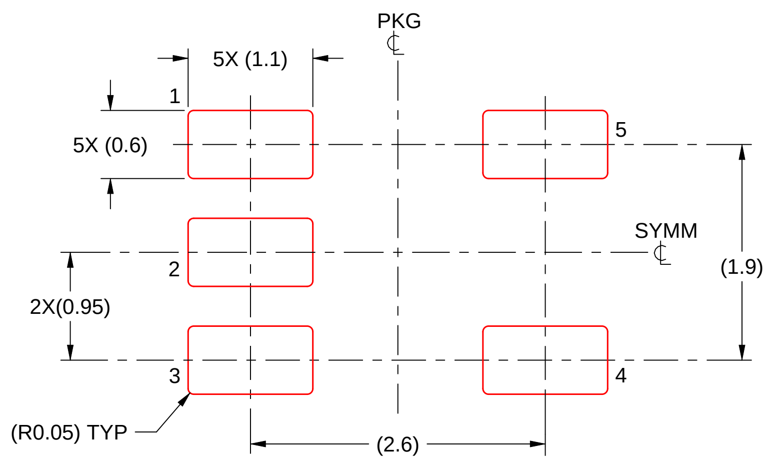


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

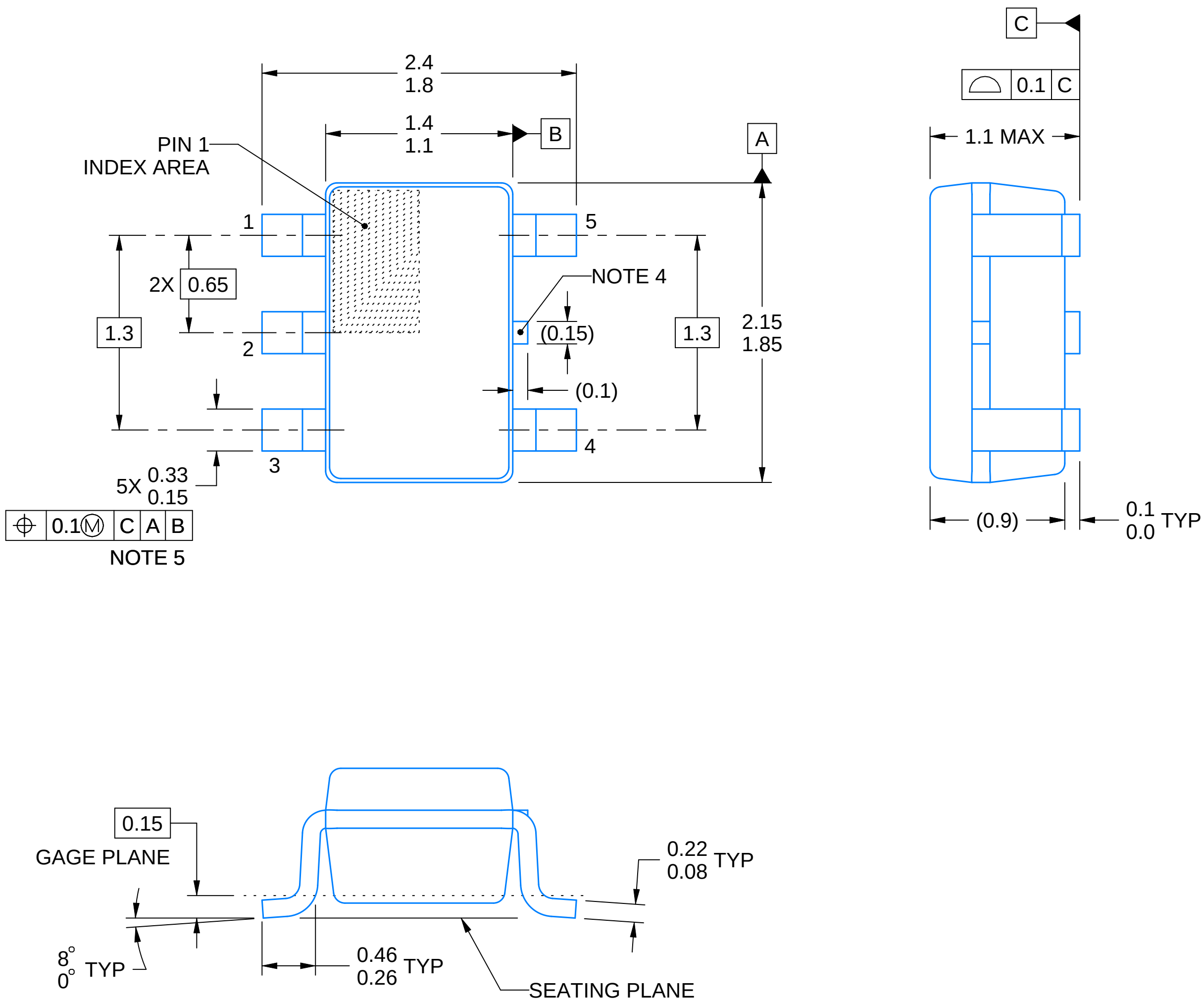


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

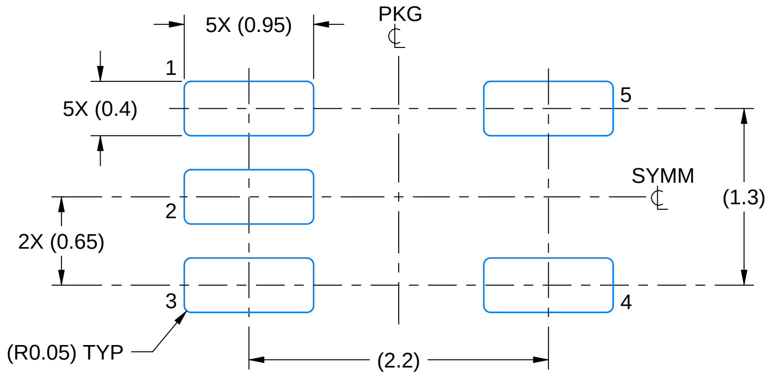
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



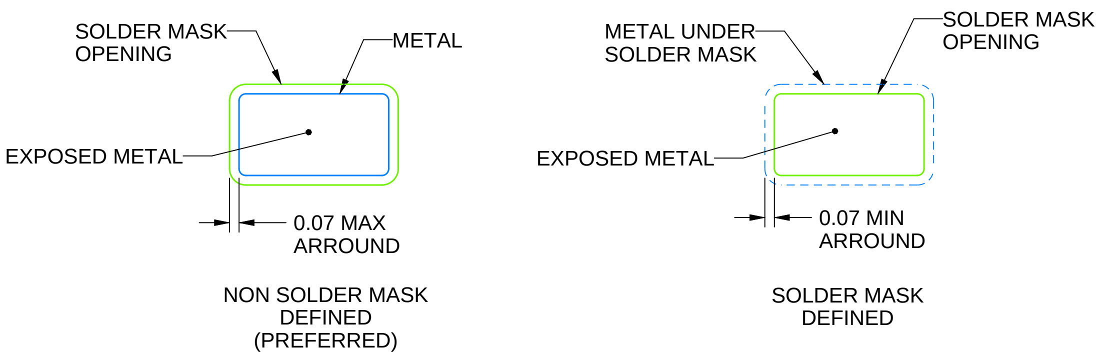
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

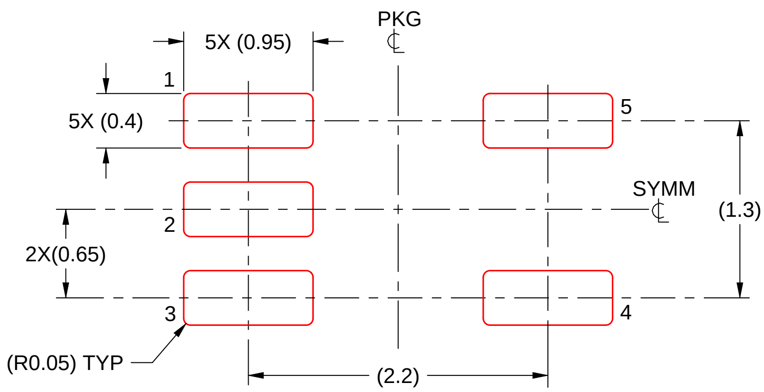


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



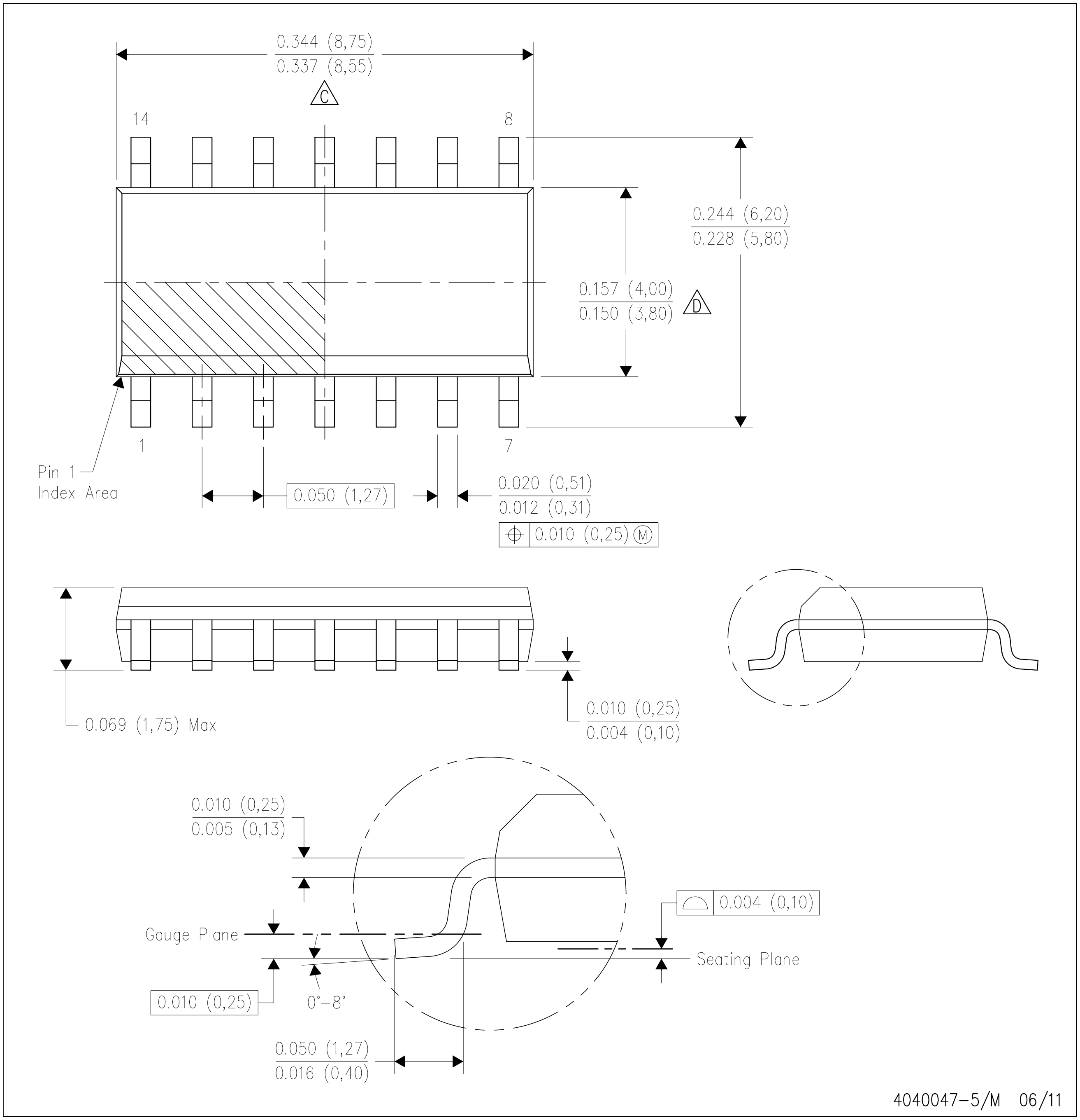
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

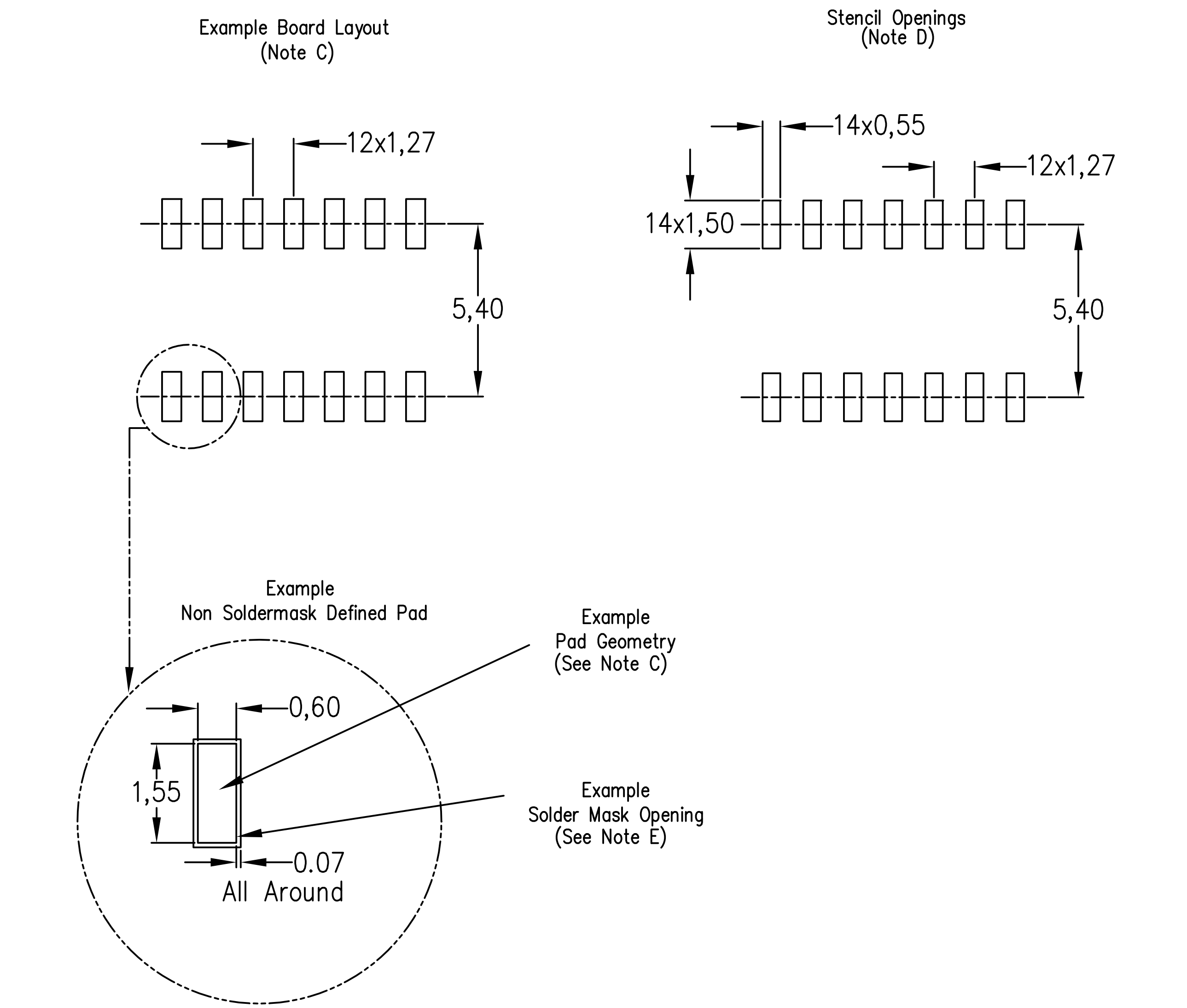
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

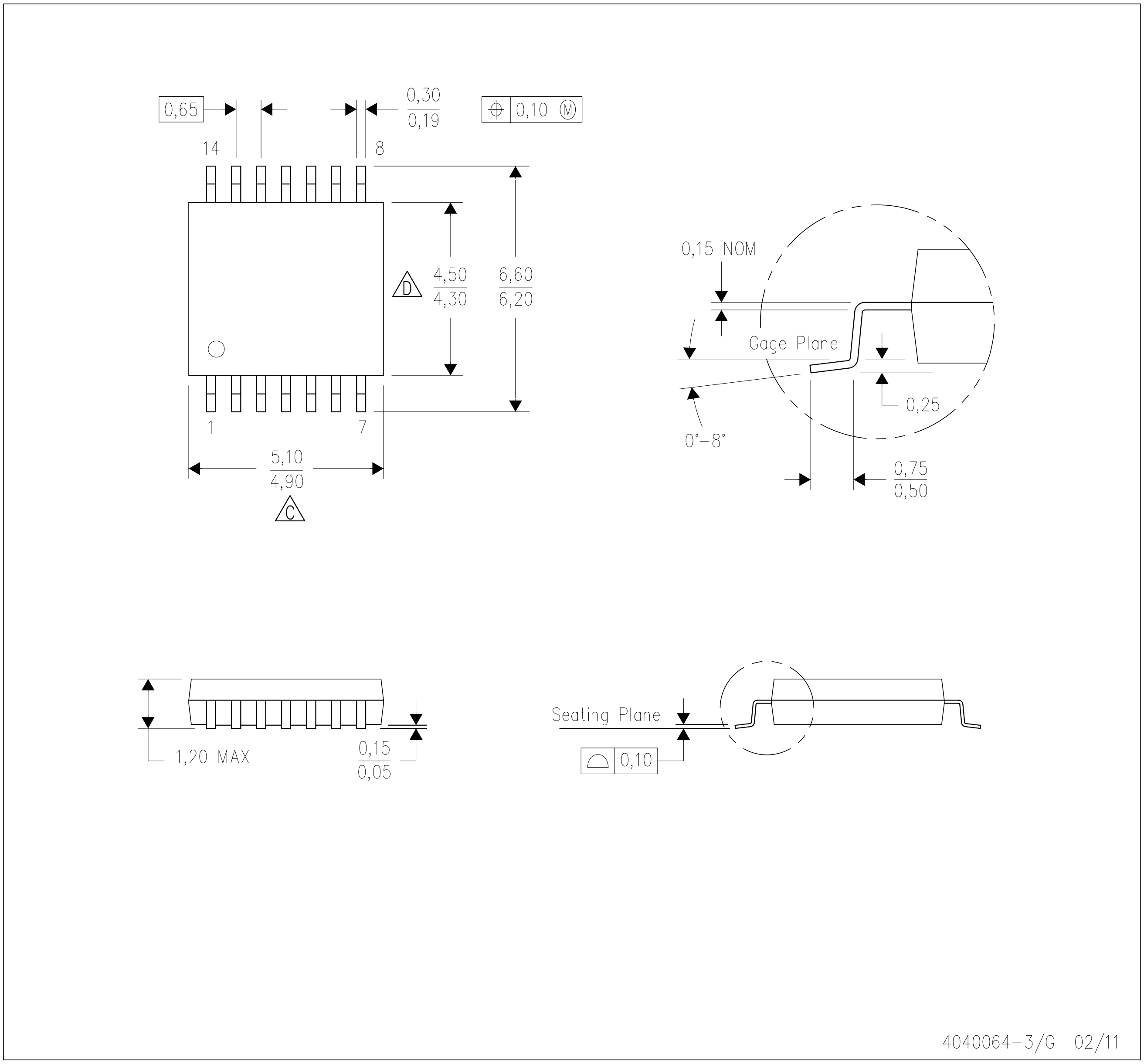
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



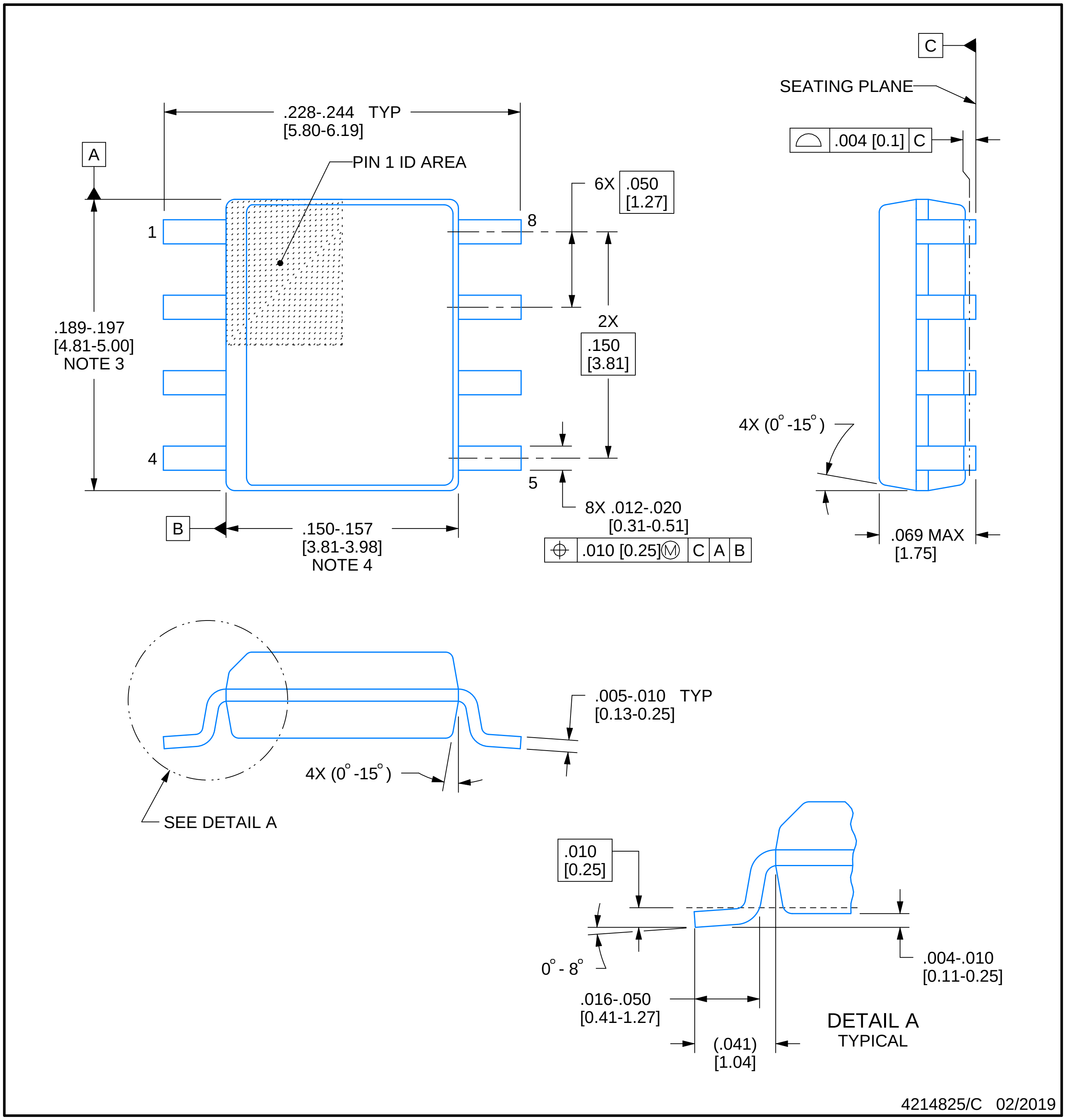
4211283–3/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



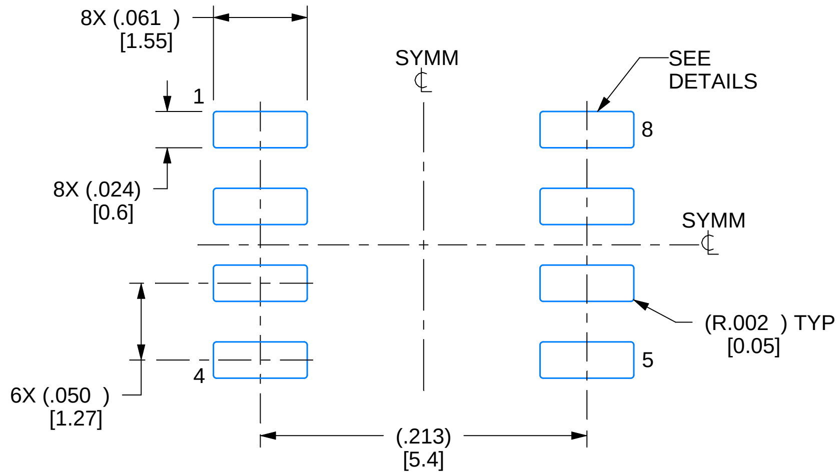
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



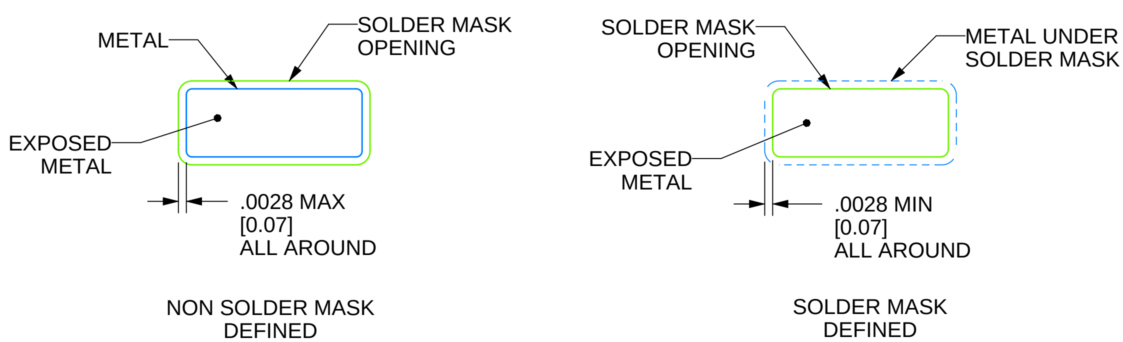
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

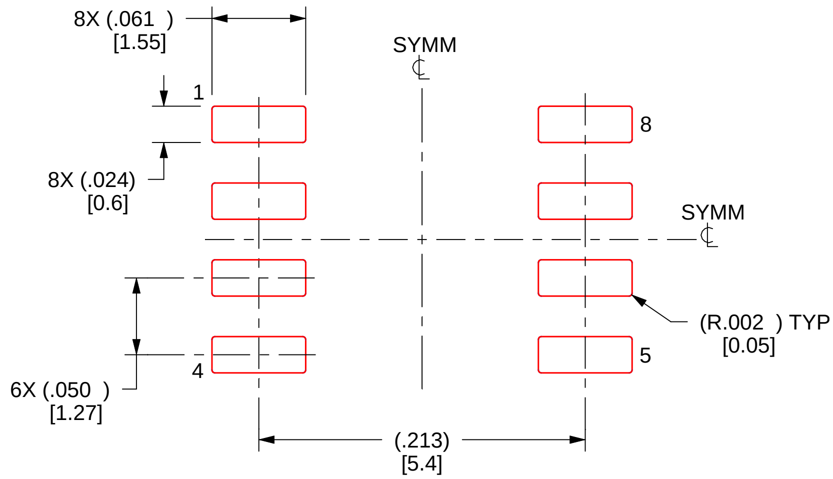


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265