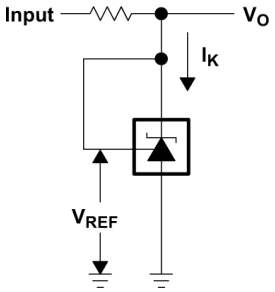
TLV431x 低電圧、可変、高精度シャント レギュレータ

1 特長

- 低電圧動作、V_{REF} = 1.24V
- 可変出力電圧、V_O = V_{REF}～6V
- 25℃でのリファレンス電圧の公差
  - TLV431B: 0.5%
  - TLV431A: 1%
  - TLV431: 1.5%
- 温度ドリフト (標準値)
  - 4mV (0℃～70℃)
  - 6mV (-40℃～85℃)
  - 11mV (-40℃～125℃)
- 低い動作カソード電流:80µA (標準値)
- 出力インピーダンス:0.25Ω (標準値)
- 超小型の SC-70 パッケージで、SOT-23-3 よりも 40% 小さい占有面積
- TLVH431 および TLVH432 の特長
  - 広い V_{KA} (1.24V～18V) と I_K (80mA)
  - SOT-89 パッケージでも供給
  - SOT-23-3 および SOT-89 パッケージで複数のピン配置を選択可能
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- 調整可能な基準電圧および電流
- フライバック SMPS の 2 次側レギュレーション
- ツェナーの代替品
- 電圧監視
- リファレンス電圧内蔵のコンパレータ



概略回路図

3 概要

TLV431 デバイスは低電圧、3 端子の可変電圧リファレンスであり、該当する産業用および民生用温度範囲全体にわたって規定の熱的安定性を維持します。出力電圧は、2 つの外付け抵抗により V_{REF} (1.24V) と 6V の間の任意の値に設定できます (「パラメータ測定情報」セクションを参照)。これらのデバイスは、広く使用されている TL431 および TL1431 シャント レギュレータ基準電圧よりも低い電圧 (1.24V)で動作します。

オプトカプラとともに使用すると、TLV431 は 3V～3.3V のスイッチング モード電源用の絶縁フィードバック回路における理想的な基準電圧です。これらのデバイスの出力インピーダンスは 0.25Ω (標準値) です。アクティブ出力回路により、非常に鋭いターンオン特性を持つことから、オンボード レギュレーションや可変電源など多くのアプリケーションにおいて、低電圧ツェナー ダイオードの非常に優れた代替品となります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLV431	DBZ (SOT-23、3)	2.92mm × 2.37mm
	DBV (SOT-23、5)	2.90mm × 2.8mm
	LP (TO-92、3)	5.2mm × 3.68mm
	PK (SOT-89、3)	4.5mm × 4.095mm
TLV431A	DBV (SOT-23、5)	2.90mm × 2.8mm
	DBZ (SOT-23、3)	2.92mm × 2.37mm
	PK (SOT-89、3)	4.5mm × 4.095mm
	LP (TO-92、3)	5.2mm × 3.68mm
	D (SOIC、8)	4.9mm × 6mm
TLV431B	DBV (SOT-23、5)	2.90mm × 2.8mm
	DBZ (SOT-23、3)	2.92mm × 2.37mm
	PK (SOT-89、3)	4.5mm × 4.095mm
	LP (TO-92、3)	5.2mm × 3.68mm
	DCK (SOT-SC70、6)	2mm × 1.5mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Pin Configuration and Functions.....3
5 Specifications.....4
5.1 Absolute Maximum Ratings.....4
5.2 ESD Ratings.....4
5.3 Recommended Operating Conditions.....4
5.4 Thermal Information.....4
5.5 Electrical Characteristics for TLV431.....5
5.6 Electrical Characteristics for TLV431A.....6
5.7 Electrical Characteristics for TLV431B.....7
5.8 Typical Characteristics.....8
6 Parameter Measurement Information.....17
7 Detailed Description.....18
7.1 Overview.....18
7.2 Functional Block Diagram.....18
7.3 Feature Description.....18
7.4 Device Functional Modes.....19
8 Applications and Implementation.....20
8.1 Application Information.....20
8.2 Typical Applications.....21
8.3 Power Supply Recommendations.....24
8.4 Layout.....24
9 Device and Documentation Support.....25
9.1 Documentation Support.....25
9.2 ドキュメントの更新通知を受け取る方法.....25
9.3 サポート・リソース.....25
9.4 Trademarks.....25
9.5 静電気放電に関する注意事項.....25
9.6 用語集.....25
10 Revision History.....25
11 Mechanical, Packaging, and Orderable Information.....26

Copyright © 2025 Texas Instruments Incorporated

4 Pin Configuration and Functions

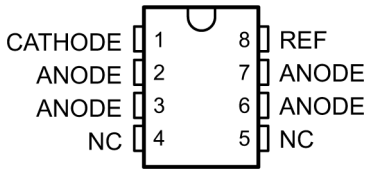
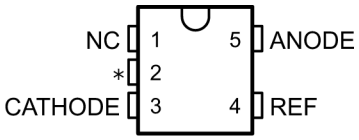


図 4-1. D (SOIC) Package (Top View)



NC − No internal connection

* Pin 2 is attached to Substrate and must be connected to ANODE or left open.

図 4-2. DBV (SOT-23-5) Package (Top View)

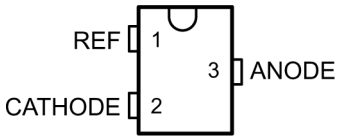


図 4-3. DBZ (SOT-23-3) Package (Top View)

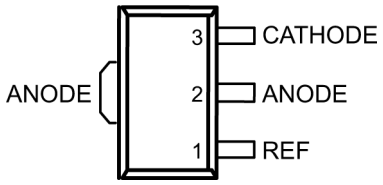
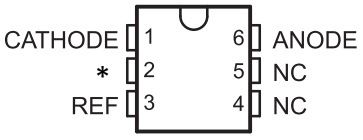


図 4-4. PK (SOT-89) Package (Top View)



NC – No internal connection

* - Must be connected to ANODE or left open

図 4-5. DCK (SC-70) Package (Top View)

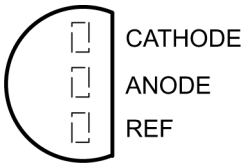


図 4-6. LP (TO-92/TO-226) Package (Top View)

表 4-1. Pin Functions

PIN							TYPE	DESCRIPTION
NAME	DBZ	DBV	PK	D	LP	DCK		
CATHODE	2	3	3	1	1	1	I/O	Shunt Current/Voltage input
REF	1	4	1	8	3	3	I	Threshold relative to common anode
ANODE	3	5	2	2, 3, 6, 7	2	6	O	Common pin, normally connected to ground
NC	—	1	—	4, 5	—	4, 5	I	No Internal Connection
*	—	2	—	—	—	2	I	Substrate Connection. Must be connected to ANODE or left open.

Copyright © 2025 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{KA}	Cathode voltage (2)		7	V
I_K	Continuous cathode current	–20	20	mA
I_{ref}	Reference current	–0.05	3	mA
	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the anode terminal, unless otherwise noted.

5.2 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
V(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		V_{REF}	6	V
I_K	Cathode current		0.1	15	mA
T_A	Operating free-air temperature	TLV431_C	0	70	°C
		TLV431_I	–40	85	
		TLV431_Q	–40	125	

5.4 Thermal Information

THERMAL METRIC (1)		TLV431x						UNIT
		DCK	D	PK	DBV	DBZ	LP	
		6 PINS	8 PINS	3 PINS	5 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	97	52	206	206	140	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	259	39	9	131	76	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

Copyright © 2025 Texas Instruments Incorporated

5.5 Electrical Characteristics for TLV431

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431			UNIT
					MIN	TYP	MAX	
V_{REF}	Reference voltage	V_{KA} = V_{REF}, I_K=10mA	T_A = 25°C		1.222	1.24	1.258	V
			T_A = full range [1] (see 図 6-1)	TLV431C	1.21		1.27	
				TLV431I	1.202		1.278	
				TLV431Q	1.194		1.286	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range[2]	V_{KA} = V_{REF}, I_K = 10mA [1] (see 図 6-1)		TLV431C		4	12	mV
				TLV431I		6	20	
				TLV431Q		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	V_{KA} = V_{REF} to 6V, I_K = 10mA (see 図 6-2)				-1.5	-2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see 図 6-2)				0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range[2]	I_K = 10mA, R1 =10kΩ, R2 = open [1] (see 図 6-2)		TLV431C		0.05	0.3	µA
				TLV431I		0.1	0.4	
				TLV431Q		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	V_{KA} = V_{REF} (see 図 6-1)		TLV431C/I		55	80	µA
				TLV431Q		55	100	
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see 図 6-3)				0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance[3]	V_{KA} = V_{REF}, f ≤ 1kHz, I_K = 0.1mA to 15mA (see 図 6-1)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device. αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is operating with two external resistors (see 図 6-2), the total dynamic impedance of the circuit is defined as: $|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1 + \frac{R1}{R2}\right)$

Copyright © 2025 Texas Instruments Incorporated

5.6 Electrical Characteristics for TLV431A

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431A			UNIT
					MIN	TYP	MAX	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10mA	T_A = 25°C		1.228	1.24	1.252	V
			T_A = full range (1) (see 図 6-1)	TLV431AC	1.221		1.259	
				TLV431AI	1.215		1.265	
				TLV431AQ	1.209		1.271	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range (2)	$V_{KA} = V_{REF}$, I_K = 10mA (1) (see 図 6-1)		TLV431AC		4	12	mV
				TLV431AI		6	20	
				TLV431AQ		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see 図 6-2)				-1.5	-2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see 図 6-2)				0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range (2)	I_K = 10mA, R1 = 10kΩ, R2 = open(1) (see 図 6-2)		TLV431AC		0.05	0.3	µA
				TLV431AI		0.1	0.4	
				TLV431AQ		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see 図 6-1)		TLV431AC/AI		55	80	µA
				TLV431AQ		55	100	
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see 図 6-3)				0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance (3)	$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see 図 6-1)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device. αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is operating with two external resistors (see 図 6-2), the total dynamic impedance of the circuit is defined as: $|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1 + \frac{R1}{R2}\right)$

Copyright © 2025 Texas Instruments Incorporated

5.7 Electrical Characteristics for TLV431B

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431B			UNIT
					MIN	TYP	MAX	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K=10mA	T_A = 25°C		1.234	1.24	1.246	V
			T_A = full range (1) (see 図 6-1)	TLV431BC	1.227		1.253	
				TLV431BI	1.224		1.259	
				TLV431BQ	1.221		1.265	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range (2)	$V_{KA} = V_{REF}$, I_K = 10mA (1) (see 図 6-1)		TLV431BC		4	12	mV
				TLV431BI		6	20	
				TLV431BQ		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see 図 6-2)				-1.5	-2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see 図 6-2)				0.1	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range (2)	I_K = 10mA, R1 =10kΩ, R2 = open (3) (see 図 6-2)		TLV431BC		0.05	0.3	µA
				TLV431BI		0.1	0.4	
				TLV431BQ		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see 図 6-1)				55	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see 図 6-3)				0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance (4)	$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see 図 6-1)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters VREF(dev) and Iref(dev) are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device. αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(4) dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is operating with two external resistors (see 図 6-2), the total dynamic impedance of the circuit is defined as: $|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1 + \frac{R1}{R2}\right)$

5.8 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

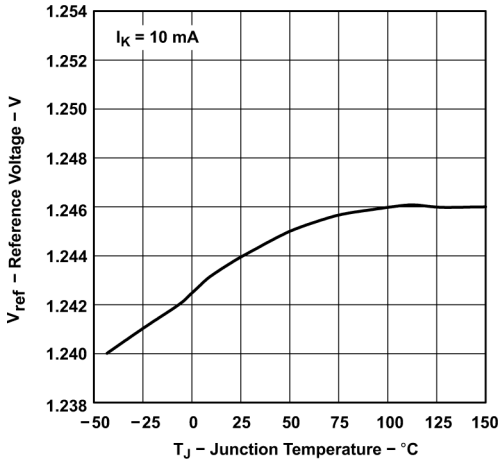


図 5-1. Reference Voltage vs Junction Temperature

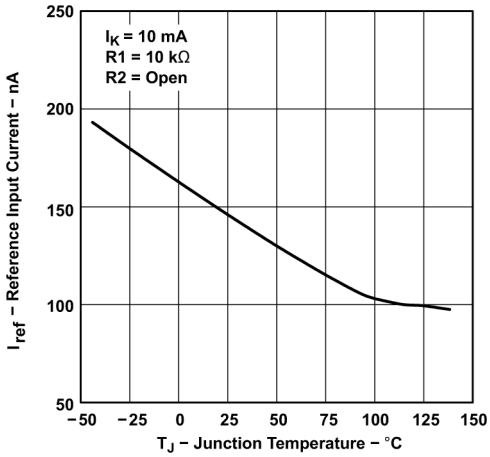


図 5-2. Reference Input Current vs Junction Temperature (for TLV431 and TLV431A)

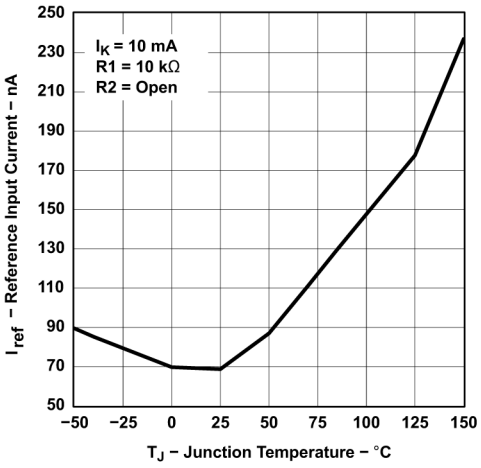


図 5-3. Reference Input Current vs Junction Temperature (for TLV431B)

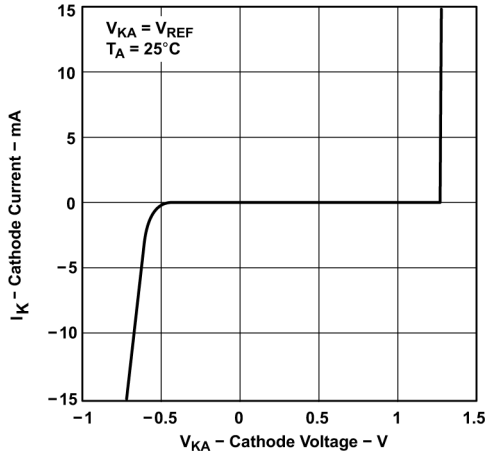


図 5-4. Cathode Current vs Cathode Voltage

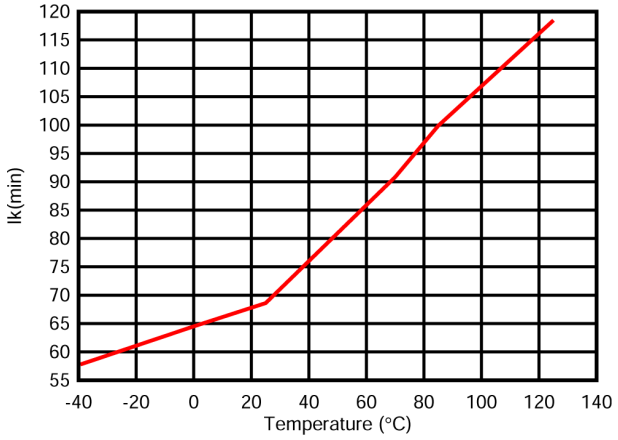


図 5-5. Minimum Cathode Current vs Temperature

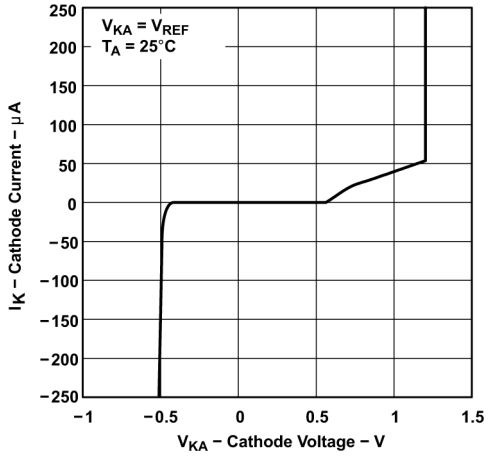


図 5-6. Cathode Current vs Cathode Voltage

Copyright © 2025 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

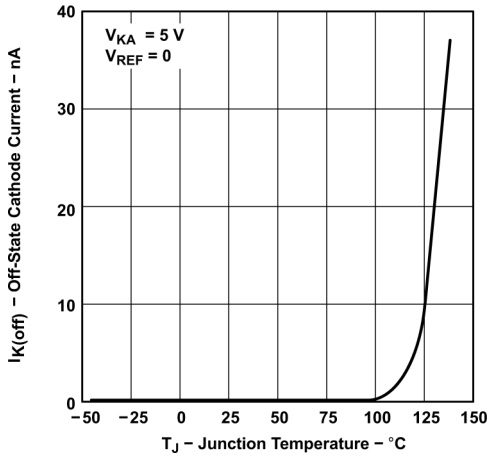


図 5-7. Off-State Cathode Current vs Junction Temperature (for TLV431 and TLV431A)

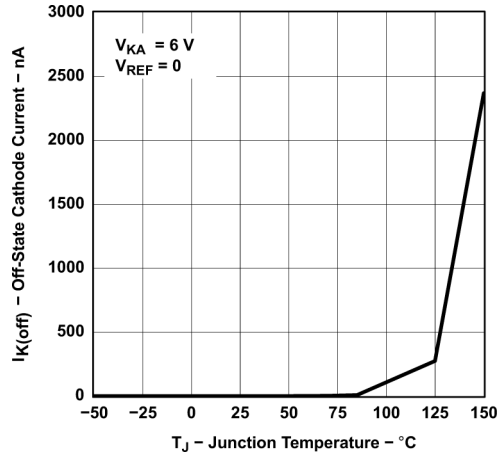


図 5-8. Off-State Cathode Current vs Junction Temperature (for TLV431B)

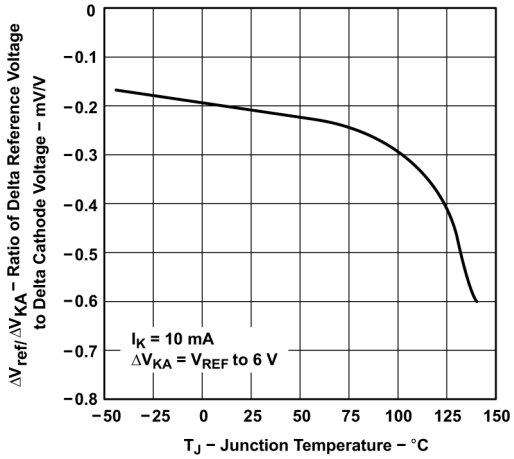


図 5-9. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431 and TLV431A)

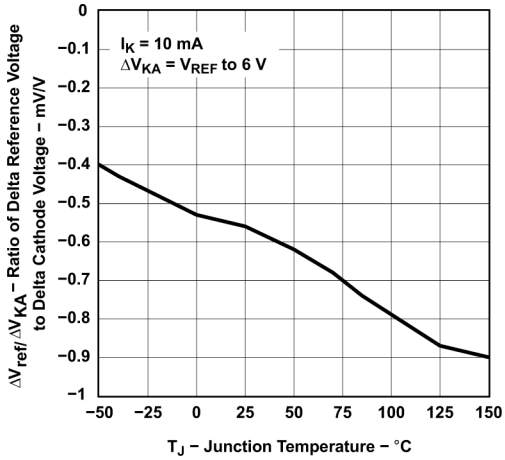


図 5-10. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431B)

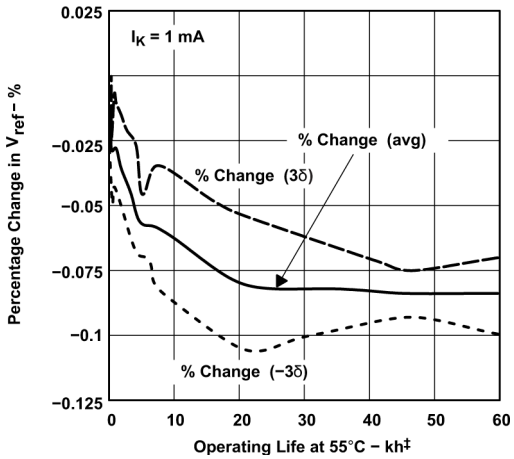
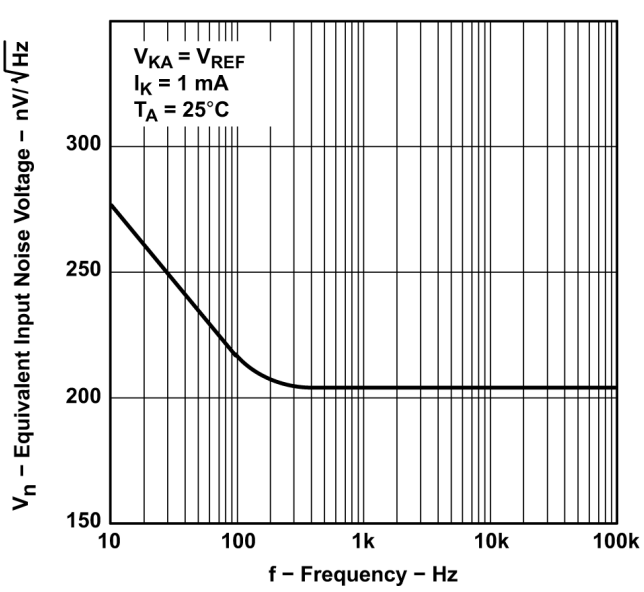
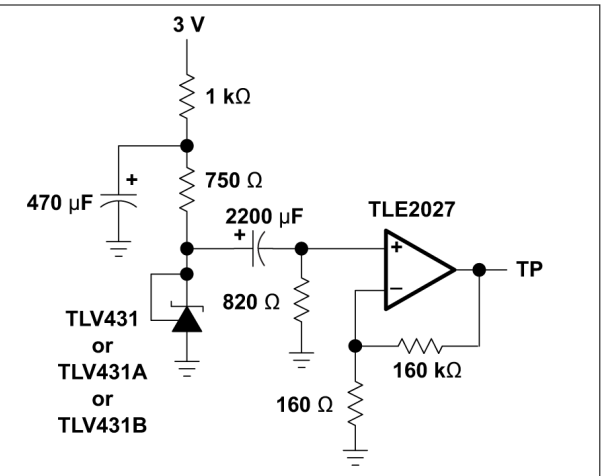


図 5-11. Percentage Change in V_{REF} vs Operating Life at 55°C

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.





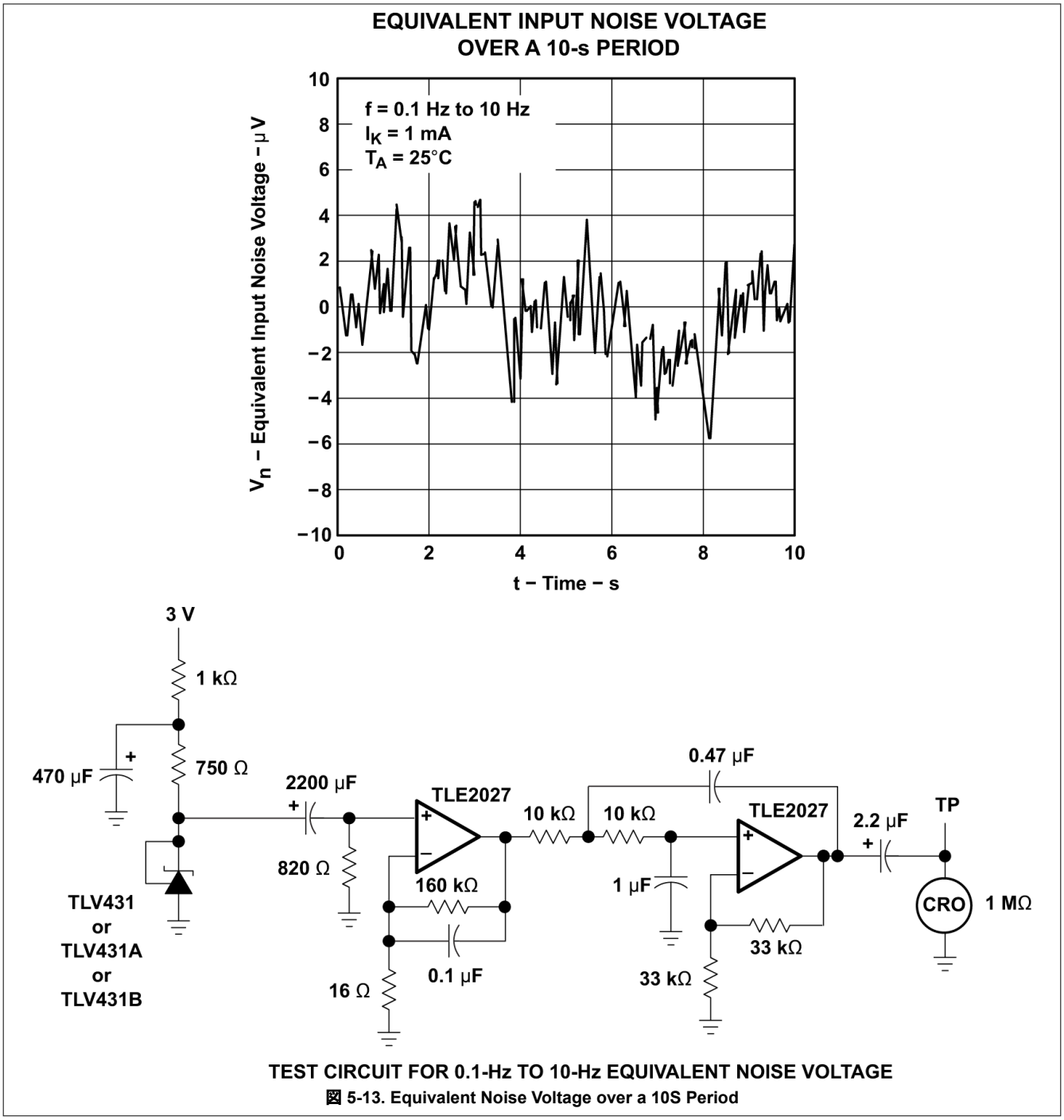
TEST CIRCUIT FOR EQUIVALENT INPUT NOISE VOLTAGE

図 5-12. Equivalent Input Noise Voltage

Copyright © 2025 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

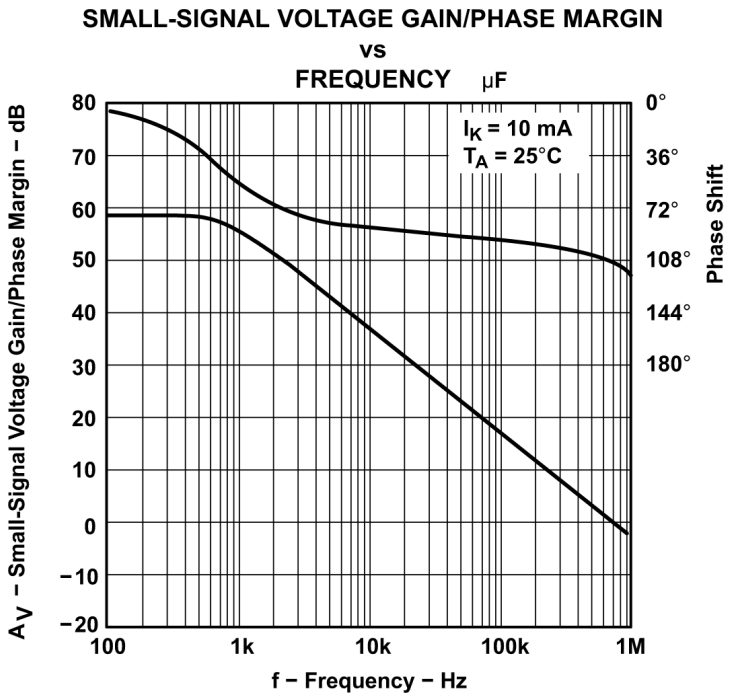


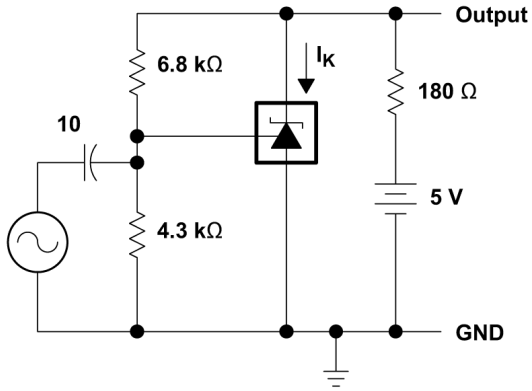
TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT NOISE VOLTAGE

図 5-13. Equivalent Noise Voltage over a 10S Period

5.8 Typical Characteristics (continued)

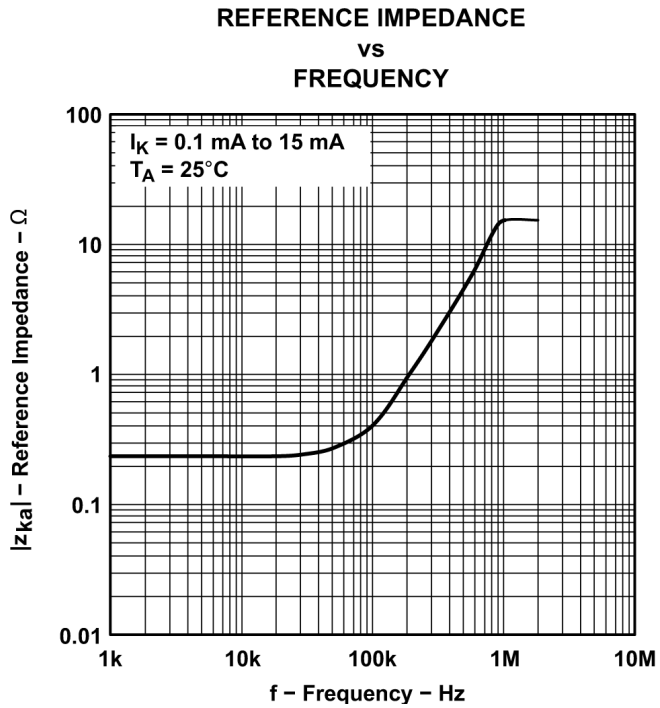
Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

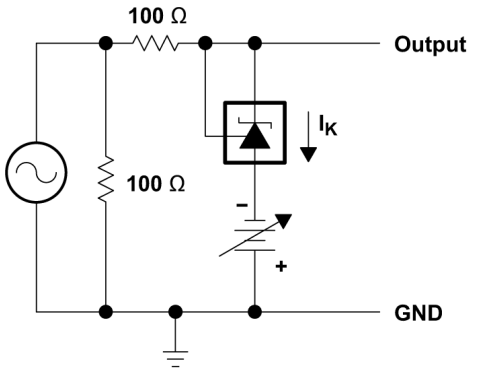




TEST CIRCUIT FOR VOLTAGE GAIN AND PHASE MARGIN

図 5-14. Voltage Gain and Phase Margin





TEST CIRCUIT FOR REFERENCE IMPEDANCE

図 5-15. Reference Impedance vs Frequency

Copyright © 2025 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

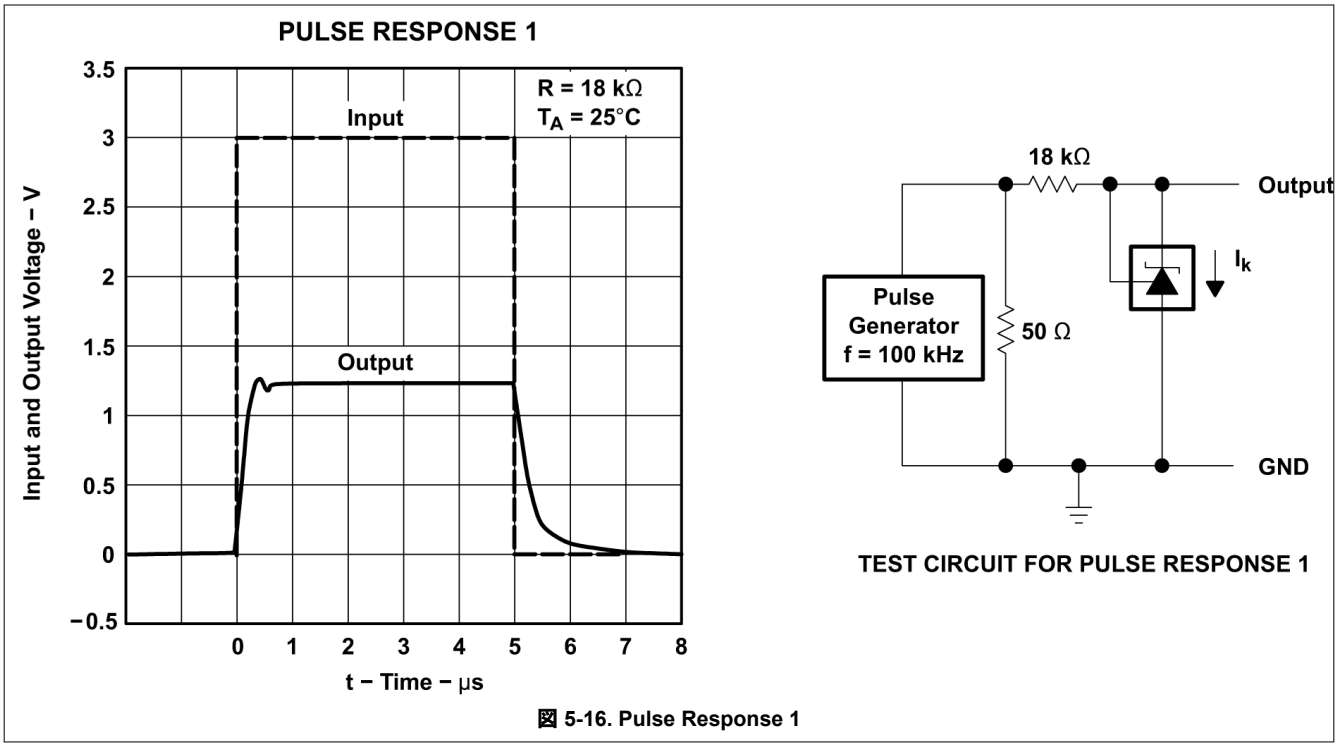


図 5-16. Pulse Response 1

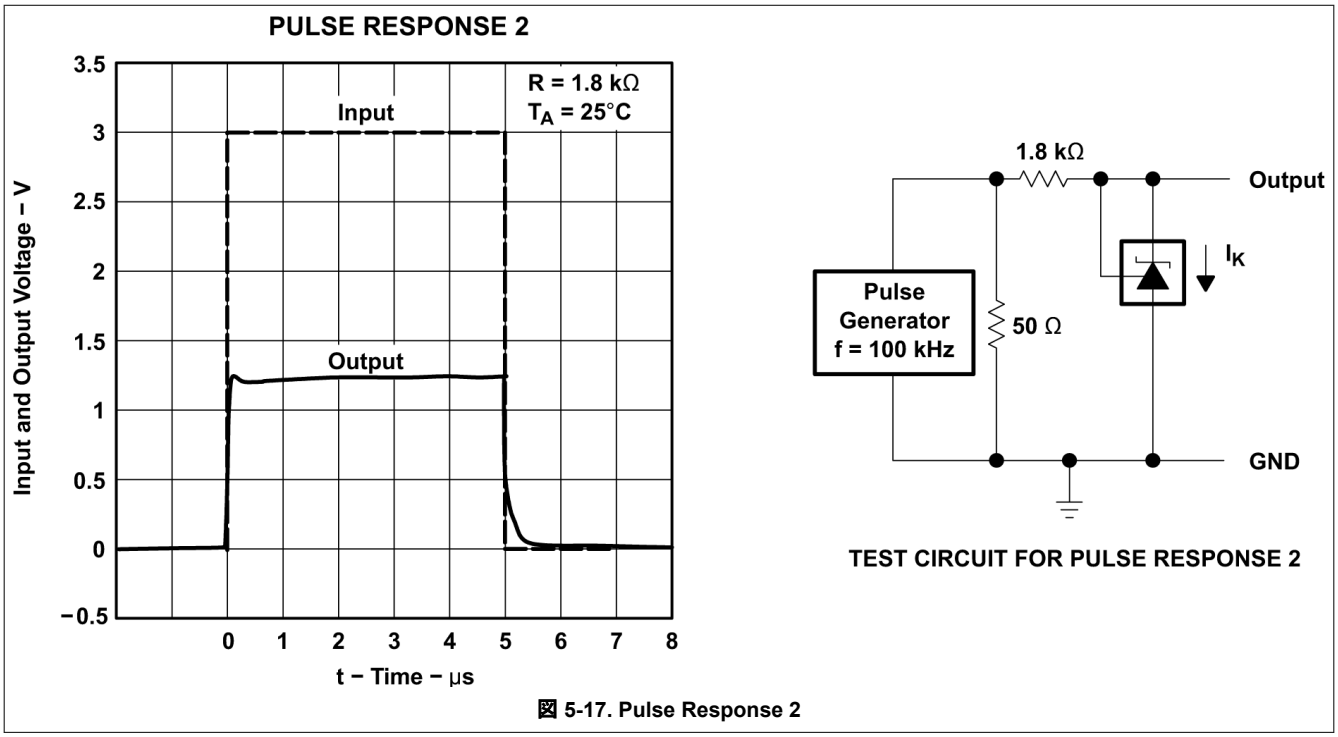
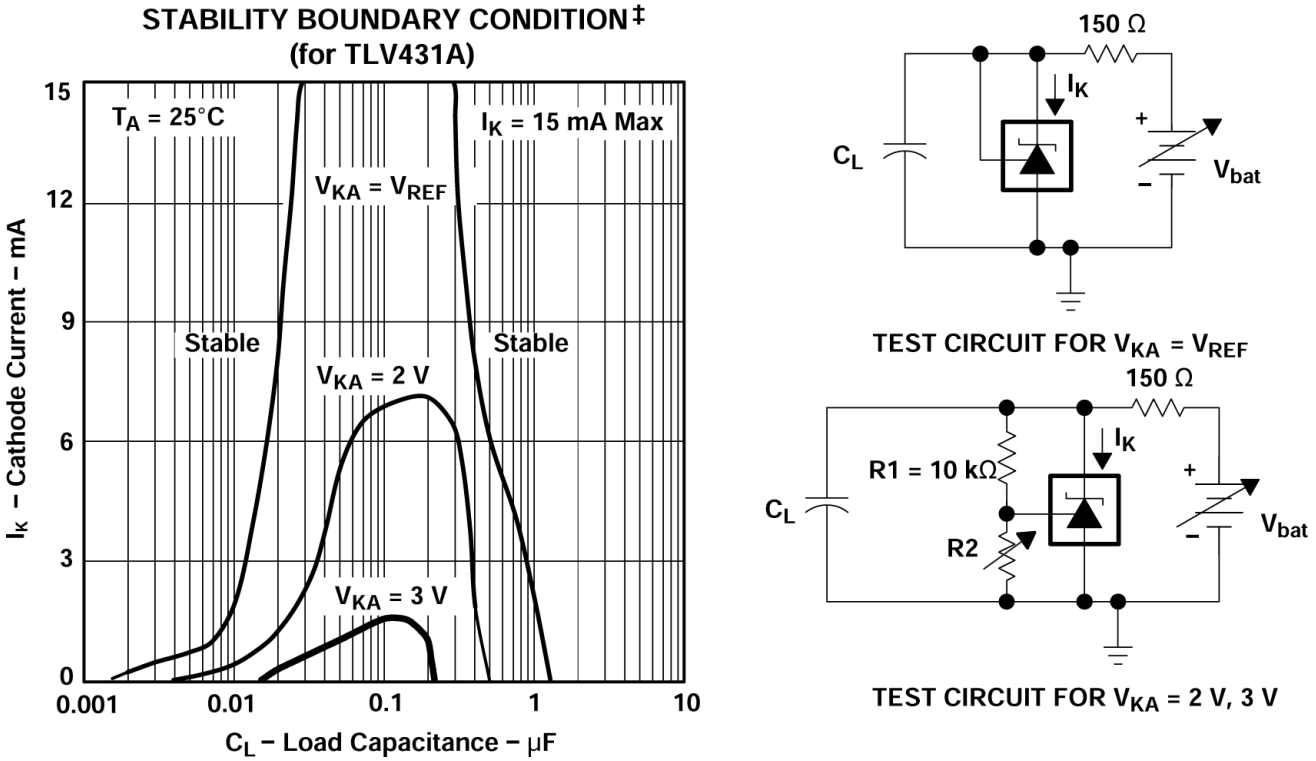


図 5-17. Pulse Response 2

Copyright © 2025 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



‡The areas under the curves represent conditions that can cause the device to oscillate. For V_{KA} = 2V and 3V curves, R2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{bat} and C_L then were adjusted to determine the ranges of stability.

図 5-18. Stability Boundary Conditions

Copyright © 2025 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

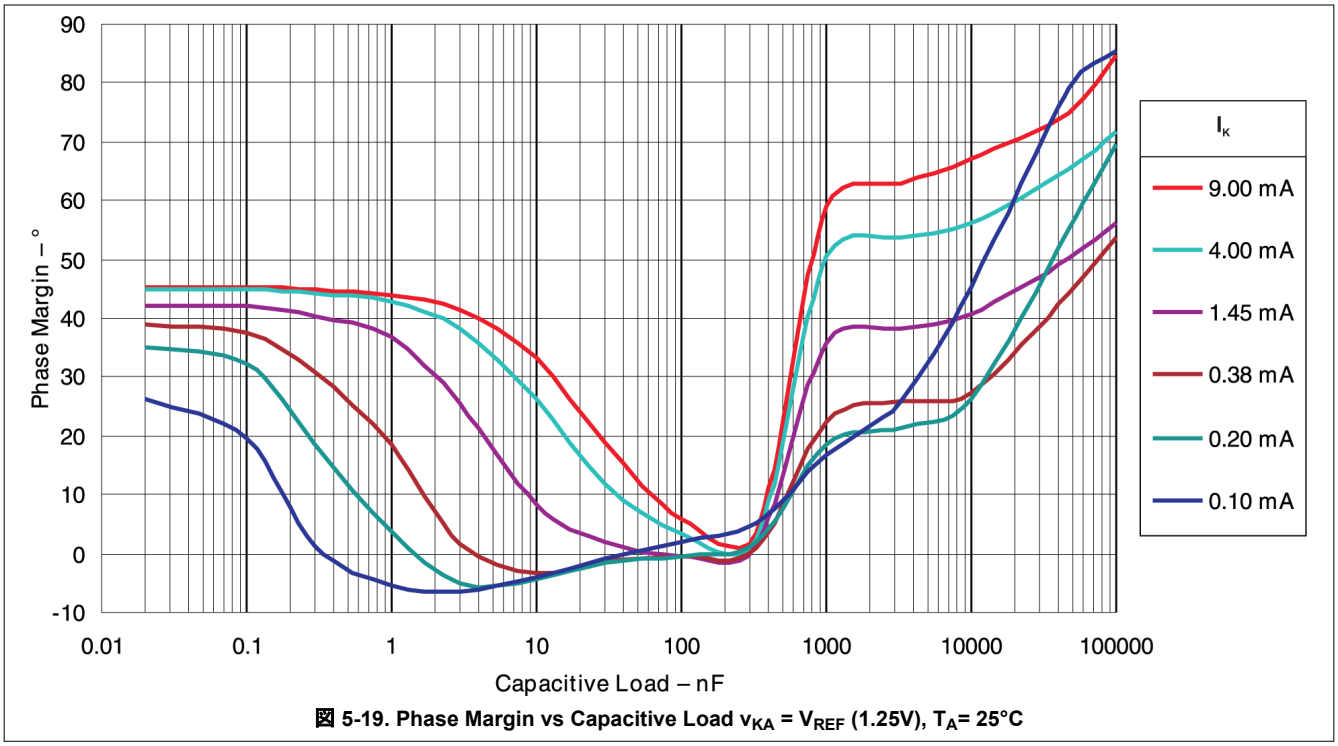


図 5-19. Phase Margin vs Capacitive Load $v_{KA} = V_{REF}$ (1.25V), T_A= 25°C

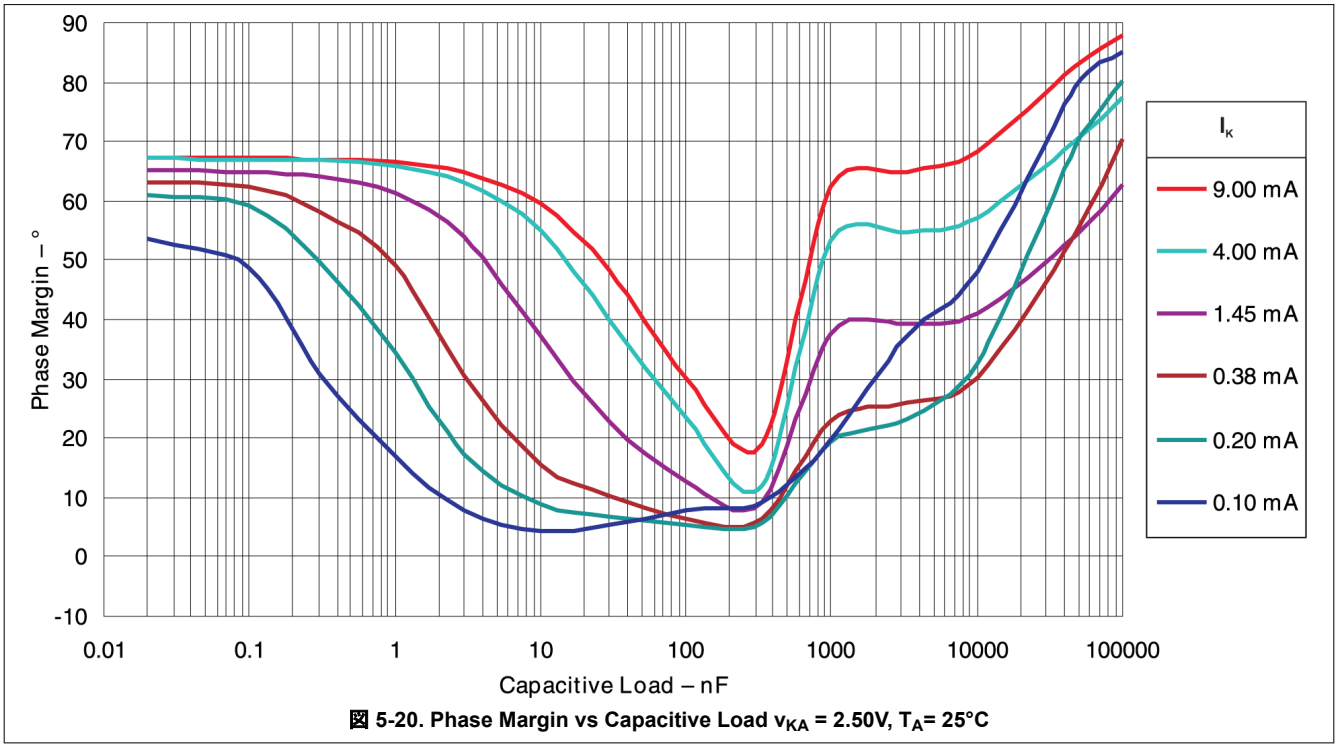


図 5-20. Phase Margin vs Capacitive Load v_{KA} = 2.50V, T_A= 25°C

Copyright © 2025 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

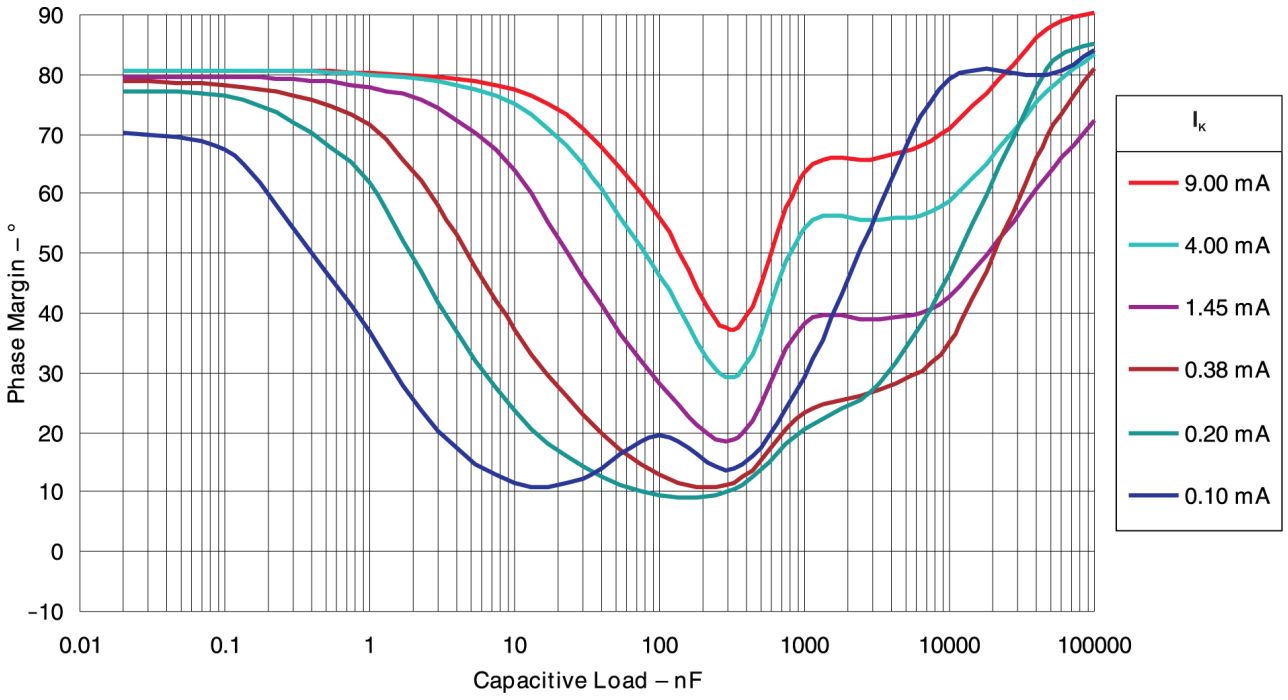


図 5-21. Phase Margin vs Capacitive Load v_{KA} = 5.00V, T_A= 25°C

Copyright © 2025 Texas Instruments Incorporated

6 Parameter Measurement Information

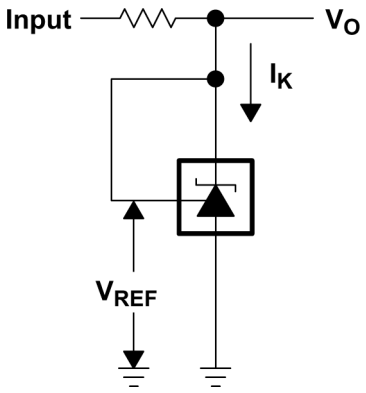


図 6-1. Test Circuit for $v_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

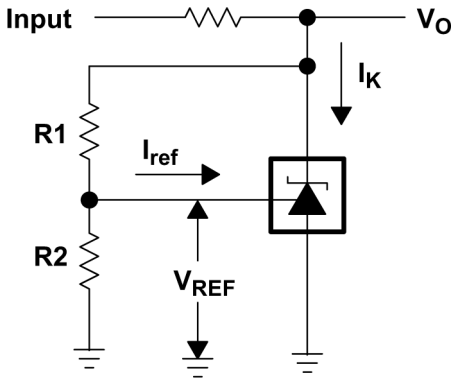


図 6-2. Test Circuit for $v_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1/R2) + I_{ref} \times R1$

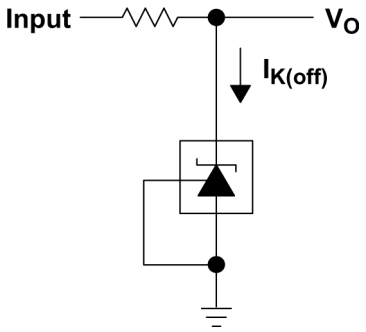


図 6-3. Test Circuit for $I_{K(off)}$

Copyright © 2025 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

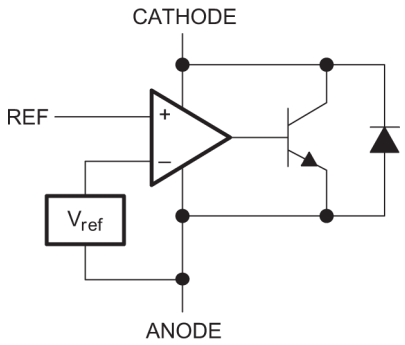
TLV431 is a low power counterpart to TL431, having lower reference voltage (1.24V vs 2.5 V) for lower voltage adjustability and lower minimum cathode current ($I_{k(min)}$= 100µA vs 1mA). Like TL431, TLV431 is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference.

TLV431 can be operated and adjusted to cathode voltages from 1.24V to 6V, making this part optimum for a wide range of end equipments in industrial, auto, telecom, and computing. For this device to behave as a shunt regulator or error amplifier, > 100µA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, 1%, and 1.5%. These reference options are denoted by B (0.5%), A (1.0%), and blank (1.5%) after the TLV431.

The TLV431xC devices are characterized for operation from 0°C to 70°C, the TLV431xI devices are characterized for operation from –40°C to 85°C, and the TLV431xQ devices are characterized for operation from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

TLV431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal darlington pair.

When operated with enough voltage headroom (≥ 1.24V) and cathode current (Ika), TLV431 forces the reference pin to 1.24V. However, the reference pin can not be left floating, as it requires I_{ref} ≥ 0.5µA (see the *Functional Block Diagram*). This is because the reference pin is driven into an NPN, which requires a base current to operate properly.

When feedback is applied from the Cathode and Reference pins, TLV431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current required in the above feedback situation must be applied to this device in open-loop, servo, or error-amplifying implementations for it to be in the proper linear region giving TLV431 enough gain.

Unlike many linear regulators, TLV431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor 図 5-19 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

Copyright © 2025 Texas Instruments Incorporated

7.4 Device Functional Modes

7.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TLV431 is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TLV431 will have the characteristics shown in 図 5-6. With such high gain in this configuration, TLV431 is typically used as a comparator. With the reference integrated makes TLV431 the preferred choice when users are trying to monitor a certain level of a single signal.

7.4.2 Closed Loop

When the cathode/output voltage or current of TLV431 is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLV431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

Copyright © 2025 Texas Instruments Incorporated

8 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

図 8-1 shows the TLV431, TLV431A, or TLV431B used in a 3.3V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} (1.24V ± 1%). The output of the regulator, plus the forward voltage drop of the optocoupler LED (1.24 + 1.4 = 2.64V), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the topology shown in 図 8-1.

The 431 family of devices are prevalent in these applications, being designers go to choice for secondary side regulation. Due to this prevalence, this section will further go on to explain operation and design in both states of TLV431 that this application will see, open loop (Comparator + Vref) and closed loop (Shunt Regulator).

Further information about system stability and using a TLV431 device for compensation can be found in the application note *Compensation Design With TL431 for UCC28600* (SLUA671).

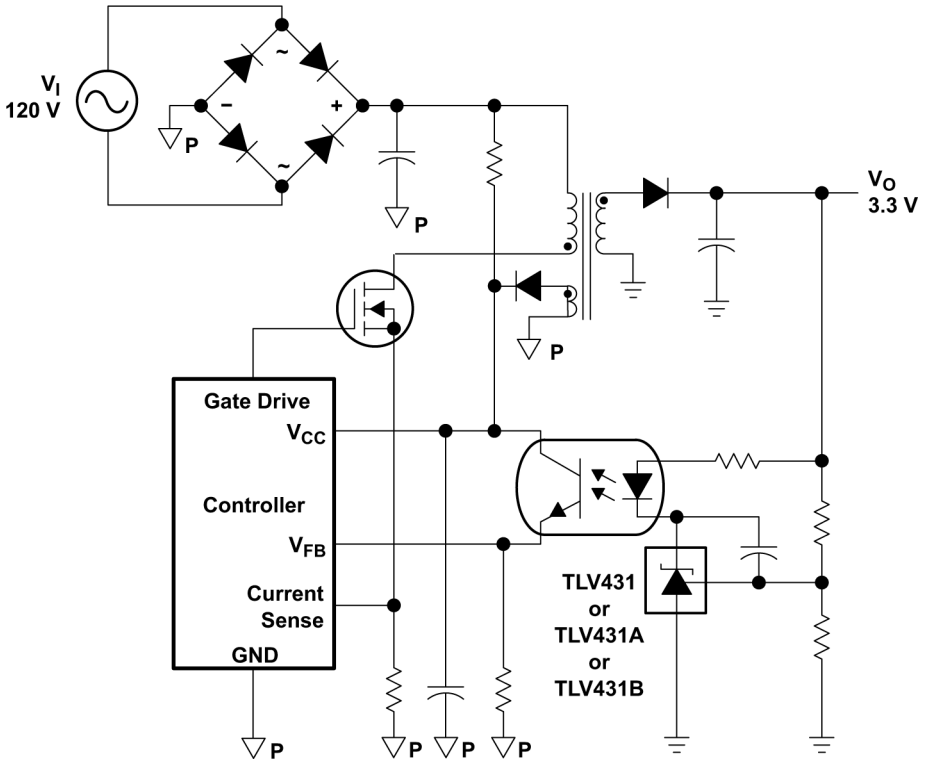


図 8-1. Flyback with Isolation Using TLV431, TLV431A, or TLV431B as Voltage Reference and Error Amplifier

Copyright © 2025 Texas Instruments Incorporated

8.2 Typical Applications

8.2.1 Comparator with Integrated Reference (Open Loop)

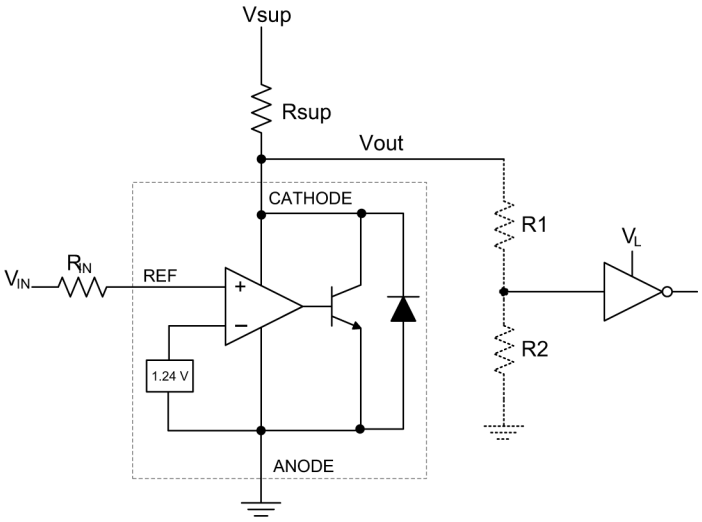


図 8-2. Comparator Application Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to 5V
Input Resistance	10kΩ
Supply Voltage	5V
Cathode Current (Ik)	500µA
Output Voltage Level	~1V - Vsup
Logic Input Thresholds VIH/VIL	VL

8.2.1.2 Detailed Design Procedure

When using TLV431 as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

8.2.1.2.1 Basic Operation

In the configuration shown in 図 8-2 TLV431 will behave as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), TLV431 will have enough open-loop gain to provide a quick response. With the TLV431's maximum operating current (I_{min}(max)) being 100µA and up to 150µA over temperature, operation below that could result in low gain, leading to a slow response.

8.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 1.24V ±(0.5%, 1.0%, or 1.5%) depending on which version is being used.

Copyright © 2025 Texas Instruments Incorporated

The more overdrive voltage provided, the faster the TLV431 will respond. This can be seen in 図 8-3 and 図 8-4 where it displays the output responses to various input voltages.

For applications where TLV431 is being used as a comparator, it is best to set the trip point to greater than the positive expected error (that is, +1.0% for the A version). For fast response, setting the trip point to > 10% of the internal V_{ref} should suffice.

For minimal voltage drop or difference from Vin to the ref pin, TI recommends using an input resistor < 10kΩ to provide I_{ref}.

8.2.1.2.3 Output Voltage and Logic Input Level

For the TLV431 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL}.

As seen in 図 8-3, TLV431's output low level voltage in open-loop/comparator mode is approximately 1V, which is sufficient for some 3.3V supplied logic. However, this does not work for 2.5V or 1.8V supplied logic. To accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TLV431's output high voltage is approximately V_{sup} due to TLV431 being open-collector. If V_{sup} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 and R2 in 図 8-2) is much greater than R_{sup} to not interfere with TLV431's ability to pull close to V_{sup} when turning off.

8.2.1.2.3.1 Input Resistance

TLV431 requires an input resistance in this application to source the reference current (I_{ref}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{ref} = V_{in} – I_{ref} × R_{in}$. Because the I_{ref} can be as high as 0.5µA, TI recommends using a resistance small enough that will mitigate the error that I_{ref} creates from V_{in}.

8.2.1.3 Application Curves

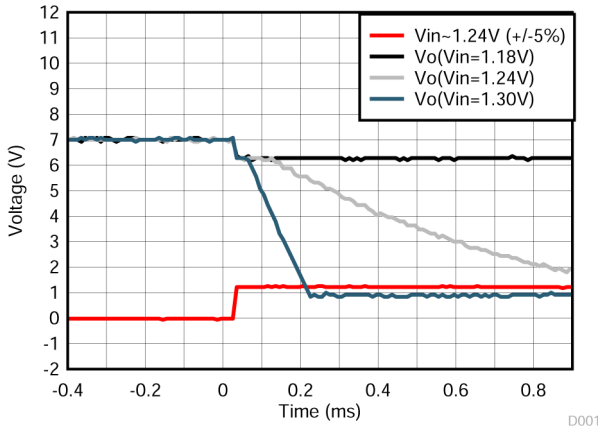


図 8-3. Output Response with Small Overdrive Voltages

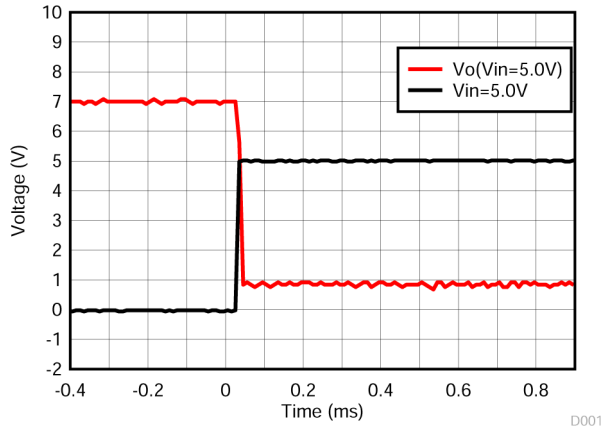


図 8-4. Output Response with Large Overdrive Voltage

Copyright © 2025 Texas Instruments Incorporated

8.2.2 Shunt Regulator/Reference

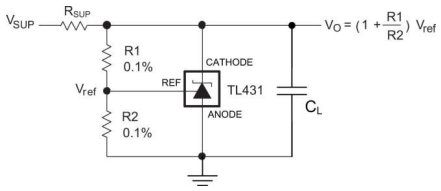


図 8-5. Shunt Regulator Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	6V
Cathode Current (Ik)	1mA
Output Voltage Level	1.24V - 6V
Load Capacitance	100pF
Feedback Resistor Values and Accuracy (R1 and R2)	10kΩ

8.2.2.2 Detailed Design Procedure

When using TLV431 as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

8.2.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in 図 8-5, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in 図 8-5. The cathode voltage can be more accurately determined by taking the cathode current in to account

$$V_O = (1 + R1 / R2) \times V_{ref} – I_{ref} \times R1 \quad (1)$$

For Equation 1 to be valid, TLV431 must be fully biased so that it has enough open-loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in *Recommended Operating Conditions* table.

8.2.2.2.2 Total Accuracy

When programming the output above unity gain (Vka = Vref), TLV431 is susceptible to other errors that may effect the overall accuracy beyond V_{ref}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ – Change in reference voltage over temperature
- $\Delta V_{ref} / \Delta V_{KA}$ – Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ – Dynamic impedance, causing a change in cathode voltage with cathode current

Copyright © 2025 Texas Instruments Incorporated

Worst-case cathode voltage can be determined taking all of the variables in to account. Application note Setting the Shunt Voltage on an Adjustable Shunt Regulator (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

8.2.2.2.3 Stability

Though TLV431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TLV431 region of stability, shown in 図 5-18. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling.

8.2.2.3 Application Curve

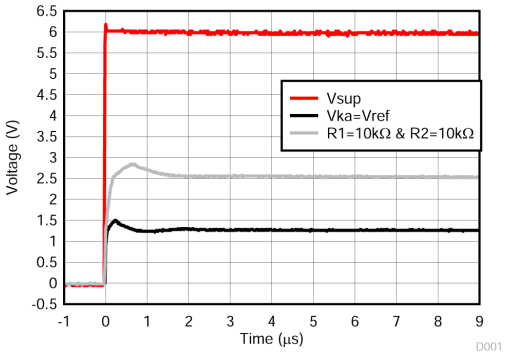


図 8-6. TLV431 Start-Up Response

8.3 Power Supply Recommendations

When using TLV431 as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in 図 5-18.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed the absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

8.4 Layout

8.4.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

8.4.2 Layout Example

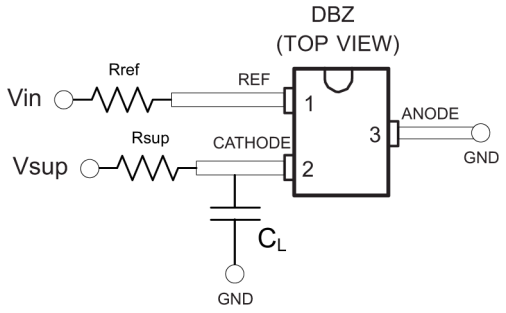


図 8-7. DBZ Layout Example

Copyright © 2025 Texas Instruments Incorporated

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Compensation Design With TL431 for UCC28600 (SLUA671)
- Setting the Shunt Voltage on an Adjustable Shunt Regulator (SLVA445)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision Y (March 2024) to Revision Z (June 2024)	Page
• Updated pinout diagrams	3

Changes from Revision X (May 2018) to Revision Y (March 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 概略回路図を「概要」から「アプリケーション」に移動	1
• Updated pinout diagrams	3
• Updated *Typical Applications Design Requiements*	23

Copyright © 2025 Texas Instruments Incorporated

Changes from Revision W (March 2018) to Revision X (May 2018) **Page**

- Changed 図 5-18 8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Copyright © 2025 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431ACDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI, YACN) (YACG, YACL, YACS)
TLV431ACDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI, YACN) (YACG, YACL, YACS)
TLV431ACDBVR1G4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI) (YACG, YACL, YACS)
TLV431ACDBVR1G4.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI) (YACG, YACL, YACS)
TLV431ACDBVRG4	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	0 to 70	YACI
TLV431ACDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI) (YACG, YACL, YACS)
TLV431ACDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI) (YACG, YACL, YACS)
TLV431ACDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YAC6, YAC8, YACB, YACS) (YAC3, YACS, YACU)
TLV431ACDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YAC8, YACB, YACS) (YAC3, YACS, YACU)
TLV431ACDBZRG4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	YAC6 YACS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431ACDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	YAC6 YACS
TLV431ACLP	NRND	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 70	V431AC
TLV431ACLP.A	NRND	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 70	V431AC
TLV431ACLPR	NRND	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	V431AC
TLV431ACLPR.A	NRND	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	V431AC
TLV431AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	TY431A
TLV431AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII, YAIN) (YAIG, YAIL, YAIS)
TLV431AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII, YAIN) (YAIG, YAIL, YAIS)
TLV431AIDBVR1G4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC) (YAIL, YAIS)
TLV431AIDBVR1G4.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC) (YAIL, YAIS)
TLV431AIDBVRG4	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	YAII
TLV431AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII) (YAIG, YAIL, YAIS)
TLV431AIDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII) (YAIG, YAIL, YAIS)
TLV431AIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAI8, YAIB, YAIS) (YAI3, YAIS, YAIU)
TLV431AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAI8, YAIB, YAIS) (YAI3, YAIS, YAIU)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431AIDBZRG4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	YAI6 YAIS
TLV431AIDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAI6 YAIS
TLV431AIDE4	NRND	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	
TLV431AIDR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A
TLV431AIDR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A
TLV431AIDRE4	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV431AILP	Obsolete	Production	TO-92 (LP) | 3	-	-	Call TI	Call TI	-40 to 85	V431AI
TLV431AILPM	NRND	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 85	V431AI
TLV431AILPM.A	NRND	Production	TO-92 (LP) | 3	2000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 85	V431AI
TLV431AILPR	NRND	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	V431AI
TLV431AILPR.A	NRND	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	V431AI
TLV431AQPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VA
TLV431AQPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VA
TLV431BCDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)
TLV431BCDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)
TLV431BCDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)
TLV431BCDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)
TLV431BCDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3G3, Y3GS, Y3GU)
TLV431BCDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(Y3G3, Y3GS, Y3GU)
TLV431BCDBZT	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3GS, Y3GU)
TLV431BCDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(Y3GS, Y3GU)
TLV431BCDBZTG4	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	Y3GS
TLV431BCDBZTG4.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	Y3GS
TLV431BCDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	YEU

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431BCDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	YEU
TLV431BCDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	YEU
TLV431BCDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	YEU
TLV431BCLP	Obsolete	Production	TO-92 (LP) | 3	-	-	Call TI	Call TI	0 to 70	TV431B
TLV431BCLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	TV431B
TLV431BCLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	TV431B
TLV431BCPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 70	VE
TLV431BCPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 70	VE
TLV431BIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)
TLV431BIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)
TLV431BIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)
TLV431BIDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)
TLV431BIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS, Y3FU)
TLV431BIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS, Y3FU)
TLV431BIDBZRG4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS)
TLV431BIDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS)
TLV431BIDBZT	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3FS, Y3FU)
TLV431BIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3FS, Y3FU)
TLV431BIDBZTG4.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3FS
TLV431BIDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	YFU
TLV431BIDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YFU
TLV431BIDCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU
TLV431BIDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU
TLV431BIDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	YFU
TLV431BIDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YFU
TLV431BILP	Obsolete	Production	TO-92 (LP) | 3	-	-	Call TI	Call TI	-40 to 85	TY431B
TLV431BILPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	TY431B
TLV431BILPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	TY431B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431BIPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	VF
TLV431BIPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	VF
TLV431BQDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)
TLV431BQDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)
TLV431BQDBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV431BQDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y3HU
TLV431BQDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y3HU
TLV431BQDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)
TLV431BQDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)
TLV431BQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3H3, Y3HS, Y3HU)
TLV431BQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(Y3H3, Y3HS, Y3HU)
TLV431BQDBZRG4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	Y3HS
TLV431BQDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y3HS
TLV431BQDBZT	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3HS, Y3HU)
TLV431BQDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(Y3HS, Y3HU)
TLV431BQDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	YGU
TLV431BQDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	YGU
TLV431BQDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	YGU
TLV431BQDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	YGU
TLV431BQLP	Obsolete	Production	TO-92 (LP) | 3	-	-	Call TI	Call TI	-40 to 125	TQ431B
TLV431BQLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	TQ431B
TLV431BQLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	TQ431B
TLV431BQPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V6
TLV431BQPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V6
TLV431CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)
TLV431CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)
TLV431CDBVRG4	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	0 to 70	Y3CI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)
TLV431CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)
TLV431CDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3C8, Y3CB, Y3CS) (Y3C3, Y3CS, Y3CU)
TLV431CDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3C8, Y3CB, Y3CS) (Y3C3, Y3CS, Y3CU)
TLV431CLP	Obsolete	Production	TO-92 (LP) | 3	-	-	Call TI	Call TI	0 to 70	V431C
TLV431CLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	V431C
TLV431CLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	V431C
TLV431IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)
TLV431IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)
TLV431IDBVR1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3I6 Y3IS
TLV431IDBVR1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3I6 Y3IS
TLV431IDBVRG4	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	Y3II
TLV431IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)
TLV431IDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)
TLV431IDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3IB, Y3IS) (Y3IU, Y3IU)
TLV431IDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3IB, Y3IS) (Y3IU, Y3IU)
TLV431IDBZRG4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	Y3I6 Y3IS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431IDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3I6 Y3IS
TLV431ILP	Obsolete	Production	TO-92 (LP) | 3	-	-	Call TI	Call TI	-40 to 85	V431I
TLV431ILPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	V431I
TLV431ILPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	V431I
TLV431QPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VB
TLV431QPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV431A, TLV431B :

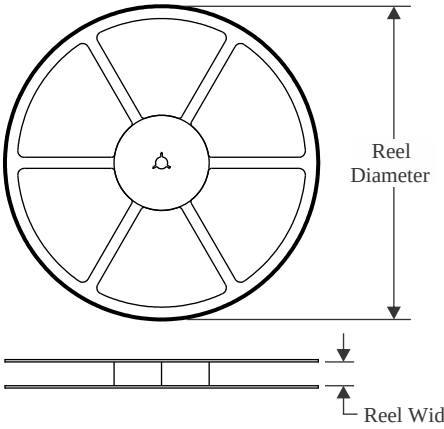
- Automotive : TLV431A-Q1, TLV431B-Q1

NOTE: Qualified Version Definitions:

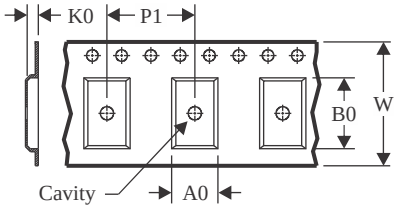
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

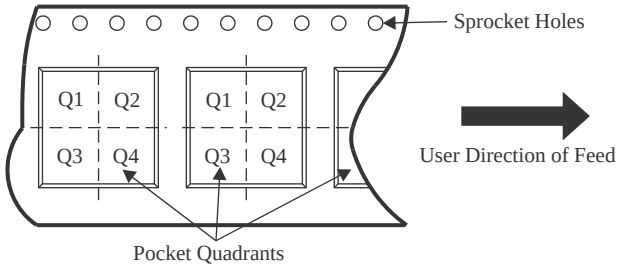


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



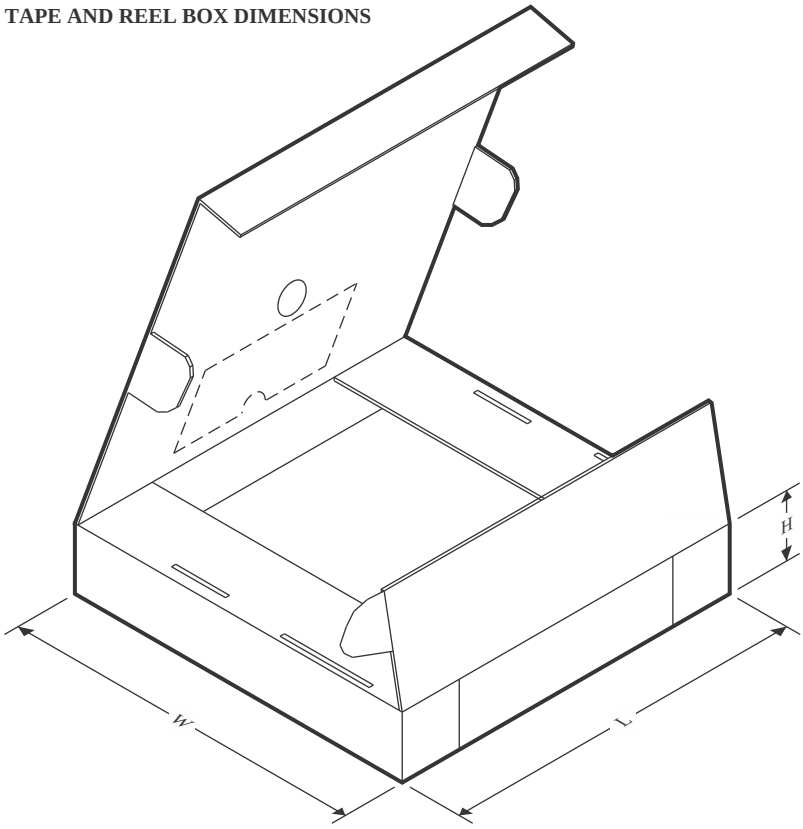
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431ACDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431ACDBVR1G4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVR1G4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431ACDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431ACDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431AIDBVR1G4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431AIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431AIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431AIDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431AIDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV431AQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431AQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BCDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BCDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BCDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431BCDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431BCDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV431BCDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BCDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BCDCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV431BCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431BIDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431BIDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIDCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV431BIDCKRG4	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIDCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV431BIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BQDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVRG4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431BQDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431BQDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BQDCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV431BQDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BQDCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV431BQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431IDBVR1G4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431IDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431IDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431IDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV431IDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431QPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431QPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431ACDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431ACDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431ACDBVR1G4	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431ACDBVR1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431ACDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431ACDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431ACDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431ACDBZRG4	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431AIDBVR1G4	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431AIDBZRG4	SOT-23	DBZ	3	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431AIDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV431AQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431AQPK	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV431BCDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BCDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431BCDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431BCDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV431BCDBZTG4	SOT-23	DBZ	3	250	210.0	185.0	35.0
TLV431BCDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TLV431BCDCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TLV431BCDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BCDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV431BCDCKT	SC70	DCK	6	250	210.0	185.0	35.0
TLV431BCPK	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV431BCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431BIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BIDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TLV431BIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BIDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431BIDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BIDBZRG4	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431BIDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV431BIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BIDCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TLV431BIDCKRG4	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV431BIDCKT	SC70	DCK	6	250	210.0	185.0	35.0
TLV431BIPK	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV431BIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BQDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431BQDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BQDBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BQDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TLV431BQDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431BQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431BQDBZRG4	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431BQDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BQDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV431BQDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TLV431BQDCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TLV431BQDCKT	SC70	DCK	6	250	200.0	183.0	25.0
TLV431BQDCKT	SC70	DCK	6	250	210.0	185.0	35.0
TLV431BQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BQPK	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV431CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431CDBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431CDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431IDBVR1G4	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV431IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431IDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431IDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431IDBZRG4	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV431IDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431QPK	SOT-89	PK	3	1000	190.0	190.0	30.0
TLV431QPK	SOT-89	PK	3	1000	340.0	340.0	38.0

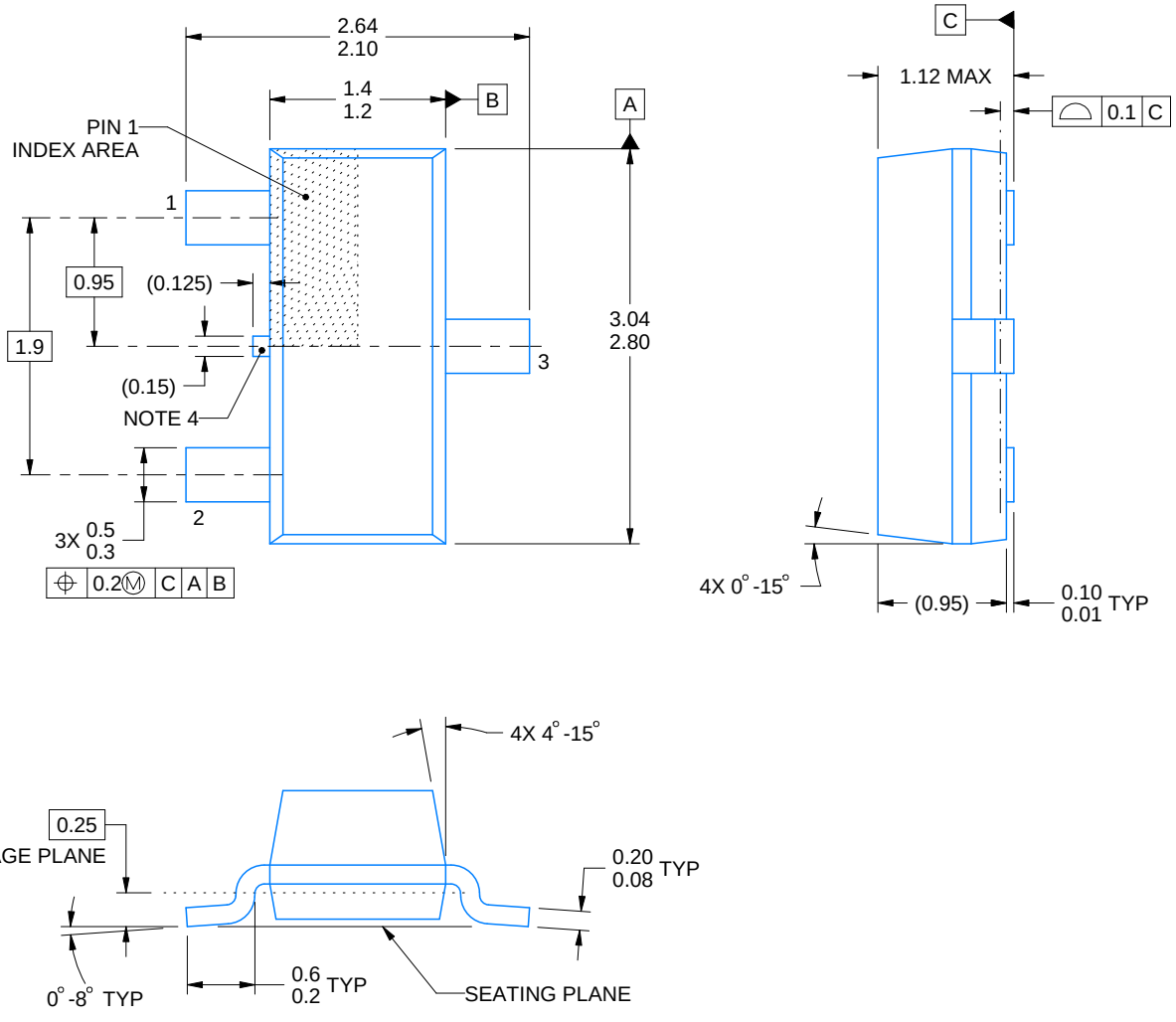
PACKAGE OUTLINE

DBZ0003A



SOT-23 - 1.12 mm max height

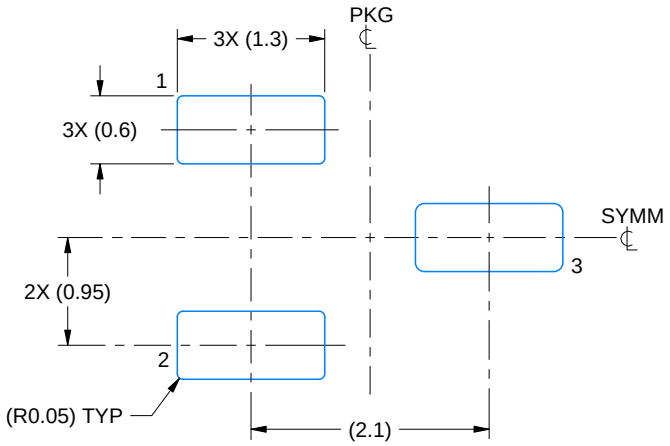
SMALL OUTLINE TRANSISTOR



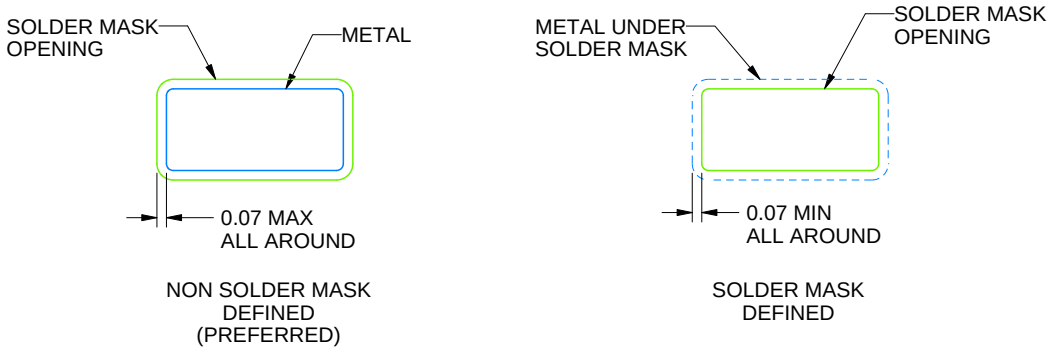
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

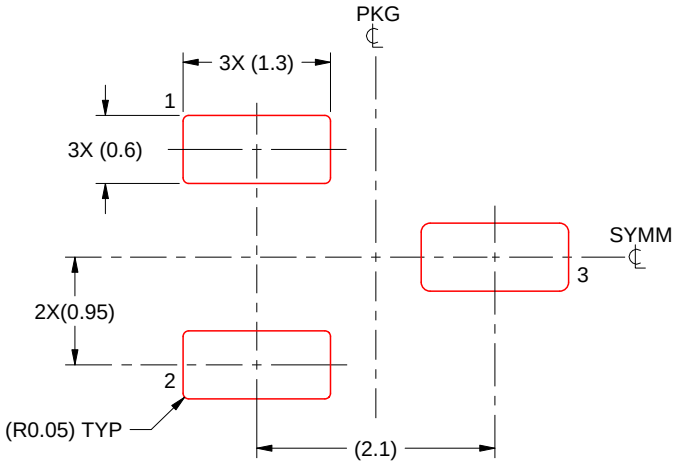


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



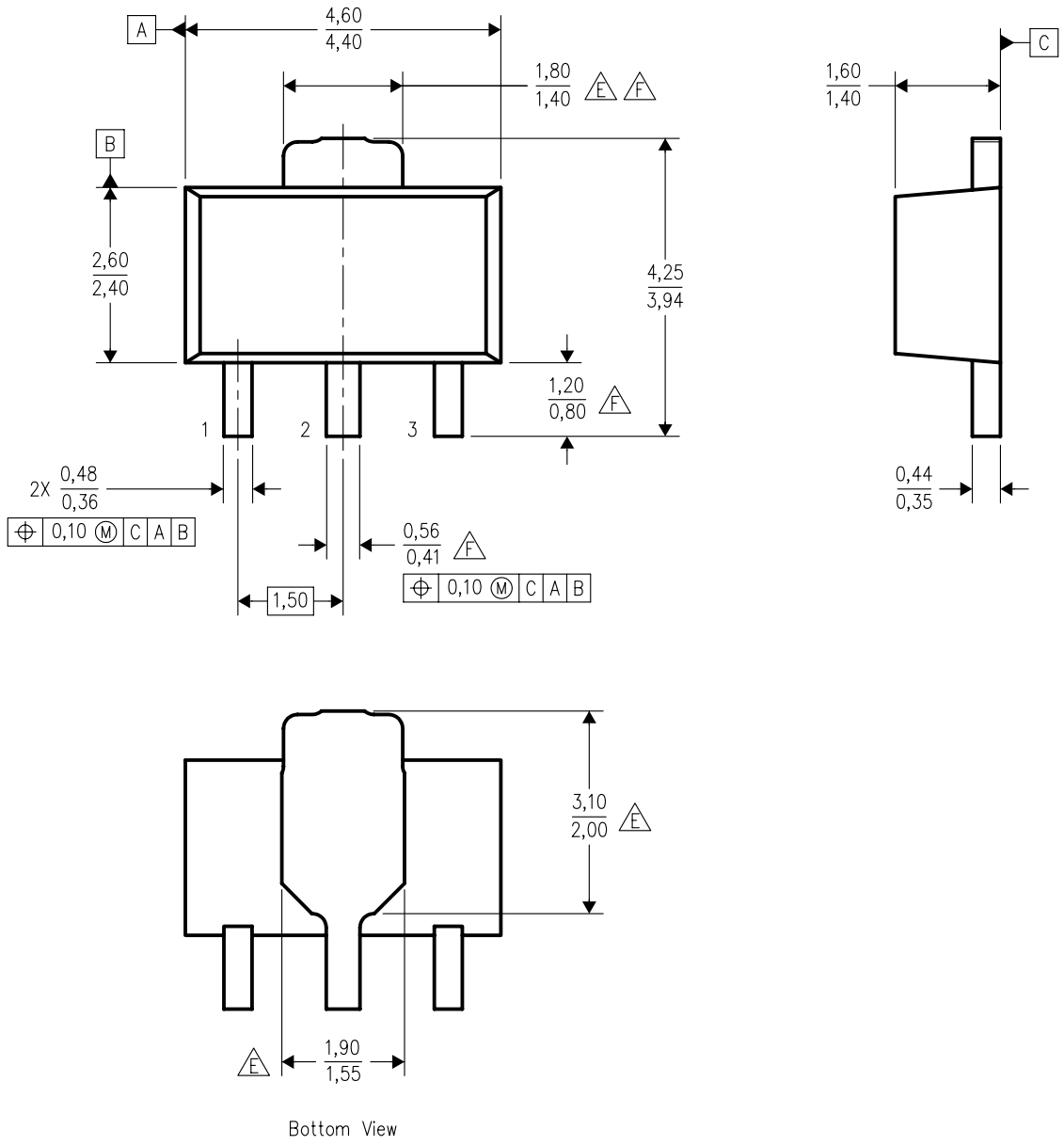
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

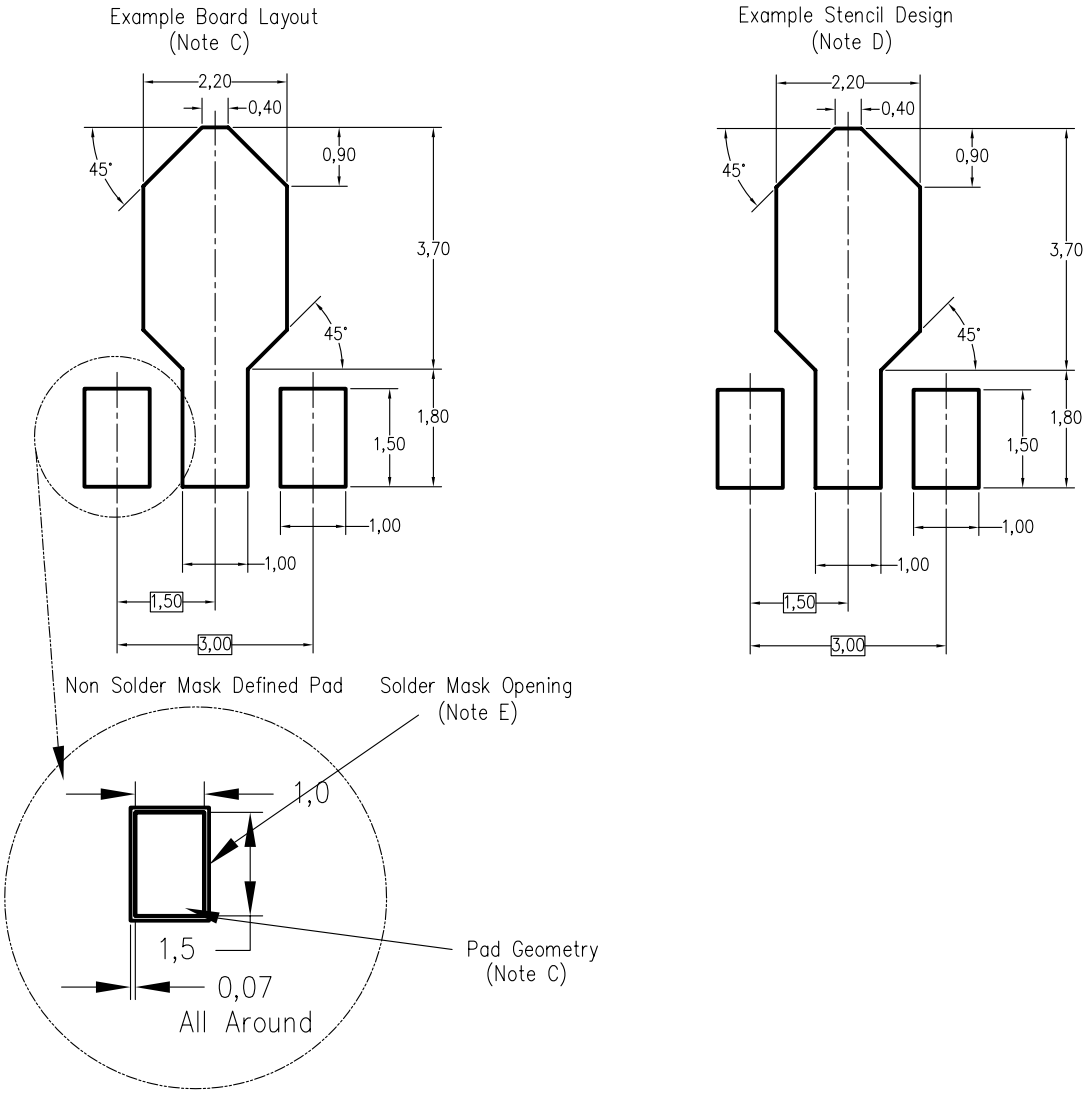
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

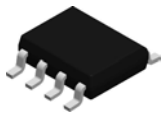
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)



4208221/A 09/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

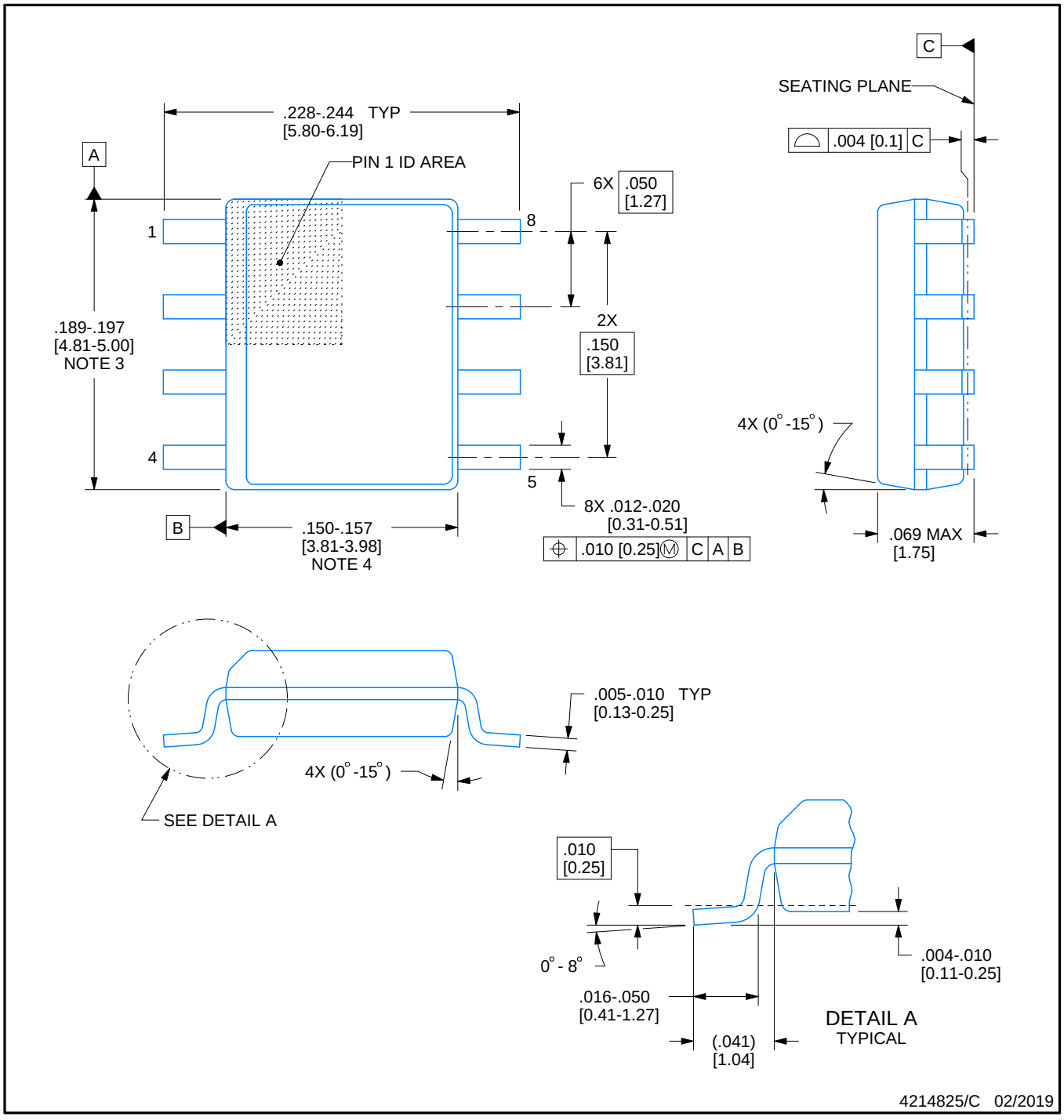


PACKAGE OUTLINE

D0008A

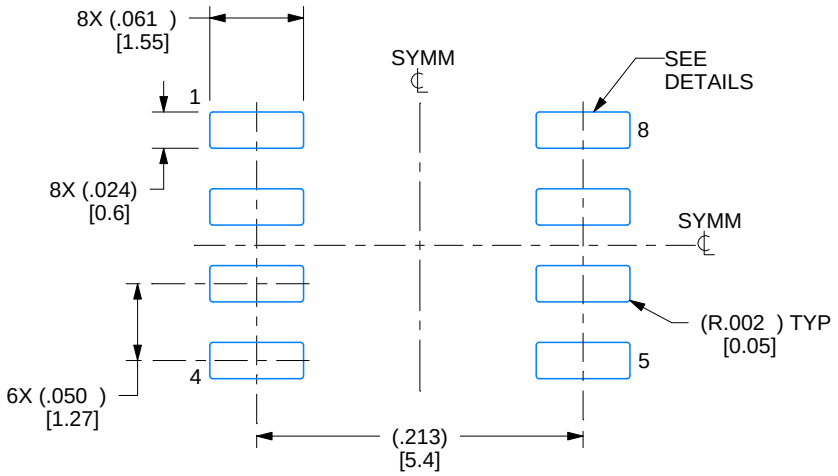
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

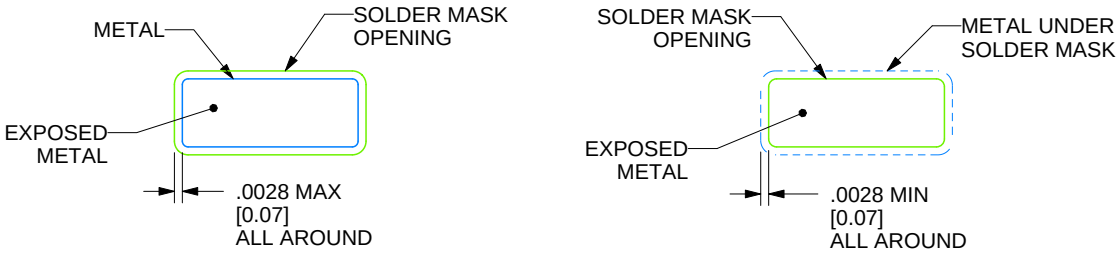


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

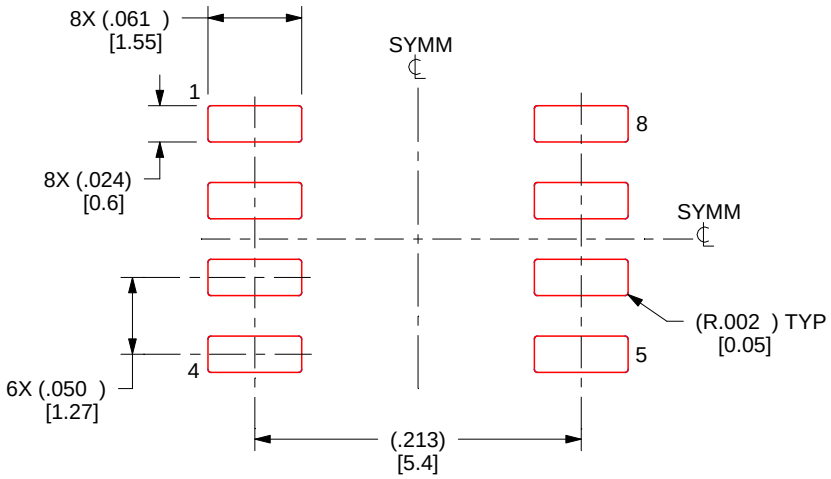
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

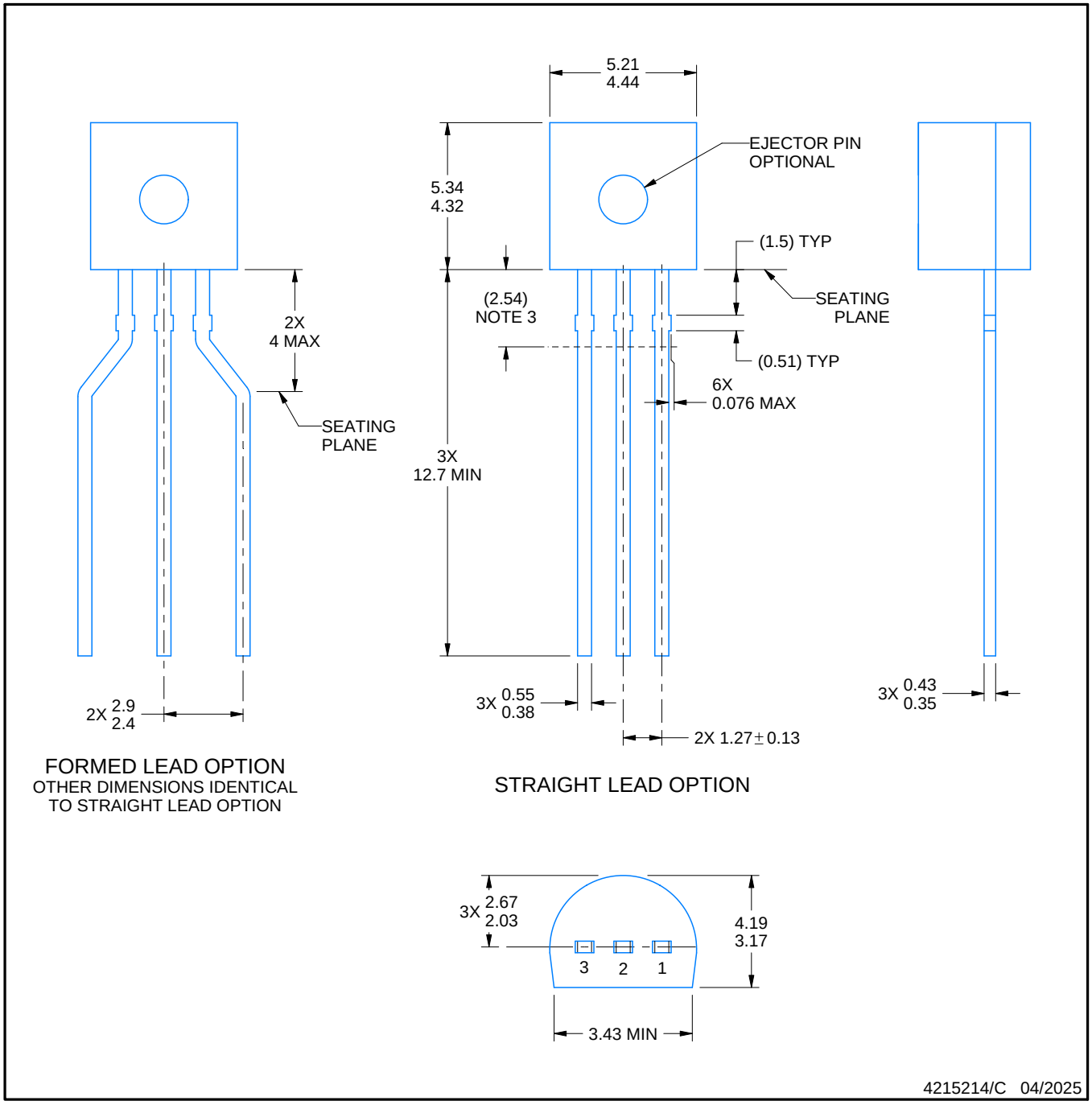
LP0003A



PACKAGE OUTLINE

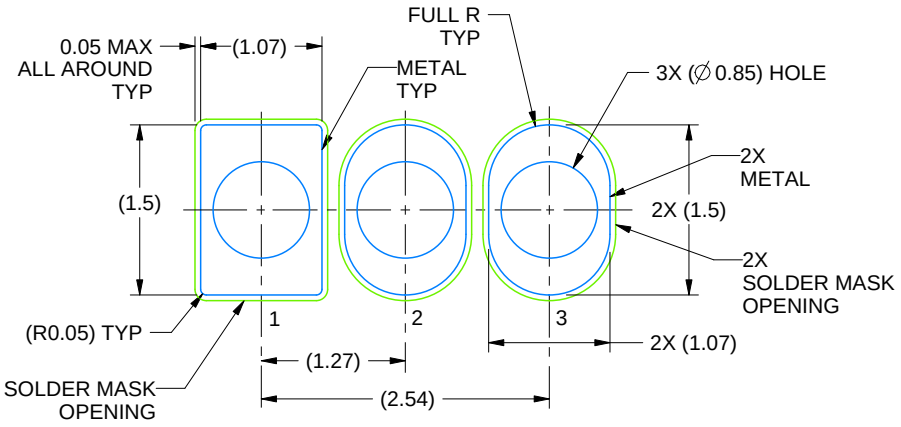
TO-92 - 5.34 mm max height

TO-92

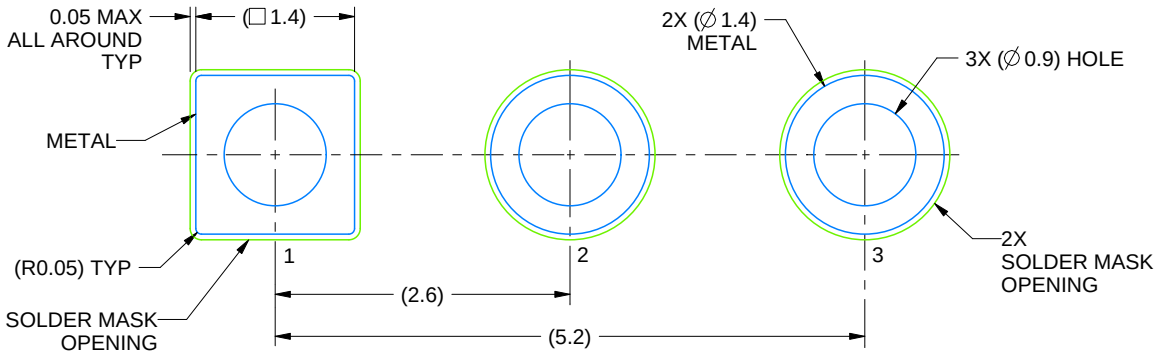


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



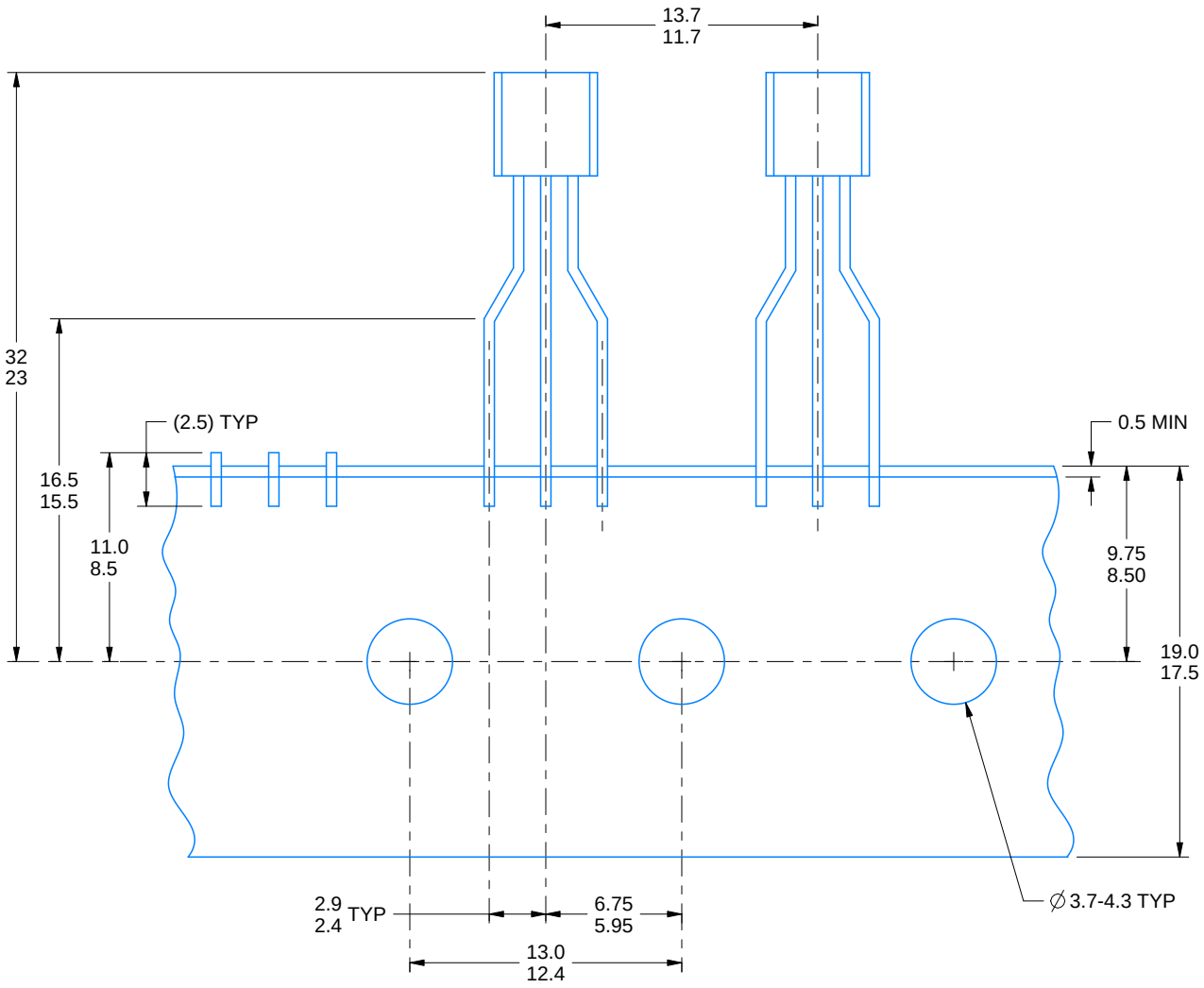
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

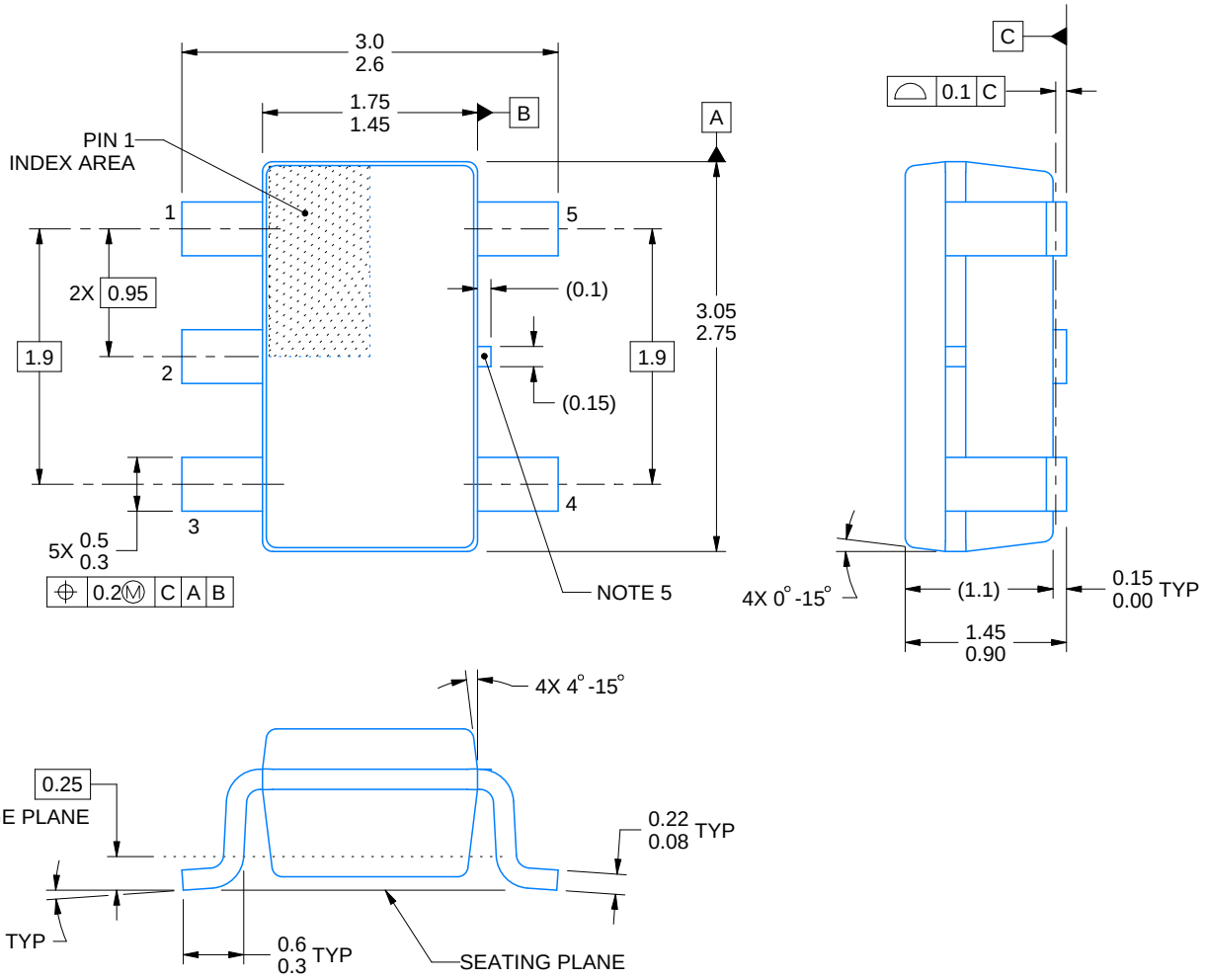
4215214/C 04/2025

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

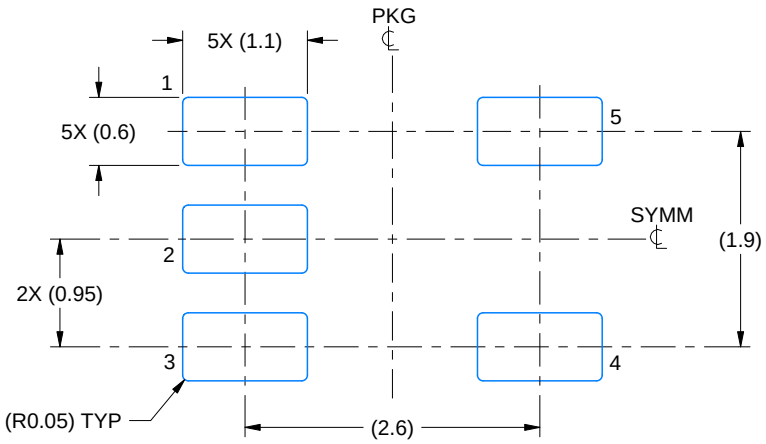
SMALL OUTLINE TRANSISTOR



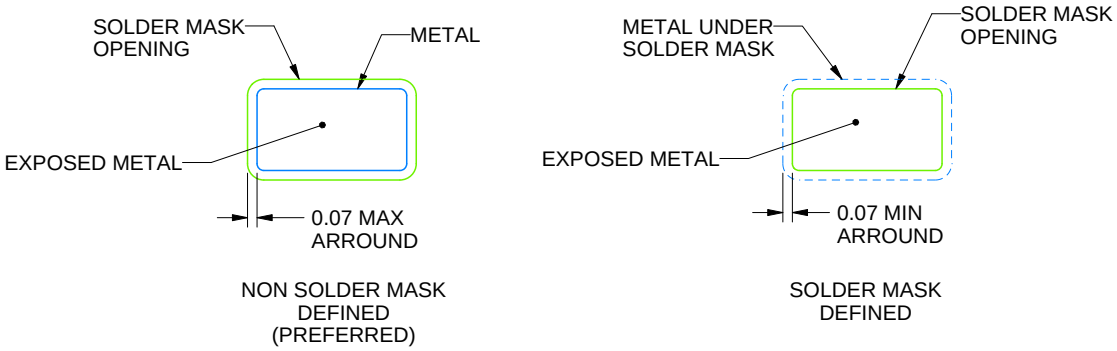
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

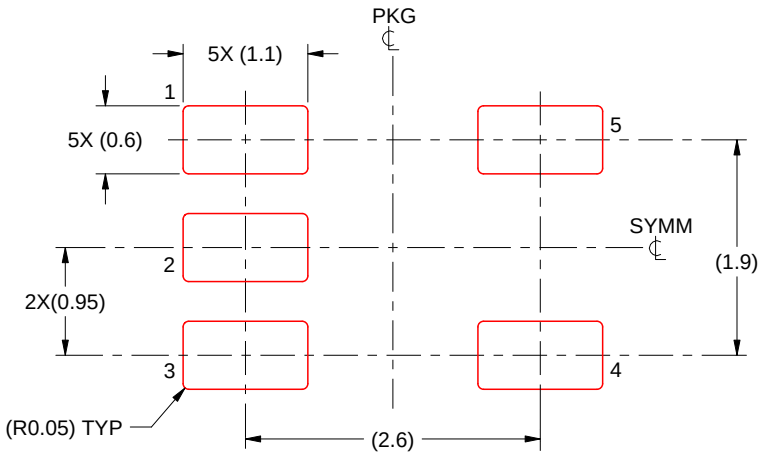


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

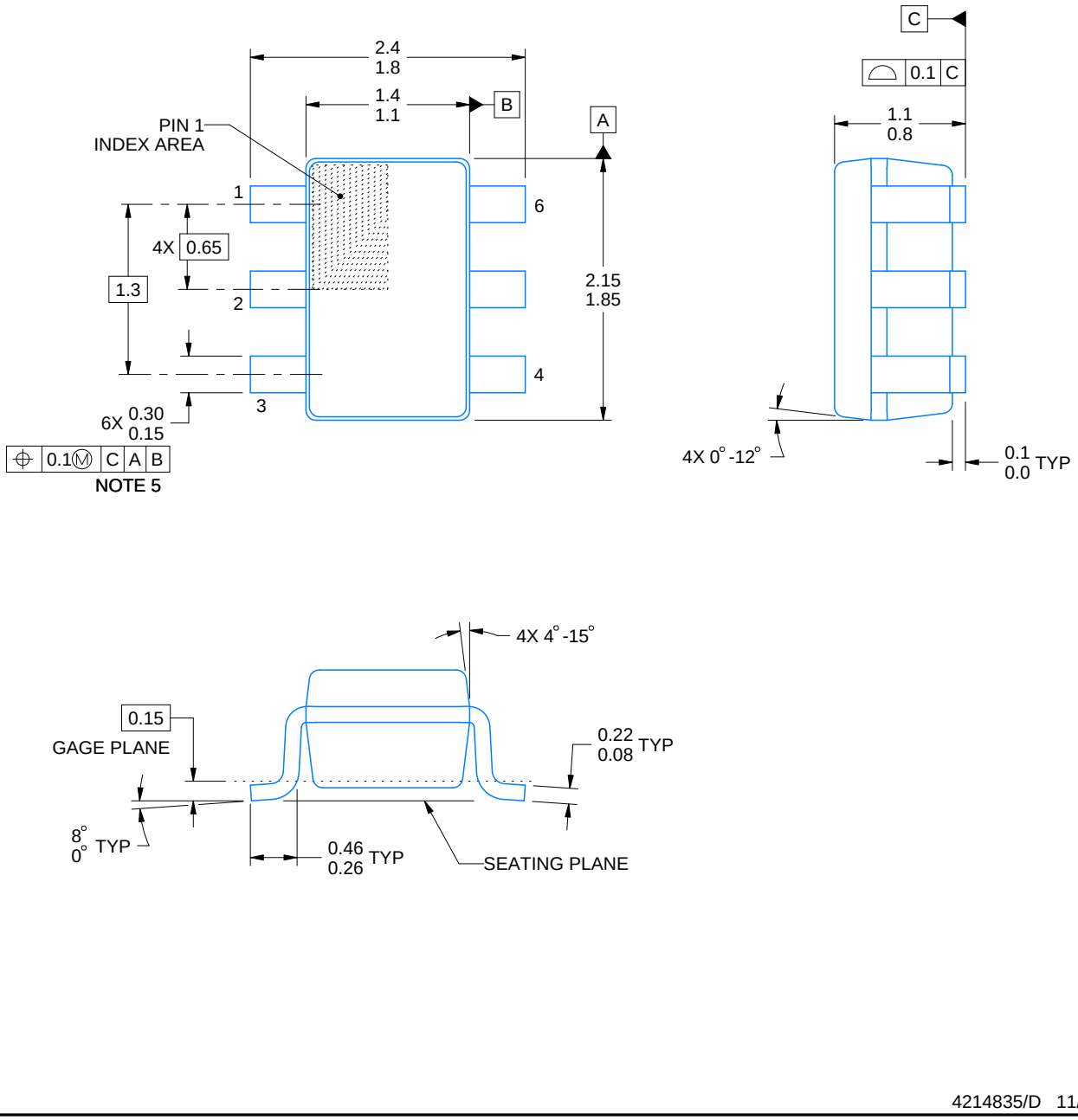
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

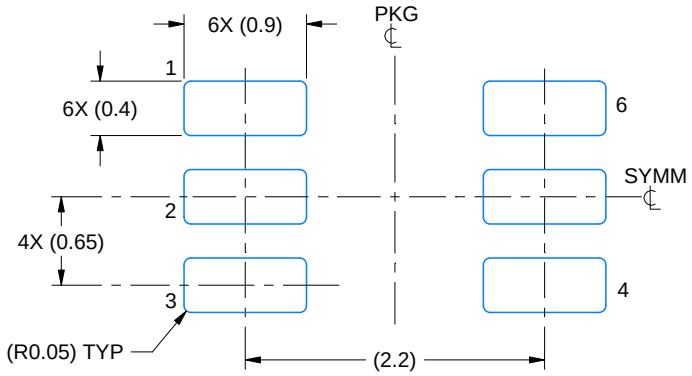
SMALL OUTLINE TRANSISTOR



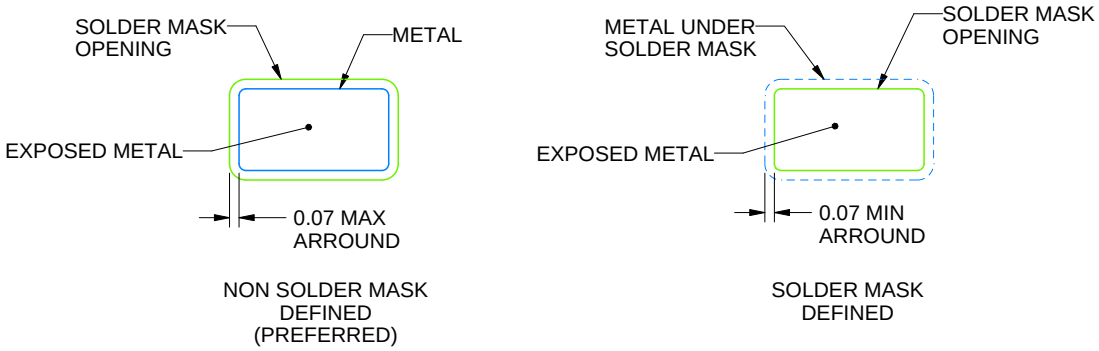
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

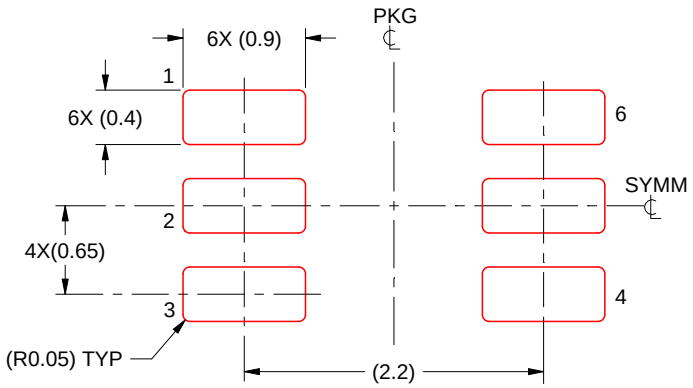


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月