参考資料

TLV431x-Q1 低電圧、高精度、可変シャント レギュレータ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃
- 低電圧動作、V_{REF} = 1.24V
- 可変出力電圧、V_O = V_{REF}～6V
- 25℃でのリファレンス電圧の公差
  - TLV431B: 0.5%
  - TLV431A: 1%
- 温度ドリフト (標準値)
  - 11mV (-40℃～125℃)
- 低い動作カソード電流:80μA (標準値)
- 出力インピーダンス:0.25Ω (標準値)
- 以下の事項は TLVH431 および TLVH432 を参照。
  - 広い V_{KA} (1.24V～18V) と I_K (80mA)
  - SOT-23-3 および SOT-89 パッケージで複数のピン配置を選択可能

2 アプリケーション

- 調整可能な基準電圧および電流
- フライバック SMPS の 2 次側レギュレーション
- ツェナーの代替品
- 電圧監視
- リファレンス電圧内蔵のコンパレータ

3 概要

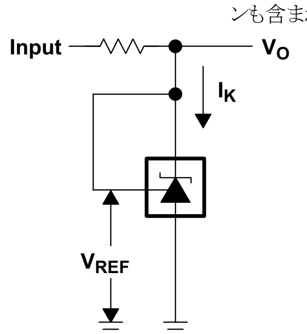
TLV431 デバイスは低電圧、3 端子の可変電圧リファレンスであり、該当する産業用および民生用温度範囲全体にわたって規定の熱的安定性を維持します。出力電圧は、スタンドアローン モードでは 1.24V、あるいは 2 つの外付け抵抗を用いて V_{REF} (1.24V) と 6V の間の任意の値に設定できます (図 6-2 を参照)。これらのデバイスは、広く使用されている TL431 および TL1431 シャント レギュレータ基準電圧よりも低い電圧(1.24V)で動作します。

TLV431 は、フォトカプラとともに使用すると 3V～3.3V のスイッチング モード用に設計された電源の、絶縁フィードバック回路における基準電圧となります。これらのデバイスの出力インピーダンスは 0.25Ω (標準値) です。アクティブ出力回路により、非常に鋭いターンオン特性を持つことから、オンボード レギュレーションや可変電源など多くのアプリケーションにおいて、低電圧ツェナー ダイオードの非常に優れた代替品となります。

製品情報

部品番号	パッケージ (ピン) (1)	本体サイズ (公称)(2)
TLV431x-Q1	SOT-23 (3)	2.90 mm × 1.30mm
	SOT-23 (5)	2.90 mm × 1.60mm

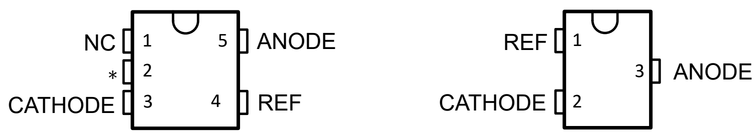
(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

Table of Contents

4 Pin Configuration and Functions



NC−No internal connection

∗ Pin 2 is attached to Substrate and must be connected to ANODE or left open.

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	DBV		
CATHODE	2	3	I/O	Shunt Current/Voltage input
REF	1	4	I	Threshold relative to common anode
ANODE	3	5	O	Common pin, normally connected to ground
NC	—	1	I	No Internal Connection
*	—	2	I	Substrate Connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{KA}	Cathode voltage[(2)]		7	V
I_K	Continuous cathode current range	–20	20	mA
I_{ref}	Reference current range	–0.05	3	mA
	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 5.4* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the anode terminal, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information

THERMAL METRIC[(1)]		TLV431x		UNIT
		DBV	DBZ	
		5 PINS	3 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	206	206	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	131	76	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		V_{REF}	6	V
I_K	Cathode current		0.1	15	mA
T_A	Operating free-air temperature range	TLV431x-Q1	–40	125	°C

5.5 Electrical Characteristics for TLV431A-Q1

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV431AQ			UNIT
				MIN	TYP	MAX	
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10mA	T_A = 25°C	1.228	1.24	1.252	V
			T_A = full range(1) (see 図 6-1)	1.209		1.271	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(2)	$V_{KA} = V_{REF}$, I_K = 10mA(1) (see 図 6-1)			11	31	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see 図 6-2)			–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see 図 6-2)			0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(2)	I_K = 10mA, R1 = 10kΩ, R2 = open(1) (see 図 6-2)			0.15	0.5	µA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see 図 6-1)			55	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see 図 6-3)			0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see 図 6-1)			0.25	0.4	Ω

(1) Full temperature range is –40°C to 125°C for TLV431x-Q1.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right)\times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.
αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see 図 6-2), the total dynamic impedance of the circuit is defined as:

$$\left|z_{ka}\right|' = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$$

5.6 Electrical Characteristics for TLV431B-Q1

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV431BQ MIN	TLV431BQ TYP	TLV431BQ MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10mA	T_A = 25°C	1.234	1.24	1.246	V
			T_A = full range(1) (see 図 6-1)	1.221		1.265	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(2)	$V_{KA} = V_{REF}$, I_K = 10mA(1) (see 図 6-1)			11	31	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see 図 6-2)			–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see 図 6-2)			0.1	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(2)	I_K = 10mA, R1 = 10kΩ, R2 = open (see 図 6-2)			0.15	0.5	µA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see 図 6-1)			55	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see 図 6-3)			0.001	0.1	µA
$\|z_{KA}\|$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see 図 6-1)			0.25	0.4	Ω

(1) Full temperature range is –40°C to 125°C for TLV431x-Q1.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.
αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see 図 6-2), the total dynamic impedance of the circuit is defined as:

$$\left|z_{ka}\right|' = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$$

5.7 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated in the *セクション 5.4* table are not implied.

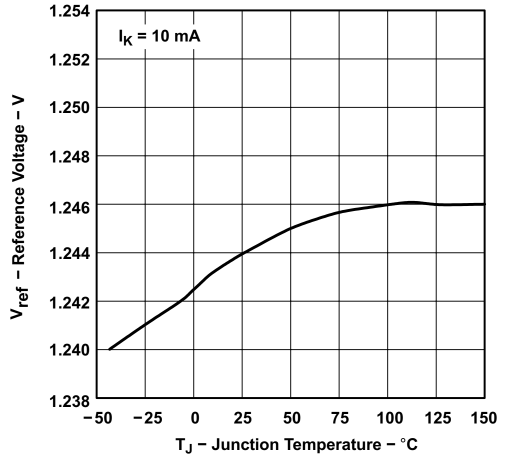


図 5-1. Reference Voltage vs Junction Temperature

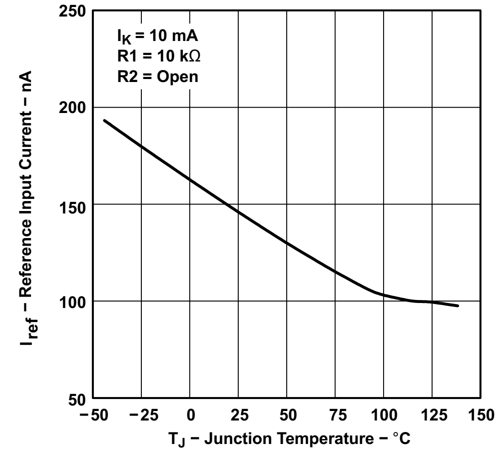


図 5-2. Reference Current vs Free- air Temperature (TLV431A)

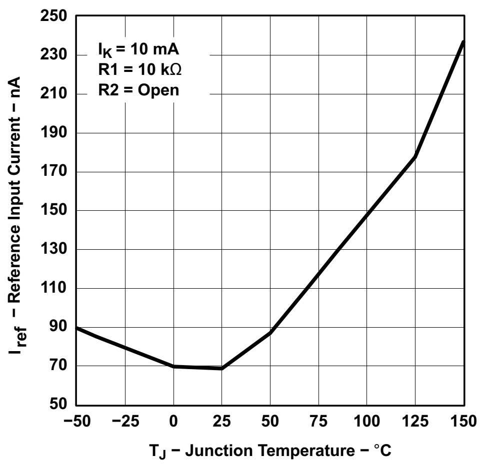


図 5-3. Reference Input Current vs Junction Temperature (for TLV431B)

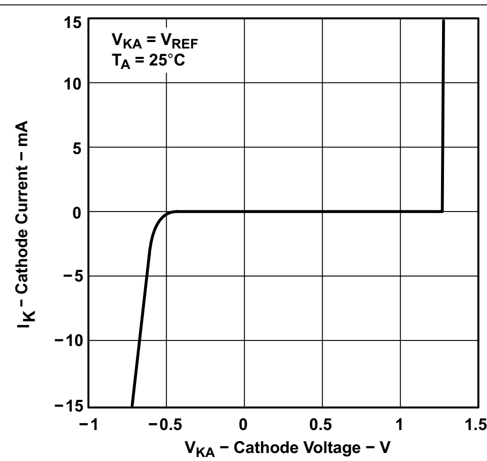


図 5-4. Cathode Current vs Cathode Voltage

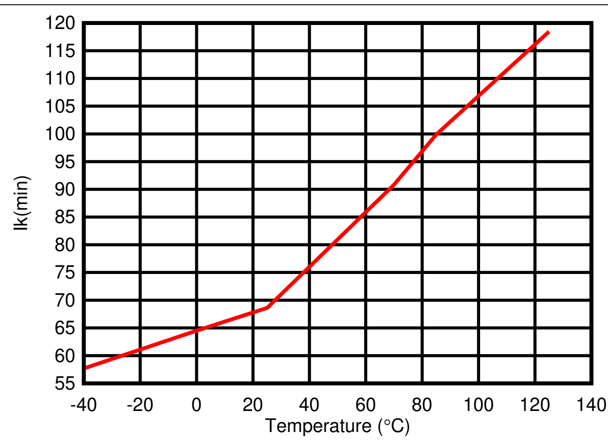


図 5-5. Minimum Cathode Current (µA) vs Temperature

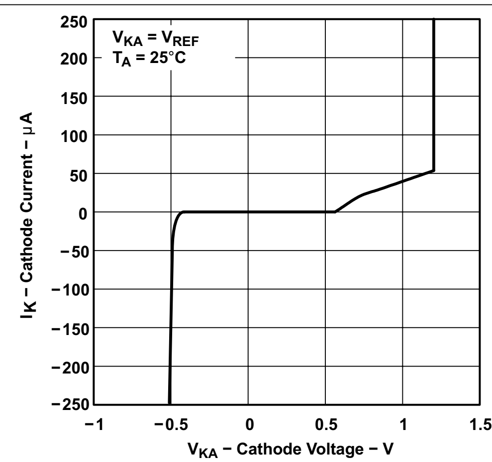


図 5-6. Cathode Current vs Cathode Voltage

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the セクション 5.4 table are not implied.

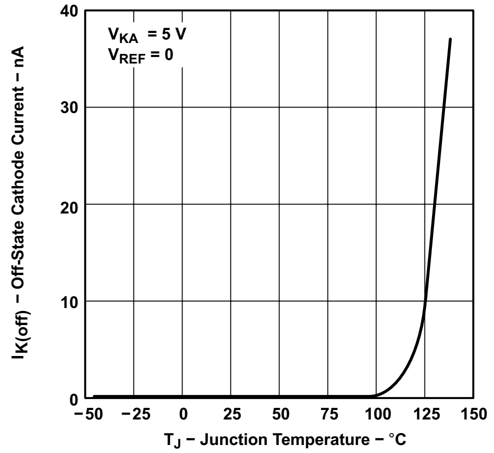


図 5-7. Off-State Cathode Current vs Junction Temperature for TLV431A

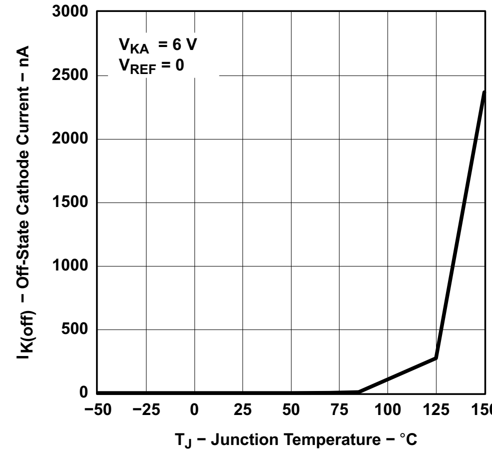


図 5-8. Off-State Cathode Current vs Junction Temperature for TLV431B

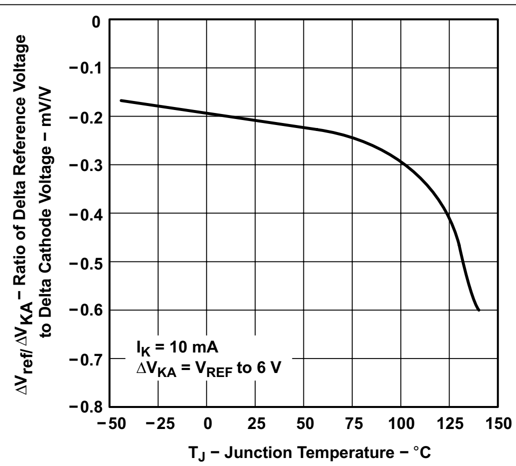


図 5-9. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature for TLV431A

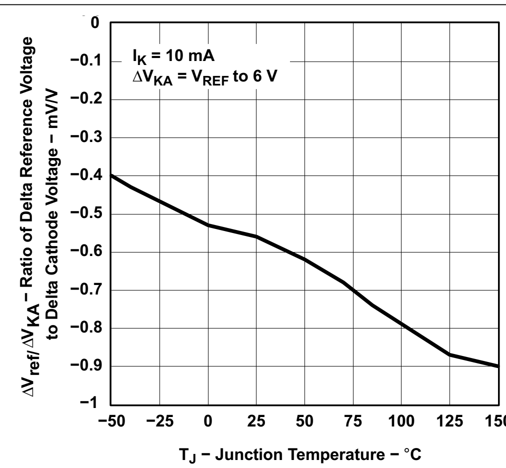
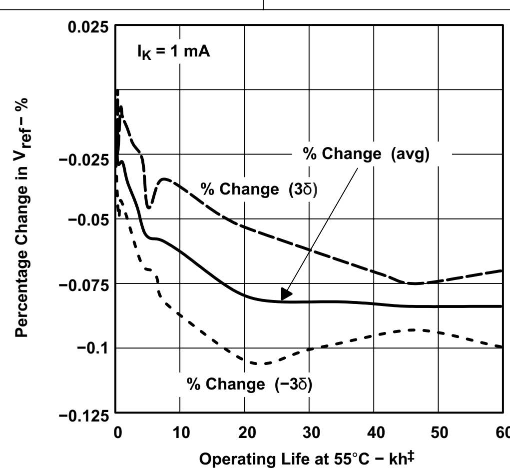


図 5-10. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431B)

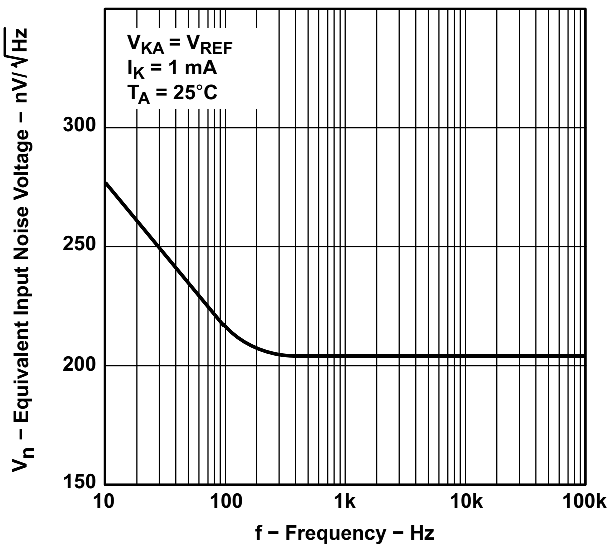


‡ Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7 eV.

図 5-11. Percentage Change in V_{REF} vs Operating Life at 55°C

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the セクション 5.4 table are not implied.



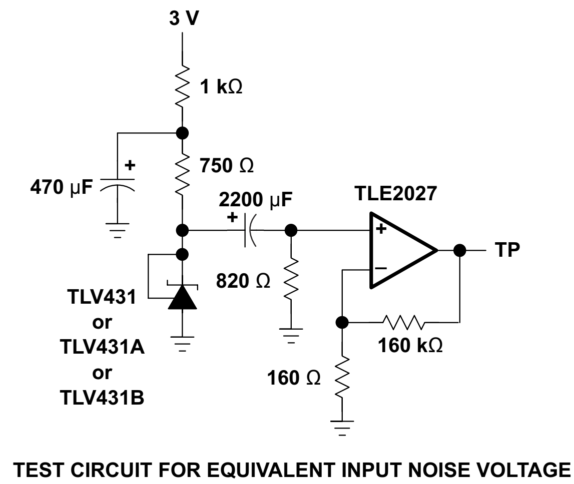
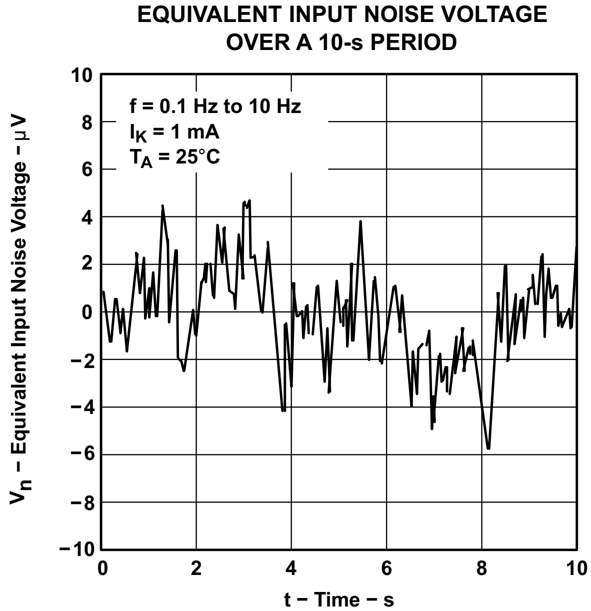
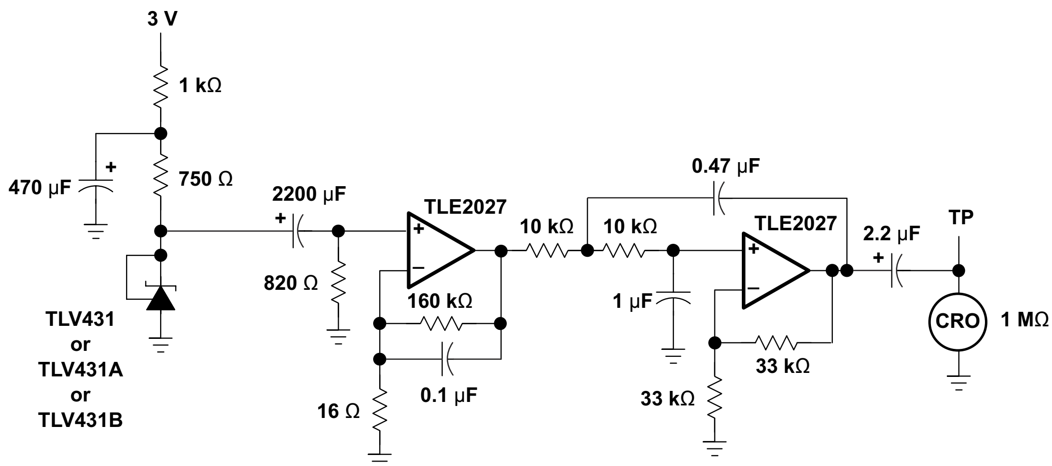


図 5-12. Equivalent Input Noise Voltage

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the セクション 5.4 table are not implied.





TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT NOISE VOLTAGE

図 5-13. Equivalent Noise Voltage over a 10s Period

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *セクション 5.4* table are not implied.

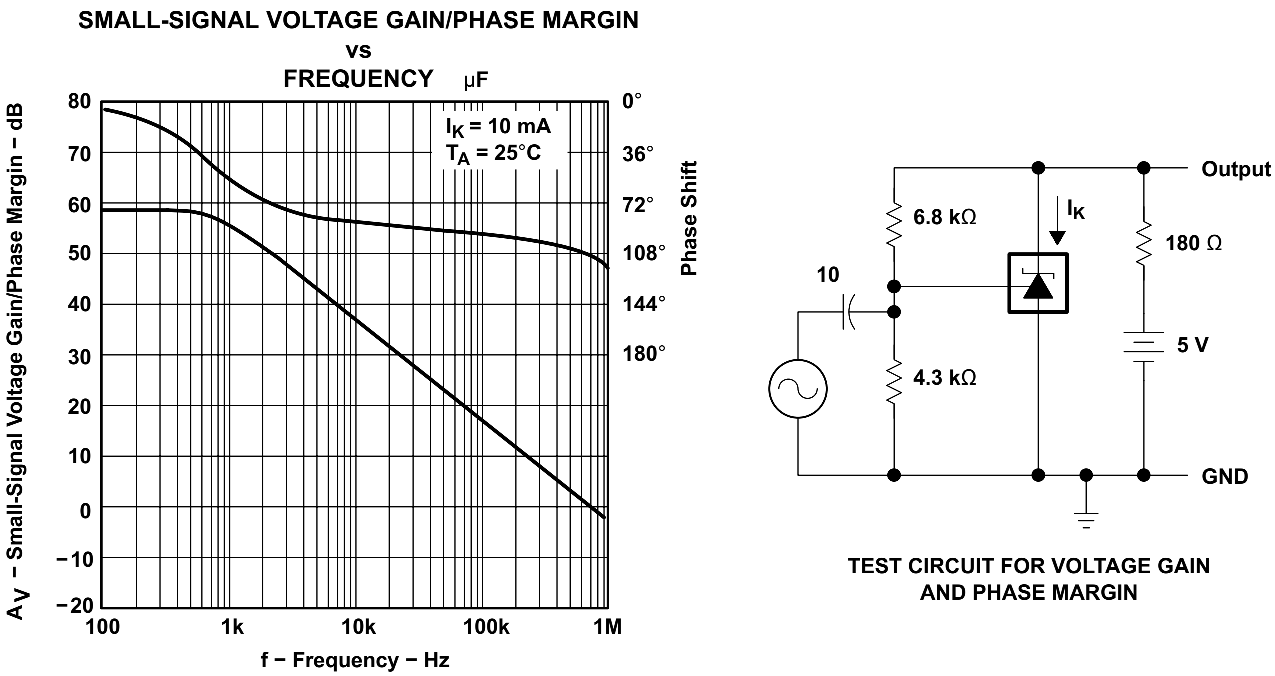


図 5-14. Voltage Gain and Phase Margin

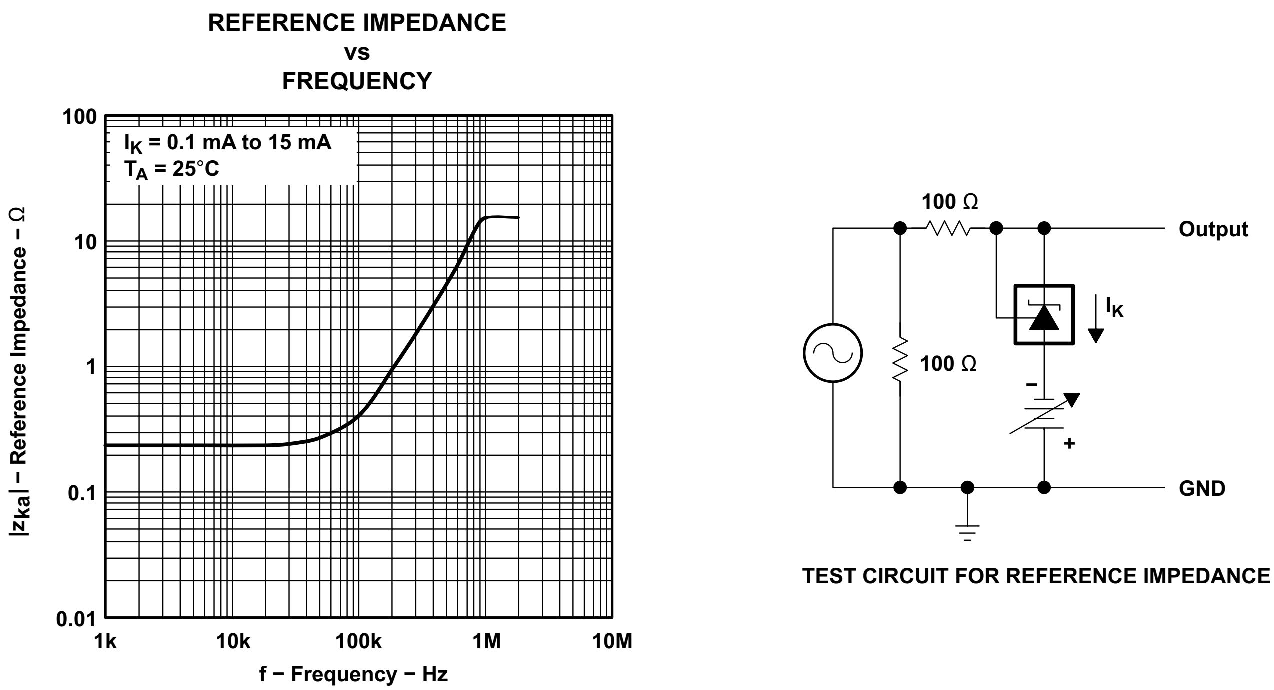


図 5-15. Reference Impedance vs Frequency

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *セクション 5.4* table are not implied.

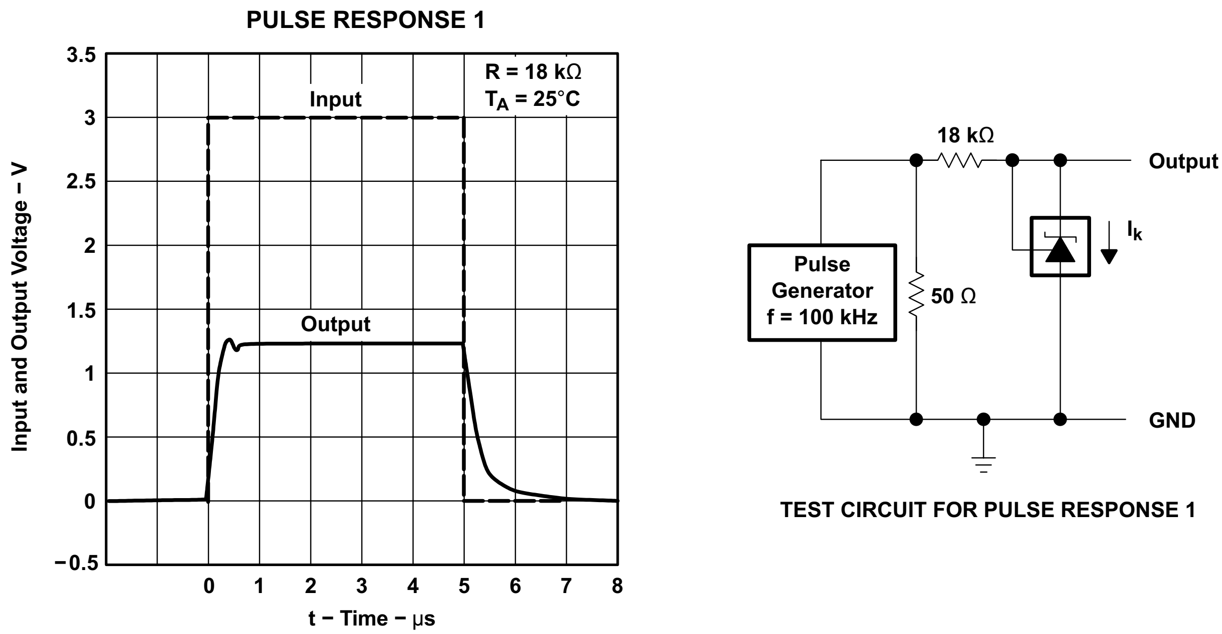


図 5-16. Pulse Response 1

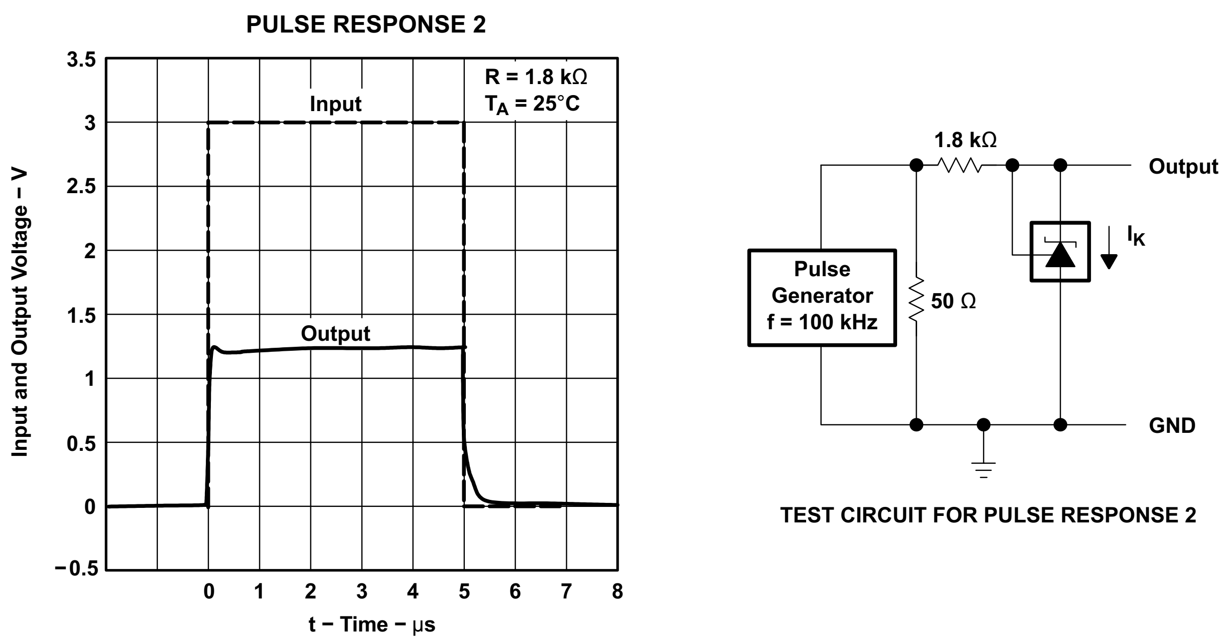
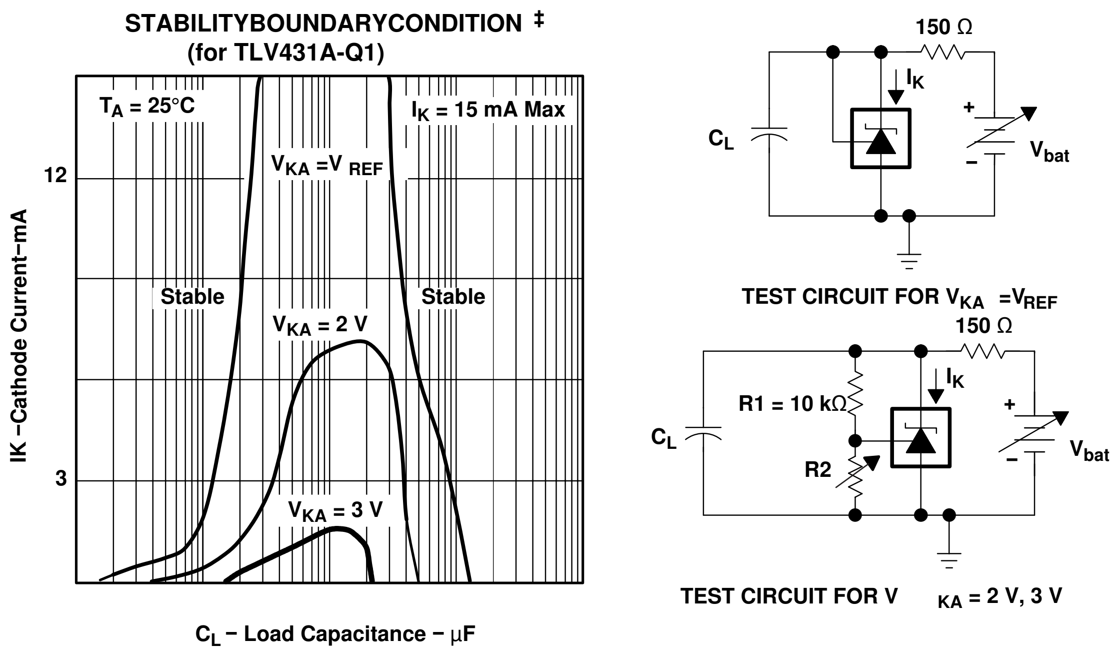


図 5-17. Pulse Response 2

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *セクション 5.4* table are not implied.



‡ The areas under the curves represent conditions that can cause the device to oscillate. For V_{KA} = 2V and 3V curves, R2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{bat} and C_L then were adjusted to determine the ranges of stability.

図 5-18. Stability Boundary Conditions

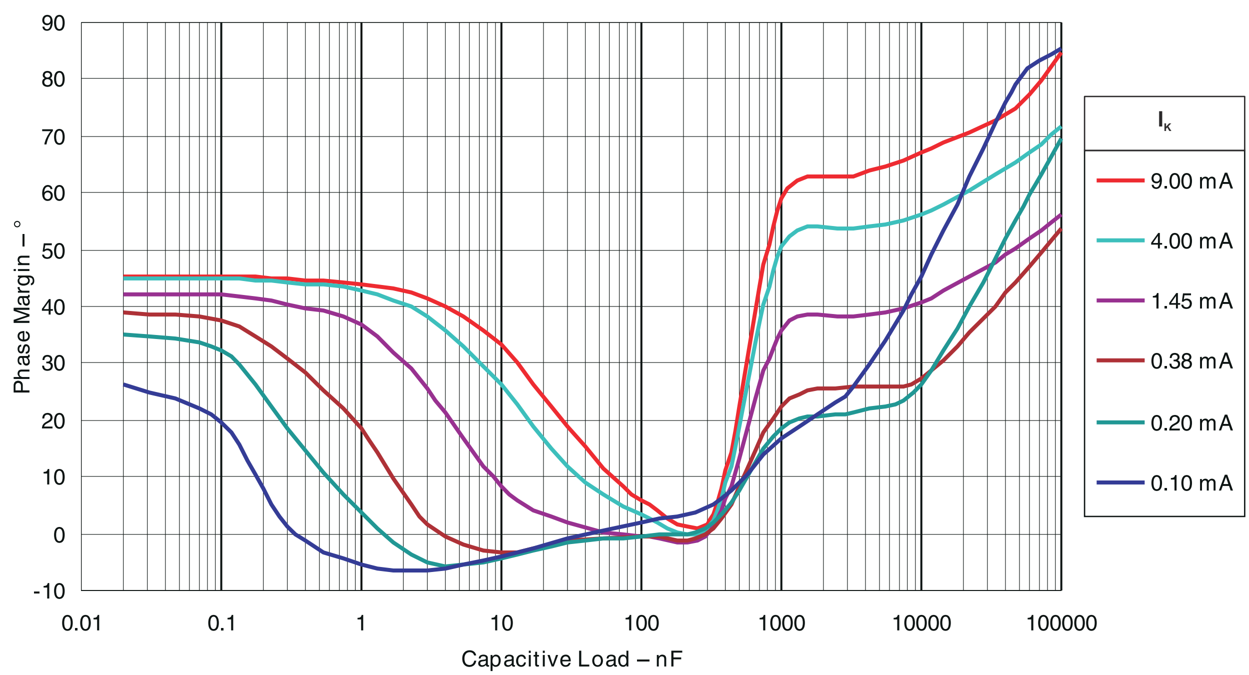


図 5-19. Phase Margin vs Capacitive Load V_{KA} = V_{REF} (1.25 V), T_A= 25°C (For TLV431B-Q1)

5.7 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the セクション 5.4 table are not implied.

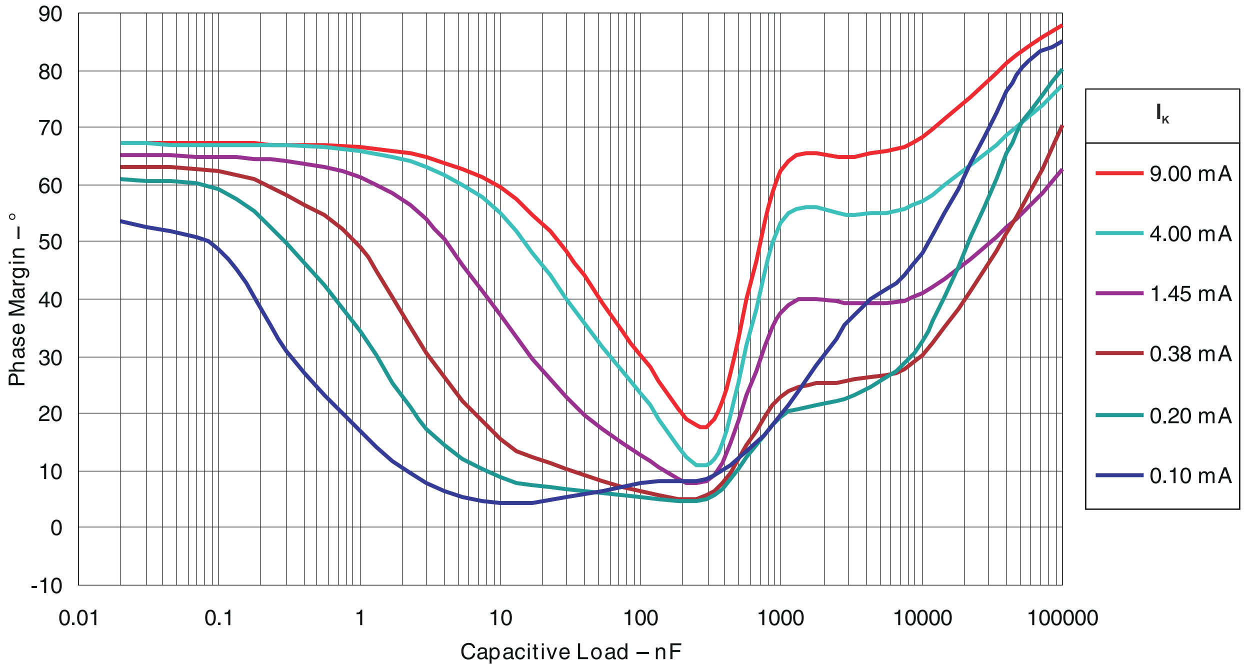


図 5-20. Phase Margin vs Capacitive Load V_{KA} = 2.50V, T_A= 25°C (For TLV431B-Q1)

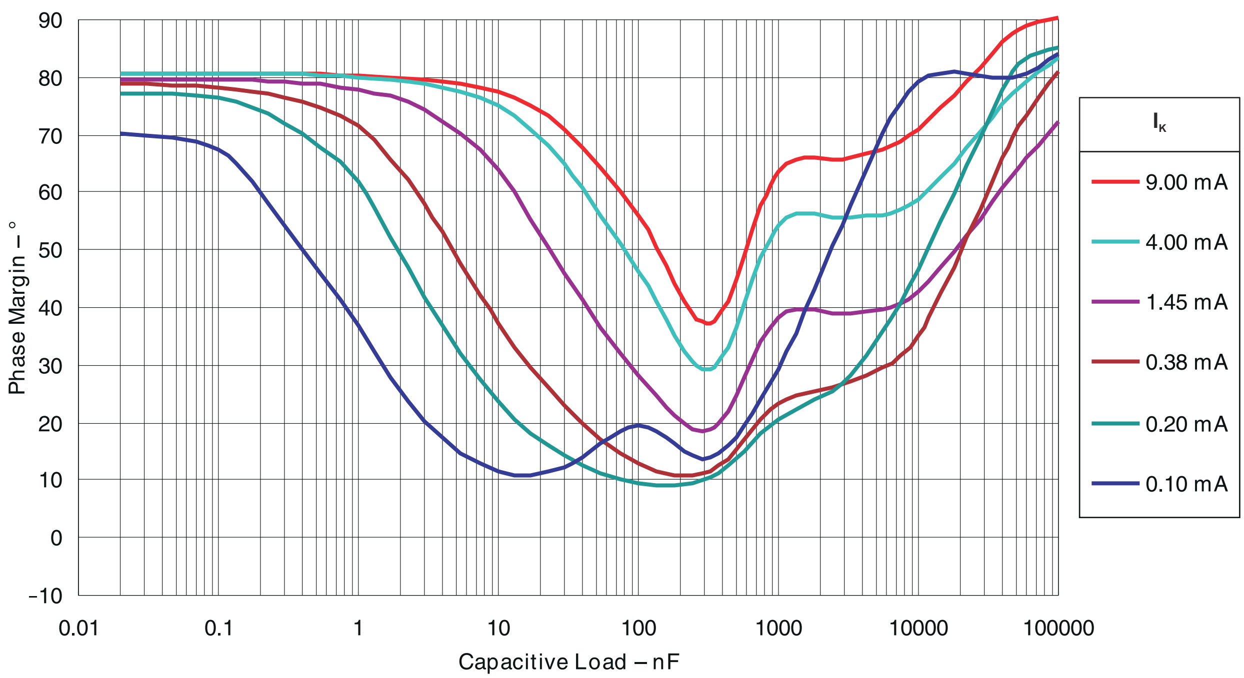


図 5-21. Phase Margin vs Capacitive Load V_{KA} = 5.00V, T_A= 25°C (For TLV431B-Q1)

6 Parameter Measurement Information

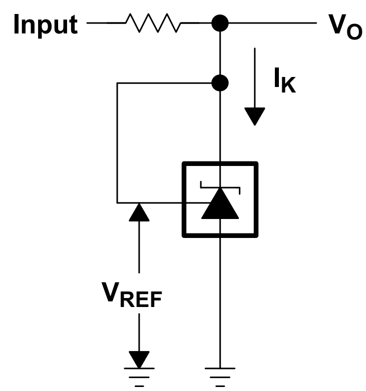


図 6-1. Test Circuit for $V_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

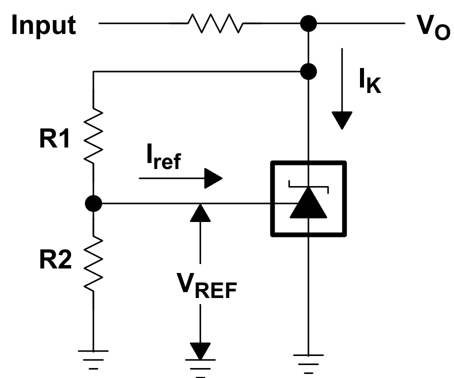


図 6-2. Test Circuit for $V_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1/R2) + I_{ref} \times R1$

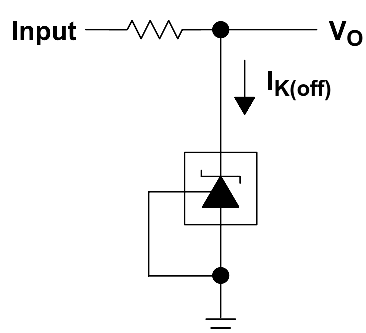


図 6-3. Test Circuit for $I_{K(off)}$

7 Detailed Description

7.1 Overview

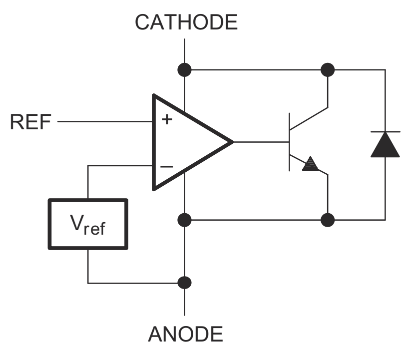
TLV431 is a low power counterpart to TL431, having lower reference voltage (1.24V vs 2.5V) for lower voltage adjustability and lower minimum cathode current ($I_{k(min)}$=100μA vs 1mA). Like TL431, the TLV431 is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp or comparator with integrated reference.

TLV431 can be operated and adjusted to cathode voltages from 1.24V to 6V, making this part optimum for a wide range of end equipments in industrial, auto, telecom & computing. For this device to behave as a shunt regulator or error amplifier, > 100μA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, and 1%. These reference options are denoted by B (0.5%) and A (1.0%) after the TLV431x-Q1.

The TLV431x-Q1 devices are characterized for operation from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

TLV431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal Darlington pair.

When operated with enough voltage headroom (≥ 1.24V) and cathode current (Ika), TLV431 forces the reference pin to 1.24V. However, the reference pin can not be left floating, as it needs I_{ref} ≥ 0.5μA (please see the *セクション 7.2*). This is because the reference pin is driven into an npn, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, TLV431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations for it to be in the proper linear region giving TLV431 enough gain.

Unlike many linear regulators, TLV431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor 図 5-18 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

7.4 Device Functional Modes

7.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TLV431 is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TLV431 will have the characteristics shown in 図 5-6. With such high gain in this configuration, TLV431 is typically used as a comparator. With the reference integrated makes TLV431 the preferred choice when users are trying to monitor a certain level of a single signal.

7.4.2 Closed Loop

When the cathode/output voltage or current of TLV431 is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLV431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

8 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

図 8-1 shows the TLV431A, or TLV431B used in a 3.3V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} (1.24V ± 1%). The output of the regulator, plus the forward voltage drop of the optocoupler LED (1.24 + 1.4 = 2.64 V), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7Vdc is possible in the topology shown in 図 8-1.

The 431 family of devices are prevalent in these applications, being designers go to choice for secondary side regulation. Due to this prevalence, this section explains the operation and design in both states of TLV431 that this application sees, open loop (Comparator + Vref) & closed loop (Shunt Regulator).

Further information about system stability and using a TLV431 device for compensation can be found in the application note *Compensation Design With TL431 for UCC28600,* SLUA671.

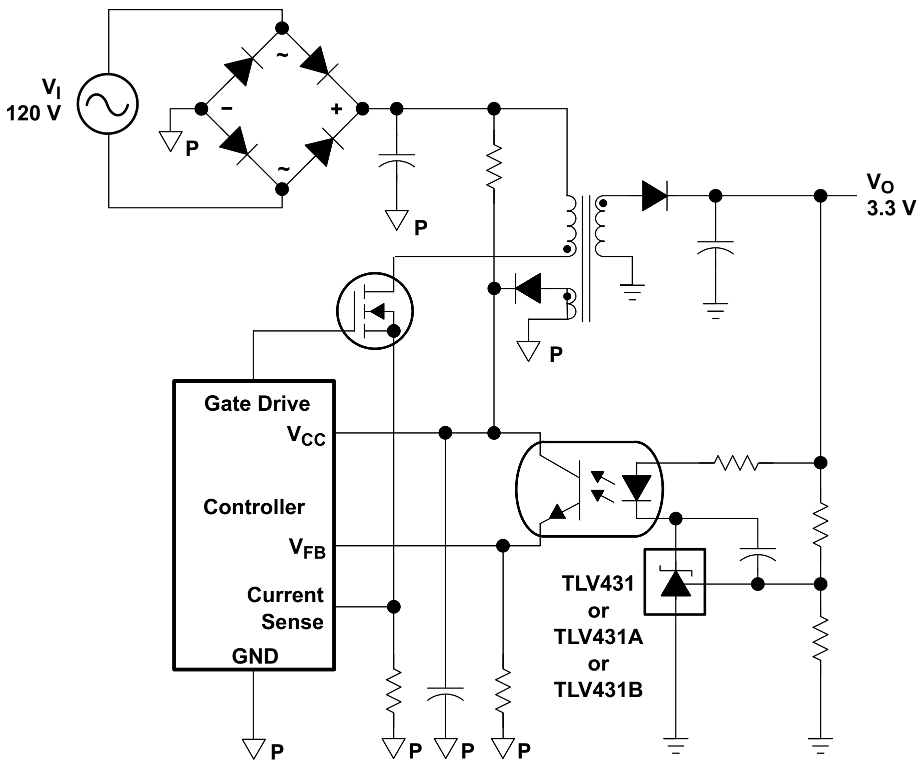


図 8-1. Flyback With Isolation Using TLV431, TLV431A, or TLV431B as Voltage Reference and Error Amplifier

8.2 Typical Applications

8.2.1 Comparator with Integrated Reference (Open Loop)

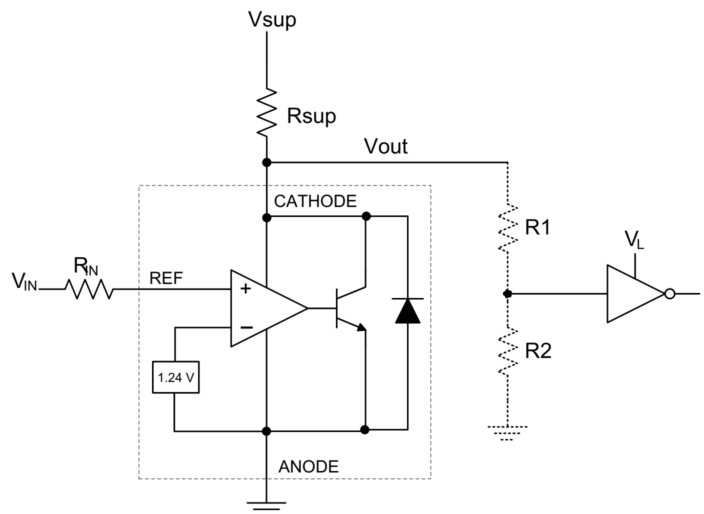


図 8-2. Comparator Application Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to 5V
Input Resistance	10kΩ
Supply Voltage	5V
Cathode Current (Ik)	500µA
Output Voltage Level	~1V - Vsup
Logic Input Thresholds VIH/VIL	VL

8.2.1.2 Detailed Design Procedure

When using TLV431 as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

8.2.1.2.1 Basic Operation

In the configuration shown in 図 8-2 TLV431 behaves as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), TLV431 has enough open loop gain to provide a quick response. With the TLV431's min Operating Current maximum (Imin) being 55uA to 100uA over temperature, operation below that can result in low gain, leading to a slow response.

8.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage is within the range of 1.24V ±(0.5% or 1.0%) depending on which version is being used.

The more overdrive voltage provided, the faster the TLV431 responds. This can be seen in figures 図 8-3 and 図 8-4, where the images display the output responses to various input voltages.

For applications where TLV431 is being used as a comparator, set the trip point to greater than the positive expected error (i.e. +1.0% for the A version). For fast response, set the trip point to > 10% of the internal V_{ref}.

For minimal voltage drop or difference from Vin to the ref pin, TI recommends using an input resistor < 10kΩ to provide I_{ref}.

8.2.1.2.3 Output Voltage and Logic Input Level

For the TLV431 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} & V_{IL}.

As seen in 図 8-3, TLV431's output low level voltage in open-loop/comparator mode is ~1 V, which is sufficient for some 3.3V supplied logic. However, would not work for 2.5V and 1.8V supplied logic. In order to accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TLV431's output high voltage is approximately V_{sup} due to TLV431 being open-collector. If V_{sup} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 & R2 in 図 8-2) is much greater than R_{sup} to not interfere with TLV431's ability to pull close to V_{sup} when turning off.

8.2.1.2.3.1 Input Resistance

TLV431 requires an input resistance in this application to source the reference current (I_{ref}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{ref}=V_{in}-I_{ref}*R_{in}$. Since I_{ref} can be as high as 0.5μA TI recommends using a resistance small enough that will mitigate the error that I_{ref} creates from V_{in}.

8.2.1.3 Application Curves

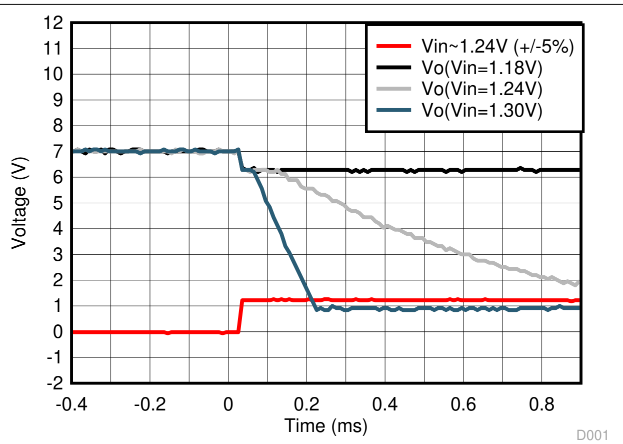


図 8-3. Output Response with Small Overdrive Voltages

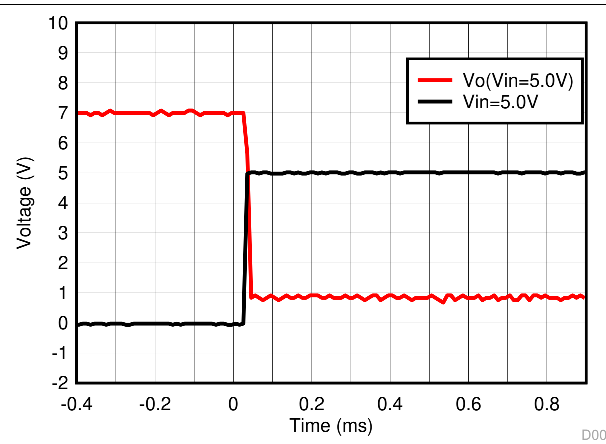


図 8-4. Output Response with Large Overdrive Voltage

8.2.2 Shunt Regulator/Reference

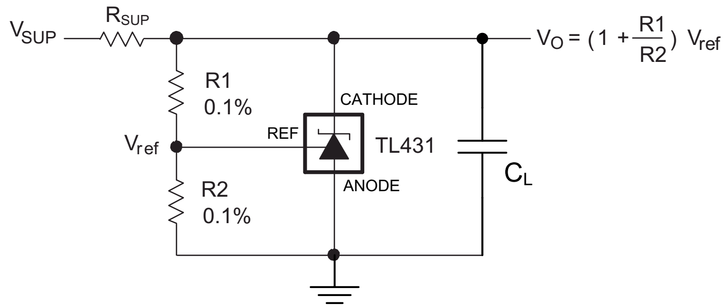


図 8-5. Shunt Regulator Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	6V
Cathode Current (Ik)	1mA
Output Voltage Level	1.24V - 6V
Load Capacitance	100pF
Feedback Resistor Values and Accuracy (R1 & R2)	10kΩ

8.2.2.2 Detailed Design Procedure

When using TLV431 as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

8.2.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in 図 8-5, with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in 図 8-5. The cathode voltage can be more accurately determined by taking in to account the cathode current:

$V_O=(1+R1/R2)*V_{ref}–I_{ref}*R1$

For this equation to be valid, TLV431 must be fully biased so that there is enough open loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in *セクション 5.4* table.

8.2.2.2.2 Total Accuracy

When programming the output above unity gain (Vka=Vref), TLV431 is susceptible to other errors that can effect the overall accuracy beyond V_{ref}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ - Change in reference voltage over temperature
- $\Delta V_{ref} / \Delta V_{KA}$ - Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ - Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account. Application note SLVA445 assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

8.2.2.2.3 Stability

Though TLV431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage can present a capacitive load that is within the TLV431 region of stability, shown in 図 5-18. Also, designers can use capacitive loads to improve the transient response or for power supply decoupling.

8.2.2.3 Application Curve

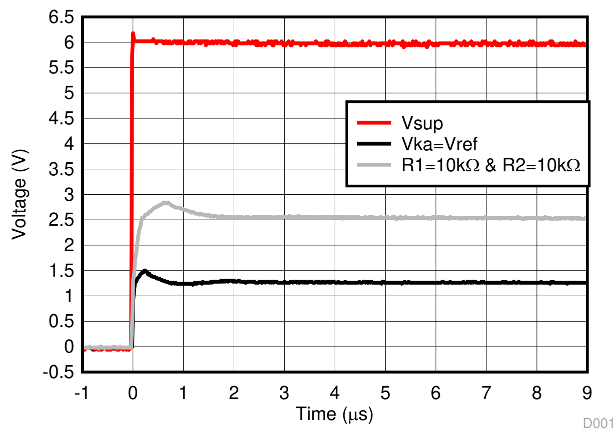


図 8-6. TLV431 Start-Up Response

8.3 Power Supply Recommendations

When using TLV431 as a Linear Regulator to supply a load, designers typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in 図 5-18.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed it's absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

8.4 Layout

8.4.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

8.4.2 Layout Example

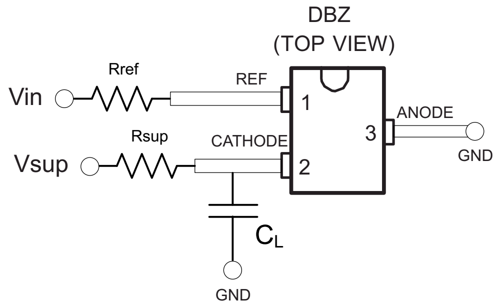


図 8-7. DBZ Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2017) to Revision B (March 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Updated pinout diagrams 3
- Updated *Typical Applications Design Requirements* 21

Changes from Revision * (December 2008) to Revision A (October 2017) **Page**

- 車載用の AEC-Q100 機能を追加 1
- Added New typical curves 15

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV431AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	VONQ
TLV431AQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VONQ
TLV431AQDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VONQ
TLV431AQDBVRQ1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VONQ
TLV431BQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	VOMQ
TLV431BQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VOMQ
TLV431BQDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOQQ
TLV431BQDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOQQ
TLV431BQDBZRQ1G4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOQQ
TLV431BQDBZRQ1G4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOQQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV431A-Q1, TLV431B-Q1 :

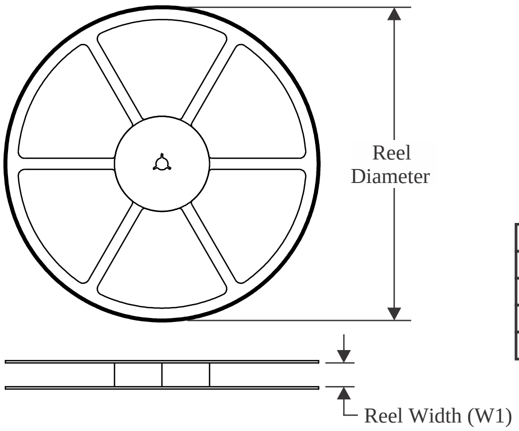
- Catalog : TLV431A, TLV431B

NOTE: Qualified Version Definitions:

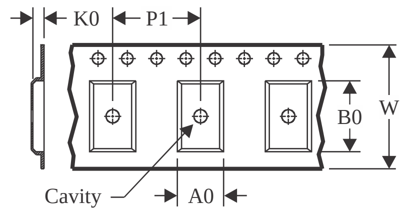
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

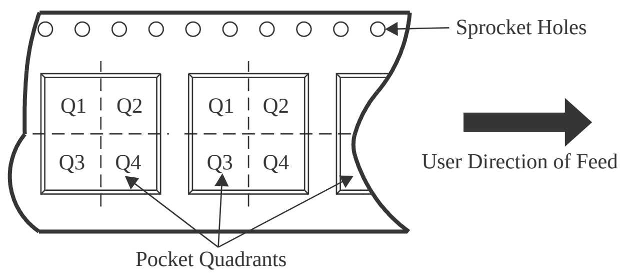


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

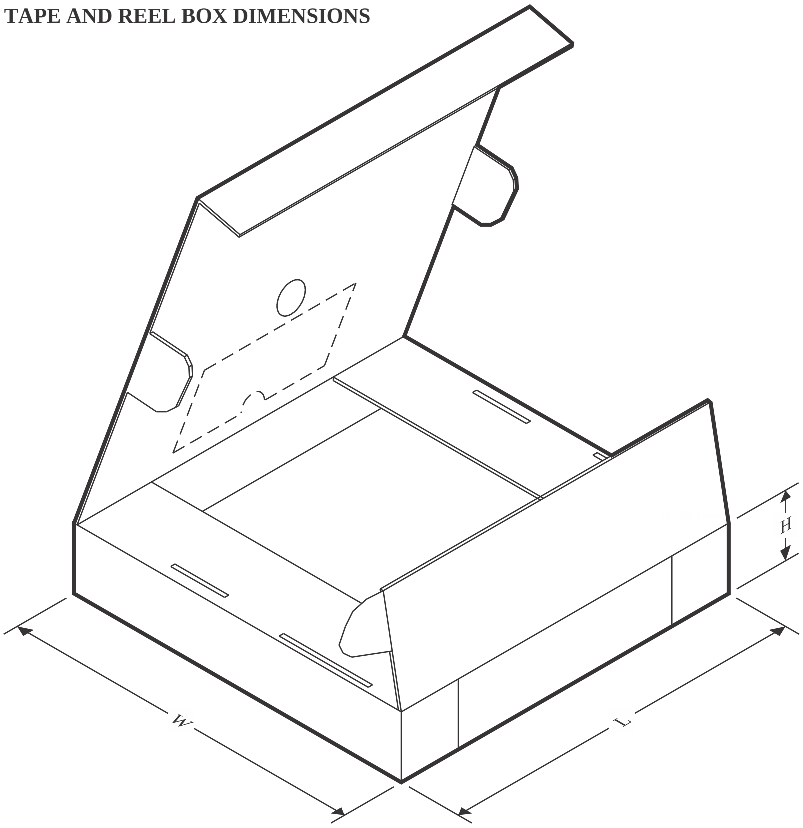
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

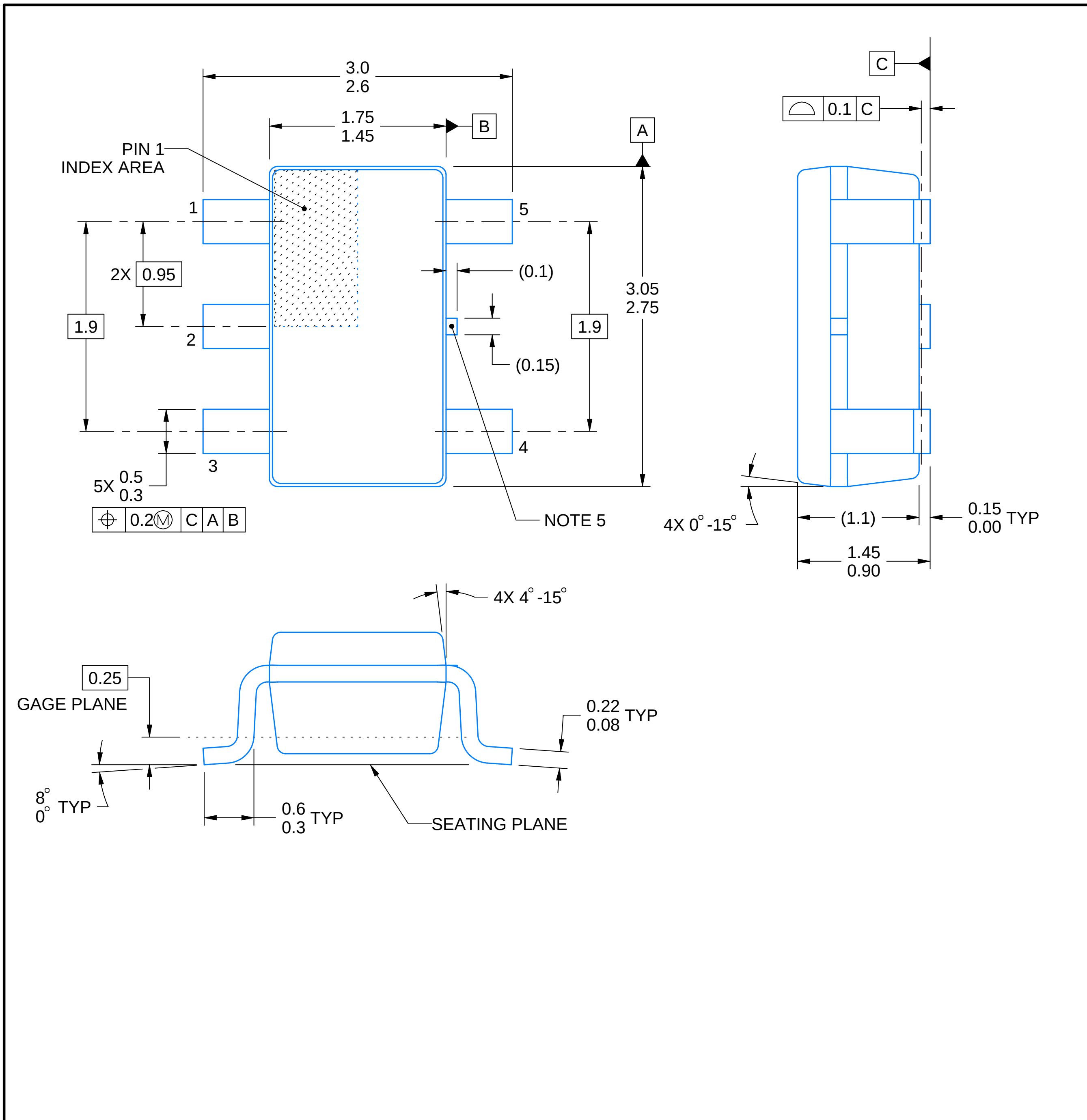
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431AQDBVRQ1G4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431BQDBZRQ1G4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

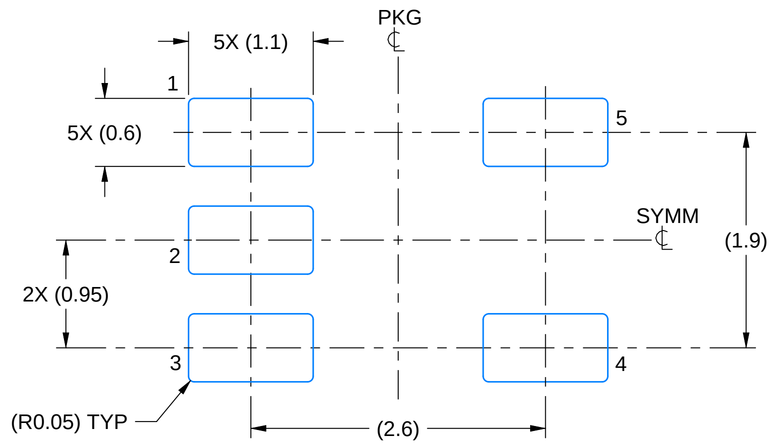
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431AQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431AQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431AQDBVRQ1G4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV431BQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431BQDBZRQ1G4	SOT-23	DBZ	3	3000	200.0	183.0	25.0



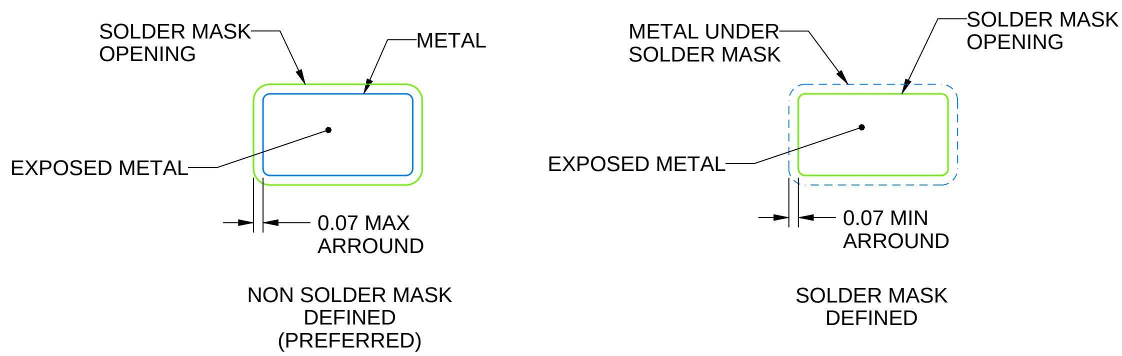
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

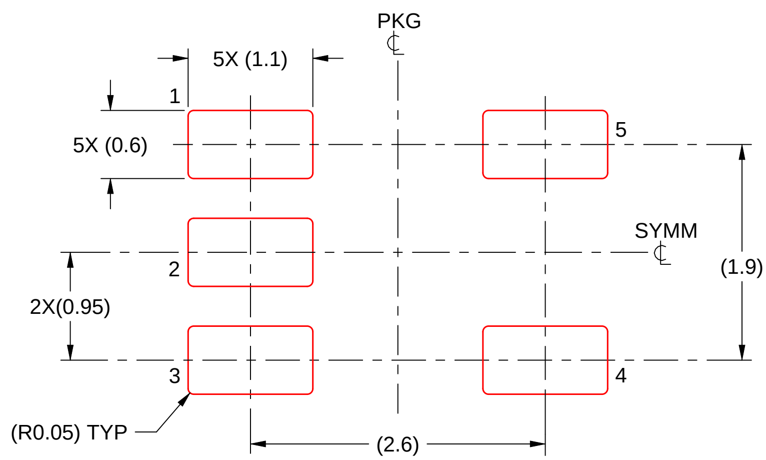


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

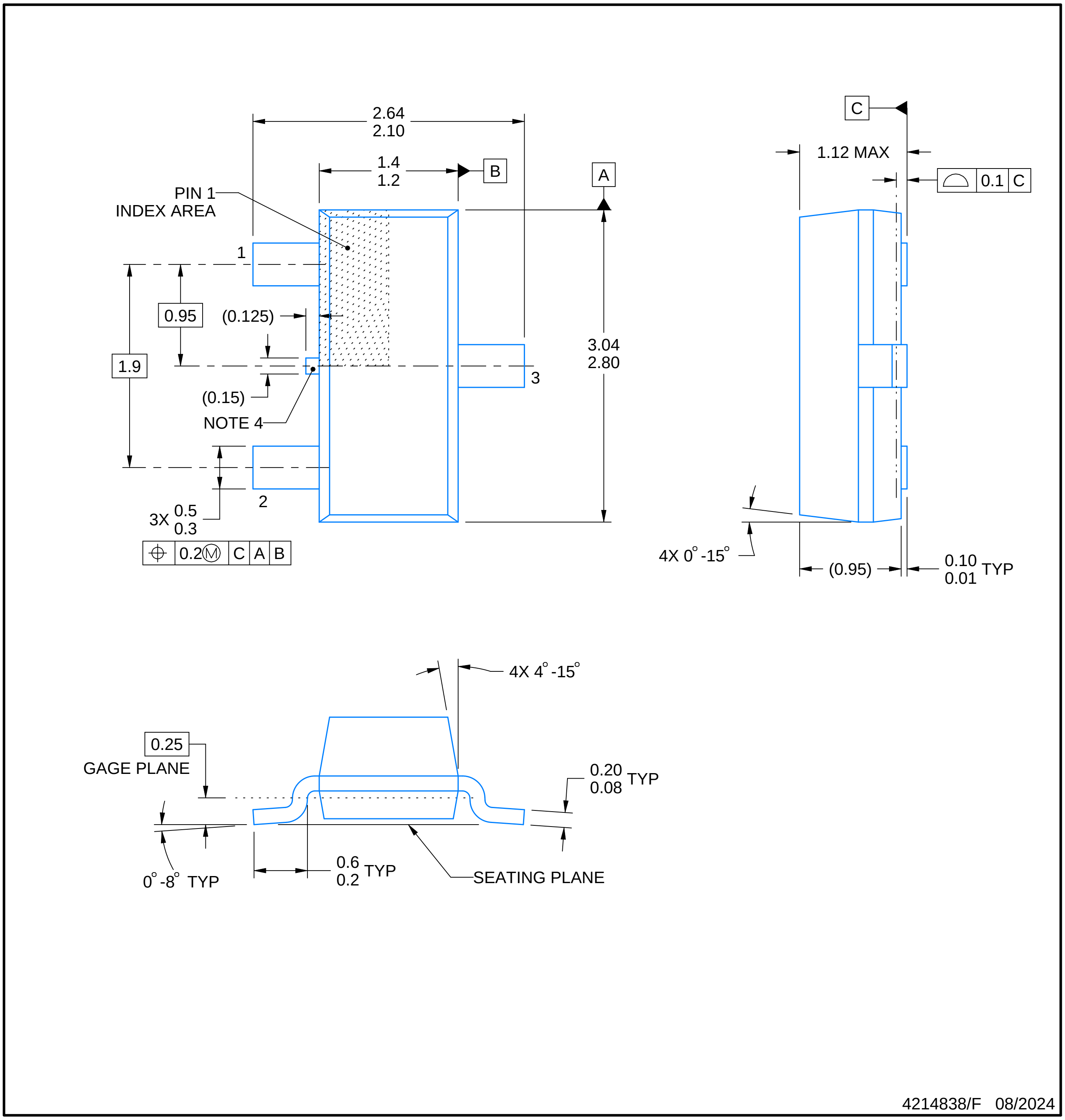
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

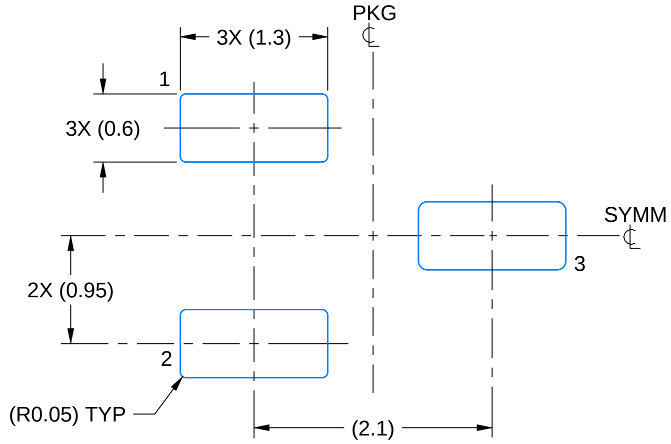
SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR

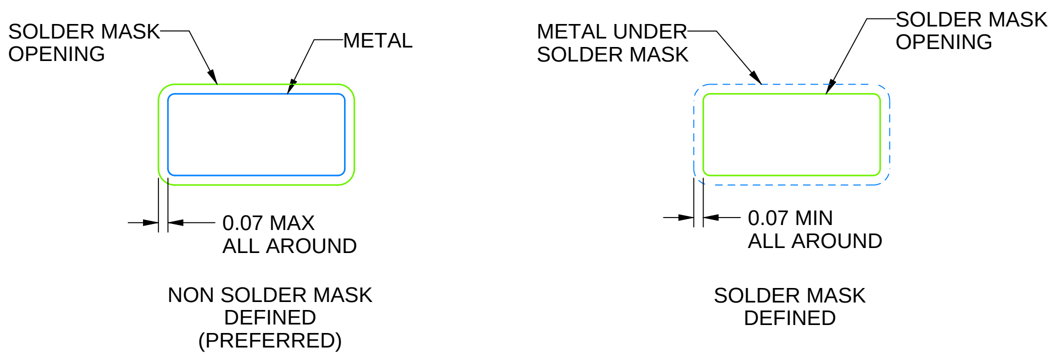


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

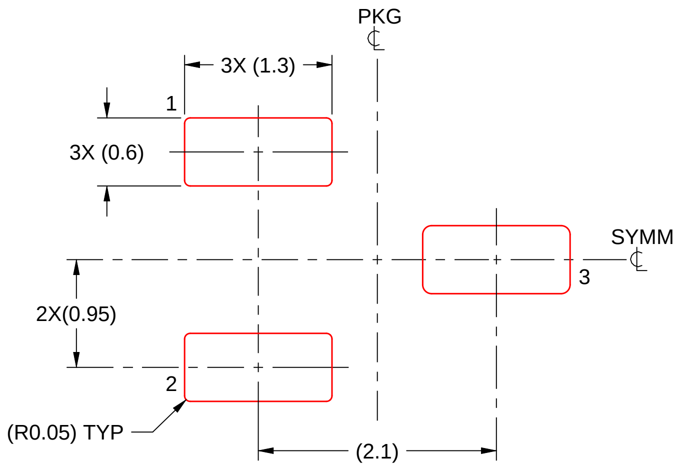


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.