

TLV6256xA 強制 PWM 機能を持つ SOT563 パッケージの 1A、2A 降圧型コンバータ

1 特長

- 強制 PWM により出力電圧リップルを低減
- 最大 95% の効率
- 低 $R_{DS(ON)}$ のスイッチ: 100mΩ / 60mΩ
- 入力電圧範囲: 2.5V~5.5V
- 出力電圧は 0.6V~ V_{IN} の範囲で調整可能
- 100% デューティ・サイクル動作による最小のドロップアウト電圧
- 標準スイッチング周波数: 1.5MHz
- パワー・グッド出力
- 過電流保護
- ソフト・スタートアップを内蔵
- サーマル・シャットダウン保護機能
- SOT563 パッケージで供給
- TLV62568、TLV62569 とピン互換
- WEBENCH® Power Designer により、カスタム設計を作成

2 アプリケーション

- 汎用 POL (ポイント・オブ・ロード) 電源
- STB / DVR
- IP ネットワーク・カメラ
- ワイヤレス・ルータ
- ソリッド・ステート・ドライブ (SSD) – エンタープライズ

3 概要

TLV62568AおよびTLV62569Aデバイスは同期整流降圧型DC/DCコンバータで、高効率と小型のソリューション向けに最適化されています。このデバイスには、最大2Aの出力電流を供給できるスイッチが内蔵されています。負荷範囲の全体にわたって、スイッチング周波数1.5MHzのパルス幅変調(PWM)モードで動作します。シャットダウン時には、消費電流が2μA未満に減少します。

内部のソフトスタート回路により、スタートアップ時の突入電流が制限されます。その他、過電流保護、サーマル・シャットダウン保護、パワー・グッドなどの機能も内蔵されています。このデバイスは、SOT563パッケージで供給されます。

製品情報⁽¹⁾

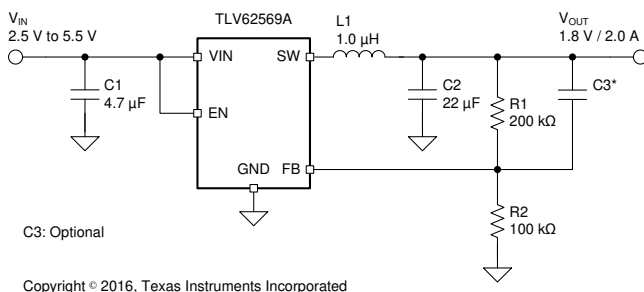
型番	パッケージ	本体サイズ(公称)
TLV62568ADRL	SOT563 (6)	1.60mm×1.60mm
TLV62568APDRL		
TLV62569ADRL		
TLV62569APDRL		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

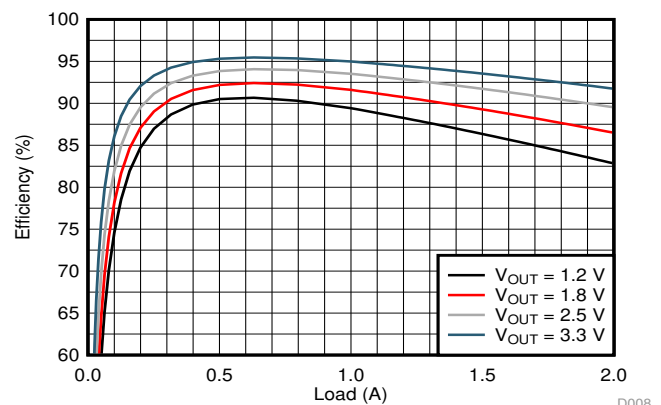
デバイスの比較

型番	出力電流	機能
TLV62568ADRL	1A	-
TLV62568APDRL		パワー・グッド
TLV62569ADRL	2A	-
TLV62569APDRL		パワー・グッド

代表的なアプリケーションの回路図



入力電圧5V時の効率



目次

1	特長	1	8	Application and Implementation	8
2	アプリケーション	1	8.1	Application Information	8
3	概要	1	8.2	Typical Application	8
4	改訂履歴	2	9	Power Supply Recommendations	13
5	Pin Configuration and Functions	3	10	Layout	13
6	Specifications	3	10.1	Layout Guidelines	13
6.1	Absolute Maximum Ratings	3	10.2	Layout Example	13
6.2	ESD Ratings	3	10.3	Thermal Considerations	14
6.3	Recommended Operating Conditions	4	11	デバイスおよびドキュメントのサポート	14
6.4	Thermal Information	4	11.1	デバイス・サポート	14
6.5	Electrical Characteristics	4	11.2	ドキュメントのサポート	14
6.6	Typical Characteristics	5	11.3	ドキュメントの更新通知を受け取る方法	14
7	Detailed Description	6	11.4	サポート・リソース	15
7.1	Overview	6	11.5	商標	15
7.2	Functional Block Diagrams	6	11.6	静電気放電に関する注意事項	15
7.3	Feature Description	6	11.7	Glossary	15
7.4	Device Functional Modes	7	12	メカニカル、パッケージ、および注文情報	15

4 改訂履歴

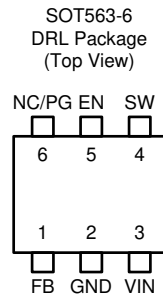
Revision A (May 2018) から Revision B に変更 Page

- 変更 Power Good pin sink current capability from 1 mA to 2 mA **7**

2018年4月発行のものから更新 Page

- ステータスを「事前情報」から「量産データ」に変更 **1**

5 Pin Configuration and Functions



Pin Functions

NAME	SOT563-6	I/O/PWR	DESCRIPTION
	PIN NUMBER		
FB	1	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	2	PWR	Ground pin.
VIN	3	PWR	Power supply voltage input.
SW	4	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
EN	5	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
PG	6	O	Power good open drain output pin for TLV62569APDRL. The pull-up resistor should not be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating.
NC	6	-	No connection pin for TLV62569ADRL. The pin can be connected to the output or the ground for enhancing thermal performance. Or leave it floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, EN, PG	-0.3	6	V
	SW (DC)	-0.3	V _{IN} + 0.3	
	SW (AC, less than 10ns) ⁽³⁾	-3.0	9	
	FB	-0.3	3	
T _J	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) While switching.

6.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2.5		5.5	V
V _{OUT}	Output voltage	0.6		V _{IN}	V
I _{OUT}	Output current	0		2	A
T _J	Junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV62568Ax, TLV62569Ax		UNIT
		JEDEC (DRL)	EVM (DRL)	
		6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	142.8	124.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.1	n/a ⁽²⁾	°C/W
R _{θJB}	Junction-to-board thermal resistance	28.9	n/a ⁽²⁾	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.4	1.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	28.7	23.1	°C/W

 (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) Not applicable to an EVM.

6.5 Electrical Characteristics

 V_{IN} = 5.0 V, T_J = 25 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _{SD}	Shutdown current into VIN pin	EN = 0 V	0.01	2		μA
V _{UVLO}	Under voltage lock out	V _{IN} falling	2.3	2.45		V
	under voltage lock out hysteresis		100			mV
T _{JSD}	Thermal shutdown	T _J rising	150			°C
		T _J falling	130			
LOGIC INTERFACE						
V _{IH}	High-level input voltage at EN pin	2.5 ≤ V _{IN} ≤ 5.5	1.2			V
V _{IL}	Low-level input voltage at EN pin	2.5 ≤ V _{IN} ≤ 5.5			0.4	V
t _{SS}	Soft startup time	From EN high to 95% of V _{OUT} nominal	0.9			ms
V _{PG}	Power good threshold	V _{FB} rising, referenced to V _{FB} nominal	95%			
		V _{FB} falling, referenced to V _{FB} nominal	90%			
V _{PG,OL}	Low-level output voltage at PG pin	I _{SINK} = 1 mA			0.4	V
I _{PG,LKG}	Input leakage current into PG pin	V _{PG} = 5 V		100		nA
t _{PG,DLY}	Power good delay time	V _{FB} falling		40		μs

Electrical Characteristics (continued)

$V_{IN} = 5.0\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{FB}	Feedback regulation voltage		0.588	0.6	0.612	V
I_{FB}	Input leakage current into FB pin	$V_{FB} = 0.6\text{ V}$		10		nA
$R_{DS(on)}$	High-side FET on resistance			100		m Ω
	Low-side FET on resistance			60		
I_{LIM}	High-side FET current limit	TLV62569A, TLV62569AP	3			A
		TLV62568A, TLV62568AP	2			
f_{SW}	Switching frequency			1.5		MHz

6.6 Typical Characteristics

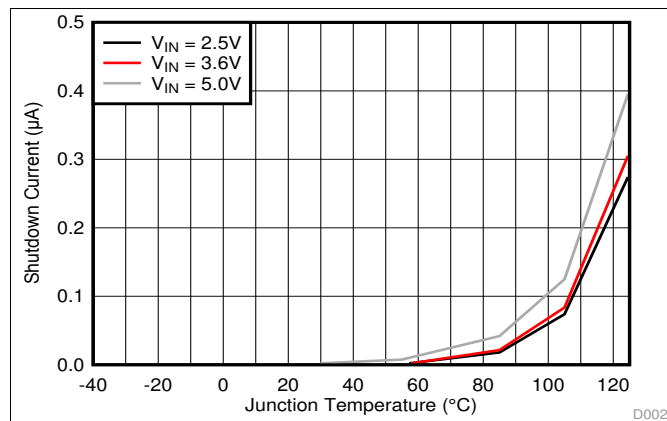


FIG 1. Shutdown Current vs Junction Temperature

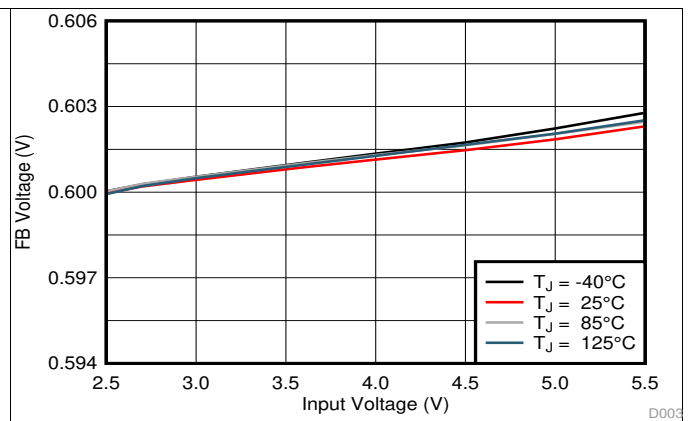


FIG 2. FB Voltage Accuracy

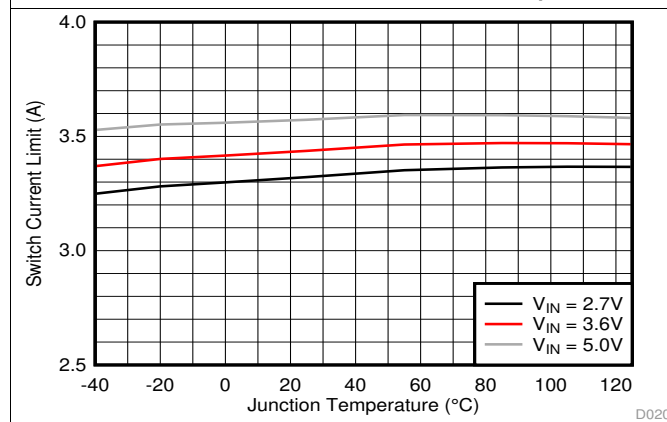


FIG 3. Switch Current Limit, TLV62569A

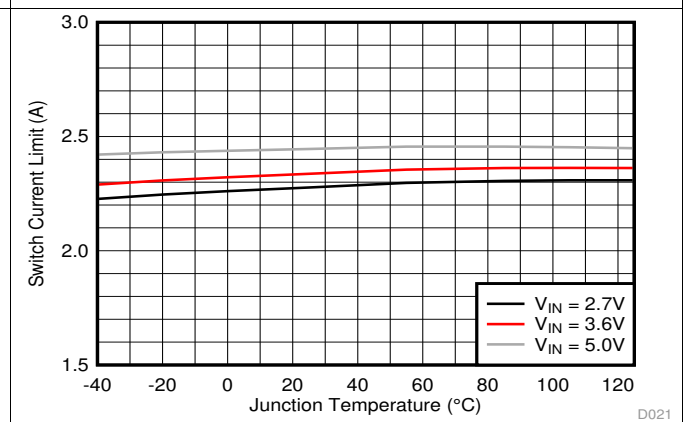


FIG 4. Switch Current Limit, TLV62568A

7 Detailed Description

7.1 Overview

The device is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM). Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.2 Functional Block Diagrams

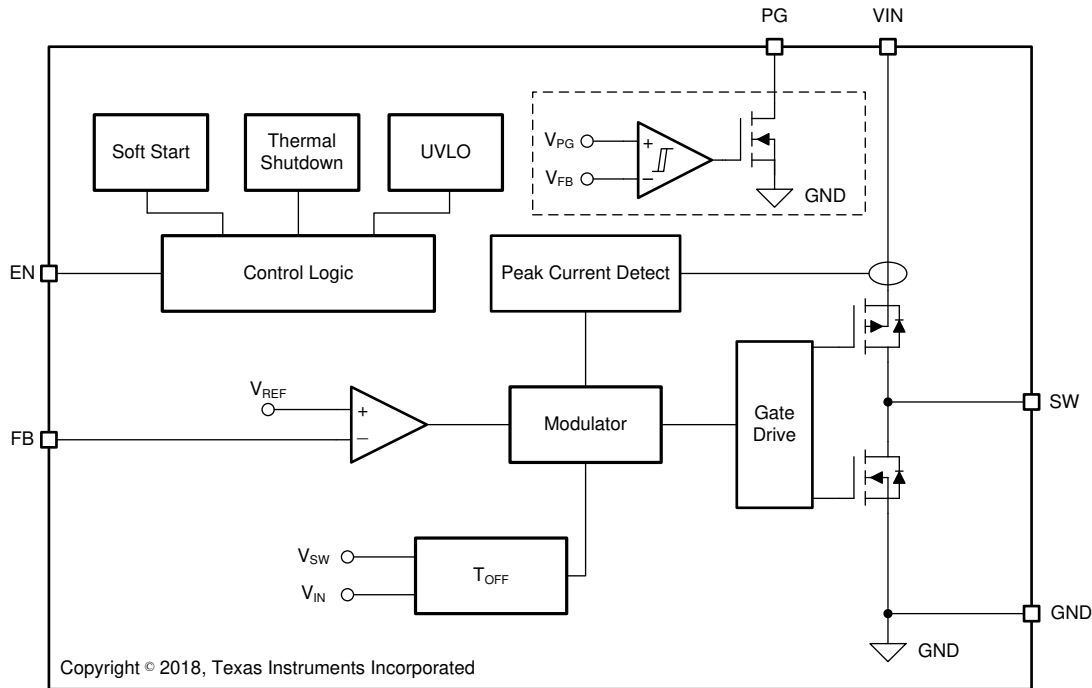


图 5. TLV62569A Functional Block Diagram

7.3 Feature Description

7.3.1 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

(1)

7.3.2 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

Feature Description (continued)

The device is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The device adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

7.3.4 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

7.3.5 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD} . Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

7.4.2 Power Good

The TLV62568AP and TLV62569AP have a power good output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4\text{ V} < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4\text{ V}$	√	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

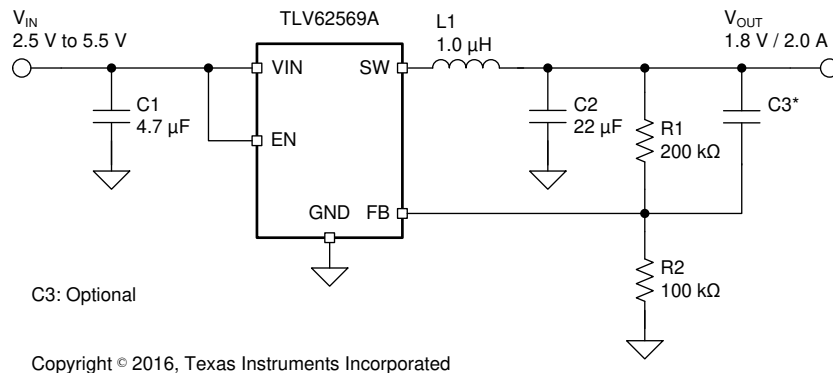


图 6. TLV62569A 1.8-V Output Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	2.0 A

表 3 lists the components used for the example.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER ⁽¹⁾
C1	4.7 μF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22 μF, Ceramic Capacitor, 6.3 V, X7T, size 0805, GRM21BD70J226ME44	Murata
L1	1.0 μH, Power Inductor, size 4mmx4mm, XAL4020-102ME	Coilcraft
R1,R2,R3	Chip resistor, 1%, size 0603	Std.
C3	Optional, 10 pF if it is needed	Std.

(1) See [Third-party Products Disclaimer](#)

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TLV62569A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting the Output Voltage

An external resistor divider is used to set output voltage according to 式 2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200 k Ω for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response (shown in 图 24). A 10-pF capacitance is recommended for R2 of 100-k Ω resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in [SLVA289](#).

8.2.2.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 4. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [μ H] ⁽¹⁾	C_{OUT} [μ F] ⁽²⁾				
		4.7	10	22	47	100
$0.6 \leq V_{OUT} < 1.2$	1				+	
$1.2 \leq V_{OUT}$	1			++ ⁽³⁾	+	

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.

(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.

(3) This LC combination is the standard value and recommended for most applications.

8.2.2.4 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 3 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple

- f_{sw} is the switching frequency
- L is the inductor value

(3)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

8.2.2.5 Input and Output Capacitor Selection

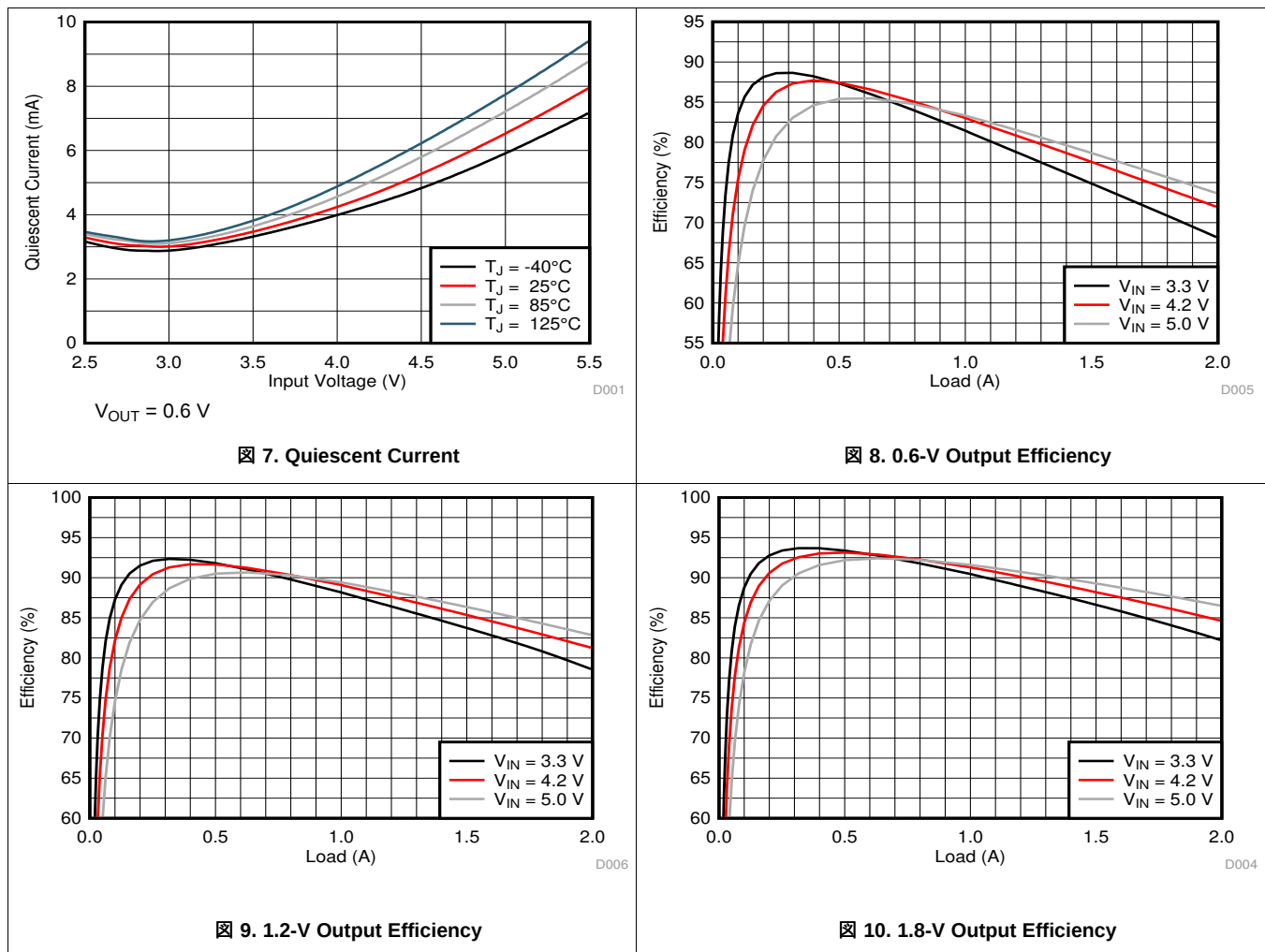
The architecture of the device allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7T or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7- μ F input capacitance is sufficient; a larger value reduces input voltage ripple.

The device is designed to operate with an output capacitor of 22 μ F to 47 μ F, as outlined in 表 4.

8.2.3 Application Performance Curves

$V_{IN} = 5$ V, $V_{OUT} = 1.8$ V, $T_A = 25$ °C, external components shown in 表 3, unless otherwise noted.



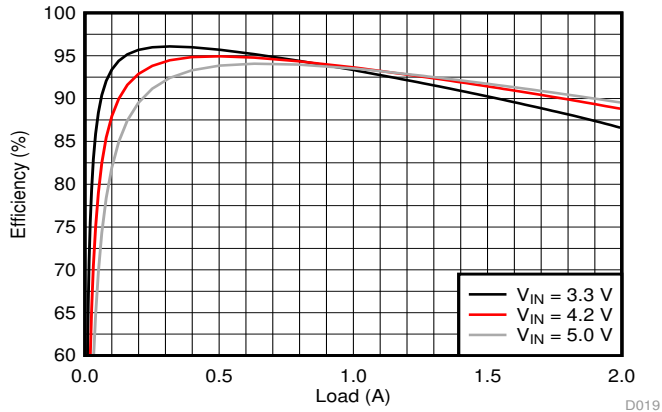


Figure 11. 2.5-V Output Efficiency

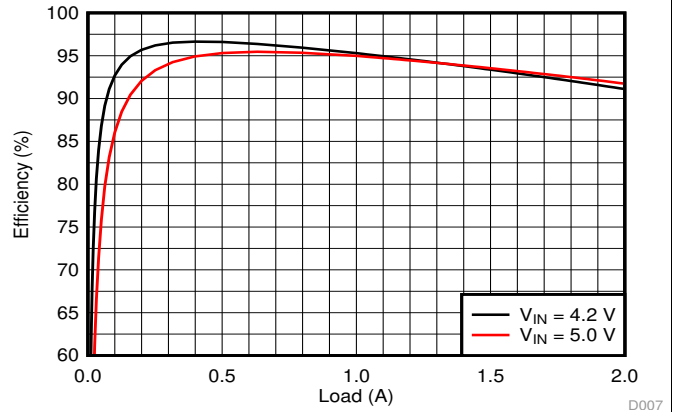


Figure 12. 3.3-V Output Efficiency

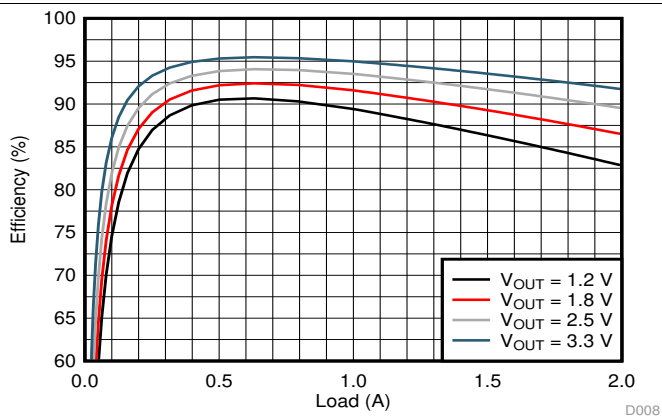


Figure 13. 5.0-V Input Efficiency

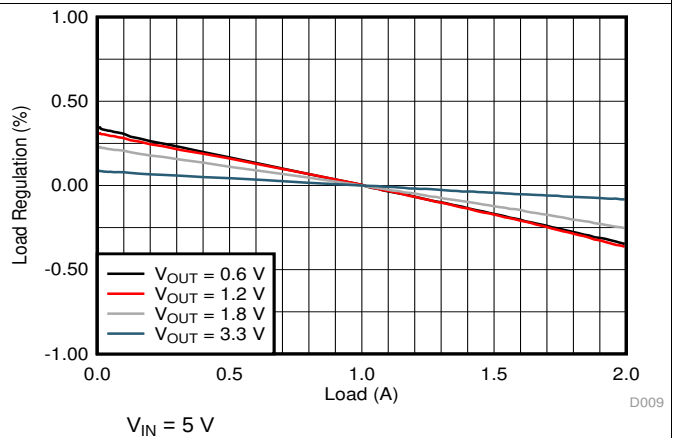


Figure 14. Load Regulation

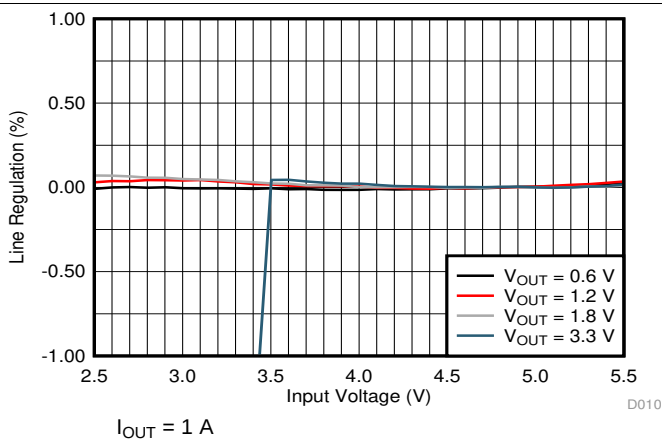
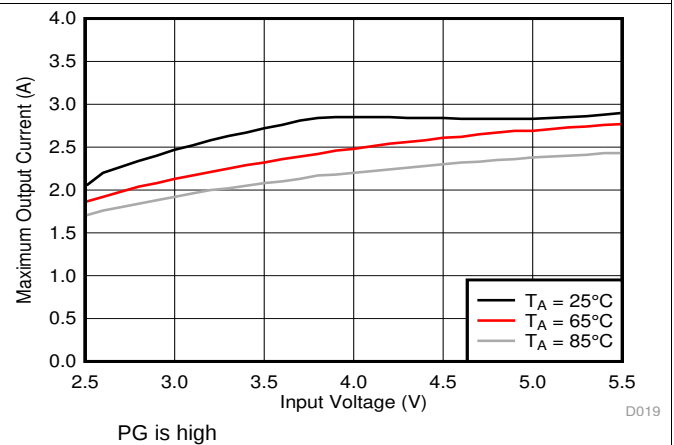


Figure 15. Line Regulation



PG is high

Figure 16. Maximum Output Current at $V_{OUT} = 1.8\text{ V}$

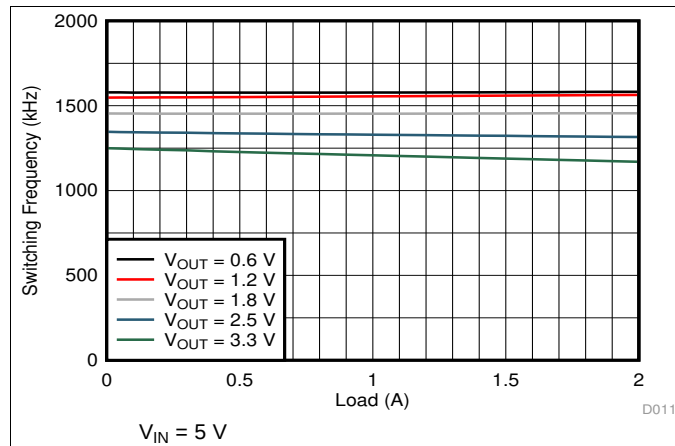


图 17. Switching Frequency vs Load

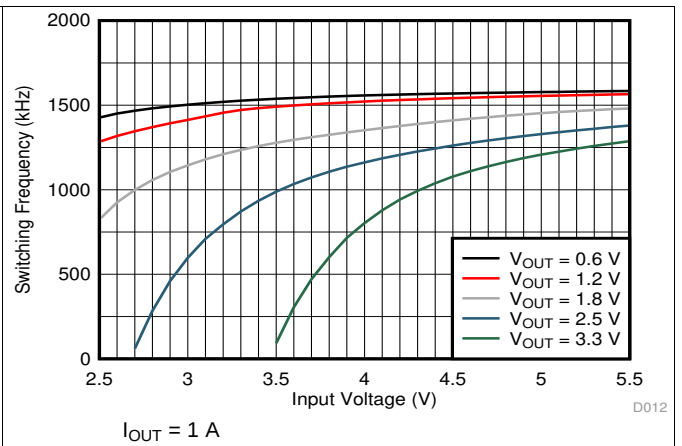


图 18. Switching Frequency vs Input Voltage

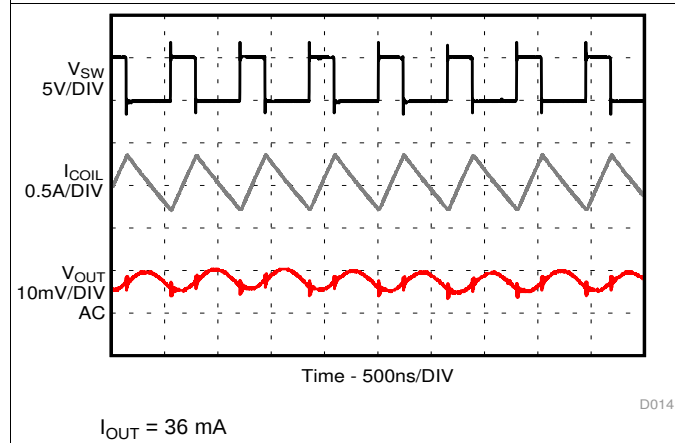


图 19. PWM Operation

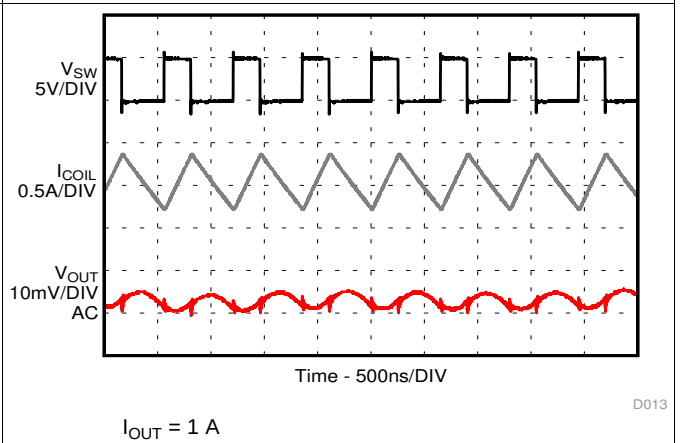


图 20. PWM Operation

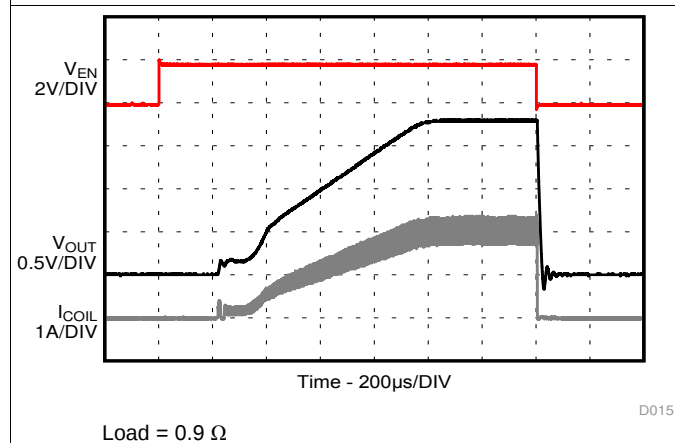


图 21. Startup and Shutdown with Load

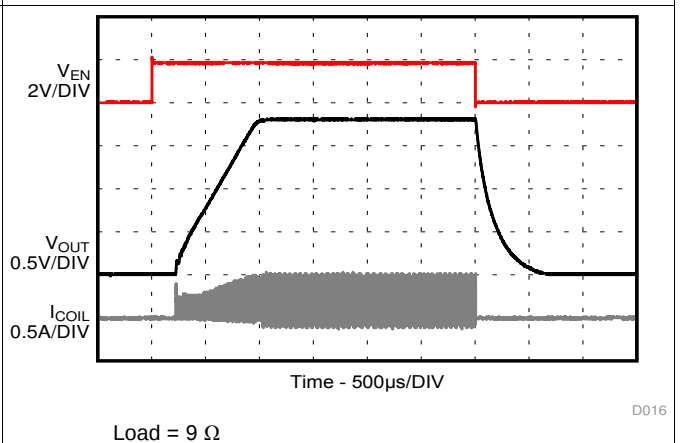
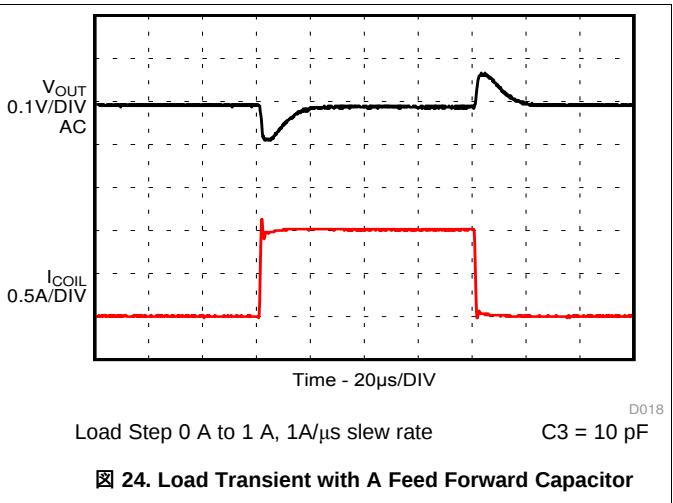
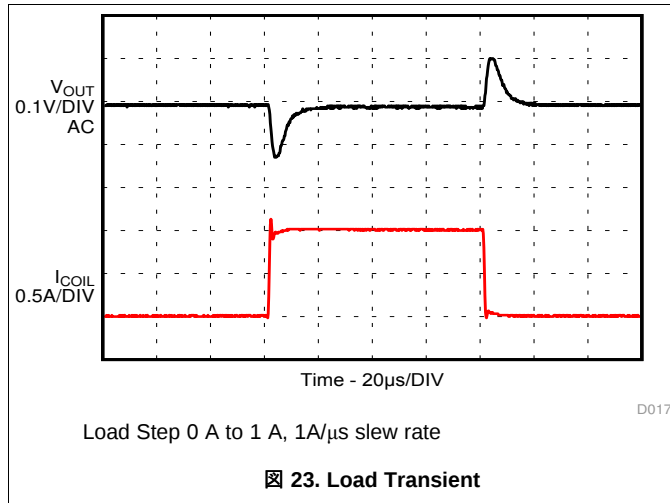


图 22. Startup and Shutdown with Load



9 Power Supply Recommendations

The power supply to the TLV62569A must have a current rating according to the supply voltage, output voltage and output current.

10 Layout

10.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62569A device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

10.2 Layout Example

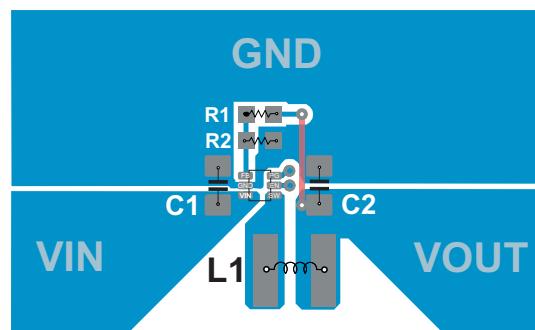


Figure 25. TLV62569APDRL Layout

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes [SZZA017](#) and [SPRA953](#).

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.1.2 開発サポート

11.1.2.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designerにより、TLV62569Aデバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WBENCHでご覧になれます。

11.2 ドキュメントのサポート

11.2.1 関連資料

- テキサス・インスツルメンツ、『[Semiconductor and IC Package Thermal Metrics](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#)』アプリケーション・レポート (英語)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.5 商標

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

11.6 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62568ADRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	(1BE, 1BF)	Samples
TLV62568ADRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	(1BE, 1BF)	Samples
TLV62568APDRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BF	Samples
TLV62568APDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BF	Samples
TLV62569ADRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BG	Samples
TLV62569ADRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BG	Samples
TLV62569APDRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BH	Samples
TLV62569APDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	1BH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

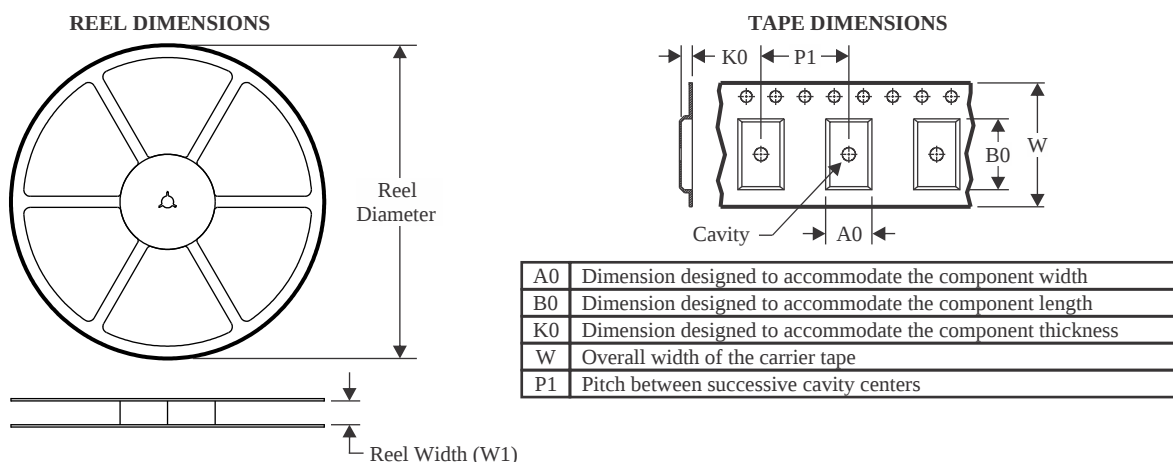
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

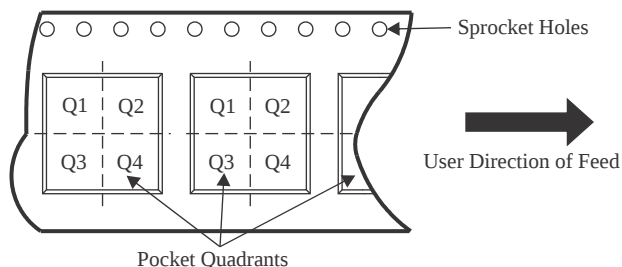
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

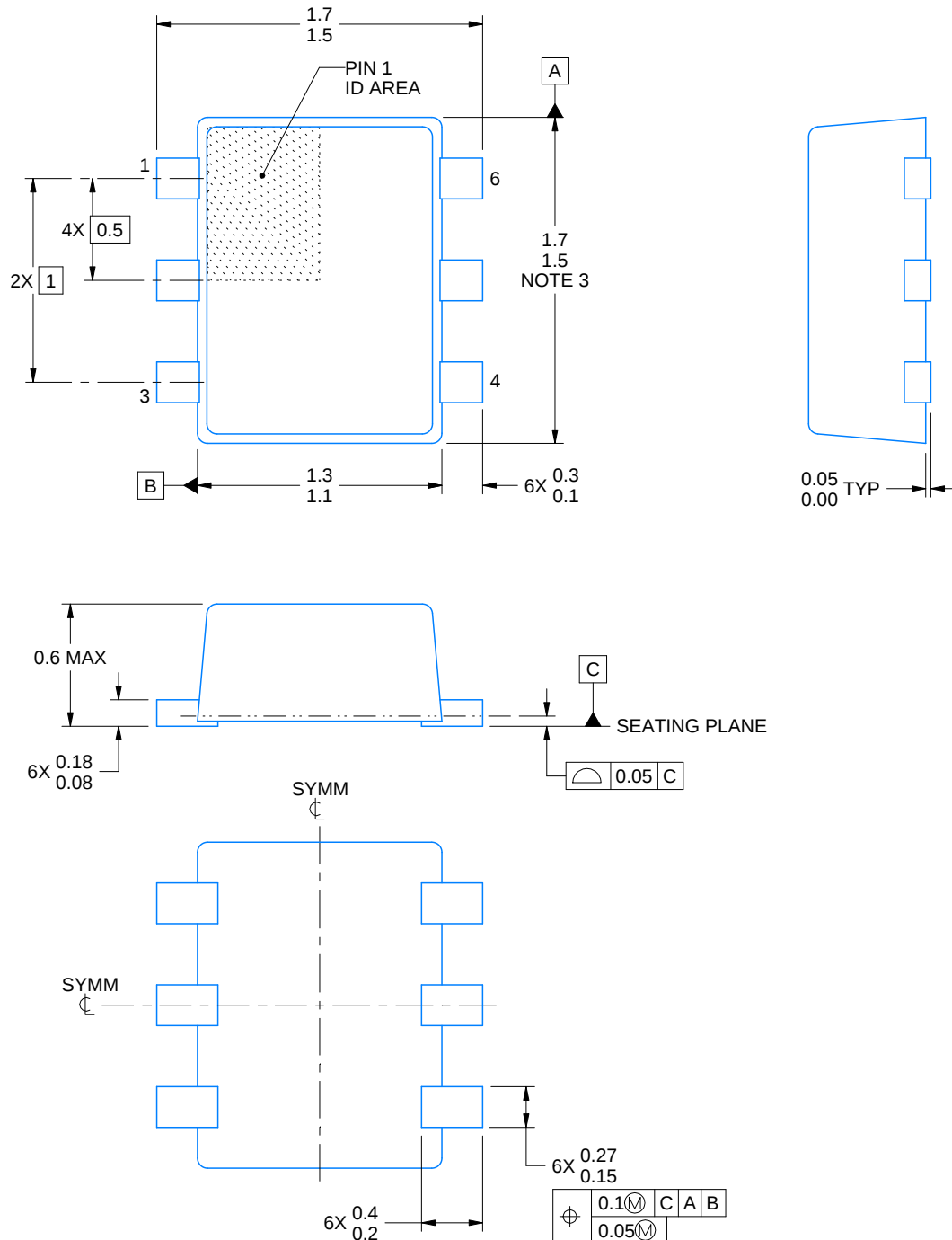
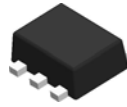
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62568ADRLR	SOT-5X3	DRL	6	3000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62568ADRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568ADRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62568ADRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568APDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62568APDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568APDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568APDRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62569ADRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569ADRLR	SOT-5X3	DRL	6	3000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62569ADRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569ADRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62569APDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62569APDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569APDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569APDRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62568ADRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62568ADRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62568ADRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62568ADRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62568APDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62568APDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62568APDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62568APDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569ADRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569ADRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569ADRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569ADRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569APDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569APDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569APDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569APDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0



4223266/C 12/2021

NOTES:

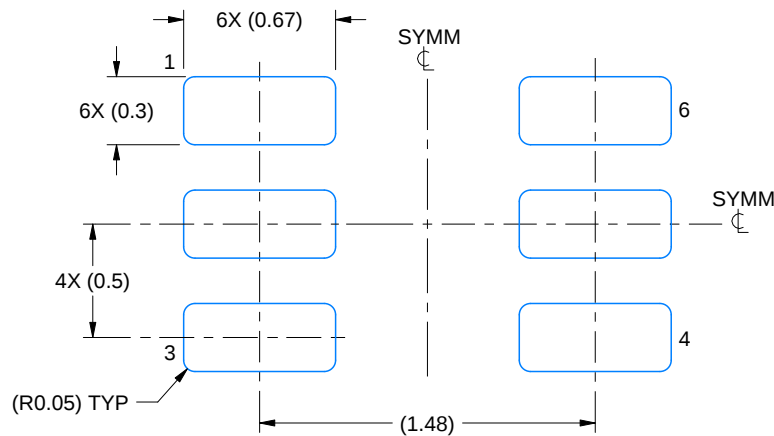
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

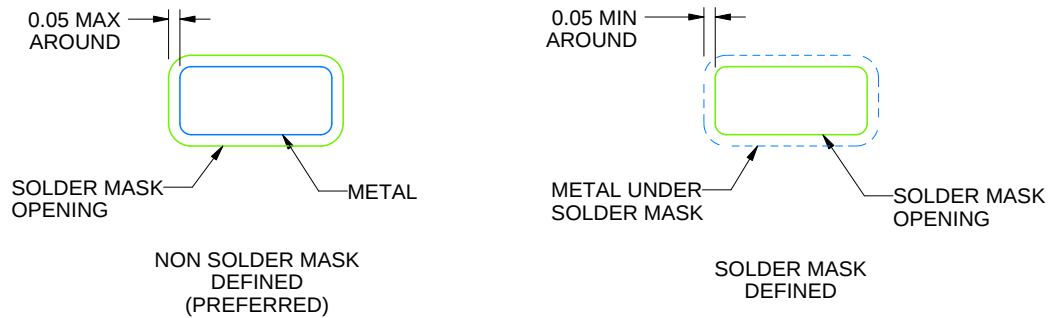
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

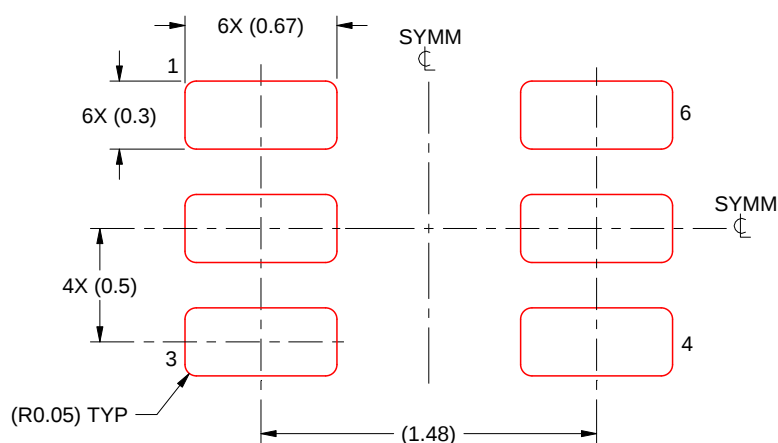
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated