TEXAS INSTRUMENTS
TLV62569, TLV62569P
JAJSCR5C – DECEMBER 2016 – REVISED OCTOBER 2017

TLV62569 2A高効率同期整流降圧型コンバータ、SOTパッケージ入り

1 特長

- 最大95%の効率
- 低$R_{DS(ON)}$のスイッチ、100mΩ/60mΩ
- 入力電圧範囲: 2.5V～5.5V
- 出力電圧は0.6V～V_{IN}の範囲で調整可能
- 省電力モードにより軽負荷時の効率を向上
- 100%デューティ·サイクル動作により低いドロップアウト電圧を実現
- 動作時の静止電流35µA
- 標準スイッチング周波数1.5MHz
- パワー・グッド出力
- 過電流保護
- 内部的なソフト・スタートアップ
- サーマル・シャットダウン保護機能
- SOTパッケージで供給
- TLV62568とピン単位で互換
- WEBENCH® Power Designerにより、TLV62569を使用するカスタム設計を作成

2 アプリケーション

- 汎用POL電源
- セットトップ・ボックス
- ネットワーク用ビデオカメラ
- ワイヤレス・ルータ
- ハードディスク・ドライバ

3 概要

TLV62569デバイスは、同期整流降圧型DC/DCコンバータで、高効率と小型のソリューション向けに最適化されています。このデバイスには、最大2Aの出力電流を供給できるスイッチが内蔵されています。

中負荷から高負荷では、デバイスはパルス幅変調(PWM)モードで、1.5MHzのスイッチング周波数で動作します。軽負荷時には、デバイスは自動的に省電力モード(PSM)へ移行し、負荷電流範囲の全体にわたって高い効率を維持します。シャットダウン時には、消費電流が2µA未満に減少します。

TLV62569の出力電圧は、外付けの分圧抵抗によって変更できます。内部のソフトスタート回路により、スタートアップ時の突入電流が制限されます。その他、過電流保護、サーマル・シャットダウン保護、パワー・グッドなどの機能も内蔵されています。このデバイスは、SOT23およびSOT563パッケージで供給されます。

製品情報(1)

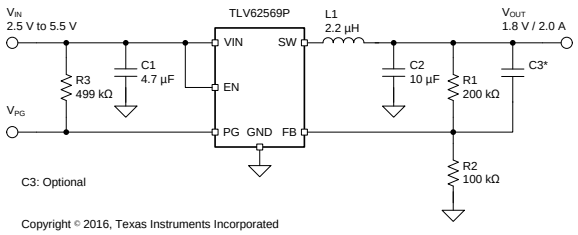
型番	パッケージ	本体サイズ(公称)
TLV62569DBV	SOT23 (5)	2.90mm×2.80mm
TLV62569PDDC	SOT23 (6)	
TLV62569DRL	SOT563 (6)	1.60mm×1.60mm
TLV62569PDRL	SOT563 (6)	

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイスの比較

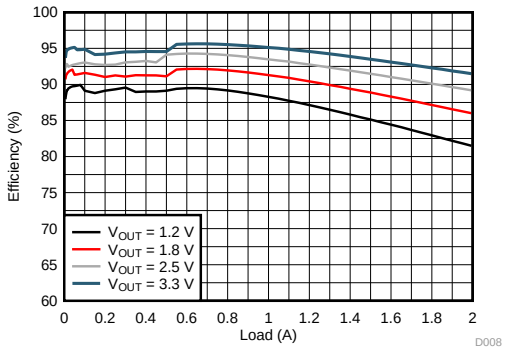
型番	機能	マーキング記号
TLV62569DBV	-	16AF
TLV62569PDDC	パワー・グッド	7G
TLV62569DRL	-	19D
TLV62569PDRL	パワー・グッド	19E

概略回路図



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5V入力電圧時の効率



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (July 2017) から Revision C に変更 **Page**

- TLV62569DRLおよびTLV62569PDRLを量産ステータスに 変更 ... 1
- 「デバイスの比較」表でTLV62569DRLおよびTLV62569PDRLのマーキング記号を 追加 ... 1
- Added DRL package thermal information ... 4
- Corrected editorial error of EN pin threshold voltage ... 4
- Added current limit for TLV62569DRL and TLV62569PDRL ... 5
- 追加 TLV62569PDRL layout example ... 13

Revision A (March 2017) から Revision B に変更 **Page**

- TLV62569PDDCを量産ステータスに 変更 ... 1
- 「デバイスの比較」表を1ページに移動 ... 1
- Added DDC package thermal information ... 4
- Added startup time of TLV62569PDDC ... 4

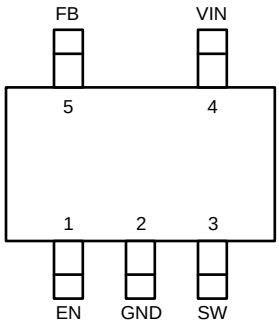
2016年12月発行のものから更新 **Page**

- WEBENCH®モデル 追加 ... 1

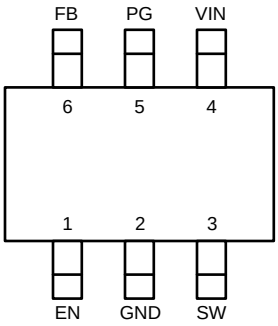
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5 Pin Configuration and Functions

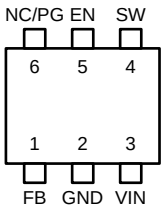
SOT23-5
DBV Package
(Top View)



SOT23-6
DDC Package
(Top View)



SOT563-6
DRL Package
(Top View)



Pin Functions

PIN NUMBER				I/O/PWR	DESCRIPTION
NAME	SOT23-5	SOT23-6	SOT563-6		
EN	1	1	5	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
GND	2	2	2	PWR	Ground pin.
SW	3	3	4	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	4	4	3	PWR	Power supply voltage input.
PG	-	5	6	O	Power good open drain output pin for TLV62569P. The pull-up resistor should not be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating.
FB	5	6	1	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
NC	-	-	6	O	No connection pin for TLV62569DRL. The pin can be connected to the output or the ground. Or leave it floating.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PG	–0.3	6	V
	SW (DC)	–0.3	V_{IN}+0.3	V
	SW (AC, less than 10ns)(3)	–3.0	9	V
	FB	–0.3	5.5	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and the device is not switching. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions (1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage	0.6		V_{IN}	V
I_{OUT}	Output current	0		2	A
T_J	Operating junction temperature	–40		125	°C
I_{SINK_PG}	Sink current at PG pin			1	mA

(1) Refer to the *Application and Implementation* section for further information.

6.4 Thermal Information

THERMAL METRIC (1)		DBV (5 Pins)	DDC (6 Pins)	DRL (6 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.2	106.2	146.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	137.5	52.9	51.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.2	31.2	27.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	11.3	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.6	31.6	27.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 5.0 V, T_J = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN pin	Not switching		35		uA
I_{SD}	Shutdown current into VIN pin	EN = 0 V		0.1	2	µA
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.3	2.45	V
	Under voltage lock out hysteresis			100		mV
T_{JSD}	Thermal shutdown	Junction temperature rising		150		°C
		Junction temperature falling		130		
LOGIC INTERFACE						
V_{IH}	High-level threshold at EN pin	2.5 V ≤ V_{IN} ≤ 5.5 V		0.95	1.2	V
V_{IL}	Low-level threshold at EN pin	2.5 V ≤ V_{IN} ≤ 5.5 V	0.4	0.85		V
t_{SS}	Soft startup time	TLV62569DBV		800		µs
		TLV62569PDDC, TLV62569DRL, TLV62569PDRL		900		
V_{PG}	Power good threshold	V_{FB} rising, referenced to V_{FB} nominal		95%		
		V_{FB} falling, referenced to V_{FB} nominal		90%		
$V_{PG,OL}$	Power good low-level output voltage	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		µA
$t_{PG,DLY}$	Power good delay time	V_{FB} falling		40		µs
OUTPUT						
V_{FB}	Feedback regulation voltage		0.588	0.6	0.612	V

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Electrical Characteristics (continued)

V_{IN} = 5.0 V, T_J = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	High-side FET on resistance			100		mΩ
	Low-side FET on resistance			60		
I_{LIM}	High-side FET current limit	TLV62569DBV, TLV62569PDDC	3			A
		TLV62569DRL, TLV62569PDRL	2.5			
f_{SW}	Switching frequency	V_{OUT} = 2.5 V		1.5		MHz

6.6 Typical Characteristics

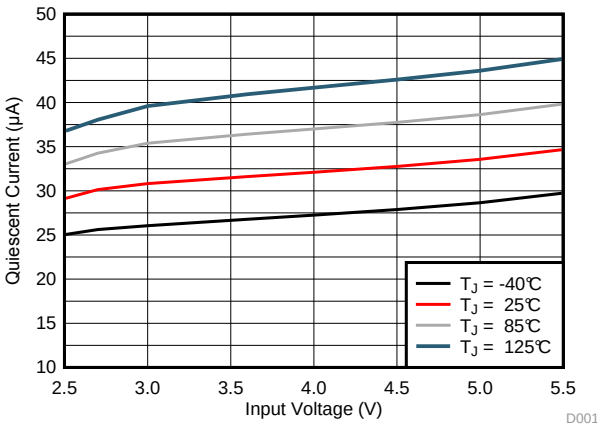


図 1. Quiescent Current vs Input Voltage

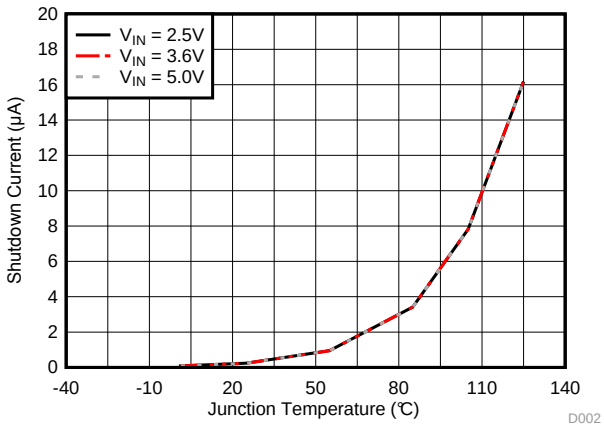


図 2. Shutdown Current vs Junction Temperature

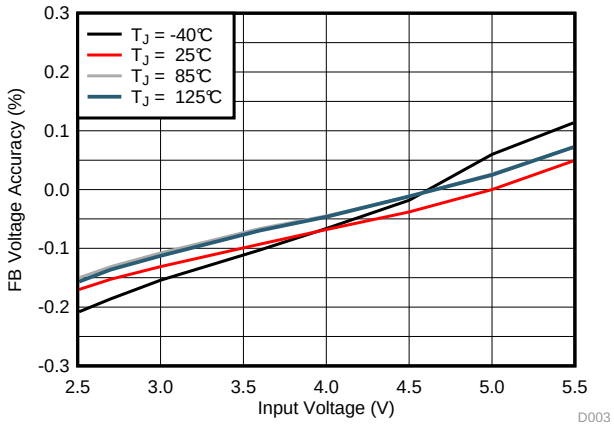


図 3. FB Voltage Accuracy

7 Detailed Description

7.1 Overview

The TLV62569 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.2 Functional Block Diagrams

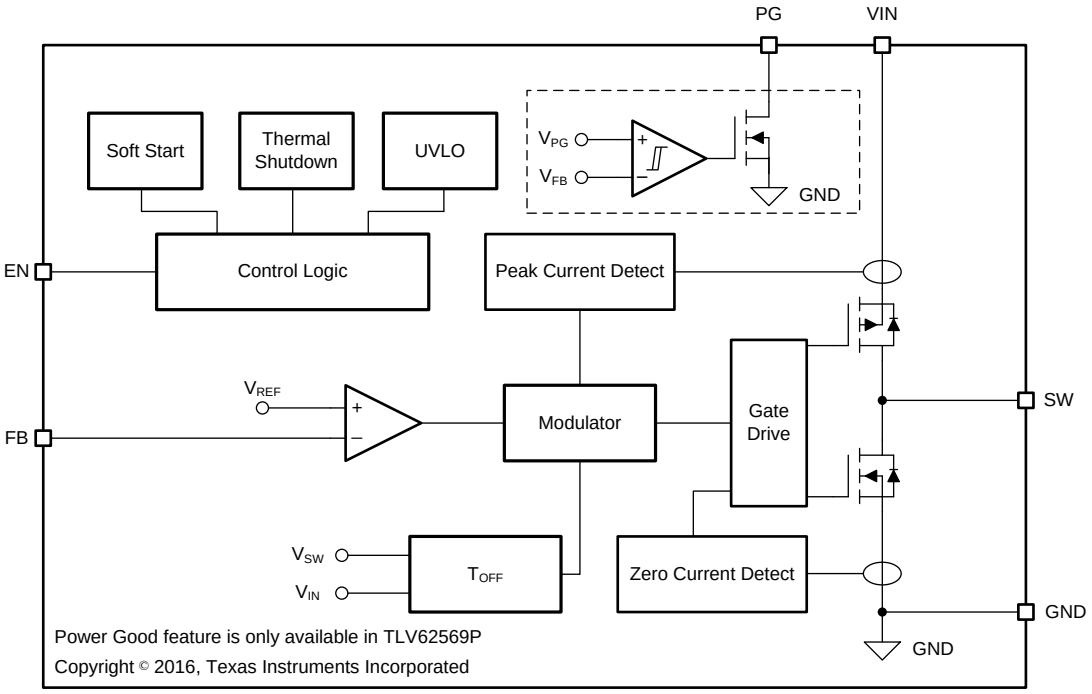


図 4. TLV62569 Functional Block Diagram

7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor.

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

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Feature Description (continued)

7.3.3 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TLV62569 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.4 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The TLV62569 adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

7.3.5 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

7.3.6 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

7.4.2 Power Good

The TLV62569P has a power good output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4\ V$	√	

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

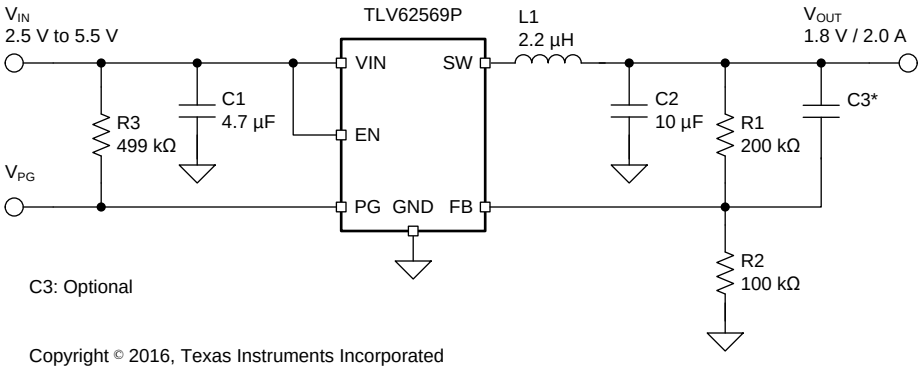


図 5. TLV62569 1.8-V Output Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	2.0 A

表 3 lists the components used for the example.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	10 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A106KE51L	Murata
L1	2.2 µH, Power Inductor, size 4mmx4mm, XAL4020-222ME	Coilcraft
R1,R2,R3	Chip resistor,1%,size 0603	Std.
C3	Optional, 6.8 pF if it is needed	Std.

(1) See *Third-party Products Disclaimer*

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62569 device with the WEBENCH® Power Designer.

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1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting the Output Voltage

An external resistor divider is used to set output voltage according to 式 2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200 kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response (shown in 図 19). 6.8-pF capacitance is recommended for R2 of 100-kΩ resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289.

8.2.2.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 4. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)				
		4.7	10	22	2 x 22	100
0.6 ≤ V_{OUT} < 1.2	1				+	
	2.2				++(3)	
1.2 ≤ V_{OUT} < 1.8	1			+	+	
	2.2			++(3)	+	
1.8 ≤ V_{OUT}	1		+	+	+	
	2.2		++(3)	+	+	

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

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8.2.2.4 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 3 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value

(3)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

8.2.2.5 Input and Output Capacitor Selection

The architecture of the TLV62569 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The TLV62569 is designed to operate with an output capacitor of 10 µF to 47 µF, as outlined in 表 4.

8.2.3 Application Performance Curves

V_{IN} = 5 V, V_{OUT} = 1.8 V, L = 2.2 µH, T_A = 25 °C, unless otherwise noted.

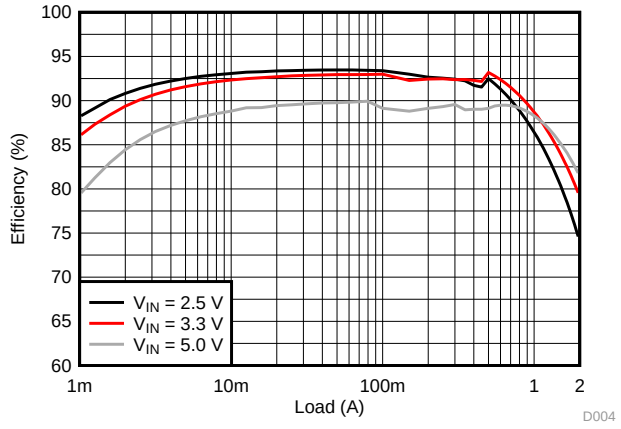


図 6. 1.2-V Output Efficiency

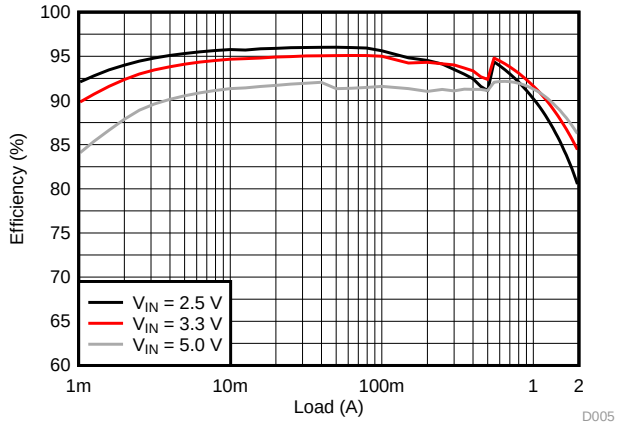


図 7. 1.8-V Output Efficiency

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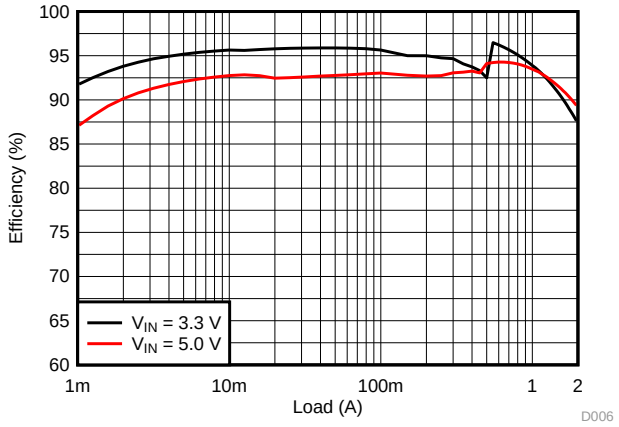


図 8. 2.5-V Output Efficiency

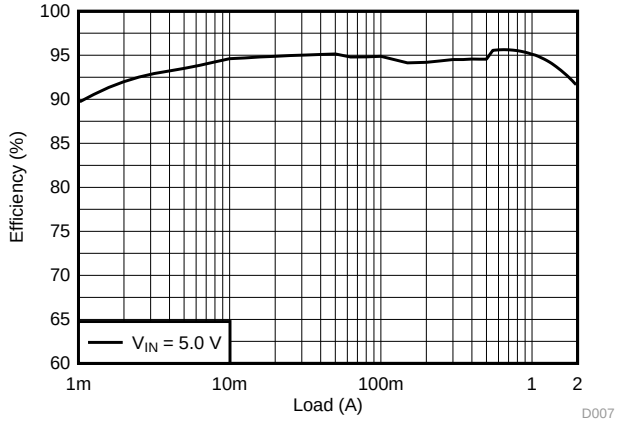
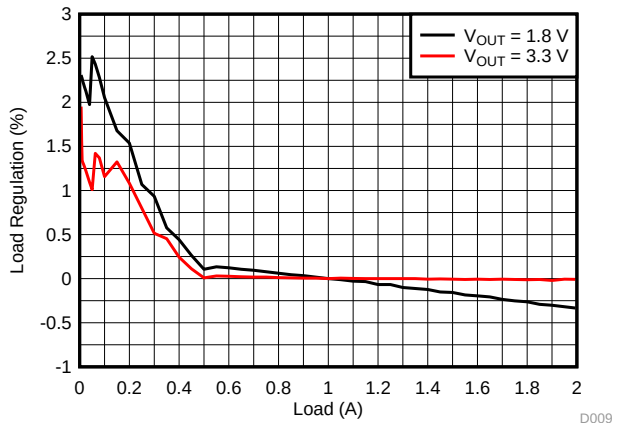
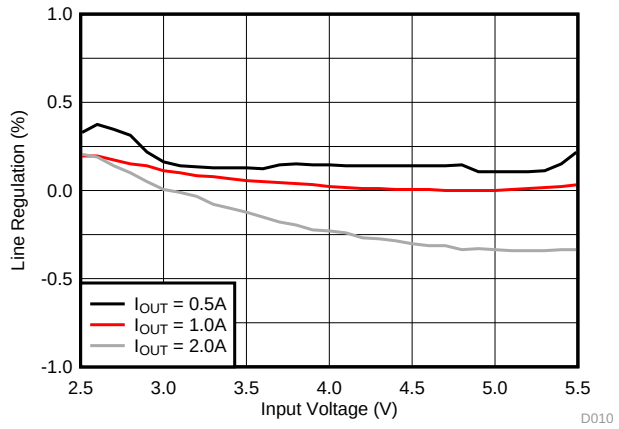


図 9. 3.3-V Output Efficiency



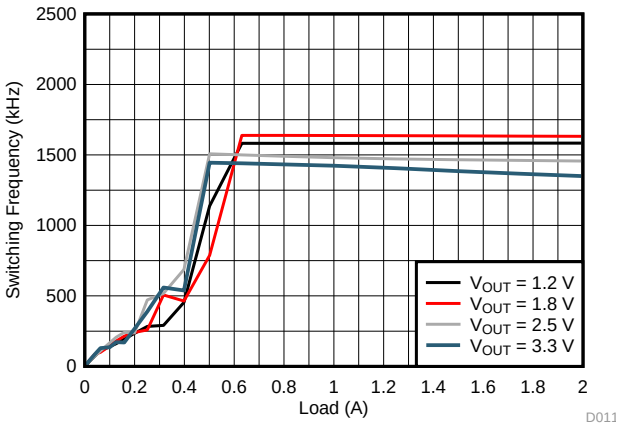
V_{IN} = 5 V

図 10. Load Regulation



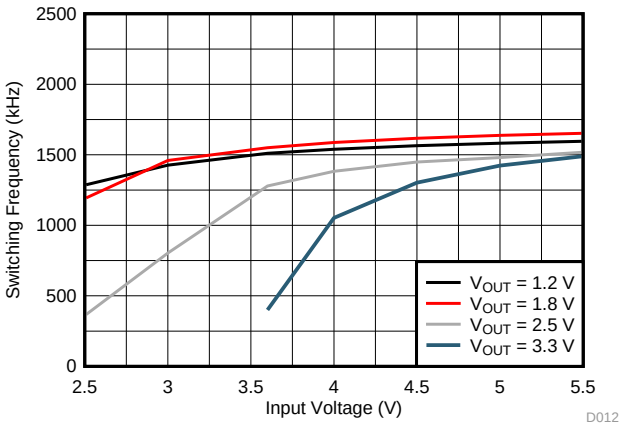
V_{OUT} = 1.8 V

図 11. Line Regulation



V_{IN} = 5 V

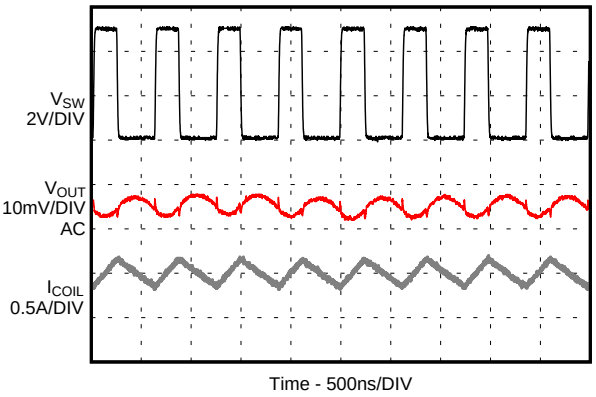
図 12. Switching Frequency vs Load



I_{OUT} = 1 A

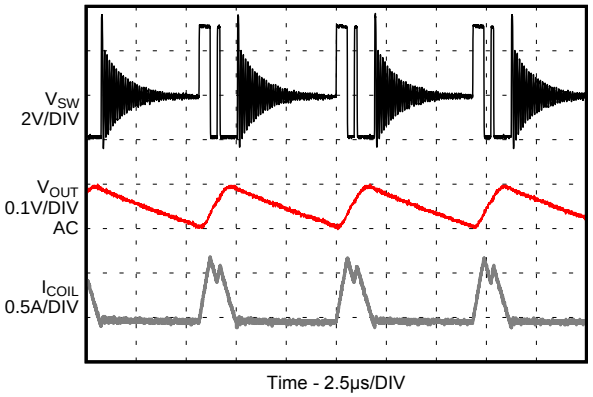
図 13. Switching Frequency vs Input Voltage

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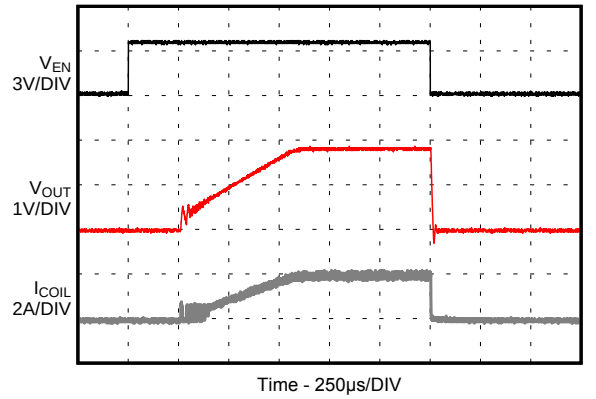
I_{OUT} = 1 A

図 14. PWM Operation



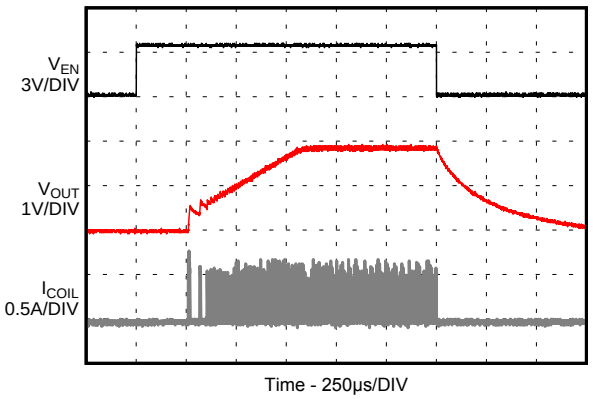
I_{OUT} = 0.1 A

図 15. Power Save Mode Operation



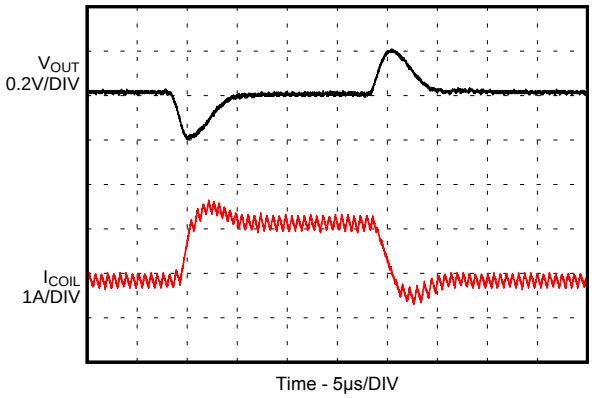
I_{OUT} = 2 A

図 16. Startup and Shutdown with Load



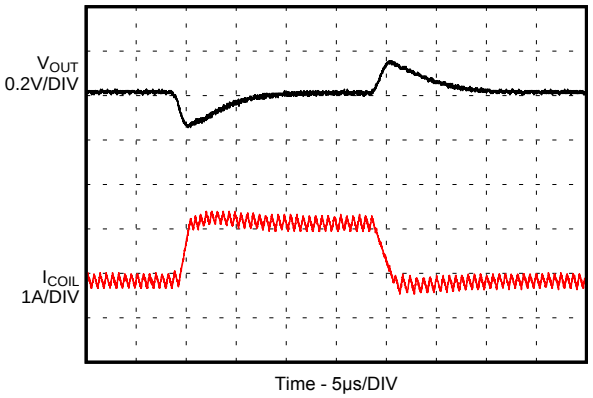
I_{OUT} = 0.1 A

図 17. Startup and Shutdown with Load



Load Step 0.8 A to 2 A, 1A/µs slew rate

図 18. Load Transient



Load Step 0.8 A to 2 A, 1A/µs slew rate C3 = 6.8 pF

図 19. Load Transient

9 Power Supply Recommendations

The power supply to the TLV62569 must have a current rating according to the supply voltage, output voltage and output current.

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10 Layout

10.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62569 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

10.2 Layout Example

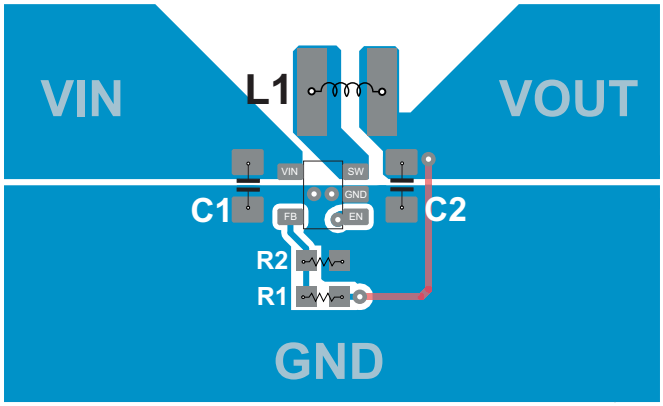


図 20. TLV62569DBV Layout

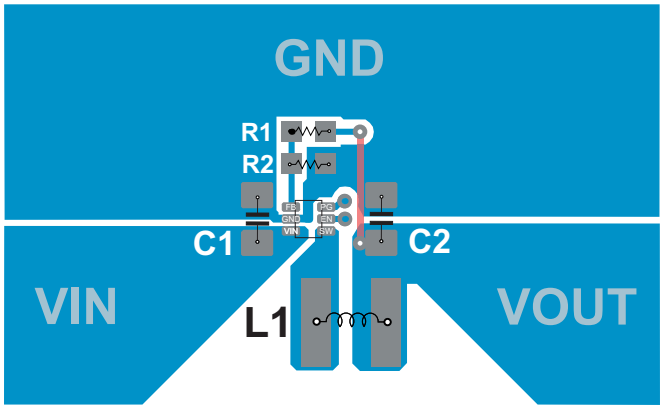


図 21. TLV62569PDRL Layout

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

11.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TLV62569を使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントのサポート

11.2.1 関連資料

『半導体およびICパッケージの熱指標』アプリケーション・レポート(SPRA953)

『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』アプリケーション・レポート(SZZA017)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV62569DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	16AF
TLV62569DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16AF
TLV62569DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16AF
TLV62569DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16AF
TLV62569DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	16AF
TLV62569DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16AF
TLV62569DRLR	Active	Production	SOT-5X3 (DRL) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	19D
TLV62569DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	19D
TLV62569DRLT	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	19D
TLV62569DRLT.A	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	19D
TLV62569PDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	(6D9, 6DW)
TLV62569PDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(6D9, 6DW)
TLV62569PDDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	(6D9, 6DW)
TLV62569PDDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(6D9, 6DW)
TLV62569PDRLR	Active	Production	SOT-5X3 (DRL) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	19E
TLV62569PDRLR.A	Active	Production	SOT-5X3 (DRL) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	19E
TLV62569PDRLT	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	19E
TLV62569PDRLT.A	Active	Production	SOT-5X3 (DRL) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	19E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

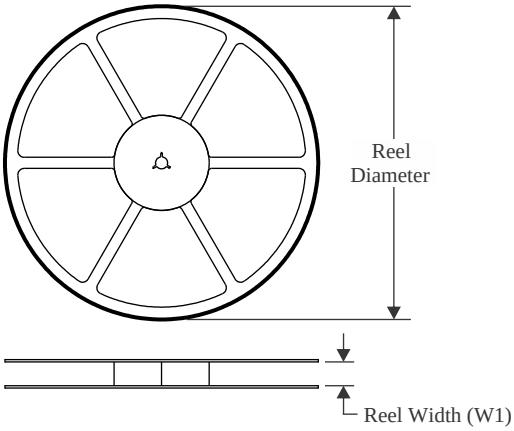
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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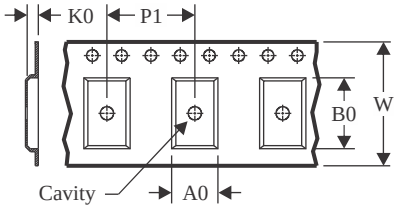
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

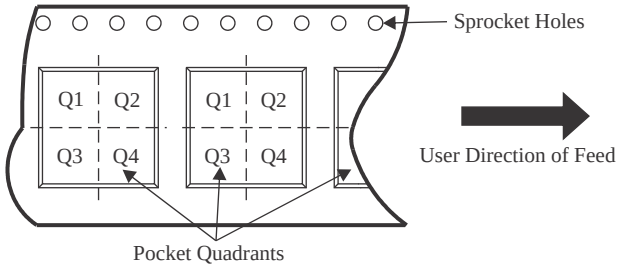


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

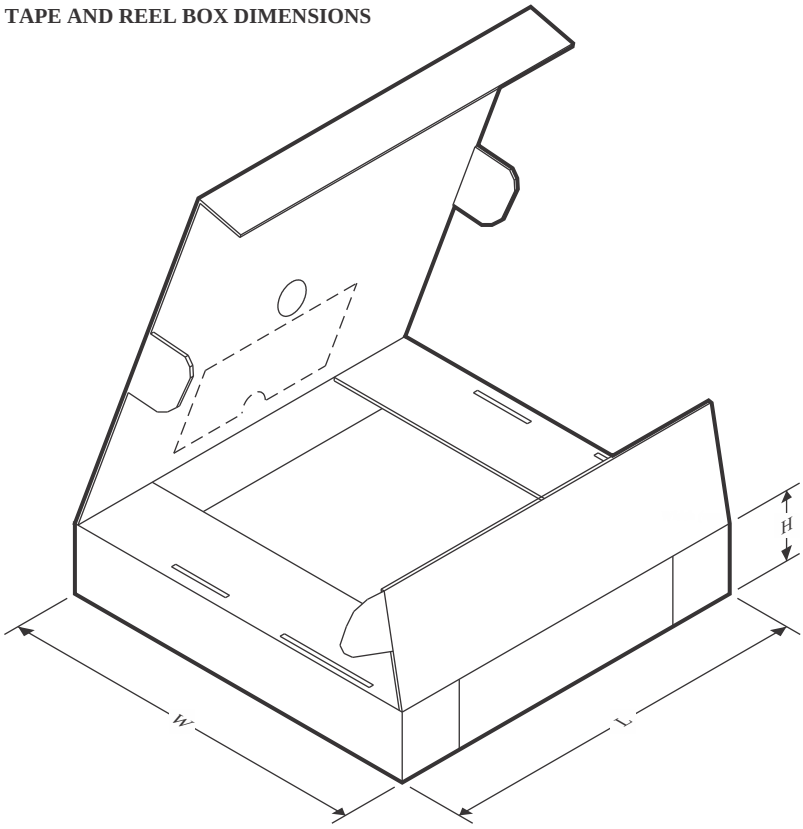


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62569DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569DRLR	SOT-5X3	DRL	6	3000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62569DRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569DRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569DRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TLV62569PDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569PDDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62569PDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62569PDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569PDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569PDRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

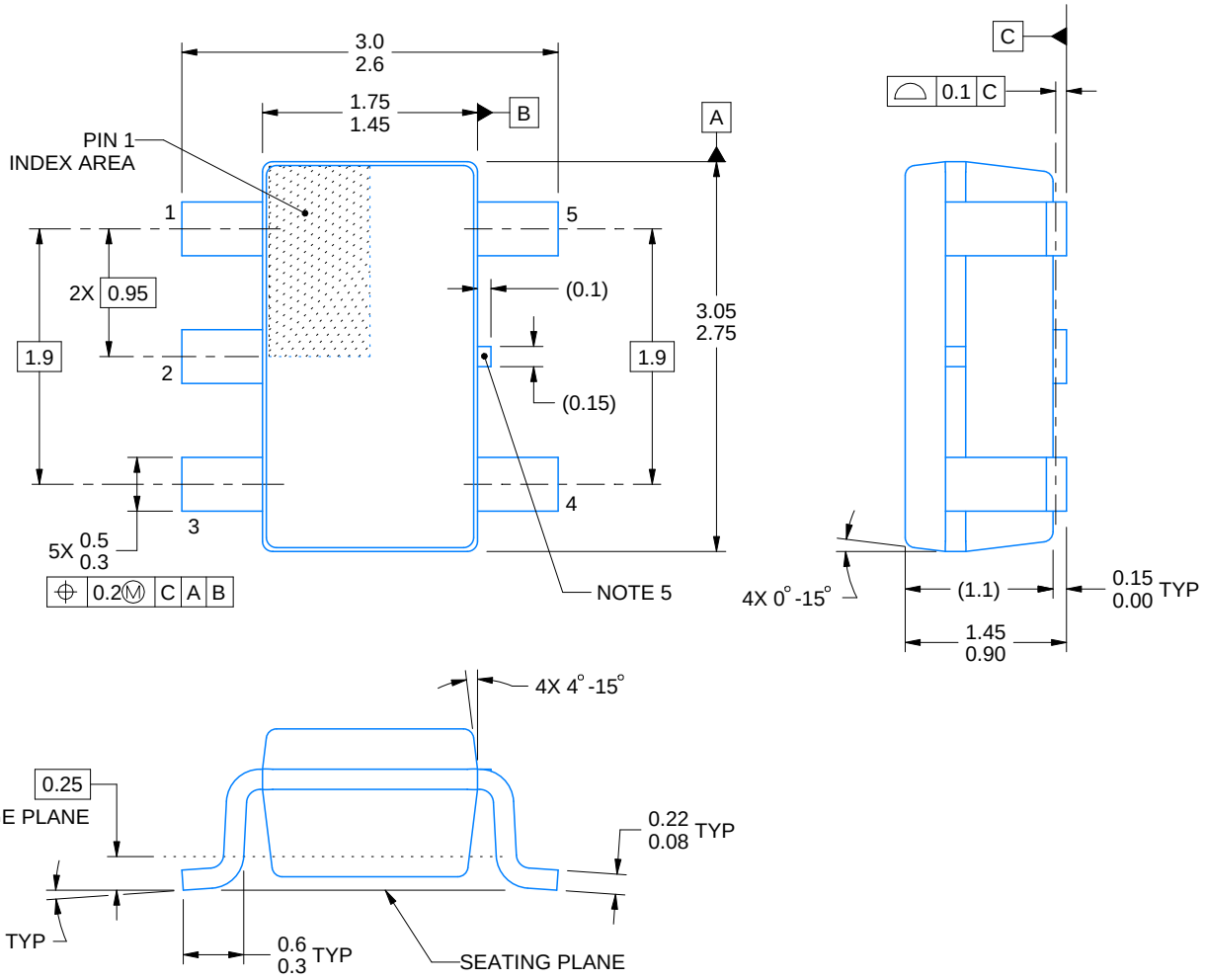
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62569DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62569DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62569DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV62569DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62569DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62569DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62569DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62569DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62569DRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569DRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569PDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TLV62569PDDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TLV62569PDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569PDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569PDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569PDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

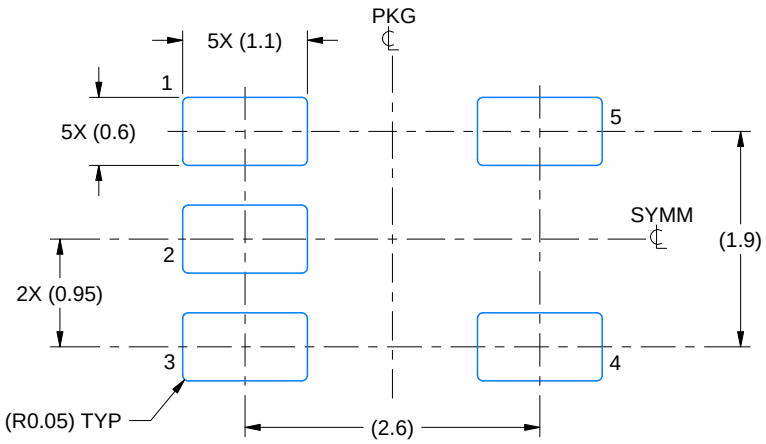
SMALL OUTLINE TRANSISTOR



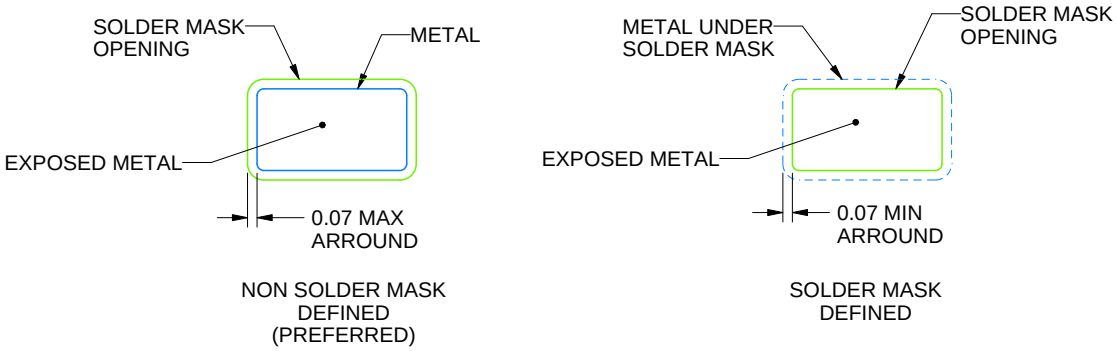
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

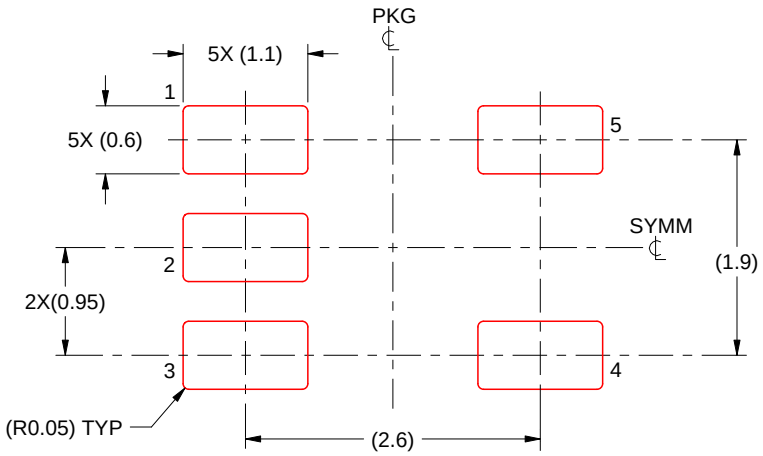


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

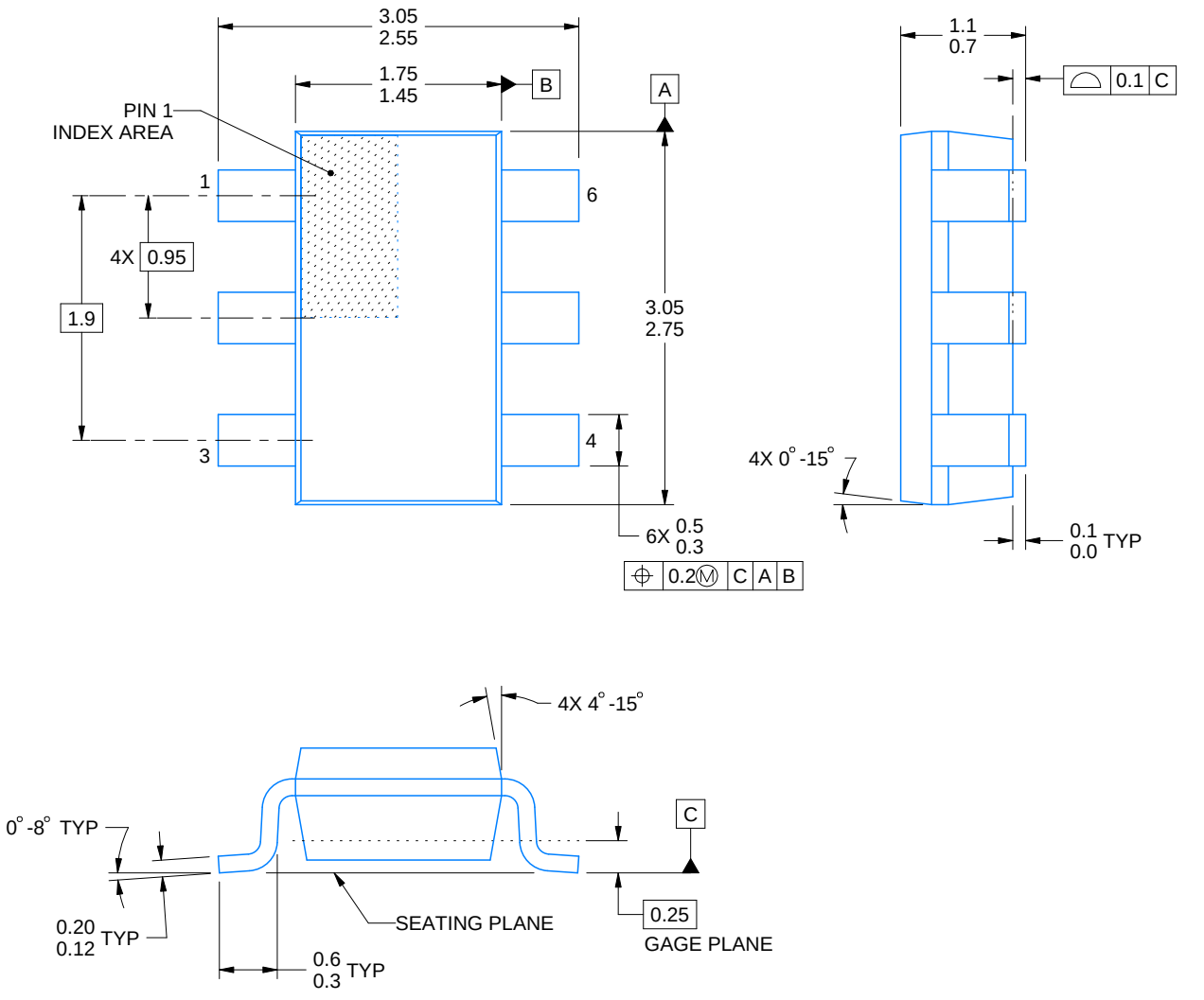
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

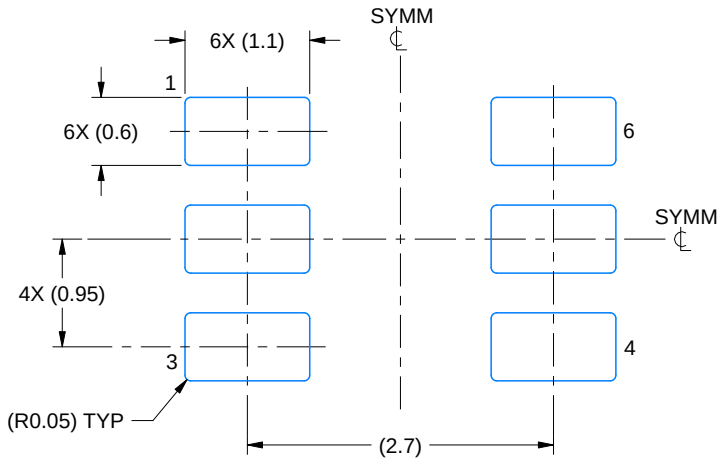
SMALL OUTLINE TRANSISTOR



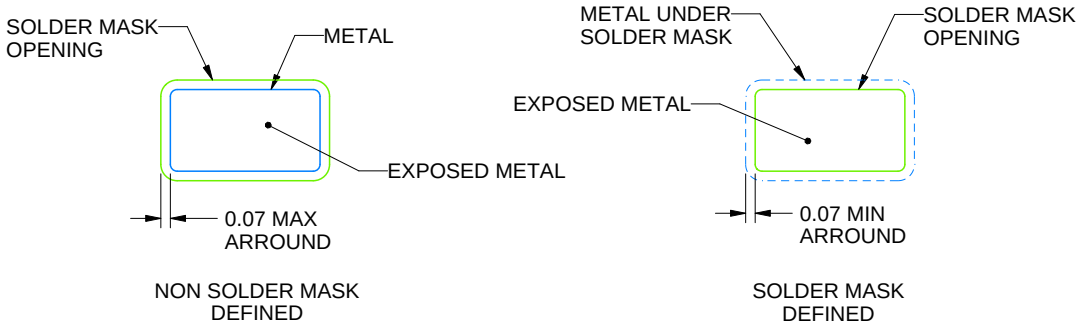
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

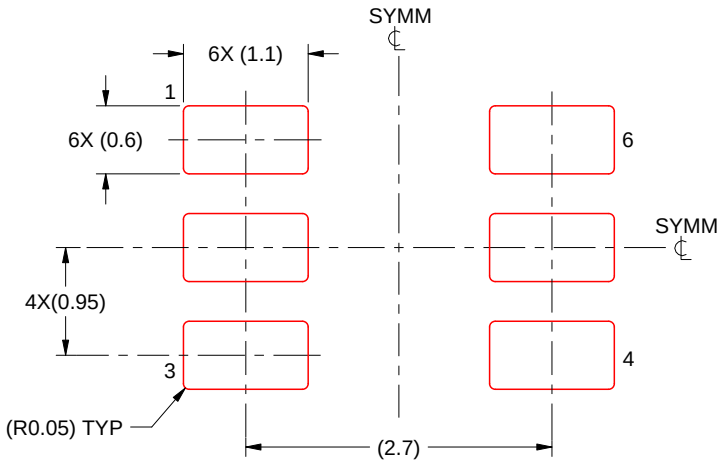


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

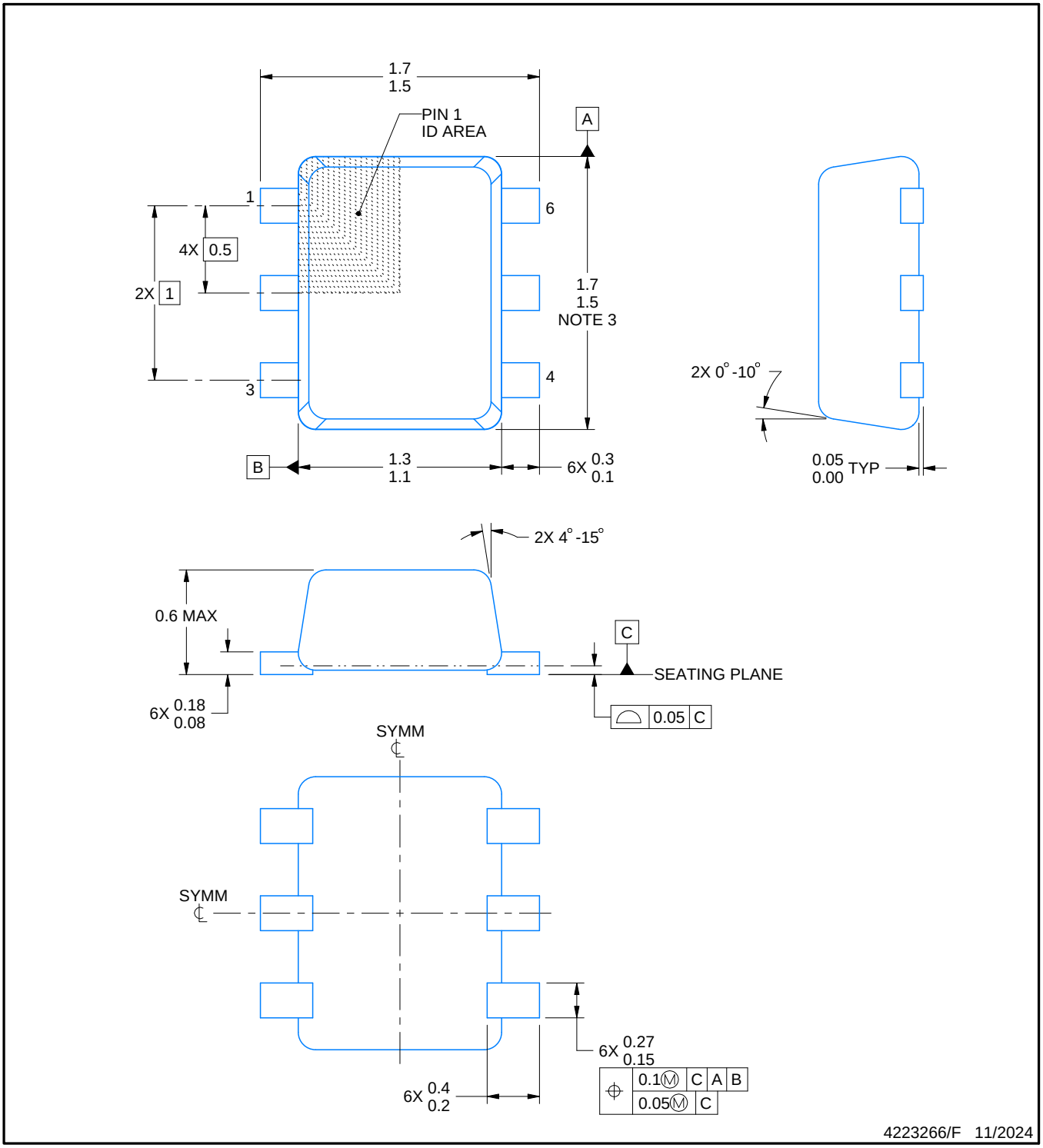


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

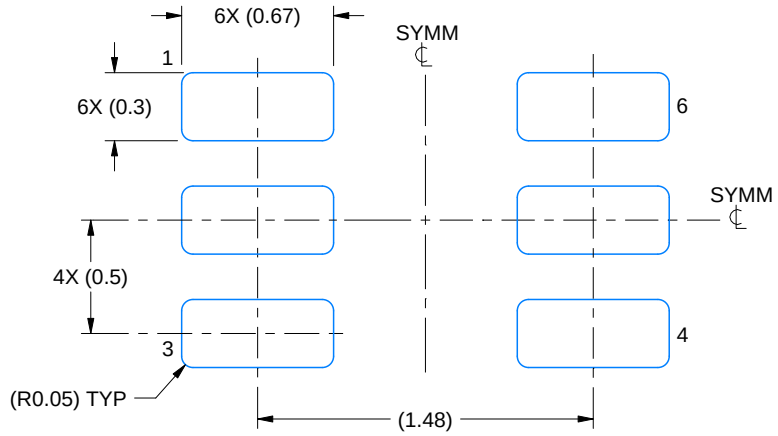
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

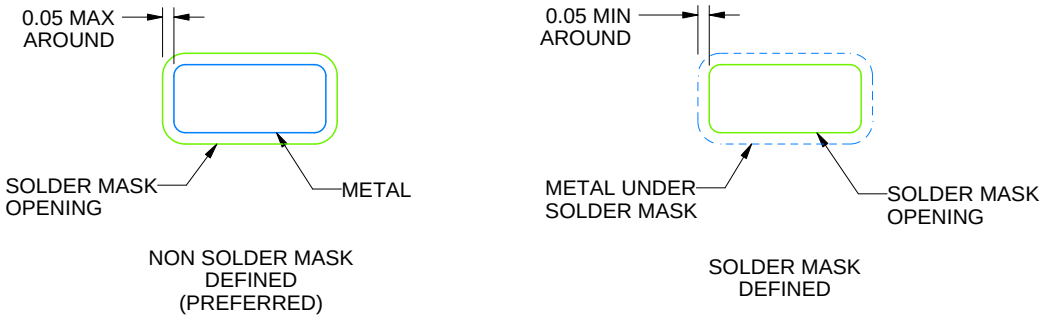
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

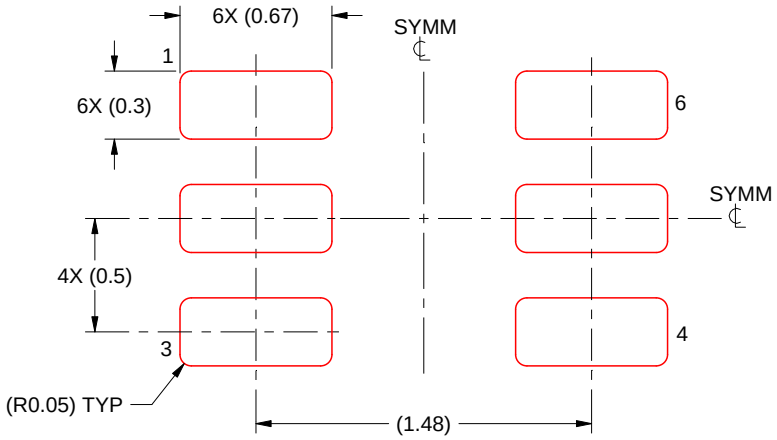
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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