TLV759P 1A、高精度で小さなパッケージの可変LDO

1 特長

- 入力電圧範囲: 1.5V～6.0V
- 可変出力電圧
  - 0.55V～5.5V
- 非常に低いドロップアウト
  - 3.3V_{OUT}、1A時に225mV（最大値）
- 高い出力精度
  - 標準値: 0.7%
  - 温度範囲(85°C)全体にわたる最大値: 1%
- I_Q：25µA（標準値）
- V_{OUT}が単調増加するソフトスタートを内蔵
- パッケージ
  - 2mm×2mmの6ピンWSON (DRV)
- アクティブ出力放電

2 アプリケーション

- セットトップ・ボックス、ゲーム機
- ホーム・シアターおよびエンターテインメント
- デスクトップ、ノートブック、ウルトラブック
- プリンタ
- サーバー
- サーモスタットおよび照明制御
- 電子POS (EPOS)

3 概要

TLV759Pは可変の1A低ドロップアウト(LDO)レギュレータです。このデバイスは、小型の6ピン、2mm×2mmのWSONパッケージで供給され、静止電流が非常に小さく、ラインおよび負荷の過渡特性が高速です。TLV759Pはドロップアウトが1Aで225mVと非常に低く、システムの電力効率向上に役立ちます。

TLV759Pは1.5V～6.0Vの入力電圧範囲に対応し、出力電圧を外部から0.55V～5.5Vの範囲で変更でき、広範なアプリケーション用に最適化されています。出力電圧が低いため、このLDOはコア電圧が低い現代のマイクロコントローラの電源として使用できます。さらに、TLV759P はI_Qが小さく、イネーブル機能によりスタンバイ電力を最小化できます。このデバイスには、突入電流を低減するソフトスタートが内蔵されており、負荷に対して制御された電圧を供給し、スタートアップ時の入力電圧降下を最小化します。

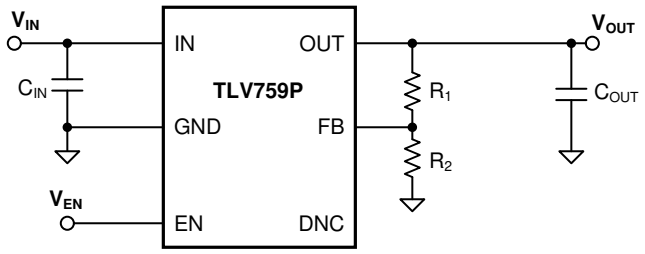
TLV759Pは小さなセラミック出力コンデンサで安定するため、ソリューション全体のサイズを小さくできます。高精度のバンドギャップおよびエラー・アンプにより、25°Cで最大0.7%、温度範囲(85°C)全体にわたって最大1%の高精度が得られます。このデバイスにはサーマル・シャットダウン、電流制限、低電圧誤動作防止(UVLO)機能が内蔵されています。TLV759Pには内部フォールドバック電流制限があり、短絡発生時の熱発散を低減するため役立ちます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
TLV759P	WSON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

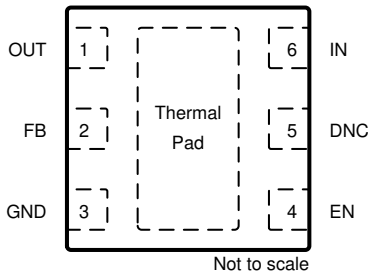
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- ドキュメントのステータスを「事前情報」から「量産データ」に 変更 ... 1

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5 Pin Configuration and Functions

DRV Package
6-Pin Adjustable WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	5	—	Do not connect
EN	4	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the LDO into shutdown mode.
FB	2	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	—	Ground pin
IN	6	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the output of the device as possible.
OUT	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible.
Thermal pad	Pad	—	Connect the thermal pad to a large area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{IN}	–0.3	6.5	V
Enable voltage, V_{EN}	–0.3	6.5	V
Output voltage, V_{OUT}	–0.3	V_{IN} + 0.3(2)	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.0 V, whichever is smaller

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		6.0	V
V_{OUT}	Output voltage	0.55		5.5	V
I_{OUT}	Output current	0		1	A
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor (1)	1		220	µF
V_{EN}	Enable voltage	0		6.0	V
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	–40		125	°C

(1) Minimun derated capacitance of 0.47 µF is required for stability

6.4 Thermal Information

THERMAL METRIC (1)		TLV759 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage	T_J = 25°C			0.55		V
	Output accuracy (1)	T_J = 25°C		–0.7%		0.7%	
		–40°C ≤ T_J ≤ +85°C		–1%		1%	
		–40°C ≤ T_J ≤ +125°C		–1.5%		1.5%	
	Line regulation	$V_{OUT(NOM)}$ + 0.5 V (2) ≤ V_{IN} ≤ 6.0 V			2	7.5	mV
	Load regulation	0.1 mA ≤ I_{OUT} ≤ 1 A, V_{IN} ≥ 2.0 V			0.03		V/A
I_{GND}	Ground current	I_{OUT} = 0 mA	T_J = 25°C	10	25	31	µA
			–40°C ≤ T_J ≤ +125°C			35	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.3 V, 1.5 V ≤ V_{IN} ≤ 6.0 V			0.1	1	µA

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included
(2) V_{IN} = 1.5V for V_{OUT} < 1.0 V

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Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{FB}	Feedback pin current				0.01	0.1	µA
I_{CL}	Output current limit	V_{IN} = $V_{OUT(NOM)}$ + 1.0 V	V_{OUT} = $V_{OUT(NOM)}$ - 0.2 V, V_{OUT} < 1.5 V	1.22	1.44	1.83	A
			V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{OUT} ≥ 1.5 V	1.22	1.44	1.83	
I_{SC}	Short-circuit current limit	V_{IN} = $V_{OUT(NOM)}$ + 1.0 V	V_{OUT} = 0 V		770		mA
V_{DO}	Dropout voltage	I_{OUT} = 1 A, –40°C ≤ T_J ≤ +125°C, V_{OUT} = 0.95 × $V_{OUT(NOM)}$	0.65 V ≤ V_{OUT} < 0.8 V		896	1050	mV
			0.8 V ≤ V_{OUT} < 0.9 V		765	920	
			0.9 V ≤ V_{OUT} < 1.0 V		700	850	
			1.0 V ≤ V_{OUT} < 1.2 V		600	750	
			1.2 V ≤ V_{OUT} < 1.5 V		464	585	
			1.5 V ≤ V_{OUT} < 1.8 V		332	440	
			1.8 V ≤ V_{OUT} < 2.5 V		264	360	
			2.5 V ≤ V_{OUT} < 3.3 V		193	270	
			3.3 V ≤ V_{OUT} ≤ 5.5 V		161	225	
PSRR	Power-supply rejection ratio	V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 50 mA	f = 1 kHz		50		dB
			f = 100 kHz		45		
			f = 1 MHz		30		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 0.9 V			53		$µV_{RMS}$
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.21	1.33	1.47	V
		V_{IN} falling		1.17	1.29	1.42	
$V_{UVLO, HYST}$	Undervoltage lockout hysteresis	V_{IN} hysteresis			40		mV
t_{STR}	Startup time	From EN low-to-high transition to V_{OUT} = $V_{OUT(NOM)}$ x 95%			500		µs
$V_{EN(HI)}$	EN pin high voltage			1.0			V
$V_{EN(LO)}$	EN pin low voltage					0.3	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 6.0 V			10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 6.0 V			95		Ω
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			170		°C
		Reset, temperature decreasing			155		

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6.6 Typical Characteristics

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

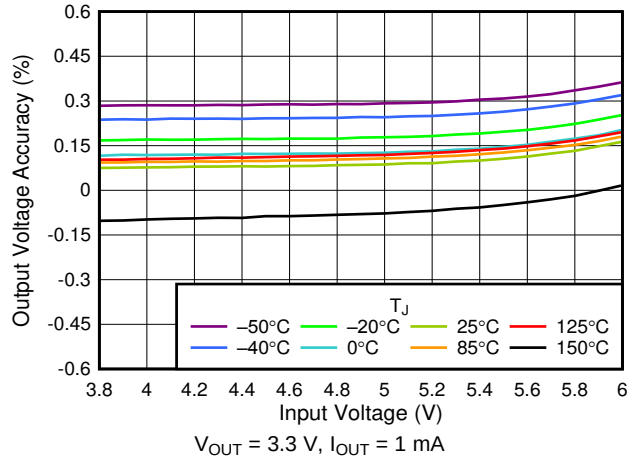


図 1. 3.3-V Line Regulation vs V_{IN}

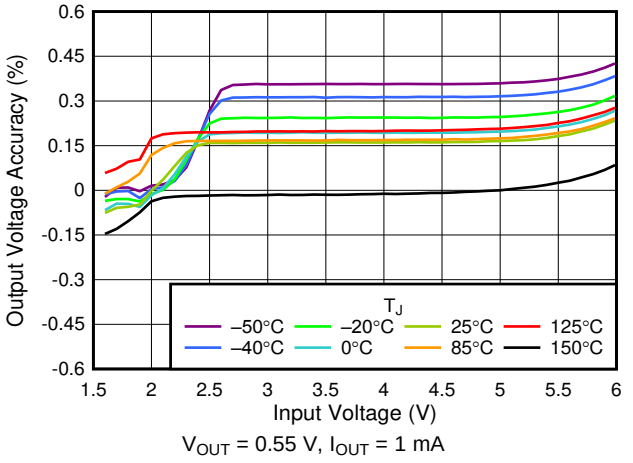


図 2. 0.55-V Line Regulation vs V_{IN}

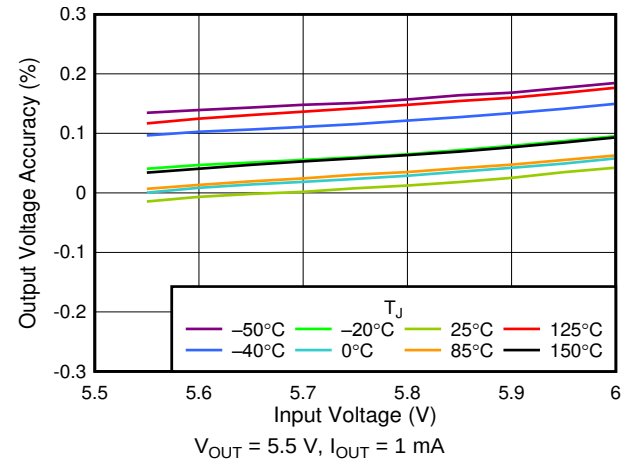


図 3. 5.5-V Line Regulation vs V_{IN}

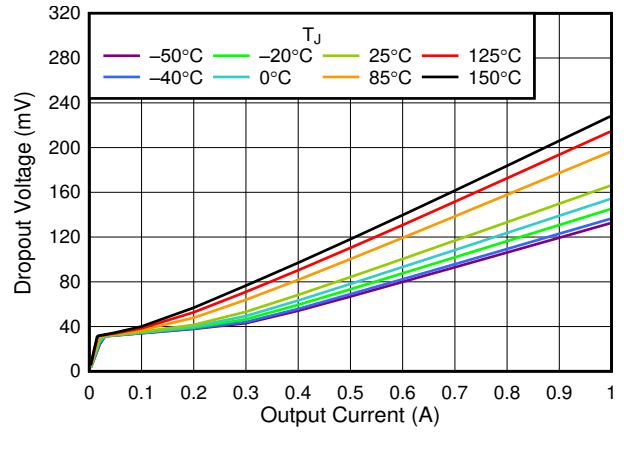


図 4. 3.3-V Dropout Voltage vs I_{OUT}

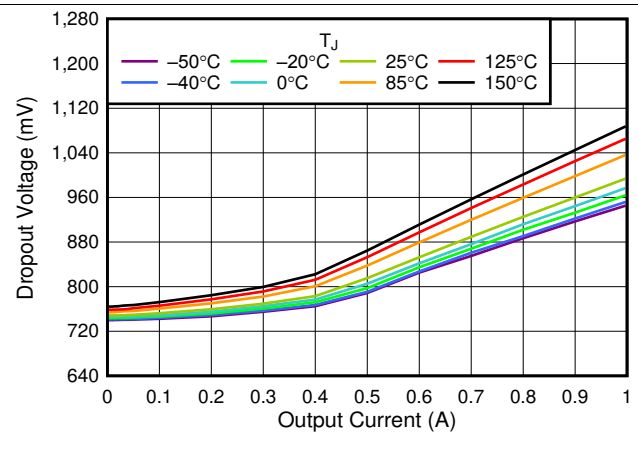


図 5. 0.55-V Dropout Voltage vs I_{OUT}

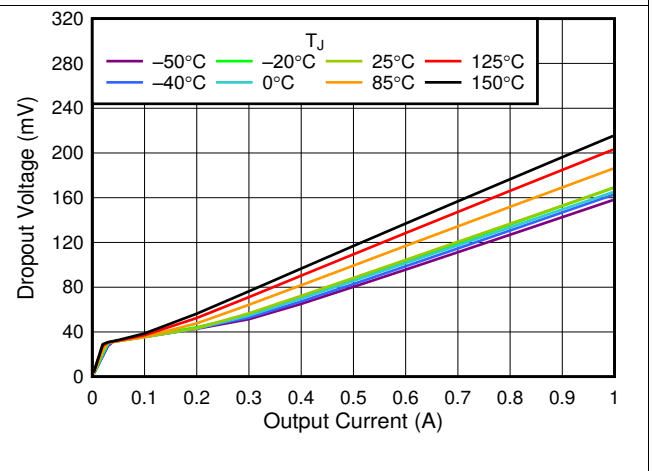


図 6. 5.5-V Dropout Voltage vs I_{OUT}

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Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

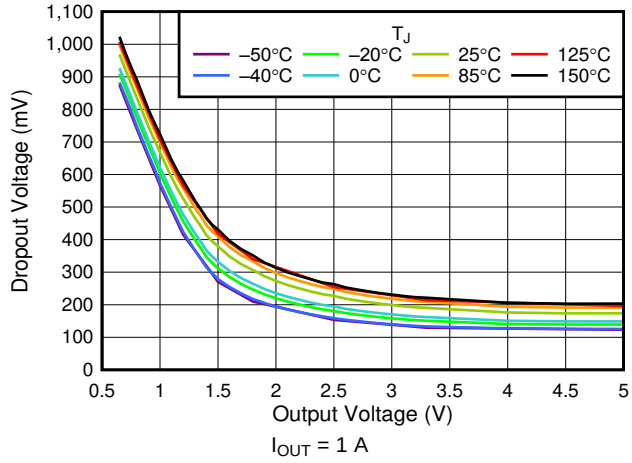


図 7. V_{DO} vs V_{OUT}

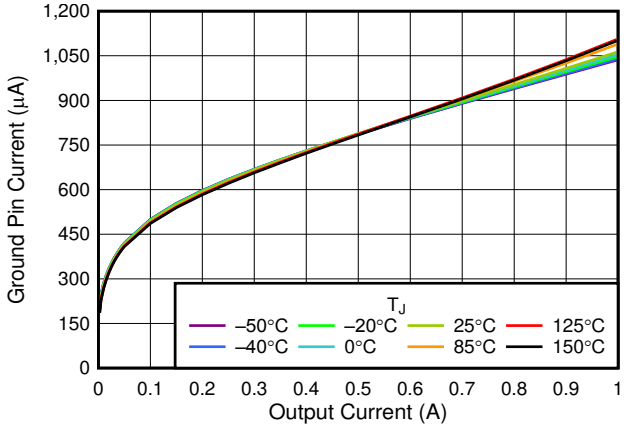


図 8. I_{GND} vs I_{OUT}

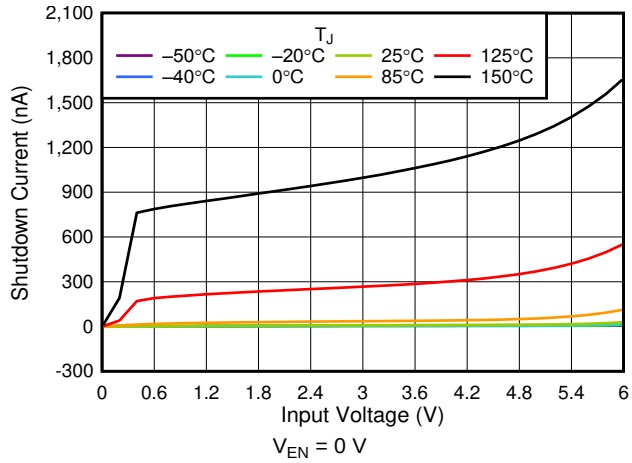


図 9. I_{SHDN} vs V_{IN}

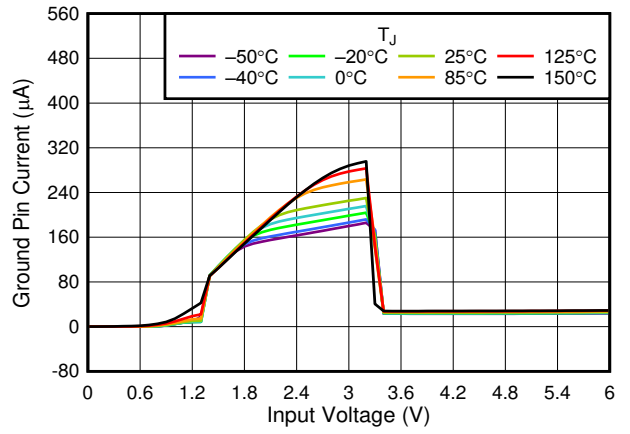


図 10. I_Q vs V_{IN}

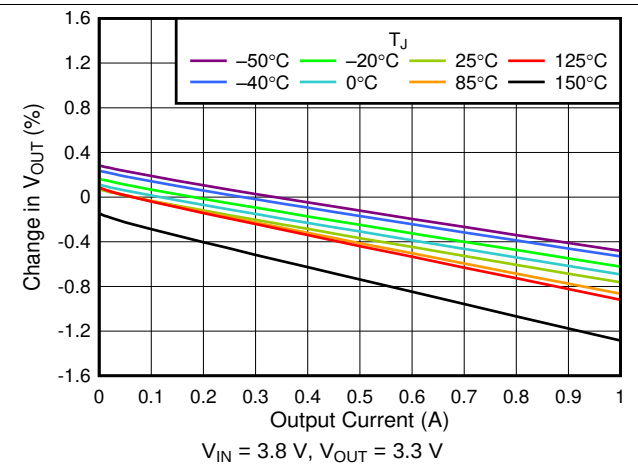


図 11. 3.3-V Load Regulation vs I_{OUT}

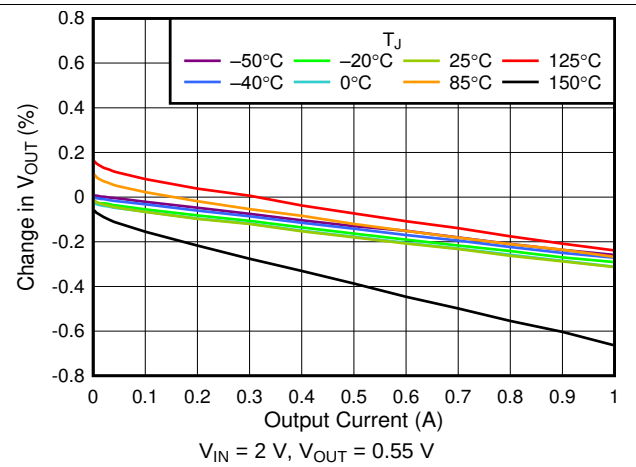


図 12. 0.55-V Load Regulation vs I_{OUT}

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Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

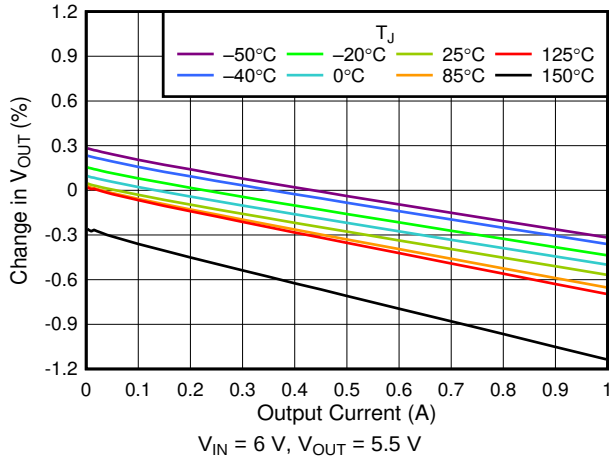


図 13. 5-V Load Regulation vs I_{OUT}

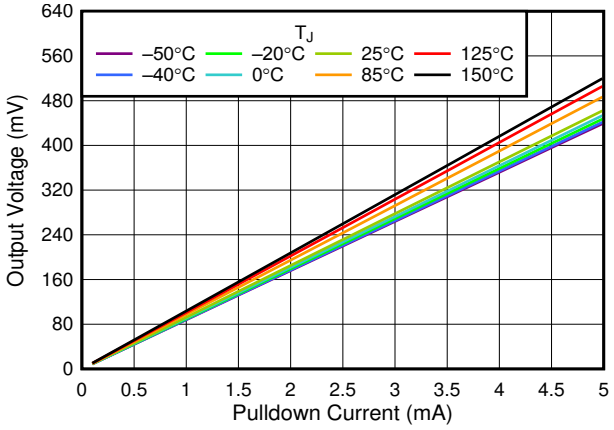


図 14. V_{OUT} vs I_{OUT} Pulldown Resistor

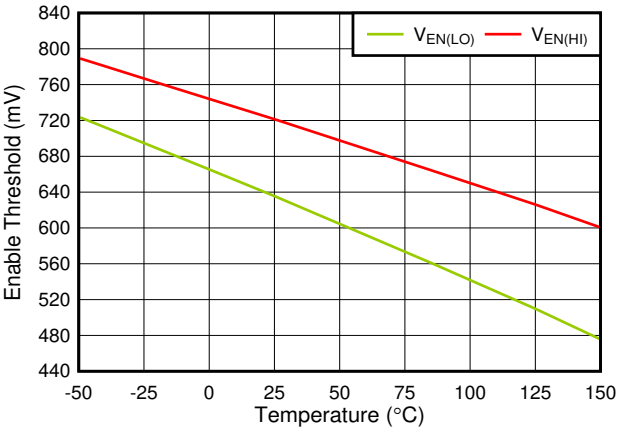


図 15. $V_{EN(HI)}$ and $V_{EN(LO)}$ vs Temperature

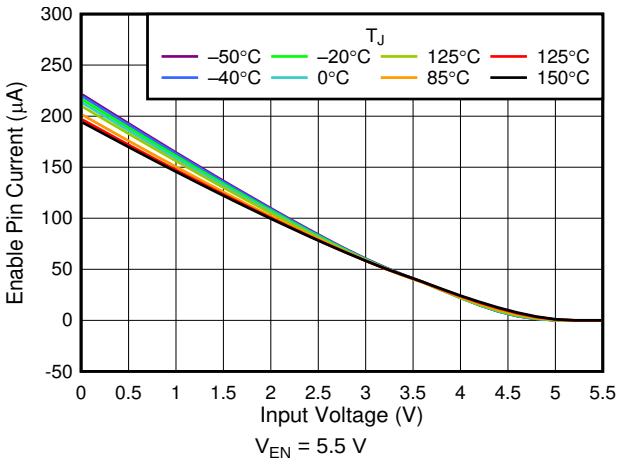


図 16. I_{EN} vs V_{IN}

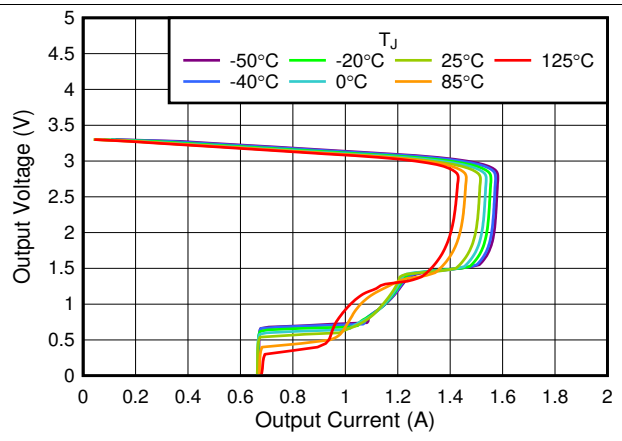


図 17. 3.3-V Foldback Current Limit vs I_{OUT}

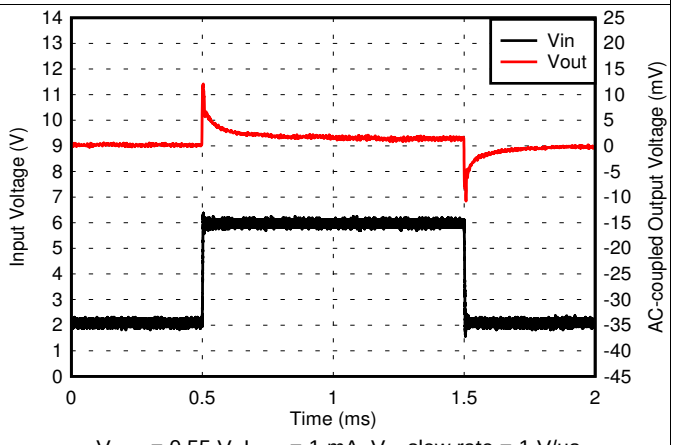
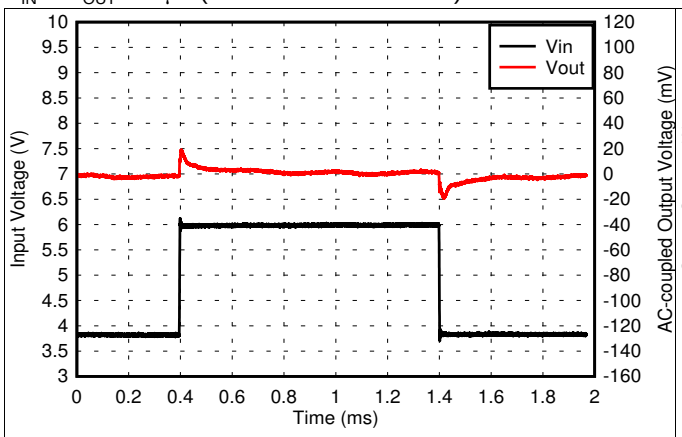


図 18. 0.55-V Line Transient

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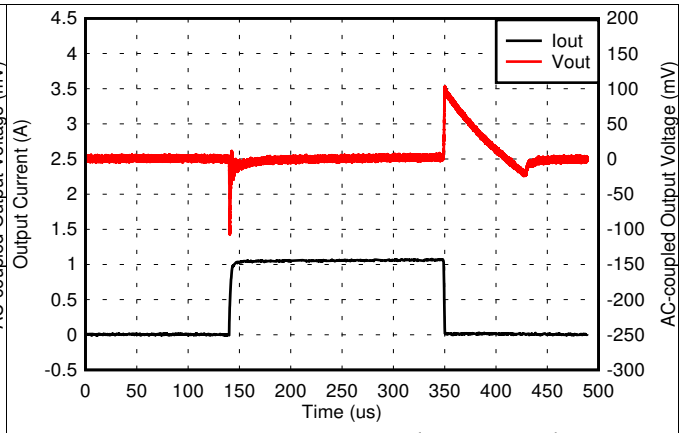
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



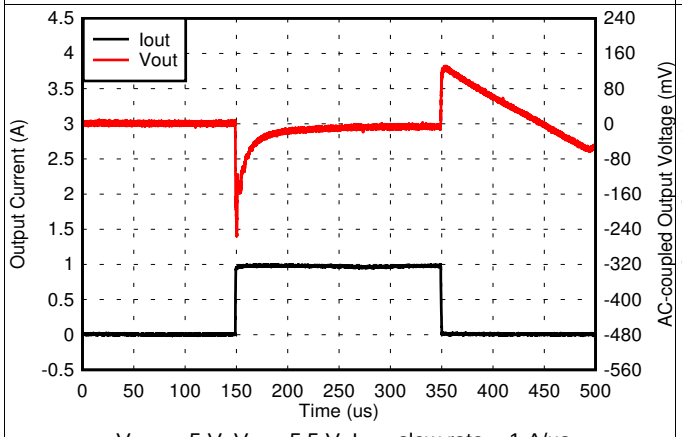
V_{OUT} = 3.3 V, I_{OUT} = 1 mA, V_{IN} slew rate = 1 V/µs

図 19. 3.3-V Line Transient



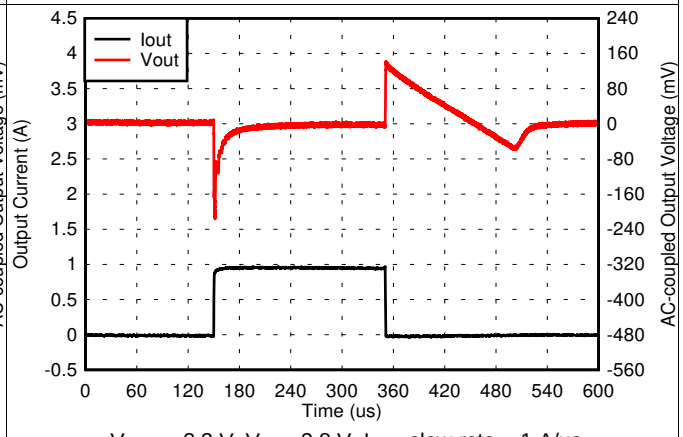
V_{OUT} = 0.55 V, V_{IN} = 2 V, I_{OUT} slew rate = 1 A/µs

図 20. 1-mA to 1-A Load Transient (0.55 V)



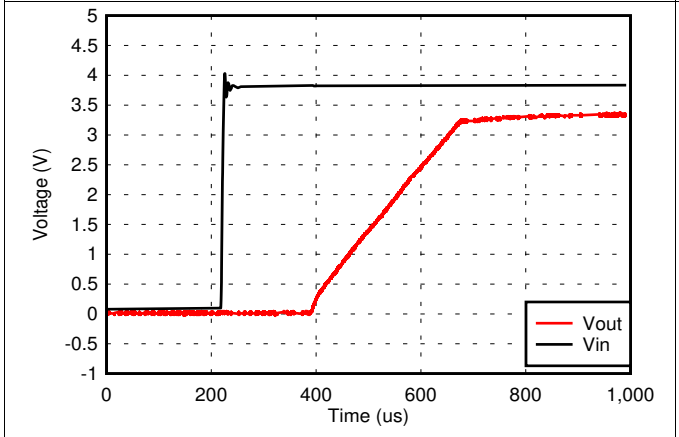
V_{OUT} = 5 V, V_{IN} = 5.5 V, I_{OUT} slew rate = 1 A/µs

図 21. 1-mA to 1-A Load Transient (5 V)



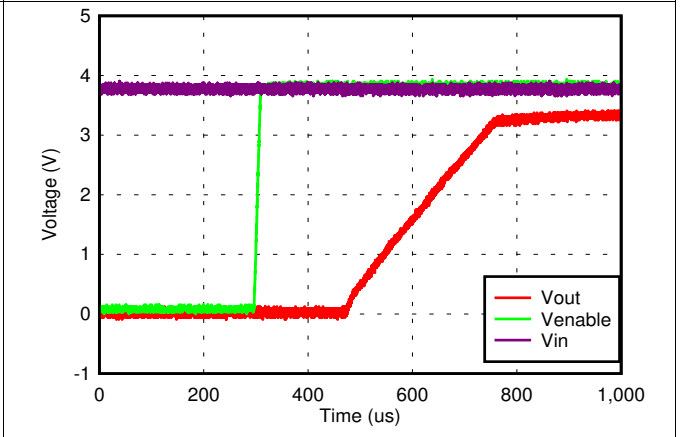
V_{OUT} = 3.3 V, V_{IN} = 3.8 V, I_{OUT} slew rate = 1 A/µs

図 22. 1-mA to 1-A Load Transient (3.3 V)



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA

図 23. V_{IN} Power-Up



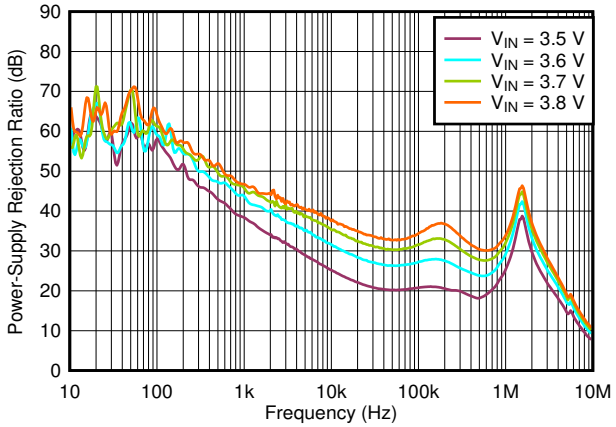
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA

図 24. Startup With EN

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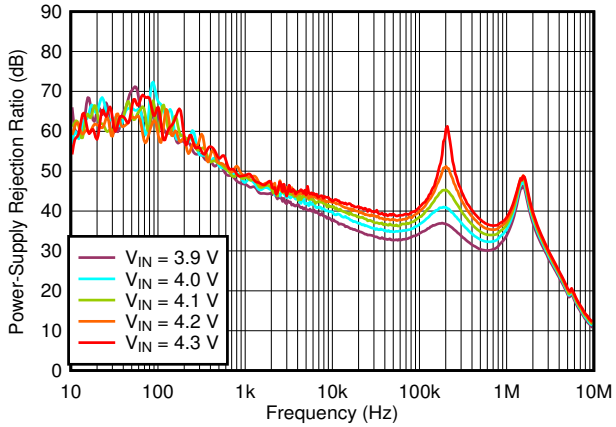
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



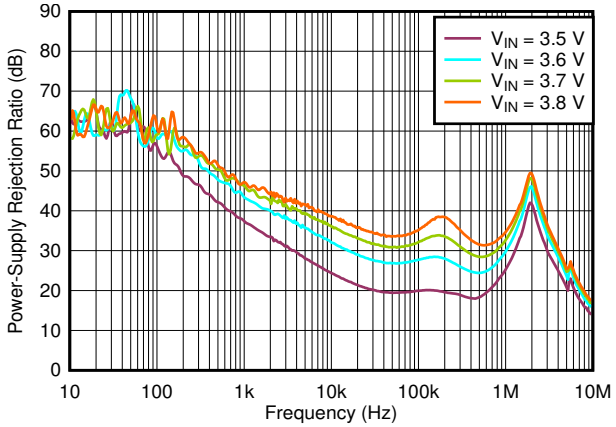
V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

図 25. PSRR vs Frequency and V_{IN}



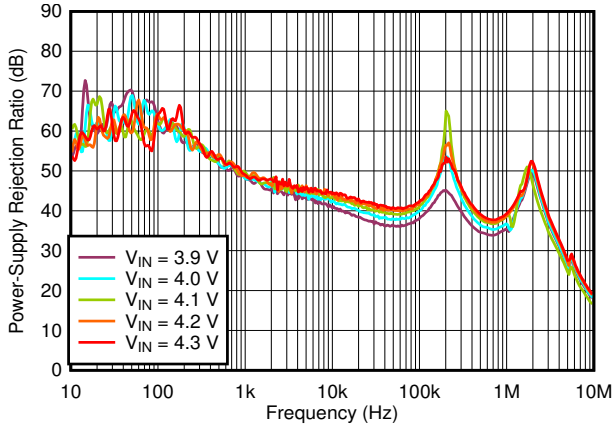
V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

図 26. PSRR vs Frequency and V_{IN}



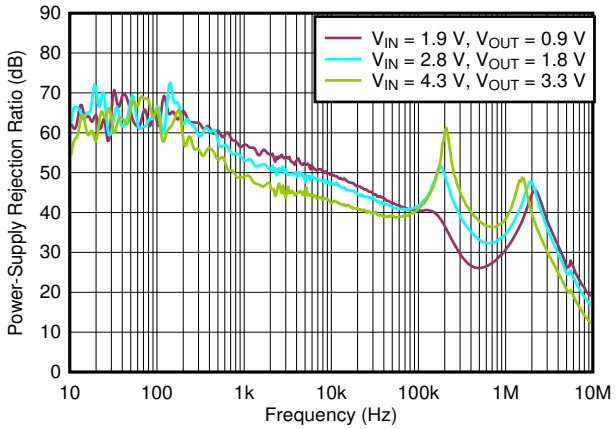
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 2.2 µF

図 27. PSRR vs Frequency and V_{IN}



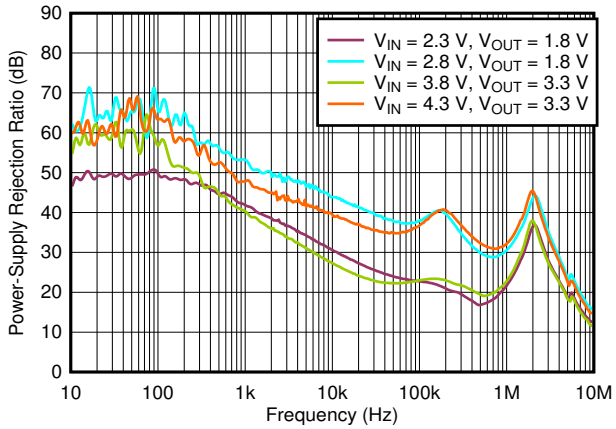
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, C_{OUT} = 2.2 µF

図 28. PSRR vs Frequency and V_{IN}



I_{OUT} = 500 mA, C_{OUT} = 2.2 µF

図 29. PSRR vs Frequency



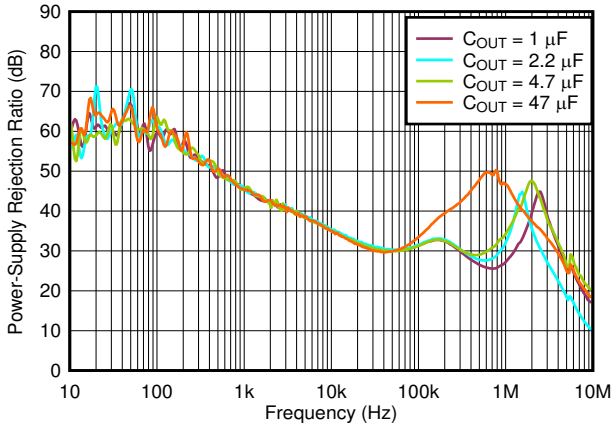
I_{OUT} = 1 A, C_{OUT} = 2.2 µF

図 30. PSRR vs Frequency

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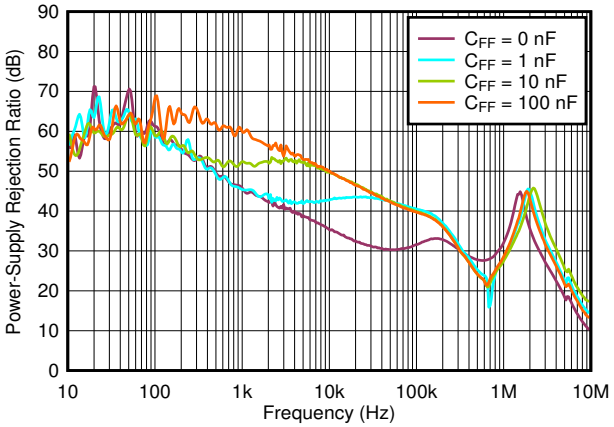
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



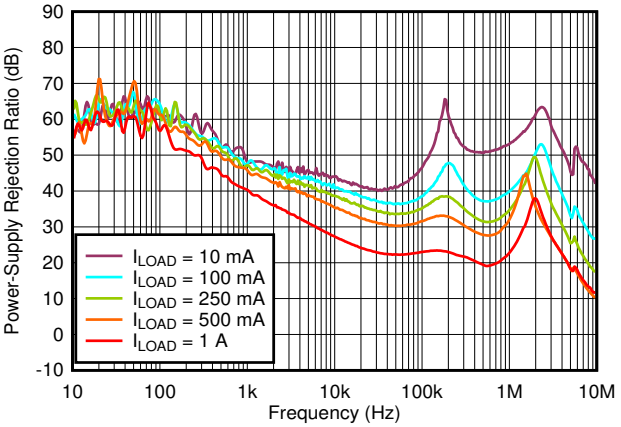
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

図 31. PSRR vs Frequency and C_{OUT}



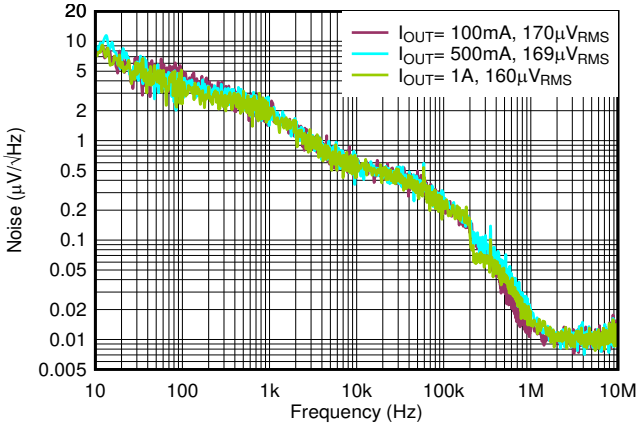
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

図 32. PSRR vs Frequency and C_{FF}



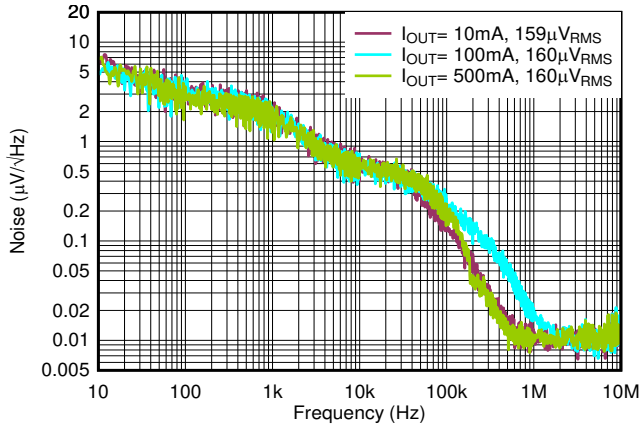
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

図 33. PSRR vs Frequency and I_{LOAD}



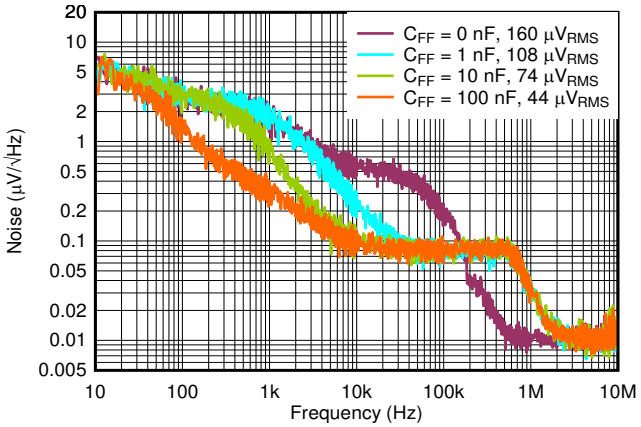
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 4.7 µF,
V_{RMS} BW = 10 Hz to 100 kHz

図 34. Output Spectral Noise Density



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF,
V_{RMS} BW = 10 Hz to 100 kHz

図 35. Output Spectral Noise Density

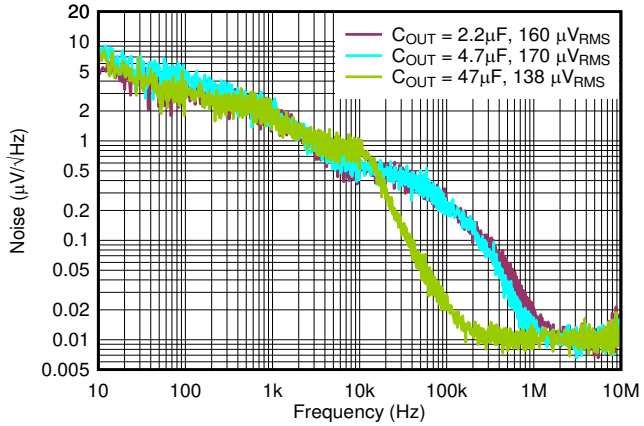


V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 2.2 µF,
V_{RMS} BW = 10 Hz to 100 kHz

図 36. Output Spectral Noise Density vs Frequency and C_{FF}

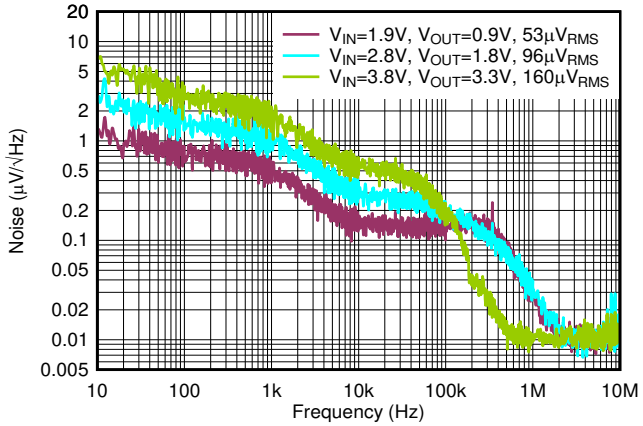
Typical Characteristics (continued)

at operating temperature range T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA, C_{FF} = 0 µF, V_{RMS} BW = 10 Hz to 100 kHz

図 37. Output Spectral Noise Density vs Frequency and C_{OUT}



I_{OUT} = 500 mA, C_{OUT} = 2.2 µF, V_{RMS} BW = 10 Hz to 100 kHz

図 38. Output Spectral Noise Density vs Frequency

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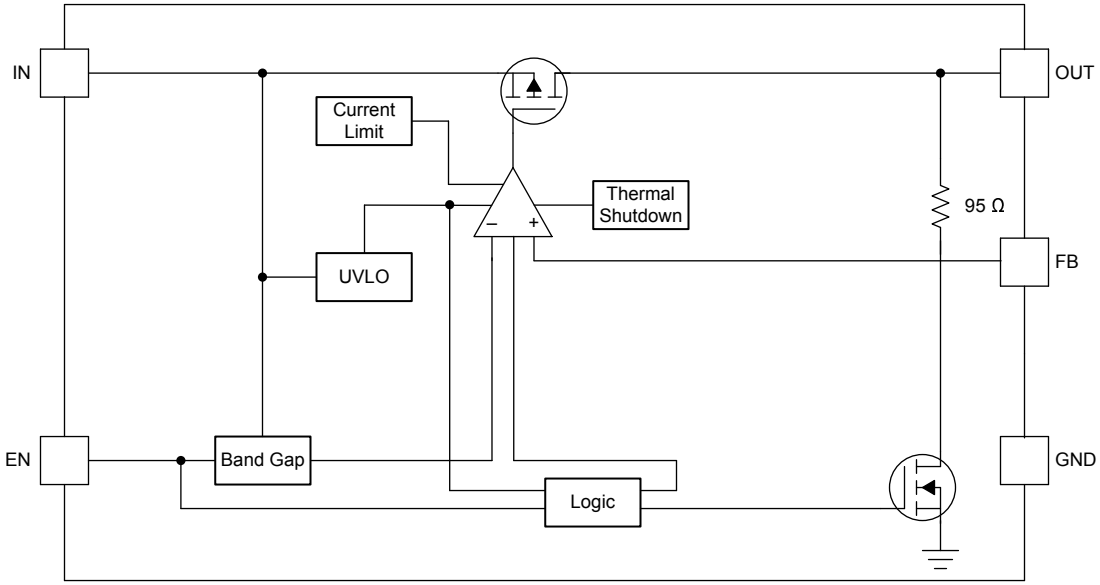
7 Detailed Description

7.1 Overview

The TLV759P is a next-generation, low-dropout regulator (LDO). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device ideal for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV759P uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a pulldown resistor ($R_{PULLDOWN}$).

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$. Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN.

The TLV759P has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor ($R_{PULLDOWN}$). 式 1 calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$

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Feature Description (continued)

7.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.4 V × $V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 39 shows a diagram of the foldback current limit.

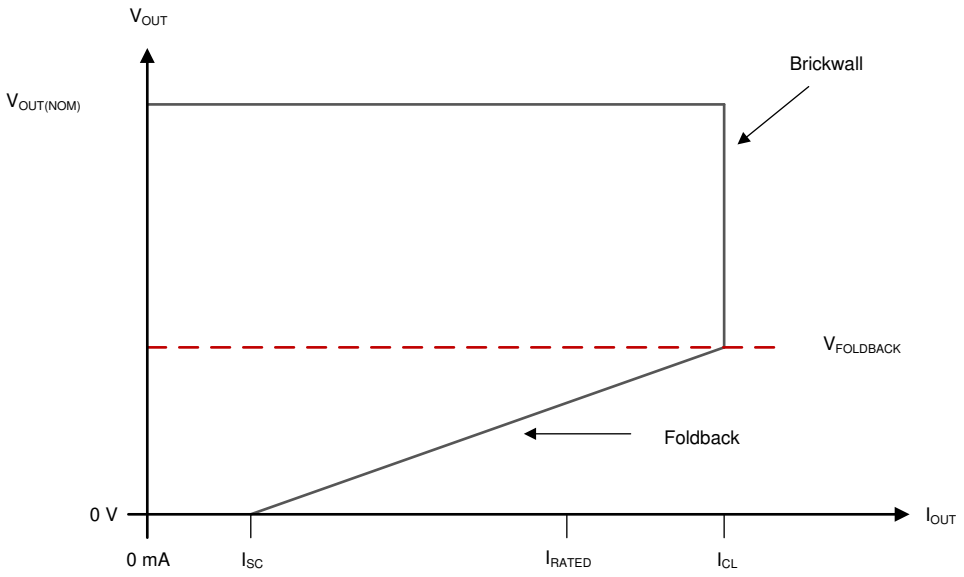


Figure 39. Foldback Current Limit

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

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Feature Description (continued)

The TLV759P internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TLV759P into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

図 40 shows that the output voltage of the TLV759P can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

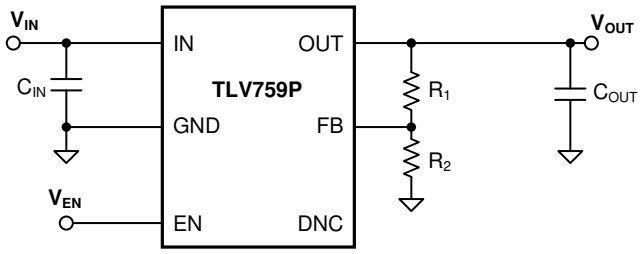


図 40. Adjustable Operation

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

For this device, V_{FB} = 0.55 V.

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

For this device, I_{FB} = 10 nA.

8.1.2 Input and Output Capacitor Selection

The TLV759P requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

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Application Information (continued)

8.1.3 Dropout Voltage

The TLV759P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in 図 41, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

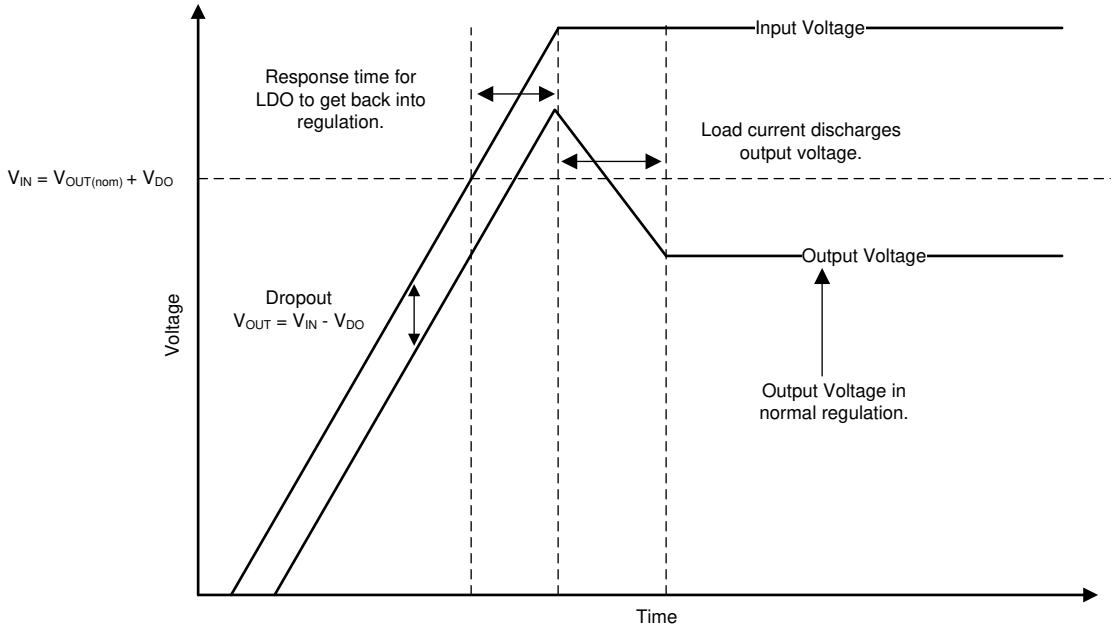


図 41. Startup Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 図 42 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

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Application Information (continued)

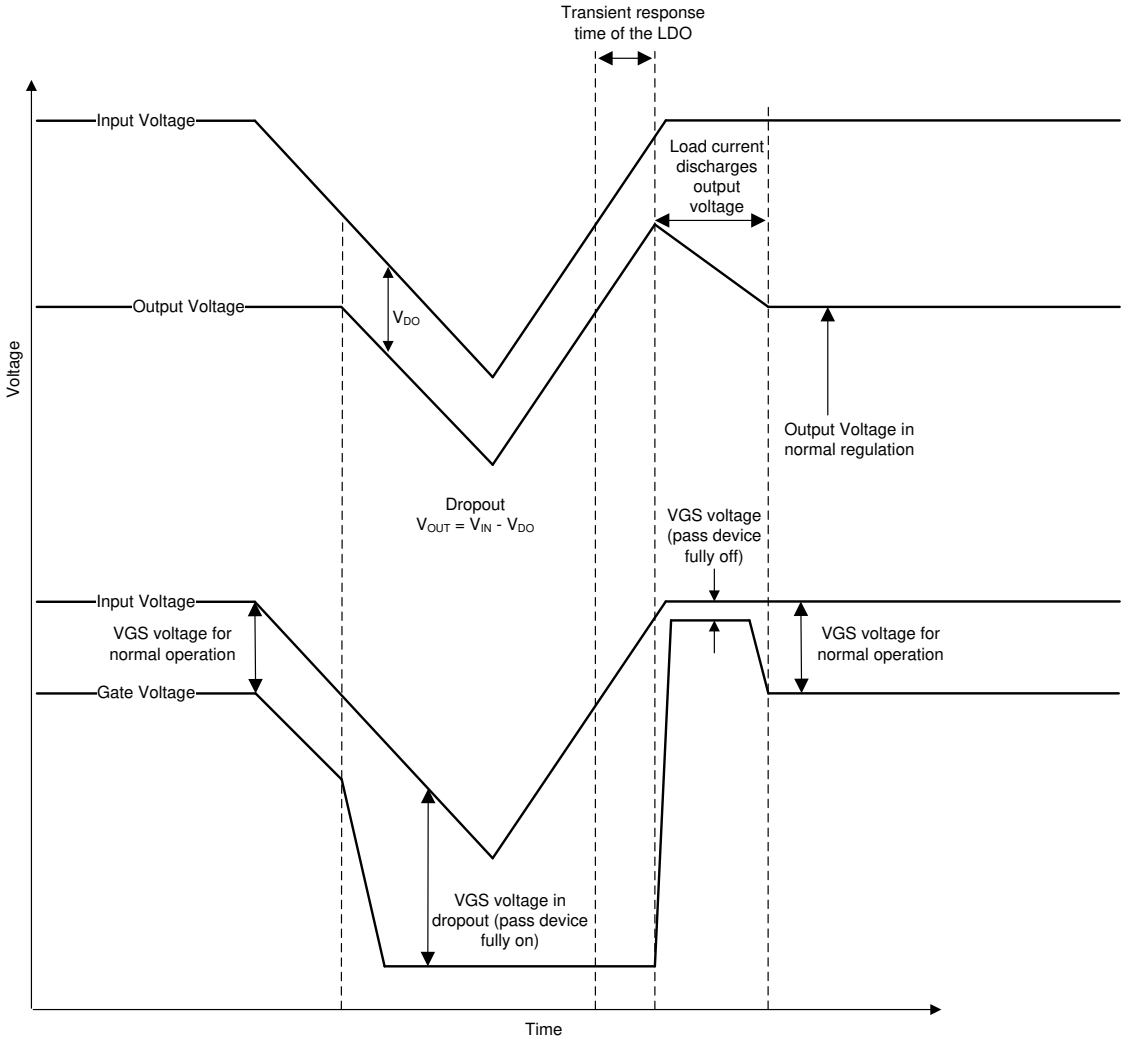


図 42. Line Transients From Dropout

8.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

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Application Information (continued)

If reverse current flow is expected in the application, external protection must be used to protect the device. 図 43 shows one approach of protecting the device.

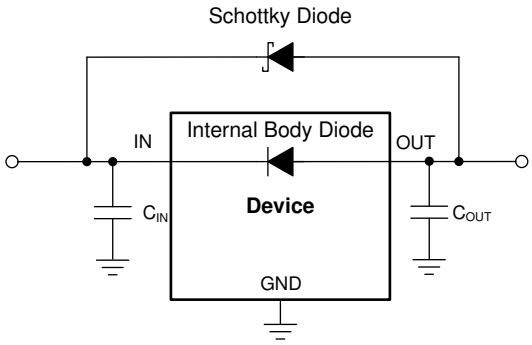


図 43. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (4)$$

NOTE

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.2 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

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8.3 Typical Application

図 44 shows the typical application circuit for the TLV759P. Input and output capacitances must be at least 1 µF.

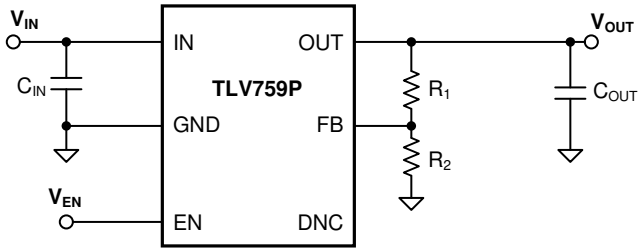


図 44. TLV759P Typical Application

8.3.1 Design Requirements

Use the parameters listed in 表 2 for typical linear regulator applications.

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	3.3 V, ±1%
Input current	1 A (maximum)
Output load	1-A DC
Maximum ambient temperature	70°C

8.3.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

図 40 illustrates the output voltage of the TLV759P. Set the output voltage using the resistor divider; see the section for details.

8.3.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use 式 6 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (6)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

8.3.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 式 7 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ as 式 8 shows and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (7)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (8)$$

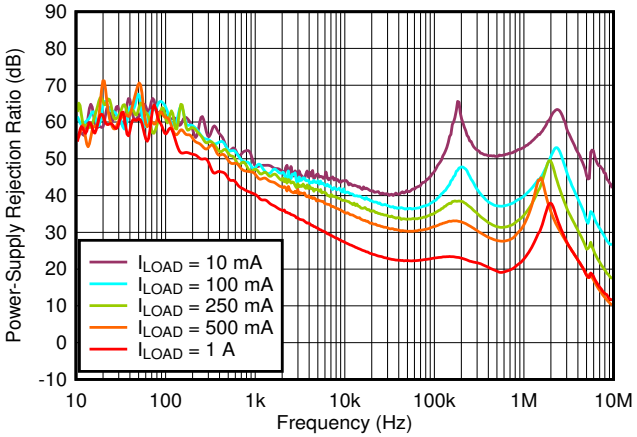
Calculate the maximum ambient temperature as 式 9 shows if the ($T_{J(MAX)}$) value does not exceed 125°C. 式 10 calculates the maximum ambient temperature with a value of 84.85°C.

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$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (9)$$

$$T_{A(MAX)} = 125°C - 80.3°C/W \times (3.8\ V - 3.3\ V) \times (1\ A) = 84.85°C \quad (10)$$

8.3.3 Application Curve



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF

図 45. PSRR vs Frequency and I_{LOAD}

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV759P.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Example

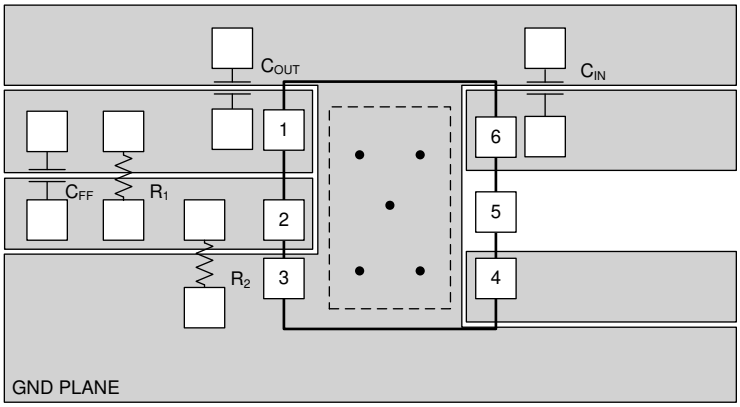


図 46. Layout Example for the DRV Package

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『低ドロップアウト・レギュレータでフィードフォワード・コンデンサを使用することの長所と短所』アプリケーション・レポート

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV75901PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MGH
TLV75901PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MGH
TLV75901PDRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MGH
TLV75901PDRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MGH
TLV75901PDRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MGH
TLV75901PDRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MGH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

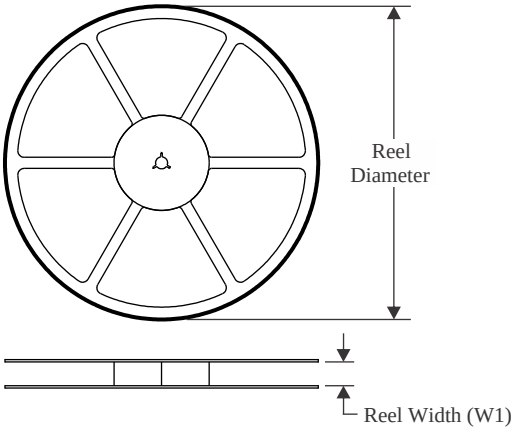
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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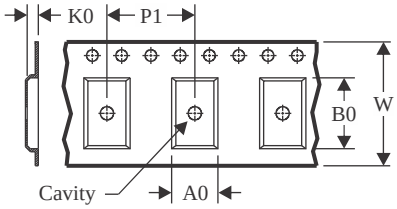
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

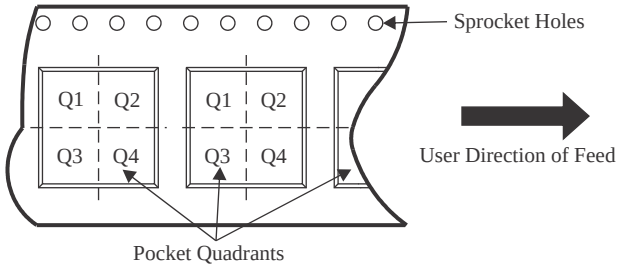


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

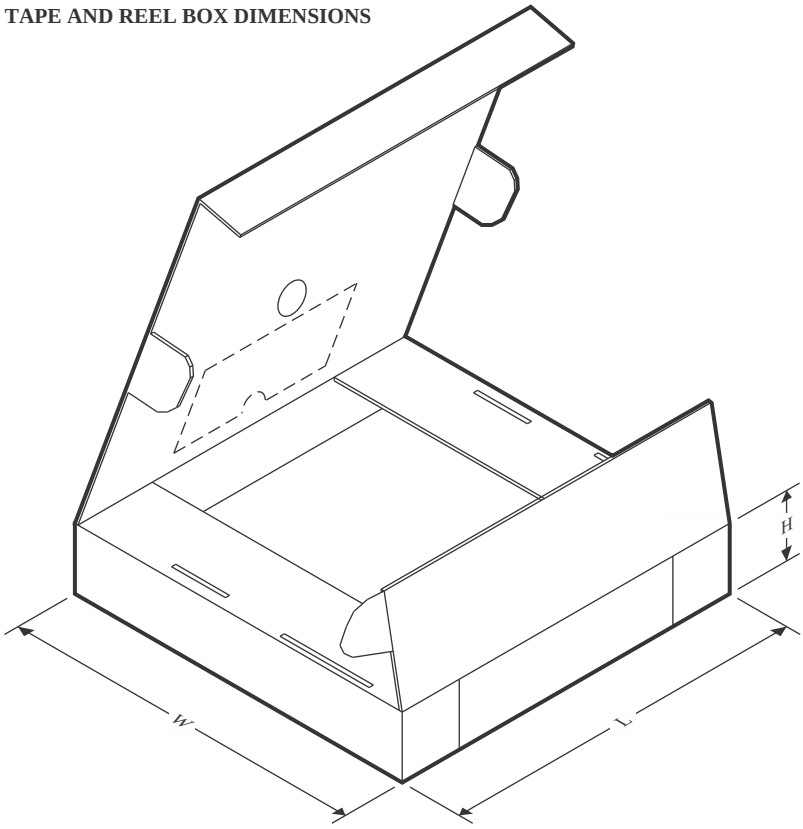
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75901PDRVR	WSON	DRV	6	3000	178.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75901PDRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75901PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

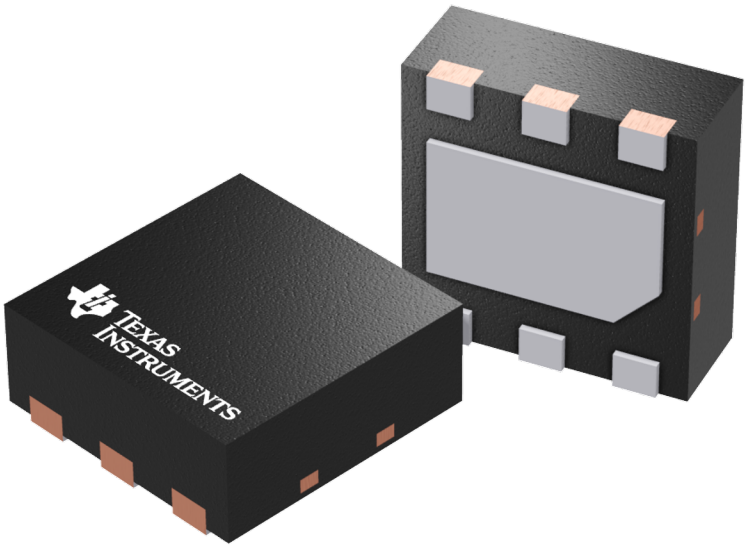


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75901PDRVR	WSON	DRV	6	3000	208.0	191.0	35.0
TLV75901PDRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75901PDRVT	WSON	DRV	6	250	210.0	185.0	35.0

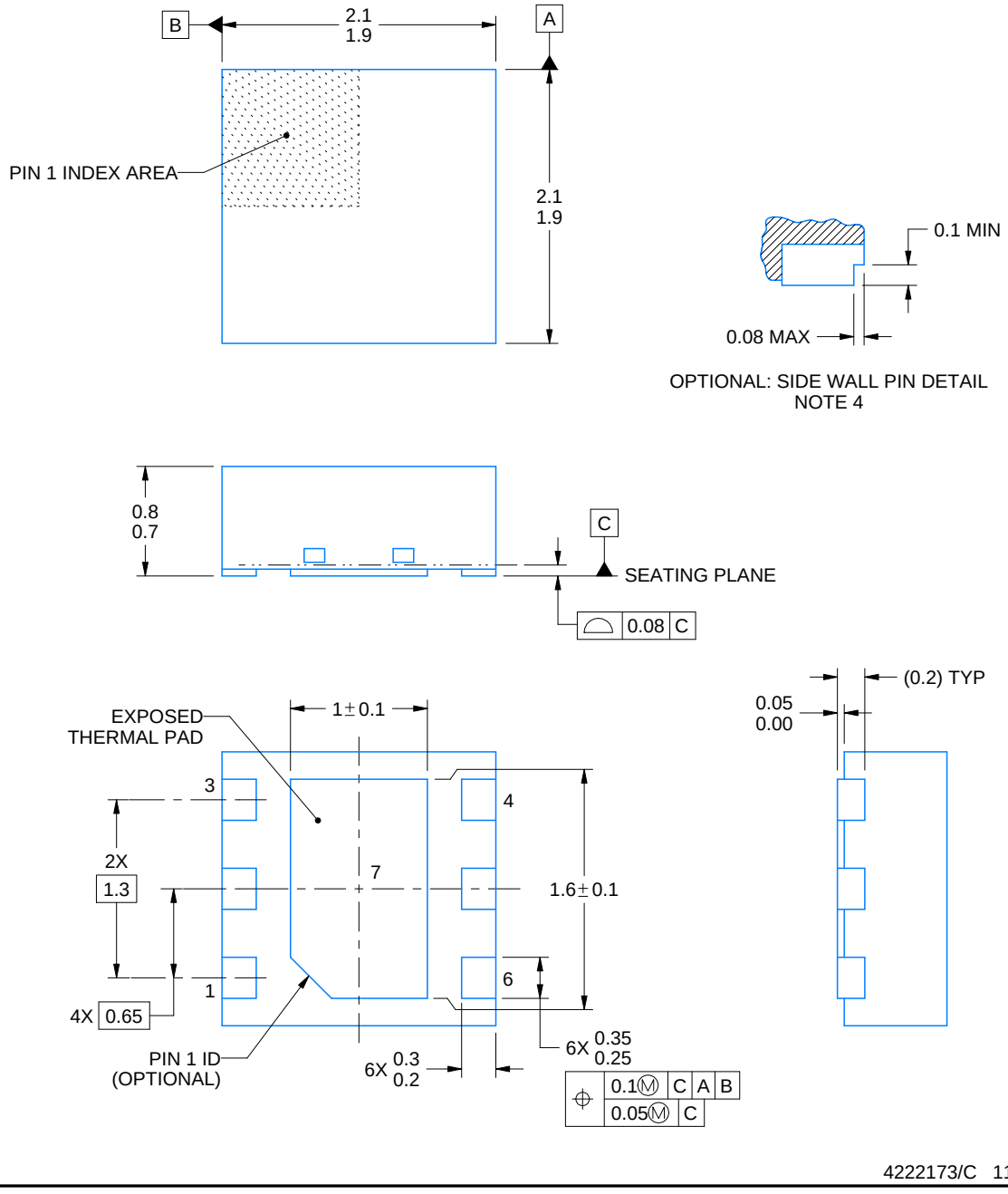
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



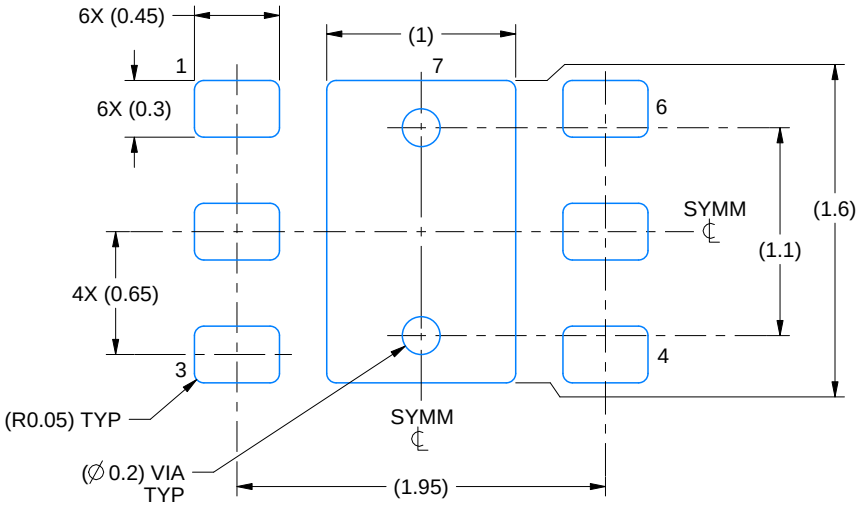
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

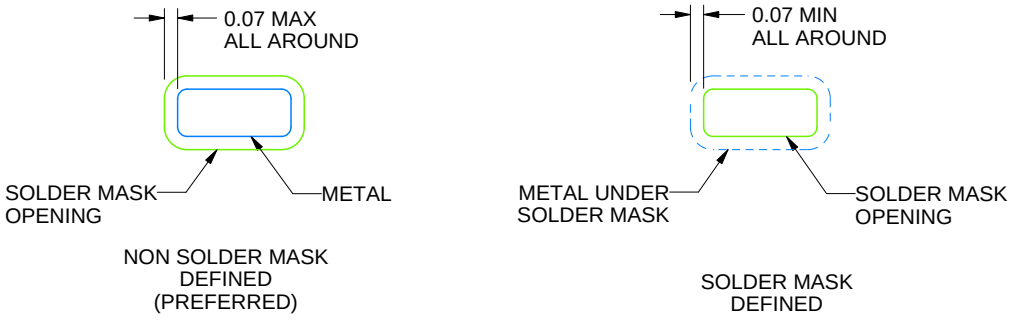


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

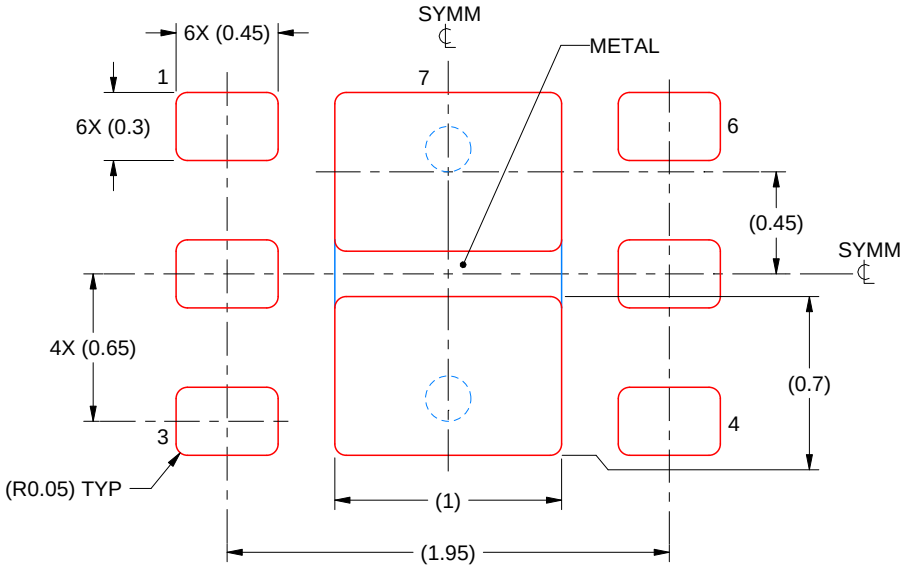


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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