TEXAS INSTRUMENTS
TMAG5170D-Q1
JAJSOV9A – MARCH 2023 – REVISED DECEMBER 2023

TMAG5170D-Q1 デュアル・ダイ高精度 3D リニア・ホール・エフェクト・センサ、SPI 付き

1 特長

- 3D ホール効果センサの性能:
  - 感度ミスマッチの温度ドリフト X-Y 軸:±2.3% (最大値)
  - X-Y 角度の熱ドリフト:±1.2° (最大値)
  - 1 軸で 20kSPS の変換レート
- 垂直方向に位置合わせされたセンシング素子を搭載した、完全絶縁型のデュアル ダイ
- 機能安全準拠:
  - 機能安全アプリケーション向けに開発
  - 機能安全マニュアルに従って適切なシステム レベル制御を実装した場合、ASIL D 要件を満たすように設計
- 車載アプリケーション用に AEC-Q100 認定取得済み:
  - 温度グレード 0:-40℃～150℃
- 構成可能 10MHz のシリアル ペリフェラル インターフェイス (SPI)、巡回冗長性検査 (CRC) 機能付き
- 温度センサと複数の磁石タイプに対応する補償機能を内蔵
- X、Y、Z の磁気範囲を個別に選択可能:
  - TMAG5170DA1-Q1:±25、±50、±100mT
  - TMAG5170DA2-Q1:±75、±150、±300mT
- スレッショルド検出のために 1.5µA しか消費しない自律的なウェークアップおよびスリープ モード
- 最大 32 倍のセンサ データ統合を実現する内蔵デジタル フィルタ
- $\overline{\text{ALERT}}$、$\overline{\text{CS}}$、または SPI 通信を使用した変換トリガ
- 電源電圧範囲:2.3V～5.5V

2 アプリケーション

- 電動パワー ステアリング
- シフタ システム
- ステアリング コラム制御
- ブレーキ システム
- ワイパー モジュール
- アクチュエータ

3 概要

TMAG5170D-Q1 は、高精度シグナル チェーンを備えた完全冗長、電気的に絶縁されたデュアル ダイ 3D ホール効果センサです。2 つのダイは垂直に整列されているため、優れたマッチング出力結果が得られ、温度ドリフト補償付きの温度センシングも含めて、各ダイを独立して構成できます。1D リニア、2D 角度、3D ジョイスティック、磁気スレッショルド交差アプリケーションなど、複数の測定タイプがサポートされています。

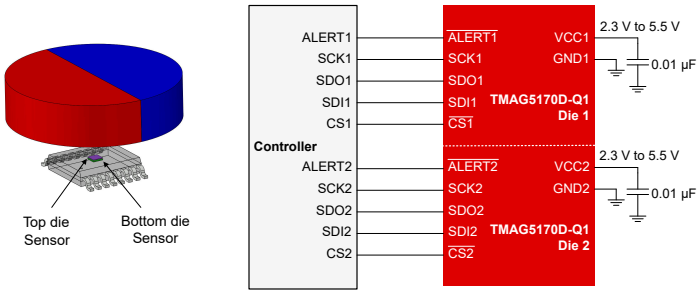
TMAG5170D-Q1 には、内部と外部の両方のフォルト条件の監視など、高信頼性の車載および産業用アプリケーションに必要なオンチップ診断機能が搭載されています。このデバイスは、ウェークアップ モードやスリープ モードなど複数の電力オプションをサポートしているため、設計者はシステム レベルのニーズに基づいてシステムの消費電力を最適化できます。

内蔵の角度計算エンジン (CORDIC) は、磁気ゲインとオフセット補正により、軸上と軸外の両方の角度測定について全 360° の角度位置情報を提供し、システムの機械的誤差発生源の影響を低減します。内蔵の $\overline{\text{ALERT}}$ 機能を使用して、センサ変換、磁気スレッショルド交差、機能安全違反のいずれかを発生させた割り込みを生成できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TMAG5170D-Q1	PW (TSSOP、16)	5.00mm × 6.40mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーションのブロック図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

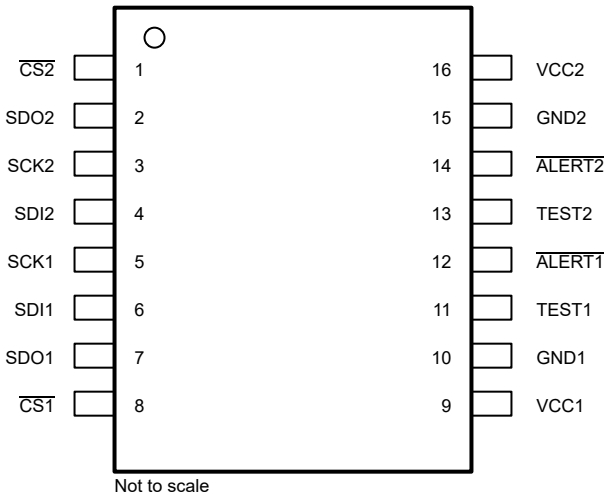


図 4-1. PW Package 16-Pin TSSOP Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	$\overline{CS2}$	I	Chip select, bottom die
2	SDO2	O	Serial data out, bottom die
3	SCK2	I	Serial clock, bottom die
4	SDI2	I	Serial data in, bottom die
5	SCK1	I	Serial clock, top die
6	SDI1	I	Serial data in, top die
7	SDO1	O	Serial data out, top die
8	$\overline{CS1}$	I	Chip select, top die
9	VCC1	P	Main power supply, top die. Handles 2.3-V to 5.5-V power supply input
10	GND1	G	Ground, top die
11	TEST1	I/O	Test input, top die, connect to ground
12	$\overline{ALERT1}$	I/O	Status output/Trigger, top die
13	TEST2	I/O	Test input, bottom die, connect to ground
14	$\overline{ALERT2}$	I/O	Status output/Trigger, bottom die
15	GND2	G	Ground, bottom die
16	VCC2	P	Main power supply, bottom die. Handles 2.3-V to 5.5-V power supply input

(1) I = input, O = output, I/O = input and output, G = ground, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{CC}	Main supply voltage, VCC1, VCC2	–0.3	7	V
I_{OUT}	Output current, SDO1, SDO2, $\overline{\text{ALERT1}}$, $\overline{\text{ALERT2}}$	–10	10	mA
V_{IO}	Pin voltage, SDO1, SDO2, $\overline{\text{ALERT1}}$, $\overline{\text{ALERT2}}$	–0.3	7	V
	Pin voltage, SDI1, $\overline{\text{CS1}}$, SCK1, SDI2, $\overline{\text{CS2}}$, SCK2	–0.3	V_{CC} + 0.3 or V_{CCIO} + 0.3	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	170	°C
T_{stg}	Storage temperature	–65	170	°C

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 8, 9, and 16)	±750	
			All pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VCC}	Main supply voltage	2.3	5.5	V
I_{OUT}	Output current, SDO1, SDO2	–2	2	mA
	Output current, $\overline{\text{ALERT1}}$, $\overline{\text{ALERT2}}$	0	2	mA
V_{IO}	Pin voltage, SDO1, SDO2, ALERT1, ALERT2	0	5.5	V
	Pin voltage, SDI1, $\overline{\text{CS1}}$, SCK1, SDI2, $\overline{\text{CS2}}$, SCK2	0	V_{CC} + 0.3 or V_{CCIO} + 0.3	V
T_A	Operating free air temperature	-40	150	C

5.4 Thermal Information

THERMAL METRIC[1]		TMAG5170D-Q1 PW (16-TSSOP) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

Over T_A = –40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output						
V_{IH}	Input logic high voltage, SDI1, CS1, SCK1, SDI2, CS2, SCK2		0.75 * V_{CC}			V
V_{IL}	Input logic low voltage, SDI1, CS1, SCK1, ALERT1, SDI2, CS2, SCK2, ALERT2				0.25 * V_{CC}	V
V_{OH}	Output HIGH voltage, SDOx pins	I_{OUT} = 2 mA	V_{CC} –0.4		V_{CC}	V
V_{OL}	Output LOW voltage, SDOx pins	I_{OUT} = -2 mA	0		0.4	V
V_{OL}	Output LOW voltage, $\overline{\text{ALERTx}}$ pins	I_{OUT} = -2 mA	0		0.4	V
$t_{FALL_\overline{ALERT}}$	$\overline{\text{ALERTx}}$ output fall time	R_{PU} = 10 kΩ C_L = 20 pF		50		ns
$t_{\overline{ALERT}}$	$\overline{\text{ALERTx}}$ output pulse width with conversion complete or threshold cross interrupt event	ALERT_MODE = 0h Interrupt & Trigger Mode		5		µs
$t_{\overline{ALERT}}$	$\overline{\text{ALERTx}}$ output pulse width with other interrupt events	ALERT_MODE = 0h Interrupt & Trigger Mode		31		µs
I_{OZ}	Output Leakage current, $\overline{\text{ALERTx}}$ pins	ALERT pin disabled V_{OZ} = 5.5 V	0	30	100	nA
Power Supply						
$V_{CC_PORRise}$	Power on reset voltage at VCCx ramping up		1.15	1.4	1.7	V
$V_{CC_PORFall}$	Power off reset voltage at VCCx ramping down		0.8	1.2	1.6	V
V_{CC_UV}	Under voltage threshold at VCCx		2.0	2.1	2.3	V
V_{CC_OV}	Over voltage threshold at VCCx		5.57	5.9	6.9	V
I_{ACTIVE}	Active mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high		3.4	4.5	mA
I_{STDBY}	Stand-by mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high		0.8	1.2	mA
I_{CFG}	Configuration mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high		0.06	0.15	mA
I_{SLP}	Sleep mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high		1.3	45	µA
I_{DEEP_SLP}	Deep sleep mode current from VCC1 or VCC2	$\overline{\text{CS}}$ high		5	300	nA
I_{CC_DCM}	Duty-cycle mode current consumption for each die One channel enabled CONV_AVG = 0h	Data active rate 1000 Hz		290		µA
		Data active rate 100 Hz		34		µA
		Data active rate 10 Hz		4.5		µA
		Data active rate 1 Hz		2.2		µA
	Duty-cycle mode current consumption for each die Two channels enabled CONV_AVG = 0h	Data active rate 1000 Hz		360		µA
		Data active rate 100 Hz		43		µA
		Data active rate 10 Hz		5		µA
		Data active rate 1 Hz		2.3		µA

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Over T_A = –40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Speed						
$t_{w_trigger}$	Pulse width for conversion trigger input signal			15		µs
$t_{measure}$	Conversion time (1) OPERATING_MODE = 2h One channel enabled	CONV_AVG = 0h(2)		50		µs
		CONV_AVG = 5h(3)		825		µs
f_{HFOSC}	Internal high-frequency oscillator speed		2.95	3.2	3.5	MHz
f_{LFOSC}	Internal low-frequency oscillator speed		13.5	16	19.5	KHz
Temperature Sensing						
T_{SENS_T0}	Reference temperature for $TADC_{T0}$		20.5	25	29.5	℃
$TADC_{T0}$	TEMP_RESULT decimal value @ T_{SENS_T0}			17522		
$TADC_{RES}$	Temp sensing resolution		58.2	60.0	61.8	LSB/℃
NRMS (T)	RMS (1 Sigma) temperature noise	CONV_AVG = 5h		0.06		℃
		CONV_AVG = 0h		0.35		℃
Sensor Location						
d_{s1_s2}	Sensor displacement in the X and Y plane			25	75	µm
A_{s1_s2}	Relative angular rotation between top and bottom sensor in degree			1	3	deg

(1) To calculate the time between conversion request and the availability of the conversion result, add the initialization time to the $t_{measure}$ as explained in Comparing Operating Modes Table. For continuous conversion, the initialization time is applicable only for the first conversion.
(2) Add 25 µs for each additional channel enabled for conversion with CONV_AVG = 0h.
(3) For conversion with CONV_AVG = 5h, each axis data is collected 32 times. If an additional channel is enabled with CONV_AVG = 5h, add 32×25 µs = 80 0µs to the $t_{measure}$ to calculate the conversion time for two axes.

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5.6 Magnetic Characteristics

Over T_A = -40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TMAG5170A1							
B_{RANGE}	Linear magnetic range	x_RANGE(2) = 0h			±50		mT
		x_RANGE(2) = 1h			±25		mT
		x_RANGE(2) = 2h			±100		mT
SENS	Sensitivity	x_RANGE(2) = 0h			654		LSB/mT
		x_RANGE(2) = 1h			1308		LSB/mT
		x_RANGE(2) = 2h			326		LSB/mT
$SENS_{ERR}$	Sensitivity error	X, Y, or Z axis T_A = 25°C	B_{RANGE} = 25 mT, 50 mT		±1.0	±3.9	%
			B_{RANGE} = 100 mT		±1.0	±4.9	%
$SENS_{ERR_DR}$	Sensitivity thermal drift	X, Y, or Z axis B_{RANGE} = 25 mT, 50 mT, 100 mT			±1.0	±3.4	%
$SENS_{LTD}$	Sensitivity Lifetime drift	X, Y, Z axes			±0.5		%
$SENS_{LE}$	Sensitivity Linearity Error	T_A = 25°C	X, Y axes		±0.1		%
			Z axis		±0.05		%
$SENS_{MIS}$	Sensitivity mismatch	T_A = 25°C	X-Y axes		±0.02	±4.5	%
			Y-Z axes		±0.17	±5.4	%
			X-Z axes		±0.15	±4.5	%
$SENS_{MIS_DR}$	Sensitivity mismatch thermal drift	X-Y axes			±0.8	±2.3	%
		Y-Z axes			±0.7	±3.1	%
		X-Z axes			±1.4	±3.1	%
B_{OFFSET}	Magnetic Offset	X, Y, or Z axis B_{RANGE} = 25 mT, 50 mT	T_A = 25°C		±10	±400	µT
		X, Y, or Z axis B_{RANGE} = 100 mT	T_A = 25°C		±150	±600	µT
B_{OFFSET_DR}	Offset thermal drift	X or Y axis			±1.0	±8.1	µT/°C
		Z axis			±0.50	±2.1	µT/°C
B_{OFFSET_LTD}	Offset Lifetime drift				±50		µT
$B_{N,RMS}$	RMS (1 Sigma) magnetic noise	X or Y axis x_RANGE(2) = 0h CONV_AVG = 0h	T_A = 25°C		140	185	µT
			T_A = 125°C		160	217	µT
		X or Y axis x_RANGE(2) = 0h CONV_AVG = 5h	T_A = 25°C		25	45	µT
			T_A = 125°C		30	55	µT
		Z axis Z_RANGE(2) = 0h CONV_AVG = 0h	T_A = 25°C		62	82	µT
			T_A = 125°C		70	90	µT
		Z axis Z_RANGE(2) = 0h CONV_AVG = 5h	T_A = 25°C		11	20	µT
			T_A = 125°C		13	23	µT
ANG_{ERR} (3)	Angle error	X-Y axes	RANGE = 0h, 2h CONV_AVG = 5h T_A = 25°C		±0.5	±1.1	deg
		X-Z, Y-Z axes			±0.5	±1.4	deg
		X-Y axes	RANGE = 0h, 2h CONV_AVG = 5h			±1.5	deg
		X-Z, Y-Z axes				±2.2	deg

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Over T_A = -40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TMAG5170A2							
B_{RANGE}	Linear magnetic range	x_RANGE(2) = 0h			±150		mT
		x_RANGE(2) = 1h			±75		mT
		x_RANGE(2) = 2h			±300		mT
SENS	Sensitivity	X, Y, or Z axis	x_RANGE(2) = 0h		218		LSB/mT
			x_RANGE(2) = 1h		436		LSB/mT
			x_RANGE(2) = 2h		108		LSB/mT
$SENS_{ERR}$	Sensitivity error	X, Y, or Z axis T_A = 25°C	B_{RANGE} = 75 mT, 150 mT		±1.0	±4.5	%
			B_{RANGE} = 300 mT		±0.7	±5.5	%
$SENS_{ERR_DR}$	Sensitivity thermal drift	X, Y, or Z axis	B_{RANGE} = 75 mT, 150 mT		±1.1	±4.2	%
			B_{RANGE} = 300 mT		±1.6	±4.1	%
$SENS_{LE}$	Sensitivity Linearity error	T_A = 25°C	X, Y axes		±0.1		%
			Z axis		±0.1		%
$SENS_{LTD}$	Sensitivity Lifetime drift	X, Y, Z axes			±0.6		%
$SENS_{MIS}$	Sensitivity mismatch	X-Y axes T_A = 25°C	B_{RANGE} = 75 mT, 150 mT		±0.9	±3.6	%
			B_{RANGE} = 300 mT		±1	±6.8	%
		Y-Z axes T_A = 25°C	B_{RANGE} = 75 mT, 150 mT		±1.6	±4.4	%
			B_{RANGE} = 300 mT		±1.4	±7.4	%
		X-Z axes T_A = 25°C	B_{RANGE} = 75 mT, 150 mT		±1.2	±4.0	%
			B_{RANGE} = 300 mT		±1.1	±6.8	%
$SENS_{MIS_DR}$	Sensitivity mismatch thermal drift	X-Y axes	B_{RANGE} = 75 mT, 150 mT		±0.5	±3.0	%
			B_{RANGE} = 300 mT		±0.5	±3.3	%
		Y-Z axes	B_{RANGE} = 75 mT, 150 mT		±0.4	±4.0	%
			B_{RANGE} = 300 mT		±0.2	±4.5	%
		X-Z axes	B_{RANGE} = 75 mT, 150 mT		±0.2	±4.0	%
			B_{RANGE} = 300 mT		±1.1	±4.4	%
B_{OFFSET}	Magnetic offset	T_A = 25°C	B_{RANGE} = 75 mT, 150 mT		±110	±600	µT
	Magnetic offset		B_{RANGE} = 300 mT		±415	±1150	µT
B_{OFFSET_DR}	Offset thermal drift	B_{RANGE} = 75 mt, 150 mT	X or Y axis		±1.0	±7.0	µT/°C
			Z axis		±1.5	±3.1	µT/°C
		B_{RANGE} = 300 mT	X, Y, or Z axis		±2.5	±8.5	µT/°C
B_{OFFSET_LTD}	Offset Lifetime drift				±25		µT

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Over T_A = -40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$B_{N,RMS}$	RMS (1 Sigma) magnetic noise	X or Y axis x_RANGE(2) = 0h CONV_AVG = 0h	T_A = 25°C		160	225	µT
			T_A = 125°C		193	270	µT
		X or Y axis x_RANGE(2) = 0h CONV_AVG = 5h	T_A = 25°C		28	55	µT
			T_A = 125°C		35	60	µT
		Z axis Z_RANGE(2) = 0h CONV_AVG = 0h	T_A = 25°C		75	120	µT
			T_A = 125°C		84	140	µT
		Z axis Z_RANGE(2) = 0h CONV_AVG = 5h	T_A = 25°C		13	26	µT
			T_A = 125°C		15	30	µT
ANG_{ERR} (3)	Angle error	X-Y, Y-Z, X-Z axes	RANGE = 0h or 1h CONV_AVG = 5h T_A = 25°C		±0.5	±1.2	deg
		X-Y axes	RANGE = 0h or 1h CONV_AVG = 5h			±1.65	deg
		Y-Z, X-Z axes				±1.9	deg
TEMPERATURE COMPENSATION							
STC	Temperature compensation (no compensation)	MAG_TEMPCO = 0h			0		%/°C
STC	Temperature compensation (for NdBFe magnet)	MAG_TEMPCO = 1h			0.12		%/°C
STC	Temperature compensation (for SmCo magnet)	MAG_TEMPCO = 2h			0.03		%/°C
STC	Temperature compensation (for Ceramic magnet)	MAG_TEMPCO = 3h			0.2		%/°C

(1) Drift at any temperature can be calculated from drift values at -40°C to 125°C.
(2) x_RANGE denotes the X_RANGE, Y_RANGE, or Z_RANGE register bits
(3) Angle measurement is performed in static condition using arctan of corresponding X, Y, and Z register values with offset and gain corrections. The input fields have peak magnitudes equal to 80% of the magnetic full range.

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5.7 Power up Timing

Over T_A = -40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} = 5.5 V						
$t_{start_power_up}$	Time to start up after V_{VCC} supply voltage crossing V_{VCC_MIN}			246		µs
t_{start_sleep}	Time to activate from sleep mode			40		µs
t_{go_sleep}	Time to go into sleep mode after $\overline{CS}$ goes high			50		µs
$t_{start_deep_sleep}$	Time to start up from deep sleep mode			246		µs
$t_{start_deep_sleep}$	Time to go into deep sleep mode after $\overline{CS}$ goes high			75		µs
t_{stand_by}	Time to go to Stand-by mode from Configuration mode			150		µs
V_{CC} = 2.3 V						
$t_{start_power_up}$	Time to start up after V_{CC} supply voltage crossing V_{CC_MIN}			260		µs
t_{start_sleep}	Time to activate from sleep mode			40		µs
t_{go_sleep}	Time to go into sleep mode after $\overline{CS}$ goes high			60		µs
$t_{start_deep_sleep}$	Time to start up from deep sleep mode			260		µs
$t_{start_deep_sleep}$	Time to go into deep sleep mode after $\overline{CS}$ goes high			75		µs
t_{stand_by}	Time to go to Stand-by mode from Configuration mode			150		µs

5.8 SPI Interface Timing

Over T_A = -40°C to 125°C range and V_{CC} = 2.3 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI Interface						
f_{SPI}	SPI clock (SCK) frequency	C_L = 25 pF V_{CC} = 2.3 V to 3.0 V			8	MHz
f_{SPI}	SPI clock (SCK) frequency	C_L = 25 pF V_{CC} = 3.0 V to 5.5 V			10	MHz
t_{whigh}	High time: SCK logic high time duration		45			ns
t_{wlow}	Low time: SCK logic low time duration		45			ns
t_{su_cs}	$\overline{CS}$ setup time: Time delay between falling edge of $\overline{CS}$ and rising edge of SCK		45			ns
t_{h_cs}	Hold time: Time between the falling edge of SCK and rising edge of $\overline{CS}$		45			ns
t_{pd_soen}	Delay time: Time delay from falling edge of $\overline{CS}$ to data valid at SDO				45	ns
t_{pd_sodis}	Delay time: Time delay from rising edge of $\overline{CS}$ to SDO transition to high-impedance				55	ns
t_{su_si}	SDI setup time: Setup time of SDI before the rising edge of SCK		25			ns
t_{h_si}	Hold time: Time between the rising edge of SCK to SDI valid		25			ns
t_{pd_so}	Propagation delay from falling edge of SCK to SDO				45	ns
t_{w_cs}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high.	C_L = 25 pF	100			ns
$t_{spi_deep_sleep}$	Setup time between $\overline{CS}$ going low and SCK start during deep sleep mode			150	320	µs

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5.9 Typical Characteristics

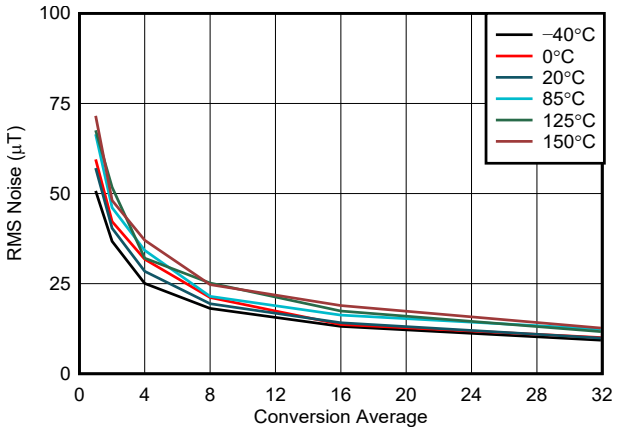


図 5-1. Z-Axis Noise vs Conversion Average, 25-mT Range

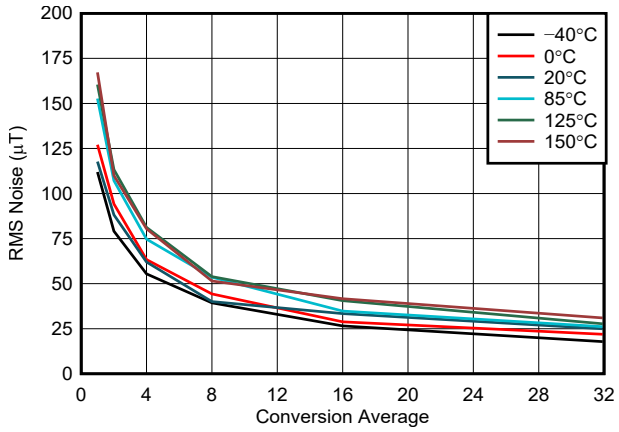


図 5-2. X, Y-Axis Noise vs Conversion Average, 25-mT Range

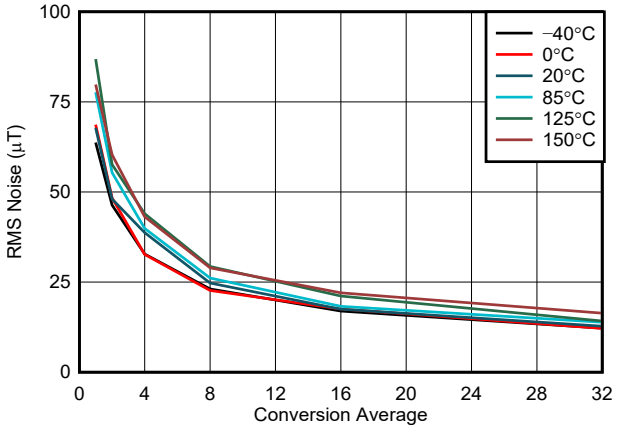


図 5-3. Z-Axis Noise vs Conversion Average, 50-mT Range

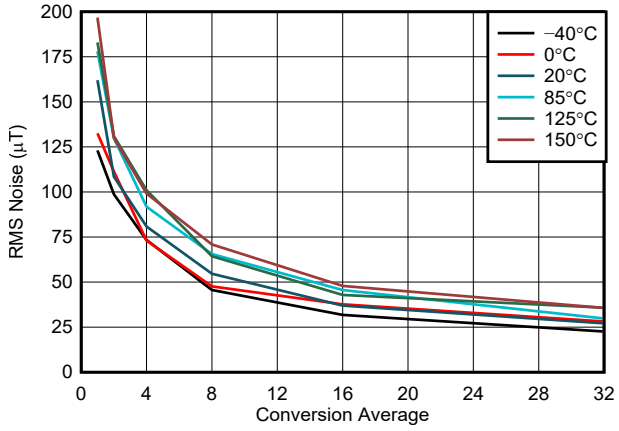


図 5-4. X, Y-Axis Noise vs Conversion Average, 50-mT Range

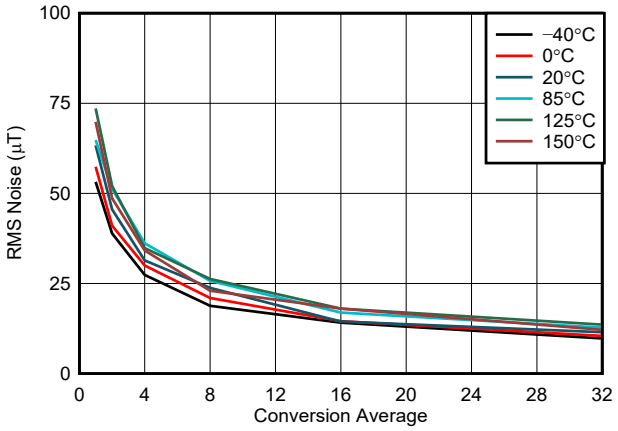


図 5-5. Z-Axis Input vs Conversion Average, 75-mT Range

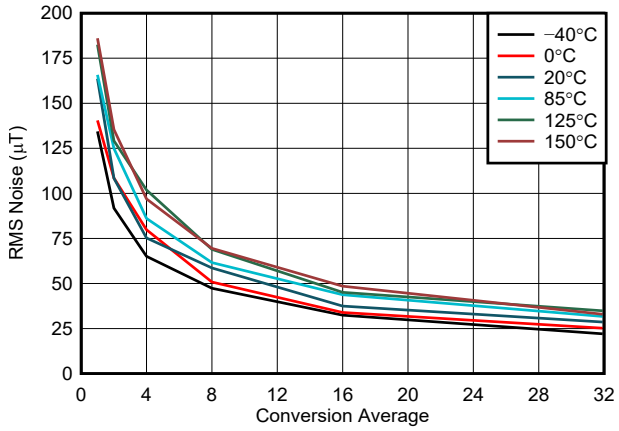


図 5-6. X, Y-Axis Noise vs Conversion Average, 75-mT Range

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5.9 Typical Characteristics (continued)

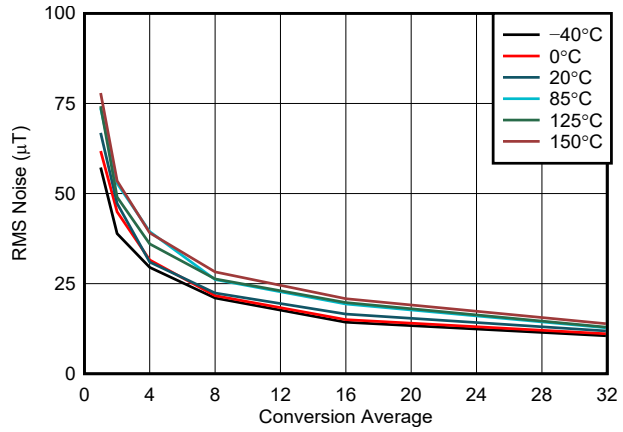


図 5-7. Z-Axis Noise vs Conversion Average, 100-mT Range

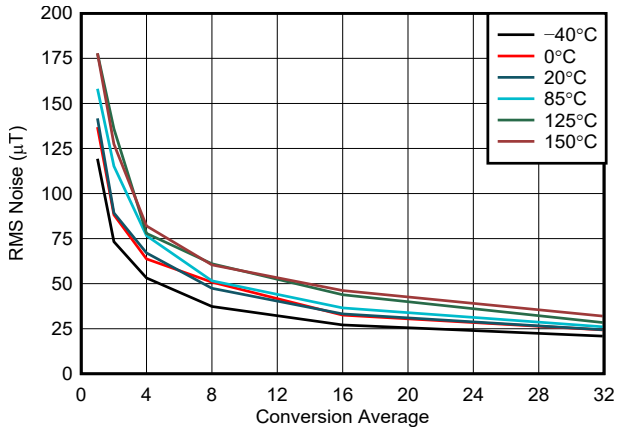


図 5-8. X, Y-Axis Noise vs Conversion Average, 100-mT Range

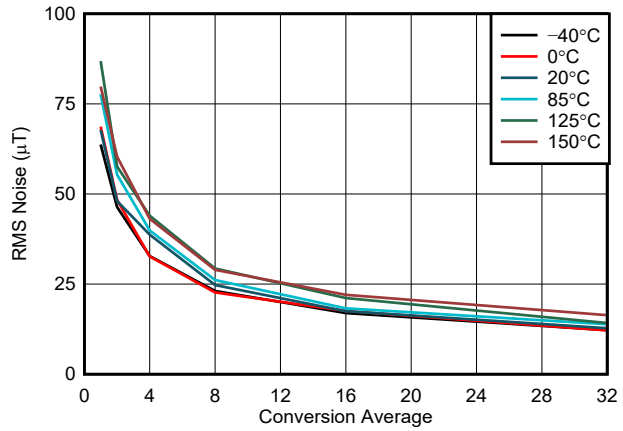


図 5-9. Z-Axis Noise vs Conversion Average, 150-mT Range

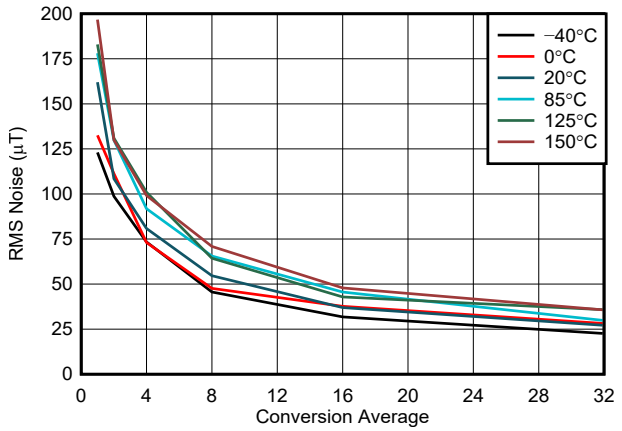


図 5-10. X, Y-Axis Noise vs Conversion Average, 150-mT Range

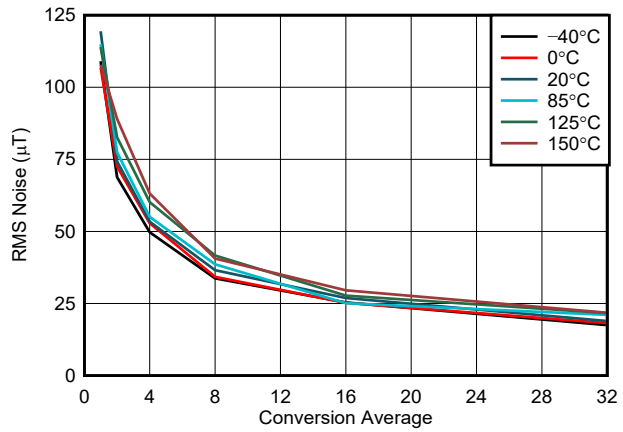


図 5-11. Z-Axis Noise vs Conversion Average, 300-mT Range

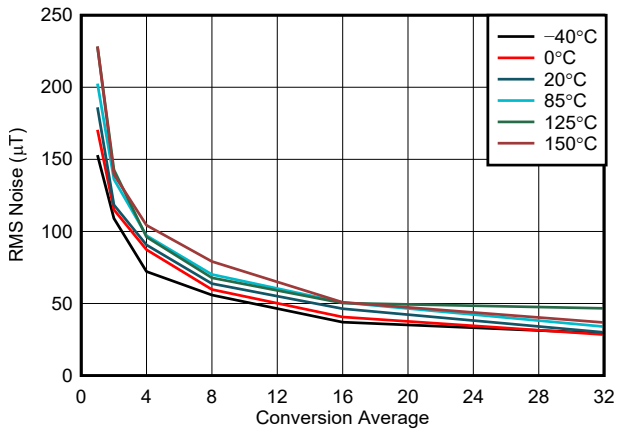


図 5-12. X, Y-Axis Noise vs Conversion Average, 300-mT Range

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5.9 Typical Characteristics (continued)

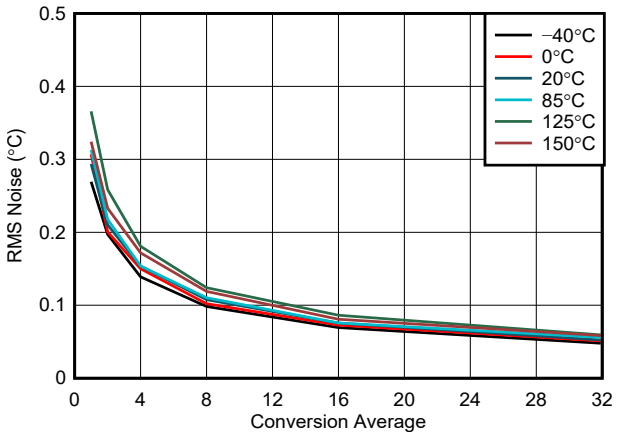


図 5-13. Temperature Sensor Noise vs Conversion Average

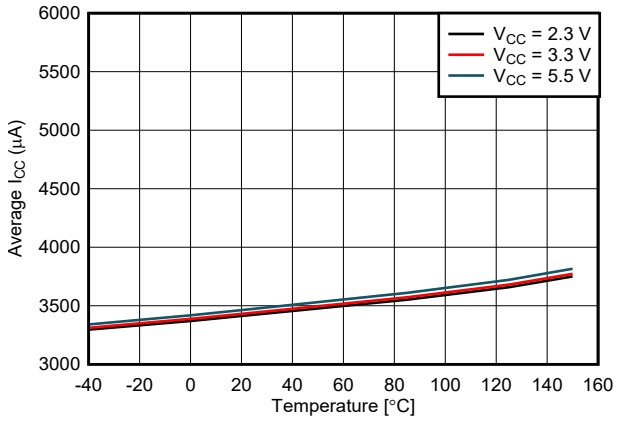


図 5-14. Active Mode Supply Current vs Temperature

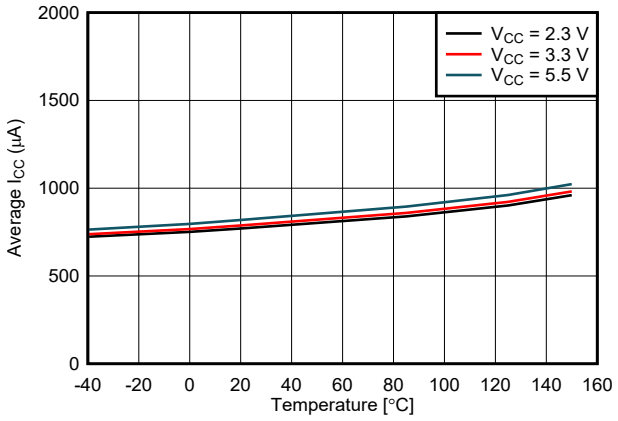


図 5-15. Standby Mode Supply Current vs Temperature

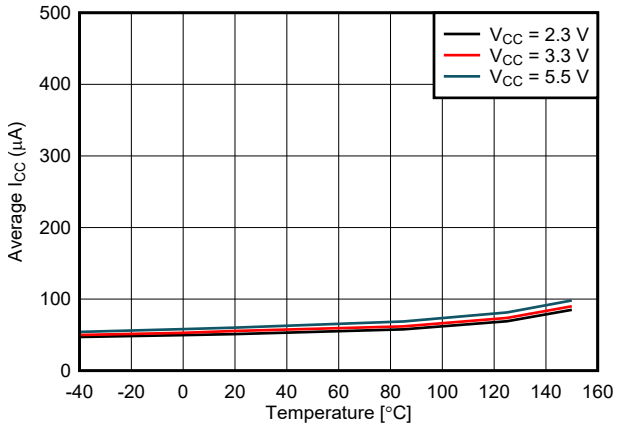


図 5-16. Configuration Mode Supply Current vs Temperature

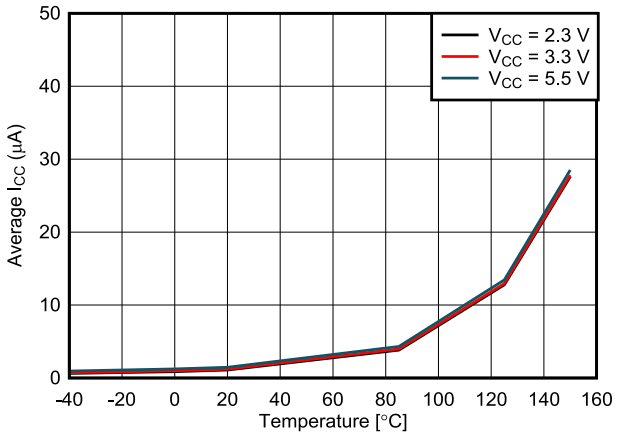


図 5-17. Sleep Mode Supply Current vs Temperature

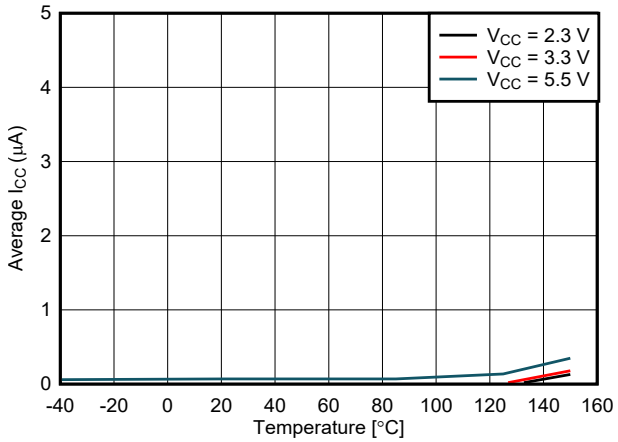


図 5-18. Deep Sleep Mode Supply Current vs Temperature

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6 Detailed Description

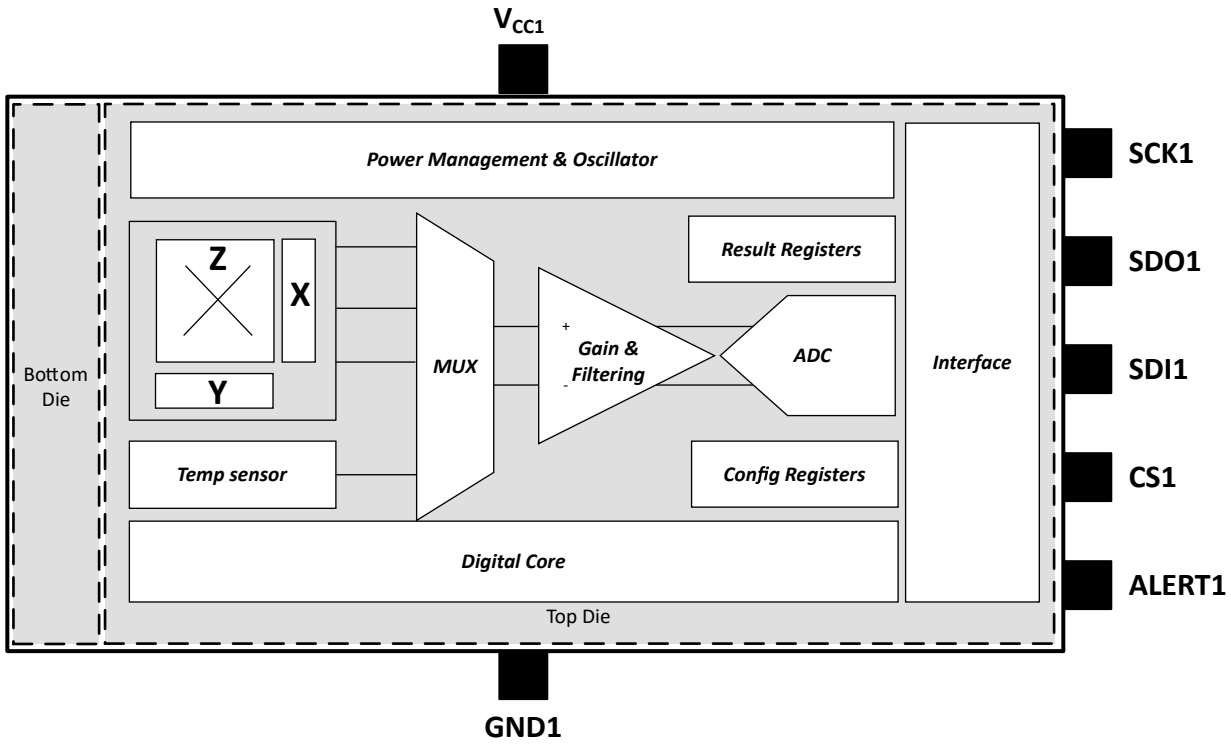
6.1 Overview

The TMAG5170D-Q1 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z magnetic data and die temperature data) is provided through the SPI. The device can be configured in multiple settings through user access registers in the SPI.

The IC consists of the following functional and building blocks:

- The Power Management & Oscillator block contains a low-power oscillator, biasing circuitry, undervoltage and overvoltage detection circuitry, and a fast oscillator.
- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall sensor data and temperature data are multiplexed through the same ADC.
- The Interface block contains the SPI control circuitry, ESD protection circuits, and all the I/O circuits. The TMAG5170D-Q1 supports SPI along with an integrated cyclic redundancy check (CRC).
- The diagnostic blocks are embedded in the circuitry to enable mandatory and user-enabled diagnostic checks.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Magnetic Flux Direction

The TMAG5170D-Q1 is sensitive to the magnetic field component in X, Y, and Z directions. The X and Y fields are in-plane with the package. The Z field is perpendicular to the top of the package. The device is sensitive to both magnetic north and south poles in each axis. As shown in 図 6-1, the device generates positive ADC codes in response to a magnetic south pole in the proximity. Similarly, the device generates negative ADC codes if magnetic north poles approach from the same directions.

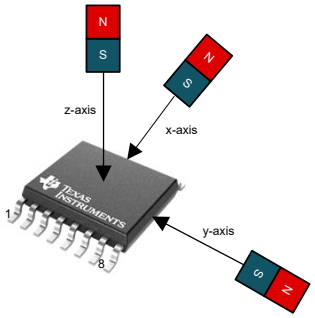


図 6-1. Direction of Applied Magnetic South Pole to Generate Positive ADC Codes

6.3.2 Sensor Location

図 6-2 shows the location of the X, Y, Z Hall elements inside the TMAG5170D-Q1.

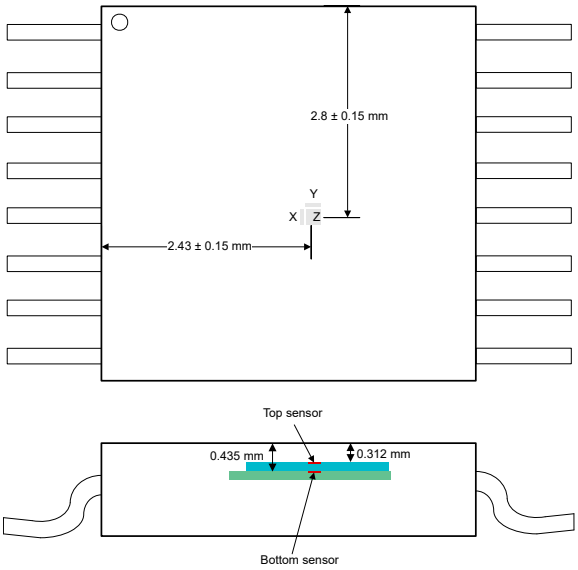


図 6-2. Location of X, Y, Z Hall Elements

6.3.3 Magnetic Range Selection

表 6-1 shows the magnetic range selection for the TMAG5170D-Q1 device. Each axis range can be independently selected irrespective of the others.

表 6-1. Magnetic Range Selection

	RANGE REGISTER SETTING	TMAG5170A1-Q1	TMAG5170A2-Q1	COMMENT
X Axis Field	X_RANGE = 0h	±50 mT	±150 mT	
	X_RANGE = 1h	±25 mT	±75 mT	Best resolution case
	X_ RANGE = 2h	±100 mT	±300 mT	Highest range, best SNR case
Y Axis Field	Y_RANGE = 0h	±50 mT	±150 mT	
	Y_RANGE = 1h	±25 mT	±75 mT	Best resolution case
	Y_RANGE = 2h	±100 mT	±300 mT	Highest range, best SNR case
Z Axis Field	Z_RANGE = 0h	±50 mT	±150 mT	
	Z_RANGE = 1h	±25 mT	±75 mT	Best resolution case
	Z_RANGE = 2h	±100 mT	±300 mT	Highest range, best SNR case

6.3.4 Update Rate Settings

The TMAG5170D-Q1 offers multiple update rates for system design flexibility. 図 6-4 shows the different update rates for the TMAG5170D-Q1 during continuous conversion.

表 6-2. Update Rate Settings

OPERATING MODE	REGISTER SETTING	UPDATE RATE			COMMENT
		SINGLE AXIS	TWO AXIS	THREE AXIS	
X, Y, Z Axis	CONV_AVG = 0h	20 kSPS	13.3 kSPS	10 kSPS	Fastest update rate
X, Y, Z Axis	CONV_AVG = 1h	13.3 kSPS	8.0 kSPS	5.7 kSPS	
X, Y, Z Axis	CONV_AVG = 2h	8.0 kSPS	4.4 kSPS	3.1 kSPS	
X, Y, Z Axis	CONV_AVG = 3h	4.4 kSPS	2.4 kSPS	1.6 kSPS	
X, Y, Z Axis	CONV_AVG = 4h	2.4 kSPS	1.2 kSPS	0.8 kSPS	
X, Y, Z Axis	CONV_AVG = 5h	1.2 kSPS	0.6 kSPS	0.4 kSPS	Best SNR case

6.3.5 ALERT Function

The $\overline{\text{ALERT}}$ pin of the TMAG5170D-Q1 supports multiple operating modes targeting different applications.

6.3.5.1 Interrupt and Trigger Mode

With ALERT_MODE at default value of 0b, the $\overline{\text{ALERT}}$ output can be configured to generate an interrupt signal for the microcontroller when a user-defined event occurs. A user-defined event can be a conversion completion or an error from diagnostic tests. The $\overline{\text{ALERT}}$ pin can also trigger a conversion start in this mode using the TRIGGER_MODE register bit.

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6.3.5.2 Magnetic Switch Mode

With ALERT_MODE set at 1b, the $\overline{\text{ALERT}}$ output is configured as a magnetic switch. One or multiple magnetic channels can be selected in the ALERT_CONFIG register. The magnetic switch thresholds are determined by the *_THRX_CONFIG register bits setting. If the measured magnetic field is greater than *_HI_THRESHOLD, or smaller than *_LO_THRESHOLD, the $\overline{\text{ALERT}}$ output will assert low. 図 6-3 shows the magnetic switch function using the X-axis magnetic field as an example.

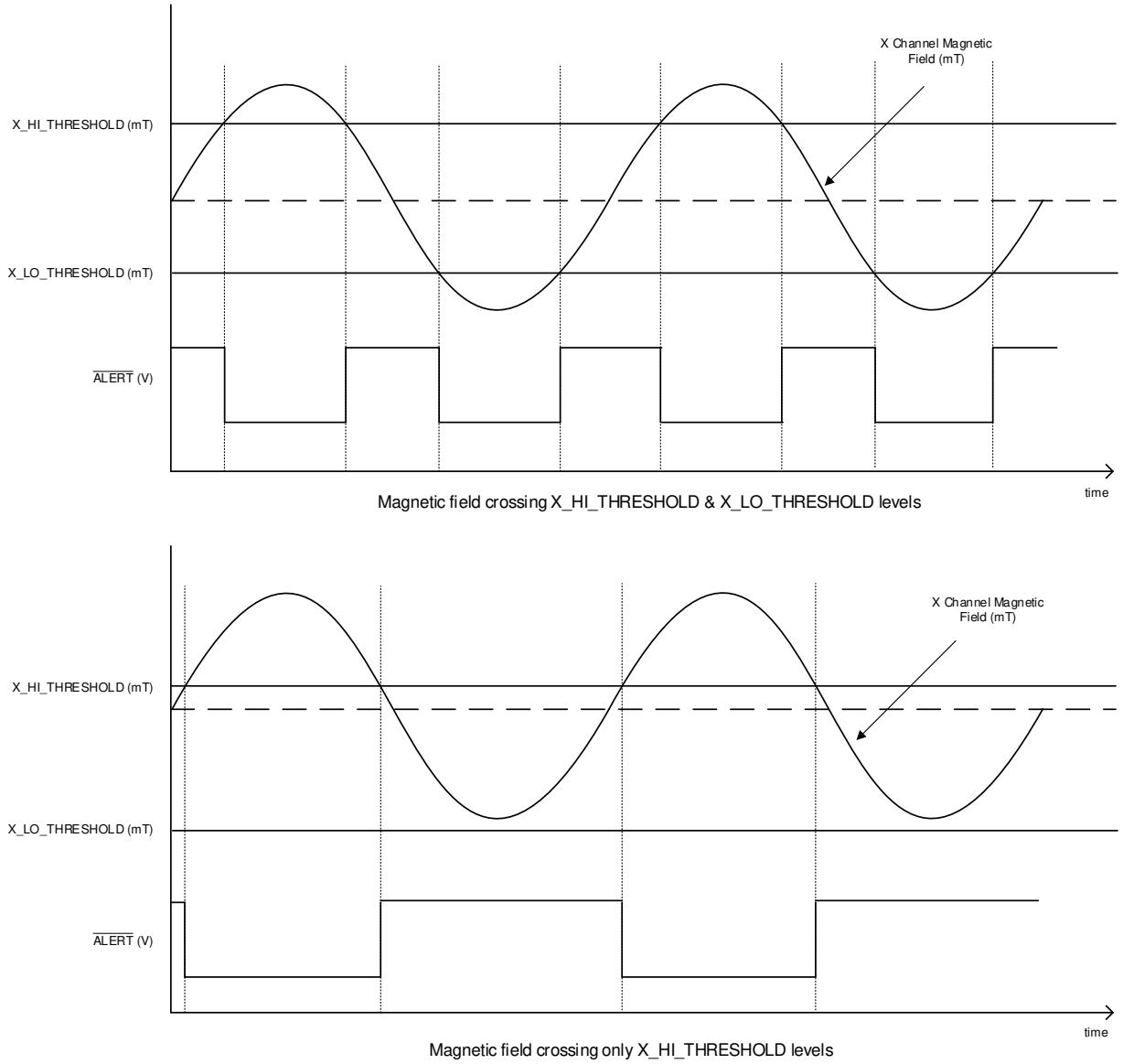


図 6-3. ALERT Pin Working as Magnetic Switch

6.3.6 Threshold Count

The THRX_COUNT bits in the ALERT_CONFIG register offer robust noise filtering and immunity against false tripping while the TMAG5170D-Q1 implements the $\overline{\text{ALERT}}$ function for a specific magnetic or temperature threshold crossing. With THRX_COUNT at default 00b, only one measured value must cross the threshold to be considered a valid threshold crossing event. With THRX_COUNT at 11b, four successive measured values must cross the threshold to be considered a valid threshold crossing. An internal counter tracks and records the number of threshold crossing for a given sensor.

The counter resets if any of the below events occur:

- The device meets the threshold cross count for the specified number per the THRX_COUNT bits, the corresponding *CH_THX bit(s) are set, and the SPI read of the SYS_STATUS register occurred
- If a measured result does not cross the threshold

When the $\overline{\text{ALERT}}$ pin is configured to work as a magnetic switch, the threshold count is active for both low-to-high and high-to-low transitions, offering noise immunity in both directions of the threshold cross.

6.3.7 Diagnostics

The TMAG5170D-Q1 supports several device and system level diagnostics features to detect, monitor, and report failures during the device operation.

In the event of a failure, the TMAG5170D-Q1 reports back to the controller through the following mechanisms:

- ERROR_STAT bit during the SDO read frame
- Direct read of the status registers through the SPI
- $\overline{\text{ALERT}}$ pin response to indicate a failure, if enabled
- No response through SDO line, or CRC error during SPI communication

The TMAG5170D-Q1 performs the following device and system level checks:

6.3.7.1 Memory Cyclic Redundancy Check (CRC)

This diagnostic mechanism checks the content of the internal memory by comparing a calculated CRC of the read content against a factory-programmed expected CRC value. During runtime, when the internal memory is read again for configuration for different channels, the CRC is checked again, providing detection of memory errors even during runtime.

Run Mode	Continuous
Configuration Register(s)	N/A
Fault Register Bit	TRIM_STAT
Impact if disabled	N/A. Cannot be disabled

6.3.7.2 $\overline{\text{ALERT}}$ Integrity Check

This diagnostic mechanism checks and compares the read back value of the $\overline{\text{ALERT}}$ pin to the value that is driven by the device. This will check the presence of an external short on $\overline{\text{ALERT}}$ pin to a higher voltage such as VCC which will prevent device to indicate a fault. When the controller is driving the $\overline{\text{ALERT}}$ pin to trigger a measurement, the controller can read the ALRT_LVL bit to check if the correct polarity of the $\overline{\text{ALERT}}$ was detected by the device, thus checking any failures on the pin.

Run Mode	Continuous
Configuration Register(s)	N/A
Fault Register Bit	ALRT_DRV and ALRT_LVL
Impact if disabled	When driven by device N/A. Cannot be disabled. When driven by controller, device may not detect a new measurement command and still report old measurement data.

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6.3.7.3 VCC Check

This diagnostic mechanism continuously checks the external voltage supply on VCC pin and flags a fault if the supply is out of range.

Run Mode	Continuous
Data Sheet Parameters	V_{CC_UV}, V_{CC_OV}
Fault Register Bit	VCC_UV and VCC_OV
Impact if disabled	N/A. Cannot be disabled.

6.3.7.4 Internal LDO Undervoltage Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the critical analog blocks and Hall sensor biasing, and flags a fault if the internal regulator falls below a threshold after which the accuracy of the magnetic field measurement cannot be guaranteed.

Run Mode	Continuous
Data Sheet Parameters	N/A
Fault Register Bit	LDO_STAT
Impact if disabled	N/A. Cannot be disabled.

6.3.7.5 Digital Core Power-On Reset Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the internal digital core, and puts the device in reset if the digital core cannot function reliably. The occurrence of the fault is detected by reading the CFG_RESET bit which can only be set at power up or if the digital core was reset.

Run Mode	Continuous
Data Sheet Parameters	N/A
Fault Register Bit	CFG_RESET
Impact if disabled	N/A. Cannot be disabled.

6.3.7.6 SDO Output Check

This diagnostic mechanism continuously compares the internally driven value by device on the SDO pin to the read-back value on SDO pin to detect any shorts to ground or power supply.

Run Mode	Continuous, every time a SPI transaction is initiated
Data Sheet Parameters	N/A
Fault Register Bit	SDO_DRV
Impact if disabled	N/A. Cannot be disabled.

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6.3.7.7 Communication Cyclic Redundancy Check (CRC)

This diagnostic mechanism for every SPI transaction will compute the CRC of the received SPI frame from the controller and check the CRC against the CRC value transmitted by the controller, and flag a fault if the values do not match. The device also embeds a CRC value as part of the SPI frame in the response for the controller to check the integrity of the received data. This check detects faults with the SPI communication block in the digital core, the SPI I/O buffers and, and the controller to check for any faults on the SPI external to the device.

Another check also runs in the background that counts the number of SPI clocks in a SPI frame and flags a fault if the number of clocks sent by the controller is not same as the expected value. This can help the controller detect any issues with the SPI.

Run Mode	Continuous, every time a SPI transaction is initiated
Configuration Register(s)	CRC_DIS to disable CRC in the SPI protocol
Fault Register Bit	CRC_STAT, FRAME_STAT
Impact if disabled	If CRC is disabled, then any fault with SPI communication will not be detected and incorrect value of measured field can be reported.

6.3.7.8 Oscillator Integrity Check

This diagnostic mechanism allows the controller to check any hardware fault with the internal oscillator. With this check, any drift of internal oscillators can be checked. The high-frequency oscillator is critical for precision measurement of the magnetic field and low-power oscillator is critical to control wake-up and sleep mode and other state machine control.

To run this check, external software code on the controller is required. The controller must instate the check by setting the OSC_CNT_CTL bits to select a particular oscillator and start the internal count on the device. At the same time, the controller also starts a counter using its own timebase. After a predetermined time, the controller issues a stop to the oscillator count by setting OSC_CNT_CTL = 03h and read the OSC_COUNT. The read value of the OSC_COUNT should not exceed the value based off maximum f_{HFOSC}, f_{LFPOSC} in the specification section. Consider the variation of controller speed and SPI communication when calculating the error margin for the OSC_COUNT.

Run Mode	On-demand as run by the external controller
Data Sheet Parameter(s)	f_{HFOSC}, f_{LFPOSC}
Configuration Register(s)	OSC_CNT_CTL
Fault Register Bit	OSC_COUNT
Impact if disabled	If the controller decides not to run this test, then any drift of HF oscillator can impact the accuracy of the reported sensor data

6.3.7.9 Magnetic Field Threshold Check

This diagnostic mechanism allows the controller to monitor the external applied field. The controller can use this check to determine if a magnetic field is present within specified thresholds. This check, though used as check at system level, can also indicate any gross problems with the signal path if a field much outside the expected range is detected and reported.

To run this check, the controller must enable the check separately for each axis and also set the thresholds for each axis independently. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if the threshold crossed, which is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	X_HLT_EN, Y_HLT_EN, Z_HLT_EN to enable test. X_THRX_CONFIG, Y_THRX_CONFIG, Z_THRX_CONFIG to set threshold
Fault Register Bit	XCH_THX, YCH_THX, ZCH_THX
Impact if disabled	Disabling this check does not have an impact on device-level failure detection but can impact at system level. Examples of system failure can be loss of magnet, magnet too far, or too close to the sensor.

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6.3.7.10 Temperature Alert Check

This diagnostic mechanism allows the controller to monitor the junction temperature of the die, which is also an indication of the ambient temperature as the device does not generate significant self-heating. This is useful to monitor the temperature at the system level accurately and alert the controller if the temperature is exceeded. The check can also be used to warn the controller if the die temperature due to some internal failure has increased beyond the expected range.

To run this check, the controller must enable the temperature check and set the threshold. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if the threshold crossed, which is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	T_HLT_EN to enable test. T_THRX_CONFIG to set threshold
Fault Register Bit	TEMP_THX
Impact if disabled	Disabling this check does not have an impact on device-level failure detection but can impact at system level increase or decrease of temperature.

6.3.7.11 Analog Front-End (AFE) Check

This diagnostic mechanism allows the controller to check the performance of the analog signal path. In this check, the device disconnects the Hall sensor from the signal path and uses an alternate resistance bridge to create a known, predetermined signal as an input to the signal path. This mechanism then checks if the measured digital value compared to a fixed value from the factory is within a pre-programmed, factory-determined value. This mechanism can detect issues with multiplexers, offset cancellation mechanism, the gain stages, the low-pass filter, and the ADC as well.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the AFE is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	SENS_STAT
Impact if disabled	If disabled, any failures or drift with the analog front-end signal path may not be detected.

6.3.7.12 Hall Resistance and Switch Matrix Check

This diagnostic mechanism allows the controller to check if the sensitivity of the Hall sensor is within the factory-determined limits by checking the resistance of the Hall-effect sensor. In this check, the biasing and multiplexing control of all directions of the Hall sensor (X, Y and Z) are also checked.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the Hall sensor is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	ZHS_STAT, YHS_STAT and XHS_STAT
Impact if disabled	If disabled, any failures or drift in the Hall-effect sensor properties and biasing will not be detected, leading to potentially incorrect magnetic field conversion

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6.3.7.13 Hall Offset Check

This diagnostic mechanism allows the controller to check if the offset of the Hall sensor is within the factory-determined limits and the offset cancellation circuitry is working properly.

To run this check, the controller must enable the check and set the scheduling for the run. During this check, the AFE is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	SENS_STAT
Impact if disabled	If disabled, any failures with offset cancellation mechanism or large drift of Hall-effect sensor may not be detected, leading to potentially incorrect magnetic field conversion.

6.3.7.14 ADC Check

This diagnostic mechanism checks ADC functionality and conversion. This check is done by converting a known band-gap voltage, which is completely independent of the ADC reference, and comparing the voltage against the factory-determined tolerance limits.

To run this check, the controller must enable the check and set the scheduling for the run. During this check the AFE is not available for magnetic field conversion. The user can configure the $\overline{\text{ALERT}}$ pin to toggle if an error is detected. This error is also reported in the user register.

Run Mode	Every time a magnetic measurement is initiated and completed
Configuration Register(s)	DIAG_EN to enable test. DIAG_SEL to schedule when the test is run
Fault Register Bit	TEMP_STAT
Impact if disabled	If disabled, any failures with ADC conversion will not be detected, leading to potentially incorrect errors in the converted magnetic field values.

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6.4 Device Functional Modes

6.4.1 Operating Modes

The TMAG5170D-Q1 supports multiple operating modes for wide array of applications as explained in 図 6-4. The device starts powering up after the VCC supply crosses the minimum threshold as specified in the *Recommended Operating Conditions* table. Any particular operating mode can be selected by setting the corresponding OPERATING_MODE register bits.

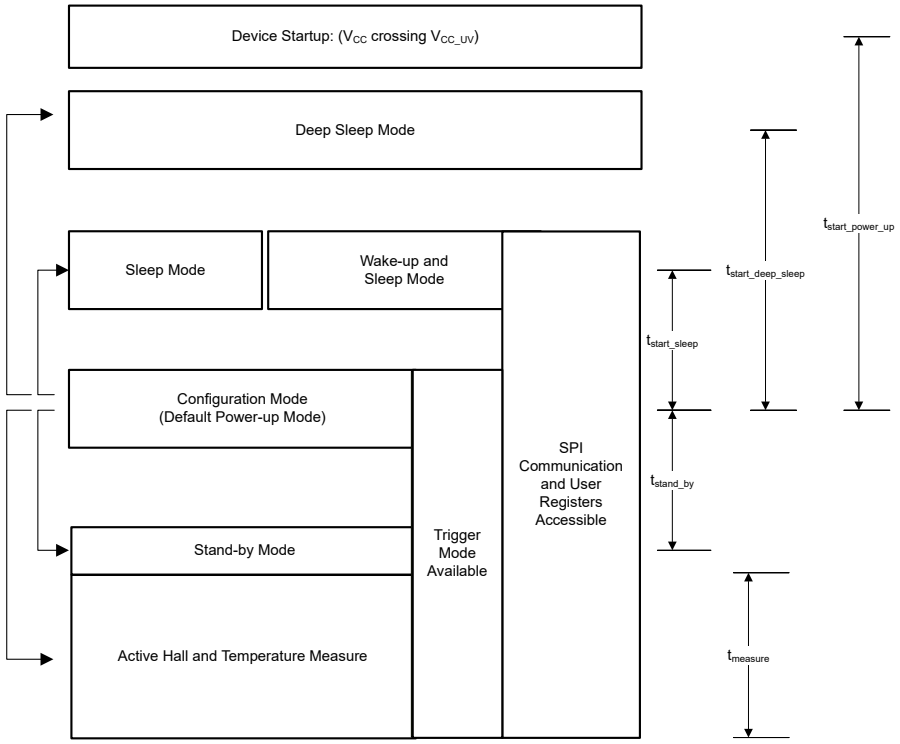


図 6-4. TMAG5170D-Q1 Power-Up Sequence

表 6-3 shows different power saving modes of the TMAG5170D-Q1.

表 6-3. Comparing Operating Modes

OPERATING MODE	DEVICE FUNCTION	INITIALIZATION TIME TO START CONVERSION(1)	DATA CONVERSION
Active Conversion	Continuously measuring X, Y, Z axis, or temperature data	10 µs	Supports continuous and trigger mode conversion
Standby Mode	Device is ready to accept SPI commands and start active conversion	35 µs	Supports trigger mode conversion
Configuration Mode	SPI and user configuration registers active	t_{stand_by} + 35 µs	Supports trigger mode conversion
Wake-up & Sleep Mode	Wakes up at a certain interval to measure the X, Y, Z axis, or temperature data	t_{start_sleep} + t_{stand_by} + 35 µs	1, 5, 10, 15, 20, 30, 100, 500, and 1000-ms intervals supported(1).
Sleep Mode	Device retains key configuration settings, and last measurement data	t_{start_sleep} + t_{stand_by} + 35 µs	The microcontroller can use sleep mode to implement other power saving intervals not supported by wake-up and sleep mode.
Deep-sleep Mode	Device does not retain key configuration settings, and last measurement data	$t_{start_deep_sleep}$ + t_{stand_by} + 35 µs	No conversion start is supported during deep-sleep mode

(1) The timing numbers are typical parameters. The values may vary depending on the internal oscillator frequency.

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6.4.1.1 Active Mode

The TMAG5170D-Q1 converts the magnetic sensor or temperature data during active mode. Active mode supports both continuous conversion and trigger mode conversion based off the OPERATING_MODE setting. Continuous operation at this mode is useful for applications where the fastest data conversion is required, and power budget is not stringent. In the active trigger mode, a controller can trigger a conversion through one of several trigger mechanisms as described in the TRIGGER_MODE register bits. When the conversion started, the time it takes to finish a conversion is denoted by $t_{measure}$. The conversion time can vary widely based off the MAG_CH_EN, CONV_AVG, DIAG_SEL, and DIAG_EN register bits setting. The average current consumption during the active conversion is I_{ACT}.

6.4.1.2 Standby Mode

In standby mode, the TMAG5170D-Q1 is ready to start sensor conversion with a trigger command from a controller. Several trigger methods are supported as defined in the TRIGGER_MODE register bits. During this operating mode, the relevant analog and digital support circuitry remain active to enable a faster conversion start. The average current consumption during this mode is denoted by I_{STDBY}. The time it takes for the device to go to standby mode from configuration mode is denoted by t_{stand_by}.

6.4.1.3 Configuration Mode (DEFAULT)

At power up, the TMAG5170D-Q1 goes into the default configuration mode. In this mode, the SPI communication and user register access are enabled. A controller may configure the device to select the desired operating mode, sensor data conversion, enable or disable diagnostic features, and so forth. The average current consumption during this mode is denoted by I_{CFG}. Similar to the standby mode, the configuration mode also supports sensor conversion start with a trigger. However, the configuration mode takes longer time to start the sensor conversion, and consumes approximately ten times less current compared to standby mode.

6.4.1.4 Sleep Mode

The TMAG5170D-Q1 supports the sleep mode where the device retains the user configuration settings and previous conversion results. A controller can wake up the device from sleep mode through either the SPI communication or the $\overline{\text{ALERT}}$ signal. The average power consumption in this mode is denoted by I_{SLP}. The time it takes for the device to go to the configuration mode from the sleep mode is denoted by t_{start_sleep}.

6.4.1.5 Wake-Up and Sleep Mode

The TMAG5170D-Q1 supports the wake-up and sleep mode where the device is configured to wake up at a certain time interval, and perform the sensor conversion as defined in the SENSOR_CONFIG register setting. When the sensor conversion is complete, an $\overline{\text{ALERT}}$ signal can be generated to notify the controller that the new conversion data is ready. It is possible to generate an $\overline{\text{ALERT}}$ signal only in the event a particular magnetic or temperature threshold is exceeded. Detail setting on $\overline{\text{ALERT}}$ signal is specified in the ALERT_CONFIG register. A controller can wake up the TMAG5170D-Q1 and access the conversion data at any time. The average power consumption in the wake-up and sleep mode is denoted by I_{VCC_DCM}. The time it takes for the device to go to configuration mode from wake-up and sleep mode is denoted by t_{start_sleep}.

6.4.1.6 Deep-Sleep Mode

For ultra-low power system, the TMAG5170D-Q1 supports a deep-sleep mode to conserve power. In this mode, the TMAG5170D-Q1 does not retain the user configuration or previous result data. The device reverts back to factory setting in this mode. The average power consumption in this mode is I_{DEEP_SLP}. The time it takes for the device to go to the configuration mode from the deep-sleep mode is denoted by t_{start_sleep}.

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6.5 Programming

6.5.1 Data Definition

6.5.1.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in the X_CH_RESULT, Y_CH_RESULT, and Z_CH_RESULT registers, respectively. ADC output stored in 16-bit result registers in 2's complement format. With fastest conversion (CONV_AVG = 0h), the ADC output loads the 12 MSB bits of the 16-bit result register along with 4 LSB bits as zeros. With CONV_AVG != 0h, all the 16 bits are used to store the results. With DATA_TYPE = 0h, the 16-bit magnetic sensor data can be accessed through regular 32-bit SPI read. The LSB size for each magnetic range is:

- 50 mT: 654 LSB/mT
- 25 mT: 1308 LSB/mT
- 100 mT: 326 LSB/mT
- 150 mT: 218 LSB/mT
- 75 mT: 436 LSB/mT
- 300 mT: 108 LSB/mT

表 6-4. 16-Bit X, Y, Z Magnetic Sensor Data Format. Two decimal places are shown.

Magnetic Field (mT)						x_CH_RESULT	
Range = 50 mT	Range = 25 mT	Range = 100 mT	Range = 150 mT	Range = 75 mT	Range = 300 mT	BINARY	HEX
-50.103	-25.051	-100.515	-150.311	-75.155	-303.407	1000 0000 0000 0000	8000h
-25.051	-12.525	-50.257	-75.155	-37.577	-151.703	1100 0000 0000 0000	C000h
-0.001	-0.001	-0.003	-0.004	-0.002	-0.009	1111 1111 1111 1111	FFFFh
0	0	0	0	0	0	0000 0000 0000 0000	0000h
0.001	0.001	0.003	0.004	0.002	0.009	0000 0000 0000 0001	0001h
25.051	12.525	50.257	75.155	37.577	151.703	0100 0000 0000 0000	4000h
50.102	25.051	100.512	150.307	75.153	303.398	0111 1111 1111 1111	7FFFh

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6.5.1.2 Temperature Sensor Data

The TMAG5170D-Q1 temperature sensor will measure temperature from –40°C to 170°C and store the result in the 16-bit TEMP_RESULT register. With CONV_AVG != 0h, and DATA_TYPE = 0h, the 16-bit temperature data can be accessed through regular 32-bit SPI read using 式 1 to calculate the temperature. If CONV_AVG = 0h or DATA_TYPE != 0h, use 式 2 to calculate the temperature.

$$T = T_{SENS_T0} + \frac{TADC_T - TADC_{T0}}{TADC_{RES}} \quad (1)$$

where

- T is the measured temperature in degree Celsius.
- T_{SENS_T0} is 25°C.
- $TADC_{RES}$ is 60.0 LSB/°C.
- $TADC_{T0}$ is 17522.
- $TADC_T$ is the TEMP_RESULT register value in decimal.

$$T = T_{SENS_T0} + \frac{16 \times \left(TADC_T - \frac{TADC_{T0}}{16}\right)}{TADC_{RES}} \quad (2)$$

表 6-5. 16-Bit Temperature Data Format. Two decimal places are shown.

TEMPERATURE (°C)	TEMP_RESULT	
	BINARY	HEX
–40	0011 0101 0011 0110	3536h
–25	0011 1000 1011 1010	38BAh
0	0011 1110 1001 0110	3E96h
25	0100 0100 0111 0010	4472h
25.01	0100 0100 0111 0011	4473h
85	0101 0010 1000 0010	5282h
125	0101 1011 1110 0010	5BE2h

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6.5.1.3 Magnetic Sensor Offset Correction

図 6-5 shows that the TMAG5170D-Q1 can enable offset correction for a pair of magnetic axes. The magnetic axes and order are selected based off the ANGLE_EN register bit settings. The MAG_OFFSET_CONFIG register stores the offset values to be corrected in 2's complement data format. The selection and order of the sensors are defined in the ANGLE_EN register bits setting. The default value of these offset correction registers are set as zero.

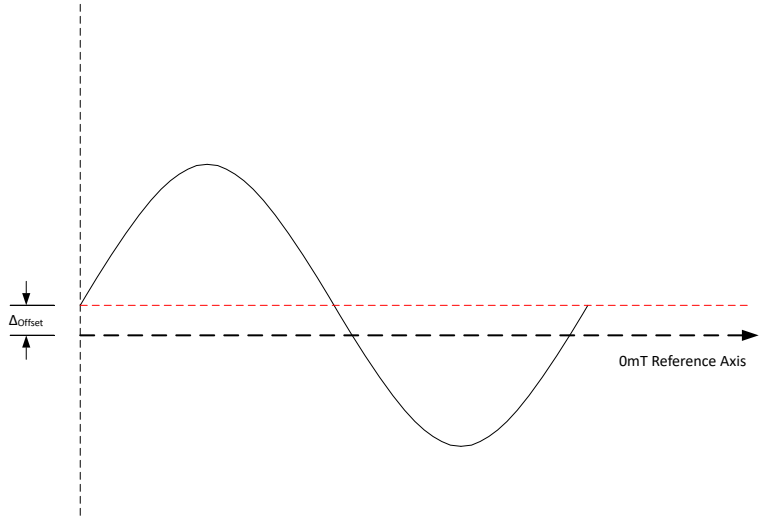


図 6-5. Magnetic Sensor Data Offset Correction

The MAG_OFFSET_CONFIG register contains OFFSET_VALUE1 and OFFSET_VALUE2 that are added to the sensor conversion results as defined by of the OFFSET_SELECTION field of the MAG_OFFSET_CONFIG register. The data format is 2's complement format with a LSB size define by the range.

- 50 mT: 25 µT/LSB
- 25 mT: 12.5 µT/LSB
- 100 mT: 50 µT/LSB
- 150 mT: 75 µT/LSB
- 75 mT: 37.5 µT/LSB
- 300 mT: 150 µT/LSB

表 6-6. 7-bit Magnetic Sensor Offset Correction Data Format. Two decimal places are shown.

Magnetic Offset (mT)						Offset_Config_x[7:0]	
Range = 50 mT	Range = 25 mT	Range = 100 mT	Range = 150 mT	Range = 75 mT	Range = 300 mT	BINARY	HEX
-1.60	-0.80	-3.20	-4.80	-2.40	-9.60	100 0000	40h
-1.35	-0.67	-2.70	-4.05	-2.02	-8.10	100 1010	4Ah
-0.02	-0.01	-0.05	-0.07	-0.03	-0.15	111 1111	7Fh
0	0	0	0	0	0	000 0000	00h
0.02	0.01	0.05	0.07	0.03	0.15	000 0001	01h
1.35	0.67	2.70	4.05	2.02	8.10	011 0110	36h
1.57	0.78	3.15	4.72	2.36	9.45	011 1111	3Fh

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6.5.1.4 Angle and Magnitude Data Definition

The TMAG5170D-Q1 calculates the angle based off the ANGLE_EN register bit settings. The 11-bit ANGLE_RESULT value stores the angle information. The data format is an unsigned angle value with a LSB size of 0.25°. The TMAG5170D-Q1 CORDIC offers angle resolution of 0.25 degree. The TMAG170 code example software package has functions that can be ported to the system microcontroller for an accurate but computationally inexpensive angle calculation using the TMAG5170D-Q1 axes readings.

表 6-7. 11-Bit Angle Data Format

ANGLE (°)	ANGLE_RESULT[10:0]	
	BINARY	HEX
0	000 0000 0000	000h
0.25	000 0000 0001	001h
90	001 0110 1000	168h
180	010 1101 0000	2D0h
270	100 0011 1000	438h
360	101 1010 0000	5A0h

During the angle calculation, the MAGNITUDE_RESULT[13:0] stores the resultant vector magnitude in the MAGNITUDE_RESULT register. MAGNITUDE_RESULT is an unsigned value with a LSB size that depends on the range of device.

- 50 mT: 40.96 LSB/mT
- 25 mT: 81.92 LSB/mT
- 100 mT: 20.48 LSB/mT
- 150 mT: 13.65$\overline{3}$ LSB/mT
- 75 mT: 27.30$\overline{6}$ LSB/mT
- 300 mT: 6.82$\overline{6}$ LSB/mT

For on-axis angular measurement the magnitude value should remain constant across the full 360° measurement.

表 6-8. 13-bit Magnitude Data Format. Only 3 decimal places are shown.

Magnitude (mT)						MAGNITUDE_RESULT[13:0]	
Range = 50 mT	Range = 25 mT	Range = 100 mT	Range = 150 mT	Range = 75 mT	Range = 300 mT	BINARY	HEX
0	0	0	0	0	0	0 0000 0000 0000	0000h
0.024	0.012	0.048	0.073	0.036	0.146	0 0000 0000 0001	0001h
6.225	3.112	12.451	18.676	9.338	37.353	0 0000 1111 1111	00FFh
35.351	17.675	70.703	106.054	53.027	212.109	0 0101 1010 1000	05A8h
70.703	35.351	141.406	212.109	106.054	424.218	0 1011 0101 0000	0B50h

6.5.2 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface used for short distance communication, usually between devices on a printed circuit board (PCB) assembly. The TMAG5170D-Q1 supports a 4-wire SPI. The primary communication between the device and the external microcontroller is through the SPI bus that provides full-duplex communication. The external microcontroller works as the SPI controller that sends command requests on the SDI pin and receives device responses on the SDO pin. The TMAG5170D-Q1 device works as the SPI peripheral device that receives command requests and sends responses (such as status and measured values) to the external microcontroller over the SDO line. The TMAG5170D-Q1 supports a fixed 32-bit frame size to communicate with a controller device. However, the 32-bit frame can be configured through DATA_TYPE register bits to support a regular single register read data packet, or a special packet to read two-channel data simultaneously.

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6.5.2.1 SCK

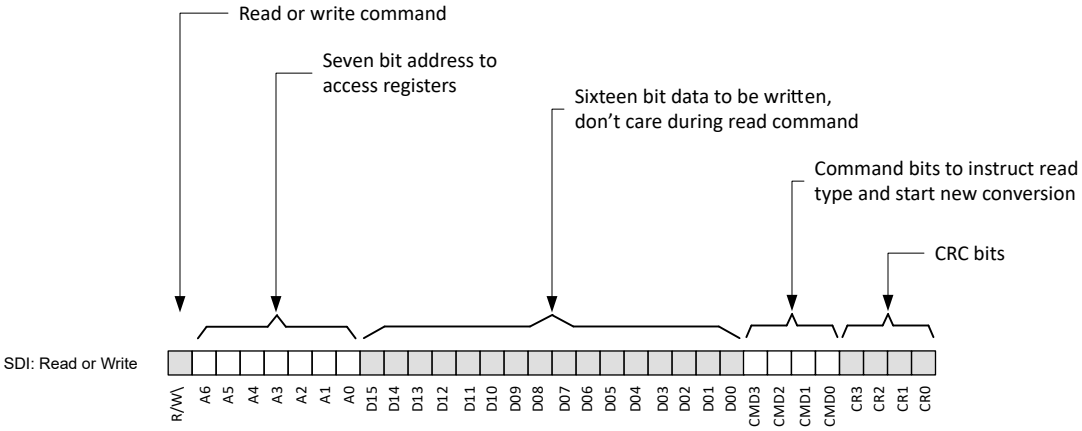
The Serial Clock (SCK) represents the controller clock signal. This clock determines the speed of data transfer and all receiving and sending are done synchronously to this clock. The output data on the SDO pin transitions on the falling edge of the SCK and input data on the SDI pin is latched on the rising edge of the SC.

6.5.2.2 $\overline{CS}$

The $\overline{CS}$ activates the SPI. As long as the $\overline{CS}$ signal is at high level, the TMAG5170D-Q1 will not accept the SCK signal or the Serial-data-in (SDI), and the Serial-data-out (SDO) is in high impedance. Hold $\overline{CS}$ low for the duration of a communication frame without toggling to ensure proper communication. The SPI is disabled each time $\overline{CS}$ is brought from low to high.

6.5.2.3 SDI

The Serial-data-in (SDI) line is used by the controller to configure the user access registers, start a new conversion, or send a read command. The SDI bits are transmitted with each SCK rising edge when the $\overline{CS}$ pin is low. 図 6-6 explains the SDI frame details. There are four command bits in the SDI line to select the status bit for the next frame or start a new conversion.



CMD0	CMD0 = 0	No conversion start through command bits
	CMD0 = 1	Start of conversion at the 32-bit SPI frame last SCK pulse falling edge
CMD1	CMD1 = 0	Display SET_COUNT [2:0] in STAT [2:0] bits at SDO next frame
	CMD1 = 1	Display DATA_TYPE [2:0] in STAT [2:0] bits at SDO next frame

* CMD2 & CMD3 are reserved bits
** SET_COUNT register bits indicate the rolling count of the conversion data set. The counter is reset after 111b.
*** DATA_TYPE register bits indicate the type of data being read through the SDO line

図 6-6. 32-Bit Frame Definition of the SDI Line

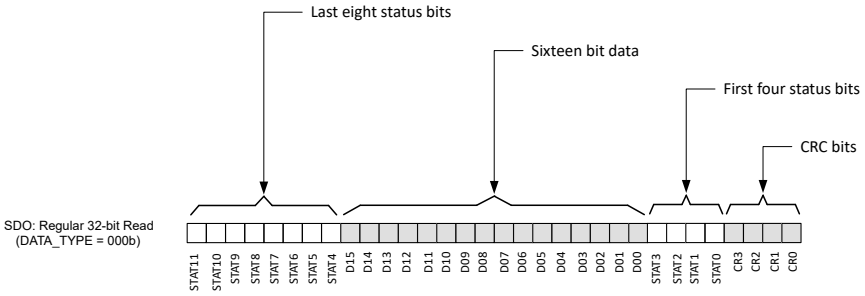
6.5.2.4 SDO

The Serial-data-out (SDO) line is used by the controller to read the data from the TMAG5170D-Q1. The TMAG5170D-Q1 will shift out command responses and ADC conversion data serially with each falling SCK edge when the $\overline{CS}$ pin is low. This pin assumes a high-impedance state when $\overline{CS}$ is high. Based off the DATA_TYPE bit setting, the TMAG5170D-Q1 supports two different SDO frames:

- *Regular 32-Bit SDO Read*
- *Special 32-Bit SDO Read*

6.5.2.4.1 Regular 32-Bit SDO Read

With DATA_TYPE = 000b, the TMAG5170D-Q1 supports a regular 16-bit register read during the 32-bit SDO frame as explained in 図 6-7. In this read mode, 12-bit status bits are displayed. All the status bits except for the ERROR_STAT bit are directly read from the status registers. The ERROR_STAT bit indicates if any error bit set in the device. 図 6-7 shows how the status bits STAT[2:0] can be changed based off CMD1 value in the previous frame.



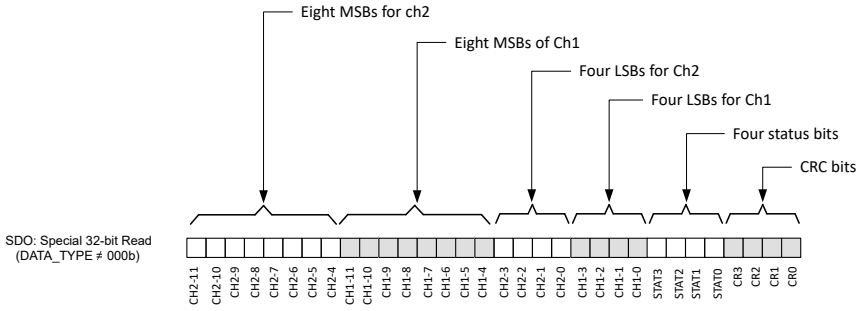
STAT11	STAT10	STAT9	STAT8	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
PREV_CRC_STAT	CFG_RESET	ALRT_STATUS1	ALRT_STATUS0	X	Y	Z	T	ERROR_STAT	Follows CMD1 instruction from previous frame		

* PREV_CRC_STAT indicates if there is any CRC error in the immediate past frame
** ERROR_STAT indicates if there is any error bit flipped in the part
*** STAT10 to STAT4 indicate select status bits from the CONV_STATUS and AFE_STATUS registers

図 6-7. Regular 32-Bit SDO Read

6.5.2.4.2 Special 32-Bit SDO Read

With DATA_TYPE > 000b, the TMAG5170D-Q1 supports a special 32-bit SDO frame for two-channel simultaneous data read. Each channel data is limited to 12 bits. This feature is useful for systems requiring faster data throughput while performing multi-axis measurements. 図 6-8 explains the detail construction of the special 32-bit SDO frame. When the device is set to special 32-bit read, the device will continue to deliver the 2-channel data set through the SDO line during consecutive read or write cycles. DATA_TYPE bits must be reset to get back to a regular read cycle. Only four status bits are transmitted in this mode. All the status bits except for the ERROR_STAT bit are directly read from the status registers. The ERROR_STAT bit indicates if any error bit set in the device. The status bits, STAT[2:0], can be changed based off CMD1 value in the previous frame.



STAT3	STAT2	STAT1	STAT0
ERROR_STAT	Follows CMD1 instruction from previous frame		

* ERROR_STAT indicates if there is any error bit set in the device

図 6-8. Special 32-Bit SDO Read

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6.5.2.5 SPI CRC

The TMAG5170D-Q1 performs mandatory CRC for SPI communication. The data integrity is maintained in both directions by a 4-bit CRC covering the content of the incoming and outgoing 32-bit messages. The four LSB bits of each 32-bit SPI frame are dedicated for the CRC. The CRC code is generated by the polynomial $x^4 + x + 1$. Initialize the CRC bits with b1111.

During the SDI write frame, the TMAG5170D-Q1 reads for the CRC data before executing a write instruction. The write instruction from the controller is ignored if there is any CRC error present in the frame. During the SDI regular read frame, the TMAG5170D-Q1 starts to deliver the requested data through SDO line in the same frame and notifies the controller of any error occurrence through the ERROR_STAT bit. If the device detects a CRC error in the SDI line, the device will invert the last bit of the SDO CRC in the same frame to promptly signal to a controller that the SPI communication is compromised. A controller can also determine the presence of a CRC error in the SDI frame by checking the Status11 bit in the next regular read frame.

注

The TMAG5170D-Q1 default mode at power up is CRC-enabled. With CRC enabled, the device will ignore all the SDI commands if proper CRC codes are not received. To disable the CRC at the SDI line, send the SPI SDI command x0F000407.

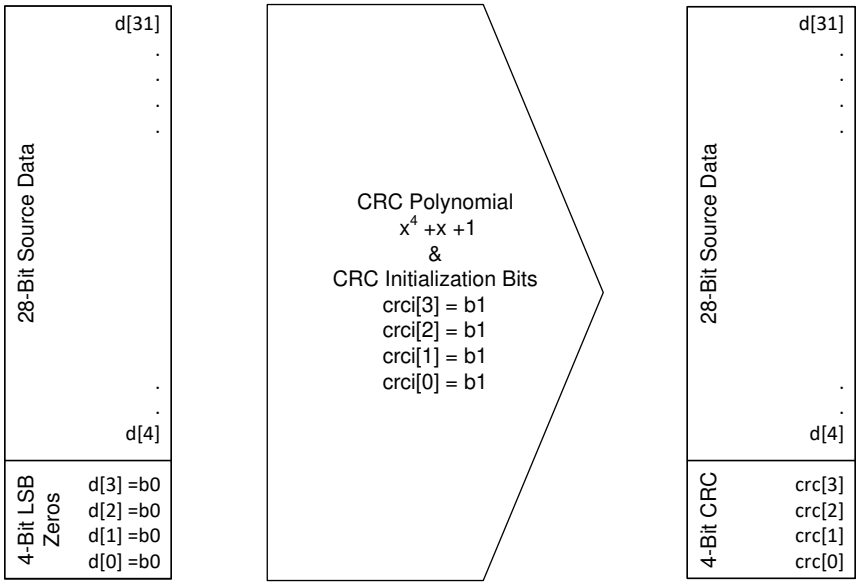


図 6-9. 4-Bit CRC Calculation

Use the following XOR function equations to calculate the 4-bit CRC. 図 6-9 describes the notations of these equations.

$$crc[0] = d[30] \wedge d[26] \wedge d[25] \wedge d[24] \wedge d[23] \wedge d[21] \wedge d[19] \wedge d[18] \wedge d[15] \wedge d[11] \wedge d[10] \wedge d[9] \wedge d[8] \wedge d[6] \wedge d[4] \wedge d[3] \wedge d[0] \wedge crci[2] \quad (3)$$

$$crc[1] = d[31] \wedge d[30] \wedge d[27] \wedge d[23] \wedge d[22] \wedge d[21] \wedge d[20] \wedge d[18] \wedge d[16] \wedge d[15] \wedge d[12] \wedge d[8] \wedge d[7] \wedge d[6] \wedge d[5] \wedge d[3] \wedge d[1] \wedge d[0] \wedge crci[2] \wedge crci[3] \quad (4)$$

$$crc[2] = d[31] \wedge d[28] \wedge d[24] \wedge d[23] \wedge d[22] \wedge d[21] \wedge d[19] \wedge d[17] \wedge d[16] \wedge d[13] \wedge d[9] \wedge d[8] \wedge d[7] \wedge d[6] \wedge d[4] \wedge d[2] \wedge d[1] \wedge crci[0] \wedge crci[3] \quad (5)$$

$$crc[3] = d[29] \wedge d[25] \wedge d[24] \wedge d[23] \wedge d[22] \wedge d[20] \wedge d[18] \wedge d[17] \wedge d[14] \wedge d[10] \wedge d[9] \wedge d[8] \wedge d[7] \wedge d[5] \wedge d[3] \wedge d[2] \wedge crci[1] \quad (6)$$

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The following shows example codes for calculating the 4-bit CRC.

```
function logic [3:0] calculate_crc4;
   input logic [27:0] frame;

   logic [31:0]       padded_frame;
   logic [3:0]           frame_crc;
   logic           inv;
   integer           i;

   padded_frame = {frame, 4'b0000};

   begin
      frame_crc = 4'hf; // initial value
      for (i=31; i >= 0; i=i-1) begin
     inv = padded_frame[i] ^ frame_crc[3];
     frame_crc[3] = frame_crc[2];
     frame_crc[2] = frame_crc[1];
     frame_crc[1] = frame_crc[0] ^ inv;
     frame_crc[0] = inv;
      end
      return frame_crc;
   end
endfunction
```

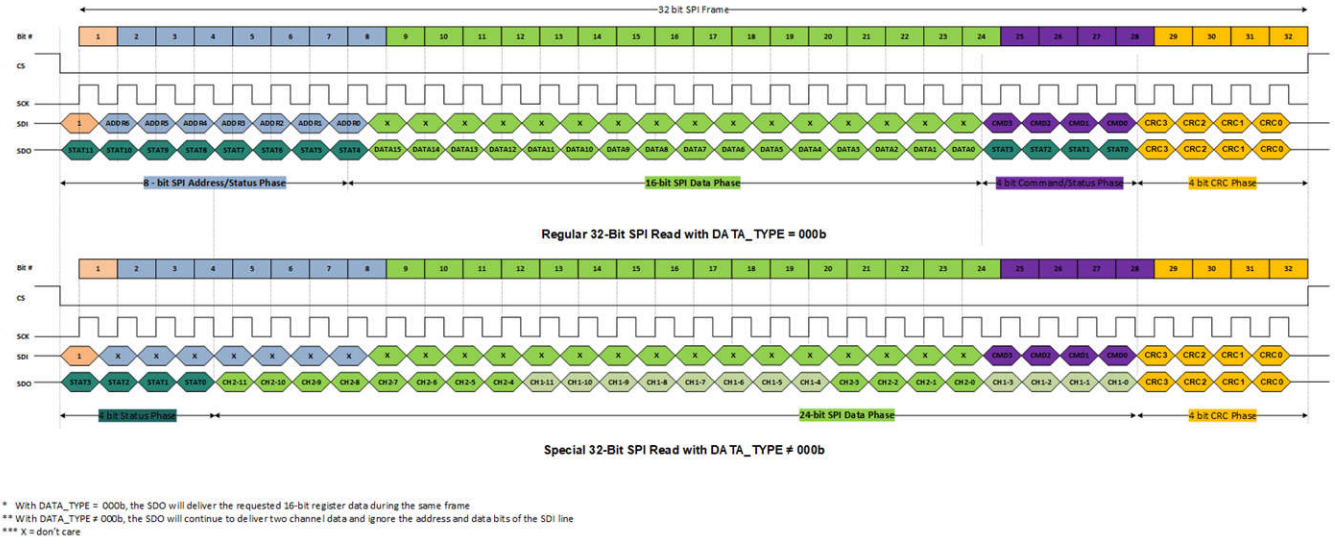
6.5.2.6 SPI Frame

With the flexible definition of the 32-bit frames, the TMAG5170D-Q1 supports a wide array of application requirements catering to multiple user-specific data throughout. Two different frame examples are shown in this section to illustrate the complete SPI bus communication:

- *32-Bit Read Frame*
- *32-Bit Write Frame*

6.5.2.6.1 32-Bit Read Frame

図 6-10 shows both regular and special SDO frames during SDI read command. The TMAG5170D-Q1 implements in-frame communication. When the controller sends a register read command during a regular read cycle, the corresponding 16-bit register data is sent through the SDO line in the same frame. During the special read cycle, the TMAG5170D-Q1 ignores the address and data bits of the SDI line and sends the two channel data set through the SDO line as defined in the DATA_TYPE register bits.



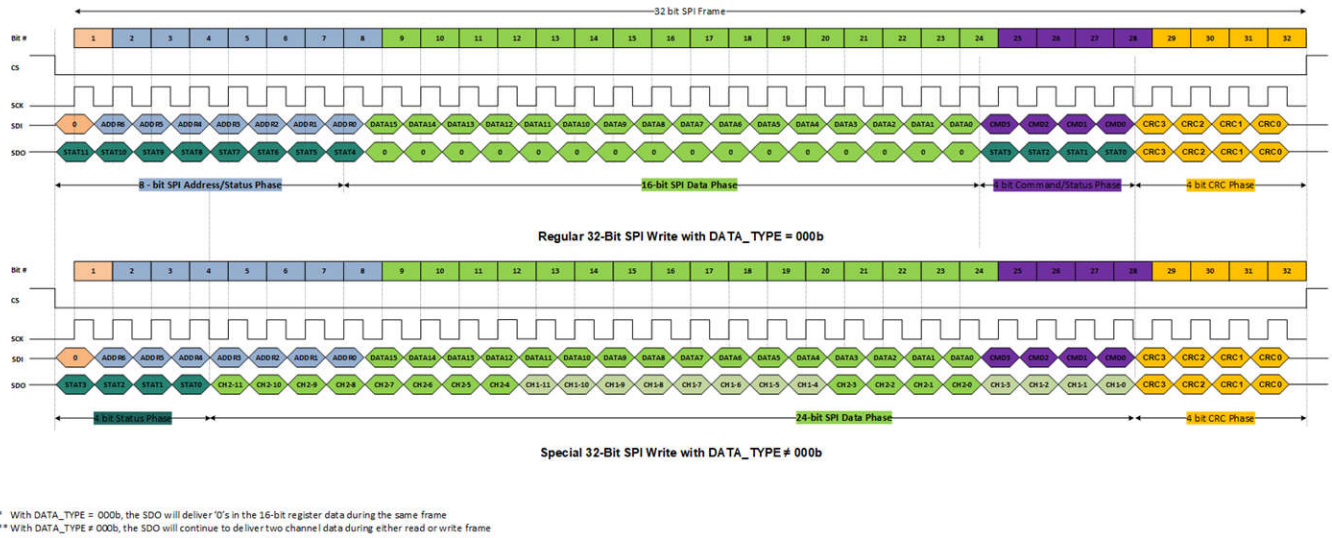
* With DATA_TYPE = 000b, the SDO will deliver the requested 16-bit register data during the same frame
** With DATA_TYPE ≠ 000b, the SDO will continue to deliver two channel data and ignore the address and data bits of the SDI line
*** X = don't care

図 6-10. 32-Bit SPI Read

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6.5.2.6.2 32-Bit Write Frame

図 6-11 shows both regular and special SDO frames during SDI write command. During a regular 32-bit frame write command through SDI, the SDO delivers '0's in place of 16-bit data placeholders. During the special frame write cycle through SDI line, the TMAG5170D-Q1 will continue to send the two channel data through SDO line as defined by the DATA_TYPE register bits.



* With DATA_TYPE = 000b, the SDO will deliver '0's in the 16-bit register data during the same frame
** With DATA_TYPE ≠ 000b, the SDO will continue to deliver two channel data during either read or write frame

図 6-11. 32-Bit Write Frame

7 Application and Implementation

注

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7.1 Application Information

7.1.1 Selecting the Sensitivity Option

Select the highest TMAG5170D-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC output range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the TMAG5170-Q1 product folder on ti.com.

7.1.2 Temperature Compensation for Magnets

The TMAG5170D-Q1 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG_TEMPCO register bits. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG_TEMPCO bit to default 00b if the device temperature compensation is not needed.

7.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG_CH_EN, CONV_AVG, DIAG_SEL, and DIAG_EN register bit settings.

7.1.3.1 Continuous Conversion

The TMAG5170D-Q1 can be set in continuous conversion mode when OPERATING_MODE is set to 010b. 図 7-1 shows few examples of continuous conversion. The input magnetic field is processed in two steps. In the first step the device spins the hall sensor elements, and integrates the sampled data. In the second step, the ADC block converts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing another magnetic sample. The temperature data is taken at the beginning of each new conversion. This temperature data is used to compensate for the magnetic thermal drift.

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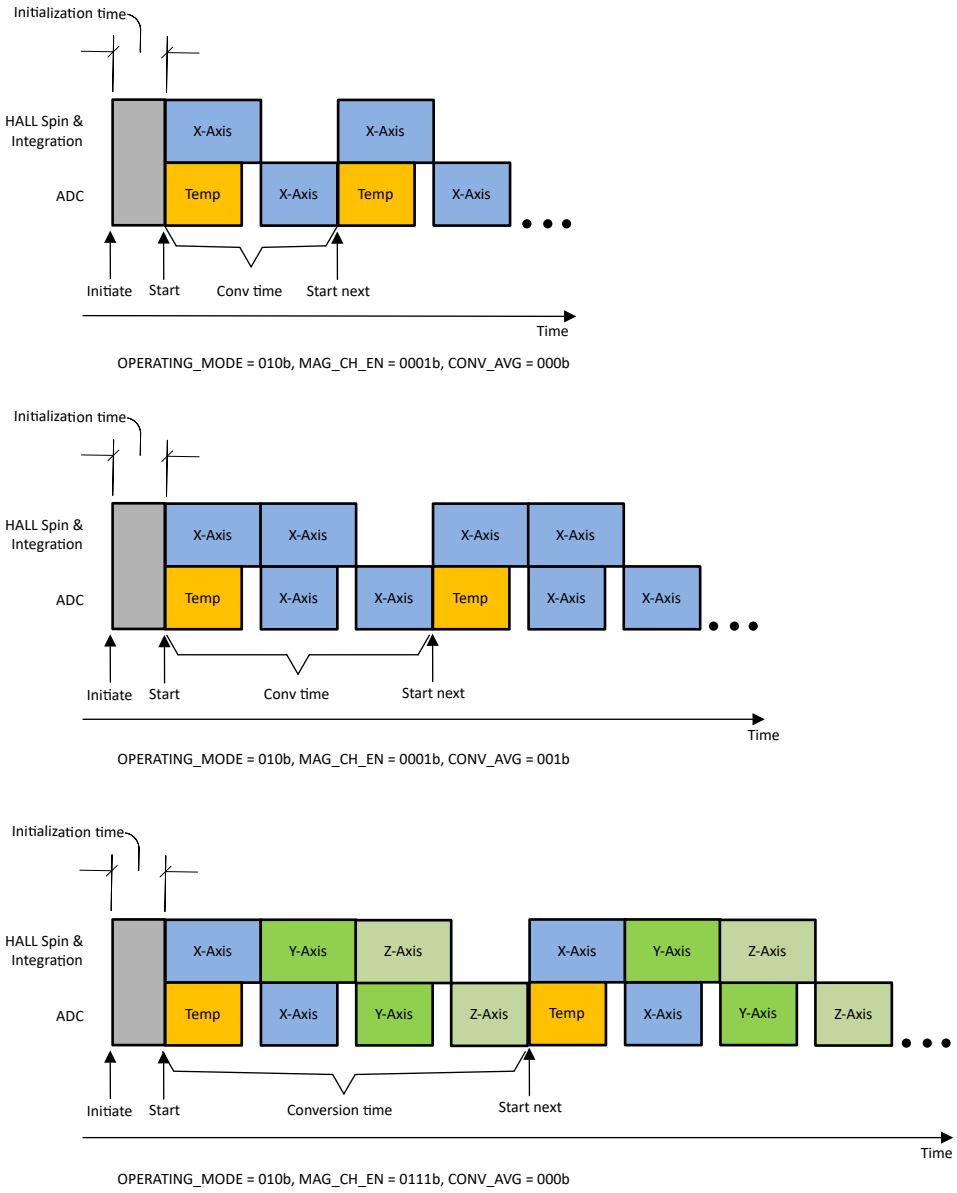


図 7-1. Continuous Conversion Examples

7.1.3.2 Trigger Conversion

The TMAG5170D-Q1 supports trigger conversion with OPERATING_MODE set to 000b, 001b, or 011b. During trigger conversion, the initialization time can vary depending on the operating mode (see 表 6-3). The trigger event can be initiated through a SPI command, $\overline{\text{ALERT}}$, or $\overline{\text{CS}}$ signal. 図 7-2 shows an example of trigger conversion with X, Y, Z, and temperature sensors activated.

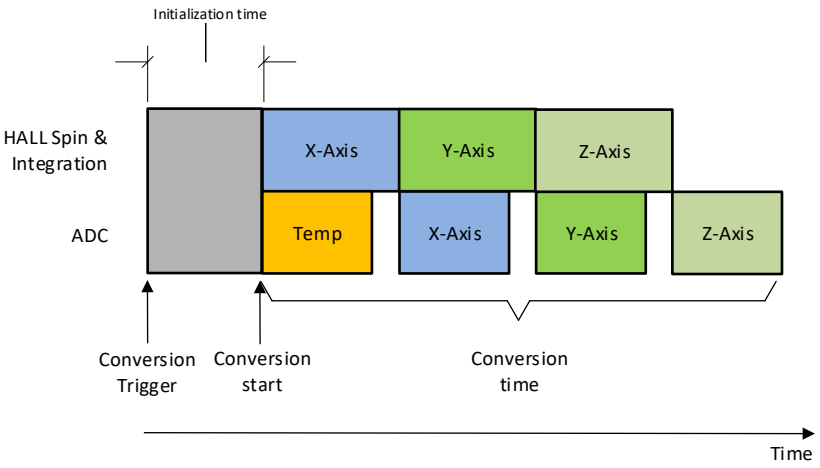


図 7-2. Trigger Conversion for X, Y, Z, and Temperature Sensors

7.1.3.3 Pseudo-Simultaneous Sampling

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5170D-Q1 offers pseudo-simultaneous sampling data collection modes to eliminate this error. 図 7-3 shows an example where MAG_CH_EN is set at 1101b to collect XZX data. 式 7 shows that the time stamps for the X and Z sensor data are the same.

$$t_Z = \frac{t_{X1} + t_{X2}}{2} \tag{7}$$

where

- t_{X1}, t_Z, t_{X2} are time stamps for X, Z, X sensor data completion as defined in 図 7-3.

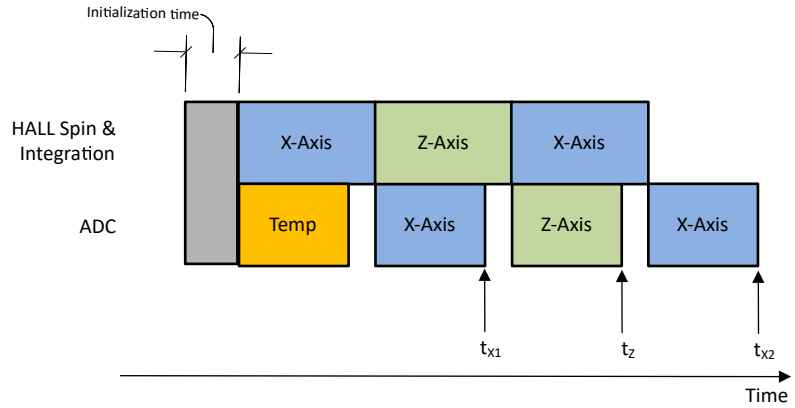


図 7-3. XZX Magnetic Field Conversion

The vertical X, Y sensors of the TMAG5170D-Q1 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

7.1.4 Error Calculation During Linear Measurement

The TMAG5170D-Q1 offers independent configurations to perform linear position measurements in X, Y, and Z axes. To calculate the expected error during linear measurement, the contributions from each of the individual error sources must be understood. The relevant error sources include sensitivity error, offset, noise, cross axis sensitivity, hysteresis, nonlinearity, drift across temperature, drift across life time, and so forth. For a 3-axis Hall

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solution like the TMAG5170D-Q1, the cross-axis sensitivity and hysteresis error sources are insignificant. Use 式 8 to estimate the linear measurement error calculation at room temperature.

$$\text{Error}_{\text{LM_25C}} = \frac{\sqrt{(\text{B} \times \text{SENS}_{\text{ER}})^2 + \text{B}_{\text{off}}^2 + \text{N}_{\text{RMS_25}}^2}}{\text{B}} \times 100\% \quad (8)$$

where

- $\text{Error}_{\text{LM_25C}}$ is total error in % during linear measurement at 25°C.
- B is input magnetic field.
- SENS_{ER} is sensitivity error at 25°C.
- B_{off} is offset error at 25°C.
- $\text{N}_{\text{RMS_25}}$ is RMS noise at 25°C.

In many applications, system level calibration at room temperature can nullify the offset and sensitivity errors at 25°C. The noise errors can be reduced by further digital averaging the sensor data in a microcontroller. Use 式 9 to estimate the linear measurement error across temperature after calibration at room temperature.

$$\text{Error}_{\text{LM_Temp}} = \frac{\sqrt{(\text{B} \times \text{SENS}_{\text{DR}})^2 + \text{B}_{\text{off_DR}}^2 + \text{N}_{\text{RMS_Temp}}^2}}{\text{B}} \times 100\% \quad (9)$$

where

- $\text{Error}_{\text{LM_Temp}}$ is total error in % during linear measurement across temperature after room temperature calibration.
- B is input magnetic field.
- SENS_{DR} is sensitivity drift from value at 25°C.
- $\text{B}_{\text{off_DR}}$ is offset drift from value at 25°C.
- $\text{N}_{\text{RMS_Temp}}$ is RMS noise across temperature.

If room temperature calibration is not performed, sensitivity and offset errors at room temperature must also account for total error calculation across temperature (see 式 10).

$$\text{Error}_{\text{LM_Temp_NCal}} = \frac{\sqrt{(\text{B} \times \text{SENS}_{\text{ER}})^2 + (\text{B} \times \text{SENS}_{\text{DR}})^2 + \text{B}_{\text{off}}^2 + \text{B}_{\text{off_DR}}^2 + \text{N}_{\text{RMS_Temp}}^2}}{\text{B}} \times 100\% \quad (10)$$

where

- $\text{Error}_{\text{LM_Temp_NCal}}$ is total error in % during linear measurement across temperature without room temperature calibration.

7.1.5 Error Calculation During Angular Measurement

The TMAG5170D-Q1 offers on-chip CORDIC to measure angle data from any of the two magnetic axes. The linear magnetic axis data can be used to calculate the angle using an external CORDIC as well. To calculate the expected error during angular measurement, the contributions from each individual error source must be understood. The relevant error sources include sensitivity error, offset, noise, axis-axis mismatch, nonlinearity, drift across temperature, drift across life time, and so forth. Use the Angle Error Calculation Tool to estimate the total error during angular measurement.

7.2 Typical Application

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5170D-Q1 offers an on-chip angle calculator that can provide angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers an angle output in complete 360

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degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

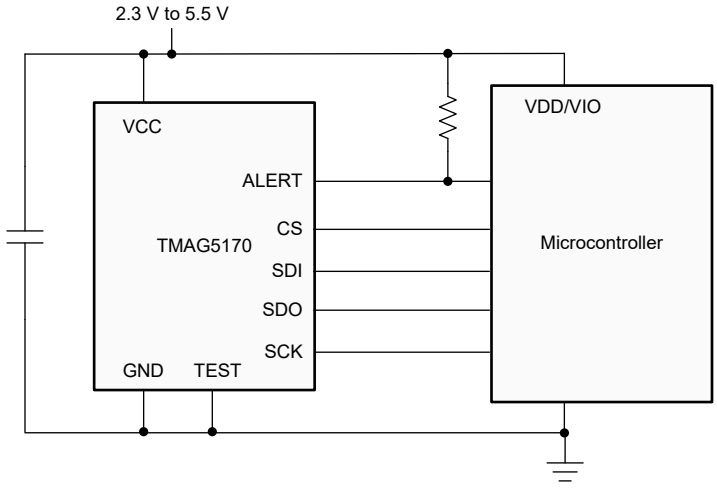


図 7-4. TMAG5170D-Q1 Application Diagram

7.2.1 Design Requirements

Use the parameters listed in 表 7-1 for this design example

表 7-1. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5170-A1	TMAG5170-A1
VCC	5 V	5 V
Magnet	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<1° for 360° rotation	<1° for 360° rotation

7.2.1.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in 図 7-5. Select the on-axis measurement topology whenever possible, as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5170D-Q1 offers an on-chip gain adjustment option to account for mechanical position misalignments.

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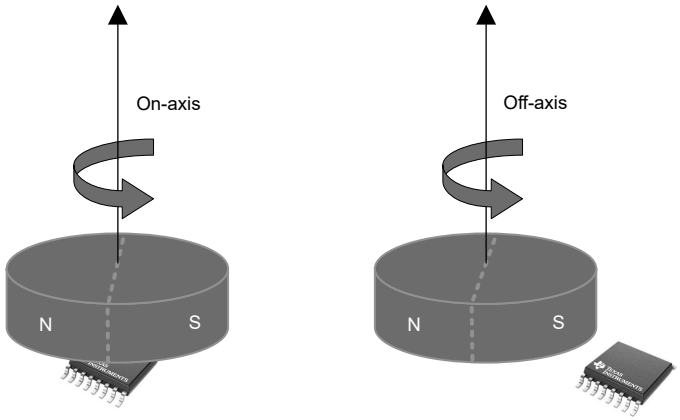


図 7-5. On-Axis vs. Off-Axis Angle Measurements

7.2.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG_GAN_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

1. Set the device at 32x average mode and rotate the shaft a full 360 degree.
2. Record the two axes sensor ADC codes for the full 360 degree rotation.
3. Measure the maximum peak-peak ADC code delta for each axis, Ax and Ay, as shown in 図 7-6 or 図 7-7.
4. Calculate the gain adjustment value for X axis:

$$G_X = \frac{A_Y}{A_X} \quad (11)$$

5. If G_X>1, apply the gain adjustment value to Y axis:

$$G_Y = \frac{1}{G_X} \quad (12)$$

6. Calculate the target binary gain setting at the GAIN_VALUE register bits:

$$G_X \text{ or } G_Y = GAIN_VALUE_{decimal} / 1024 \quad (13)$$

Example 1: If A_X = A_Y = 60,000, the GAIN_SELECTION resister bits can be set as 00b. The GAIN_VALUE register bits are don't care bits in this case.

Example 2: If A_X= 60,000, A_Y = 45,000, the G_X = 45,000/60,000 =0.75. Select 01b for the GAIN_SELECTION register bits.

Example 3: If A_X= 45,000, A_Y = 60,000, the G_X = (60,000/45,000) =1.33. Since G_X >1, the gain adjustment needs to be applied to Y axis with G_Y =1/G_X. Select 10b for the GAIN_SELECTION register bits.

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7.2.3 Application Curves

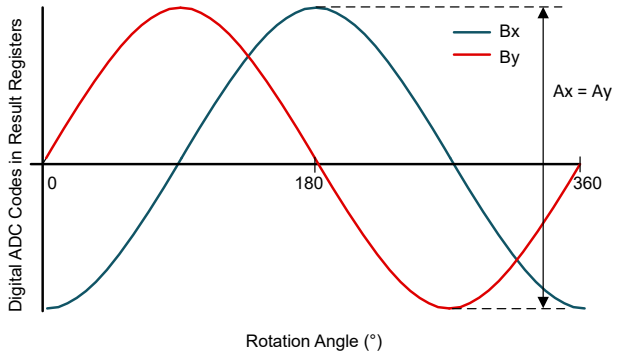


図 7-6. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement

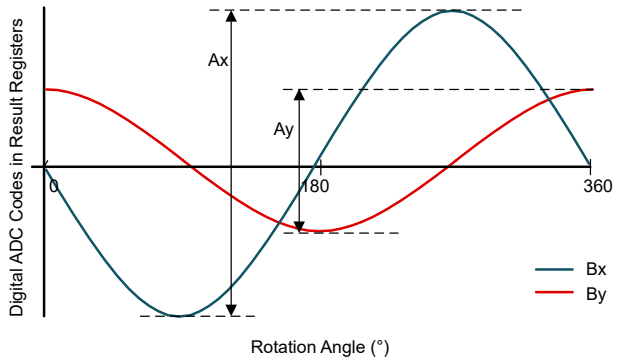
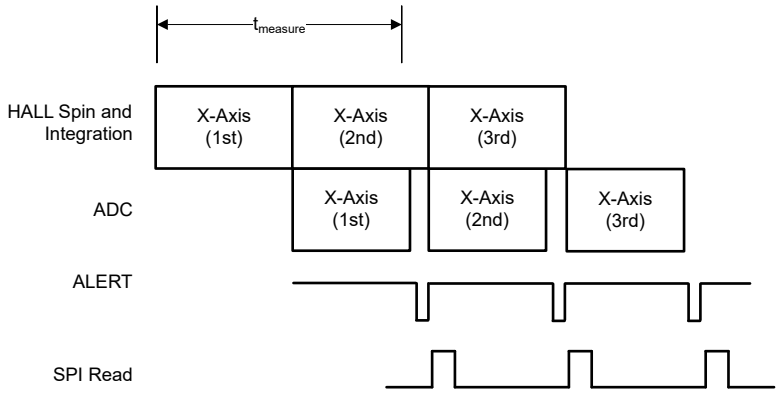


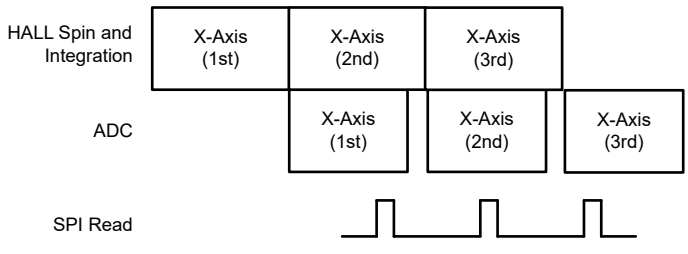
図 7-7. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement

7.3 Best Design Practices

The TMAG5170D-Q1 updates the result registers at the end of a conversion. SPI read of the result register must be synchronized with the conversion update time to ensure reading the updated result data. The conversion update time, $t_{measure}$ is defined in the *Electrical Characteristics* table. 図 7-8 shows examples of correct and incorrect SPI read timings for applications with strict timing budgets. Use the $\overline{\text{ALERT}}$ signal to notify the controller when a conversion is complete.



SPI Read Synchronized with Conversion Complete



SPI Read not Synchronized with Conversion Complete

図 7-8. SPI Read During Continuous Conversion

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7.4 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF between each VCC and GND pins. Connect the TEST pins to the respective ground planes.

7.5 Layout

7.5.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall-effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

7.5.2 Layout Example

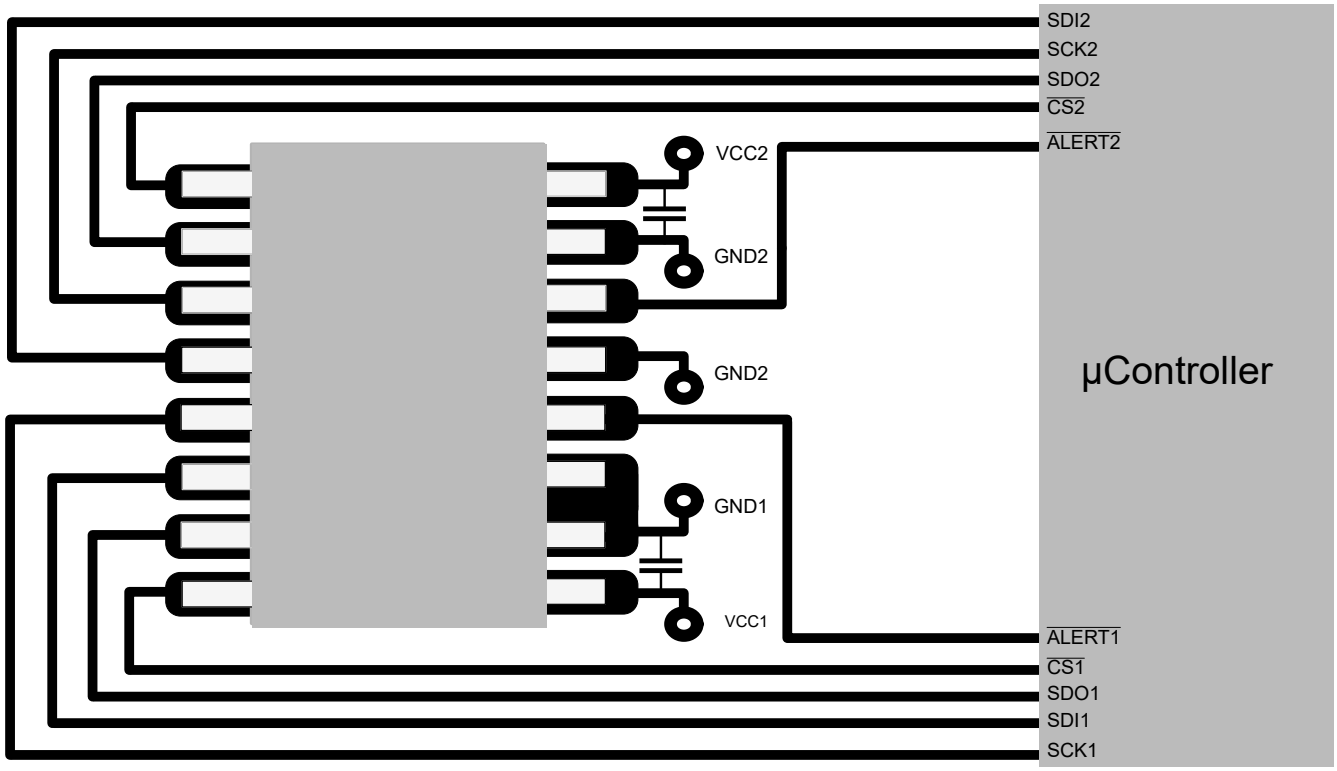


図 7-9. Layout Example With TMAG5170D-Q1

8 Register Map

All register addresses not listed should be considered as reserved locations and the register contents should not be modified.

表 8-1. TMAG5170D-Q1 Registers

Address	Type	Reset	Acronym	Register Name	Section
00h	R/W	0000h	DEVICE_CONFIG	Configure Device Operation Modes	Go
01h	R/W	0000h	SENSOR_CONFIG	Configure Device Operation Modes	Go
02h	R/W	0000h	SYSTEM_CONFIG	Configure Device Operation Modes	Go
03h	R/W	0000h	ALERT_CONFIG	Configure Device Operation Modes	Go
04h	R/W	7D83h	X_THRX_CONFIG	Configure Device Operation Modes	Go
05h	R/W	7D83h	Y_THRX_CONFIG	Configure Device Operation Modes	Go
06h	R/W	7D83h	Z_THRX_CONFIG	Configure Device Operation Modes	Go
07h	R/W	6732h	T_THRX_CONFIG	Configure Device Operation Modes	Go
08h	R/W	0000h	CONV_STATUS	Conversion Status Register	Go
09h	R	0000h	X_CH_RESULT	Conversion Result Register	Go
0Ah	R	0000h	Y_CH_RESULT	Conversion Result Register	Go
0Bh	R	0000h	Z_CH_RESULT	Conversion Result Register	Go
0Ch	R	0000h	TEMP_RESULT	Conversion Result Register	Go
0Dh	R	8000h	AFE_STATUS	Status Register	Go
0Eh	R	0000h	SYS_STATUS	Status Register	Go
0Fh	R/W	00x0h	TEST_CONFIG	Test Configuration Register	Go
10h	R	0000h	OSC_MONITOR	Conversion Result Register	Go
11h	R/W	0000h	MAG_GAIN_CONFIG	Configure Device Operation Modes	Go
12h	R/W	0000h	MAG_OFFSET_CONFIG	Configure Device Operation Modes	Go
13h	R	0000h	ANGLE_RESULT	Conversion Result Register	Go
14h	R	0000h	MAGNITUDE_RESULT	Conversion Result Register	Go

表 8-2. TMAG5170D-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.1 DEVICE_CONFIG Register (Address = 00h) [Reset = 0000h]

Return to Register Map.

表 8-3. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	CONV_AVG	R/W	0h	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution) 0h = 1x - 10.0 kSPS (3-axes) or 20 kSPS (1 axis) 1h = 2x - 5.7 kSPS (3-axes) or 13.3 kSPS (1 axis) 2h = 4x - 3.1 kSPS (3-axes) or 8.0 kSPS (1 axis) 3h = 8x - 1.6 kSPS (3-axes) or 4.4 kSPS (1 axis) 4h = 16x - 0.8 kSPS (3-axes) or 2.4 kSPS (1 axis) 5h = 32x - 0.4 kSPS (3-axes) or 1.2 kSPS (1 axis) 6h = Code not used, defaults to 000b if selected 7h = Code not used, defaults to000b if selected
11-10	RESERVED	R	0h	Reserved
9-8	MAG_TEMPCO	R/W	0h	Temperature coefficient of sense magnet 0h = 0%/ deg C (Current sensor applications) 1h = 0.12%/deg C (NdBFe) 2h = 0.03% /deg C (SmCo) 3h = 0.2%/deg C (Ceramic)
7	RESERVED	R	0h	Reserved
6-4	OPERATING_MODE	R/W	0h	Selects operating mode 0h = Configuration mode, Default (TRIGGER_MODE active) 1h = Stand-by mode (TRIGGER_MODE active) 2h = Active measure mode (Continuous conversion) 3h = Active trigger mode (TRIGGER_MODE active) 4h = Wake-up and sleep mode (duty-cycled mode) 5h = Sleep mode 6h = Deep sleep mode (wakes up at CS signal from controller) 7h = Code not used, defaults to 000b if selected
3	T_CH_EN	R/W	0h	Enables temperature compensation of the sensor data. Set this bit to '1b' for precision performance. If only temperature channel is enabled, the CONV_AVG register bits need to set at 000b. 0h = Temp channel disabled, Default 1h = Temp channel enabled
2	T_RATE	R/W	0h	Temperature conversion rate. The rate is linked to the CONV_AVG field 0h = Same as other sensors per CONV_AVG, Default 1h = Once per conversion set
1	T_HLT_EN	R/W	0h	Enables temperature limit check 0h = Temperature limit check off, Default 1h = Temperature limit check on
0	RESERVED	R	0h	Reserved

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8.2 SENSOR_CONFIG Register (Address = 01h) [Reset = 0000h]

Return to Register Map.

表 8-4. SENSOR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	ANGLE_EN	R/W	0h	Enable angle calculation using two axis data 0h = No angle calculation (default) 1h = X-Y-angle calculation enabled 2h = Y-Z-angle calculation enabled 3h = X-Z-angle calculation enabled
13:10	SLEEPTIME	R/W	0h	Selects the time spent in low power mode between conversions when OPERATING_MODE =010b 0h = 1 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms 4h = 20 ms 5h = 30 ms 6h = 50 ms 7h = 100 ms 8h = 500 ms 9h = 1000 ms Ah = Code not used, defaults to 0000b if selected Bh = Code not used, defaults to 0000b if selected Ch = Code not used, defaults to 0000b if selected Dh = Code not used, defaults to 0000b if selected Eh = Code not used, defaults to 0000b if selected Fh = Code not used, defaults to 0000b if selected
9:6	MAG_CH_EN	R/W	0h	Enables data acquisition of the magnetic axis channel(s) 0h = All magnetic channels of OFF, DEFAUT 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channels enabled 4h = Z channel enabled 5h = Z, X channels enabled 6h = Y, Z channels enabled 7h = X, Y, Z channels enabled 8h = XYX channels enabled 9h = YXY channels enabled Ah = YZY channels enabled Bh = ZYZ channels enabled Ch = ZXZ channels enabled Dh = XZX channels enabled Eh = XYZYX channels enabled Fh = XYZZYX channels enabled
5:4	Z_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from ±25 mT to ±300 mT 0h = ±50 mT (TMAG5170A1)/ ±150 mT(TMAG5170A2), Default 1h = ±25 mT (TMAG5170A1)/ ±75 mT(TMAG5170A2) 2h = ±100 mT (TMAG5170A1)/ ±300 mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected
3:2	Y_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from ±25 mT to ±300 mT 0h = ±50 mT (TMAG5170A1)/ ±150 mT(TMAG5170A2), Default 1h = ±25 mT (TMAG5170A1)/ ±75 mT(TMAG5170A2) 2h = ±100 mT (TMAG5170A1)/ ±300 mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected
1:0	X_RANGE	R/W	0h	Enables different magnetic ranges to support magnetic fields from ±25 mT to ±300 mT 0h = ±50 mT (TMAG5170A1)/ ±150 mT(TMAG5170A2), Default 1h = ±25 mT (TMAG5170A1)/ ±75 mT(TMAG5170A2) 2h = ±100 mT (TMAG5170A1)/ ±300 mT(TMAG5170A2) 3h = Code not used, defaults to 00b if selected

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SYSTEM_CONFIG Register (Address = 02h) [Reset = 0000h]

Return to Register Map.

表 8-5. SYSTEM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0h	Reserved
13:12	DIAG_SEL	R/W	0h	Selects a diagnostic mode run 0h = Run all data path diagnostics all together, Default 1h = Run only enabled data path diagnostics all together 2h = Run all data path diagnostics in sequence 3h = Run only enabled data path diagnostics in sequence
11	RESERVED	R	0h	Reserved
10:9	TRIGGER_MODE	R/W	0h	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the modes explicitly mentioned in OPERATING_MODE. 0h = Conversion start at SPI command, Default 1h = Conversion start at $\overline{CS}$ pulse 2h = Conversion start at $\overline{ALERT}$ pulse 3h = Code not used, defaults to 00b if selected
8:6	DATA_TYPE	R/W	0h	Data Type to be accessed from results registers via SPI 0h = Default 32-bit register access 1h = 12-Bit XY data access 2h = 12-Bit XZ data access 3h = 12-Bit ZY data access 4h = 12-Bit XT data access 5h = 12-Bit YT data access 6h = 12-Bit ZT data access 7h = 12-Bit AM data access
5	DIAG_EN	R/W	0h	Enables user controlled AFE diagnostic tests 0h = Execution of AFE diagnostics is disabled, Default 1h = Execution of AFE diagnostics is enabled
4:3	RESERVED	R	0h	Reserved
2	Z_HLT_EN	R/W	0h	Enables magnetic field limit check on Z axis 0h = Z axis limit check off, Default 1h = Z axis limit check on
1	Y_HLT_EN	R/W	0h	Enables magnetic field limit check on Y axis 0h = Y axis limit check off, Default 1h = Y axis limit check on
0	X_HLT_EN	R/W	0h	Enables magnetic field limit check on X axis 0h = X axis limit check off, Default 1h = X axis limit check on

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8.3 ALERT_CONFIG Register (Address = 03h) [Reset = 0000h]

Return to Register Map.

表 8-6. ALERT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0h	Reserved
13	ALERT_LATCH	R/W	0h	Latched $\overline{\text{ALERT}}$ mode select 0h = $\overline{\text{ALERT}}$ sources are not latched. $\overline{\text{ALERT}}$ is asserted only while the source of the $\overline{\text{ALERT}}$ response is present 1h = $\overline{\text{ALERT}}$ sources are latched. $\overline{\text{ALERT}}$ response is latched when the source of the $\overline{\text{ALERT}}$ is asserted until cleared on Read of the corresponding status register (AFE_STATUS, SYS_STATUS, or result registers)
12	ALERT_MODE	R/W	0h	ALERT mode select 0h = Interrupt mode 1h = Switch mode. This mode overrides any interrupt function (ALERT trigger is also disabled), and implements Hall switch function based off the *_THRX_ALRT settings. In the switch mode the corresponding X_HLT_EN, Y_HLT_EN, Z_HLT_EN need to be set.
11	STATUS_ALRT	R/W	0h	Enable $\overline{\text{ALERT}}$ response when any flag in the AFE_STATUS or SYS_STATUS registers are set 0h = $\overline{\text{ALERT}}$ is not asserted when any of the AFE_STATUS or SYS_STATUS bit is set 1h = $\overline{\text{ALERT}}$ output is asserted when any of the AFE_STATUS or SYS_STATUS bit is set
10:9	RESERVED	R	0h	Reserved
8	RSLT_ALRT	R/W	0h	Enable $\overline{\text{ALERT}}$ response when the configured set of conversions is complete 0h = $\overline{\text{ALERT}}$ is not used to signal when the configured set of conversions are complete 1h = $\overline{\text{ALERT}}$ output is asserted when the configured set of conversions are complete
7:6	RESERVED	R	0h	Reserved
5:4	THRX_COUNT	R/W	0h	Number of conversions above the HIGH threshold or below the LOW threshold before the $\overline{\text{ALERT}}$ response is initiated 0h = 1-Conversion result 1h = 2-Conversion results 2h = 3-Conversion results 3h = 4-Conversion results
3	T_THRX_ALRT	R/W	0h	Temperature threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when temperature thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when temperature thresholds are crossed
2	Z_THRX_ALRT	R/W	0h	Z-Channel threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when Z-Axis magnetic thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when Z-Axis magnetic thresholds are crossed
1	Y_THRX_ALRT	R/W	0h	Y-Channel threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when Y-Axis magnetic thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when Y-Axis magnetic thresholds are crossed
0	X_THRX_ALRT	R/W	0h	X-Channel threshold $\overline{\text{ALERT}}$ enable 0h = $\overline{\text{ALERT}}$ is not used to signal when X-Axis magnetic thresholds are crossed 1h = $\overline{\text{ALERT}}$ output is asserted when X-Axis magnetic thresholds are crossed

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8.4 X_THRX_CONFIG Register (Address = 04h) [Reset = 7D83h]

Return to Register Map.

表 8-7. X_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	X_HI_THRESHOLD	R/W	7Dh	X-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (X_RANGE/128)*X_HI_THRESHOLD. Default to 98% of the full-scale
7:0	X_LO_THRESHOLD	R/W	83h	X-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (X_RANGE/128)*X_LO_THRESHOLD. Default to -98% of the full-scale

Y_THRX_CONFIG Register (Address = 05h) [Reset = 7D83h]

Return to Register Map.

表 8-8. Y_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Y_HI_THRESHOLD	R/W	7Dh	Y-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (Y_RANGE/128)*Y_HI_THRESHOLD. Default to 98% of the full-scale.
7:0	Y_LO_THRESHOLD	R/W	83h	Y-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (Y_RANGE/128)*Y_LO_THRESHOLD. Default to -98% of the full-scale.

Z_THRX_CONFIG Register (Address = 06h) [Reset = 7D83h]

Return to Register Map.

表 8-9. Z_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Z_HI_THRESHOLD	R/W	7Dh	Z-Axis maximum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as:(Z_RANGE/128)*Z_HI_THRESHOLD. Default to 98% of the full-scale
7:0	Z_LO_THRESHOLD	R/W	83h	Z-Axis minimum magnetic field threshold. User input as 2's complement 8-bit binary number. The threshold in mT can be calculated as: (Z_RANGE/128)*X_LO_THRESHOLD. Default to -98% of the full-scale

T_THRX_CONFIG Register (Address = 07h) [Reset = 6732h]

Return to Register Map.

表 8-10. T_THRX_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	T_HI_THRESHOLD	R/W	67h	Temperature maximum threshold. User input as 2's complement 8-bit binary number. Each LSB in this field corresponds to 4.267°C. Default value of 67h represents 172°C.
7:0	T_LO_THRESHOLD	R/W	32h	Temperature minimum threshold. User input as 2's complement 8-bit binary number. Each LSB in this field corresponds to 4.267°C. Default value of 32h represents -53°C.

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CONV_STATUS Register (Address = 08h) [Reset = 0000h]

Return to Register Map.

表 8-11. CONV_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0h	Reserved
13	RDY	R	0h	Conversion data buffer is ready. 0h = Conversion data not valid (result registers hold previous conversion value) 1h = Conversion data valid
12	A	R	0h	Angle/Magnitude data from current conversion 0h = Data is not current 1h = Data is current
11	T	R	0h	Temperature data from current conversion 0h = Temperature data is not current 1h = Temperature data is current
10	Z	R	0h	Z-Channel data from current conversion 0h = Z-Channel data is not current 1h = Z-Channel data is current
9	Y	R	0h	Y-Channel data from current conversion 0h = Y-Channel data is not current 1h = Y-Channel data is current
8	X	R	0h	X-Channel data from current conversion 0h = X-Channel data is not current 1h = X-Channel data is current
7	RESERVED	R	0h	Reserved
6:4	SET_COUNT	R	0h	Rolling count of conversion data sets
3:2	RESERVED	R	0h	Reserved
1:0	ALRT_STATUS	R	0h	State of $\overline{\text{ALERT}}$ response 0h = No $\overline{\text{ALERT}}$ conditions 1h = AFE status flag set 2h = SYS status flag set 3h = Flags set in both AFE and SYS status registers

X_CH_RESULT Register (Address = 09h) [Reset = 0000h]

Return to Register Map.

表 8-12. X_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	X_CH_RESULT	R	0000h	X-Channel data conversion results

Y_CH_RESULT Register (Address = 0Ah) [Reset = 0000h]

Return to Register Map.

表 8-13. Y_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Y_CH_RESULT	R	0000h	Y-Channel data conversion results

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8.5 Z_CH_RESULT Register (Address = 0Bh) [Reset = 0000h]

Return to Register Map.

表 8-14. Z_CH_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Z_CH_RESULT	R	0000h	Z-Channel data conversion results

TEMP_RESULT Register (Address = 0Ch) [Reset = 0000h]

Return to Register Map.

表 8-15. TEMP_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TEMP_RESULT	R	0000h	Temperature sensor data conversion results

AFE_STATUS Register (Address = 0Dh) [Reset = 8000h]

Return to Register Map.

表 8-16. AFE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_RESET	RC	1h	Device power up status. This bit is reset when microcontroller reads the AFE_STATUS register. 0h = Device reset has been acknowledged and cleared 1h = Device has experienced a hardware reset after a power down or brown-out
14:13	RESERVED	R	0h	Reserved
12	SENS_STAT	RC	0h	Analog front end sensor diagnostic status 0h = No error detected 1h = Analog front end sensor diagnostic test failed
11	TEMP_STAT	RC	0h	Temperature sensor diagnostic status 0h = No error detected 1h = Analog front end temperature sensor diagnostic test failed
10	ZHS_STAT	RC	0h	Z-Axis hall sensor diagnostic status 0h = No error detected 1h = Z-Axis hall sensor diagnostic test failed
9	YHS_STAT	RC	0h	Y-Axis hall sensor diagnostic status 0h = No error detected 1h = Y-Axis hall sensor diagnostic test failed
8	XHS_STAT	RC	0h	X-Axis hall sensor diagnostic status 0h = No error detected 1h = X-Axis hall sensor diagnostic test failed
7:2	RESERVED	R	0h	Reserved
1	TRIM_STAT	RC	0h	Trim data error 0h = No trim data errors were detected 1h = Trim data error was detected
0	LDO_STAT	RC	0h	LDO error 0h = No faults in the internal LDO supplied power were detected 1h = A fault in the internal LDO supplied power was detected

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8.6 SYS_STATUS Register (Address = 0Eh) [Reset = 0000h]

Return to Register Map.

表 8-17. SYS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALRT_LVL	R	0h	Reflects the current state of the $\overline{\text{ALERT}}$ pin feed-back path 0h = The input $\overline{\text{ALERT}}$ logic level is low 1h = The input $\overline{\text{ALERT}}$ logic level is high
14	ALRT_DRV	RC	0h	Each time the open drain $\overline{\text{ALERT}}$ signal is driven, the feedback circuit checks if the $\overline{\text{ALERT}}$ output goes Low. An error flag is generated at the ALRT_DRV bit if the output does not go Low. 0h = No $\overline{\text{ALERT}}$ drive error detected 1h = $\overline{\text{ALERT}}$ drive error detected
13	SDO_DRV	RC	0h	The Logic value driven output on SDO was not the value of the SDO Pin Feed-back path when SDO is being driven by the device 0h = No SDO drive error detected 1h = SDO drive error detected
12	CRC_STAT	RC	0h	Cyclic redundancy check error 0h = No cyclic redundancy check error was detected 1h = Cyclic redundancy check error was detected for a SPI transaction
11	FRAME_STAT	RC	0h	Incorrect number of clocks in SPI frame 0h = No frame error was detected 1h = Incorrect number of clocks detected for a SPI transaction
10:8	OPERATING_STAT	R	0h	Reports the status of operating mode 0h = Config state 1h = Standby state 2h = Active measure (Continuous Mode) state 3h = Active triggered mode state 4h = DCM active state 5h = DCM Sleep state 6h = Sleep state
7:6	RESERVED	R	0h	Reserved
5	VCC_OV	RC	0h	VCC over-voltage detection in active or stand-by mode 0h = No over-voltage detected on VCC 1h = VCC was detected to be over-voltage
4	VCC_UV	RC	0h	VCC under voltage detection in active or stand-by mode 0h = No under-voltage was detected on VCC 1h = VCC was detected to be under-voltage
3	TEMP_THX	RC	0h	Temperature threshold crossing detected 0h = No temperature threshold crossing detected 1h = Temperature threshold crossing detected
2	ZCH_THX	RC	0h	Z-Channel threshold crossing detected 0h = No Z-Axis magnetic field threshold crossing detected 1h = Z-Axis magnetic field threshold crossing detected
1	YCH_THX	RC	0h	Y-Channel threshold crossing detected 0h = No Y-Axis magnetic field threshold crossing detected 1h = Y-Axis magnetic field threshold crossing detected
0	XCH_THX	RC	0h	X-Channel threshold crossing detected 0h = No X-Axis magnetic field threshold crossing detected 1h = X-Axis magnetic field threshold crossing detected

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8.7 TEST_CONFIG Register (Address = 0Fh) [Reset = 00x0]

Return to Register Map.

表 8-18. TEST_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R	001h	Reserved
5:4	VER	R	xh	Indicates the version of the device 0h = A1 rev 1h = A2 rev 2h = reserved 3h = reserved
3	RESERVED	R	0h	Reserved
2	CRC_DIS	R/W	0h	Enable or disable CRC in SPI communication 0h = CRC enabled in SPI communication (Default) 1h = CRC disabled in SPI communication
1:0	OSC_CNT_CTL	R/W	0h	Oscillator count control - starts, stops, and resets the counter driven by the HFOSC or LFOSC oscillator to facilitate oscillator frequency and integrity checks 0h = Reset OSC counter (default) 1h = Start OSC counter driven by HFOSC 2h = Start OSC counter driven by LFOSC 3h = Stop OSC counter

OSC_MONITOR Register (Address = 10h) [Reset = 0000h]

Return to Register Map.

表 8-19. OSC_MONITOR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OSC_COUNT	R	0000h	Oscillator Counter. The number of selected oscillator clock cycles that have been counted since Oscillator Counter was started. The HFOSC and LFOSC clock roll-over the 16-bit counter once reaching the max value.

MAG_GAIN_CONFIG Register (Address = 11h) [Reset = 0000h]

Return to Register Map.

表 8-20. MAG_GAIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	GAIN_SELECTION	R/W	0h	Enables the selection of a particular Hall axis for amplitude correction to get accurate angle measurement 0h = No axis is selected (Default) 1h = X-axis is selected 2h = Y-axis is selected 3h = Z-axis is selected
13:11	RESERVED	R	0h	Reserved
10:0	GAIN_VALUE	R/W	000h	11-bit gain value determined by controller to adjust the a particular Hall axis value. The gain value is anywhere between 0 and 2. Gain is calculated as 'user entered value/1024'.

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8.8 MAG_OFFSET_CONFIG Register (Address = 12h) [Reset = 0000h]

Return to Register Map.

表 8-21. MAG_OFFSET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	OFFSET_SELECTION	R/W	0h	Enables the selection of a particular Hall axis for offset correction to get accurate angle measurement: 00b = No axis is selected for offset correction (Default). 01b = Only OFFSET_VALUE1 is used for offset correction. Applied to X axis when ANGLE_EN = 01b or 11b, and to Y axis when ANGLE_EN =10b. No axis is selected if ANGLE_EN =00b. 10b = Only OFFSET_VALUE2 is used for offset correction. Applied to Y axis when ANGLE_EN = 01b, and to Z axis when ANGLE_EN =10b or 11b. No axis is selected if ANGLE_EN =00b. 11b = Both OFFSET_VALUE1 and OFFSET_VALUE2 are used for offset correction. OFFSET_VALUE1 applied to X axis when ANGLE_EN = 01b or 11b, and to Y axis when ANGLE_EN =10b. OFFSET_VALUE2 applied to Y axis when ANGLE_EN = 01b, and to Z axis when ANGLE_EN =10b or 11b. No axis is selected if ANGLE_EN =00b.
13:7	OFFSET_VALUE1	R/W	00h	7-bit, 2' complement offset value determined by controller to adjust a particular Hall axis value. The range of possible offset valid entries can be +/-64. The offset value is calculated from the user input as the 7 LSB bits of a 11-bit range per SENSOR_CONFIG register setting for the corresponding axis. Default offset value is 0.
6:0	OFFSET_VALUE2	R/W	00h	7-bit, 2' complement offset value determined by controller to adjust a particular Hall axis value. The range of possible offset valid entries can be +/-64. The offset value is calculated from the user input as the 7 LSB bits of a 11-bit range per SENSOR_CONFIG register setting for the corresponding axis. Default offset value is 0.

ANGLE_RESULT Register (Address = 13h) [Reset = 0000h]

Return to Register Map.

表 8-22. ANGLE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R	0h	Reserved
12:2	ANGLE_RESULT[10:0]	R	000h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 11 LSB bits. The LSB size is 0.25°
1:0	Reserved	R	0h	Reserved

MAGNITUDE_RESULT Register (Address = 14h) [Reset = 0000h]

Return to Register Map.

表 8-23. MAGNITUDE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MAGNITUDE_RESULT	R	0000h	Resultant vector magnitude (during angle measurement) result. This value should be constant during 360 degree measurements

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9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2023) to Revision A (December 2023)	Page
• データシート ステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMAG5170DA1EPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	5170DA1
TMAG5170DA1EPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	5170DA1
TMAG5170DA2EPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	5170DA2
TMAG5170DA2EPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	5170DA2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

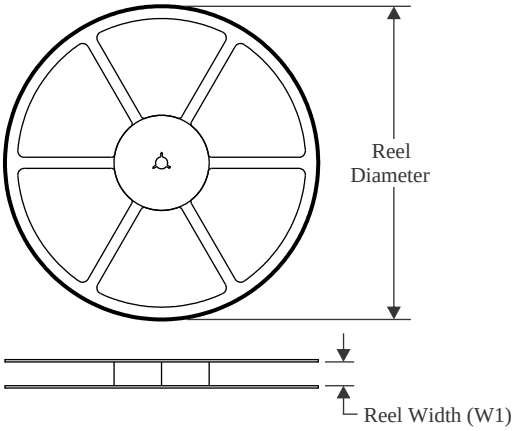
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

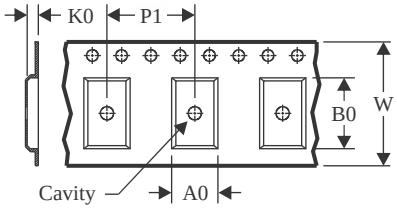
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

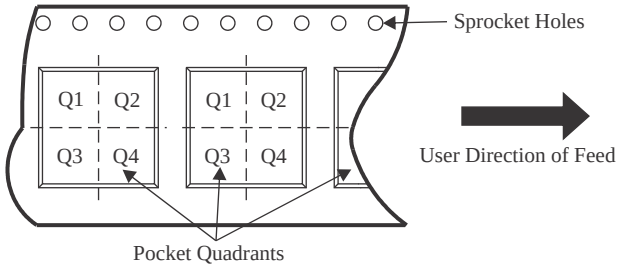


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

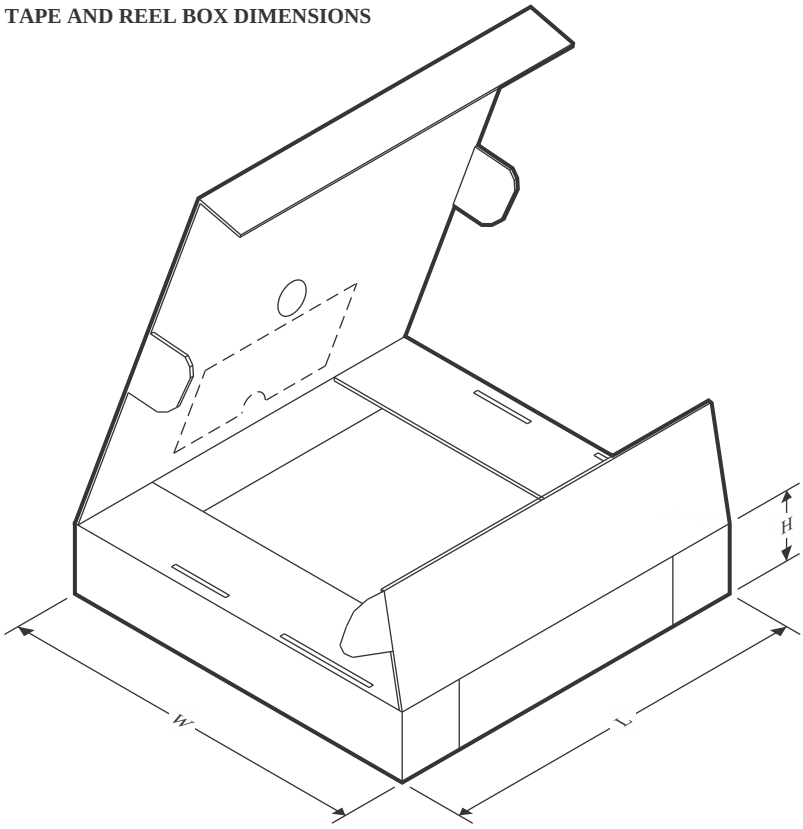
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMAG5170DA1EPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
TMAG5170DA2EPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

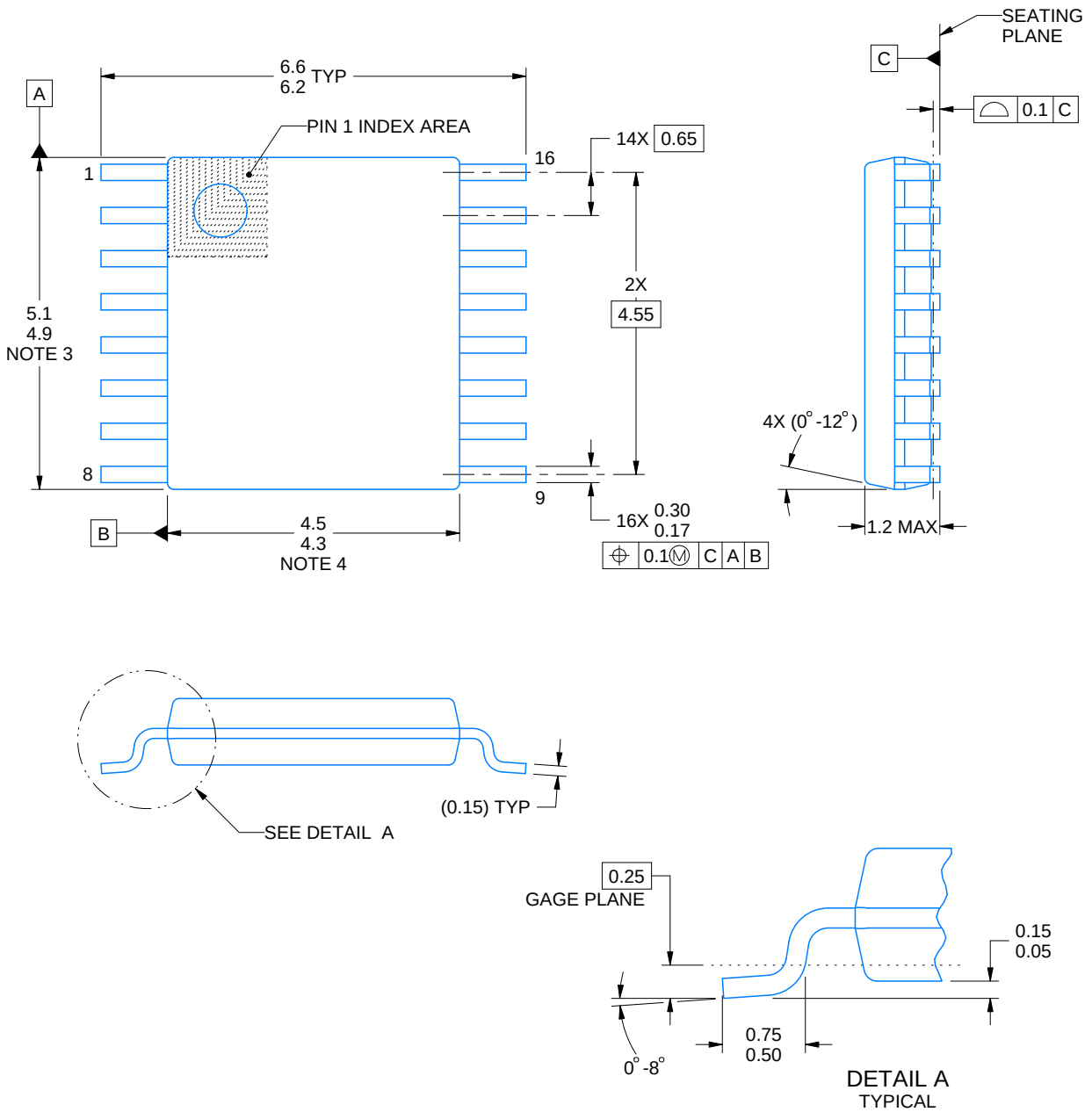
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMAG5170DA1EPWRQ1	TSSOP	PW	16	2000	340.0	340.0	38.0
TMAG5170DA2EPWRQ1	TSSOP	PW	16	2000	340.0	340.0	38.0

PACKAGE OUTLINE

PW0016A

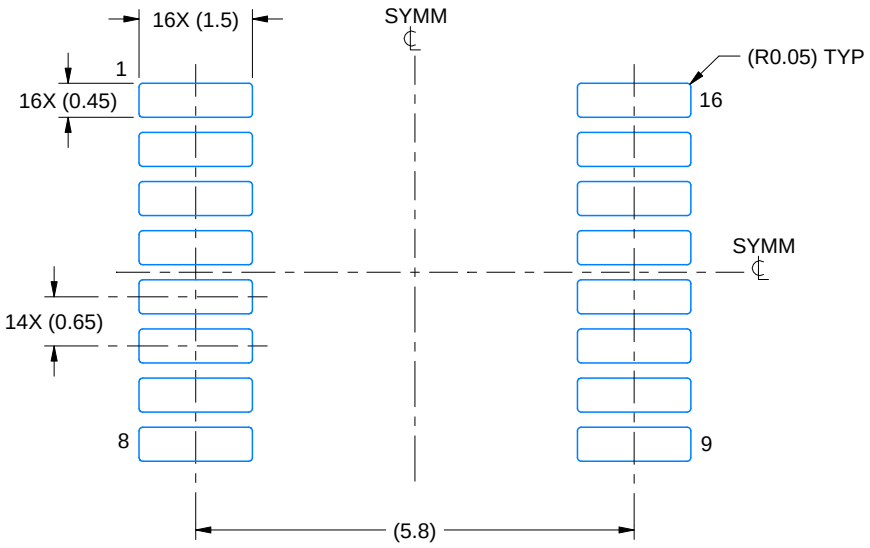
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

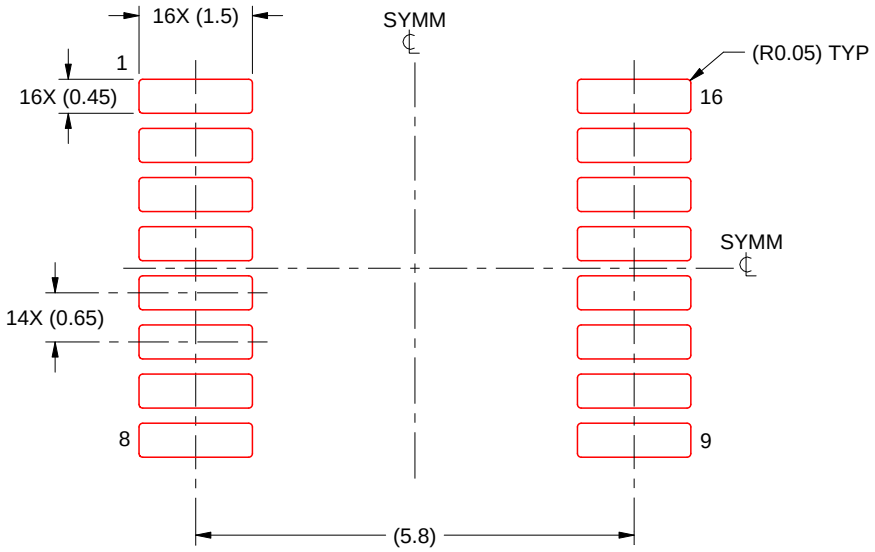


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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