TEXAS INSTRUMENTS
TMP116, TMP116N
JAJSDF4A – MAY 2017 – REVISED MAY 2019

TMP116 高精度、低消費電力、デジタル温度センサ SMBus および I²C 互換インターフェイス搭載

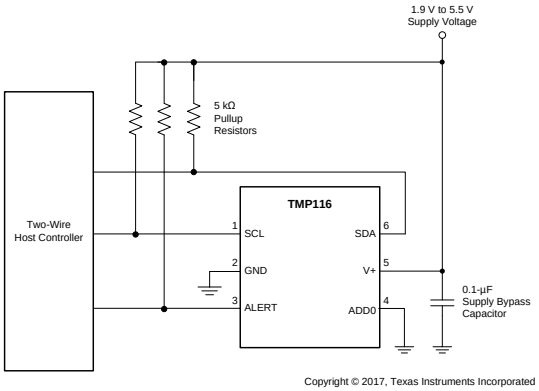
1 特長

- TMP116 の較正なしでの精度
  - -10°C～+85°C の範囲で±0.2°C (最大値)
  - -40°C～+105°C の範囲で±0.25°C (最大値)
  - +105°C～+125°Cの範囲で±0.3°C (最大値)
- TMP116N の精度 (較正不要)
  - -25°C～+85°C の範囲で±0.3°C (最大値)
  - -40°C～+125°C の範囲で±0.4°C (最大値)
- 低い静止電流
  - 1Hz の変換サイクルで 3.5µA
  - 250nA のシャットダウン電流
- 電源電圧範囲：1.9V～5.5V
- 分解能：0.0078°C で 16 ビット (1 LSB)
- 温度アラート制限をプログラム可能
- 平均化を選択可能
- 汎用 EEPROM：64 ビット
- NIST トレース可能
- SMBus™および I²C インターフェイスとの互換性

2 アプリケーション

- 医療用グレード：ASTM および ISO 仕様に合致
- 環境監視およびサーモスタット
- ウェアラブル
- アセットの追跡およびコールド・チェーン
- ガス・メータおよび熱メータ
- 試験 / 測定機器
- RTD の代替：PT100、PT500、PT1000
- 熱電対の冷接点補償

概略回路図



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3 概要

TMP116 (TMP116、TMP116N) は、EEPROM メモリが内蔵された低消費電力、高精度温度センサのファミリです。TMP116 は較正不要で、温度の測定結果を 16 ビット、分解能 0.0078℃、精度 ±0.2℃ で報告します。TMP116 は I²C および SMBus™ インターフェイス互換で、アラート機能をプログラムでき、単一のバスにより最大 4 つのデバイスをサポートできます。

TMP116の消費電流は最小限で、パワーセービング機能も搭載されているため、自己発熱が最小限で、測定精度が向上します。TMP116は1.9V～5.5Vで動作し、標準の消費電力は3.5µAです。

TMP116は-55℃～+125℃の温度範囲で動作し、この温度範囲にわたってClass A RTDを超える精度を実現し、PT100 RTDの一般的な励起電流の1/5未満の電流しか消費しません。TMP116はRTDよりも使いやすく、較正、外付け回路、配線のマッチング、ケルビン接続が不要です。

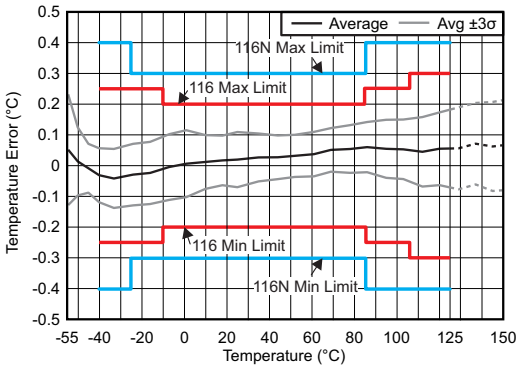
TMP116ユニットは製造時のセットアップで100%テスト済みであり、このテストはNISTトレース可能で、ISO/IEC 17025で認められた標準に対して較正済みの機器により検証されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TMP116	WSON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

温度精度



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目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Two-Wire Interface Timing ... 6
6.7 Typical Characteristics ... 7
7 **Detailed Description** ... 10
7.1 Overview ... 10
7.2 Functional Block Diagrams ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 12
7.5 Programming ... 17
7.6 Registers Map ... 24
8 **Application and Implementation** ... 32
8.1 Application Information ... 32
9 **Power Supply Recommendations** ... 36
10 **Layout** ... 36
10.1 Layout Guidelines ... 36
10.2 Layout Example ... 38
11 デバイスおよびドキュメントのサポート ... 39
11.1 ドキュメントのサポート ... 39
11.2 ドキュメントの更新通知を受け取る方法 ... 39
11.3 コミュニティ・リソース ... 39
11.4 商標 ... 39
11.5 静電気放電に関する注意事項 ... 39
11.6 Glossary ... 39
12 メカニカル、パッケージ、および注文情報 ... 40

4 改訂履歴

2017年5月発行のものから更新 **Page**

- 特長に「*平均化を選択可能*」を追加 ... 1
- Added thermal mass parameter to the *Thermal Information* table ... 4
- Added tablenote to the temperature cycling and hysteresis parameter ... 5
- Added TI recommendation to not solder the thermal pad to the PCB in the *Layout Guidelines* section ... 36

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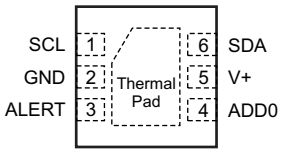
5 Pin Configuration and Functions

DRV Package
6-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCL	I	Serial clock
2	GND	—	Ground
3	ALERT	O	Overtemperature alert or data-ready signal. Open-drain output; requires a pullup resistor if used.
4	ADD0	I	Address select. Connect to GND, V+, SDA, or SCL.
5	V+	I	Supply voltage: 1.9 V to 5.5 V
6	SDA	I/O	Serial data input and open-drain output; requires a pullup resistor.

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6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Supply voltage, V+	–0.3	6	V
Voltage at SCL, SDA, ALERT, and ADD0	–0.3	6	V
Operating junction temperature, T_J	–55	150	°C
Storage temperature, T_{stg}	–65	150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.9	3.3	5.5	V
T_A	Operating free-air temperature	–55		150	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP116 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.6	°C/W
M_T	Thermal Mass	5.1	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

minimum and maximum specifications are over –55°C to +125°C and V+ = 1.9 V to 5.5 V (unless otherwise noted); typical specifications are at T_A = 25°C and V+ = 3.3 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE-TO-DIGITAL CONVERTER							
	Temperature accuracy(1)	TMP116	–10°C to +85°C, V+ = 3.3 V	–0.2	±0.1	0.2	°C
			–40°C to +105°C, V+ = 3.0 V to 3.6 V	–0.25	±0.2	0.25	
			+105°C to +125°C, V+ = 3.0 V to 3.6 V	–0.3	±0.25	0.3	
			–40°C to +125°C, V+ = 1.9 V to 5.5 V(2)	–0.4	±0.3	0.4	
		TMP116N	–25°C to +85°C, V+ = 3.3 V	–0.3	±0.2	0.3	
			–40°C to +125°C, V+ = 3.0 V to 3.6 V	–0.4	±0.3	0.4	
			–40°C to +125°C V+ = 1.9 V to 5.5 V(2)	–0.5	±0.4	0.5	
	DC power-supply sensitivity		One-shot mode, 8 averages, T_A = 25°C	0	20	55	m°C/V
	Temperature resolution (LSB)				7.8125		m°C
	Repeatability(3)		V+ = 3.3 V, 8 averages, 1-Hz sampling		±1		LSB
	Long-term stability and drift		300 hours at 150°C(4)		±0.02		°C
	Temperature cycling and hysteresis(1)(5)				±1		LSB
DIGITAL INPUT/OUTPUT							
	Input capacitance				3		pF
V_{IH}	Input logic high level			0.7 (V+)			V
V_{IL}	Input logic low level					0.3 (V+)	V
I_{IN}	Input current			–0.2		0.2	µA
$V_{OL}S$	SDA output logic low level		I_{OL} = –3 mA	0		0.4	V
$V_{OL}A$	$\overline{\text{ALERT}}$ output logic low level		I_{OL} = –3 mA	0		0.4	V
POWER SUPPLY							
I_Q	Quiescent current		Active conversion, serial bus inactive		135	220	µA
			1-Hz conversion cycle, averaging mode off, serial bus inactive, 25°C		3.5	4.5	
			1-Hz conversion cycle, 8 averages mode, serial bus inactive, 25°C		16	22	
			1-Hz conversion cycle, averaging mode off, serial bus active, SCL frequency = 400 kHz		21		
I_{SB}	Standby current(6)		Serial bus inactive, SCL and SDA = V+, 25°C		1.25	2.1	µA
I_{SD}	Shutdown current		Serial bus inactive, SCL and SDA = V+, 25°C		0.25	0.5	µA
			Serial bus inactive, SCL and SDA = V+, 125°C			8.5	
			Serial bus active, SCL frequency = 400 kHz		17		
I_{EE}	EEPROM write quiescent current		ADC conversion off; serial bus inactive		240		µA
V_{POR}	Power-on-reset threshold voltage		V+ rising		1.6		V
	Brownout detect		V+ falling		1.1		V
	Reset time		Time required by device to reset		1.5		ms
	Active conversion time		1 conversion	13.5	15.5	17	ms

(1) 8 averages, 1-Hz conversion cycle. Measurements are taken in oil bath.
(2) ±0.75°C maximum error between –55°C to –40°C.
(3) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(4) Long-term stability is determined using accelerated operational life testing at a junction temperature of 150°C.
(5) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room → hot → room → cold → room. The temperatures used for this test are –40°C, 25°C, and 125°C.
(6) Quiescent current between conversions.

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Electrical Characteristics (continued)

minimum and maximum specifications are over –55°C to +125°C and V+ = 1.9 V to 5.5 V (unless otherwise noted); typical specifications are at T_A = 25°C and V+ = 3.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EEPROM					
Programming time			7		ms
Number of writes		1,000	50,000		Times
Data retention time		10	100		Years

6.6 Two-Wire Interface Timing

minimum and maximum specifications are over –55°C to 125°C and V+ = 1.9 V to 5.5 V (unless otherwise noted); typical specifications are at T_A = 25°C and V+ = 3.3 V; values are based on statistical analysis of samples tested during initial release

		MIN	MAX	UNIT
f_{SCL}	SCL operating frequency	1	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	1300		ns
$t_{HD;STA}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		ns
$t_{SU;STA}$	Repeated START condition setup time	600		ns
$t_{SU;STO}$	STOP condition setup time	600		ns
$t_{HD;DAT}$	Data hold time	0		ns
$t_{VD;DAT}$	Data valid time (1)		0.9	µs
$t_{SU;DAT}$	Data setup time	100		ns
t_{LOW}	SCL clock low period	1300		ns
t_{HIGH}	SCL clock high period	600		ns
t_F – SDA	Data fall time	20 × (V+ / 5.5)	300	ns
t_F, t_R – SCL	Clock fall and rise time		300	ns
t_R	Rise time for SCL ≤ 100 kHz		1000	ns
	Serial bus timeout (SDA bus released if there is no clock)	20	40	ms

(1) $t_{VD;DATA}$ = time for data signal from SCL low to SDA output (high to low, depending on which is worse).

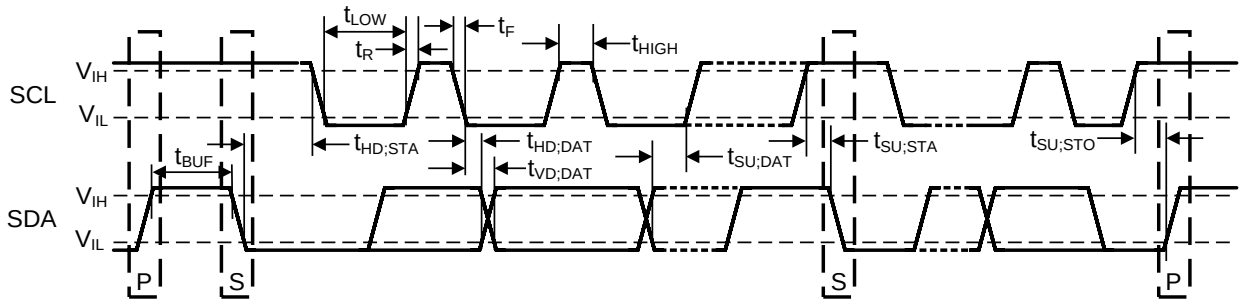

図 1. Two-Wire Timing Diagram

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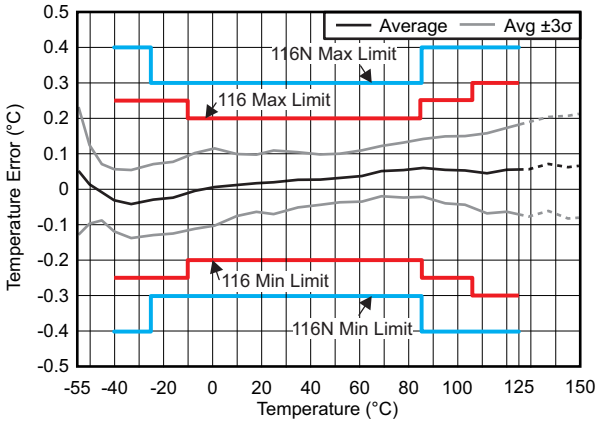
6.7 Typical Characteristics

at T_A = 25°C, V+ = 3.3 V, and measurement taken in oil bath (unless otherwise noted)



1-Hz conversion cycle, 8 averages mode

図 2. Temperature Error vs Temperature

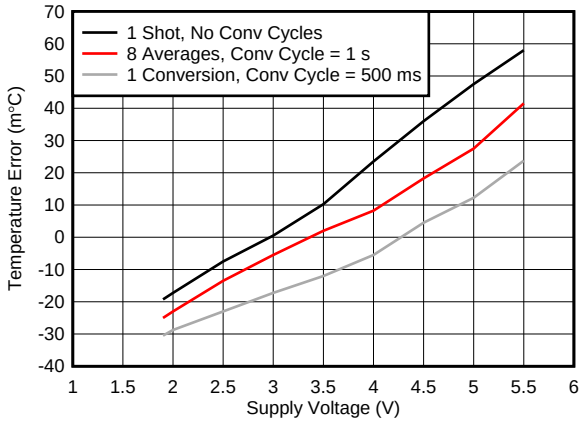
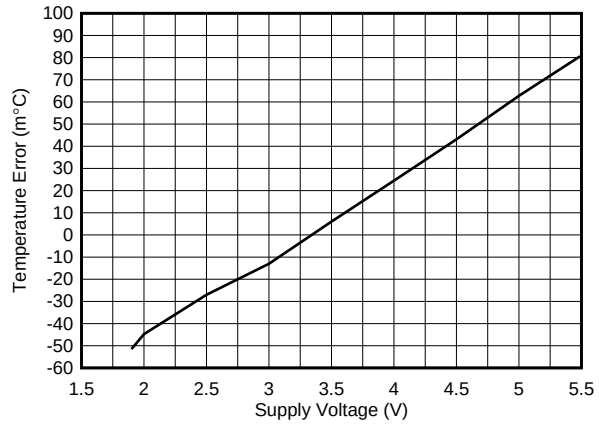


図 3. Temperature Error vs Supply Voltage



Continuous conversion, no conversion cycle normalized to 3.3V

図 4. Temperature Error vs Supply Voltage in still air

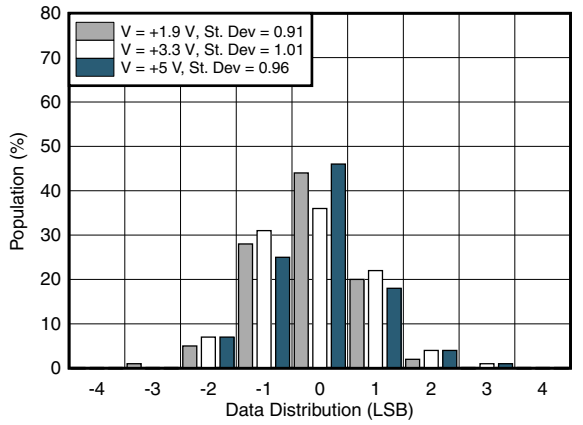


図 5. Data Reading Distribution Over Supply Voltage (No Averaging)

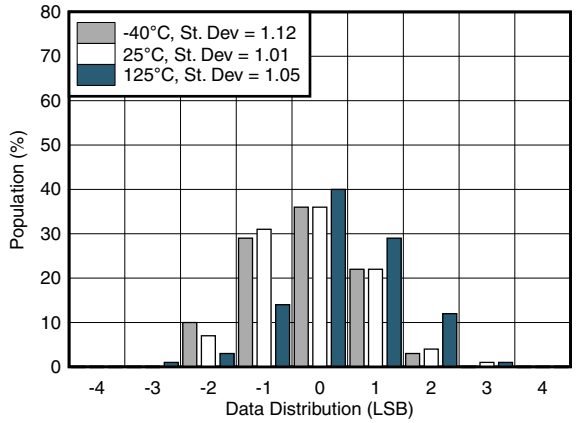


図 6. Data Reading Distribution Over Temperature (No Averaging)

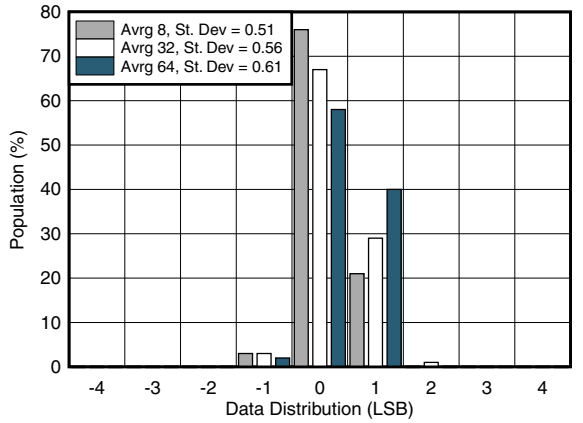


図 7. Data Reading Distribution Over Averaging Number

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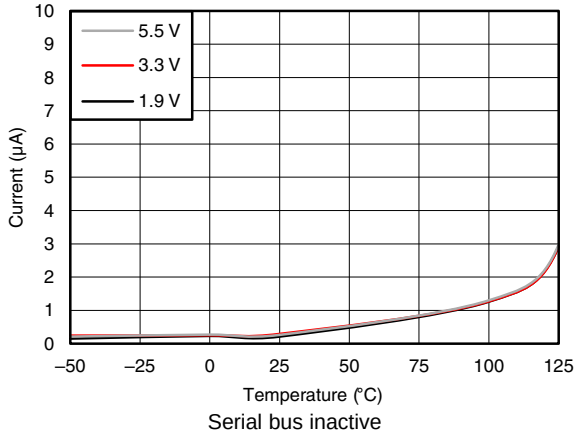
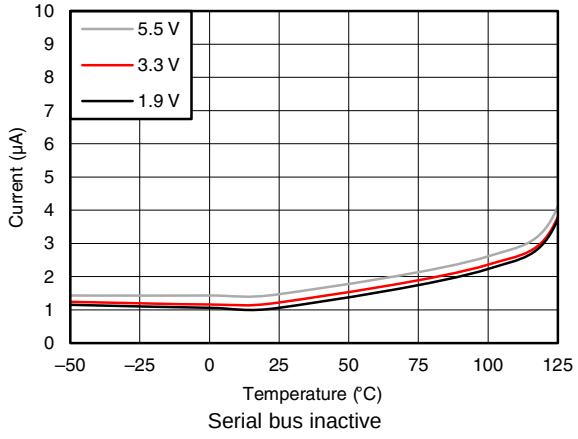
Typical Characteristics (continued)

at T_A = 25°C, V+ = 3.3 V, and measurement taken in oil bath (unless otherwise noted)



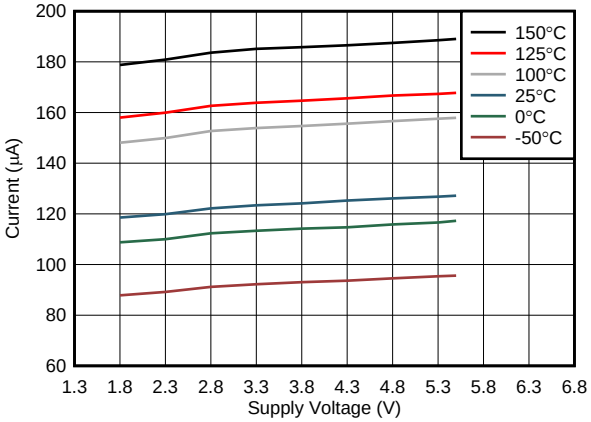
Serial bus inactive

図 8. Quiescent Current in Shutdown Mode



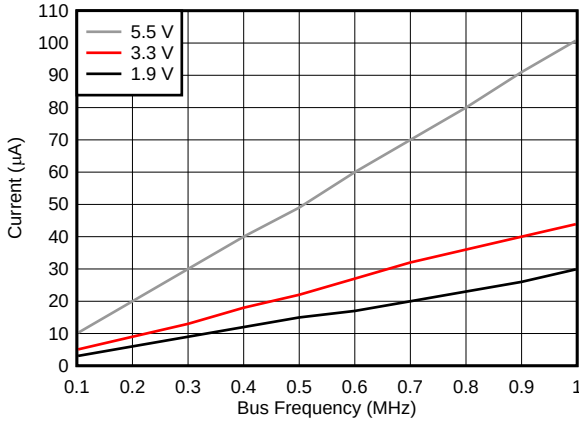
Serial bus inactive

図 9. Quiescent Current in Standby Mode



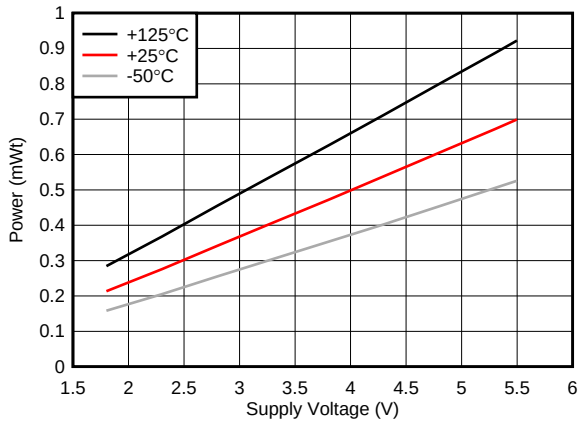
Continuous conversion mode, serial bus inactive

図 10. Quiescent Current During Active Conversion



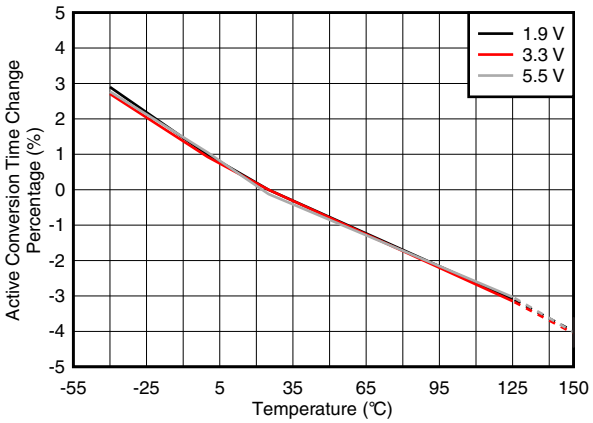
SCL, SDA, ADD0 pins are constantly clocked

図 11. Quiescent Current in Shutdown Mode



Serial bus inactive

図 12. Power Consumption During Active Conversion



Normalized to 25°C and V+ = 3.3 V

図 13. Active Conversion Time vs Temperature

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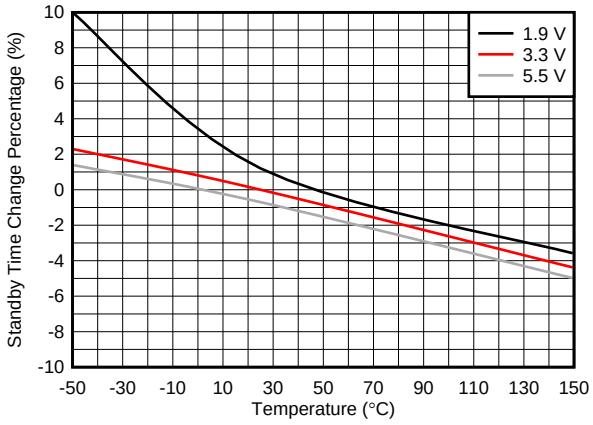
Typical Characteristics (continued)

at T_A = 25°C, V+ = 3.3 V, and measurement taken in oil bath (unless otherwise noted)



Normalized to 25°C and V+ = 3.3 V

図 14. Standby Time vs Temperature

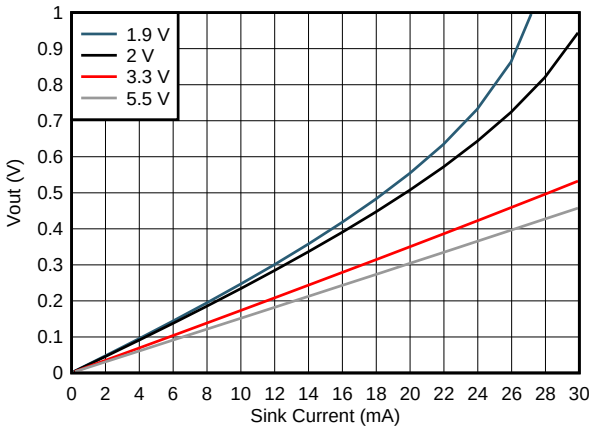
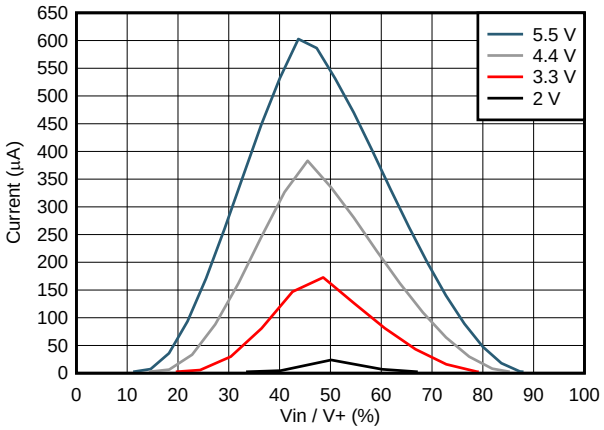


図 15. ALERT Pin Output Voltage vs Pin Sink Current



Input voltage of SCL, SDA, or ADD0 pin

図 16. Supply Current vs Input Cell Input Voltage

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7 Detailed Description

7.1 Overview

The TMP116 is a digital output temperature sensor that is optimal for thermal-management and thermal-protection applications. The TMP116 is two-wire, SMBus, and I^2C interface-compatible. The device is specified over an operating temperature range of –55°C to +125°C. 図 17 shows a block diagram of the TMP116. 図 18 shows the ESD protection circuitry contained in the TMP116.

7.2 Functional Block Diagrams

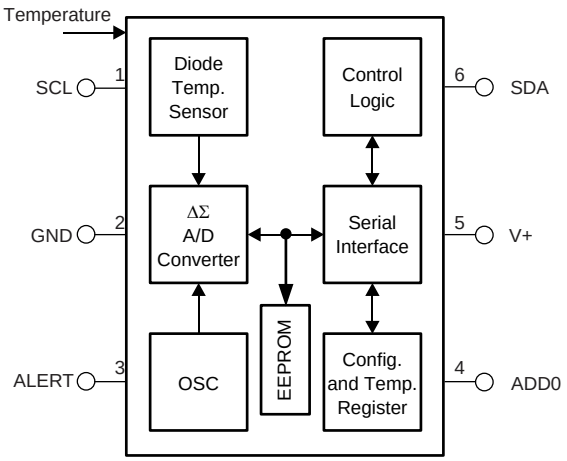

図 17. Internal Block Diagram

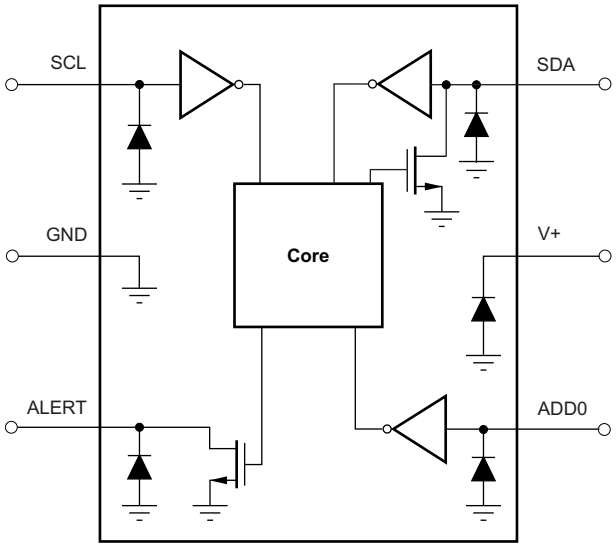

図 18. Equivalent Internal ESD Circuitry

7.3 Feature Description

7.3.1 Power Up

After the supply voltage reaches within the operating range, the device requires 1.5 ms to power up before conversions begin. The device can be programmed to startup in shutdown mode as well; see the *EEPROM Programming* section. The temperature register stores –256°C before the first conversion end.

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Feature Description (continued)

7.3.2 Temperature Result and Limits

At the end of every conversion or averaging cycle, the device updates the temperature register with the conversion result. The data reading in the result register is in two's complement format, has a data width of 16 bits, and a resolution of 7.8125 m°C. 表 1 shows multiple examples of possible binary data that can be read from the temperature result register and the corresponding hexadecimal and decimal equivalents.

The TMP116 also has alert status flags and alert pin functionality that use the temperature limits stored in the low limit register and high limit register. The alert registers use the same data format as the temperature register.

表 1. 16-Bit Temperature Data Format

TEMPERATURE (°C)	TEMPERATURE REGISTER VALUE (0.0078125°C RESOLUTION)	
	BINARY	HEX
–256	1000 0000 0000 0000	8000
–25	1111 0011 1000 0000	F380
–0.1250	1111 1111 1111 0000	FFF0
–0.0078125	1111 1111 1111 1111	FFFF
0	0000 0000 0000 0000	0000
0.0078125	0000 0000 0000 0001	0001
0.1250	0000 0000 0001 0000	0010
1	0000 0000 1000 0000	0080
25	0000 1100 1000 0000	0C80
100	0011 0010 0000 0000	3200
255.9921	0111 1111 1111 1111	7FFF

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7.4 Device Functional Modes

7.4.1 Temperature Conversions

The TMP116 can be configured to operate in various conversion modes by using the MOD[1:0] bits. These modes provide flexibility to operate the device in the most power efficient way required for the intended application.

7.4.1.1 Conversion Cycle

When the device is operating in continuous conversion mode (see the *Continuous Conversion Mode (CC)* section), every conversion cycle consists of an active conversion period followed by a standby period. During active conversion the device typically consumes 135 µA, and during the low-power standby period the device typically consumes 1.25 µA, as indicated in 表 1. 図 19 shows a current consumption profile of a conversion cycle. The duration of the active conversion period and standby period can be configured using the CONV[2:0] and AVG[1:0] bits in the configuration register, thereby allowing the average current consumption of the device to be optimized based on the application requirements. Changing the conversion cycle period also affects the temperature result update rate because the temperature result register is updated at the end of every conversion or averaging cycle.

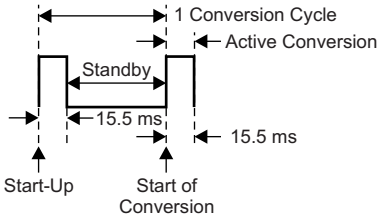

図 19. Conversion Cycle Timing Diagram

7.4.1.2 Averaging

Noise in the conversion result can be reduced by configuring the device to report the average of multiple temperature conversions using the AVG[1:0] bits. When the TMP116 is configured to perform averaging, the device executes the configured number of conversions while accumulating the results and reports the average of all conversion results at the end of the process. As illustrated in the noise histograms of 図 6 and 図 7, the temperature result output has a repeatability of approximately ±3 LSBs when there is no averaging and ±1 LSB when the device is configured to perform eight averages or higher. As illustrated in 図 20, this improvement in noise performance is achieved with the tradeoff of an increase in the active conversion time in a conversion cycle, thereby increasing the average active current consumption. For example, a single active conversion typically takes 15.5 ms so if the device is configured to report an average of eight conversions then the active conversion time is 124 ms (15.5 ms × 8). Use 式 1 to factor in this increase in active conversion time to accurately calculate the average current consumption of the device. The average current consumption of the device can be decreased by increasing the amount of time the device spends in standby period as compared to active conversion. Under the factory EEPROM settings, the device is configured to report an average of eight conversions with a conversion cycle time of 1 second.

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Device Functional Modes (continued)

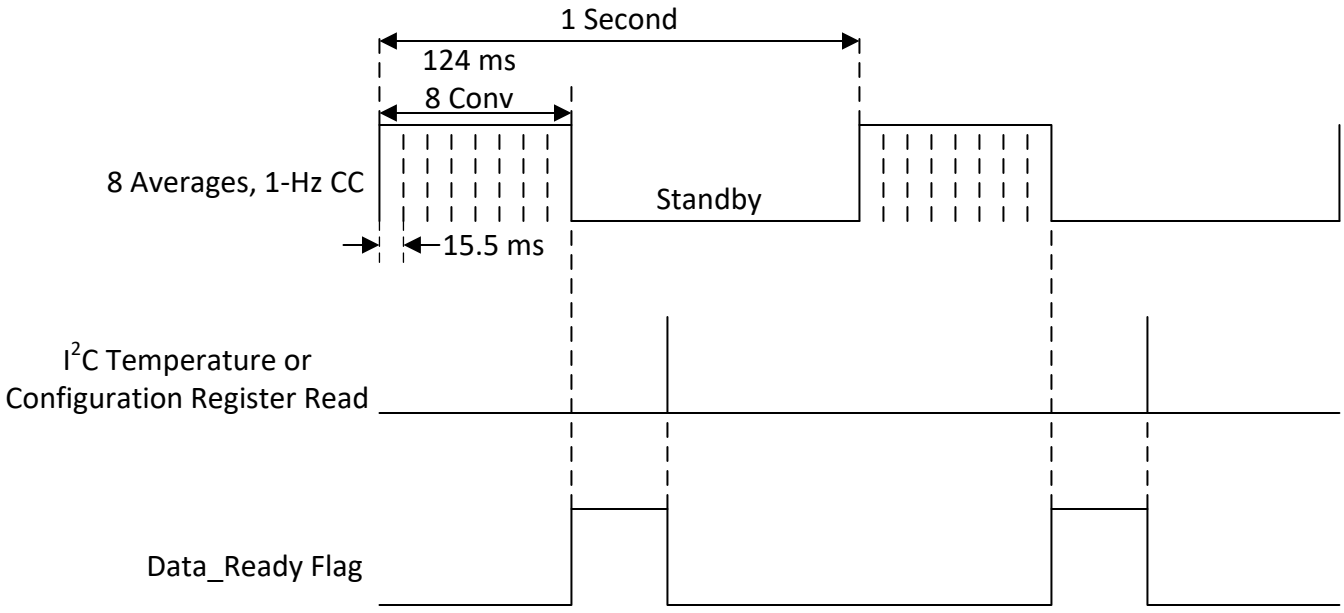

図 20. Averaging Timing Diagram

Use 式 1 to calculate the average current consumption of the device in continuous mode.

$$\frac{(\text{Active Current Consumption} \times \text{Active Conversion Time}) + (\text{Standby Current Consumption} \times \text{Standby Time})}{\text{Conversion Cycle Time}} \quad (1)$$

7.4.1.3 Continuous Conversion Mode (CC)

When the MOD[1:0] bits are set to 00, the TMP116 operates in continuous conversion mode. In this mode, the device continuously performs temperature conversions as illustrated in 図 19 and updates the temperature result register at the end of every conversion or averaging cycle. As described in the *Conversion Cycle* section, every conversion cycle consists of an active conversion period followed by a standby period whose duration can be configured using the CONV and AVG bits in the configuration register. The configuration is based on the temperature accuracy, power consumption, and temperature update rate. At the end of a conversion, the Data_Ready flag in the configuration register is set. The Data_Ready flag is cleared by reading the configuration register or the temperature result register. The state of the Data_Ready flag can also be monitored on the ALERT pin by setting the DR/nAlert_EN bit in the configuration register.

7.4.1.4 Shutdown Mode (SD)

When 01 is written to the MOD bits in the configuration register, the device instantly aborts the currently running conversion and enters a low-power shutdown mode. In this mode, the device powers down all active circuitry. In SD mode, the device typically consumes only 250 nA, which makes the TMP116 suitable for low-power consumption applications, such as battery-operated systems.

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Device Functional Modes (continued)

7.4.1.5 One-Shot Mode (OS)

When in shutdown mode, a single conversion can be performed by writing 11 to MOD bits in the configuration register, referred to as a one-shot conversion. After completing a one-shot conversion, the device returns to the low-power shutdown mode. A one-shot conversion cycle only consists of active conversion time and no standby period unlike CC mode. Thus, the duration of a one-shot conversion is only affected by the settings in the AVG bits. 図 21 shows a timing diagram for this mode with an AVG setting of 00 and 図 22 shows a timing diagram for this mode with an AVG setting of 01. At the end of a one-shot conversion, the Data_Ready flag in the configuration register is set. The Data_Ready flag is cleared by read of the configuration register or temperature result register. The state of the Data_Ready flag can also be monitored on the ALERT pin by setting the DR/nAlert_EN bit in the configuration register.

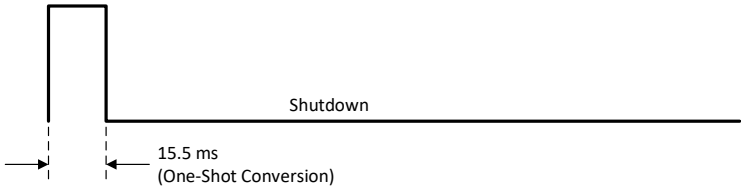

図 21. One-Shot Timing Diagram With No Averaging

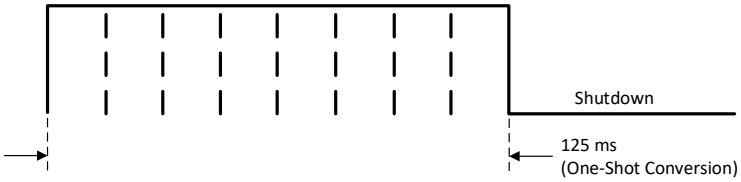

図 22. One-Shot Timing Diagram With 8 Averages

7.4.2 Therm and Alert Modes

The TMP116 can be used to detect if the temperature has crossed a certain temperature limit or if the device is within a certain temperature range by using the therm or alert functions built into the device. At the end of every conversion, the TMP116 compares the converted temperature result to the values stored in the low limit register and high limit register and sets or clears the corresponding status flags in the configuration register, as described in this section.

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Device Functional Modes (continued)

7.4.2.1 Alert Mode

When the T/nA bit in the configuration register is set to 0, the device is in alert mode. In this mode, the device compares the conversion result at the end of every conversion with the values in the low limit register and high limit register. If the temperature result exceeds the value in the high limit register, the HIGH_Alert status flag in the configuration register is set. On the other hand, if the temperature result is lower than the value in the low limit register, the LOW_Alert status flag in the configuration register is set. As shown in 図 23, in alert mode the status flags can be cleared by performing an I^2C read of the configuration register.

Configuring the device in alert mode also affects the behaviour of the ALERT pin. In this mode, the device asserts the ALERT pin when either the HIGH_Alert or the LOW_Alert status flag is set as shown in 図 23. The ALERT pin can be deasserted by either performing an I^2C read of the configuration register (which also clears the status flags) or by performing an SMBus alert response command (see the *SMBus Alert Function* section). The polarity of the ALERT pin can be changed by using the POL bit setting in the configuration register.

This mode effectively makes the device behave like a window limit detector and can be used in applications where detecting if the temperature goes outside of the specified range is needed.

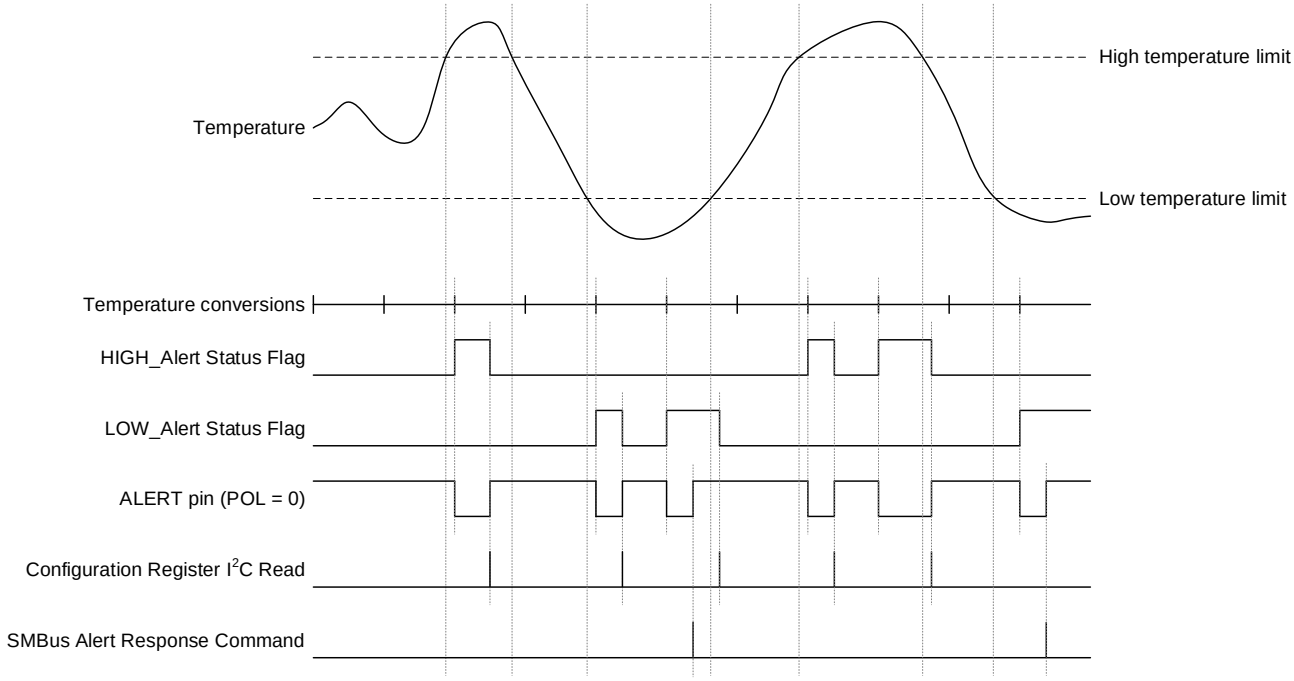

図 23. Alert Mode Timing Diagram

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Device Functional Modes (continued)

7.4.2.2 Therm Mode

When the T/nA bit in the configuration register is set to 1 the device is in therm mode. In this mode, the device compares the conversion result at the end of every conversion with the values in the low limit register and high limit register and sets the HIGH_Alert status flag in the configuration register if the temperature exceeds the value in the high limit register. When set, the device clears the HIGH_Alert status flag if the conversion result goes below the value in the low limit register. Thus, the difference between the high and low limits effectively acts like a hysteresis. In this mode, the LOW_Alert status flag is disabled and always reads 0. Unlike the alert mode, I^2C reads of the configuration register do not affect the status bits. The HIGH_Alert status flag is only set or cleared at the end of conversions based on the value of the temperature result compared to the high and low limits.

As in alert mode, configuring the device in therm mode also affects the behaviour of the ALERT pin. In this mode, the device asserts the ALERT pin if the HIGH_Alert status flag is set and deasserts the ALERT pin when the HIGH_Alert status flag is cleared. In therm mode, the ALERT pin cannot be cleared by performing an I^2C read of the configuration register or by performing an SMBus alert response command. As in alert mode, the polarity of the active state of the ALERT pin can be changed by using the POL bit setting in the configuration register.

Thus, this mode effectively makes the device behave like a high-limit threshold detector and can be used in applications where detecting if the temperature has gone above a desired threshold is needed. 図 24 shows a timing diagram of this mode.

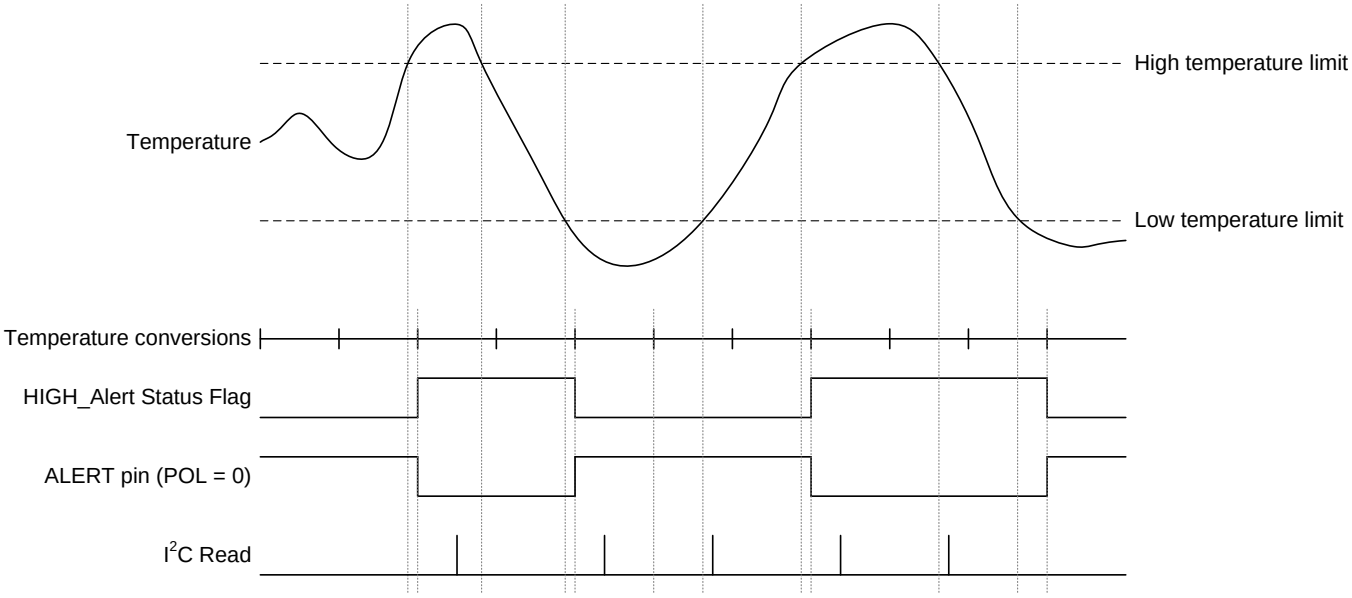

図 24. Therm Mode Timing Diagram

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7.5 Programming

7.5.1 EEPROM Programming

7.5.1.1 EEPROM Overview

The device consists of a user-programmable EEPROM that can be used for two purposes:

- Storing the reset values of configuration register and alert registers
- Four 16-bit locations for general-purpose use; see the EEPROM[4:1] registers

On reset, the device goes through a reset sequence that loads the values programmed in the EEPROM into the respective register map locations. This process takes approximately 1.5 ms. When the reset sequence is completed the device starts operating in accordance to the configuration parameters that are loaded from the EEPROM. Any I^2C writes performed during this initial period to the registers are ignored. I^2C read transactions can still be performed with the device during the reset period. While the reset sequence is being executed, the EEPROM_Busy status flag in the EEPROM unlock register is cleared.

During production, the EEPROM in the TMP116 is programmed with reset values as shown in 表 3. The *Programming the EEPROM* section describes how to change these values. Additionally, during production a unique ID is programmed in the general-purpose EEPROM locations. This unique ID is used to support NIST traceability. The TMP116 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards. Only reprogram the general-purpose EEPROM[4:1] locations if NIST traceability is not desired.

7.5.1.2 Programming the EEPROM

To prevent accidental programming, the EEPROM is locked by default. When locked, any I^2C writes to the register map locations are performed only on the volatile registers and not on the EEPROM.

図 25 illustrates a flow chart describing the EEPROM programming sequence. To program the EEPROM, first unlock the EEPROM by setting the EUN bit in the EEPROM unlock register. After the EEPROM is unlocked, any subsequent I^2C writes to the register map locations program a corresponding non-volatile memory location in the EEPROM. Programming a single location typically takes 7 ms to complete and consumes 230 µA. Do not perform any I^2C writes until programming is completed. During programming, the EEPROM_busy flag is set. Read this flag to monitor if the programming is complete. After programming the desired data, issue a general-call reset command to trigger a software reset. The programmed data from the EEPROM are then loaded to the corresponding register map locations as part of the reset sequence. This command also clears the EUN bit and automatically locks the EEPROM to prevent any further accidental programming. The application must avoid temperature conversions when the EEPROM is unlocked.

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Programming (continued)

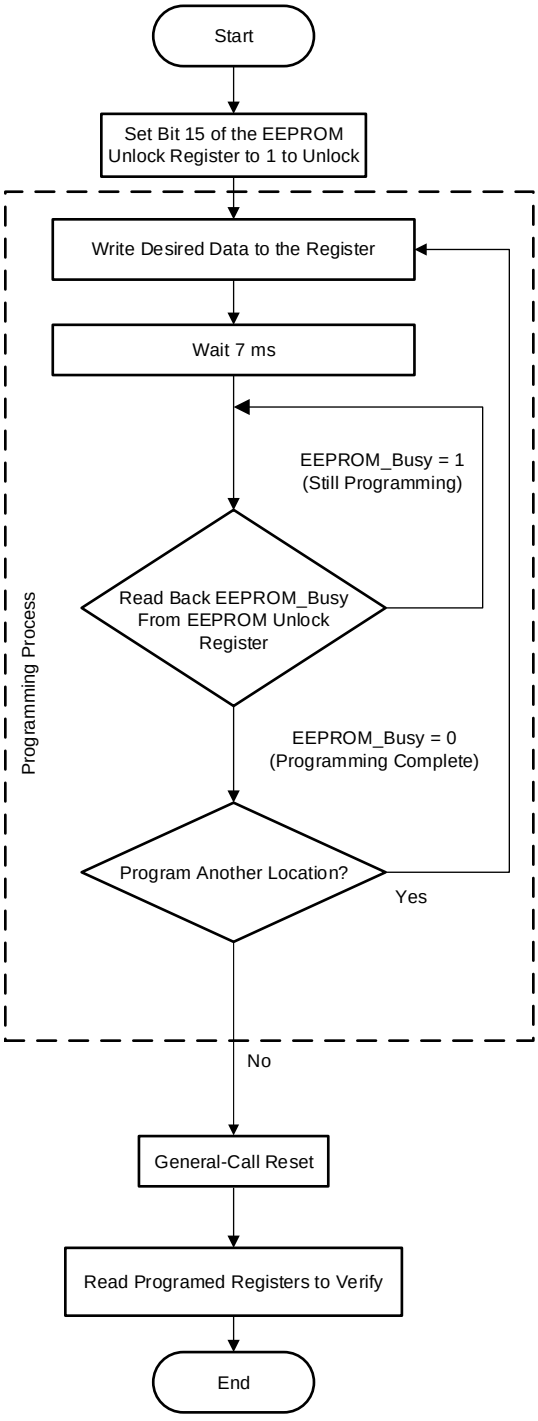

図 25. EEPROM Programming Sequence

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Programming (continued)

7.5.2 Pointer Register

図 26 shows the internal register structure of the TMP116. The 8-bit pointer register of the device is used to address a given data register. The power-up reset value is 00. By default, the TMP116 reads the temperature on power-up.

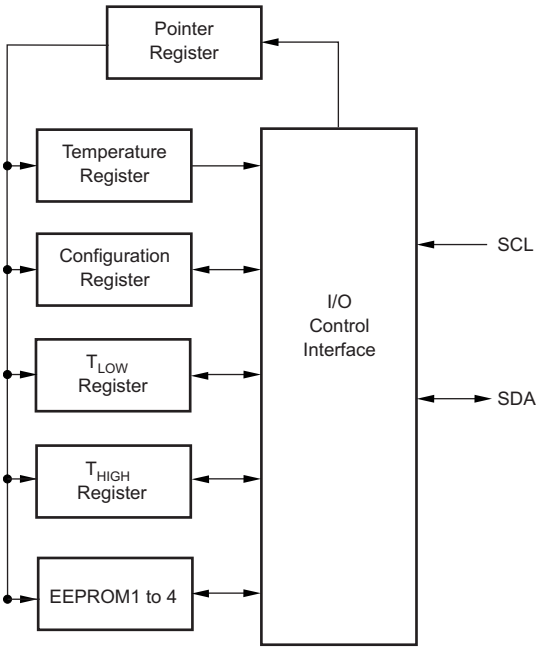

図 26. Internal Registers Structures

7.5.3 I²C and SMBus Interface

7.5.3.1 Serial Interface

The TMP116 operates as a slave device on the two-wire, SMBus and I²C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL pins. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The device supports the transmission protocol for fast (1 kHz to 400 kHz) mode. Register bytes are sent with the most significant byte first, followed by the least significant byte.

7.5.3.1.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus is controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high- to low-logic level when the SCL pin is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and pulling the SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer, the SDA pin must remain stable when the SCL pin is high because any change in the SDA pin when the SCL pin is high is interpreted as a START or STOP signal.

When all data are transferred, the master generates a repeated START or STOP condition. The STOP condition is indicated by pulling the SDA pin from low to high when the SCL pin is high.

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Programming (continued)

7.5.3.1.2 Serial Bus Address

To communicate with the TMP116, the master must first address slave devices through an address byte. The address byte consists of seven address bits and a read-write (R/W) bit indicating the intent of executing a read or write operation.

The TMP116 features an address pin to allow up to four devices to be addressed on a single bus. 表 2 describes the pin connection used to properly address up to four devices. *x* represents the read-write (R/$\overline{W}$) bit.

表 2. Address Pin and Slave Addresses

DEVICE ADDRESS	ADD0 PIN CONNECTION
1001000x	Ground
1001001x	V+
1001010x	SDA
1001011x	SCL

7.5.3.1.3 Writing and Reading Operation

Accessing a particular register on the TMP116 is accomplished by writing the register address to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP116 requires a value for the pointer register.

When reading from the TMP116, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing an address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command; see 図 28 for details of this sequence. If repeated reads from the same register are desired, continuously sending the pointer register bytes is not necessary because the TMP116 retains the pointer register value until the value is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.

7.5.3.1.4 Slave Mode Operations

The TMP116 can operate as a slave receiver or slave transmitter. As a slave device, the TMP116 never drives the SCL line.

7.5.3.1.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address with the R/$\overline{W}$ bit low. The TMP116 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP116 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP116 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

7.5.3.1.4.2 Slave Transmitter Mode

The first byte transmitted by the master is the slave address with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *not-acknowledge* on reception of any data byte or by generating a START or STOP condition.

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7.5.3.1.5 SMBus Alert Function

The TMP116 supports the SMBus alert function. When the ALERT pin is connected to an SMBus alert signal and a master senses that an alert condition is present, the master can send out an SMBus ALERT command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus ALERT command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the alert condition is caused by the temperature exceeding $T_{(HIGH)}$ or falling below $T_{(LOW)}$. The LSB is high if the temperature is greater than $T_{(HIGH)}$, or low if the temperature is less than $T_{(LOW)}$; see 図 29 for details of this sequence.

If multiple devices on the bus respond to the SMBus ALERT command, arbitration during the slave address portion of the SMBus ALERT command determines which device clears the alert status of that device. The device with the lowest two-wire address wins the arbitration. If the TMP116 wins the arbitration, the TMP116 ALERT pin becomes inactive at the completion of the SMBus ALERT command. If the TMP116 loses the arbitration, the TMP116 ALERT pin remains active.

7.5.3.1.6 General-Call Reset Function

The TMP116 responds to a two-wire, general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP116 internal registers are reset to power-up values.

7.5.3.1.7 Timeout Function

The TMP116 resets the serial interface if the SCL line is held low by the master or the SDA line is held low by the TMP116 for 35 ms (typical) between a START and STOP condition. The TMP116 releases the SDA line if the SCL pin is pulled low and waits for a START condition from the host controller. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for the SCL operating frequency.

7.5.3.1.8 Timing Diagrams

The TMP116 is two-wire, SMBus, and I^2C interface-compatible. 図 27 to 図 30 describe the various operations on the TMP116. Parameters for 図 1 are defined in *Two-Wire Interface Timing*. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte transmitted by the slave.

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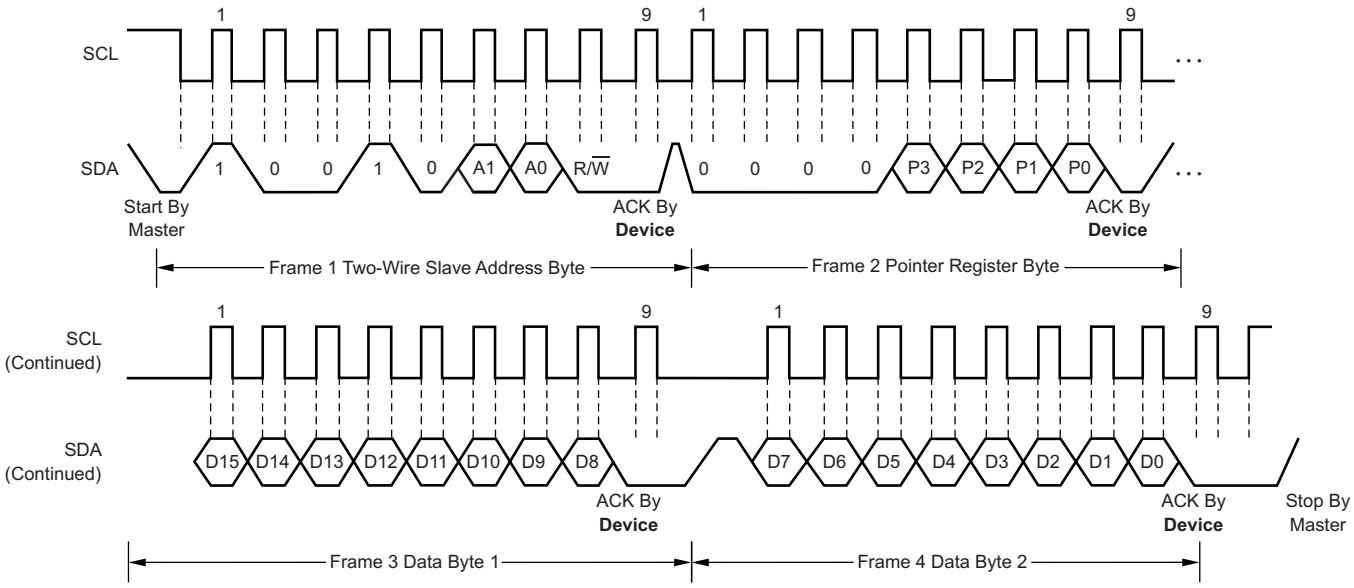

図 27. Write Word Command Timing Diagram

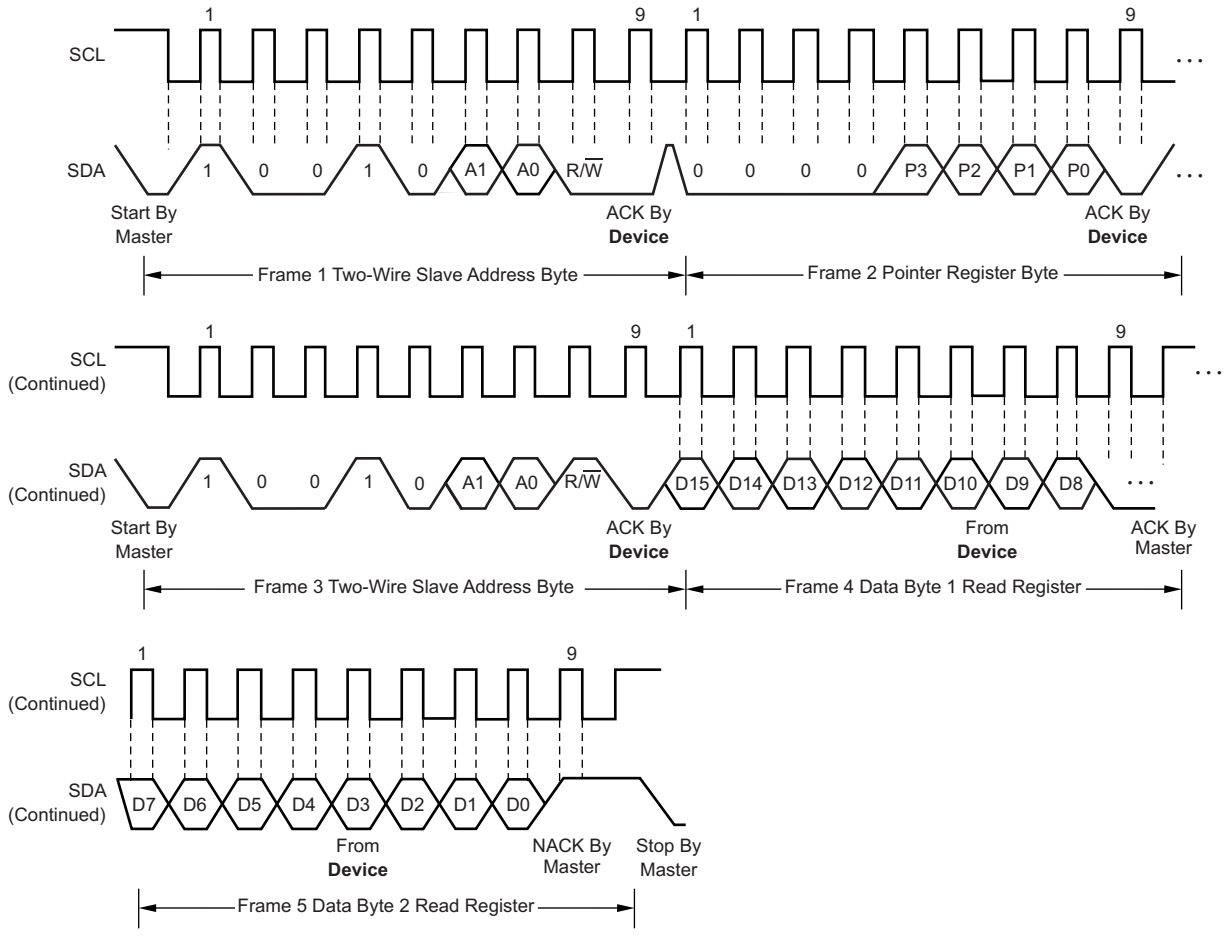

図 28. Read Word Command Timing Diagram

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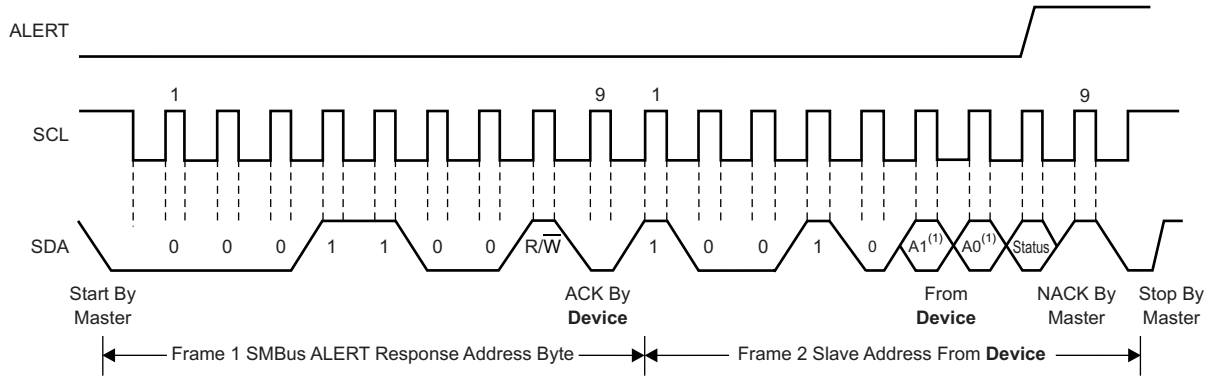

図 29. SMBus ALERT Timing Diagram

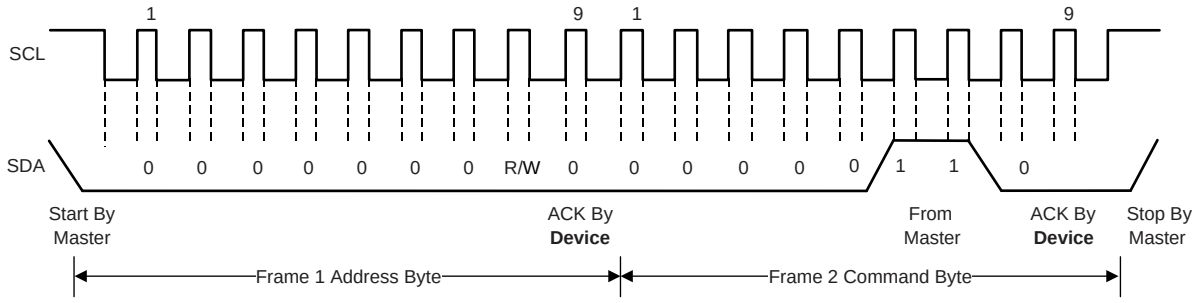

図 30. General-Call Reset Command Timing Diagram

7.6 Registers Map

表 3. Register Map

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	8000h	TEMP	Temperature register	Go
01h	R/W	0220h(1)	CFGR	Configuration register	Go
02h	R/W	6000h(1)	HIGH_LIM	High limit register	Go
03h	R/W	8000h(1)	LOW_LIM	Low limit register	Go
04h	R/W	0000h	EEPROM_UL	EEPROM unlock register	Go
05h	R/W	0000h(1)	EEPROM1	EEPROM1 register	Go
06h	R/W	0000h(1)	EEPROM2	EEPROM2 register	Go
07h	R/W	0000h(1)	EEPROM3	EEPROM3 register	Go
08h	R/W	0000h(1)	EEPROM4	EEPROM4 register	Go
0Fh	R	1116h	DEVICE_ID	Device ID register	Go

(1) This value is stored in electrically-erasable, programmable read-only memory (EEPROM) during device manufacturing. The device reset value can be changed by writing the relevant code in the EEPROM cells (see the *EEPROM Overview* section).

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7.6.1 Register Descriptions

表 4. TMP116 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 Temperature Register (address = 00h) [default reset = 8000h]

This register is a 16-bit, read-only register that stores the output of the most recent conversion. One LSB equals 7.8125 m°C. Data are represented in binary two's complement format. Following power-up or a general-call reset, the temperature register reads –256°C until the first conversion is complete (see the *Power Up* section).

図 31. Temperature Register

15	14	13	12	11	10	9	8
T15	T14	T13	T12	T11	T10	T9	T8
R-1	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

表 5. Temperature Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	T[15:0]	R	8000h	16-bit, read-only register that stores the most recent temperature conversion results.

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7.6.1.2 Configuration Register (address = 01h) [Factory default reset = 0220h]

図 32. Configuration Register

15	14	13	12	11	10	9	8
HIGH_Alert	LOW_Alert	Data_Ready	EEPROM_Busy	MOD1(1)	MOD0(2)	CONV2(2)	CONV1(2)
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0
7	6	5	4	3	2	1	0
CONV0(2)	AVG1(2)	AVG0(2)	T/nA(2)	POL(2)	DR/Alert(2)	—	—
R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R-0	R-0

(1) The MOD1 bit cannot be stored in EEPROM. The device can only be programmed to start up in shutdown mode or continuous conversion mode.
(2) These bits can be stored in EEPROM. The factory setting for this register is 0220.

表 6. Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	HIGH_Alert	R	0	High Alert flag: 1: Set when the conversion result is higher than the high limit 0: Cleared on read of configuration register Therm mode: 1: Set when the conversion result is higher than the therm limit 0: Cleared when the conversion result is lower than the hysteresis
14	LOW_Alert	R	0	Low Alert flag: 1: Set when the conversion result is lower than the low limit 0: Cleared when the configuration register is read Therm mode: Always set to 0
13	Data_Ready	R	0	Data ready flag. This flag indicates that the conversion is complete and the temperature register can be read. Every time the temperature register or configuration register is read, this bit is cleared. This bit is set at the end of the conversion when the temperature register is updated. Data ready can be directed to the ALERT pin by setting bit 2 of the configuration register.
12	EEPROM_Busy	R	0	EEPROM busy flag. The value 1 of the flag indicates that the EEPROM is busy during programming or power-up.
11:10	MOD[1:0]	R/W	0	Set Temperature conversion mode. 00: Continuous conversion (CC) 01: Shutdown (SD) 10: Continuous conversion (CC), same as 00 (reads back = 00) 11: One-shot conversion (OS)
9:7	CONV[2:0]	R/W	100	Conversion cycle bit. See 表 7 for the standby time between conversions.
6:5	AVG[1:0]	R/W	01	Conversion averaging modes. These bits determine the number of conversion results that are collected and averaged before updating the temperature register. The average is an accumulated average and not a running average. 表 7 lists the bit settings for AVG.
4	T/nA	R/W	0	Therm/alert mode select. 1: Therm mode 0: Alert mode
3	POL	R/W	0	ALERT pin polarity bit. 1: Active high 0: Active low
2	DR/Alert	R/W	0	ALERT pin select bit. 1: ALERT pin reflects the status of the data ready flag 0: ALERT pin reflects the status of the alert flags
1:0	—	R	0	Not used

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表 7. Conversion Cycle Time in CC Mode

	AVG[1:0] = 00	AVG[1:0] = 01	AVG[1:0] = 10	AVG[1:0] = 11
Number of averaged samples	1	8	32	64
Active conversion time	15.5 ms	125 ms	500 ms	1 s
CONV[2:0] = 000	15.5 ms(1)	125 ms(1)	500 ms(1)	1 s(1)
CONV[2:0] = 001	125 ms(2)	125 ms(1)	500 ms(1)	1 s(1)
CONV[2:0] = 010	250 ms(2)	250 ms(3)	500 ms(1)	1 s(1)
CONV[2:0] = 011	500 ms(2)	500 ms(3)	500 ms(1)	1 s(1)
CONV[2:0] = 100	1 s(2)	1 s(3)	1 s(4)	1 s(1)
CONV[2:0] = 101	4 s(2)	4 s(3)	4 s(4)	4 s(5)
CONV[2:0] = 110	8 s(2)	8 s(3)	8 s(4)	8 s(5)
CONV[2:0] = 111	16 s(2)	16 s(3)	16 s(4)	16 s(5)

(1) In this mode there is no standby time in the conversion cycle.
(2) In this mode the standby time is the difference of the value and 15.5 ms.
(3) In this mode the standby time is the difference of the value and 125 ms.
(4) In this mode the standby time is the difference of the value and 500 ms.
(5) In this mode the standby time is the difference of the value and 1 s.

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7.6.1.3 High Limit Register (address = 02h) [Factory default reset = 6000h]

This register is a 16-bit, read/write register that stores the high limit for comparison with the temperature result. The register format is same as the temperature register. Following power-up or a general-call reset, the high-limit register is loaded with the stored value from the EEPROM. The factory default reset value is 6000h or 192°C.

図 33. High Limit Register

15	14	13	12	11	10	9	8
H15	H14	H13	H12	H11	H10	H9	H8
R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
H7	H6	H5	H4	H3	H2	H1	H0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8. High Limit Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	H[15:0]	R/W	6000h	16-bit, read/write register that stores the high limit for comparison with the temperature result.

7.6.1.4 Low Limit Register (address = 03h) [Factory default reset = 8000h]

This register is configured as a 16-bit, read/write register that stores the low limit for comparison with the temperature result. The register format is same as the temperature register. Following power-up or reset, the low-limit register is loaded with the stored value from the EEPROM. The factory default reset value is 8000h or –256°C.

図 34. Low Limit Register

15	14	13	12	11	10	9	8
L15	L14	L13	L12	L11	L10	L9	L8
R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9. Low Limit Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	L[15:0]	R/W	8000h	16-bit, read/write register that stores the low limit for comparison with the temperature result.

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7.6.1.5 EEPROM Unlock Register (address = 04h) [reset = 0000h]

図 35. EEPROM Unlock Register

15	14	13	12	11	10	9	8
EUN	EEPROM_Busy	—	—	—	—	—	—
R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

表 10. EEPROM Unlock Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	EUN	R/W	0	EEPROM unlock. 0: EEPROM is locked for programming: writes to all EEPROM addresses (such as configuration, limits, and EEPROM locations 1-4) are written to registers in digital logic and are not programmed in the EEPROM 1: EEPROM unlocked for programming: any writes to writable registers program the respective location in the EEPROM
14	EEPROM_Busy	R	0	EEPROM busy. This flag is the mirror of the EEPROM busy flag (bit 12) in the configuration register. 0: Indicates that the EEPROM is ready, which means that the EEPROM has finished the last transaction and is ready to accept new commands 1: Indicates that the EEPROM is busy, which means that the EEPROM is currently completing a programming operation or performing power-up on reset load
13:0	—	R	0	Not used

7.6.1.6 EEPROM1 Register (address = 05h) [reset = XXXXh]

The EEPROM1 register is a 16-bit register that be used as a scratch pad by the customer to store general-purpose data. This register has a corresponding EEPROM location. Writes to this address when the EEPROM is locked write data into the register and not to the EEPROM. Writes to this register when the EEPROM is unlocked causes the corresponding EEPROM location to be programmed; see the *Programming the EEPROM* section. EEPROM[4:1] are preprogrammed during manufacturing with the unique ID that can be overwritten. In order to support NIST traceability, do not delete or reprogram EEPROM[4:1].

図 36. EEPROM1 Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

表 11. EEPROM1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	D[15:0]	R/W	xxxxh	This 16-bit register can be used as a scratch pad by the customer.

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7.6.1.7 EEPROM2 Register (address = 06h) [reset = XXXXh]

This register function the same as the EEPROM1 register.

図 37. EEPROM2 Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

表 12. EEPROM2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	D[15:0]	R/W	xxxxh	This 16-bit register can be used as a scratch pad by the customer.

7.6.1.8 EEPROM3 Register (address = 07h) [reset = 0000h]

This register function is the same as the EEPROM1 register.

図 38. EEPROM3 Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 13. EEPROM3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	D[15:0]	R/W	0	This 16-bit register can be used as a scratch pad by the customer.

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7.6.1.9 EEPROM4 Register (address = 08h) [reset = XXXXh]

This register function is the same as the EEPROM1 register.

図 39. EEPROM4 Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

表 14. EEPROM4 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	D[15:0]	R/W	xxxxh	This 16-bit register can be used as a scratch pad by the customer.

7.6.1.10 Device ID Register (address = 0Fh) [reset = 1116h]

This read-only register indicates the device ID.

図 40. Device ID Register

15	14	13	12	11	10	9	8
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R-0	R-0	R-0	R-1	R-0	R-0	R-0	R-1
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R-0	R-0	R-0	R-1	R-0	R-1	R-1	R-0

表 15. Device ID Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	DID[15:0]	R	1116h	These bits indicate the device ID.

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8 Application and Implementation

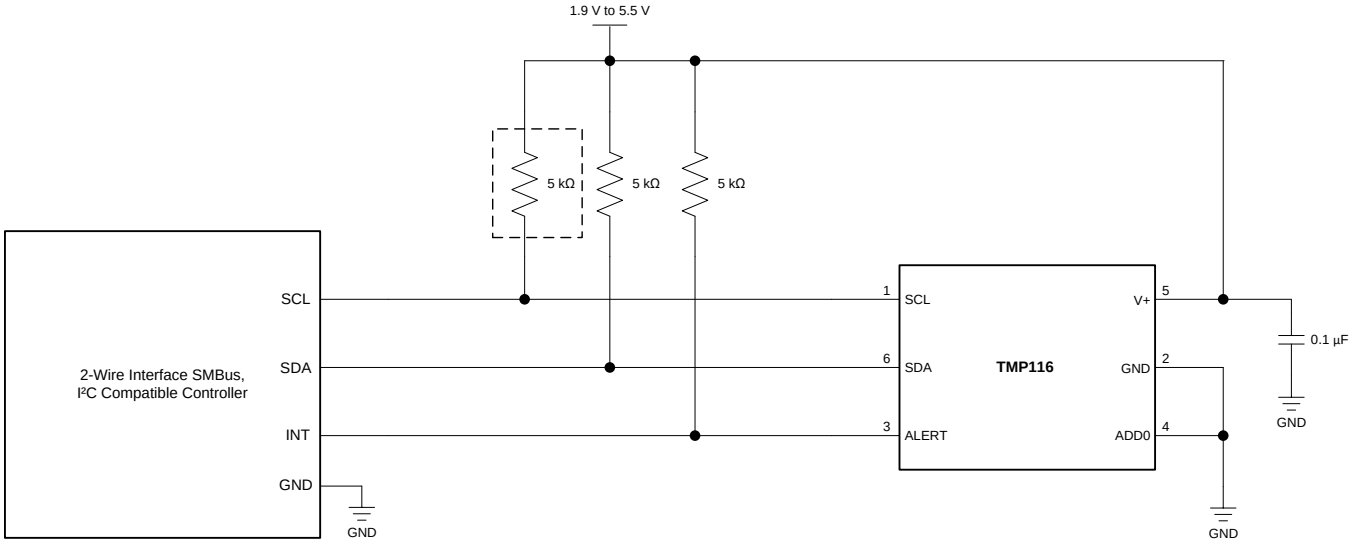
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP116 is used to measure the temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus.

8.1.1 Typical Application



NOTE: The SDA and ALERT pins require pullup resistors.

図 41. Typical Connections

8.1.1.1 Design Requirements

The TMP116 operates only as a slave device and communicates with the host through the I^2C-compatible serial interface. SCL is the input pin, SDA is a bidirectional pin, and ALERT is the output. The TMP116 requires a pullup resistor on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ. A 0.1-µF bypass capacitor is recommended to be connected between V+ and GND. An SCL pullup resistor is required if the system microprocessor SCL pin is open-drain. Use a ceramic capacitor type with according temperature range, placed as close as possible to the V+ pin of the TMP116. The ALERT output pin can be connected to a microcontroller interrupt that triggers an event that occurred when the temperature limit exceeds the programmable value or indicates conversion end. It is recommended that the ALERT pin be connected to ground.

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Application Information (continued)

8.1.1.2 Detailed Design Procedure

8.1.1.2.1 Noise and Averaging

The device temperature sampling distribution (without internal averaging) covers an area of approximately six neighboring codes. The noise area of the six codes remains the same at full supply and full temperature range with a standard deviation of approximately 1 LSB. The device provides an averaging tool for 8, 32, and 64 samples. As illustrated in 図 7, even the 8-sample averaging reduces the internal noise distribution to a theoretical minimum of 2 LSB. This averaging means that if the system temperature slowly changes and the supply voltage is stable, then the 8-sample averaging can be enough to neutralize the device internal noise and provide stable temperature readings. However, if the system temperature is noisy (such as when measuring air flow temperatures) or noisy power supply line or intensive communication in the I^2C line, then higher averaging numbers are recommended to be used.

8.1.1.2.2 Self-Heating Effect (SHE)

During ADC conversion some power is dissipated that heats the device despite the small power consumption of the TMP116. Consider the self-heating effect (SHE) for certain precise measurements. 図 42 shows the device SHE in still air at 25°C after the supply is switched on. The device package, is soldered to the 11-mm × 20-mm × 1.1-mm size coupon board. The board is located horizontally, with the device on top. The TMP116 is in continuous conversion mode with 64 sampling averaging and zero conversion cycle time. There is no digital bus activity aside from reading temperature data one time each second. As shown in 図 42, the SHE stabilization time in still air is greater when the device dissipates more power.

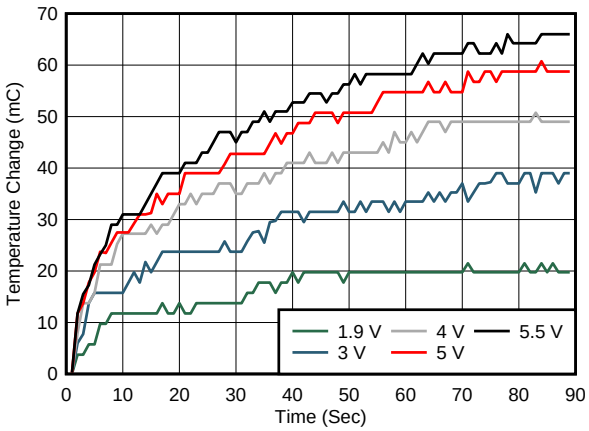

図 42. Self-Heating in Still Air vs. Temperature and Dissipated Power

The SHE drift is strongly proportional to the device dissipated power. The SHE drift is also proportional to the device temperature because the consumption current with the same supply voltage increases with temperature. 図 43 shows the SHE drifts versus temperature and dissipated power at 25°C for the same coupon board and the same conditions described previously.

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Application Information (continued)

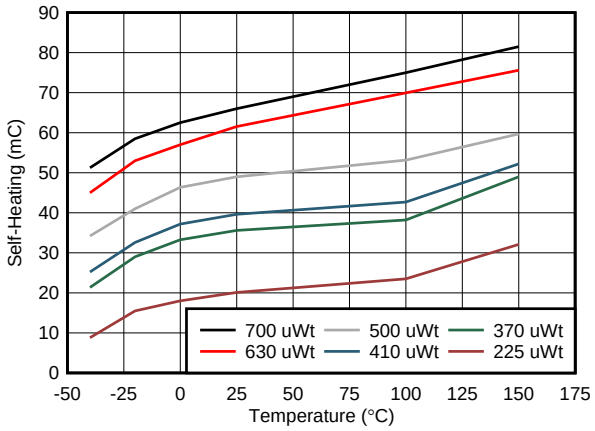

図 43. Self-Heating in Still Air vs. Temperature and Dissipated Power at 25°C

To estimate the SHE for similar size boards, calculate the device consumption power for 25°C and use the corresponding power line shown in 図 43. For example, in CC mode without duty cycle at a 3.3-V supply at 25°C, the device dissipates 410 µWt. So self-heating in still air is approximately 40 m°C for the described condition and rises to 52 m°C at 150°C.

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Application Information (continued)

The following methods can reduce the SHE:

- System calibration removes not only the self-heating error and power-supply rejection ratio (PSRR) effect but also compensates the temperature shift caused by the thermal resistance between the device and the measured object.
- If practical, use the device one-shot mode. If continuous conversion is needed, use the conversion cycle mode with significant standby time. For example, in most cases an 8-sample averaging (125 ms) with a 1-second conversion cycle provides enough time for the device to cool down to the environment temperature and removes the SHE.
- Use the minimal acceptable power supply voltage.
- Use a printed-circuit board (PCB) layout that provides minimal thermal resistance to the device.
- Avoid using small-value pullup resistors on the SDA and ALERT pins. Instead, use pullup resistors larger than 2 kΩ.
- Ensure that the SCL and SDA signal levels remain below 10% or above 90% of the device supply voltage.
- Avoid heavy bypass traffic on the data line. Communication to other devices on the same data line increases the supply current even if the device is in SD mode.
- Use the highest available communication speed.

8.1.1.2.3 Synchronized Temperature Measurements

When four temperature measurements are needed in four different places simultaneously, triggering by reset is recommended. In this method, four devices are programed with control registers set to CC mode with a conversion cycle time of 16 s. All four devices are connected to same two-wire bus with four different bus addresses. The bus general-call reset command is issued by the master. This command triggers all devices to reset (which takes approximately 1.5 ms) and triggers a simultaneous temperature sampling according to configuration registers setting. The master has 16 seconds to read data from the devices.

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9 Power Supply Recommendations

The TMP116 operates on a power-supply range from 1.9 V to 5.5 V. The device is trimmed for operation at a 3.3-V supply, but can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required, which must be placed as close as possible to the device. A recommended value for this supply bypass capacitor is 100 nF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

The TMP116 is a very low-power device and generates low noise on the supply bus. Applying an RC filter to the V+ pin of the device can further reduce any noise that the TMP116 might propagate to other components. R_F in 図 44 must be less than 0.5 kΩ and C_F must be at least 100 nF. Take care that the V+ pin voltage is not less than 1.9 V. The package thermal pad is not connected to the device ground and should be left unsoldered for the best measurement accuracy. If the thermal pad is soldered it must be left floating or connected to ground.

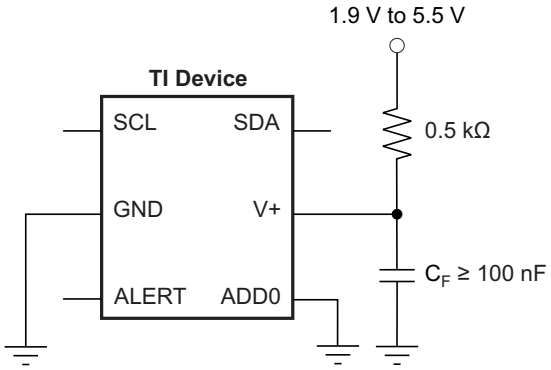

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図 44. Noise-Reduction Techniques

10 Layout

10.1 Layout Guidelines

注

To achieve a high precision temperature reading for a rigid PCB, do not solder down the thermal pad. For a flexible PCB, the user can solder the thermal pad to increase board level reliability. If thermal pad is soldered it should be connected to the ground or left floating.

For more information on board layout, refer to the related *Precise Temperature Measurements With TMP116* (SNOA986) and *Wearable Temperature Sensing Layout Considerations Optimized for Thermal Response* (SNIA021) application reports on ti.com.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF. In some cases, the pullup resistor can be the heat source, therefore, maintain some distance between the resistor and the device.

Mount the TMP116 on the PCB pad to provide the minimum thermal resistance to the measured object surface or to the surrounding air. The PCB layout should minimize the device self-heating effect, reduce the time delay as temperature changes, and minimize the temperature offset between the device and the measured object.

1. Soldering the TMP116 thermal pad to the PCB minimizes the thermal resistance to the PCB, reduces the response time as temperature changes and minimizes the temperature offset between the device and measured object. Simultaneously the soldering of the thermal pad will, however, introduce mechanical stress that can be a source of additional measurement error. For cases when system calibration is not planned, TI recommends not soldering the thermal pad to the PCB. Due to the small thermal mass of the device, not soldering the thermal pad will have a minimal impact on the described characteristics. Manual device soldering to PCB creates additional mechanical stress to package, therefore to prevent precision degradation

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Layout Guidelines (continued)

a standard PCB reflow oven process is highly recommended.

2. If the device is used to measure solid surface temperature:
   - Use PCB with minimal thickness.
   - Prevent PCB bending which can create a mechanical stress to package.
   - Cover bottom of the PCB with copper plane.
   - Remove bottom solder mask and cover exposed copper with gold layer if possible.
   - Use thermal conductive paste between PCB and object surface.
   - If PCB has unused internal layers, extend these layers under the sensor.
   - Minimize amount of copper wires on top of the board.
   - To minimize temperature “leakage” to surrounding air locate sensor in place with minimal air movement. Horizontal surfaces are preferable.
   - To minimize temperature offset due to “leakage” to surrounding air cover sensor with thermo isolating foam, tape or at least cover with a stain.
3. If the device is used to measure moving air temperature:
   - Because moving air temperature usually has a lot of fluctuations the PCB increased thermal mass reduces measurement noise.
   - Design PCB soldering pads bigger than usual, especially package corner pads.
   - Use a PCB with thicker copper layers if possible.
   - Cover both side of unused board space with copper layer.
   - Place PCB vertically along air flow.
4. If the device is used to measure still air temperature:
   - Miniaturize the board to reduce thermal mass. Smaller thermal mass results in faster thermal response.
   - Place two copper planes of equal size to the top and bottom of the exposed pad.
   - Remove the top solder mask.
   - To prevent oxidation, cover any exposed copper with solder paste.
   - Thermal isolation is required to avoid thermal coupling from heat source components through the PCB.
   - Avoid running the copper plane underneath the temperature sensor.
   - Maximize the air gap between the sensor and the surrounding copper areas (anti-etch), especially when close to the heat source.
   - Create a PCB cutout between sensor and other circuits. Leave a narrow channel away from heat source components as a routing bridge into the island.
   - If the heat source is top side, avoid running traces on top; instead, route all signals on the bottom side.
   - Place the board vertically to improve air flow and to reduce dust collection.

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10.2 Layout Example

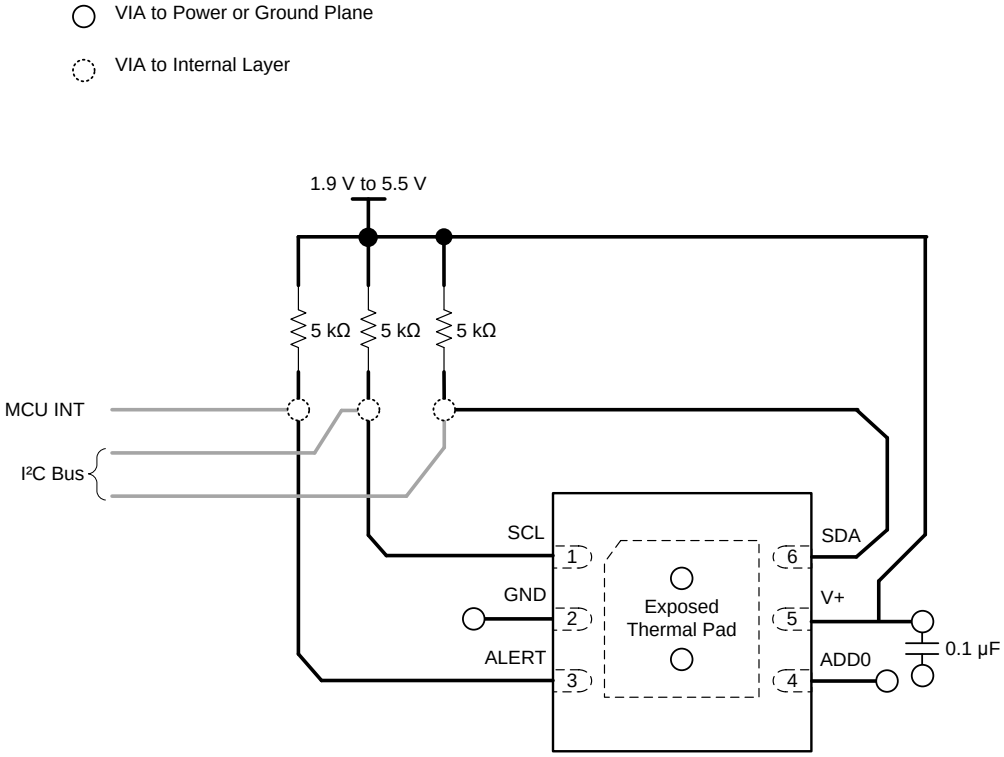

図 45. Layout Recommendation

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『*TMP116 Ambient Air Temperature Measurement* application report』(SNOA966) (英語)
- テキサス・インスツルメンツ、『*Replacing Resistance Temperature Detectors with the TMP116 Temp Sensor* application report』(SNOA969) (英語)
- テキサス・インスツルメンツ、『*Temperature Sensors: PCB Guidelines for Surface Mount Devices* application report』(SNOA967) (英語)
- テキサス・インスツルメンツ、『*Precise Temperature Measurements With TMP116* application report』(SNOA986) (英語)
- テキサス・インスツルメンツ、『*Wearable Temperature Sensing Layout Considerations Optimized for Thermal Response* application report』(SNIA021) (英語)
- テキサス・インスツルメンツ、『*TMPx75 Temperature Sensor With I^2C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout*』データシート (SBOS288) (英語)
- テキサス・インスツルメンツ、『*TMP275 I2C および SMBus インターフェイス付きで業界標準の LM75 フォーム・ファクタおよびピン配置の±0.5℃温度センサ*』データシート (SBOS363)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP116AIDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T116
TMP116AIDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T116
TMP116AIDRVT	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-55 to 125	T116
TMP116NAIDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	116N
TMP116NAIDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	116N
TMP116NAIDRVT	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-55 to 125	116N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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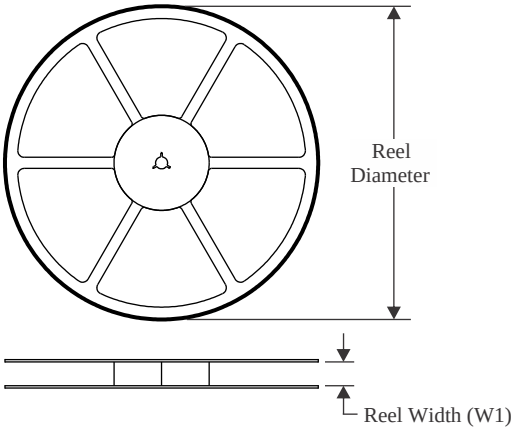
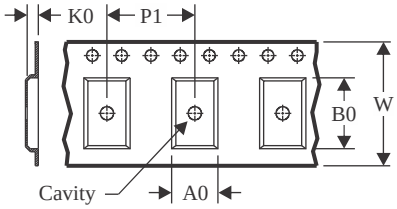
TAPE AND REEL INFORMATION

REEL DIMENSIONS

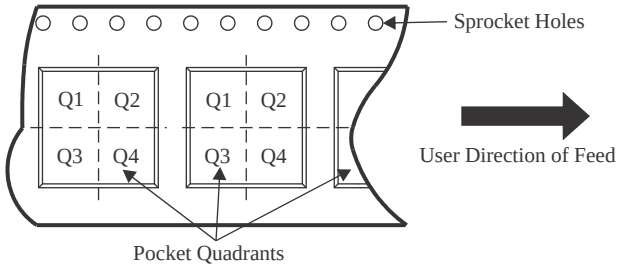


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

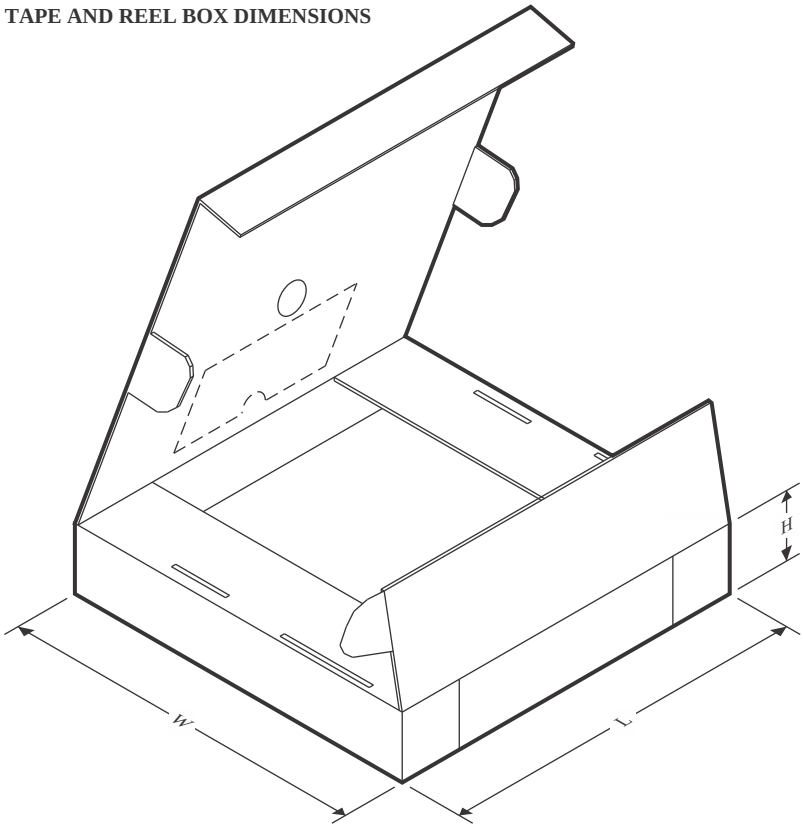
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP116AIDRVR	WSON	DRV	6	3000	178.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TMP116NAIDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

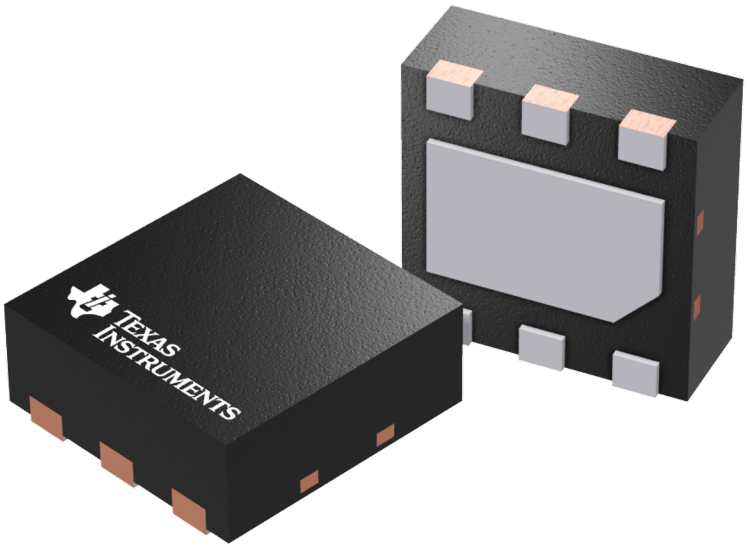


*All dimensions are nominal

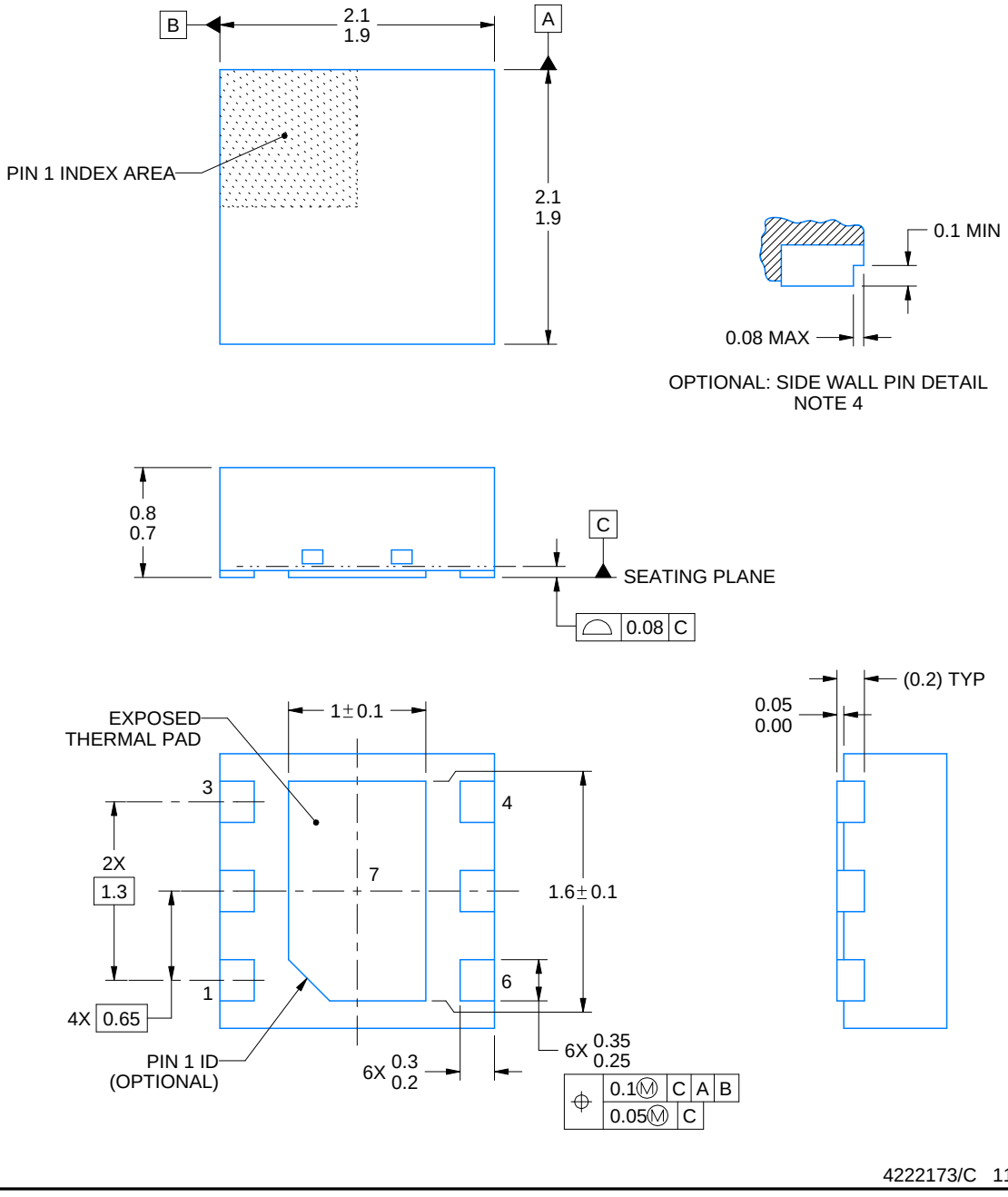
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP116AIDRVR	WSON	DRV	6	3000	208.0	191.0	35.0
TMP116NAIDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

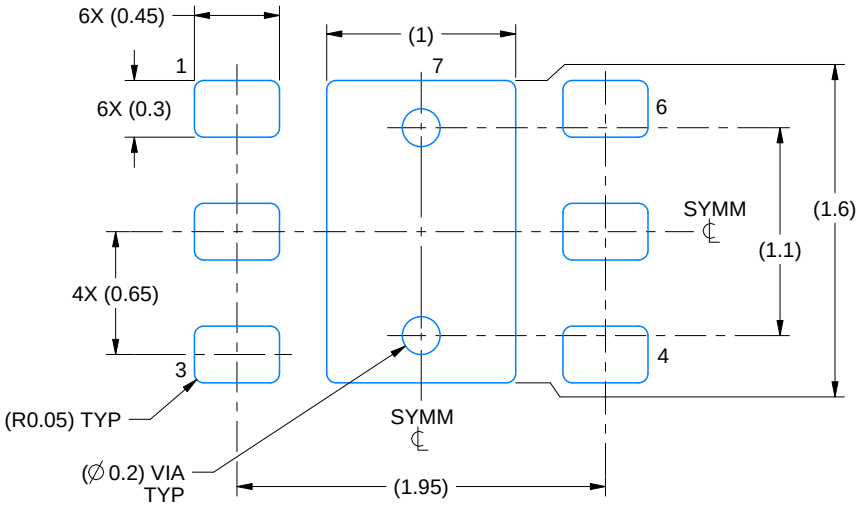


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

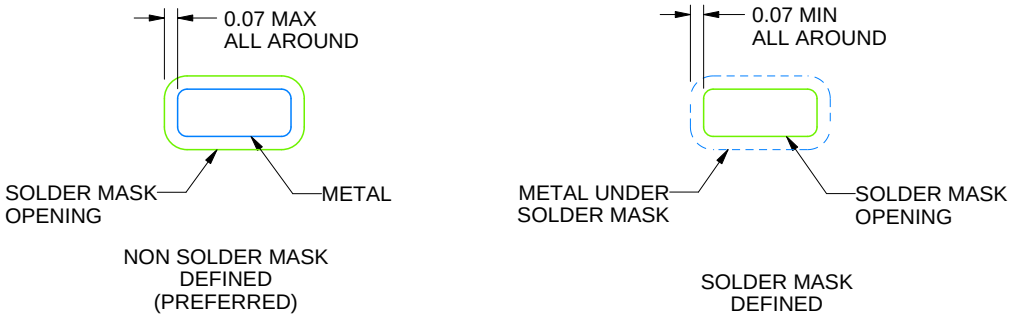


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

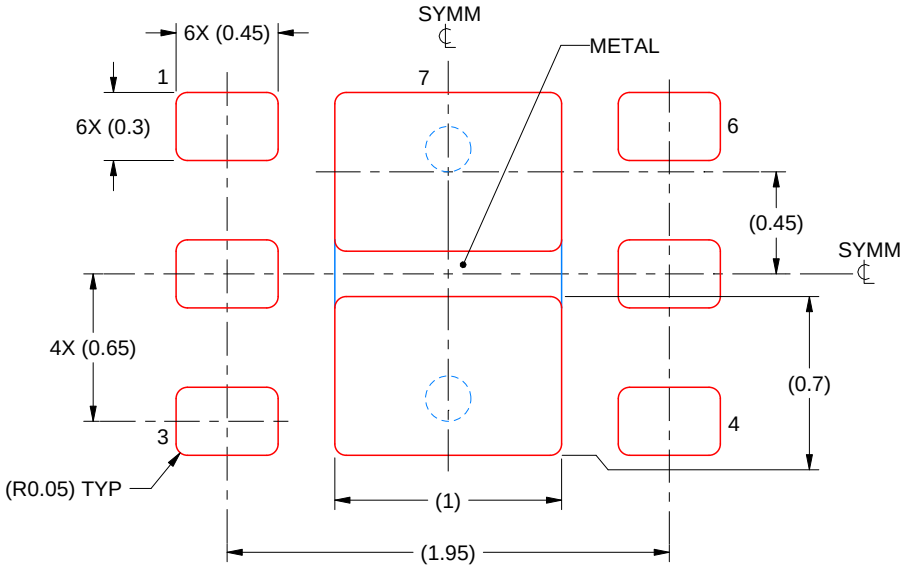


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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