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## 4 Revision History

Changes from Revision L (December 2015) to Revision M (October 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Changed Absolute maximum Supply voltage of TMP75 from 7 V to 6.5 V.....	5
• Added applicable pins to Input voltage specification.....	5
• Changed Absolute maximum Input Voltage of TMP75 on SCL, SDA, A0, and A1 pins from 7 V to 6.5 V.....	5
• Changed Absolute maximum of TMP75 A2 pin voltage from 7 V to (V+)+0.3.....	5
• Removed ESD Machine Model specification from TMP75.....	5
• Updated TMP75 D and DGK package Thermal Information.....	5
• Updated TMP175 D package Thermal Information.....	5
• Added register settings to Conversion time specification for clarity.....	6
• Changed minimum Data setup specification time from 10 ns to 20 ns.....	7
• Moved Timeout specification to I2C Interface Timing table.....	7
• Changed TMP75 Timeout specification minimum from 25 to 20.....	7
• Changed TMP75 Timeout specification maximum from 74 to 30.....	7
• Removed BYTE column from the <i>Configuration Register</i> table.....	18
• Changed TMP75 consecutive fault setting F[1:0] = 11 from 6 to 4 and F[1:0] = 10 from 4 to 3.....	19
• Added behavior clarification when changing thermostat modes on TMP75.....	20
• Changed bypass capacitor recommendation from 0.1 μF to 0.01 μF.....	22
• Updated recommended pull-up resistor size to standard 4.7 kΩ.....	22
• Removed <i>Related Links</i> section.....	25
• Added <i>Receiving Notification of Documentation Updates</i> section.....	25

Changes from Revision K (April 2015) to Revision L (December 2015)	Page
• 「特長」の2番目の箇条書き項目を変更：TMP75 デバイスに NIST トレース可能を追加.....	1
• 「概要」セクションに最後の段落を追加.....	1
• 1 ページから「概略回路図」を削除.....	1
• Changed 図 7-1.....	14

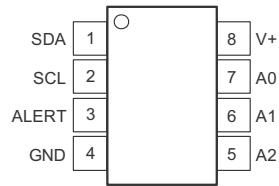
Changes from Revision J (December 2007) to Revision K (April 2015)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよび	

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ドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。..... 1

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## 5 Pin Configuration and Functions



NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

**图 5-1. DGK and D Packages 8-Pin VSSOP and SOIC Top View**

**表 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.
2	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	GND	—	Ground
5	A2	I	Address select. Connect to GND, V+ or (for the TMP175 device only) leave these pins floating.
6	A1		
7	A0		
8	V+	I	Supply voltage, 2.7 V to 5.5 V

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted<sup>(1)</sup>

		MIN	MAX	UNIT
Power Supply, V+	TMP175		7	V
	TMP75		6.5	V
Input voltage	TMP175, SCL, SDA, A2, A1, A0	-0.5	7	V
	TMP75 SCL, SDA, A1, A0	-0.3	6.5	V
	TMP75 A2 pin	-0.3	(V+) +0.3	V
Input current	TMP175		10	mA
Operating Temperature		-55	127	°C
Operating junction temperature, T <sub>J</sub>			150	°C
Storage temperature, T <sub>stg</sub>		-60	130	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
	Electrostatic discharge (TMP175)	Machine model (MM)	±300	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V+	Supply voltage	2.7		5.5	V
T <sub>A</sub>	Operating ambient temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMP75	TMP75	TMP175	TMP175	UNIT
		DGK(VSSOP)	D(SOIC)	DGK(VSSOP)	D(SOIC)	
		8-pins	8-pins	8-pins	8-pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	202.5	130.4	185	130.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	82	76.9	76.1	70.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	124.4	72.3	106.4	73.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	17.9	32	14.1	21.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	122.6	71.9	104.8	73.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W
M <sub>T</sub>	Thermal Mass	16.6	64.2	—	—	mJ/°C

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

at  $T_A = -40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$  and  $V_+ = 2.7\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted); typical specification are at  $T_A = 25\text{ }^\circ\text{C}$  and  $V_+ = 3.3\text{ V}$

PARAMETER	TEST CONDITIONS	TMP175			TMP75			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
<b>TEMPERATURE INPUT</b>										
	Range		-40		125		-40		125	$^\circ\text{C}$
$T_{ERR}$	Temperature accuracy	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$		$\pm 0.5$	$\pm 1.5$		$\pm 0.5$	$\pm 2$		$^\circ\text{C}$
$T_{ERR}$	Temperature accuracy	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$		$\pm 1$	$\pm 2$		$\pm 1$	$\pm 3$		$^\circ\text{C}$
PSR	Temperature accuracy (temperature error vs supply)			$\pm 200$	$\pm 500$		$\pm 200$	$\pm 500$		m $^\circ\text{C}/\text{V}$
$T_{RES}$	Temperature resolution	Selectable		0.0625			0.0625			$^\circ\text{C}$
<b>DIGITAL INPUT/OUTPUT</b>										
$C_{IN}$	Input capacitance			3			3			pF
$V_{IH}$	Input logic high level	SDA, SCL, A0, A1, A2	0.7(V+)		6		0.7(V+)		6	V
$V_{IL}$	Input logic low level	SDA, SCL, A0, A1, A2	-0.5		0.3(V+)		-0.5		0.3(V+)	V
$I_{IN}$	Input leakage current	SDA, SCL, A0, A1, A2			1				1	$\mu\text{A}$
HYST	Hysteresis	SDA, SCL		500			500			mV
$V_{OL}$	Low-level output logic SDA	$I_{OL} = 3\text{ mA}$	0	0.15	0.4		0	0.15	0.4	V
$V_{OL}$	Low-level output logic ALERT	$I_{OL} = 4\text{ mA}$	0	0.15	0.4		0	0.15	0.4	V
	Resolution	Selectable	9		12		9		12	Bits
	Conversion time	R1 = 0, R0 = 0; 9-bit		27.5	37.5		27.5	37.5		ms
		R1 = 0, R0 = 1; 10-bit		55	75		55	75		
		R1 = 1, R0 = 0 11-bit		110	150		110	150		
		R1 = 1, R0 = 1; 12-bit		220	300		220	300		
<b>POWER SUPPLY</b>										
	Operating Range		2.7		5.5		2.7		5.5	V
$I_{DD\_AVG}$	Average current consumption	Serial bus inactive		50	85		50	85		$\mu\text{A}$
		Serial bus active, SCL frequency = 400 kHz		100			100			
		Serial bus active, SCL frequency = 3.4 MHz		410			410			
$I_{DD\_SD}$	Shutdown current	Serial bus inactive		0.1	3		0.1	3		$\mu\text{A}$
		Serial bus active, SCL frequency = 400 kHz		60			60			
		Serial bus active, SCL frequency = 3.4 MHz		380			380			

## 6.6 I<sup>2</sup>C Interface Timing

see the [Timing Diagrams](#) and [Two-Wire Timing Diagrams](#) sections for additional information (unless otherwise noted)<sup>(1)</sup>

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	1	400	1	2380	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1.3		0.16		$\mu$ s
$t_{(SUSTA)}$	Repeated START condition setup time	0.6		0.16		$\mu$ s
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	0.6		0.16		$\mu$ s
$t_{(SUSTO)}$	STOP condition setup time	0.6		0.16		$\mu$ s
$t_{(HDDAT)}$	Data hold time	4	900	4	120	ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock low period	1.3		0.28		$\mu$ s
$t_{(HIGH)}$	SCL clock high period	0.6		0.06		$\mu$ s
$t_{RC}$	Clock rise time		300		40	ns
$t_{RC}$	Clock rise time for SCLK $\leq$ 100 kHz		1000			ns
$t_F$	Clock fall time		300		40	ns
$t_{timeout}$	Timeout (SCL = GND or SDA = GND) TMP175	25	74	25	74	ms
$t_{timeout}$	Timeout (SCL = GND or SDA = GND) TMP75	20	30	20	30	

(1) Compatible with standard mode timings

## 6.7 Typical Characteristics

at  $T_A = 25\text{ }^\circ\text{C}$  and  $V_+ = 5\text{ V}$  (unless otherwise noted)

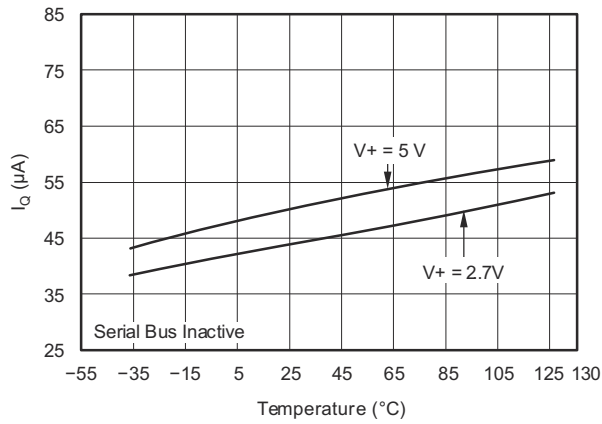


Figure 6-1. Quiescent Current vs Temperature

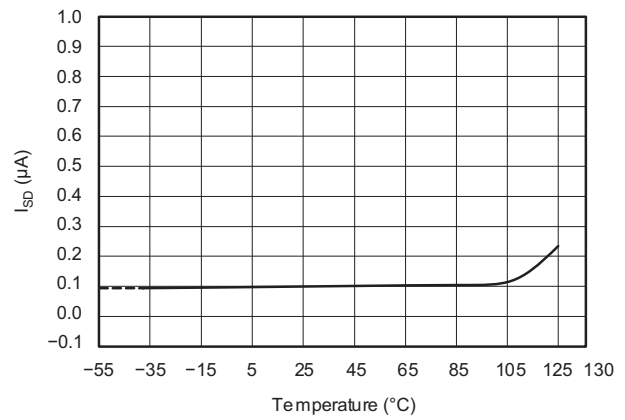


Figure 6-2. Shutdown Current vs Temperature

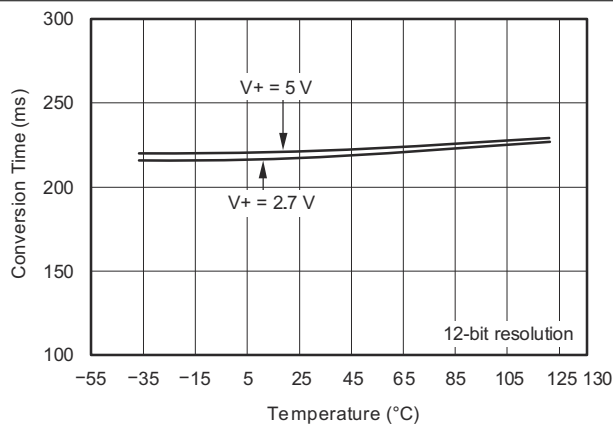


Figure 6-3. Conversion Time vs Temperature

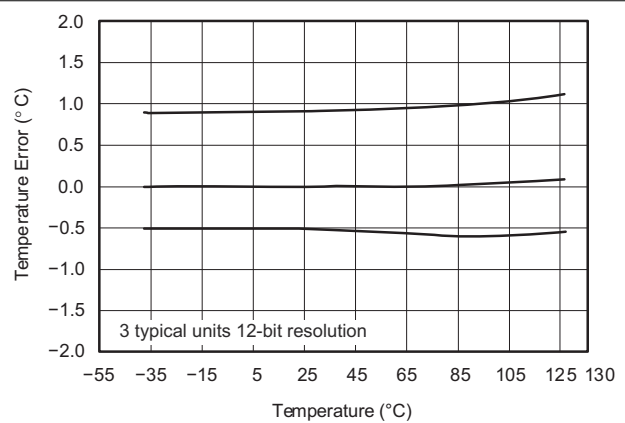


Figure 6-4. Temperature Accuracy vs Temperature

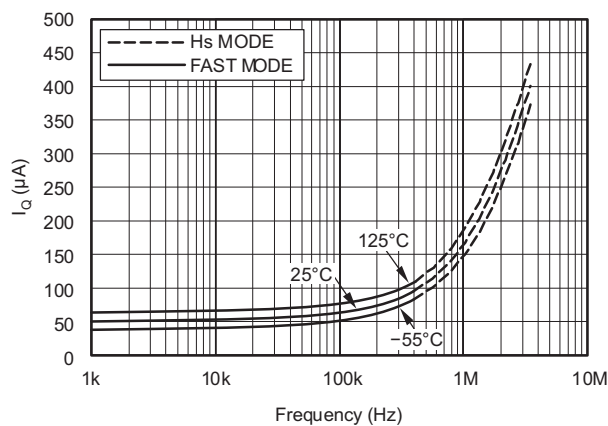


Figure 6-5. Quiescent Current With Bus Activity vs Temperature



## 7.3 Feature Description

### 7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only Temperature register. The Temperature register of the TMP175 or TMP75 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are listed in [表 7-6](#) and [表 7-7](#). The first 12 bits are used to indicate temperature with all remaining bits equal to zero. Data format for temperature is listed in [表 7-1](#). Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature register reads 0 °C until the first conversion is complete.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits (MSBs) in the Temperature register are used with the unused least significant bits (LSBs) set to zero.

**表 7-1. Temperature Data Format**

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-55	1100 1001 0000	C90

### 7.3.2 Serial Interface

The TMP175 and TMP75 operate only as slave devices on the SMBus, two-wire, and I<sup>2</sup>C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP175 and TMP75 support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2 MHz) modes. All data bytes are transmitted MSB first.

#### 7.3.2.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high to low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition indicated by pulling SDA from low to high when SCL is high.

### 7.3.2.2 Serial Bus Address

To communicate with the TMP175 and TMP75, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP175 features three address pins to allow up to 27 devices to be addressed on a single bus interface. [表 7-2](#) describes the pin logic levels used to properly connect up to 27 devices. A 1 indicates the pin is connected to the supply (VCC); a 0 indicates the pin is connected to GND; *float* indicates the pin is left unconnected. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

The TMP75 features three address pins allowing up to eight devices to be connected per bus. Pin logic levels are described in [表 7-3](#). The address pins of the TMP175 and TMP75 are read after reset, at start of communication, or in response to a two-wire address acquire request. After the state of the pins are read, the address is latched to minimize power dissipation associated with detection.

**表 7-2. Address Pins and Slave Addresses for the TMP175**

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111
Float	0	0	1110000
Float	0	Float	1110001
Float	0	1	1110010
Float	1	0	1110011
Float	1	Float	1110100
Float	1	1	1110101
Float	Float	0	1110110
Float	Float	1	1110111
0	Float	0	0101000
0	Float	1	0101001
1	Float	0	0101010
1	Float	1	0101011
0	0	Float	0101100
0	1	Float	0101101
1	0	Float	0101110
1	1	Float	0101111
0	Float	Float	0110101
1	Float	Float	0110110
Float	Float	Float	0110111

**表 7-3. Address Pins and Slave Addresses for the TMP75**

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

### 7.3.2.3 Writing and Reading to the TMP175 and TMP75

Accessing a particular register on the TMP175 and TMP75 devices is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP175 and TMP75 requires a value for the Pointer register (see [Figure 7-2](#)).

When reading from the TMP175 and TMP75 devices, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a slave address byte with the R/  $\bar{W}$  bit low, followed by the Pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/  $\bar{W}$  bit high to initiate the read command. See [Figure 7-4](#) for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP175 and TMP75 remember the Pointer register value until the value is changed by the next write operation.

Register bytes are sent MSB first, followed by the LSB.

### 7.3.2.4 Slave Mode Operations

The TMP175 and TMP75 can operate as a slave receiver or slave transmitter.

#### 7.3.2.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/  $\bar{W}$  bit low. The TMP175 or TMP75 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The TMP175 or TMP75 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP175 and TMP75 acknowledge reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

#### 7.3.2.4.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/  $\bar{W}$  bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

### 7.3.2.5 SMBus Alert Function

The TMP175 and TMP75 support the SMBus Alert function. When the TMP75 and TMP175 are operating in interrupt mode (TM = 1), the ALERT pin of the TMP75 or TMP175 can be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP75 or TMP175 is active, the devices acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding  $T_{HIGH}$  or falling below  $T_{LOW}$  caused the ALERT

condition. This bit is high if the temperature is greater than or equal to  $T_{HIGH}$ . This bit is low if the temperature is less than  $T_{LOW}$ . See [Figure 7-5](#) for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determine which device clears its ALERT status. If the TMP75 or TMP175 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP75 or TMP175 loses the arbitration, its ALERT pin remains active.

### 7.3.2.6 General Call

The TMP175 and TMP75 respond to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP175 and TMP75 latch the status of their address pins, but do not reset. If the second byte is 00000110, the TMP175 and TMP75 latch the status of their address pins and reset their internal registers to their power-up values.

### 7.3.2.7 High-Speed Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP175 and TMP75 devices do not acknowledge this byte, but do switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 2 MHz. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP175 and TMP75 switch the input and output filter back to fast-mode operation.

### 7.3.2.8 Time-out Function

The TMP175 resets the serial interface if either SCL or SDA is held low for 54 ms (typical) between a START and STOP condition. The TMP175 releases the bus if it is pulled low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

## 7.3.3 Timing Diagrams

The TMP175 and TMP75 devices are two-wire, SMBus, and I<sup>2</sup>C interface-compatible. [Figure 7-1](#) to [Figure 7-5](#) describe the various operations on the TMP175. The following list provides bus definitions. Parameters for [Figure 7-1](#) are defined in the [I<sup>2</sup>C Interface Timing](#).

**Bus Idle:** Both SDA and SCL lines remain high.

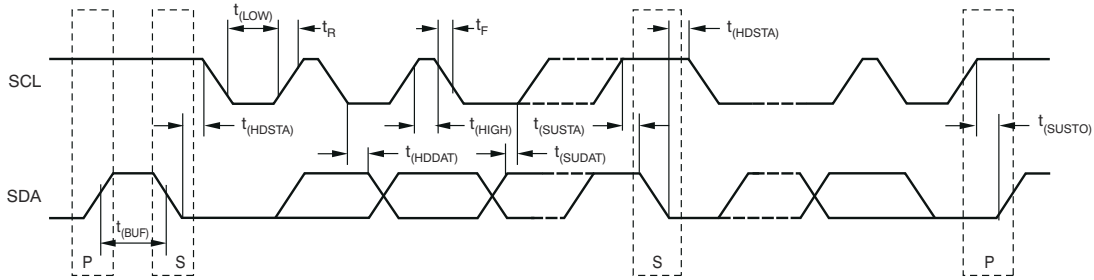
**Start Data Transfer:** A change in the state of the SDA line, from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

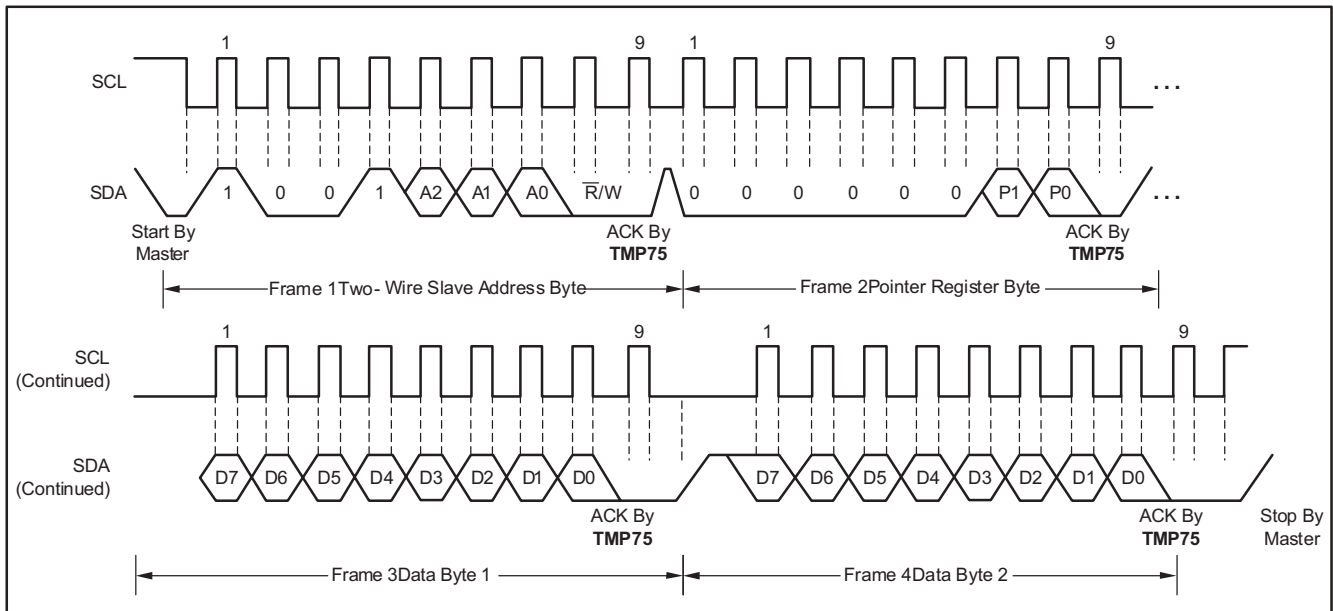
**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that is transmitted by the slave.

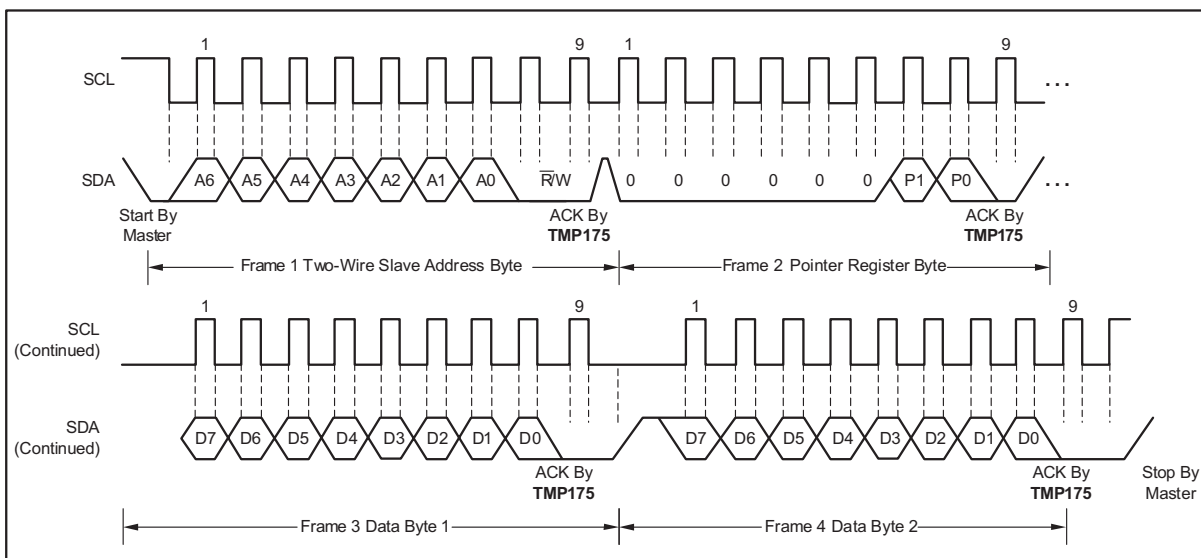
### 7.3.4 Two-Wire Timing Diagrams



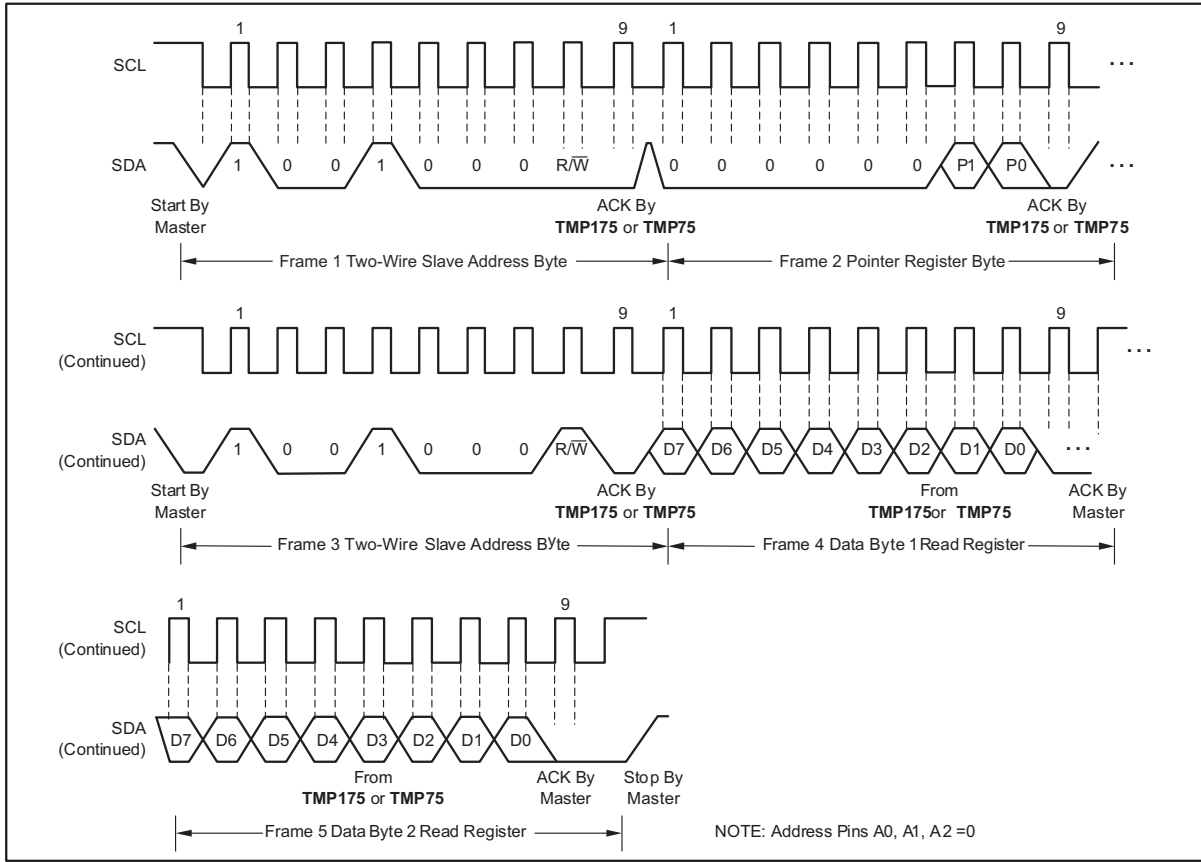
7-1. Two-Wire Timing Diagram



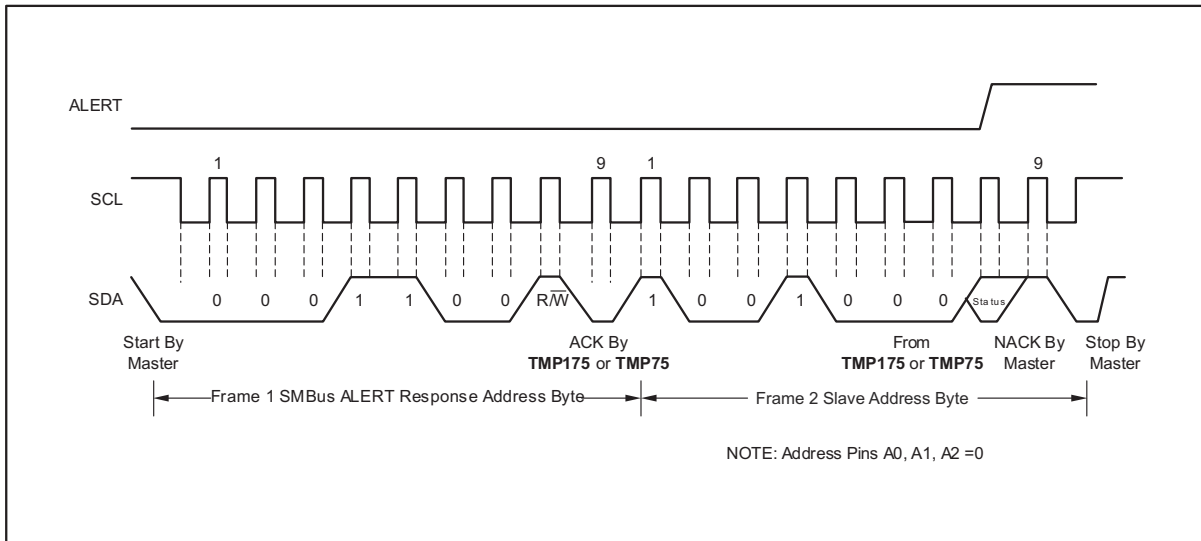
7-2. Two-Wire Timing Diagram for the TMP75 Write Word Format



7-3. Two-Wire Timing Diagram for the TMP175 Write Word Format



**Figure 7-4. Two-Wire Timing Diagram for Read Word Format**



**Figure 7-5. Timing Diagram for SMBus ALERT**

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode (SD)

The shutdown mode of the TMP175 and TMP75 devices lets the user save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1  $\mu\text{A}$ . Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

### 7.4.2 One-shot (OS)

The TMP175 and TMP75 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP175 and TMP75 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

### 7.4.3 Thermostat Mode (TM)

The thermostat mode bit of the TMP175 and TMP75 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the [High and Low Limit Registers](#) section.

#### 7.4.4 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the  $T_{(\text{HIGH})}$  register and remains active until the temperature falls below the value in the  $T_{(\text{LOW})}$  register. For more information on the comparator mode, see the [High and Low Limit Registers](#) section.

#### 7.4.5 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds  $T_{(\text{HIGH})}$  or goes below  $T_{(\text{LOW})}$  registers. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the [High and Low Limit Registers](#) section.

## 7.5 Programming

### 7.5.1 Pointer Register

Figure 7-6 shows the internal register structure of the TMP175 and TMP75. The 8-bit Pointer register of the devices is used to address a given data register. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 7-4 identifies the bits of the Pointer register byte. Table 7-5 describes the pointer address of the registers available in the TMP175 and TMP75. Power-up reset value of P1/P0 is 00.

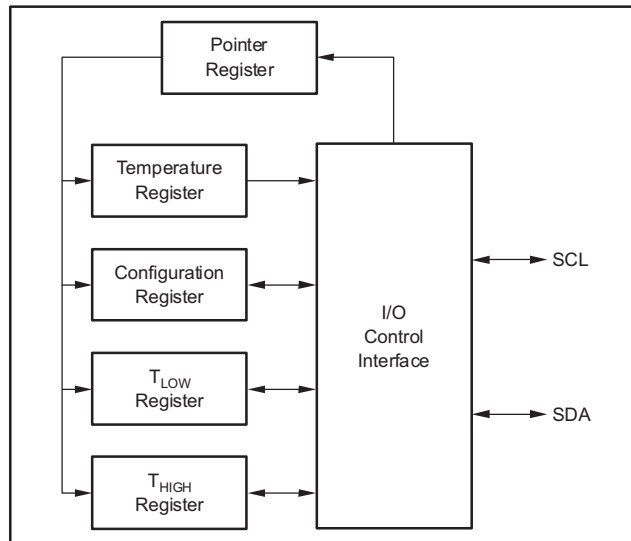


Figure 7-6. Internal Register Structure of the TMP175 and TMP75

#### 7.5.1.1 Pointer Register Byte (pointer = N/A) [reset = 00h]

Table 7-4. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

#### 7.5.1.2 Pointer Addresses of the TMP175

Table 7-5. Pointer Addresses of the TMP175 and TMP75

P1	P0	TYPE	REGISTER
0	0	R only, default	Temperature register
0	1	R/W	Configuration register
1	0	R/W	T <sub>LOW</sub> register
1	1	R/W	T <sub>HIGH</sub> register

## 7.5.2 Temperature Register

The Temperature register of the TMP175 or TMP75 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in [表 7-6](#) and [表 7-7](#). Byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Following power-up or reset value, the Temperature register reads 0 °C until the first conversion is complete.

**表 7-6. Byte 1 of the Temperature Register**

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

**表 7-7. Byte 2 of the Temperature Register**

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

## 7.5.3 Configuration Register

The Configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP175 and TMP75 is shown in [表 7-8](#), followed by a breakdown of the register bits. The power-up or reset value of the Configuration register are all bits equal to 0.

**表 7-8. Configuration Register Format**

D7	D6	D5	D4	D3	D2	D1	D0
OS	R1	R0	F1	F0	POL	TM	SD

### 7.5.3.1 Shutdown Mode (SD)

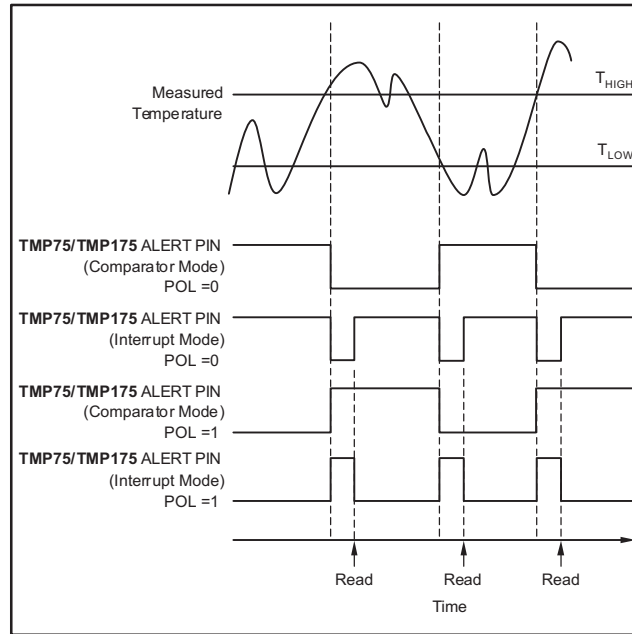
The shutdown mode of the TMP175 and TMP75 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1  $\mu$ A. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

### 7.5.3.2 Thermostat Mode (TM)

The thermostat mode bit of the TMP175 and TMP75 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the [High and Low Limit Registers](#) section.

### 7.5.3.3 Polarity (POL)

The polarity bit of the TMP175 lets the user adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is illustrated in [Figure 7-7](#).



**图 7-7. Output Transfer Function Diagrams**

### 7.5.3.4 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the  $T_{HIGH}$  and  $T_{LOW}$  registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. [Table 7-9](#) defines the number of measured faults that can be programmed to trigger an alert condition in the device. For  $T_{HIGH}$  and  $T_{LOW}$  register format and byte order, see the [High and Low Limit Registers](#) section.

**表 7-9. Fault Settings of the TMP175 and TMP75**

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4 (TMP175); 3 (TMP75)
1	1	6 (TMP175); 4 (TMP75)

### 7.5.3.5 Converter Resolution (R1/R0)

The converter resolution bits control the resolution of the internal ADC converter. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. 表 7-10 identifies the resolution bits and the relationship between resolution and conversion time.

表 7-10. Resolution of the TMP175 and TMP75

R1	R0	RESOLUTION	CONVERSION TIME (Typical)
0	0	9 bits (0.5 °C)	27.5 ms
0	1	10 bits (0.25 °C)	55 ms
1	0	11 bits (0.125 °C)	110 ms
1	1	12 bits (0.0625 °C)	220 ms

### 7.5.3.6 One-Shot (OS)

The TMP175 and TMP75 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP175 and TMP75 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

### 7.5.4 High and Low Limit Registers

In comparator mode (TM = 0), the ALERT pin of the TMP175 and TMP75 becomes active when the temperature equals or exceeds the value in  $T_{HIGH}$  and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated  $T_{LOW}$  value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds  $T_{HIGH}$  for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it only become active again by the temperature falling below  $T_{LOW}$ . When the temperature falls below  $T_{LOW}$ , the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds  $T_{HIGH}$ . The ALERT pin can also be cleared by resetting the device with the general call reset command. This action also clears the state of the internal registers in the device by returning the device to comparator mode (TM = 0). Changing thermostat mode on the TMP75 will clear existing alert in either mode.

Both operational modes are represented in 图 7-7. 表 7-11, 表 7-12, 表 7-13, and 表 7-14 describe the format for the  $T_{HIGH}$  and  $T_{LOW}$  registers. The most significant byte is sent first, followed by the least significant byte. Power-up reset values for  $T_{HIGH}$  and  $T_{LOW}$  are:

$$T_{HIGH} = 80\text{ }^{\circ}\text{C and } T_{LOW} = 75\text{ }^{\circ}\text{C}$$

The format of the data for  $T_{HIGH}$  and  $T_{LOW}$  is the same as for the Temperature register.

**表 7-11. Byte 1 of the  $T_{HIGH}$  Register**

D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4

**表 7-12. Byte 2 of the  $T_{HIGH}$  Register**

D7	D6	D5	D4	D3	D2	D1	D0
H3	H2	H1	H0	0	0	0	0

**表 7-13. Byte 1 of the  $T_{LOW}$  Register**

D7	D6	D5	D4	D3	D2	D1	D0
L11	L10	L9	L8	L7	L6	L5	L4

**表 7-14. Byte 2 of the  $T_{LOW}$  Register**

D7	D6	D5	D4	D3	D2	D1	D0
L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature,  $T_{HIGH}$ , and  $T_{LOW}$  registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in  $T_{HIGH}$  and  $T_{LOW}$  can affect the ALERT output even if the converter is configured for 9-bit resolution.

## 8 Application and Implementation

### Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The TMP175 and TMP75 devices are used to measure the PCB temperature of the location it is mounted. The TMP175 and TMP75 feature SMBus, two-wire, and I<sup>2</sup>C interface compatibility, with the TMP175 allowing up to 27 devices on one bus and the TMP75 allowing up to eight devices on one bus. The TMP175 and TMP75 both feature an SMBus Alert function. The TMP175 and TMP75 require no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although a 0.01- $\mu$ F bypass capacitor is recommended.

The sensing device of the TMP175 and TMP75 devices is the device itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

### 8.2 Typical Application

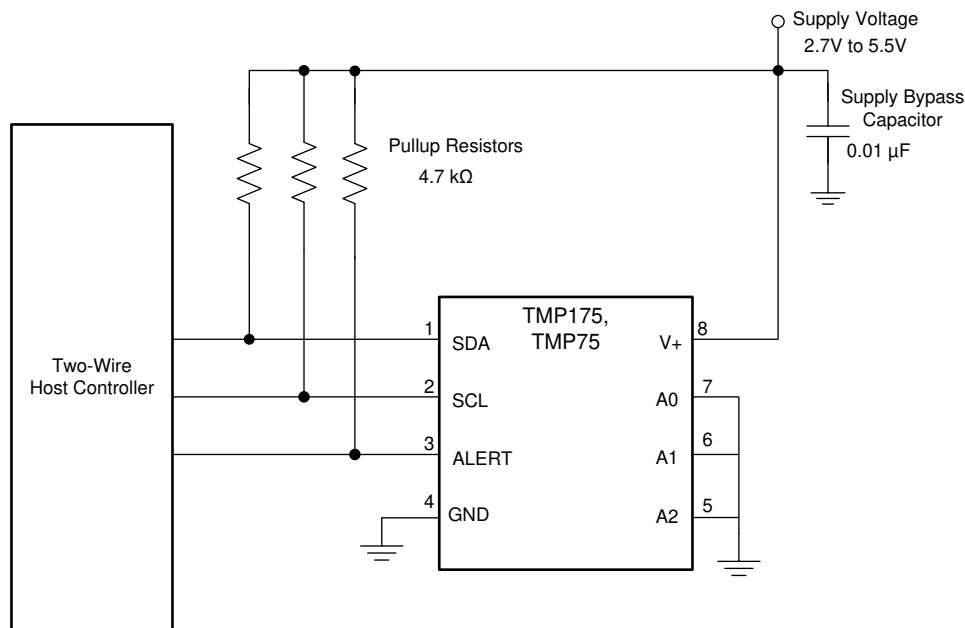


図 8-1. Typical Connections of the TMP175 and TMP75

#### 8.2.1 Design Requirements

The TMP175 and TMP75 devices requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistor is 4.7 k $\Omega$ . In some applications the pullup resistor can be lower or higher than 4.7 k $\Omega$  but must not exceed 3 mA of current on the SCL and SDA pins, and must not exceed 4 mA on the ALERT pin. A 0.01- $\mu$ F bypass capacitor is recommended, as shown in 图 8-1. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than  $V_S$  through the pullup resistors. For TMP175, to configure one of 27 different addresses on the bus, connect A0, A1, and A2 to either the GND or V+ pin, or float. Float indicates the pin is left unconnected. For the TMP75, to configure one of eight different addresses on the bus, connect A0, A1, and A2 to either the GND or V+ pin.

### 8.2.2 Detailed Design Procedure

Place the TMP175 and TMP75 devices in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

### 8.2.3 Application Curve

Figure 8-2 shows the step response of the TMP175 and TMP75 devices to a submersion in an oil bath of 100 °C from room temperature (27 °C). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 s. The time-constant result depends on the printed-circuit-board (PCB) that the TMPx175 devices are mounted. For this test, the TMP175 and TMP75 devices were soldered to a two-layer PCB that measured 0.375 inch × 0.437 inch.

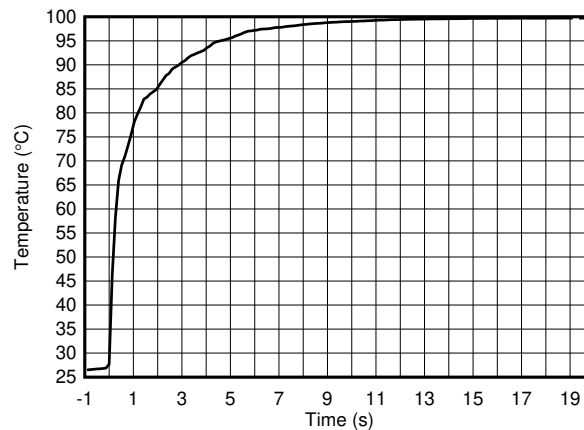


Figure 8-2. Temperature Step Response

## 9 Power Supply Recommendations

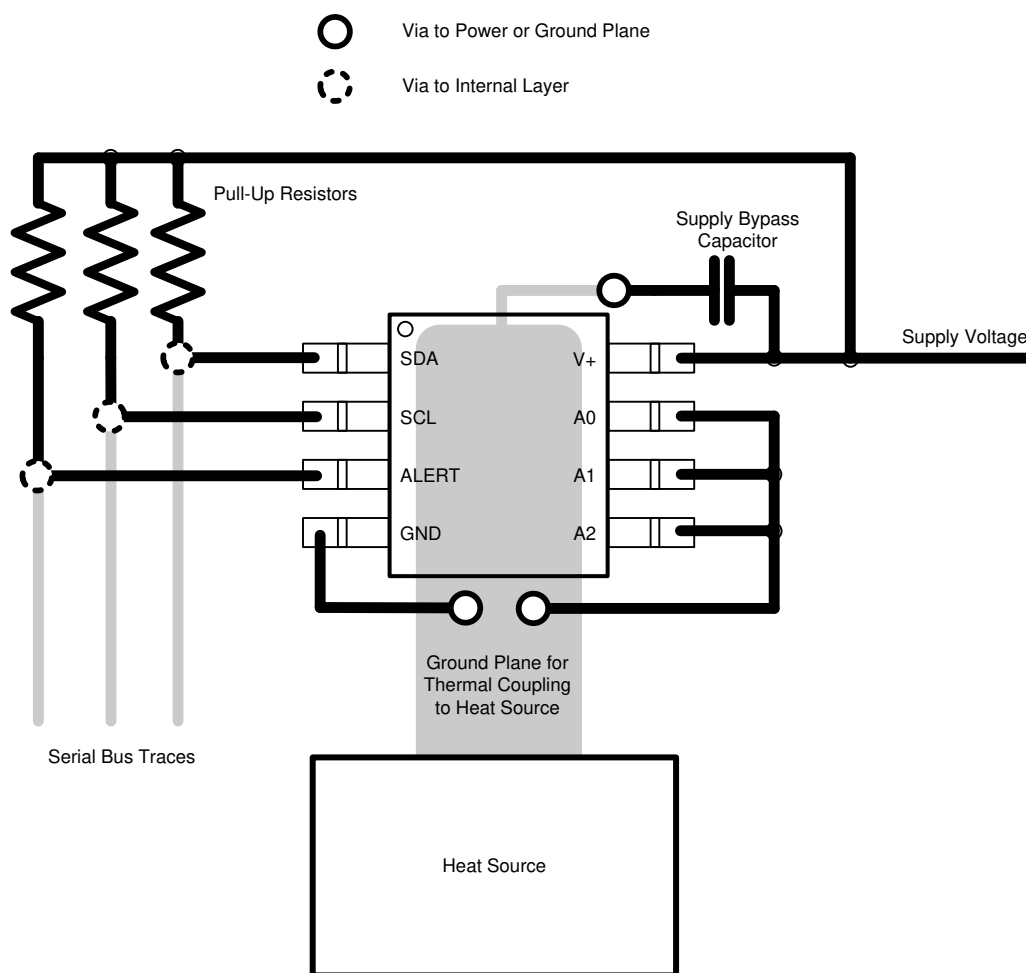
The TMP175 and TMP75 devices operate with a power supply in the range of 2.7 V to 5.5 V. A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01  $\mu\text{F}$ . Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

## 10 Layout

### 10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01  $\mu\text{F}$ . Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins SDA, SCL, and ALERT through 4.7-k $\Omega$  pullup resistors.

### 10.2 Layout Example



**10-1. Layout Example**

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.

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### 11.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TMP175AID</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	TMP175
<a href="#">TMP175AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DABQ
TMP175AIDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DABQ
<a href="#">TMP175AIDGKT</a>	Obsolete	Production	VSSOP (DGK)   8	-	-	Call TI	Call TI	-40 to 125	DABQ
<a href="#">TMP175AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMP175
TMP175AIDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMP175
<a href="#">TMP75AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	T127
TMP75AIDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T127
TMP75AIDGKR1G4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	-	Call TI	Call TI	-40 to 125	T127
<a href="#">TMP75AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	Call TI   Nipdau	Level-1-260C-UNLIM	-40 to 125	TMP75
TMP75AIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	TMP75
TMP75AIDR1G4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMP75
TMP75AIDR1G4.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMP75

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TMP175, TMP75 :**

- Automotive : [TMP175-Q1](#), [TMP75-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP175AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP175AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP175AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP75AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMP75AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP75AIDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP175AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP175AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
TMP175AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TMP75AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	36.0
TMP75AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP75AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TMP75AIDR1G4	SOIC	D	8	2500	353.0	353.0	32.0

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

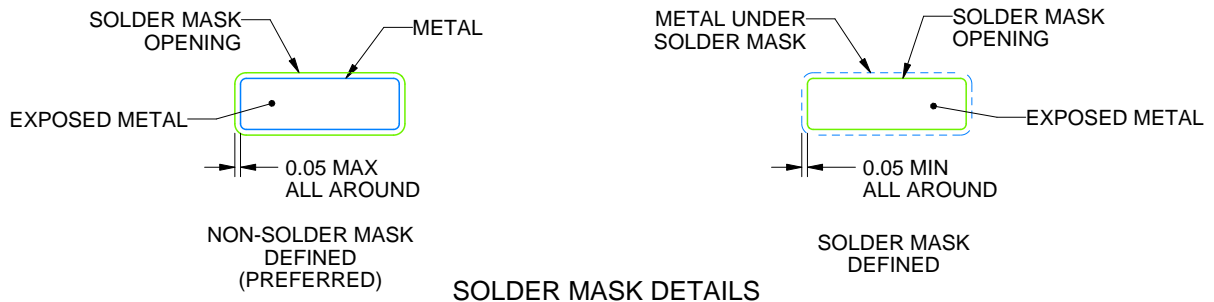
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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