# TMS320C6742™ 固定および浮動小数点DSP

## 1 デバイスの概要

### 1.1 特長

- 200MHz C674x固定/浮動小数点VLIW DSP
- C674x 命令セット機能
  - C67x+およびC64x+ ISAのスーパーセット
  - 上限値: 1600MIPS、1200 MFLOPS
  - アドレス可能バイト(8/16/32/64ビット・データ)
  - 8ビット オーバーフロー保護
  - ビット・フィールドの抽出、セット、クリア
  - 正規化、飽和、ビット・カウント
  - 16ビットのコンパクトな命令群
- C674x レベル2 キャッシュ・メモリ・アーキテクチャ
  - 32KB L1PプログラムRAM/キャッシュ
  - 32KB L1DデータRAM/キャッシュ
  - 64KB マッピングされたユニファイド L2 RAM/キャッシュ
  - フレキシブルなRAM/キャッシュ・パーティション(L1およびL2)
- 拡張ダイレクト・メモリ・アクセス・コントローラ3（EDMA 3）:
  - チャネル・コントローラ×2
  - 転送コントローラ×3
  - 独立したDMAチャネル×64
  - クイックDMAチャネル×16
  - プログラマブルなバースト転送サイズ
- TMS320C674x 浮動小数点 VLIW DSPコア
  - 非アラインド・サポート付きのロード/ストア・アーキテクチャ
  - 汎用32ビット・レジスタ×64
  - 32/40ビットALU機能ユニット×6
    - 32ビット整数、SP (IEEE単精度/32ビット)およびDP (IEEE倍精度/64ビット)浮動小数点をサポート
    - 1クロックにSPを4つまで追加すること、2クロック毎にDPを4つまで追加することをサポート
    - サイクル毎の平方根逆数近似(RSQRxP)操作、浮動小数点(SPまたはDP)逆数近似(RCPxP) 2回までをサポート
  - 2つの乗算機能ユニット:
    - 混合精度IEEE浮動小数点乗算のサポート範囲:
      - 2 SP × SP → SP (1クロックごと)
      - 2 SP × SP → DP (2クロックごと)
      - 2 SP × DP → DP (3クロックごと)
      - 2 DP × DP → DP (4クロックごと)
    - 固定小数点乗算では、クロック・サイクルごとに32×32ビット乗算2回、16×16ビット乗算4回、8×8ビット乗算8回のいずれかと、複素乗算をサポート
  - 命令パッキングによるコード・サイズの削減
  - 全命令の条件
  - モジュロ・ループ操作へのハードウェアによるサポート
  - 保護されたモード操作
  - エラー検出とプログラム・リダイレクト用の例外サポート
- ソフトウェア・サポート:
  - TI DSP BIOS™
  - チップ・サポートおよびDSPライブラリ
- 1.8Vまたは3.3V LVCMOS I/O (DDR2インターフェイスを除く)
- 2種の外部メモリ・インターフェイス:
  - EMIFA
    - NOR (8または16ビット幅データ)
    - NAND (8または16ビット幅データ)
    - 128MBアドレス空間の16ビットSDRAM
  - 次のいずれかを使用するDDR2/Mobile DDRメモリ・コントローラ
    - 256MBアドレス空間の16ビットDDR2 SDRAM
    - 256MBアドレス空間の16ビットmDDR SDRAM
- 構成可能な16550 UARTモジュール×1:
  - モデム制御信号機能
  - 16バイトFIFO
  - 16xまたは13x のオーバー・サンプリング・オプション
- 1つのシリアル・ペリフェラル・インターフェイス(SPI)、複数のチップ・セレクトを搭載
- 2つのマスタおよびスレーブ$I^2C$ Bus™
- 1つのホスト・ポート・インターフェイス(HPI)、16ビット幅の多重化アドレス/データ・バスにより広帯域幅を実現

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- マルチチャネル・オーディオ・シリアル・ポート (McASP)×1:
  - 2つのクロック・ゾーンと16本のシリアル・データ・ピン
  - TDM、I2S、類似フォーマットをサポート
  - DIT可能
  - 送受信用FIFOバッファ
- 1 マルチチャネル・バッファ・シリアル・ポート (McBSP):
  - TDM、I2S、類似フォーマットをサポート
  - AC97 オーディオ・コーデック・インターフェイス
  - 通信インターフェイス (ST-Bus、H100)
  - 128チャネルTDM
  - 送受信用FIFOバッファ
- 32kHz発振器と個別の電源レールを持つリアルタイム・クロック(RTC)
- 64ビット汎用タイマ(32ビット タイマ2個として構成可能)×1
- 64ビット汎用タイマ、またはウォッチドッグ・タイマ(32ビット タイマ2個として構成可能)×1
- 高分解能拡張パルス幅変調回路(eHRPWM)×2:
  - 周期および周波数制御機能付きの専用16ビット・タイム・ベース・カウンタ
  - シングル・エッジ出力×6、デュアル・エッジ対称出力×6、またはデュアル・エッジ非対称出力×3
  - デッドバンド生成
  - 高周波数キャリアによるPWMチョッピング
  - トリップ・ゾーン入力
- 32ビット拡張入力キャプチャ(eCAP) モジュール:
  - キャプチャ入力(×3)、または補助パルス幅変調回路(APWM)出力(×3)として構成可能
  - 最大4つのイベント・タイムスタンプをシングル・ショットでキャプチャ
- パッケージ:
  - 361ボール 鉛フリー・プラスチック・ボール・グリッド・アレイ(PBGA) [ZCEサフィックス]、0.65mm ボール・ピッチ
  - 361ボール 鉛フリーPBGA [ZWTサフィックス]、0.80mm ボール・ピッチ
- 商用、または拡張温度


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## 1.2 アプリケーション

- 貨幣検査
- 生体認証による識別
- マシン・ビジョン(ローエンド)

## 1.3 概要

TMS320C6742 固定および浮動小数点DSPは、C674x DSPコアを基礎とする、低消費電力のアプリケーション・プロセッサです。このDSPは、TMS320C6000™ DSPプラットフォームの他のプロセッサよりもはるかに少ない電力を実現します。

このデバイスにより、相手先ブランドの製造業者(OEM)と相手先ブランドの設計製造業者(ODM)が、完全に統合されたミックスド・プロセッサ・ソリューションの柔軟性を最大限に生かしたプロセッサ性能、堅牢なオペレーティング・システム、豊富なユーザー・インターフェイスを持つデバイスを、迅速に売り出すことが可能になります。

デバイスのDSPコアでは、2レベルのキャッシュ・ベース・アーキテクチャが使用されています。

レベル1のプログラム・キャッシュ(L1P)は32KB ダイレクト・マップ・キャッシュで、レベル1のデータ・キャッシュ(L1D)は32KB 2ウェイ、セット・アソシエイティブ・キャッシュです。レベル 2・プログラム・キャッシュ(L2P)は、プログラムおよびデータ空間で共有される64KBのメモリ空間で構成されています。L2メモリは、マップされたメモリ、キャッシュ、またはこれらの組み合わせとして構成可能です。

ペリフェラル・セットは、以下を含みます: $I^2C$ Busインターフェイス×1; 16個のシリアライザとFIFOバッファ付きマルチチャネル・オーディオ・シリアル・ポート(McASP)×1; FIFOバッファ付きマルチチャネル・バッファード・シリアル・ポート(McBSP)×1; 複数チップ選択付きのシリアル・ペリフェラル・インターフェイス (SPI)×1; それぞれ構成可能(1つはウォッチドッグとして構成可能)な64ビット汎用タイマ×2; 構成可能な16ビット ホスト・ポート・インターフェイス(HPI)×1; 他のペリフェラルと多重化可能で、プログラマブルな割り込みおよびイベント生成モード付きのピンを各バンクが16ピン含む、汎用入出力(GPIO)ピンのバンク×9(最大); UARTインターフェイス(それぞれが $\overline{\text{RTS}}$と $\overline{\text{CTS}}$を持つ)×1; 高分解能拡張パルス幅変調回路(eHRPWM)ペリフェラル×2; 3つのキャプチャ入力または3つのAPWM出力として構成可能な32ビット拡張キャプチャ(eCAP) モジュール・ペリフェラル×3; 外部メモリ・インターフェイス×2: より低速なメモリまたはペリフェラル向けの非同期およびSDRAM外部メモリ・インターフェイス(EMIFA)×1; より高速なDDR2/Mobile DDR コントローラ×1。

豊富なペリフェラル・セットは、外部ペリフェラル・デバイスを制御する機能と、外部プロセッサと通信する機能を提供します。各ペリフェラルの詳細については、本書の関連セクションと、関連ペリフェラルのリファレンス・ガイドを参照してください。

デバイスには、DSP向けの開発ツールの一式が含まれます。これらのツールには、Cコンパイラ、プログラミングとスケジューリングを簡略化するDSPアセンブリ・オプティマイザ、およびソース・コードの実行を見やすくする Windows®デバッガ・インターフェイスが含まれています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ |
|---|---|---|
| TMS320C6742ZCE | NFBGA (361) | 13.00mm×13.00mm |
| TMS320C6742ZWT | NFBGA (361) | 16.00mm×16.00mm |

(1) これらのデバイスの詳細については、「8」を参照してください。

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## 1.4 機能ブロック図

デバイスの機能ブロック図を図 1-1に示します。

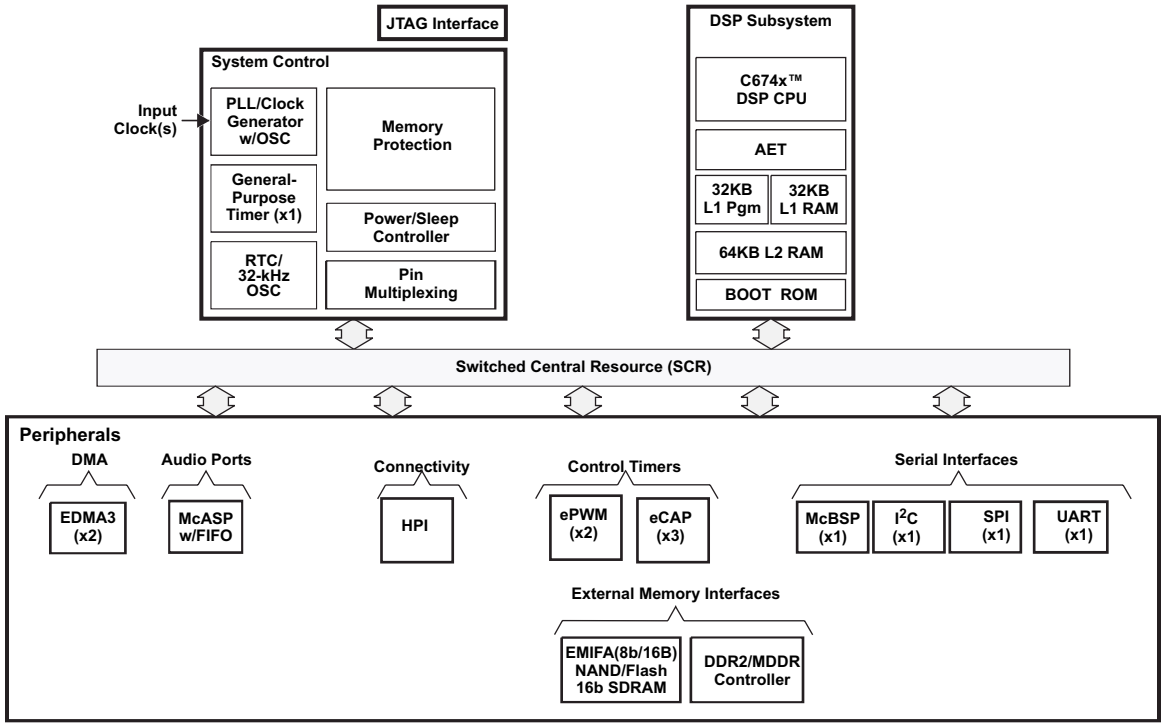



**図 1-1. 機能ブロック図**


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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from March 31, 2014 to January 31, 2017 | Page |
|---|---|
| • Removed internal pullup designation from $\overline{\text{RESET}}$ in Table 3-5 | 25 |
| • Added footnote to CLKOUT Description in Table 3-6 | 26 |


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# 3 Device Comparison

## 3.1 Device Characteristics

Table 3-1 provides an overview of the device. The table shows significant features of the device, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

**Table 3-1. Characteristics of C6742**

| HARDWARE FEATURES | | C6742 |
|---|---|---|
| Peripherals<br>Not all peripherals pins are available at the same time (for more detail, see the Device Configurations section). | DDR2/mDDR Memory Controller | DDR2, 16-bit bus width, up to 156 MHz<br>Mobile DDR, 16-bit bus width, up to 150 MHz |
| | EMIFA | Asynchronous (8/16-bit bus width) RAM, Flash, 16-bit SDRAM, NOR, NAND |
| | EDMA3 | 64 independent channels, 16 QDMA channels, 2 channel controllers, 3 transfer controllers |
| | Timers | 2 64-Bit General Purpose (each configurable as 2 separate 32-bit timers, one configurable as Watch Dog) |
| | UART | 1 (with RTS and CTS flow control) |
| | SPI | 1 (with one hardware chip select) |
| | $I^2C$ | 1 ( Master/Slave) |
| | Multichannel Audio Serial Port [McASP] | 1 (each with transmit/receive, FIFO buffer, 16 serializers) |
| | Multichannel Buffered Serial Port [McBSP] | 1 (with transmit/receive, FIFO buffer, 16) |
| | eHRPWM | 4 Single Edge, 4 Dual Edge Symmetric, or 2 Dual Edge Asymmetric Outputs |
| | eCAP | 3 32-bit capture inputs or 3 32-bit auxiliary PWM outputs |
| | UHPI | 1 (16-bit multiplexed address/data) |
| | General-Purpose Input/Output Port | 9 banks of 16-bit |
| On-Chip Memory | Size (Bytes) | 128KB RAM |
| | Organization | **DSP**<br>32KB L1 Program (L1P)/Cache (up to 32KB)<br>32KB L1 Data (L1D)/Cache (up to 32KB)<br>64KB Unified Mapped RAM/Cache (L2)<br>DSP Memories can be made accessible to EDMA3 and other peripherals. |
| C674x CPU ID + CPU Rev ID | Control Status Register (CSR.[31:16]) | 0x1400 |
| C674x Megamodule Revision | Revision ID Register (MM_REVID[15:0]) | 0x0000 |
| JTAG BSDL_ID | DEVIDR0 Register | see Section 6.24.4.1, *JTAG Peripheral Register Description* |
| CPU Frequency | MHz | 674x DSP 200 MHz |
| Voltage | Core (V) | Variable (1.2 V - 1.0V) |
| | I/O (V) | 1.8V or 3.3 V |
| Packages | | 13 mm x 13 mm, 361-Ball 0.65 mm pitch, PBGA (ZCE) |
| | | 16 mm x 16 mm, 361-Ball 0.80 mm pitch, PBGA (ZWT) |
| Product Status(1) | Product Preview (PP), Advance Information (AI), or Production Data (PD) | PD |

(1) ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice. PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## 3.2 Device Compatibility

The C674x DSP core is code-compatible with the C6000™ DSP platform and supports features of both the C64x+ and C67x+ DSP families.

## 3.3 DSP Subsystem

The DSP Subsystem includes the following features:

- C674x DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB)
- 32KB L1 Data (L1D)/Cache (up to 32KB)
- 64KB Unified Mapped RAM/Cache (L2)
- Boot ROM (cannot be used for application code)
- Little endian

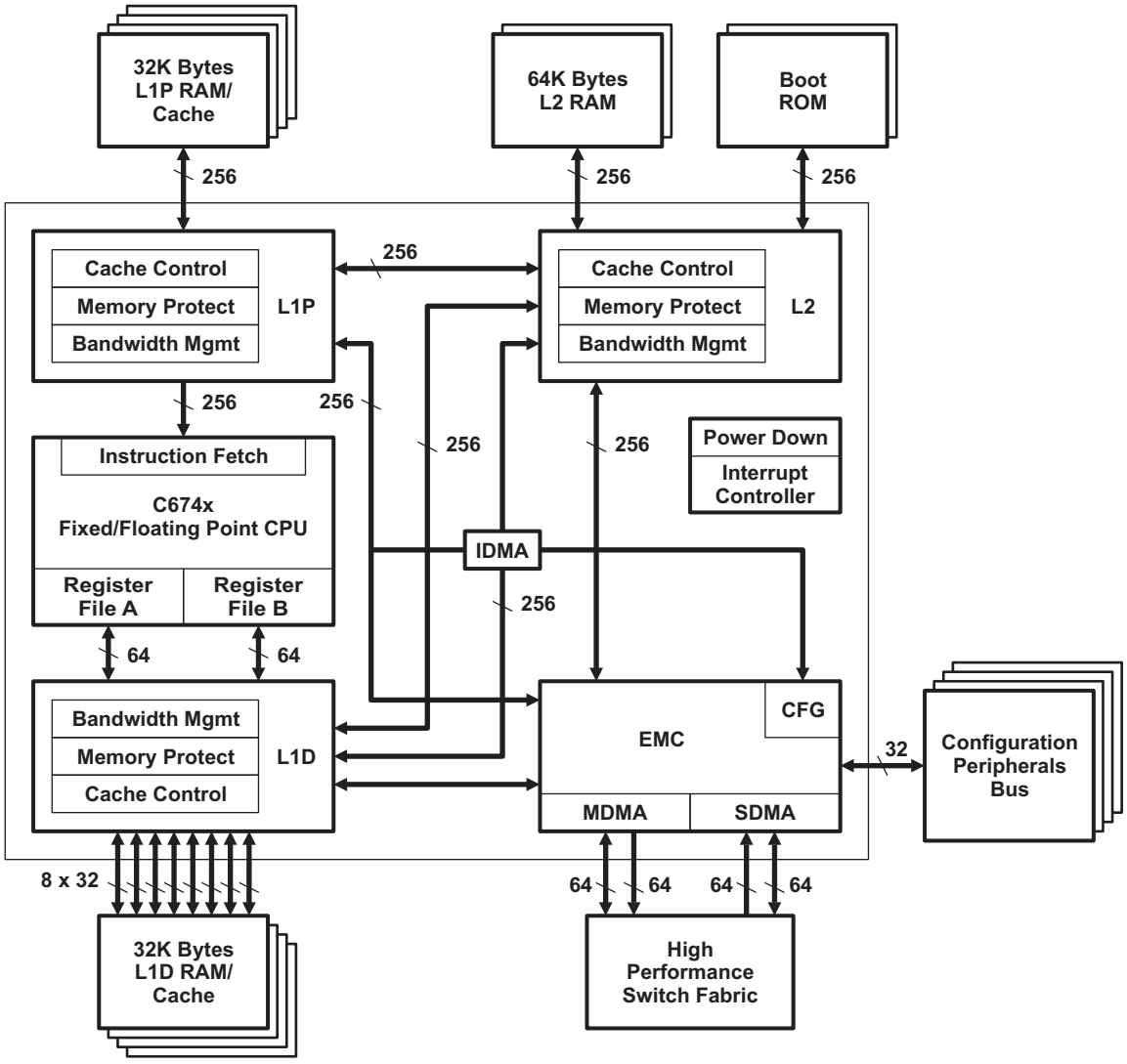



**Figure 3-1. C674xMegamodule Block Diagram**


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### 3.3.1 C674x DSP CPU Description

The C674x Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 3-2. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C674x CPU combines the performance of the C64x+ core with the floating-point capabilities of the C67x+ core.

Each C674x .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C674x core enhances the .S unit in several ways. On the previous cores, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C674x core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C674x compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C674x CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.

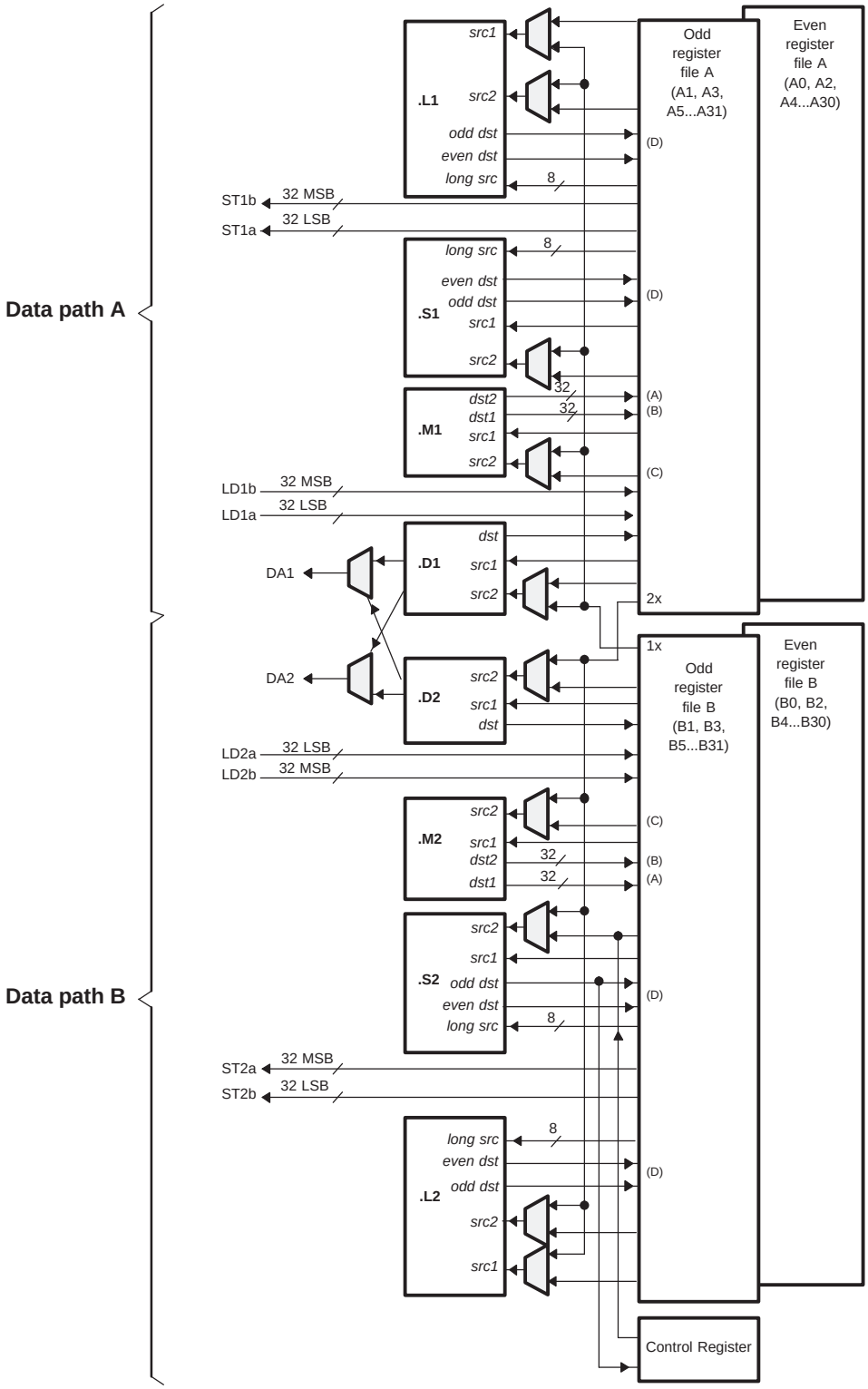
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- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C674x CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRUFE8)
- *TMS320C64x Technical Overview* (literature number SPRU395)


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A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

**Figure 3-2. TMS320C674x CPU (DSP Core) Data Paths**

### 3.3.2 DSP Memory Mapping

The DSP memory map is shown in Section 3.4.

By default the DSP also has access to most on and off chip memory areas.

Additionally, the DSP megamodule includes the capability to limit access to its internal memories through its SDMA port; without needing an external MPU unit.

#### 3.3.2.1 External Memories

The DSP has access to the following External memories:

- Asynchronous EMIF / SDRAM / NAND / NOR Flash (EMIFA)
- SDRAM (DDR2)

#### 3.3.2.2 DSP Internal Memories

The DSP has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

#### 3.3.2.3 C674x CPU

The C674x core uses a two-level cache-based architecture. The Level 1 Program cache (L1P) is 32 KB direct mapped cache and the Level 1 Data cache (L1D) is 32 KB 2-way set associated cache. The Level 2 memory/cache (L2) consists of a 64 KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or a combination of both.

Table 3-2 shows a memory map of the C674x CPU cache registers for the device.

**Table 3-2. C674x Cache Registers**

| Byte Address | Register Name | Register Description |
|---|---|---|
| 0x0184 0000 | L2CFG | L2 Cache configuration register |
| 0x0184 0020 | L1PCFG | L1P Size Cache configuration register |
| 0x0184 0024 | L1PCC | L1P Freeze Mode Cache configuration register |
| 0x0184 0040 | L1DCFG | L1D Size Cache configuration register |
| 0x0184 0044 | L1DCC | L1D Freeze Mode Cache configuration register |
| 0x0184 0048 - 0x0184 0FFC | - | Reserved |
| 0x0184 1000 | EDMAWEIGHT | L2 EDMA access control register |
| 0x0184 1004 - 0x0184 1FFC | - | Reserved |
| 0x0184 2000 | L2ALLOC0 | L2 allocation register 0 |
| 0x0184 2004 | L2ALLOC1 | L2 allocation register 1 |
| 0x0184 2008 | L2ALLOC2 | L2 allocation register 2 |
| 0x0184 200C | L2ALLOC3 | L2 allocation register 3 |
| 0x0184 2010 - 0x0184 3FFF | - | Reserved |
| 0x0184 4000 | L2WBAR | L2 writeback base address register |
| 0x0184 4004 | L2WWC | L2 writeback word count register |
| 0x0184 4010 | L2WIBAR | L2 writeback invalidate base address register |
| 0x0184 4014 | L2WIWC | L2 writeback invalidate word count register |
| 0x0184 4018 | L2IBAR | L2 invalidate base address register |
| 0x0184 401C | L2IWC | L2 invalidate word count register |
| 0x0184 4020 | L1PIBAR | L1P invalidate base address register |
| 0x0184 4024 | L1PIWC | L1P invalidate word count register |
| 0x0184 4030 | L1DWIBAR | L1D writeback invalidate base address register |


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**Table 3-2. C674x Cache Registers (continued)**

| Byte Address | Register Name | Register Description |
|---|---|---|
| 0x0184 4034 | L1DWIWC | L1D writeback invalidate word count register |
| 0x0184 4038 | - | Reserved |
| 0x0184 4040 | L1DWBAR | L1D Block Writeback |
| 0x0184 4044 | L1DWWC | L1D Block Writeback |
| 0x0184 4048 | L1DIBAR | L1D invalidate base address register |
| 0x0184 404C | L1DIWC | L1D invalidate word count register |
| 0x0184 4050 - 0x0184 4FFF | - | Reserved |
| 0x0184 5000 | L2WB | L2 writeback all register |
| 0x0184 5004 | L2WBINV | L2 writeback invalidate all register |
| 0x0184 5008 | L2INV | L2 Global Invalidate without writeback |
| 0x0184 500C - 0x0184 5027 | - | Reserved |
| 0x0184 5028 | L1PINV | L1P Global Invalidate |
| 0x0184 502C - 0x0184 5039 | - | Reserved |
| 0x0184 5040 | L1DWB | L1D Global Writeback |
| 0x0184 5044 | L1DWBINV | L1D Global Writeback with Invalidate |
| 0x0184 5048 | L1DINV | L1D Global Invalidate without writeback |
| 0x0184 8000 – 0x0184 80FF | MAR0 - MAR63 | Reserved 0x0000 0000 – 0x3FFF FFFF |
| 0x0184 8100 – 0x0184 817F | MAR64 – MAR95 | Memory Attribute Registers for EMIFA SDRAM Data (CS0)<br>External memory addresses 0x4000 0000 – 0x5FFF FFFF |
| 0x0184 8180 – 0x0184 8187 | MAR96 - MAR97 | Memory Attribute Registers for EMIFA Async Data (CS2)<br>External memory addresses 0x6000 0000 – 0x61FF FFFF |
| 0x0184 8188 – 0x0184 818F | MAR98 – MAR99 | Memory Attribute Registers for EMIFA Async Data (CS3)<br>External memory addresses 0x6200 0000 – 0x63FF FFFF |
| 0x0184 8190 – 0x0184 8197 | MAR100 – MAR101 | Memory Attribute Registers for EMIFA Async Data (CS4)<br>External memory addresses 0x6400 0000 – 0x65FF FFFF |
| 0x0184 8198 – 0x0184 819F | MAR102 – MAR103 | Memory Attribute Registers for EMIFA Async Data (CS5)<br>External memory addresses 0x6600 0000 – 0x67FF FFFF |
| 0x0184 81A0 – 0x0184 81FF | MAR104 – MAR127 | Reserved 0x6800 0000 – 0x7FFF FFFF |
| 0x0184 8200 | MAR128 | Reserved 0x8000 0000 - 0x81FF FFFF |
| 0x0184 8204 – 0x0184 82FF | MAR129 – MAR191 | Reserved 0x8200 0000 – 0xBFFF FFFF |
| 0x0184 8300 – 0x0184 837F | MAR192 – MAR223 | Memory Attribute Registers for DDR2 Data (CS2)<br>External memory addresses 0xC000 0000 – 0xDFFF FFFF |
| 0x0184 8380 – 0x0184 83FF | MAR224 – MAR255 | Reserved 0xE000 0000 – 0xFFFF FFFF |

**Table 3-3. C674x L1/L2 Memory Protection Registers**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A000 | L2MPFAR | L2 memory protection fault address register |
| 0x0184 A004 | L2MPFSR | L2 memory protection fault status register |
| 0x0184 A008 | L2MPFCR | L2 memory protection fault command register |
| 0x0184 A00C - 0x0184 A0FF | - | Reserved |
| 0x0184 A100 | L2MPLK0 | L2 memory protection lock key bits [31:0] |
| 0x0184 A104 | L2MPLK1 | L2 memory protection lock key bits [63:32] |
| 0x0184 A108 | L2MPLK2 | L2 memory protection lock key bits [95:64] |
| 0x0184 A10C | L2MPLK3 | L2 memory protection lock key bits [127:96] |
| 0x0184 A110 | L2MPLKCMD | L2 memory protection lock key command register |
| 0x0184 A114 | L2MPLKSTAT | L2 memory protection lock key status register |
| 0x0184 A118 - 0x0184 A1FF | - | Reserved |
| 0x0184 A200 | L2MPPA0 | L2 memory protection page attribute register 0 (controls memory address 0x0080 0000 - 0x0080 1FFF) |

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**Table 3-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A204 | L2MPPA1 | L2 memory protection page attribute register 1 (controls memory address 0x0080 2000 - 0x0080 3FFF) |
| 0x0184 A208 | L2MPPA2 | L2 memory protection page attribute register 2 (controls memory address 0x0080 4000 - 0x0080 5FFF) |
| 0x0184 A20C | L2MPPA3 | L2 memory protection page attribute register 3 (controls memory address 0x0080 6000 - 0x0080 7FFF) |
| 0x0184 A210 | L2MPPA4 | L2 memory protection page attribute register 4 (controls memory address 0x0080 8000 - 0x0080 9FFF) |
| 0x0184 A214 | L2MPPA5 | L2 memory protection page attribute register 5 (controls memory address 0x0080 A000 - 0x0080 BFFF) |
| 0x0184 A218 | L2MPPA6 | L2 memory protection page attribute register 6 (controls memory address 0x0080 C000 - 0x0080 DFFF) |
| 0x0184 A21C | L2MPPA7 | L2 memory protection page attribute register 7 (controls memory address 0x0080 E000 - 0x0080 FFFF) |
| 0x0184 A220 | L2MPPA8 | L2 memory protection page attribute register 8 (controls memory address 0x0081 0000 - 0x0081 1FFF) |
| 0x0184 A224 | L2MPPA9 | L2 memory protection page attribute register 9 (controls memory address 0x0081 2000 - 0x0081 3FFF) |
| 0x0184 A228 | L2MPPA10 | L2 memory protection page attribute register 10 (controls memory address 0x0081 4000 - 0x0081 5FFF) |
| 0x0184 A22C | L2MPPA11 | L2 memory protection page attribute register 11 (controls memory address 0x0081 6000 - 0x0081 7FFF) |
| 0x0184 A230 | L2MPPA12 | L2 memory protection page attribute register 12 (controls memory address 0x0081 8000 - 0x0081 9FFF) |
| 0x0184 A234 | L2MPPA13 | L2 memory protection page attribute register 13 (controls memory address 0x0081 A000 - 0x0081 BFFF) |
| 0x0184 A238 | L2MPPA14 | L2 memory protection page attribute register 14 (controls memory address 0x0081 C000 - 0x0081 DFFF) |
| 0x0184 A23C | L2MPPA15 | L2 memory protection page attribute register 15 (controls memory address 0x0081 E000 - 0x0081 FFFF) |
| 0x0184 A240 | L2MPPA16 | L2 memory protection page attribute register 16 (controls memory address 0x0082 0000 - 0x0082 1FFF) |
| 0x0184 A244 | L2MPPA17 | L2 memory protection page attribute register 17 (controls memory address 0x0082 2000 - 0x0082 3FFF) |
| 0x0184 A248 | L2MPPA18 | L2 memory protection page attribute register 18 (controls memory address 0x0082 4000 - 0x0082 5FFF) |
| 0x0184 A24C | L2MPPA19 | L2 memory protection page attribute register 19 (controls memory address 0x0082 6000 - 0x0082 7FFF) |
| 0x0184 A250 | L2MPPA20 | L2 memory protection page attribute register 20 (controls memory address 0x0082 8000 - 0x0082 9FFF) |
| 0x0184 A254 | L2MPPA21 | L2 memory protection page attribute register 21 (controls memory address 0x0082 A000 - 0x0082 BFFF) |
| 0x0184 A258 | L2MPPA22 | L2 memory protection page attribute register 22 (controls memory address 0x0082 C000 - 0x0082 DFFF) |
| 0x0184 A25C | L2MPPA23 | L2 memory protection page attribute register 23 (controls memory address 0x0082 E000 - 0x0082 FFFF) |
| 0x0184 A260 | L2MPPA24 | L2 memory protection page attribute register 24 (controls memory address 0x0083 0000 - 0x0083 1FFF) |
| 0x0184 A264 | L2MPPA25 | L2 memory protection page attribute register 25 (controls memory address 0x0083 2000 - 0x0083 3FFF) |
| 0x0184 A268 | L2MPPA26 | L2 memory protection page attribute register 26 (controls memory address 0x0083 4000 - 0x0083 5FFF) |
| 0x0184 A26C | L2MPPA27 | L2 memory protection page attribute register 27 (controls memory address 0x0083 6000 - 0x0083 7FFF) |
| 0x0184 A270 | L2MPPA28 | L2 memory protection page attribute register 28 (controls memory address 0x0083 8000 - 0x0083 9FFF) |


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**Table 3-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A274 | L2MPPA29 | L2 memory protection page attribute register 29 (controls memory address 0x0083 A000 - 0x0083 BFFF) |
| 0x0184 A278 | L2MPPA30 | L2 memory protection page attribute register 30 (controls memory address 0x0083 C000 - 0x0083 DFFF) |
| 0x0184 A27C | L2MPPA31 | L2 memory protection page attribute register 31 (controls memory address 0x0083 E000 - 0x0083 FFFF) |
| 0x0184 A280 | L2MPPA32 | L2 memory protection page attribute register 32 (controls memory address 0x0070 0000 - 0x0070 7FFF) |
| 0x0184 A284 | L2MPPA33 | L2 memory protection page attribute register 33 (controls memory address 0x0070 8000 - 0x0070 FFFF) |
| 0x0184 A288 | L2MPPA34 | L2 memory protection page attribute register 34 (controls memory address 0x0071 0000 - 0x0071 7FFF) |
| 0x0184 A28C | L2MPPA35 | L2 memory protection page attribute register 35 (controls memory address 0x0071 8000 - 0x0071 FFFF) |
| 0x0184 A290 | L2MPPA36 | L2 memory protection page attribute register 36 (controls memory address 0x0072 0000 - 0x0072 7FFF) |
| 0x0184 A294 | L2MPPA37 | L2 memory protection page attribute register 37 (controls memory address 0x0072 8000 - 0x0072 FFFF) |
| 0x0184 A298 | L2MPPA38 | L2 memory protection page attribute register 38 (controls memory address 0x0073 0000 - 0x0073 7FFF) |
| 0x0184 A29C | L2MPPA39 | L2 memory protection page attribute register 39 (controls memory address 0x0073 8000 - 0x0073 FFFF) |
| 0x0184 A2A0 | L2MPPA40 | L2 memory protection page attribute register 40 (controls memory address 0x0074 0000 - 0x0074 7FFF) |
| 0x0184 A2A4 | L2MPPA41 | L2 memory protection page attribute register 41 (controls memory address 0x0074 8000 - 0x0074 FFFF) |
| 0x0184 A2A8 | L2MPPA42 | L2 memory protection page attribute register 42 (controls memory address 0x0075 0000 - 0x0075 7FFF) |
| 0x0184 A2AC | L2MPPA43 | L2 memory protection page attribute register 43 (controls memory address 0x0075 8000 - 0x0075 FFFF) |
| 0x0184 A2B0 | L2MPPA44 | L2 memory protection page attribute register 44 (controls memory address 0x0076 0000 - 0x0076 7FFF) |
| 0x0184 A2B4 | L2MPPA45 | L2 memory protection page attribute register 45 (controls memory address 0x0076 8000 - 0x0076 FFFF) |
| 0x0184 A2B8 | L2MPPA46 | L2 memory protection page attribute register 46 (controls memory address 0x0077 0000 - 0x0077 7FFF) |
| 0x0184 A2BC | L2MPPA47 | L2 memory protection page attribute register 47 (controls memory address 0x0077 8000 - 0x0077 FFFF) |
| 0x0184 A2C0 | L2MPPA48 | L2 memory protection page attribute register 48 (controls memory address 0x0078 0000 - 0x0078 7FFF) |
| 0x0184 A2C4 | L2MPPA49 | L2 memory protection page attribute register 49 (controls memory address 0x0078 8000 - 0x0078 FFFF) |
| 0x0184 A2C8 | L2MPPA50 | L2 memory protection page attribute register 50 (controls memory address 0x0079 0000 - 0x0079 7FFF) |
| 0x0184 A2CC | L2MPPA51 | L2 memory protection page attribute register 51 (controls memory address 0x0079 8000 - 0x0079 FFFF) |
| 0x0184 A2D0 | L2MPPA52 | L2 memory protection page attribute register 52 (controls memory address 0x007A 0000 - 0x007A 7FFF) |
| 0x0184 A2D4 | L2MPPA53 | L2 memory protection page attribute register 53 (controls memory address 0x007A 8000 - 0x007A FFFF) |
| 0x0184 A2D8 | L2MPPA54 | L2 memory protection page attribute register 54 (controls memory address 0x007B 0000 - 0x007B 7FFF) |
| 0x0184 A2DC | L2MPPA55 | L2 memory protection page attribute register 55 (controls memory address 0x007B 8000 - 0x007B FFFF) |
| 0x0184 A2E0 | L2MPPA56 | L2 memory protection page attribute register 56 (controls memory address 0x007C 0000 - 0x007C 7FFF) |

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**Table 3-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A2E4 | L2MPPA57 | L2 memory protection page attribute register 57 (controls memory address 0x007C 8000 - 0x007C FFFF) |
| 0x0184 A2E8 | L2MPPA58 | L2 memory protection page attribute register 58 (controls memory address 0x007D 0000 - 0x007D 7FFF) |
| 0x0184 A2EC | L2MPPA59 | L2 memory protection page attribute register 59 (controls memory address 0x007D 8000 - 0x007D FFFF) |
| 0x0184 A2F0 | L2MPPA60 | L2 memory protection page attribute register 60 (controls memory address 0x007E 0000 - 0x007E 7FFF) |
| 0x0184 A2F4 | L2MPPA61 | L2 memory protection page attribute register 61 (controls memory address 0x007E 8000 - 0x007E FFFF) |
| 0x0184 A2F8 | L2MPPA62 | L2 memory protection page attribute register 62 (controls memory address 0x007F 0000 - 0x007F 7FFF) |
| 0x0184 A2FC | L2MPPA63 | L2 memory protection page attribute register 63 (controls memory address 0x007F 8000 - 0x007F FFFF) |
| 0x0184 A300 - 0x0184 A3FF | - | Reserved |
| 0x0184 A400 | L1PMPFAR | L1P memory protection fault address register |
| 0x0184 A404 | L1PMPFSR | L1P memory protection fault status register |
| 0x0184 A408 | L1PMPFCR | L1P memory protection fault command register |
| 0x0184 A40C - 0x0184 A4FF | - | Reserved |
| 0x0184 A500 | L1PMPLK0 | L1P memory protection lock key bits [31:0] |
| 0x0184 A504 | L1PMPLK1 | L1P memory protection lock key bits [63:32] |
| 0x0184 A508 | L1PMPLK2 | L1P memory protection lock key bits [95:64] |
| 0x0184 A50C | L1PMPLK3 | L1P memory protection lock key bits [127:96] |
| 0x0184 A510 | L1PMPLKCMD | L1P memory protection lock key command register |
| 0x0184 A514 | L1PMPLKSTAT | L1P memory protection lock key status register |
| 0x0184 A518 - 0x0184 A5FF | - | Reserved |
| 0x0184 A600 - 0x0184 A63F | - | Reserved (1) |
| 0x0184 A640 | L1PMPPA16 | L1P memory protection page attribute register 16 (controls memory address 0x00E0 0000 - 0x00E0 07FF) |
| 0x0184 A644 | L1PMPPA17 | L1P memory protection page attribute register 17 (controls memory address 0x00E0 0800 - 0x00E0 0FFF) |
| 0x0184 A648 | L1PMPPA18 | L1P memory protection page attribute register 18 (controls memory address 0x00E0 1000 - 0x00E0 17FF) |
| 0x0184 A64C | L1PMPPA19 | L1P memory protection page attribute register 19 (controls memory address 0x00E0 1800 - 0x00E0 1FFF) |
| 0x0184 A650 | L1PMPPA20 | L1P memory protection page attribute register 20 (controls memory address 0x00E0 2000 - 0x00E0 27FF) |
| 0x0184 A654 | L1PMPPA21 | L1P memory protection page attribute register 21 (controls memory address 0x00E0 2800 - 0x00E0 2FFF) |
| 0x0184 A658 | L1PMPPA22 | L1P memory protection page attribute register 22 (controls memory address 0x00E0 3000 - 0x00E0 37FF) |
| 0x0184 A65C | L1PMPPA23 | L1P memory protection page attribute register 23 (controls memory address 0x00E0 3800 - 0x00E0 3FFF) |
| 0x0184 A660 | L1PMPPA24 | L1P memory protection page attribute register 24 (controls memory address 0x00E0 4000 - 0x00E0 47FF) |
| 0x0184 A664 | L1PMPPA25 | L1P memory protection page attribute register 25 (controls memory address 0x00E0 4800 - 0x00E0 4FFF) |
| 0x0184 A668 | L1PMPPA26 | L1P memory protection page attribute register 26 (controls memory address 0x00E0 5000 - 0x00E0 57FF) |
| 0x0184 A66C | L1PMPPA27 | L1P memory protection page attribute register 27 (controls memory address 0x00E0 5800 - 0x00E0 5FFF) |

(1) These addresses correspond to the L1P memory protection page attribute registers 0-15 (L1PMPPA0-L1PMPPA15) of the C674x megamaodule. These registers are not supported for this device.


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**Table 3-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A670 | L1PMPPA28 | L1P memory protection page attribute register 28 (controls memory address 0x00E0 6000 - 0x00E0 67FF) |
| 0x0184 A674 | L1PMPPA29 | L1P memory protection page attribute register 29 (controls memory address 0x00E0 6800 - 0x00E0 6FFF) |
| 0x0184 A678 | L1PMPPA30 | L1P memory protection page attribute register 30 (controls memory address 0x00E0 7000 - 0x00E0 77FF) |
| 0x0184 A67C | L1PMPPA31 | L1P memory protection page attribute register 31 (controls memory address 0x00E0 7800 - 0x00E0 7FFF) |
| 0x0184 A67F – 0x0184 ABFF | - | Reserved |
| 0x0184 AC00 | L1DMPFAR | L1D memory protection fault address register |
| 0x0184 AC04 | L1DMPFSR | L1D memory protection fault status register |
| 0x0184 AC08 | L1DMPFCR | L1D memory protection fault command register |
| 0x0184 AC0C - 0x0184 ACFF | - | Reserved |
| 0x0184 AD00 | L1DMPLK0 | L1D memory protection lock key bits [31:0] |
| 0x0184 AD04 | L1DMPLK1 | L1D memory protection lock key bits [63:32] |
| 0x0184 AD08 | L1DMPLK2 | L1D memory protection lock key bits [95:64] |
| 0x0184 AD0C | L1DMPLK3 | L1D memory protection lock key bits [127:96] |
| 0x0184 AD10 | L1DMPLKCMD | L1D memory protection lock key command register |
| 0x0184 AD14 | L1DMPLKSTAT | L1D memory protection lock key status register |
| 0x0184 AD18 - 0x0184 ADFF | - | Reserved |
| 0x0184 AE00 - 0x0184 AE3F | - | Reserved (2) |
| 0x0184 AE40 | L1DMPPA16 | L1D memory protection page attribute register 16 (controls memory address 0x00F0 0000 - 0x00F0 07FF) |
| 0x0184 AE44 | L1DMPPA17 | L1D memory protection page attribute register 17 (controls memory address 0x00F0 0800 - 0x00F0 0FFF) |
| 0x0184 AE48 | L1DMPPA18 | L1D memory protection page attribute register 18 (controls memory address 0x00F0 1000 - 0x00F0 17FF) |
| 0x0184 AE4C | L1DMPPA19 | L1D memory protection page attribute register 19 (controls memory address 0x00F0 1800 - 0x00F0 1FFF) |
| 0x0184 AE50 | L1DMPPA20 | L1D memory protection page attribute register 20 (controls memory address 0x00F0 2000 - 0x00F0 27FF) |
| 0x0184 AE54 | L1DMPPA21 | L1D memory protection page attribute register 21 (controls memory address 0x00F0 2800 - 0x00F0 2FFF) |
| 0x0184 AE58 | L1DMPPA22 | L1D memory protection page attribute register 22 (controls memory address 0x00F0 3000 - 0x00F0 37FF) |
| 0x0184 AE5C | L1DMPPA23 | L1D memory protection page attribute register 23 (controls memory address 0x00F0 3800 - 0x00F0 3FFF) |
| 0x0184 AE60 | L1DMPPA24 | L1D memory protection page attribute register 24 (controls memory address 0x00F0 4000 - 0x00F0 47FF) |
| 0x0184 AE64 | L1DMPPA25 | L1D memory protection page attribute register 25 (controls memory address 0x00F0 4800 - 0x00F0 4FFF) |
| 0x0184 AE68 | L1DMPPA26 | L1D memory protection page attribute register 26 (controls memory address 0x00F0 5000 - 0x00F0 57FF) |
| 0x0184 AE6C | L1DMPPA27 | L1D memory protection page attribute register 27 (controls memory address 0x00F0 5800 - 0x00F0 5FFF) |
| 0x0184 AE70 | L1DMPPA28 | L1D memory protection page attribute register 28 (controls memory address 0x00F0 6000 - 0x00F0 67FF) |
| 0x0184 AE74 | L1DMPPA29 | L1D memory protection page attribute register 29 (controls memory address 0x00F0 6800 - 0x00F0 6FFF) |
| 0x0184 AE78 | L1DMPPA30 | L1D memory protection page attribute register 30 (controls memory address 0x00F0 7000 - 0x00F0 77FF) |

(2) These addresses correspond to the L1D memory protection page attribute registers 0-15 (L1DMPPA0-L1DMPPA15) of the C674x megamaodule. These registers are not supported for this device.

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**Table 3-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 AE7C | L1DMPPA31 | L1D memory protection page attribute register 31 (controls memory address 0x00F0 7800 - 0x00F0 7FFF) |
| 0x0184 AE80 – 0x0185 FFFF | - | Reserved |


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## 3.4 Memory Map Summary

**Note:** Read/Write accesses to illegal or reserved addresses in the memory map may cause undefined behavior.

**Table 3-4. C6742 Top Level Memory Map**

| Start Address | End Address | Size | DSP Mem Map | EDMA Mem Map | Master Peripheral Mem Map |
|---|---|---|---|---|---|
| 0x0000 0000 | 0x006F FFFF | | | | |
| 0x0070 0000 | 0x007F FFFF | 1024K | DSP L2 ROM(1) | | |
| 0x0080 0000 | 0x0080 FFFF | 64K | DSP L2 RAM | | |
| 0x0081 0000 | 0x00DF FFFF | | | | |
| 0x00E0 0000 | 0x00E0 7FFF | 32K | DSP L1P RAM | | |
| 0x00E0 8000 | 0x00EF FFFF | | | | |
| 0x00F0 0000 | 0x00F0 7FFF | 32K | DSP L1D RAM | | |
| 0x00F0 8000 | 0x017F FFFF | | | | |
| 0x0180 0000 | 0x0180 FFFF | 64K | DSP Interrupt Controller | | |
| 0x0181 0000 | 0x0181 0FFF | 4K | DSP Powerdown Controller | | |
| 0x0181 1000 | 0x0181 1FFF | 4K | DSP Security ID | | |
| 0x0181 2000 | 0x0181 2FFF | 4K | DSP Revision ID | | |
| 0x0181 3000 | 0x0181 FFFF | 52K | | | |
| 0x0182 0000 | 0x0182 FFFF | 64K | DSP EMC | | |
| 0x0183 0000 | 0x0183 FFFF | 64K | DSP Internal Reserved | | |
| 0x0184 0000 | 0x0184 FFFF | 64K | DSP Memory System | | |
| 0x0185 0000 | 0x01BF FFFF | | | | |
| 0x01C0 0000 | 0x01C0 7FFF | 32K | EDMA3 CC | | |
| 0x01C0 8000 | 0x01C0 83FF | 1K | EDMA3 TC0 | | |
| 0x01C0 8400 | 0x01C0 87FF | 1K | EDMA3 TC1 | | |
| 0x01C0 8800 | 0x01C0 FFFF | | | | |
| 0x01C1 0000 | 0x01C1 0FFF | 4K | PSC 0 | | |
| 0x01C1 1000 | 0x01C1 1FFF | 4K | PLL Controller 0 | | |
| 0x01C1 2000 | 0x01C1 3FFF | | | | |
| 0x01C1 4000 | 0x01C1 4FFF | 4K | SYSCFG0 | | |
| 0x01C1 5000 | 0x01C1 FFFF | | | | |
| 0x01C2 0000 | 0x01C2 0FFF | 4K | Timer0 | | |
| 0x01C2 1000 | 0x01C2 1FFF | 4K | Timer1 | | |
| 0x01C2 2000 | 0x01C2 2FFF | 4K | I2C 0 | | |
| 0x01C2 3000 | 0x01C2 3FFF | 4K | RTC | | |
| 0x01C2 4000 | 0x01C4 FFFF | | | | |
| 0x01C4 2000 | 0x01C4 2FFF | 4K | UART 0 | | |
| 0x01C4 3000 | 0x01CF FFFF | | | | |
| 0x01D0 0000 | 0x01D0 0FFF | 4K | McASP 0 Control | | |
| 0x01D0 1000 | 0x01D0 1FFF | 4K | McASP 0 AFIFO Ctrl | | |
| 0x01D0 2000 | 0x01D0 2FFF | 4K | McASP 0 Data | | |
| 0x01D0 3000 | 0x01D1 0FFF | | | | |
| 0x01D1 1000 | 0x01D1 17FF | 2K | McBSP1 | | |
| 0x01D1 1800 | 0x01D1 1FFF | 2K | McBSP1 FIFO Ctrl | | |
| 0x01D1 2000 | 0x01E0 FFFF | | | | |
| 0x01E1 0000 | 0x01E1 0FFF | 4K | UHPI | | |
| 0x01E1 1000 | 0x01E1 3FFF | | | | |

(1) The DSP L2 ROM is used for boot purposes and cannot be programmed with application code

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**Table 3-4. C6742 Top Level Memory Map (continued)**

| Start Address | End Address | Size | DSP Mem Map | EDMA Mem Map | Master Peripheral Mem Map |
|---|---|---|---|---|---|
| 0x01E1 4000 | 0x01E1 4FFF | 4K | Memory Protection Unit 1 (MPU 1) | | |
| 0x01E1 5000 | 0x01E1 5FFF | 4K | Memory Protection Unit 2 (MPU 2) | | |
| 0x01E1 6000 | 0x01E1 9FFF | | | | |
| 0x01E1 A000 | 0x01E1 AFFF | 4K | PLL Controller 1 | | |
| 0x01E1 B000 | 0x01E2 5FFF | | | | |
| 0x01E2 6000 | 0x01E2 6FFF | 4K | GPIO | | |
| 0x01E2 7000 | 0x01E2 7FFF | 4K | PSC 1 | | |
| 0x01E2 8000 | 0x01E2 BFFF | | | | |
| 0x01E2 C000 | 0x01E2 CFFF | 4K | SYSCFG1 | | |
| 0x01E2 D000 | 0x01E2 FFFF | | | | |
| 0x01E3 0000 | 0x01E3 7FFF | 32K | EDMA3 CC1 | | |
| 0x01E3 8000 | 0x01E3 83FF | 1K | EDMA3 TC2 | | |
| 0x01E3 8400 | 0x01EF FFFF | | | | |
| 0x01F0 0000 | 0x01F0 0FFF | 4K | eHRPWM 0 | | |
| 0x01F0 1000 | 0x01F0 1FFF | 4K | HRPWM 0 | | |
| 0x01F0 2000 | 0x01F0 2FFF | 4K | eHRPWM 1 | | |
| 0x01F0 3000 | 0x01F0 3FFF | 4K | HRPWM 1 | | |
| 0x01F0 4000 | 0x01F0 5FFF | | | | |
| 0x01F0 6000 | 0x01F0 6FFF | 4K | ECAP 0 | | |
| 0x01F0 7000 | 0x01F0 7FFF | 4K | ECAP 1 | | |
| 0x01F0 8000 | 0x01F0 8FFF | 4K | ECAP 2 | | |
| 0x01F0 9000 | 0x01F0 DFFF | | | | |
| 0x01F0 E000 | 0x01F0 EFFF | 4K | SPI1 | | |
| 0x01F0 F000 | 0x01F1 FFFF | | | | |
| 0x01F1 1000 | 0x01F1 1FFF | 4K | McBSP1 FIFO Data | | |
| 0x01F1 2000 | 0x116F FFFF | | | | |
| 0x1170 0000 | 0x117F FFFF | 1024K | DSP L2 ROM(1) | | |
| 0x1180 0000 | 0x1180 FFFF | 64K | DSP L2 RAM | | |
| 0x1181 0000 | 0x11DF FFFF | | | | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | DSP L1P RAM | | |
| 0x11E0 8000 | 0x11EF FFFF | | | | |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | DSP L1D RAM | | |
| 0x11F0 8000 | 0x3FFF FFFF | | | | |
| 0x4000 0000 | 0x5FFF FFFF | 512M | EMIFA SDRAM data (CS0) | | |
| 0x6000 0000 | 0x61FF FFFF | 32M | EMIFA async data (CS2) | | |
| 0x6200 0000 | 0x63FF FFFF | 32M | EMIFA async data (CS3) | | |
| 0x6400 0000 | 0x65FF FFFF | 32M | EMIFA async data (CS4) | | |
| 0x6600 0000 | 0x67FF FFFF | 32M | EMIFA async data (CS5) | | |
| 0x6800 0000 | 0x6800 7FFF | 32K | EMIFA Control Regs | | |
| 0x6800 8000 | 0xAFFF FFFF | | | | |
| 0xB000 0000 | 0xB000 7FFF | 32K | DDR2/mDDR Control Regs | | |
| 0xB000 8000 | 0xBFFF FFFF | | | | |
| 0xC000 0000 | 0xCFFF FFFF | 256M | DDR2/mDDR Data | | |
| 0xD000 0000 | 0xFFFF FFFF | | | | |


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## 3.5 Pin Assignments

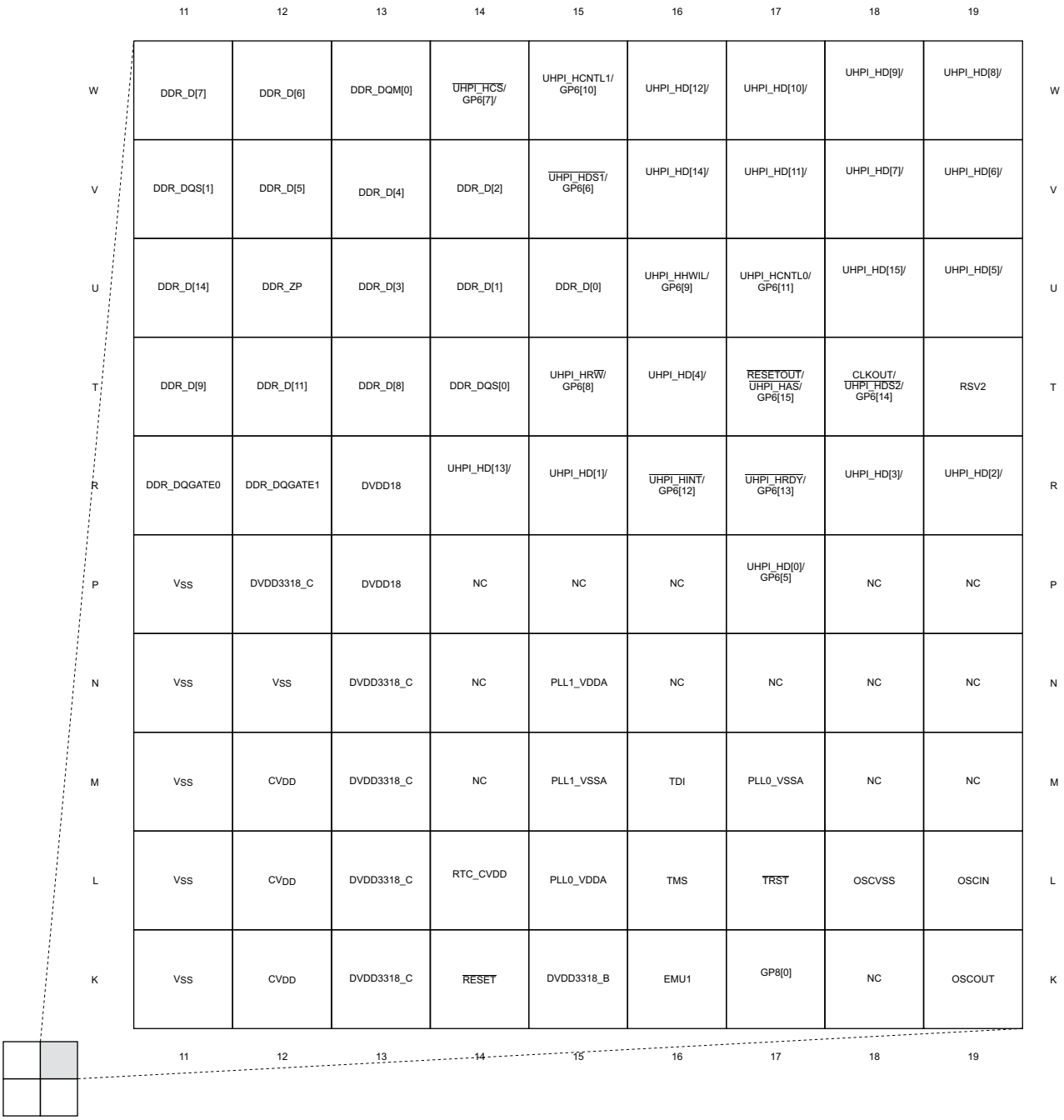
Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings.

### *3.5.1 Pin Map (Bottom View)*

The following graphics show the bottom view of the ZCE and ZWT packages pin assignments in four quadrants (A, B, C, and D). The pin assignments for both packages are identical.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| W | GP7[8] | GP7[9] | GP7[10] | DDR_A[10] | DDR_A[6] | DDR_A[2] | $\overline{\text{DDR_CLKN}}$ | DDR_CLKP | $\overline{\text{DDR_RAS}}$ | DDR_D[15] | W |
| V | GP7[11] | GP7[12] | GP7[13] | DDR_A[12] | DDR_A[5] | DDR_A[3] | DDR_CKE | DDR_BA[0] | $\overline{\text{DDR_CS}}$ | DDR_D[13] | V |
| U | GP7[14] | GP7[15] | GP7[0]/ BOOT[0] | DDR_A[8] | DDR_A[4] | DDR_A[7] | DDR_A[0] | DDR_BA[2] | $\overline{\text{DDR_CAS}}$ | DDR_D[12] | U |
| T | GP7[1]/ BOOT[1] | GP7[2]/ BOOT[2] | GP7[3]/ BOOT[3] | DDR_A[11] | DDR_A[13] | DDR_A[9] | DDR_A[1] | $\overline{\text{DDR_WE}}$ | DDR_BA[1] | DDR_D[10] | T |
| R | GP7[4]/ BOOT[4] | GP7[5]/ BOOT[5] | GP7[6]/ BOOT[6] | DVDD3318_C | GP6[0] | DDR_VREF | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | DDR_DQM[1] | R |
| P | RSV3 | RSV3 | NC | GP7[7]/ BOOT[7] | DVDD3318_C | DVDD3318_C | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | P |
| N | NC | NC | NC | RSV3 | $V_{SS}$ | DDR_DVDD18 | $RV_{DD}$ | $CV_{DD}$ | DDR_DVDD18 | DDR_DVDD18 | N |
| M | $V_{SS}$ | RSV3 | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | M |
| L | NC | NC | $V_{SS}$ | $DV_{DD3318_C}$ | $V_{SS}$ | $DV_{DD18}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | L |
| K | $V_{SS}$ | $V_{SS}$ | GP6[3] | GP6[1] | $DV_{DD18}$ | $CV_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

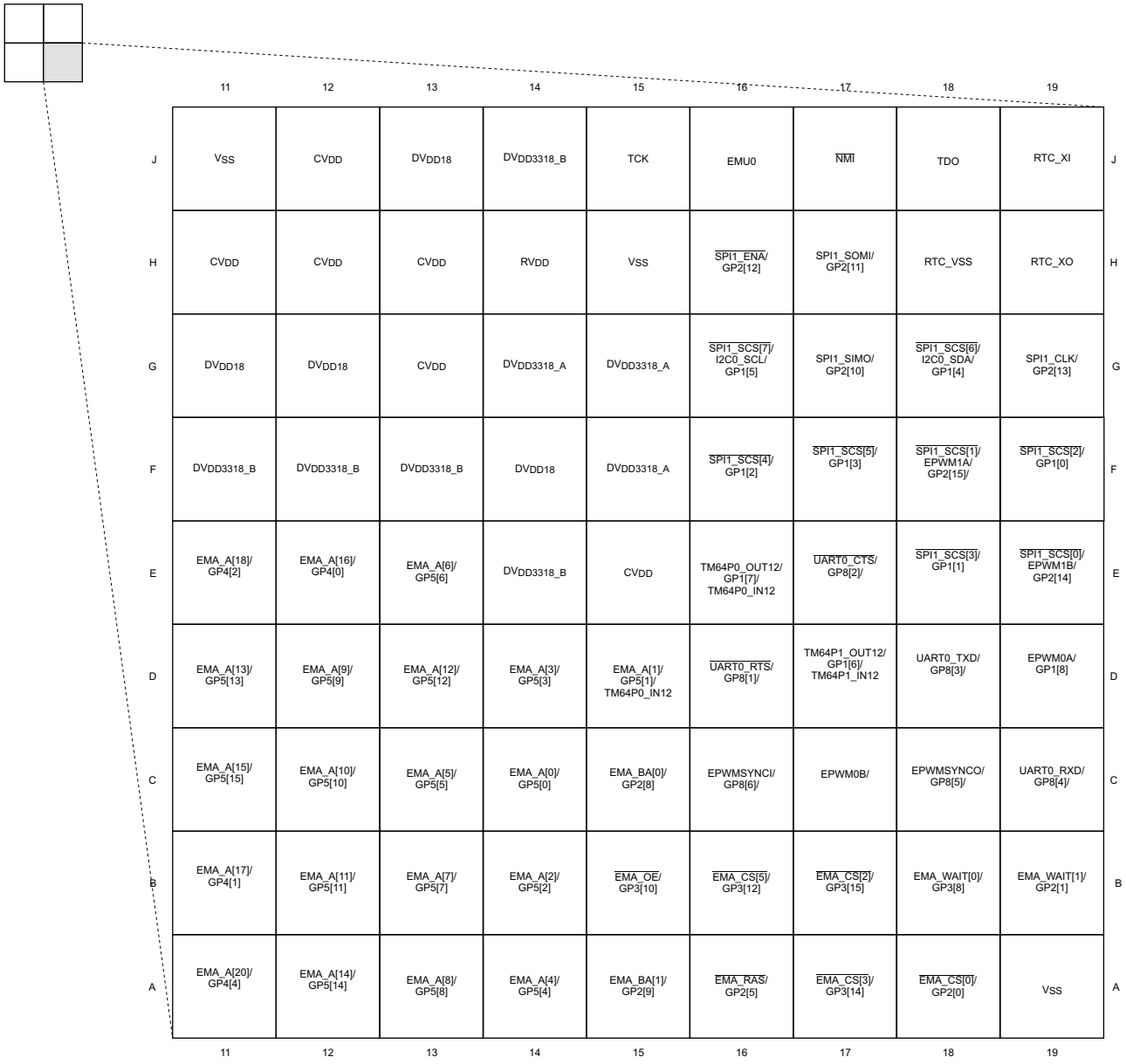
**Figure 3-3. Pin Map (Quad A)**



| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|---|---|---|---|---|---|---|---|---|---|---|
| W | DDR_D[7] | DDR_D[6] | DDR_DQM[0] | UHPI_HCS/ GP6[7]/ | UHPI_HCNTL1/ GP6[10] | UHPI_HD[12]/ | UHPI_HD[10]/ | UHPI_HD[9]/ | UHPI_HD[8]/ | W |
| V | DDR_DQS[1] | DDR_D[5] | DDR_D[4] | DDR_D[2] | UHPI_HDS1/ GP6[6] | UHPI_HD[14]/ | UHPI_HD[11]/ | UHPI_HD[7]/ | UHPI_HD[6]/ | V |
| U | DDR_D[14] | DDR_ZP | DDR_D[3] | DDR_D[1] | DDR_D[0] | UHPI_HHWIL/ GP6[9] | UHPI_HCNTL0/ GP6[11] | UHPI_HD[15]/ | UHPI_HD[5]/ | U |
| T | DDR_D[9] | DDR_D[11] | DDR_D[8] | DDR_DQS[0] | UHPI_HRW/ GP6[8] | UHPI_HD[4]/ | RESETOUT/ UHPI_HAS/ GP6[15] | CLKOUT/ UHPI_HDS2/ GP6[14] | RSV2 | T |
| R | DDR_DQGATE0 | DDR_DQGATE1 | DVDD18 | UHPI_HD[13]/ | UHPI_HD[1]/ | UHPI_HINT/ GP6[12] | UHPI_HRDY/ GP6[13] | UHPI_HD[3]/ | UHPI_HD[2]/ | R |
| P | $V_{SS}$ | DVDD3318_C | DVDD18 | NC | NC | NC | UHPI_HD[0]/ GP6[5] | NC | NC | P |
| N | $V_{SS}$ | $V_{SS}$ | DVDD3318_C | NC | PLL1_VDDA | NC | NC | NC | NC | N |
| M | $V_{SS}$ | $CV_{DD}$ | DVDD3318_C | NC | PLL1_VSSA | TDI | PLL0_VSSA | NC | NC | M |
| L | $V_{SS}$ | $CV_{DD}$ | DVDD3318_C | RTC_CVDD | PLL0_VDDA | TMS | TRST | OSCVSS | OSCIN | L |
| K | $V_{SS}$ | $CV_{DD}$ | DVDD3318_C | RESET | DVDD3318_B | EMU1 | GP8[0] | NC | OSCOUT | K |
| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

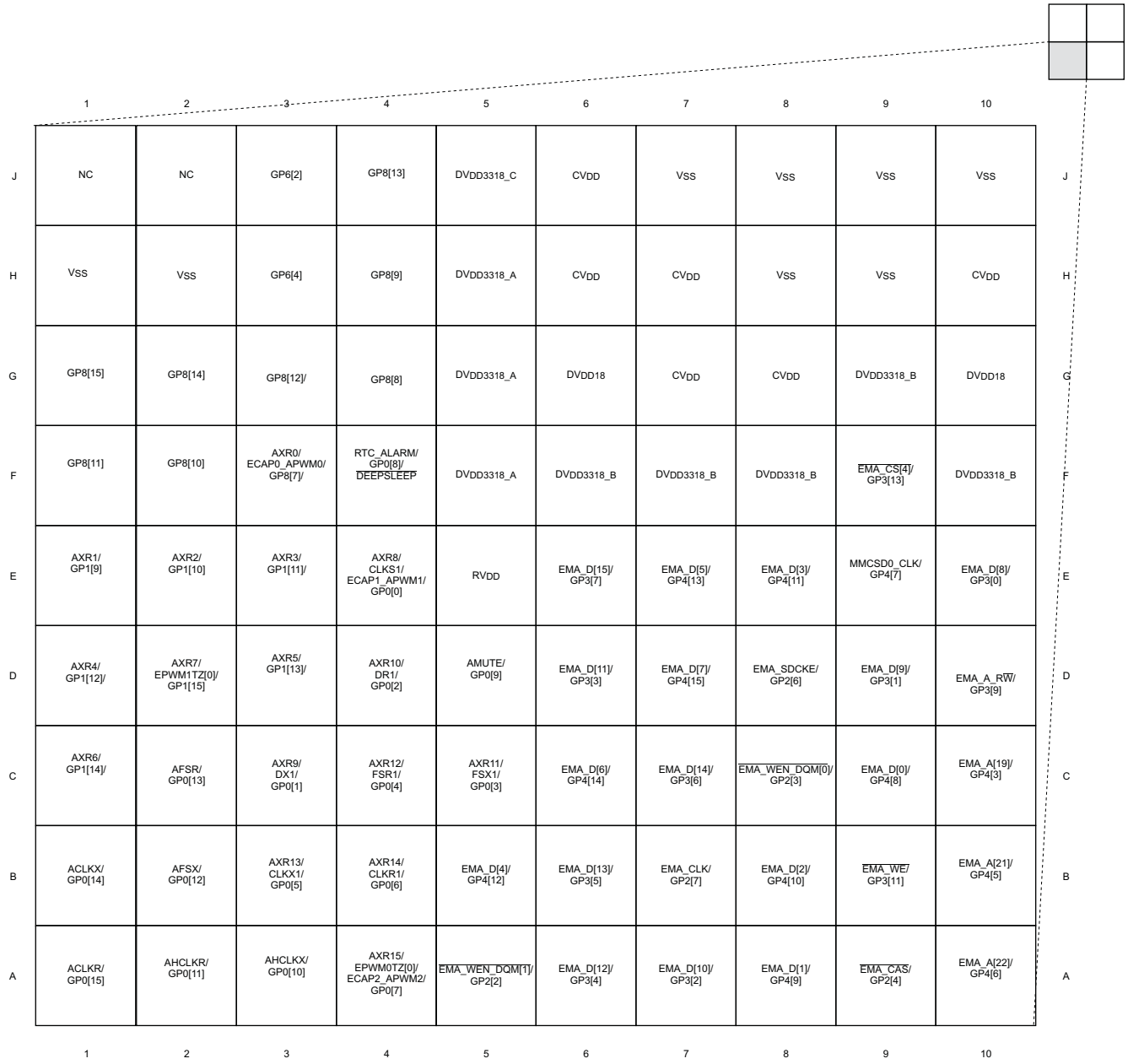
**Figure 3-4. Pin Map (Quad B)**


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| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|---|---|---|---|---|---|---|---|---|---|---|
| J | $V_{SS}$ | $CV_{DD}$ | $DV_{DD18}$ | $DV_{DD3318_B}$ | TCK | EMU0 | $\overline{NMI}$ | TDO | RTC_XI | J |
| H | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $RV_{DD}$ | $V_{SS}$ | $\overline{SPI1_ENA}$/ GP2[12] | SPI1_SOMI/ GP2[11] | RTC_VSS | RTC_XO | H |
| G | $DV_{DD18}$ | $DV_{DD18}$ | $CV_{DD}$ | $DV_{DD3318_A}$ | $DV_{DD3318_A}$ | $\overline{SPI1_SCS[7]}$/ I2C0_SCL/ GP1[5] | SPI1_SIMO/ GP2[10] | $\overline{SPI1_SCS[6]}$/ I2C0_SDA/ GP1[4] | SPI1_CLK/ GP2[13] | G |
| F | $DV_{DD3318_B}$ | $DV_{DD3318_B}$ | $DV_{DD3318_B}$ | $DV_{DD18}$ | $DV_{DD3318_A}$ | $\overline{SPI1_SCS[4]}$/ GP1[2] | $\overline{SPI1_SCS[5]}$/ GP1[3] | $\overline{SPI1_SCS[1]}$/ EPWM1A/ GP2[15]/ | $\overline{SPI1_SCS[2]}$/ GP1[0] | F |
| E | EMA_A[18]/ GP4[2] | EMA_A[16]/ GP4[0] | EMA_A[6]/ GP5[6] | $DV_{DD3318_B}$ | $CV_{DD}$ | TM64P0_OUT12/ GP1[7]/ TM64P0_IN12 | $\overline{UART0_CTS}$/ GP8[2]/ | $\overline{SPI1_SCS[3]}$/ GP1[1] | $\overline{SPI1_SCS[0]}$/ EPWM1B/ GP2[14] | E |
| D | EMA_A[13]/ GP5[13] | EMA_A[9]/ GP5[9] | EMA_A[12]/ GP5[12] | EMA_A[3]/ GP5[3] | EMA_A[1]/ GP5[1]/ TM64P0_IN12 | $\overline{UART0_RTS}$/ GP8[1]/ | TM64P1_OUT12/ GP1[6]/ TM64P1_IN12 | UART0_TXD/ GP8[3]/ | EPWM0A/ GP1[8] | D |
| C | EMA_A[15]/ GP5[15] | EMA_A[10]/ GP5[10] | EMA_A[5]/ GP5[5] | EMA_A[0]/ GP5[0] | EMA_BA[0]/ GP2[8] | EPWMSYNCI/ GP8[6]/ | EPWM0B/ | EPWMSYNCO/ GP8[5]/ | UART0_RXD/ GP8[4]/ | C |
| B | EMA_A[17]/ GP4[1] | EMA_A[11]/ GP5[11] | EMA_A[7]/ GP5[7] | EMA_A[2]/ GP5[2] | $\overline{EMA_OE}$/ GP3[10] | $\overline{EMA_CS[5]}$/ GP3[12] | $\overline{EMA_CS[2]}$/ GP3[15] | EMA_WAIT[0]/ GP3[8] | EMA_WAIT[1]/ GP2[1] | B |
| A | EMA_A[20]/ GP4[4] | EMA_A[14]/ GP5[14] | EMA_A[8]/ GP5[8] | EMA_A[4]/ GP5[4] | EMA_BA[1]/ GP2[9] | $\overline{EMA_RAS}$/ GP2[5] | $\overline{EMA_CS[3]}$/ GP3[14] | $\overline{EMA_CS[0]}$/ GP2[0] | $V_{SS}$ | A |
| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

**Figure 3-5. Pin Map (Quad C)**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| J | NC | NC | GP6[2] | GP8[13] | DVDD3318_C | CVDD | VSS | VSS | VSS | VSS |
| H | VSS | VSS | GP6[4] | GP8[9] | DVDD3318_A | CVDD | CVDD | VSS | VSS | CVDD |
| G | GP8[15] | GP8[14] | GP8[12]/ | GP8[8] | DVDD3318_A | DVDD18 | CVDD | CVDD | DVDD3318_B | DVDD18 |
| F | GP8[11] | GP8[10] | AXR0/ ECAP0_APWM0/ GP8[7]/ | RTC_ALARM/ GP0[8]/ DEEPSLEEP | DVDD3318_A | DVDD3318_B | DVDD3318_B | DVDD3318_B | EMA_CS[4]/ GP3[13] | DVDD3318_B |
| E | AXR1/ GP1[9] | AXR2/ GP1[10] | AXR3/ GP1[11]/ | AXR8/ CLKS1/ ECAP1_APWM1/ GP0[0] | RVDD | EMA_D[15]/ GP3[7] | EMA_D[5]/ GP4[13] | EMA_D[3]/ GP4[11] | MMCSD0_CLK/ GP4[7] | EMA_D[8]/ GP3[0] |
| D | AXR4/ GP1[12]/ | AXR7/ EPWM1TZ[0]/ GP1[15] | AXR5/ GP1[13]/ | AXR10/ DR1/ GP0[2] | AMUTE/ GP0[9] | EMA_D[11]/ GP3[3] | EMA_D[7]/ GP4[15] | EMA_SDCKE/ GP2[6] | EMA_D[9]/ GP3[1] | EMA_A_RW/ GP3[9] |
| C | AXR6/ GP1[14]/ | AFSR/ GP0[13] | AXR9/ DX1/ GP0[1] | AXR12/ FSR1/ GP0[4] | AXR11/ FSX1/ GP0[3] | EMA_D[6]/ GP4[14] | EMA_D[14]/ GP3[6] | EMA_WEN_DQM[0]/ GP2[3] | EMA_D[0]/ GP4[8] | EMA_A[19]/ GP4[3] |
| B | ACLKX/ GP0[14] | AFSX/ GP0[12] | AXR13/ CLKX1/ GP0[5] | AXR14/ CLKR1/ GP0[6] | EMA_D[4]/ GP4[12] | EMA_D[13]/ GP3[5] | EMA_CLK/ GP2[7] | EMA_D[2]/ GP4[10] | EMA_WE/ GP3[11] | EMA_A[21]/ GP4[5] |
| A | ACLKR/ GP0[15] | AHCLKR/ GP0[11] | AHCLKX/ GP0[10] | AXR15/ EPWM0TZ[0]/ ECAP2_APWM2/ GP0[7] | EMA_WEN_DQM[1]/ GP2[2] | EMA_D[12]/ GP3[4] | EMA_D[10]/ GP3[2] | EMA_D[1]/ GP4[9] | EMA_CAS/ GP2[4] | EMA_A[22]/ GP4[6] |

**Figure 3-6. Pin Map (Quad D)**

## 3.6 Pin Multiplexing Control

Device level pin multiplexing is controlled by registers PINMUX0 - PINMUX19 in the SYSCFG module.

For the device family, pin multiplexing can be controlled on a pin-by-pin basis. Each pin that is multiplexed with several different functions has a corresponding 4-bit field in one of the PINMUX registers.

Pin multiplexing selects which of several peripheral pin functions controls the pin's IO buffer **output** data and **output enable** values only. The default pin multiplexing control for almost every pin is to select 'none' of the peripheral functions in which case the pin's IO buffer is held tri-stated.

Note that the **input** from each pin is always routed to **all** of the peripherals that share the pin; the PINMUX registers have no effect on input from a pin.


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## 3.7 Terminal Functions

Table 3-5 to Table 3-23 identify the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin type (I, O, IO, OZ, or PWR), whether the pin/ball has any internal pullup/pulldown resistors, whether the pin/ball is configurable as an IO in GPIO mode, and a functional pin description.

### 3.7.1 Device Reset, NMI and JTAG

**Table 3-5. Reset, NMI and JTAG Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **RESET** | | | | | |
| **$\overline{\text{RESET}}$** | K14 | I | — | B | Device reset input |
| **$\overline{\text{NMI}}$** | J17 | I | IPU | B | Non-Maskable Interrupt |
| **$\overline{\text{RESETOUT}}$** / $\overline{\text{UHPI_HAS}}$ / GP6[15] | T17 | O(4) | CP[21] | C | Reset output |
| **JTAG** | | | | | |
| **TMS** | L16 | I | IPU | B | JTAG test mode select |
| **TDI** | M16 | I | IPU | B | JTAG test data input |
| **TDO** | J18 | O | IPU | B | JTAG test data output |
| **TCK** | J15 | I | IPU | B | JTAG test clock |
| **$\overline{\text{TRST}}$** | L17 | I | IPD | B | JTAG test reset |
| **EMU0** | J16 | I/O | IPU | B | Emulation pin |
| **EMU1** | K16 | I/O | IPU | B | Emulation pin |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor. CP[n] = configurable pull-up/pull-down (where n is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.
(4) Open drain mode for $\overline{\text{RESETOUT}}$ function.

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### 3.7.2 High-Frequency Oscillator and PLL

**Table 3-6. High-Frequency Oscillator and PLL Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **CLKOUT** / $\overline{\text{UHPI_HDS2}}$ / GP6[14] | T18 | O | CP[22] | C | PLL Observation Clock(4) |
| **1.2-V OSCILLATOR** | | | | | |
| **OSCIN** | L19 | I | — | — | Oscillator input |
| **OSCOUT** | K19 | O | — | — | Oscillator output |
| **OSCVSS** | L18 | GND | — | — | Oscillator ground |
| **1.2-V PLL0** | | | | | |
| **PLL0_VDDA** | L15 | PWR | — | — | PLL analog $V_{DD}$ (1.2-V filtered supply) |
| **PLL0_VSSA** | M17 | GND | — | — | PLL analog $V_{SS}$ (for filter) |
| **1.2-V PLL1** | | | | | |
| **PLL1_VDDA** | N15 | PWR | — | — | PLL analog $V_{DD}$ (1.2-V filtered supply) |
| **PLL1_VSSA** | M15 | GND | — | — | PLL analog $V_{SS}$ (for filter) |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

(4) **Note**: The CLKOUT clock output is provided as PLL observation clock, and is provided for debug purposes only. It may be routed to a test point, but should never be connected to a load.


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### 3.7.3 Real-Time Clock and 32-kHz Oscillator

**Table 3-7. Real-Time Clock (RTC) and 1.2-V, 32-kHz Oscillator Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **RTC_XI** | J19 | I | — | — | RTC 32-kHz oscillator input |
| **RTC_XO** | H19 | O | — | — | RTC 32-kHz oscillator output |
| **RTC_ALARM** / GP0[8] / $\overline{\text{DEEPSLEEP}}$ | F4 | O | CP[0] | A | RTC Alarm |
| **RTC_CVDD** | L14 | PWR | — | — | RTC module core power (isolated from chip $CV_{DD}$) |
| **RTC_$V_{ss}$** | H18 | GND | — | — | Oscillator ground |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

### 3.7.4 DEEPSLEEP Power Control

**Table 3-8. DEEPSLEEP Power Control Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| RTC_ALARM / GP0[8] / **$\overline{\text{DEEPSLEEP}}$** | F4 | I | CP[0] | A | DEEPSLEEP power control output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 3.7.5 External Memory Interface A (EMIFA)

**Table 3-9. External Memory Interface A (EMIFA) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **EMA_D[15]** / GP3[7] | E6 | I/O | CP[17] | B | EMIFA data bus |
| **EMA_D[14]** / GP3[6] | C7 | I/O | CP[17] | B | |
| **EMA_D[13]** / GP3[5] | B6 | I/O | CP[17] | B | |
| **EMA_D[12]** / GP3[4] | A6 | I/O | CP[17] | B | |
| **EMA_D[11]** / GP3[3] | D6 | I/O | CP[17] | B | |
| **EMA_D[10]** / GP3[2] | A7 | I/O | CP[17] | B | |
| **EMA_D[9]** / GP3[1] | D9 | I/O | CP[17] | B | |
| **EMA_D[8]** / GP3[0] | E10 | I/O | CP[17] | B | |
| **EMA_D[7]** / GP4[15] | D7 | I/O | CP[17] | B | |
| **EMA_D[6]** / GP4[14] | C6 | I/O | CP[17] | B | |
| **EMA_D[5]** / GP4[13] | E7 | I/O | CP[17] | B | |
| **EMA_D[4]** / GP4[12] | B5 | I/O | CP[17] | B | |
| **EMA_D[3]** / GP4[11] | E8 | I/O | CP[17] | B | |
| **EMA_D[2]** / GP4[10] | B8 | I/O | CP[17] | B | |
| **EMA_D[1]** / GP4[9] | A8 | I/O | CP[17] | B | |
| **EMA_D[0]** / GP4[8] | C9 | I/O | CP[17] | B | |
| **EMA_A[22]** / GP4[6] | A10 | O | CP[18] | B | EMIFA address bus |
| **EMA_A[21]** / GP4[5] | B10 | O | CP[18] | B | |
| **EMA_A[20]** / GP4[4] | A11 | O | CP[18] | B | |
| **EMA_A[19]** / GP4[3] | C10 | O | CP[18] | B | |
| **EMA_A[18]** / GP4[2] | E11 | O | CP[18] | B | |
| **EMA_A[17]** / GP4[1] | B11 | O | CP[18] | B | |
| **EMA_A[16]** / GP4[0] | E12 | O | CP[18] | B | |
| **EMA_A[15]** / GP5[15] | C11 | O | CP[19] | B | |
| **EMA_A[14]** / GP5[14] | A12 | O | CP[19] | B | |
| **EMA_A[13]** / GP5[13] | D11 | O | CP[19] | B | |
| **EMA_A[12]** / GP5[12] | D13 | O | CP[19] | B | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 3-9. External Memory Interface A (EMIFA) Terminal Functions (continued)**

| SIGNAL | | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **EMA_A[11]** / GP5[11] | B12 | O | CP[19] | B | EMIFA address bus |
| **EMA_A[10]** / GP5[10] | C12 | O | CP[19] | B | |
| **EMA_A[9]** / GP5[9] | D12 | O | CP[19] | B | |
| **EMA_A[8]** / GP5[8] | A13 | O | CP[19] | B | |
| **EMA_A[7]** / GP5[7] | B13 | O | CP[20] | B | |
| **EMA_A[6]** / GP5[6] | E13 | O | CP[20] | B | |
| **EMA_A[5]** / GP5[5] | C13 | O | CP[20] | B | |
| **EMA_A[4]** / GP5[4] | A14 | O | CP[20] | B | |
| **EMA_A[3]** / GP5[3] | D14 | O | CP[20] | B | |
| **EMA_A[2]** / GP5[2] | B14 | O | CP[20] | B | |
| **EMA_A[1]** / GP5[1] | D15 | O | CP[20] | B | |
| **EMA_A[0]** / GP5[0] | C14 | O | CP[20] | B | |
| **EMA_BA[0]** / GP2[8] | C15 | O | CP[16] | B | EMIFA bank address |
| **EMA_BA[1]** / GP2[9] | A15 | O | CP[16] | B | |
| **EMA_CLK** / GP2[7] | B7 | O | CP[16] | B | EMIFA clock |
| **EMA_SDCKE** / GP2[6] | D8 | O | CP[16] | B | EMIFA SDRAM clock enable |
| **$\overline{\text{EMA_RAS}}$** / GP2[5] | A16 | O | CP[16] | B | EMIFA SDRAM row address strobe |
| **$\overline{\text{EMA_CAS}}$** / GP2[4] | A9 | O | CP[16] | B | EMIFA SDRAM column address strobe |
| **$\overline{\text{EMA_CS[0]}}$** / GP2[0] | A18 | O | CP[16] | B | EMIFA SDRAM Chip Select |
| **$\overline{\text{EMA_CS[2]}}$** / GP3[15] | B17 | O | CP[16] | B | EMIFA Async chip select |
| **$\overline{\text{EMA_CS[3]}}$** / GP3[14] | A17 | O | CP[16] | B | |
| **$\overline{\text{EMA_CS[4]}}$** / GP3[13] | F9 | O | CP[16] | B | |
| **$\overline{\text{EMA_CS[5]}}$** / GP3[12] | B16 | O | CP[16] | B | |
| **EMA_A_$\overline{\text{RW}}$** / GP3[9] | D10 | O | CP[16] | B | EMIFA Async Read/Write control |
| **$\overline{\text{EMA_WE}}$** / GP3[11] | B9 | O | CP[16] | B | EMIFA SDRAM write enable |
| **$\overline{\text{EMA_WEN_DQM[1]}}$** / GP2[2] | A5 | O | CP[16] | B | EMIFA write enable/data mask for EMA_D[15:8] |
| **$\overline{\text{EMA_WEN_DQM[0]}}$** / GP2[3] | C8 | O | CP[16] | B | EMIFA write enable/data mask for EMA_D[7:0] |
| **$\overline{\text{EMA_OE}}$** / GP3[10] | B15 | O | CP[16] | B | EMIFA output enable |
| **EMA_WAIT[0]** / GP3[8] | B18 | I | CP[16] | B | EMIFA wait input/interrupt |
| **EMA_WAIT[1]** / GP2[1] | B19 | I | CP[16] | B | |

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### 3.7.6 DDR2/mDDR Controller

**Table 3-10. DDR2/mDDR Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **DDR_D[15]** | W10 | I/O | IPD | DDR2 SDRAM data bus |
| **DDR_D[14]** | U11 | I/O | IPD | |
| **DDR_D[13]** | V10 | I/O | IPD | |
| **DDR_D[12]** | U10 | I/O | IPD | |
| **DDR_D[11]** | T12 | I/O | IPD | |
| **DDR_D[10]** | T10 | I/O | IPD | |
| **DDR_D[9]** | T11 | I/O | IPD | |
| **DDR_D[8]** | T13 | I/O | IPD | |
| **DDR_D[7]** | W11 | I/O | IPD | |
| **DDR_D[6]** | W12 | I/O | IPD | |
| **DDR_D[5]** | V12 | I/O | IPD | |
| **DDR_D[4]** | V13 | I/O | IPD | |
| **DDR_D[3]** | U13 | I/O | IPD | |
| **DDR_D[2]** | V14 | I/O | IPD | |
| **DDR_D[1]** | U14 | I/O | IPD | |
| **DDR_D[0]** | U15 | I/O | IPD | |
| **DDR_A[13]** | T5 | O | IPD | DDR2 row/column address |
| **DDR_A[12]** | V4 | O | IPD | |
| **DDR_A[11]** | T4 | O | IPD | |
| **DDR_A[10]** | W4 | O | IPD | |
| **DDR_A[9]** | T6 | O | IPD | |
| **DDR_A[8]** | U4 | O | IPD | |
| **DDR_A[7]** | U6 | O | IPD | |
| **DDR_A[6]** | W5 | O | IPD | |
| **DDR_A[5]** | V5 | O | IPD | |
| **DDR_A[4]** | U5 | O | IPD | |
| **DDR_A[3]** | V6 | O | IPD | |
| **DDR_A[2]** | W6 | O | IPD | |
| **DDR_A[1]** | T7 | O | IPD | |
| **DDR_A[0]** | U7 | O | IPD | |
| **DDR_CLKP** | W8 | O | IPD | DDR2 clock (positive) |
| **$\overline{\text{DDR_CLKN}}$** | W7 | O | IPD | DDR2 clock (negative) |
| **DDR_CKE** | V7 | O | IPD | DDR2 clock enable |
| **$\overline{\text{DDR_WE}}$** | T8 | O | IPD | DDR2 write enable |
| **$\overline{\text{DDR_RAS}}$** | W9 | O | IPD | DDR2 row address strobe |
| **$\overline{\text{DDR_CAS}}$** | U9 | O | IPD | DDR2 column address strobe |
| **$\overline{\text{DDR_CS}}$** | V9 | O | IPD | DDR2 chip select |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.


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**Table 3-10. DDR2/mDDR Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **DDR_DQM[0]** | W13 | O | IPD | DDR2 data mask outputs |
| **DDR_DQM[1]** | R10 | O | IPD | |
| **DDR_DQS[0]** | T14 | I/O | IPD | DDR2 data strobe inputs/outputs |
| **DDR_DQS[1]** | V11 | I/O | IPD | |
| **DDR_BA[2]** | U8 | O | IPD | DDR2 SDRAM bank address |
| **DDR_BA[1]** | T9 | O | IPD | |
| **DDR_BA[0]** | V8 | O | IPD | |
| **DDR_DQGATE0** | R11 | O | IPD | DDR2 loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE1 with same constraints as used for DDR clock and data. |
| **DDR_DQGATE1** | R12 | I | IPD | DDR2 loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE0 with same constraints as used for DDR clock and data. |
| **DDR_ZP** | U12 | O | — | DDR2 reference output for drive strength calibration of N and P channel outputs. Tie to ground via 50 ohm resistor @ 5% tolerance. |
| **DDR_VREF** | R6 | I | — | DDR voltage input for the DDR2/mDDR I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary. |
| **DDR_DVDD18** | N6, N9, N10, P7, P8, P9, P10, R7, R8, R9 | PWR | — | DDR PHY 1.8V power supply pins |

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### 3.7.7 Serial Peripheral Interface Modules (SPI)

**Table 3-11. Serial Peripheral Interface (SPI) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **SPI1** | | | | | |
| **SPI1_CLK** / GP2[13] | G19 | I/O | CP[15] | A | SPI1 clock |
| **SPI1_ENA** / GP2[12] | H16 | I/O | CP[15] | A | SPI1 enable |
| **SPI1_SCS[0]** / EPWM1B / GP2[14] | E19 | I/O | CP[14] | A | SPI1 chip selects |
| **SPI1_SCS[1]** / EPWM1A / GP2[15] | F18 | I/O | CP[14] | A | |
| **SPI1_SCS[2]** / GP1[0] | F19 | I/O | CP[13] | A | |
| **SPI1_SCS[3]** / GP1[1] | E18 | I/O | CP[13] | A | |
| **SPI1_SCS[4]** / GP1[2] | F16 | I/O | CP[12] | A | |
| **SPI1_SCS[5]** / GP1[3] | F17 | I/O | CP[12] | A | |
| **SPI1_SCS[6]** / I2C0_SDA / GP1[4] | G18 | I/O | CP[11] | A | |
| **SPI1_SCS[7]** / I2C0_SCL / GP1[5] | G16 | I/O | CP[11] | A | |
| **SPI1_SIMO** / GP2[10] | G17 | I/O | CP[15] | A | SPI1 data slave-in-master-out |
| **SPI1_SOMI** / GP2[11] | H17 | I/O | CP[15] | A | SPI1 data slave-out-master-in |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 3.7.8 Enhanced Capture/Auxiliary PWM Modules (eCAP0)

The eCAP Module pins function as either input captures or auxiliary PWM 32-bit outputs, depending upon how the eCAP module is programmed.

**Table 3-12. Enhanced Capture Module (eCAP) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **eCAP0** | | | | | |
| AXR0 / **ECAP0_APWM0** / GP8[7] | F3 | I/O | CP[6] | A | enhanced capture 0 input or auxiliary PWM 0 output |
| **eCAP1** | | | | | |
| AXR8 / CLKS1 / **ECAP1_APWM1** / GP0[0] | E4 | I/O | CP[3] | A | enhanced capture 1 input or auxiliary PWM 1 output |
| **eCAP2** | | | | | |
| AXR15 / EPWM0TZ[0] / **ECAP2_APWM2** / GP0[7] | A4 | I/O | CP[1] | A | enhanced capture 2 input or auxiliary PWM 2 output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 3.7.9 Enhanced Pulse Width Modulators (eHRPWM)

**Table 3-13. Enhanced Pulse Width Modulator (eHRPWM) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **eHRPWM0** | | | | | |
| **EPWM0A** / GP1[8] | D19 | I/O | CP[7] | A | eHRPWM0 A output (with high-resolution) |
| **EPWM0B** | C17 | I/O | CP[7] | A | eHRPWM0 B output |
| AXR15 / **EPWM0TZ[0]** / ECAP2_APWM2 / GP0[7] | A4 | I | CP[1] | A | eHRPWM0 trip zone input |
| **EPWMSYNCI** / GP8[6] | C16 | I | CP[7] | A | eHRPWM0 sync input |
| **EPWMSYNCO** / GP8[5] | C18 | I/O | CP[7] | A | eHRPWM0 sync output |
| **eHRPWM1** | | | | | |
| $\overline{\text{SPI1_SCS[1]}}$ / **EPWM1A** / GP2[15] | F18 | I/O | CP[14] | A | eHRPWM1 A output (with high-resolution) |
| $\overline{\text{SPI1_SCS[0]}}$ / **EPWM1B** / GP2[14] | E19 | I/O | CP[14] | A | eHRPWM1 B output |
| AXR7 / **EPWM1TZ[0]** / GP1[15] | D2 | I | CP[4] | A | eHRPWM1 trip zone input |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 3.7.10 Boot

**Table 3-14. Boot Mode Selection Terminal Functions(1)**

| SIGNAL | | TYPE(2) | PULL(3) | POWER GROUP(4) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| GP7[7] / **BOOT[7]** | P4 | I | CP[29] | C | Boot Mode Selection Pins |
| GP7[6] / **BOOT[6]** | R3 | I | CP[29] | C | |
| GP7[5] / **BOOT[5]** | R2 | I | CP[29] | C | |
| GP7[4] / **BOOT[4]** | R1 | I | CP[29] | C | |
| GP7[3] / **BOOT[3]** | T3 | I | CP[29] | C | |
| GP7[2] / **BOOT[2]** | T2 | I | CP[29] | C | |
| GP7[1] / **BOOT[1]** | T1 | I | CP[29] | C | |
| GP7[0] / **BOOT[0]** | U3 | I | CP[29] | C | |

(1) Boot decoding is defined in the bootloader application report.
(2) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(3) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.
(4) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 3.7.11 Universal Asynchronous Receiver/Transmitters (UART0)

**Table 3-15. Universal Asynchronous Receiver/Transmitter (UART) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **UART0** | | | | | |
| **UART0_RXD** / GP8[4] | C19 | I | CP[8] | A | UART0 receive data |
| **UART0_TXD** / GP8[3] | D18 | O | CP[8] | A | UART0 transmit data |
| **$\overline{\text{UART0_RTS}}$** / GP8[1] | D16 | O | CP[9] | A | UART0 ready-to-send output |
| **$\overline{\text{UART0_CTS}}$** / GP8[2] | E17 | I | CP[9] | A | UART0 clear-to-send input |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 3.7.12 Inter-Integrated Circuit Modules(I2C0)

**Table 3-16. Inter-Integrated Circuit (I2C) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **I2C0** | | | | | |
| $\overline{\text{SPI1_SCS[6]}}$ / **I2C0_SDA** / GP1[4] | G18 | I/O | CP[11] | A | I2C0 serial data |
| $\overline{\text{SPI1_SCS[7]}}$ / **I2C0_SCL** / GP1[5] | G16 | I/O | CP[11] | A | I2C0 serial clock |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 3.7.13 Timers

**Table 3-17. Timers Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **TIMER0** | | | | | |
| TM64P0_OUT12 / GP1[7] /**TM64P0_IN12** | E16 | I | CP[10] | A | Timer0 lower input |
| **TM64P0_OUT12** / GP1[7] / TM64P0_IN12 | E16 | O | CP[10] | A | Timer0 lower output |
| **TIMER1 (Watchdog)** | | | | | |
| TM64P1_OUT12 / GP1[6] / **TM64P1_IN12** | D17 | I | CP[10] | A | Timer1 lower input |
| **TM64P1_OUT12** / GP1[6] / TM64P1_IN12 | D17 | O | CP[10] | A | Timer1 lower output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 3.7.14 Multichannel Audio Serial Ports (McASP)

**Table 3-18. Multichannel Audio Serial Ports Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP0** | | | | | |
| **AXR15** / EPWM0TZ[0] / ECAP2_APWM2 / GP0[7] | A4 | I/O | CP[1] | A | McASP0 serial data |
| **AXR14** / CLKR1 / GP0[6] | B4 | I/O | CP[2] | A | |
| **AXR13** / CLKX1 / GP0[5] | B3 | I/O | CP[2] | A | |
| **AXR12** / FSR1 / GP0[4] | C4 | I/O | CP[2] | A | |
| **AXR11** / FSX1 / GP0[3] | C5 | I/O | CP[2] | A | |
| **AXR10** / DR1 / GP0[2] | D4 | I/O | CP[2] | A | |
| **AXR9** / DX1 / GP0[1] | C3 | I/O | CP[2] | A | |
| **AXR8** / CLKS1 / ECAP1_APWM1 / GP0[0] | E4 | I/O | CP[3] | A | |
| **AXR7** / EPWM1TZ[0] / GP1[15] | D2 | I/O | CP[4] | A | |
| **AXR6** / GP1[14] | C1 | I/O | CP[5] | A | |
| **AXR5** / GP1[13] | D3 | I/O | CP[5] | A | |
| **AXR4** / GP1[12] | D1 | I/O | CP[5] | A | |
| **AXR3** / GP1[11] | E3 | I/O | CP[5] | A | |
| **AXR2** / GP1[10] | E2 | I/O | CP[5] | A | |
| **AXR1** / GP1[9] | E1 | I/O | CP[5] | A | |
| **AXR0** / ECAP0_APWM0 / GP8[7] | F3 | I/O | CP[6] | A | |
| **AHCLKX** / GP0[10] | A3 | I/O | CP[0] | A | McASP0 transmit master clock |
| **ACLKX** / GP0[14] | B1 | I/O | CP[0] | A | McASP0 transmit bit clock |
| **AFSX** / GP0[12] | B2 | I/O | CP[0] | A | McASP0 transmit frame sync |
| **AHCLKR** / GP0[11] | A2 | I/O | CP[0] | A | McASP0 receive master clock |
| **ACLKR** / GP0[15] | A1 | I/O | CP[0] | A | McASP0 receive bit clock |
| **AFSR** / GP0[13] | C2 | I/O | CP[0] | A | McASP0 receive frame sync |
| **AMUTE** / GP0[9] | D5 | I/O | CP[0] | A | McASP0 mute output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 3.7.15 Multichannel Buffered Serial Ports (McBSP)

**Table 3-19. Multichannel Buffered Serial Ports (McBSPs) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **McBSP1** | | | | | |
| AXR8 / **CLKS1** / ECAP1_APWM1 / GP0[0] | E4 | I | CP[3] | A | McBSP1 sample rate generator clock input |
| AXR14 / **CLKR1** / GP0[6] | B4 | I/O | CP[2] | A | McBSP1 receive clock |
| AXR12 / **FSR1** / GP0[4] | C4 | I/O | CP[2] | A | McBSP1 receive frame sync |
| AXR10 / **DR1** / GP0[2] | D4 | I | CP[2] | A | McBSP1 receive data |
| AXR13 / **CLKX1** / GP0[5] | B3 | I/O | CP[2] | A | McBSP1 transmit clock |
| AXR11 / **FSX1** / GP0[3] | C5 | I/O | CP[2] | A | McBSP1 transmit frame sync |
| AXR9 / **DX1** / GP0[1] | C3 | O | CP[2] | A | McBSP1 transmit data |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 3.7.16 Universal Host-Port Interface (UHPI)

**Table 3-20. Universal Host-Port Interface (UHPI) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **UHPI_HD[15]** | U18 | I/O | CP[26] | C | UHPI data bus |
| **UHPI_HD[14]** | V16 | I/O | CP[26] | C | |
| **UHPI_HD[13]** | R14 | I/O | CP[26] | C | |
| **UHPI_HD[12]** | W16 | I/O | CP[26] | C | |
| **UHPI_HD[11]** | V17 | I/O | CP[26] | C | |
| **UHPI_HD[10]** | W17 | I/O | CP[26] | C | |
| **UHPI_HD[9]** | W18 | I/O | CP[26] | C | |
| **UHPI_HD[8]** | W19 | I/O | CP[26] | C | |
| **UHPI_HD[7]** | V18 | I/O | CP[27] | C | |
| **UHPI_HD[6]** | V19 | I/O | CP[27] | C | |
| **UHPI_HD[5]** | U19 | I/O | CP[27] | C | |
| **UHPI_HD[4]** | T16 | I/O | CP[27] | C | |
| **UHPI_HD[3]** | R18 | I/O | CP[27] | C | |
| **UHPI_HD[2]** | R19 | I/O | CP[27] | C | |
| **UHPI_HD[1]** | R15 | I/O | CP[27] | C | |
| **UHPI_HD[0]** / GP6[5] | P17 | I/O | CP[27] | C | |
| **UHPI_HCNTL0** / GP6[11] | U17 | I | CP[24] | C | UHPI access control |
| **UHPI_HCNTL1** / GP6[10] | W15 | I | CP[24] | C | |
| **UHPI_HHWIL** / GP6[9] | U16 | I | CP[24] | C | UHPI half-word identification control |
| **UHPI_HR$\overline{W}$** / GP6[8] | T15 | I | CP[24] | C | UHPI read/write |
| **$\overline{UHPI_HCS}$** / GP6[7] | W14 | I | CP[25] | C | UHPI chip select |
| **$\overline{UHPI_HDS1}$** / GP6[6] | V15 | I | CP[25] | C | UHPI data strobe |
| CLKOUT / **$\overline{UHPI_HDS2}$** / GP6[14] | T18 | I | CP[22] | C | |
| **$\overline{UHPI_HINT}$** / GP6[12] | R16 | O | CP[23] | C | UHPI host interrupt |
| **$\overline{UHPI_HRDY}$** / GP6[13] | R17 | O | CP[23] | C | UHPI ready |
| $\overline{RESETOUT}$ / **$\overline{UHPI_HAS}$** / GP6[15] | T17 | I | CP[21] | C | UHPI address strobe |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 3.7.17 General Purpose Input Output

**Table 3-21. General Purpose Input Output Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **GP0** | | | | | |
| ACLKR / **GP0[15]** | A1 | I/O | CP[0] | A | GPIO Bank 0 |
| ACLKX / **GP0[14]** | B1 | I/O | CP[0] | A | |
| AFSR / **GP0[13]** | C2 | I/O | CP[0] | A | |
| AFSX / **GP0[12]** | B2 | I/O | CP[0] | A | |
| AHCLKR**GP0[11]** | A2 | I/O | CP[0] | A | |
| AHCLKX / **GP0[10]** | A3 | I/O | CP[0] | A | |
| AMUTE **GP0[9]** | D5 | I/O | CP[0] | A | |
| RTC_ALARM / **GP0[8]** / $\overline{\text{DEEPSLEEP}}$ | F4 | I/O | CP[0] | A | |
| AXR15 / EPWM0TZ[0] / ECAP2_APWM2 / **GP0[7]** | A4 | I/O | CP[1] | A | |
| AXR14 / CLKR1 / **GP0[6]** | B4 | I/O | CP[2] | A | |
| AXR13 / CLKX1 / **GP0[5]** | B3 | I/O | CP[2] | A | |
| AXR12 / FSR1 / **GP0[4]** | C4 | I/O | CP[2] | A | |
| AXR11 / FSX1 / **GP0[3]** | C5 | I/O | CP[2] | A | |
| AXR10 / DR1 / **GP0[2]** | D4 | I/O | CP[2] | A | |
| AXR9 / DX1 / **GP0[1]** | C3 | I/O | CP[2] | A | |
| AXR8 / CLKS1 / ECAP1_APWM1 /**GP0[0]** | E4 | I/O | CP[3] | A | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see the Device Configuration section. For electrical specifications on pullup and internal pulldown circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 3-21. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **GP1** | | | | | |
| AXR7 / EPWM1TZ[0] / **GP1[15]** | D2 | I/O | CP[4] | A | GPIO Bank 1 |
| AXR6 / **GP1[14]** | C1 | I/O | CP[5] | A | |
| AXR5 / **GP1[13]** | D3 | I/O | CP[5] | A | |
| AXR4 / **GP1[12]** | D1 | I/O | CP[5] | A | |
| AXR3 / **GP1[11]** | E3 | I/O | CP[5] | A | |
| AXR2 / **GP1[10]** | E2 | I/O | CP[5] | A | |
| AXR1 / **GP1[9]** | E1 | I/O | CP[5] | A | |
| EPWM0A / **GP1[8]** | D19 | I/O | CP[7] | A | |
| TM64P0_OUT12 / **GP1[7]** / TM64P0_IN12 | E16 | I/O | CP[10] | A | |
| TM64P1_OUT12 / **GP1[6]** / TM64P1_IN12 | D17 | I/O | CP[10] | A | |
| $\overline{\text{SPI1_SCS[7]}}$ / I2C0_SCL / **GP1[5]** | G16 | I/O | CP[11] | A | |
| $\overline{\text{SPI1_SCS[6]}}$ / I2C0_SDA / **GP1[4]** | G18 | I/O | CP[11] | A | |
| $\overline{\text{SPI1_SCS[5]}}$ / **GP1[3]** | F17 | I/O | CP[12] | A | |
| $\overline{\text{SPI1_SCS[4]}}$ / **GP1[2]** | F16 | I/O | CP[12] | A | |
| $\overline{\text{SPI1_SCS[3]}}$ / **GP1[1]** | E18 | I/O | CP[13] | A | |
| $\overline{\text{SPI1_SCS[2]}}$ / **GP1[0]** | F19 | I/O | CP[13] | A | |

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**Table 3-21. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **GP2** | | | | | |
| $\overline{\text{SPI1_SCS[1]}}$ / EPWM1A / **GP2[15]** | F18 | I/O | CP[14] | A | GPIO Bank 2 |
| $\overline{\text{SPI1_SCS[0]}}$ / EPWM1B / **GP2[14]** | E19 | I/O | CP[14] | A | |
| SPI1_CLK / **GP2[13]** | G19 | I/O | CP[15] | A | |
| $\overline{\text{SPI1_ENA}}$ / **GP2[12]** | H16 | I/O | CP[15] | A | |
| SPI1_SOMI / **GP2[11]** | H17 | I/O | CP[15] | A | |
| SPI1_SIMO / **GP2[10]** | G17 | I/O | CP[15] | A | |
| EMA_BA[1] / **GP2[9]** | A15 | I/O | CP[16] | B | |
| EMA_BA[0] / **GP2[8]** | C15 | I/O | CP[16] | B | |
| EMA_CLK / **GP2[7]** | B7 | I/O | CP[16] | B | |
| EMA_SDCKE / **GP2[6]** | D8 | I/O | CP[16] | B | |
| $\overline{\text{EMA_RAS}}$ / **GP2[5]** | A16 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CAS}}$ / **GP2[4]** | A9 | I/O | CP[16] | B | |
| $\overline{\text{EMA_WEN_DQM[0]}}$ / **GP2[3]** | C8 | I/O | CP[16] | B | |
| $\overline{\text{EMA_WEN_DQM[1]}}$ / **GP2[2]** | A5 | I/O | CP[16] | B | |
| EMA_WAIT[1] / **GP2[1]** | B19 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CS[0]}}$ / **GP2[0]** | A18 | I/O | CP[16] | B | |
| **GP3** | | | | | |
| $\overline{\text{EMA_CS[2]}}$ / **GP3[15]** | B17 | I/O | CP[16] | B | GPIO Bank 3 |
| $\overline{\text{EMA_CS[3]}}$ / **GP3[14]** | A17 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CS[4]}}$ / **GP3[13]** | F9 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CS[5]}}$ / **GP3[12]** | B16 | I/O | CP[16] | B | |
| $\overline{\text{EMA_WE}}$ / **GP3[11]** | B9 | I/O | CP[16] | B | |
| $\overline{\text{EMA_OE}}$ / **GP3[10]** | B15 | I/O | CP[16] | B | |
| EMA_A_$\overline{\text{RW}}$ / **GP3[9]** | D10 | I/O | CP[16] | B | |
| EMA_WAIT[0] / **GP3[8]** | B18 | I/O | CP[16] | B | |
| EMA_D[15] / **GP3[7]** | E6 | I/O | CP[17] | B | |
| EMA_D[14] / **GP3[6]** | C7 | I/O | CP[17] | B | |
| EMA_D[13] / **GP3[5]** | B6 | I/O | CP[17] | B | |
| EMA_D[12] / **GP3[4]** | A6 | I/O | CP[17] | B | |
| EMA_D[11] / **GP3[3]** | D6 | I/O | CP[17] | B | |
| EMA_D[10] / **GP3[2]** | A7 | I/O | CP[17] | B | |
| EMA_D[9] / **GP3[1]** | D9 | I/O | CP[17] | B | |
| EMA_D[8] / **GP3[0]** | E10 | I/O | CP[17] | B | |


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**Table 3-21. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **GP4** | | | | | |
| EMA_D[7] / **GP4[15]** | D7 | I/O | CP[17] | B | GPIO Bank 4 |
| EMA_D[6] / **GP4[14]** | C6 | I/O | CP[17] | B | |
| EMA_D[5] / **GP4[13]** | E7 | I/O | CP[17] | B | |
| EMA_D[4] / **GP4[12]** | B5 | I/O | CP[17] | B | |
| EMA_D[3] / **GP4[11]** | E8 | I/O | CP[17] | B | |
| EMA_D[2] / **GP4[10]** | B8 | I/O | CP[17] | B | |
| EMA_D[1] / **GP4[9]** | A8 | I/O | CP[17] | B | |
| EMA_D[0] / **GP4[8]** | C9 | I/O | CP[17] | B | |
| **GP4[7]** | E9 | I/O | CP[18] | B | |
| EMA_A[22] / **GP4[6]** | A10 | I/O | CP[18] | B | |
| EMA_A[21] / **GP4[5]** | B10 | I/O | CP[18] | B | |
| EMA_A[20] / **GP4[4]** | A11 | I/O | CP[18] | B | |
| EMA_A[19] / **GP4[3]** | C10 | I/O | CP[18] | B | |
| EMA_A[18] / **GP4[2]** | E11 | I/O | CP[18] | B | |
| EMA_A[17] / **GP4[1]** | B11 | I/O | CP[18] | B | |
| EMA_A[16] / **GP4[0]** | E12 | I/O | CP[18] | B | |
| **GP5** | | | | | |
| EMA_A[15] / **GP5[15]** | C11 | I/O | CP[19] | B | GPIO Bank 5 |
| EMA_A[14] / **GP5[14]** | A12 | I/O | CP[19] | B | |
| EMA_A[13] / **GP5[13]** | D11 | I/O | CP[19] | B | |
| EMA_A[12] / **GP5[12]** | D13 | I/O | CP[19] | B | |
| EMA_A[11] / **GP5[11]** | B12 | I/O | CP[19] | B | |
| EMA_A[10] / **GP5[10]** | C12 | I/O | CP[19] | B | |
| EMA_A[9] / **GP5[9]** | D12 | I/O | CP[19] | B | |
| EMA_A[8] / **GP5[8]** | A13 | I/O | CP[19] | B | |
| EMA_A[7] / **GP5[7]** | B13 | I/O | CP[20] | B | |
| EMA_A[6] / **GP5[6]** | E13 | I/O | CP[20] | B | |
| EMA_A[5] / **GP5[5]** | C13 | I/O | CP[20] | B | |
| EMA_A[4] / **GP5[4]** | A14 | I/O | CP[20] | B | |
| EMA_A[3] / **GP5[3]** | D14 | I/O | CP[20] | B | |
| EMA_A[2] / **GP5[2]** | B14 | I/O | CP[20] | B | |
| EMA_A[1] / **GP5[1]** | D15 | I/O | CP[20] | B | |
| EMA_A[0] / **GP5[0]** | C14 | I/O | CP[20] | B | |

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**Table 3-21. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **GP6** | | | | | |
| $\overline{\text{RESETOUT}}$ / $\overline{\text{UHPI_HAS}}$ / **GP6[15]** | T17 | I/O | CP[21] | C | GPIO Bank 6 |
| CLKOUT / $\overline{\text{UHPI_HDS2}}$ / **GP6[14]** | T18 | I/O | CP[22] | C | |
| $\overline{\text{UHPI_HRDY}}$ / **GP6[13]** | R17 | I/O | CP[23] | C | |
| $\overline{\text{UHPI_HINT}}$ / **GP6[12]** | R16 | I/O | CP[23] | C | |
| UHPI_HCNTL0 / **GP6[11]** | U17 | I/O | CP[24] | C | |
| UHPI_HCNTL1 / **GP6[10]** | W15 | I/O | CP[24] | C | |
| UHPI_HHWIL / **GP6[9]** | U16 | I/O | CP[24] | C | |
| UHPI_HR$\overline{\text{W}}$ **/GP6[8]** | T15 | I/O | CP[24] | C | |
| $\overline{\text{UHPI_HCS}}$ **GP6[7]** | W14 | I/O | CP[25] | C | |
| $\overline{\text{UHPI_HDS1}}$ / **GP6[6]** | V15 | I/O | CP[25] | C | |
| UHPI_HD[0] / **GP6[5]** | P17 | I/O | CP[27] | C | |
| **GP6[4]** | H3 | I/O | CP[30] | C | |
| **GP6[3]** | K3 | I/O | CP[30] | C | |
| **GP6[2]** | J3 | I/O | CP[30] | C | |
| **GP6[1]** | K4 | I/O | CP[30] | C | |
| **GP6[0]** | R5 | I/O | CP[31] | C | |
| **GP7** | | | | | |
| **GP7[15]** | U2 | I/O | CP[28] | C | GPIO Bank 7 |
| **GP7[14]** | U1 | I/O | CP[28] | C | |
| **GP7[13]** | V3 | I/O | CP[28] | C | |
| **GP7[12]** | V2 | I/O | CP[28] | C | |
| **GP7[11]** | V1 | I/O | CP[28] | C | |
| **GP7[10]** | W3 | I/O | CP[28] | C | |
| **GP7[9]** | W2 | I/O | CP[28] | C | |
| **GP7[8]** | W1 | I/O | CP[28] | C | |
| **GP7[7]** / BOOT[7] | P4 | I/O | CP[29] | C | |
| **GP7[6]** / BOOT[6] | R3 | I/O | CP[29] | C | |
| **GP7[5]**/ BOOT[5] | R2 | I/O | CP[29] | C | |
| **GP7[4]** / BOOT[4] | R1 | I/O | CP[29] | C | |
| **GP7[3]** / BOOT[3] | T3 | I/O | CP[29] | C | |
| **GP7[2]** / BOOT[2] | T2 | I/O | CP[29] | C | |
| **GP7[1]** / BOOT[1] | T1 | I/O | CP[29] | C | |
| **GP7[0]** / BOOT[0] | U3 | I/O | CP[29] | C | |


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**Table 3-21. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **GP8** | | | | | |
| **GP8[15]** | G1 | I/O | CP30] | C | GPIO Bank 8 |
| **GP8[14]** | G2 | I/O | CP[30] | C | |
| **GP8[13]** | J4 | I/O | CP[30] | C | |
| **GP8[12]** | G3 | I/O | CP[30] | C | |
| **GP8[11]** | F1 | I/O | CP[31] | C | |
| **GP8[10]** | F2 | I/O | CP[31] | C | |
| **GP8[9]** | H4 | I/O | CP[31] | C | |
| **GP8[8]** | G4 | I/O | CP[31] | C | |
| AXR0 / ECAP0_APWM0 / **GP8[7]** | F3 | I/O | CP[6] | A | |
| EPWMSYNCI / **GP8[6]** | C16 | I/O | CP[7] | A | |
| EPWMSYNCO / **GP8[5]** | C18 | I/O | CP[7] | A | |
| UART0_RXD / **GP8[4]** | C19 | I/O | CP[8] | A | |
| UART0_TXD / **GP8[3]** | D18 | I/O | CP[8] | A | |
| $\overline{\text{UART0_CTS}}$ / **GP8[2]** | E17 | I/O | CP[9] | A | |
| $\overline{\text{UART0_RTS}}$ / **GP8[1]** | D16 | I/O | CP[9] | A | |
| **GP8[0]**(4) | K17 | I/O | IPD | B | |

(4) GP8[0] is initially configured as a reserved function after reset and will not be in a predictable state. This signal will only be stable after the GPIO configuration for this pin has been completed. Users should carefully consider the system implications of this pin being in an unknown state after reset.

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### 3.7.18 Reserved and No Connect

**Table 3-22. Reserved and No Connect Terminal Functions**

| SIGNAL | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **RSV2** | T19 | PWR | Reserved. For proper device operation, this pin must be tied either directly to CVDD or left unconnected (do not connect to ground). |
| **RSV3** | M2, N4, P1, P2 | PWR | Reserved. On revision 1.x silicon, these pins must be tied to a static 1.2V supply. On revision 2.x silicon and later, these pins may be either tied to a static 1.2V supply or left unconnected. |
| **NC** | M3, M14, N16 | | Pin M3 should be left unconnected (***do not*** connect to power or ground)<br>Pins M14 and N16 may be left unconnected or connected to ground (VSS) |
| **NC** | J1, J2, K18, L1, L2, M18, M19, N1, N2, N3, N14, N17, N18, N19, P3, P14, P15, P16 P18, P19 | — | These pins should be left unconnected. |

(1) PWR = Supply voltage.


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### 3.7.19 Supply and Ground

**Table 3-23. Supply and Ground Terminal Functions**

| SIGNAL | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **CVDD** (Core supply) | E15, G7, G8, G13, H6, H7, H10, H11, H12, H13, J6, J12, K6, K12, L12, M8, M9, N8, M12 | PWR | Variable (1.2V - 1.0V) core supply voltage pins |
| **RVDD** (Internal RAM supply) | E5, H14, N7 | PWR | 1.2V internal ram supply voltage pins |
| **DVDD18** (I/O supply) | F14, G6, G10, G11, G12, J13, K5, L6, P13, R13 | PWR | 1.8V I/O supply voltage pins. DVDD18 must be powered even if all of the DVDD3318_x supplies are operated at 3.3V. |
| **DVDD3318_A** (I/O supply) | F5, F15, G5, G14, G15, H5 | PWR | 1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group A |
| **DVDD3318_B** (I/O supply) | E14, F6, F7, F8, F10, F11, F12, F13, G9, J14, K15 | PWR | 1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group B |
| **DVDD3318_C** (I/O supply) | J5, K13, L4, L13, M13, N13, P5, P6, P12, R4 | PWR | 1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group C |
| **VSS** (Ground) | A19, H8, H9, H15, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L5, L7, L8, L9, L10, L11, M4, M5, M6, M7, M10, M11, N5, N11, N12, P11 | GND | Ground pins. |
| **DDR_DVDD18** | N6, N9, N10, P7, P8, P9, P10, R7, R8, R9 | PWR | DDR PHY 1.8V power supply pins |

(1) PWR = Supply voltage, GND - Ground.

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## 3.8 Unused Pin Configurations

All signals multiplexed with multiple functions may be used as an alternate function if a given peripheral is not used. Unused non-multiplexed signals and some other specific signals should be handled as specified in the tables below.

If NMI is unused, it should be pulled-high externally through a 10k-ohm resistor to supply DVDD3318_B.

**Table 3-24. Unused RTC Signal Configuration**

| SIGNAL NAME | Configuration |
|---|---|
| RTC_XI | May be held high (CVDD) or low |
| $\overline{\text{RTC_XO}}$ | No Connect |
| RTC_ALARM | May be used as GPIO or other peripheral function |
| RTC_CVDD | Connect to CVDD |
| RTC_VSS | VSS |

**Table 3-25. Unused DDR2/mDDR Memory Controller Signal Configuration**

| SIGNAL NAME | Configuration (1) |
|---|---|
| DDR_D[15:0] | No Connect |
| DDR_A[13:0] | No Connect |
| DDR_CLKP | No Connect |
| DDR_CLKN | No Connect |
| DDR_CKE | No Connect |
| DDR_WE | No Connect |
| DDR_RAS | No Connect |
| DDR_CAS | No Connect |
| DDS_CS | No Connect |
| DDR_DQM[1:0] | No Connect |
| DDR_DQS[1:0] | No Connect |
| DDR_BA[2:0] | No Connect |
| DDR_DQGATE0 | No Connect |
| DDR_DQGATE1 | No Connect |
| DDR_ZP | No Connect |
| DDR_VREF | No Connect |
| DDR_DVDD18 | No Connect |

(1) The DDR2/mDDR input buffers are enabled by default on device power up and a maximum current draw of 25mA can result on the 1.8V supply. To minimize power consumption, the DDR2/mDDR controller input receivers should be placed in power-down mode by setting VTPIO[14] = 1.


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# 4 Device Configuration

## 4.1 Boot Modes

This device supports a variety of boot modes through an internal DSP ROM bootloader. This device does not support dedicated hardware boot modes; therefore, all boot modes utilize the internal DSP ROM. The input states of the BOOT pins are sampled and latched into the BOOTCFG register, which is part of the system configuration (SYSCFG) module, when device reset is deasserted. Boot mode selection is determined by the values of the BOOT pins.

See *Using the TMS320C6748/C6746/C6742 Bootloader* (SPRAAT2) for more details on the ROM Boot Loader.

The following boot modes are supported:

- NAND Flash boot
  - 8-bit NAND
  - 16-bit NAND (supported on ROM revisions after d800k002 -- see the bootloader documents mentioned above to determine the ROM revision)
- NOR Flash boot
  - NOR Direct boot (8-bit or 16-bit)
  - NOR Legacy boot (8-bit or 16-bit)
  - NOR AIS boot (8-bit or 16-bit)
- HPI Boot
- I2C0 Boot
  - EEPROM (Master Mode)
  - External Host (Slave Mode)
- SPI1 Boot
  - Serial Flash (Master Mode)
  - SERIAL EEPROM (Master Mode)
  - External Host (Slave Mode)
- UART0 Boot
  - External Host

## 4.2 SYSCFG Module

The following system level features of the chip are controlled by the SYSCFG peripheral:

- Readable Device, Die, and Chip Revision ID
- Control of Pin Multiplexing
- Priority of bus accesses different bus masters in the system
- Capture at power on reset the chip BOOT pin values and make them available to software
- Control of the DeepSleep power management function
- Enable and selection of the programmable pin pullups and pulldowns
- Special case settings for peripherals:
  - Locking of PLL controller settings
  - Default burst sizes for EDMA3 transfer controllers
  - Selection of the source for the eCAP module input capture (including on chip sources)
  - McASP AMUTEIN selection and clearing of AMUTE status for the McASP
  - Clock source selection for EMIFA
  - DDR2 Controller PHY settings
- Selects the source of emulation suspend signal (from DSP) of peripherals supporting this function.

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Many registers are accessible only by a host (DSP) when it is operating in its privileged mode. (ex. from the kernel, but not from user space code).

**Table 4-1. System Configuration (SYSCFG) Module Register Access**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | REGISTER ACCESS |
|---|---|---|---|
| 0x01C1 4000 | REVID | Revision Identification Register | — |
| 0x01C1 4008 | DIEIDR0 | Device Identification Register 0 | — |
| 0x01C1 400C | DIEIDR1 | Device Identification Register 1 | — |
| 0x01C1 4010 | DIEIDR2 | Device Identification Register 2 | — |
| 0x01C1 4014 | DIEIDR3 | Device Identification Register 3 | — |
| 0x01C1 4020 | BOOTCFG | Boot Configuration Register | Privileged mode |
| 0x01C1 4038 | KICK0R | Kick 0 Register | Privileged mode |
| 0x01C1 403C | KICK1R | Kick 1 Register | Privileged mode |
| 0x01C1 4044 | HOST1CFG | Host 1 Configuration Register | — |
| 0x01C1 40E0 | IRAWSTAT | Interrupt Raw Status/Set Register | Privileged mode |
| 0x01C1 40E4 | IENSTAT | Interrupt Enable Status/Clear Register | Privileged mode |
| 0x01C1 40E8 | IENSET | Interrupt Enable Register | Privileged mode |
| 0x01C1 40EC | IENCLR | Interrupt Enable Clear Register | Privileged mode |
| 0x01C1 40F0 | EOI | End of Interrupt Register | Privileged mode |
| 0x01C1 40F4 | FLTADDRR | Fault Address Register | Privileged mode |
| 0x01C1 40F8 | FLTSTAT | Fault Status Register | — |
| 0x01C1 4110 | MSTPRI0 | Master Priority 0 Registers | Privileged mode |
| 0x01C1 4114 | MSTPRI1 | Master Priority 1 Registers | Privileged mode |
| 0x01C1 4118 | MSTPRI2 | Master Priority 2 Registers | Privileged mode |
| 0x01C1 4120 | PINMUX0 | Pin Multiplexing Control 0 Register | Privileged mode |
| 0x01C1 4124 | PINMUX1 | Pin Multiplexing Control 1 Register | Privileged mode |
| 0x01C1 4128 | PINMUX2 | Pin Multiplexing Control 2 Register | Privileged mode |
| 0x01C1 412C | PINMUX3 | Pin Multiplexing Control 3 Register | Privileged mode |
| 0x01C1 4130 | PINMUX4 | Pin Multiplexing Control 4 Register | Privileged mode |
| 0x01C1 4134 | PINMUX5 | Pin Multiplexing Control 5 Register | Privileged mode |
| 0x01C1 4138 | PINMUX6 | Pin Multiplexing Control 6 Register | Privileged mode |
| 0x01C1 413C | PINMUX7 | Pin Multiplexing Control 7 Register | Privileged mode |
| 0x01C1 4140 | PINMUX8 | Pin Multiplexing Control 8 Register | Privileged mode |
| 0x01C1 4144 | PINMUX9 | Pin Multiplexing Control 9 Register | Privileged mode |
| 0x01C1 4148 | PINMUX10 | Pin Multiplexing Control 10 Register | Privileged mode |
| 0x01C1 414C | PINMUX11 | Pin Multiplexing Control 11 Register | Privileged mode |
| 0x01C1 4150 | PINMUX12 | Pin Multiplexing Control 12 Register | Privileged mode |
| 0x01C1 4154 | PINMUX13 | Pin Multiplexing Control 13 Register | Privileged mode |
| 0x01C1 4158 | PINMUX14 | Pin Multiplexing Control 14 Register | Privileged mode |
| 0x01C1 415C | PINMUX15 | Pin Multiplexing Control 15 Register | Privileged mode |
| 0x01C1 4160 | PINMUX16 | Pin Multiplexing Control 16 Register | Privileged mode |
| 0x01C1 4164 | PINMUX17 | Pin Multiplexing Control 17 Register | Privileged mode |
| 0x01C1 4168 | PINMUX18 | Pin Multiplexing Control 18 Register | Privileged mode |
| 0x01C1 416C | PINMUX19 | Pin Multiplexing Control 19 Register | Privileged mode |
| 0x01C1 4170 | SUSPSRC | Suspend Source Register | Privileged mode |
| 0x01C1 4174 | CHIPSIG | Chip Signal Register | — |
| 0x01C1 4178 | CHIPSIG_CLR | Chip Signal Clear Register | — |
| 0x01C1 417C | CFGCHIP0 | Chip Configuration 0 Register | Privileged mode |
| 0x01C1 4180 | CFGCHIP1 | Chip Configuration 1 Register | Privileged mode |


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**Table 4-1. System Configuration (SYSCFG) Module Register Access (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | REGISTER ACCESS |
|---|---|---|---|
| 0x01C1 4188 | CFGCHIP3 | Chip Configuration 3 Register | Privileged mode |
| 0x01C1 418C | CFGCHIP4 | Chip Configuration 4 Register | Privileged mode |
| 0x01E2 C000 | VTPIO_CTL | VTPIO COntrol Register | Privileged mode |
| 0x01E2 C004 | DDR_SLEW | DDR Slew Register | Privileged mode |
| 0x01E2 C008 | DeepSleep | DeepSleep Register | Privileged mode |
| 0x01E2 C00C | PUPD_ENA | Pullup / Pulldown Enable Register | Privileged mode |
| 0x01E2 C010 | PUPD_SEL | Pullup / Pulldown Selection Register | Privileged mode |
| 0x01E2 C014 | RXACTIVE | RXACTIVE Control Register | Privileged mode |

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## 4.3 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- Boot and Configuration Pins: If the pin is both routed out and 3-stated (not driven), an external pullup/pulldown resistor is strongly recommended, even if the IPU/IPD matches the desired value/state.
- Other Input Pins: If the IPU/IPD does not match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the boot and configuration pins, if they are both routed out and 3-stated (not driven), it is strongly recommended that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device boot and configuration pins. In addition, applying external pullup/pulldown resistors on the boot and configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest $V_{IL}$ level of all inputs connected to the net. For a pullup resistor, this should be above the highest $V_{IH}$ level of all inputs on the net. A reasonable choice would be to target the $V_{OL}$ or $V_{OH}$ levels for the logic family of the limiting device; which, by definition, have margin to the $V_{IL}$ and $V_{IH}$ levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the IO supply rail.
- For most systems, a 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.
- For most systems, a 20-kΩ resistor can be used to compliment the IPU/IPD on the boot and configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.
- For more detailed information on input current ($I_I$), and the low-/high-level input voltages ($V_{IL}$ and $V_{IH}$) for the device, see Section 5.3, Recommended Operating Conditions.
- For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table.


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# 5 Specifications

## 5.1 Absolute Maximum Ratings Over Operating Junction Temperature Range (Unless Otherwise Noted) (1)

| | | |
|---|---|---|
| Supply voltage ranges | Core Logic, Variable and Fixed (CVDD, RVDD, RTC_CVDD, PLL0_VDDA , PLL1_VDDA) (2) | -0.5 V to 1.4 V |
| | I/O, 1.8V (DDR_DVDD18) (2) | -0.5 V to 2 V |
| | I/O, 3.3V (DVDD3318_A, DVDD3318_B, DVDD3318_C) (2) | -0.5 V to 3.8V |
| Input voltage ($V_I$) ranges | Oscillator inputs (OSCIN, RTC_XI), 1.2V | -0.3 V to CVDD + 0.3V |
| | Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Steady State) | -0.3V to DVDD + 0.3V |
| | Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Transient Overshoot/Undershoot) | DVDD + 20% up to 20% of Signal Period |
| Output voltage ($V_O$) ranges | Dual-voltage LVCMOS outputs, 3.3V or 1.8V (Steady State) | -0.3 V to DVDD + 0.3V |
| | Dual-voltage LVCMOS outputs, operated at 3.3V (Transient Overshoot/Undershoot) | DVDD + 20% up to 20% of Signal Period |
| | Dual-voltage LVCMOS outputs, operated at 1.8V (Transient Overshoot/Undershoot) | DVDD + 30% up to 30% of Signal Period |
| Clamp Current | Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the I/O's internal diode protection cells. | ±20mA |
| Operating Junction Temperature ranges, $T_J$ | Commercial (default) | 0°C to 90°C |
| | Extended (A version) | -40°C to 105°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS, PLL0_VSSA, OSCVSS, RTC_VSS

## 5.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Storage temperature range, $T_{stg}$ | (default) | -55 | 150 | °C |
| ESD Stress Voltage, $V_{ESD}$ (1) | Human Body Model (HBM) | >1 | >1 | kV |
| | Charged Device Model (CDM) | >500 | >500 | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

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## 5.3 Recommended Operating Conditions

| | NAME | DESCRIPTION | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply Voltage | CVDD | Core Logic Supply Voltage (variable) | 1.2V operating point | 1.14 | 1.2 | 1.32 | V |
| | | | 1.1V operating point | 1.05 | 1.1 | 1.16 | V |
| | | | 1.0V operating point | 0.95 | 1.0 | 1.05 | V |
| | RVDD | Internal RAM Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | RTC_CVDD(1) | RTC Core Logic Supply Voltage | | 0.9 | 1.2 | 1.32 | V |
| | PLL0_VDDA | PLL0 Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | PLL1_VDDA | PLL1 Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | DVDD18(2) | 1.8V Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| | DDR_DVDD18 (2) | DDR2 PHY Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| | DDR_VREF | DDR2/mDDR reference voltage | | 0.49* DDR_DVDD18 | 0.5* DDR_DVDD18 | 0.51* DDR_DVDD18 | V |
| | DDR_ZP | DDR2/mDDR impedance control, connected via 50Ω resistor to Vss | | | Vss | | V |
| | DVDD3318_A | Power Group A Dual-voltage IO Supply Voltage | 1.8V operating point | 1.71 | 1.8 | 1.89 | V |
| | | | 3.3V operating point | 3.15 | 3.3 | 3.45 | V |
| | DVDD3318_B | Power Group B Dual-voltage IO Supply Voltage | 1.8V operating point | 1.71 | 1.8 | 1.89 | V |
| | | | 3.3V operating point | 3.15 | 3.3 | 3.45 | V |
| | DVDD3318_C | Power Group C Dual-voltage IO Supply Voltage | 1.8V operating point | 1.71 | 1.8 | 1.89 | V |
| | | | 3.3V operating point | 3.15 | 3.3 | 3.45 | V |
| Supply Ground | VSS | Core Logic Digital Ground | | 0 | 0 | 0 | V |
| | PLL0_VSSA | PLL0 Ground | | | | | |
| | PLL1_VSSA | PLL1 Ground | | | | | |
| | OSCVSS(3) | Oscillator Ground | | | | | |
| | RTC_VSS(3) | RTC Oscillator Ground | | | | | |
| Voltage Input High | $V_{IH}$ | High-level input voltage, Dual-voltage I/O, 3.3V(4) | | 2 | | | V |
| | | High-level input voltage, Dual-voltage I/O, 1.8V (4) | | 0.65*DVDD | | | V |
| | | High-level input voltage, RTC_XI | | 0.8*RTC_CVDD | | | V |
| | | High-level input voltage, OSCIN | | 0.8*CVDD | | | V |
| Voltage Input Low | $V_{IL}$ | Low-level input voltage, Dual-voltage I/O, 3.3V(4) | | | | 0.8 | V |
| | | Low-level input voltage, Dual-voltage I/O, 1.8V (4) | | | | 0.35*DVDD | V |
| | | Low-level input voltage, RTC_XI | | | | 0.2*RTC_CVDD | V |
| | | Low-level input voltage, OSCIN | | | | 0.2*CVDD | V |
| Transition Time | $t_t$ | Transition time, 10%-90%, All Inputs (unless otherwise specified in the electrical data sections) | | | | 0.25P or 10 (5) | ns |
| Operating Frequency | $F_{PLL0_SYSCLK1,6}$ | Commercial temperature grade (default) | CVDD = 1.2V operating point | 0 | | 200 | MHz |
| | | | CVDD = 1.1V operating point | 0 | | 150 | |
| | | | CVDD = 1.0V operating point | 0 | | 100 | |
| | | Extended temperature grade (A suffix) | CVDD = 1.2V operating point | 0 | | 200 | MHz |
| | | | CVDD = 1.1V operating point | 0 | | 150 | |
| | | | CVDD = 1.0V operating point | 0 | | 100 | |

(1) The RTC provides an option for isolating the RTC_CVDD from the CVDD to reduce current leakage when the RTC is powered independently. If these power supplies are not isolated (CTRL.SPLITPOWER=0), RTC_CVDD must be equal to or greater than CVDD. If these power supplies are isolated (CTRL.SPLITPOWER=1), RTC_CVDD may be lower than CVDD.
(2) DVDD18 must be powered even if all of the DVDD3318_x x supplies are operated at 3.3V.
(3) When an external crystal is used oscillator (OSC_VSS, RTC_VSS) ground must be kept separate from other grounds and connected directly to the crystal load capacitor ground. These pins are shorted to VSS on the device itself and should not be connected to VSS on the circuit board. If a crystal is not used and the clock input is driven directly, then the oscillator VSS may be connected to board ground.
(4) These IO specifications apply to the dual-voltage IOs only and do not apply to DDR2/mDDR . DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard.
(5) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.


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## 5.4 Notes on Recommended Power-On Hours (POH)

**The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.**

To avoid significant degradation, the device power-on hours (POH) must be limited to the following:

**Table 5-1. Recommended Power-On Hours**

| Silicon Revision | Speed Grade | Operating Junction Temperature (Tj) | Nominal CVDD Voltage (V) | Power-On Hours [POH] (hours) |
|---|---|---|---|---|
| A | 200 MHz | 0 to 90 °C | 1.2V | 100,000 |
| B/E | 200 MHz | 0 to 90 °C | 1.2V | 100,000 |
| B/E | 200 MHz | -40 to 105 °C | 1.2V | 100,000 |

**Note:** Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

**The above notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.**

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## 5.5 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Junction Temperature (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage (dual-voltage LVCMOS IOs at 3.3V)(1) | DVDD= 3.15V, $I_{OH}$ = -2 mA | 2.4 | | | V |
| | | DVDD= 3.15V, $I_{OH}$ = -100 µA | 2.95 | | | V |
| | High-level output voltage (dual-voltage LVCMOS IOs at 1.8V)(1) | DVDD= 1.71V, $I_{OH}$ = -2 mA | DVDD-0.45 | | | V |
| $V_{OL}$ | Low-level output voltage (dual-voltage LVCMOS I/Os at 3.3V)(1) | DVDD= 3.15V, $I_{OL}$ = 2mA | | | 0.4 | V |
| | | DVDD= 3.15V, $I_{OL}$ = 100 µA | | | 0.2 | V |
| | Low-level output voltage (dual-voltage LVCMOS I/Os at 1.8V)(1) | DVDD= 1.71V, $I_{OL}$ = 2mA | | | 0.45 | V |
| $I_I$ (2) | Input current(1) (dual-voltage LVCMOS I/Os) | $V_I$ = VSS to DVDD without opposing internal resistor | | | ±9 | µA |
| | | $V_I$ = VSS to DVDD with opposing internal pullup resistor (3) | 70 | | 310 | µA |
| | | $V_I$ = VSS to DVDD with opposing internal pulldown resistor (3) | -75 | | -270 | µA |
| | Input current (DDR2/mDDR I/Os) | $V_I$ = VSS to DVDD with opposing internal pulldown resistor (3) | -77 | | -286 | µA |
| $I_{OH}$ | High-level output current(1) (dual-voltage LVCMOS I/Os) | | | | -6 | mA |
| $I_{OL}$ | Low-level output current(1) (dual-voltage LVCMOS I/Os) | | | | 6 | mA |
| Capacitance | Input capacitance (dual-voltage LVCMOS) | | | 3 | | pF |
| | Output capacitance (dual-voltage LVCMOS) | | | 3 | | pF |

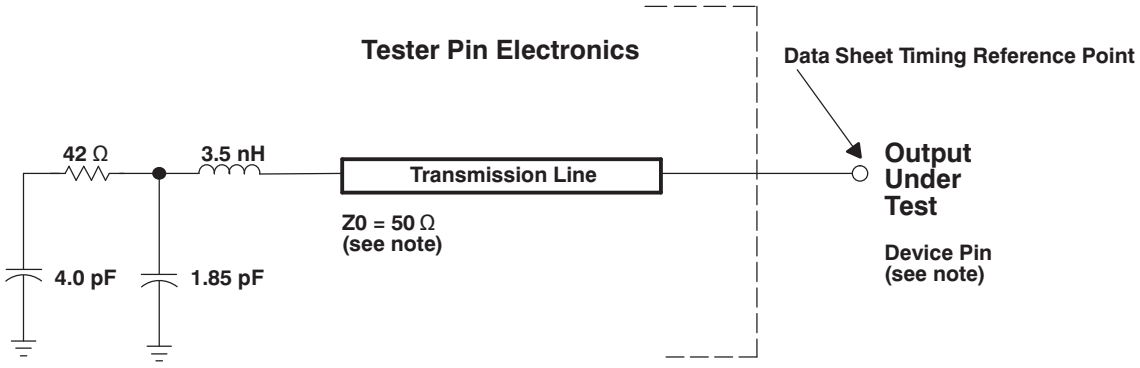
(1) These IO specifications apply to the dual-voltage IOs only and do not apply to the DDR2/mDDR interface. DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard.
(2) $I_I$ applies to input-only pins and bi-directional pins. For input-only pins, $I_I$ indicates the input leakage current. For bi-directional pins, $I_I$ indicates the input leakage current and off-state (Hi-Z) output leakage current.
(3) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor. The pull-up and pull-down strengths shown represent the minimum and maximum strength across process variation.


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# 6 Peripheral Information and Electrical Specifications

## 6.1 Parameter Information

### *6.1.1 Parameter Information Device-Specific Information*




A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin and the input signals are driven between 0V and the appropriate IO supply rail for the signal.

**Figure 6-1. Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 6.1.1.1 Signal Transition Levels

All input and output timing parameters are referenced to $V_{ref}$ for both "0" and "1" logic levels.

For 3.3 V I/O, $V_{ref}$ = 1.65 V.

For 1.8 V I/O, $V_{ref}$ = 0.9 V.

For 1.2 V I/O, $V_{ref}$ = 0.6 V.

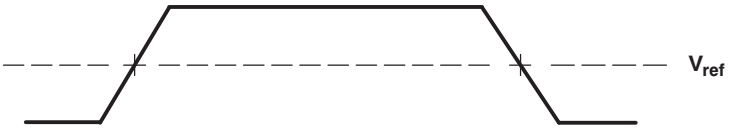



**Figure 6-2. Input and Output Voltage Reference Levels for AC Timing Measurements**

All rise and fall transition timing parameters are referenced to $V_{IL}$ MAX and $V_{IH}$ MIN for input clocks, $V_{OL}$MAX and $V_{OH}$ MIN for output clocks

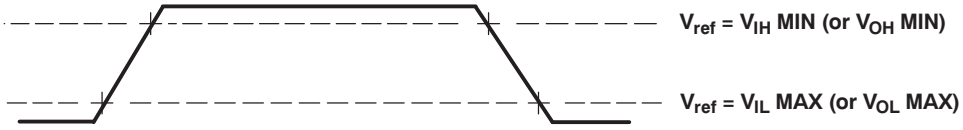



**Figure 6-3. Rise and Fall Transition Time Voltage Reference Levels**

## 6.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.

## 6.3 Power Supplies

### *6.3.1 Power-On Sequence*

The device should be powered-on in the following order:

1. RTC (RTC_CVDD) may be powered from an external device (such as a battery) prior to all other supplies being applied or powered-up at the same time as CVDD. If the RTC is not used, RTC_CVDD should be connected to CVDD. RTC_CVDD should not be left unpowered while CVDD is powered.
2. Core logic supplies:
   a. All variable 1.2V - 1.0V core logic supplies (CVDD)
   b. All static core logic supplies (RVDD, PLL0_VDDA, PLL1_VDDA). If voltage scaling is not used on the device, groups 2a) and 2b) can be controlled from the same power supply and powered up together.
3. All static 1.8V IO supplies (DVDD18, DDR_DVDD18) and any of the LVCMOS IO supply groups used at 1.8V nominal (DVDD3318_A, DVDD3318_B, or DVDD3318_C).
4. LVCMOS IO supply groups used at 3.3V nominal (DVDD3318_A, DVDD3318_B, or DVDD3318_C).

There is no specific required voltage ramp rate for any of the supplies as long as the LVCMOS supplies operated at 3.3V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed the STATIC 1.8V supplies by more than 2 volts.

RESET must be maintained active until all power supplies have reached their nominal values.

### *6.3.2 Power-Off Sequence*

The power supplies can be powered-off in any order as long as LVCMOS supplies operated at 3.3V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed static 1.8V supplies by more than 2 volts. There is no specific required voltage ramp down rate for any of the supplies (except as required to meet the above mentioned voltage condition).


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## 6.4 Reset

### 6.4.1 Power-On Reset (POR)

A power-on reset (POR) is required to place the device in a known good state after power-up. Power-On Reset is initiated by bringing RESET and TRST low at the same time. POR sets all of the device internal logic to its default state. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence, and RTCK/GP8[0]. During reset, GP8[0] is configured as a reserved function, and its behavior is not deterministic; the user should be aware that this pin will drive a level, and fact may toggle, during reset. RESETOUT in an output for use by other controllers in the system that indicates the device is currently in reset.

While both TRST and RESET need to be asserted upon power up, only RESET needs to be released for the device to boot properly. TRST may be asserted indefinitely for normal operation, keeping the JTAG port interface and device's emulation logic in the reset state.

TRST only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. Note: TRST is synchronous and must be clocked by TCK; otherwise, the boundary scan logic may not respond as expected after TRST is asserted.

RESET must be released only in order for boundary-scan JTAG to read the variant field of IDCODE correctly. Other boundary-scan instructions work correctly independent of current state of RESET. For maximum reliability, the device includes an internal pulldown on the TRST pin to ensure that TRST will always be asserted upon power up and the device's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of a pullup resistor on TRST. When using this type of JTAG controller, assert TRST to intialize the device after powerup and externally drive TRST high before attempting any emulation or boundary scan operations.

A summary of the effects of Power-On Reset is given below:

- All internal logic (including emulation logic and the PLL logic) is reset to its default state
- Internal memory is not maintained through a POR
- RESETOUT goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a POR. A software sequence is required to reset the RTC

**CAUTION: A watchdog reset triggers a POR.**

### 6.4.2 Warm Reset

A warm reset provides a limited reset to the device. Warm Reset is initiated by bringing only RESET low (TRST is maintained high through a warm reset). Warm reset sets certain portions of the device to their default state while leaving others unaltered. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence, and RTCK/GP8[0]. During reset, GP8[0] is configured as a reserved function, and its behavior is not deterministic; the user should be aware that this pin will drive a level, and fact may toggle, during reset. RESETOUT is an output for use by other controllers in the system that indicates the device is currently in reset.

During an emulation, the emulator will maintain TRST high and hence only warm reset (not POR) is available during emulation debug and development.

A summary of the effects of Warm Reset is given below:

- All internal logic (except for the emulation logic and the PLL logic) is reset to its default state
- Internal memory is maintained through a warm reset
- RESETOUT goes active
- All device pins go to a high-impedance state

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- The RTC peripheral is not reset during a warm reset. A software sequence is required to reset the RTC


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### 6.4.3 Reset Electrical Data Timings

Table 6-1 assumes testing over the recommended operating conditions.

**Table 6-1. Reset Timing Requirements ((1), (2))**

| NO. | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{w(RSTL)}$ | Pulse width, $\overline{RESET}$/$\overline{TRST}$ low | 100 | | 100 | | 100 | | ns |
| 2 | $t_{su(BPV-RSTH)}$ | Setup time, boot pins valid before $\overline{RESET}$/$\overline{TRST}$ high | 20 | | 20 | | 20 | | ns |
| 3 | $t_{h(RSTH-BPV)}$ | Hold time, boot pins valid after $\overline{RESET}$/$\overline{TRST}$ high | 20 | | 20 | | 20 | | ns |
| 4 | $t_{d(RSTH-RESETOUTH)}$ | $\overline{RESET}$ high to $\overline{RESETOUT}$ high; Warm reset | 4096 | | 4096 | | 4096 | | cycles(3) |
| | | $\overline{RESET}$ high to $\overline{RESETOUT}$ high; Power-on Reset | 6169 | | 6169 | | 6169 | | |
| 5 | $t_{d(RSTL-RESETOUTL)}$ | Delay time, $\overline{RESET}$/$\overline{TRST}$ low to $\overline{RESETOUT}$ low | | 14 | | 16 | | 20 | ns |

(1) $\overline{RESETOUT}$ is multiplexed with other pin functions. See the Terminal Functions table, Table 3-5 for details.
(2) For power-on reset (POR), the reset timings in this table refer to $\overline{RESET}$ and $\overline{TRST}$ together. For warm reset, the reset timings in this table refer to $\overline{RESET}$ only ($\overline{TRST}$ is held high).
(3) OSCIN cycles.

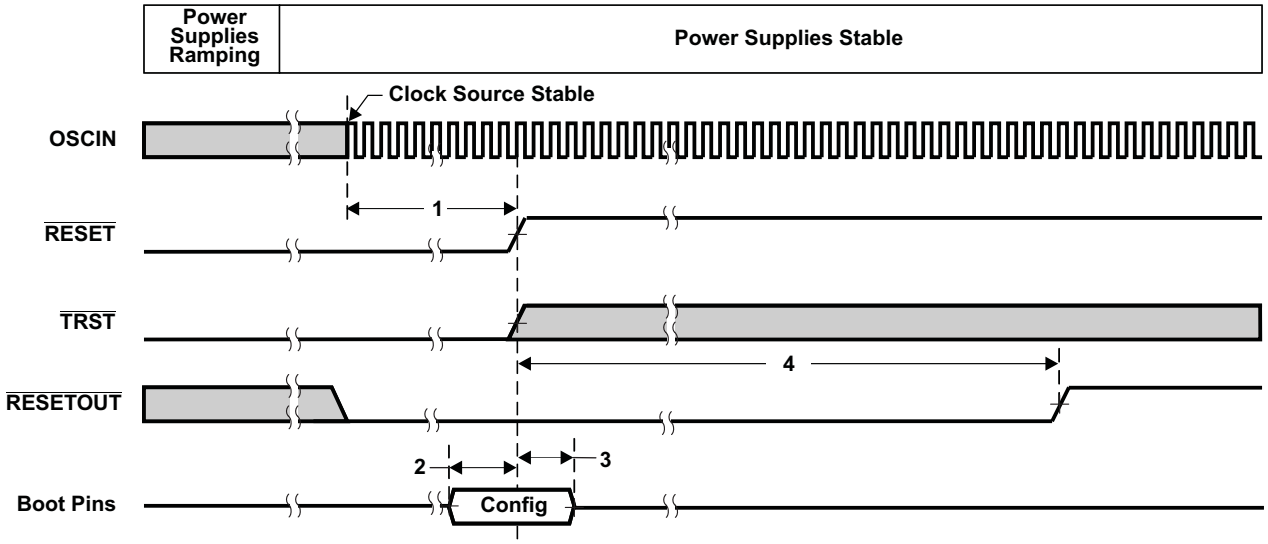



**Figure 6-4. Power-On Reset ($\overline{RESET}$ and $\overline{TRST}$ active) Timing**

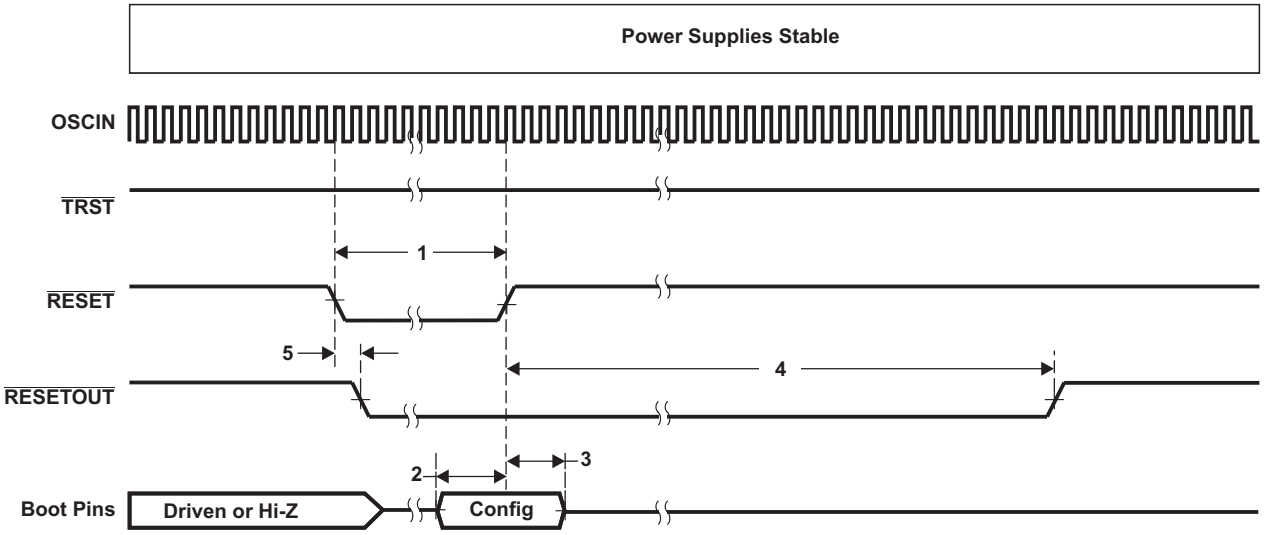



**Figure 6-5. Warm Reset (RESET active, TRST high) Timing**


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## 6.5 Crystal Oscillator or External Clock Input

The device includes two choices to provide an external clock input, which is fed to the on-chip PLLs to generate

high-frequency system clocks. These options are illustrated in Figure 6-6 and Figure 6-7. For input clock frequencies between 12 and 20 MHz, a crystal with 80 ohm max ESR is recommended. For input clock frequencies between 20 and 30 MHz, a crystal with 60 ohm max ESR is recommended. Typical load capacitance values are 10-20 pF, where the load capacitance is the series combination of C1 and C2.

The CLKMODE bit in the PLLCTL register must be 0 to use the on-chip oscillator. If CLKMODE is set to 1, the internal oscillator is disabled.

Figure 6-6 illustrates the option that uses on-chip 1.2V oscillator with external crystal circuit. Figure 6-7 illustrates the option that uses an external 1.2V clock input.

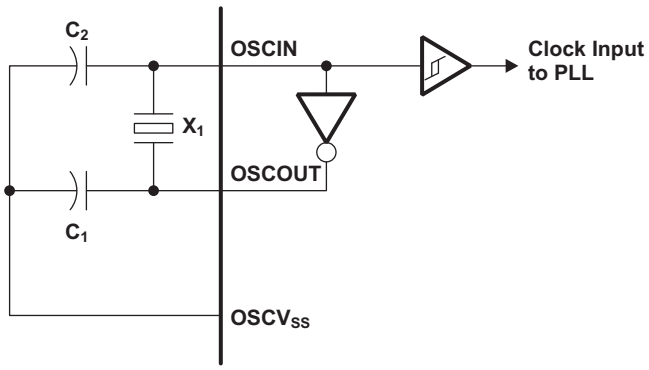



**Figure 6-6. On-Chip Oscillator**

**Table 6-2. Oscillator Timing Requirements**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{osc}$ | Oscillator frequency range (OSCIN/OSCOUT) | 12 | 30 | MHz |

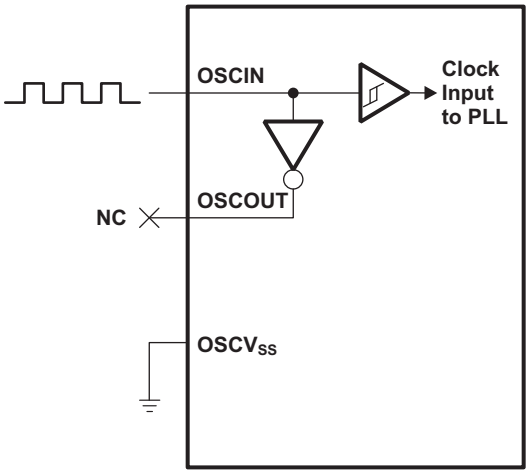



**Figure 6-7. External 1.2V Clock Source**

**Table 6-3. OSCIN Timing Requirements for an Externally Driven Clock**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{OSCIN}$ | OSCIN frequency range | 12 | 50 | MHz |
| $t_{c(OSCIN)}$ | Cycle time, external clock driven on OSCIN | 20 | | ns |
| $t_{w(OSCINH)}$ | Pulse width high, external clock on OSCIN | 0.4 $t_{c(OSCIN)}$ | | ns |
| $t_{w(OSCINL)}$ | Pulse width low, external clock on OSCIN | 0.4 $t_{c(OSCIN)}$ | | ns |
| $t_{t(OSCIN)}$ | Transition time, OSCIN | | 0.25P or 10 (1) | ns |
| $t_{j(OSCIN)}$ | Period jitter, OSCIN | | 0.02P | ns |

(1) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

## 6.6 Clock PLLs

The device has two PLL controllers that provide clocks to different parts of the system. PLL0 provides clocks (though various dividers) to most of the components of the device. PLL1 provides clocks to the DDR2/mDDR Controller and provides an alternate clock source for the ASYNC3 clock domain. This allows the peripherals on the ASYNC3 clock domain to be immune to frequency scaling operation on PLL0.

The PLL controller provides the following:

- Glitch-Free Transitions (on changing clock settings)
- Domain Clocks Alignment
- Clock Gating
- PLL power down

The various clock outputs given by the controller are as follows:

- Domain Clocks: SYSCLK [1:n]
- Auxiliary Clock from reference clock source: AUXCLK

Various dividers that can be used are as follows:

- Post-PLL Divider: POSTDIV
- SYSCLK Divider: D1, ¼, Dn

Various other controls supported are as follows:

- PLL Multiplier Control: PLLM
- Software programmable PLL Bypass: PLLEN


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### 6.6.1 PLL Device-Specific Information

The device DSP generates the high-frequency internal clocks it requires through an on-chip PLL.

The PLL requires some external filtering components to reduce power supply noise as shown in Figure 6-8.

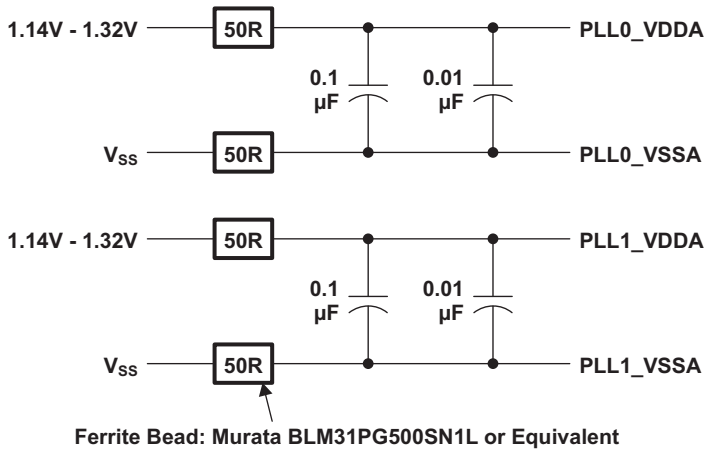



**Figure 6-8. PLL External Filtering Components**

The external filtering components shown above provide noise immunity for the PLLs. PLL0_VDDA and PLL1_VDDA should not be connected together to provide noise immunity between the two PLLs. Likewise, PLL0_VSSA and PLL1_VSSA should not be connected together.

The input to the PLL is either from the on-chip oscillator or from an external clock on the OSCIN pin. PLL0 outputs seven clocks that have programmable divider options. PLL1 outputs three clocks that have programmable divider options. Figure 6-9 illustrates the high-level view of the PLL Topology.

The PLLs are disabled by default after a device reset. They must be configured by software according to the allowable operating conditions listed in Table 6-4 before enabling the device to run from the PLL by setting PLLEN = 1.

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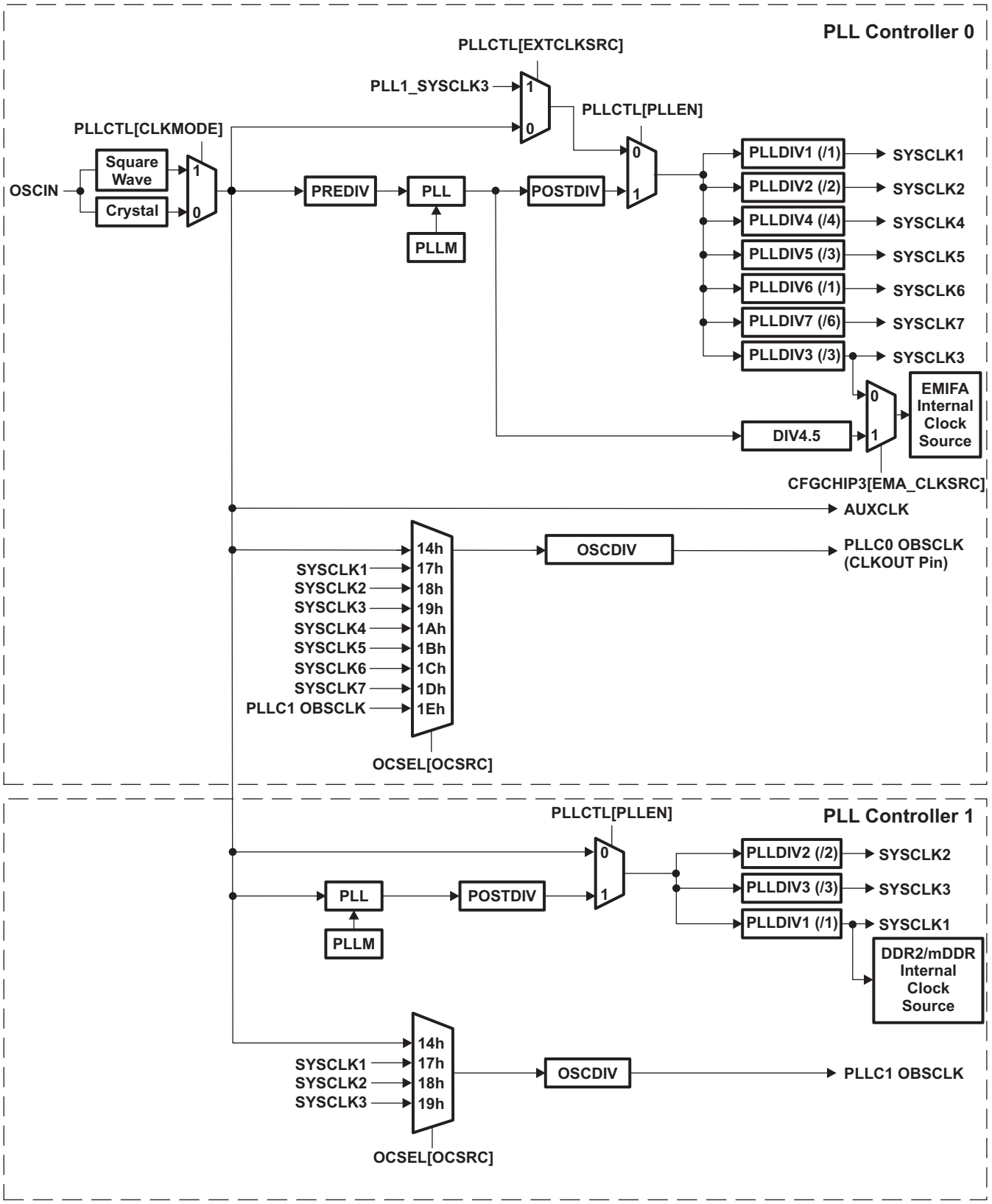



**Figure 6-9. PLL Topology**


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**Table 6-4. Allowed PLL Operating Conditions (PLL0 and PLL1)**

| NO. | PARAMETER | Default Value | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | **PLLRST**: Assertion time during initialization | N/A | 1000 | N/A | ns |
| 2 | **Lock time**: The time that the application has to wait for the PLL to acquire lock before setting PLLEN, after changing PREDIV, PLLM, or OSCIN | N/A | N/A | Max PLL Lock Time = $\frac{2000\,N}{\sqrt{m}}$ where N = Pre-Divider Ratio M = PLL Multiplier (1) | OSCIN cycles |
| 3 | **PREDIV**: Pre-divider value | /1 | /1 | /32 | - |
| 4 | **PLLREF**: PLL input frequency | | 12 | 30 (if internal oscillator is used) 50 (if external clock is used) | MHz |
| 5 | **PLLM**: PLL multiplier values | x20 | x4 | x32 | |
| 6 | **PLLOUT**: PLL output frequency | N/A | 300 | 600 | MHz |
| 7 | **POSTDIV**: Post-divider value | /1 | /1 | /32 | - |

(1) The multiplier values must be chosen such that the PLL output frequency (at PLLOUT) is between 300 and 600 MHz, but the frequency going into the SYSCLK dividers (after the post divider) cannot exceed the maximum clock frequency defined for the device at a given voltage operating point.

### 6.6.2 Device Clock Generation

PLL0 is controlled by PLL Controller 0 and PLL1 is controlled by PLL Controller 1. PLLC0 and PLLC1 manage the clock ratios, alignment, and gating for the system clocks to the chip. The PLLCs are responsible for controlling all modes of the PLL through software, in terms of pre-division of the clock inputs (PLLC0 only), multiply factors within the PLLs, and post-division for each of the chip-level clocks from the PLLs outputs. PLLC0 also controls reset propagation through the chip, clock alignment, and test points.

PLLC0 provides clocks for the majority of the system but PLLC1 provides clocks to the DDR2/mDDR Controller and the ASYNC3 clock domain to provide frequency scaling immunity to a defined set or peripherals. The ASYNC3 clock domain can either derive its clock from PLL1_SYSCLK2 (for frequency scaling immunity from PLL0) or from PLL0_SYSCLK2 (for synchronous timing with PLL0) depending on the application requirements. In addition, some peripherals have specific clock options independent of the ASYNC clock domain.

### 6.6.3 Dynamic Voltage and Frequency Scaling (DVFS)

The processor supports multiple operating points by scaling voltage and frequency to minimize power consumption for a given level of processor performance.

Frequency scaling is achieved by modifying the setting of the PLL controllers' multipliers, post-dividers (POSTDIV), and system clock dividers (SYSCLKn). Modification of the POSTDIV and SYSCLK values does not require relocking the PLL and provides lower latency to switch between operating points, but at the expense of the frequencies being limited by the integer divide values (only the divide values are altered the PLL multiplier is left unmodified). Non integer divide frequency values can be achieved by changing both the multiplier and the divide values, but when the PLL multiplier is changed the PLL must relock, incurring additional latency to change between operating points. Detailed information on modifying the PLL Controller settings can be found in the *TMS320C6742 DSP System Reference Guide* (SPRUGM5).

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Voltage scaling is enabled from outside the device by controlling an external voltage regulator. The processor may communicate with the regulator using GPIOs, I2C or some other interface. When switching between voltage-frequency operating points, the voltage must always support the desired frequency. When moving from a high-performance operating point to a lower performance operating point, the frequency should be lowered first followed by the voltage. When moving from a low-performance operating point to a higher performance operating point, the voltage should be raised first followed by the frequency. Voltage operating points refer to the CVdd voltage at that point. Other static supplies must be maintained at their nominal voltages at all operating points.

The maximum voltage slew rate for CVdd supply changes is 1 mV/us.

For additional information on power management solutions from TI for this processor, follow the Power Management link in the Product Folder on www.ti.com for this processor.

The processor supports multiple clock domains some of which have clock ratio requirements to each other. SYSCLK1:SYSCLK2:SYSCLK4:SYSCLK6 are synchronous to each other and the SYSCLKn dividers must always be configured such that the ratio between these domains is 1:2:4:1. The ASYNC and ASYNC3 clock domains are asynchronous to the other clock domains and have no specific ratio requirement.

Table 6-5 summarizes the maximum internal clock frequencies at each of the voltage operating points.

**Table 6-5. Maximum Internal Clock Frequencies at Each Voltage Operating Point**

| CLOCK SOURCE | CLOCK DOMAIN | | 1.2V NOM | 1.1V NOM | 1.0V NOM |
|---|---|---|---|---|---|
| PLL0_SYSCLK1 | DSP subsystem | | 200 MHz | 150 MHz | 100 MHz |
| PLL0_SYSCLK2 | SYSCLK2 clock domain peripherals and optional clock source for ASYNC3 clock domain peripherals | | 100 MHz | 75 MHz | 50 MHz |
| PLL0_SYSCLK3 | Optional clock for ASYNC1 clock domain (See ASYNC1 row) | | | | |
| PLL0_SYSCLK4 | SYSCLK4 domain peripherals | | 50 MHz | 37.5 MHz | 25 MHz |
| PLL0_SYSCLK5 | Not used on this processor | | - | - | - |
| PLL0_SYSCLK6 | Not used on this processor | | - | - | - |
| PLL0_SYSCLK7 | Not used on this processor | | - | - | - |
| PLL1_SYSCLK1 | DDR2/mDDR Interface clock source (memory interface clock is one-half of the value shown) | | 312 MHz | 300 MHz | 266 MHz |
| PLL1_SYSCLK2 | Optional clock source for ASYNC3 clock domain peripherals | | 150 MHz | 100 MHz | 75 MHz |
| PLL1_SYSCLK3 | Alternate clock source input to PLL Controller 0 | | 75 MHz | 75 MHz | 75 MHz |
| McASP AUXCLK | Bypass clock source for the McASP | | 50 MHz | 50 MHz | 50 MHz |
| PLL0_AUXCLK | Not used on this processor | | - | - | - |
| ASYNC1 | ASYNC Clock Domain (EMIFA) | Async Mode | 148 MHz | 75 MHz | 50 MHz |
| | | SDRAM Mode | 100 MHz | 66.6 MHz | 50 MHz |
| ASYNC2 | ASYNC2 Clock Domain (multiple peripherals) | | 50 MHz | 50 MHz | 50 MHz |

Some interfaces have specific limitations on supported modes/speeds at each operating point. See the corresponding peripheral sections of this document for more information.

TI provides software components (called the Power Manager) to perform DVFS and abstract the task from the user. The Power Manager controls changing operating points (both frequency and voltage) and handles the related tasks involved such as informing/controlling peripherals to provide graceful transitions between operating points. The Power Manager is bundled as a component of DSP/BIOS.


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## 6.7 Interrupts

The device has a large number of interrupts to service the needs of its many peripherals and subsystems.

### *6.7.1 DSP Interrupts*

The C674x DSP interrupt controller combines device events into 12 prioritized interrupts. The source for each of the 12 CPU interrupts is user programmable and is listed in Table 6-6. Also, the interrupt controller controls the generation of the CPU exceptions, NMI, and emulation interrupts. Table 6-7 summarizes the C674x interrupt controller registers and memory locations.

Refer to the *C674x DSP MegaModule Reference Guide* (SPRUFK5) and the *TMS320C674x DSP CPU and Instruction Set Reference Guide* (SPRUFE8) for details of the C674x interrupts.

**Table 6-6. C6742 DSP Interrupts**

| EVT# | Interrupt Name | Source |
|---|---|---|
| 0 | EVT0 | C674x Int Ctl 0 |
| 1 | EVT1 | C674x Int Ctl 1 |
| 2 | EVT2 | C674x Int Ctl 2 |
| 3 | EVT3 | C674x Int Ctl 3 |
| 4 | T64P0_TINT12 | Timer64P0 - TINT12 |
| 5 | SYSCFG_CHIPINT2 | SYSCFG CHIPSIG Register |
| 6 | - | Reserved |
| 7 | EHRPWM0 | HiResTimer/PWM0 Interrupt |
| 8 | EDMA3_0_CC0_INT1 | EDMA3_0 Channel Controller 0 Shadow Region 1 Transfer Completion Interrupt |
| 9 | EMU_DTDMA | C674x-ECM |
| 10 | EHRPWM0TZ | HiResTimer/PWM0 Trip Zone Interrupt |
| 11 | EMU_RTDXRX | C674x-RTDX |
| 12 | EMU_RTDXTX | C674x-RTDX |
| 13 | IDMAINT0 | C674x-EMC |
| 14 | IDMAINT1 | C674x-EMC |
| 15-17 | - | Reserved |
| 18 | EHRPWM1 | HiResTimer/PWM1 Interrupt |
| 19-22 | - | Reserved |
| 22 | - | Reserved |
| 23 | EHRPWM1TZ | HiResTimer/PWM1 Trip Zone Interrupt |
| 24-33 | - | Reserved |
| 34 | UHPI_DSPINT | UHPI DSP Interrupt |
| 35 | - | Reserved |
| 36 | IIC0_INT | I2C0 |
| 37 | - | Reserved |
| 38 | UART0_INT | UART0 |
| 39 | - | Reserved |
| 40 | T64P1_TINT12 | Timer64P1 Interrupt 12 |
| 41 | GPIO_B1INT | GPIO Bank 1 Interrupt |
| 42 | - | Reserved |
| 43 | SPI1_INT | SPI1 |
| 44 | - | Reserved |
| 45 | ECAP0 | ECAP0 |
| 46 | - | Reserved |
| 47 | ECAP1 | ECAP1 |

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**Table 6-6. C6742 DSP Interrupts (continued)**

| EVT# | Interrupt Name | Source |
|---|---|---|
| 48 | T64P1_TINT34 | Timer64P1 Interrupt 34 |
| 49 | GPIO_B2INT | GPIO Bank 2 Interrupt |
| 50 | - | Reserved |
| 51 | ECAP2 | ECAP2 |
| 52 | GPIO_B3INT | GPIO Bank 3 Interrupt |
| 53 | - | Reserved |
| 54 | GPIO_B4INT | GPIO Bank 4 Interrupt |
| 55 | EMIFA_INT | EMIFA |
| 56 | EDMA3_0_CC0_ERRINT | EDMA3_0 Channel Controller 0 Error Interrupt |
| 57 | EDMA3_0_TC0_ERRINT | EDMA3_0 Transfer Controller 0 Error Interrupt |
| 58 | EDMA3_0_TC1_ERRINT | EDMA3_0 Transfer Controller 1 Error Interrupt |
| 59 | GPIO_B5INT | GPIO Bank 5 Interrupt |
| 60 | DDR2_MEMERR | DDR2 Memory Error Interrupt |
| 61 | MCASP0_INT | McASP0 Combined RX/TX Interrupts |
| 62 | GPIO_B6INT | GPIO Bank 6 Interrupt |
| 63 | RTC_IRQS | RTC Combined |
| 64 | T64P0_TINT34 | Timer64P0 Interrupt 34 |
| 65 | GPIO_B0INT | GPIO Bank 0 Interrupt |
| 66 | - | Reserved |
| 67 | SYSCFG_CHIPINT3 | SYSCFG_CHIPSIG Register |
| 68 | - | Reserved |
| 69 | - | Reserved |
| 70 | PSC0_ALLINT | PSC0 |
| 71 | PSC1_ALLINT | PSC1 |
| 72 | GPIO_B7INT | GPIO Bank 7 Interrupt |
| 73 | - | Reserved |
| 74 | PROTERR | SYSCFG Protection Shared Interrupt |
| 75 | GPIO_B8INT | GPIO Bank 8 Interrupt |
| 76-88 | - | Reserved |
| 89 | MCBSP1_RINT | McBSP1 Receive Interrupt |
| 90 | MCBSP1_XINT | McBSP1 Transmit Interrupt |
| 91 | EDMA3_1_CC0_INT1 | EDMA3_1 Channel Controller 0 Shadow Region 1 Transfer Completion Interrupt |
| 92 | EDMA3_1_CC0_ERRINT | EDMA3_1 Channel Controller 0 Error Interrupt |
| 93 | EDMA3_1_TC0_ERRINT | EDMA3_1 Transfer Controller 0 Error Interrupt |
| 94-95 | - | Reserved |
| 96 | INTERR | C674x-Int Ctl |
| 97 | EMC_IDMAERR | C674x-EMC |
| 98 - 112 | - | Reserved |
| 113 | PMC_ED | C674x-PMC |
| 114 - 115 | - | Reserved |
| 116 | UMC_ED1 | C674x-UMC |
| 117 | UMC_ED2 | C674x-UMC |
| 118 | PDC_INT | C674x-PDC |
| 119 | SYS_CMPA | C674x-SYS |
| 120 | PMC_CMPA | C674x-PMC |
| 121 | PMC_CMPA | C674x-PMC |
| 122 | DMC_CMPA | C674x-DMC |


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**Table 6-6. C6742 DSP Interrupts (continued)**

| EVT# | Interrupt Name | Source |
|---|---|---|
| 123 | DMC_CMPA | C674x-DMC |
| 124 | UMC_CMPA | C674x-UMC |
| 125 | UMC_CMPA | C674x-UMC |
| 126 | EMC_CMPA | C674x-EMC |
| 127 | EMC_BUSERR | C674x-EMC |

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**Table 6-7. C674x DSP Interrupt Controller Registers**

| BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0180 0000 | EVTFLAG0 | Event flag register 0 |
| 0x0180 0004 | EVTFLAG1 | Event flag register 1 |
| 0x0180 0008 | EVTFLAG2 | Event flag register 2 |
| 0x0180 000C | EVTFLAG3 | Event flag register 3 |
| 0x0180 0020 | EVTSET0 | Event set register 0 |
| 0x0180 0024 | EVTSET1 | Event set register 1 |
| 0x0180 0028 | EVTSET2 | Event set register 2 |
| 0x0180 002C | EVTSET3 | Event set register 3 |
| 0x0180 0040 | EVTCLR0 | Event clear register 0 |
| 0x0180 0044 | EVTCLR1 | Event clear register 1 |
| 0x0180 0048 | EVTCLR2 | Event clear register 2 |
| 0x0180 004C | EVTCLR3 | Event clear register 3 |
| 0x0180 0080 | EVTMASK0 | Event mask register 0 |
| 0x0180 0084 | EVTMASK1 | Event mask register 1 |
| 0x0180 0088 | EVTMASK2 | Event mask register 2 |
| 0x0180 008C | EVTMASK3 | Event mask register 3 |
| 0x0180 00A0 | MEVTFLAG0 | Masked event flag register 0 |
| 0x0180 00A4 | MEVTFLAG1 | Masked event flag register 1 |
| 0x0180 00A8 | MEVTFLAG2 | Masked event flag register 2 |
| 0x0180 00AC | MEVTFLAG3 | Masked event flag register 3 |
| 0x0180 00C0 | EXPMASK0 | Exception mask register 0 |
| 0x0180 00C4 | EXPMASK1 | Exception mask register 1 |
| 0x0180 00C8 | EXPMASK2 | Exception mask register 2 |
| 0x0180 00CC | EXPMASK3 | Exception mask register 3 |
| 0x0180 00E0 | MEXPFLAG0 | Masked exception flag register 0 |
| 0x0180 00E4 | MEXPFLAG1 | Masked exception flag register 1 |
| 0x0180 00E8 | MEXPFLAG2 | Masked exception flag register 2 |
| 0x0180 00EC | MEXPFLAG3 | Masked exception flag register 3 |
| 0x0180 0104 | INTMUX1 | Interrupt mux register 1 |
| 0x0180 0108 | INTMUX2 | Interrupt mux register 2 |
| 0x0180 010C | INTMUX3 | Interrupt mux register 3 |
| 0x0180 0140 - 0x0180 0144 | - | Reserved |
| 0x0180 0180 | INTXSTAT | Interrupt exception status |
| 0x0180 0184 | INTXCLR | Interrupt exception clear |
| 0x0180 0188 | INTDMASK | Dropped interrupt mask register |
| 0x0180 01C0 | EVTASRT | Event assert register |


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## 6.8 Power and Sleep Controller (PSC)

The Power and Sleep Controllers (PSC) are responsible for managing transitions of system power on/off, clock on/off, resets (device level and module level). It is used primarily to provide granular power control for on chip modules (peripherals and CPU). A PSC module consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, PSC interrupts, a state machine for each peripheral/module it controls. An LPSC is associated with every module that is controlled by the PSC and provides clock and reset control.

The PSC includes the following features:

- Provides a software interface to:
  - Control module clock enable/disable
  - Control module reset
  - Control CPU local reset
- Supports IcePick emulation features: power, clock and reset

  PSC0 controls 16 local PSCs.

  PSC1 controls 32 local PSCs.

**Table 6-8. Power and Sleep Controller (PSC) Registers**

| PSC0 BYTE ADDRESS | PSC1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C1 0000 | 0x01E2 7000 | REVID | Peripheral Revision and Class Information Register |
| 0x01C1 0018 | 0x01E2 7018 | INTEVAL | Interrupt Evaluation Register |
| 0x01C1 0040 | 0x01E2 7040 | MERRPR0 | Module Error Pending Register 0 (module 0-15) (PSC0)<br>Module Error Pending Register 0 (module 0-31) (PSC1) |
| 0x01C1 0050 | 0x01E2 7050 | MERRCR0 | Module Error Clear Register 0 (module 0-15) (PSC0)<br>Module Error Clear Register 0 (module 0-31) (PSC1) |
| 0x01C1 0060 | 0x01E2 7060 | PERRPR | Power Error Pending Register |
| 0x01C1 0068 | 0x01E2 7068 | PERRCR | Power Error Clear Register |
| 0x01C1 0120 | 0x01E2 7120 | PTCMD | Power Domain Transition Command Register |
| 0x01C1 0128 | 0x01E2 7128 | PTSTAT | Power Domain Transition Status Register |
| 0x01C1 0200 | 0x01E2 7200 | PDSTAT0 | Power Domain 0 Status Register |
| 0x01C1 0204 | 0x01E2 7204 | PDSTAT1 | Power Domain 1 Status Register |
| 0x01C1 0300 | 0x01E2 7300 | PDCTL0 | Power Domain 0 Control Register |
| 0x01C1 0304 | 0x01E2 7304 | PDCTL1 | Power Domain 1 Control Register |
| 0x01C1 0400 | 0x01E2 7400 | PDCFG0 | Power Domain 0 Configuration Register |
| 0x01C1 0404 | 0x01E2 7404 | PDCFG1 | Power Domain 1 Configuration Register |
| 0x01C1 0800 | 0x01E2 7800 | MDSTAT0 | Module 0 Status Register |
| 0x01C1 0804 | 0x01E2 7804 | MDSTAT1 | Module 1 Status Register |
| 0x01C1 0808 | 0x01E2 7808 | MDSTAT2 | Module 2 Status Register |
| 0x01C1 080C | 0x01E2 780C | MDSTAT3 | Module 3 Status Register |
| 0x01C1 0810 | 0x01E2 7810 | MDSTAT4 | Module 4 Status Register |
| 0x01C1 0814 | 0x01E2 7814 | MDSTAT5 | Module 5 Status Register |
| 0x01C1 0818 | 0x01E2 7818 | MDSTAT6 | Module 6 Status Register |
| 0x01C1 081C | 0x01E2 781C | MDSTAT7 | Module 7 Status Register |
| 0x01C1 0820 | 0x01E2 7820 | MDSTAT8 | Module 8 Status Register |
| 0x01C1 0824 | 0x01E2 7824 | MDSTAT9 | Module 9 Status Register |
| 0x01C1 0828 | 0x01E2 7828 | MDSTAT10 | Module 10 Status Register |
| 0x01C1 082C | 0x01E2 782C | MDSTAT11 | Module 11 Status Register |
| 0x01C1 0830 | 0x01E2 7830 | MDSTAT12 | Module 12 Status Register |
| 0x01C1 0834 | 0x01E2 7834 | MDSTAT13 | Module 13 Status Register |

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**Table 6-8. Power and Sleep Controller (PSC) Registers (continued)**

| PSC0 BYTE ADDRESS | PSC1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C1 0838 | 0x01E2 7838 | MDSTAT14 | Module 14 Status Register |
| 0x01C1 083C | 0x01E2 783C | MDSTAT15 | Module 15 Status Register |
| - | 0x01E2 7840 | MDSTAT16 | Module 16 Status Register |
| - | 0x01E2 7844 | MDSTAT17 | Module 17 Status Register |
| - | 0x01E2 7848 | MDSTAT18 | Module 18 Status Register |
| - | 0x01E2 784C | MDSTAT19 | Module 19 Status Register |
| - | 0x01E2 7850 | MDSTAT20 | Module 20 Status Register |
| - | 0x01E2 7854 | MDSTAT21 | Module 21 Status Register |
| - | 0x01E2 7858 | MDSTAT22 | Module 22 Status Register |
| - | 0x01E2 785C | MDSTAT23 | Module 23 Status Register |
| - | 0x01E2 7860 | MDSTAT24 | Module 24 Status Register |
| - | 0x01E2 7864 | MDSTAT25 | Module 25 Status Register |
| - | 0x01E2 7868 | MDSTAT26 | Module 26 Status Register |
| - | 0x01E2 786C | MDSTAT27 | Module 27 Status Register |
| - | 0x01E2 7870 | MDSTAT28 | Module 28 Status Register |
| - | 0x01E2 7874 | MDSTAT29 | Module 29 Status Register |
| - | 0x01E2 7878 | MDSTAT30 | Module 30 Status Register |
| - | 0x01E2 787C | MDSTAT31 | Module 31 Status Register |
| 0x01C1 0A00 | 0x01E2 7A00 | MDCTL0 | Module 0 Control Register |
| 0x01C1 0A04 | 0x01E2 7A04 | MDCTL1 | Module 1 Control Register |
| 0x01C1 0A08 | 0x01E2 7A08 | MDCTL2 | Module 2 Control Register |
| 0x01C1 0A0C | 0x01E2 7A0C | MDCTL3 | Module 3 Control Register |
| 0x01C1 0A10 | 0x01E2 7A10 | MDCTL4 | Module 4 Control Register |
| 0x01C1 0A14 | 0x01E2 7A14 | MDCTL5 | Module 5 Control Register |
| 0x01C1 0A18 | 0x01E2 7A18 | MDCTL6 | Module 6 Control Register |
| 0x01C1 0A1C | 0x01E2 7A1C | MDCTL7 | Module 7 Control Register |
| 0x01C1 0A20 | 0x01E2 7A20 | MDCTL8 | Module 8 Control Register |
| 0x01C1 0A24 | 0x01E2 7A24 | MDCTL9 | Module 9 Control Register |
| 0x01C1 0A28 | 0x01E2 7A28 | MDCTL10 | Module 10 Control Register |
| 0x01C1 0A2C | 0x01E2 7A2C | MDCTL11 | Module 11 Control Register |
| 0x01C1 0A30 | 0x01E2 7A30 | MDCTL12 | Module 12 Control Register |
| 0x01C1 0A34 | 0x01E2 7A34 | MDCTL13 | Module 13 Control Register |
| 0x01C1 0A38 | 0x01E2 7A38 | MDCTL14 | Module 14 Control Register |
| 0x01C1 0A3C | 0x01E2 7A3C | MDCTL15 | Module 15 Control Register |
| - | 0x01E2 7A40 | MDCTL16 | Module 16 Control Register |
| - | 0x01E2 7A44 | MDCTL17 | Module 17 Control Register |
| - | 0x01E2 7A48 | MDCTL18 | Module 18 Control Register |
| - | 0x01E2 7A4C | MDCTL19 | Module 19 Control Register |
| - | 0x01E2 7A50 | MDCTL20 | Module 20 Control Register |
| - | 0x01E2 7A54 | MDCTL21 | Module 21 Control Register |
| - | 0x01E2 7A58 | MDCTL22 | Module 22 Control Register |
| - | 0x01E2 7A5C | MDCTL23 | Module 23 Control Register |
| - | 0x01E2 7A60 | MDCTL24 | Module 24 Control Register |
| - | 0x01E2 7A64 | MDCTL25 | Module 25 Control Register |
| - | 0x01E2 7A68 | MDCTL26 | Module 26 Control Register |
| - | 0x01E2 7A6C | MDCTL27 | Module 27 Control Register |
| - | 0x01E2 7A70 | MDCTL28 | Module 28 Control Register |


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**Table 6-8. Power and Sleep Controller (PSC) Registers (continued)**

| PSC0 BYTE ADDRESS | PSC1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| - | 0x01E2 7A74 | MDCTL29 | Module 29 Control Register |
| - | 0x01E2 7A78 | MDCTL30 | Module 30 Control Register |
| - | 0x01E2 7A7C | MDCTL31 | Module 31 Control Register |

### 6.8.1 Power Domain and Module Topology

The device includes two PSC modules.

Each PSC module controls clock states for several of the on chip modules, controllers and interconnect components. Table 6-9 and Table 6-10 lists the set of peripherals/modules that are controlled by the PSC, the power domain they are associated with, the LPSC assignment and the default (power-on reset) module states. The module states and terminology are defined in Section 6.8.1.2.

**Table 6-9. PSC0 Default Module Configuration**

| LPSC Number | Module Name | Power Domain | Default Module State | Auto Sleep/Wake Only |
|---|---|---|---|---|
| 0 | EDMA3 Channel Controller 0 | AlwaysON (PD0) | SwRstDisable | — |
| 1 | EDMA3 Transfer Controller 0 | AlwaysON (PD0) | SwRstDisable | — |
| 2 | EDMA3 Transfer Controller 1 | AlwaysON (PD0) | SwRstDisable | — |
| 3 | EMIFA (Br7) | AlwaysON (PD0) | SwRstDisable | — |
| 4 | — | — | — | — |
| 5 | — | — | — | — |
| 6 | — | — | — | — |
| 7 | — | — | — | — |
| 8 | — | — | — | — |
| 9 | UART 0 | AlwaysON (PD0) | SwRstDisable | — |
| 10 | SCR0 (Br 0, Br 1, Br 2, Br 8) | AlwaysON (PD0) | Enable | Yes |
| 11 | SCR1 (Br 4) | AlwaysON (PD0) | Enable | Yes |
| 12 | SCR2 (Br 3, Br 5, Br 6) | AlwaysON (PD0) | Enable | Yes |
| 13 | — | — | — | — |
| 14 | — | — | — | — |
| 15 | DSP | PD_DSP (PD1) | Enable | — |

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**Table 6-10. PSC1 Default Module Configuration**

| LPSC Number | Module Name | Power Domain | Default Module State | Auto Sleep/Wake Only |
|---|---|---|---|---|
| 0 | EDMA3 Channel Controller 1 | AlwaysON (PD0) | SwRstDisable | — |
| 1 | — | — | — | — |
| 2 | — | — | — | — |
| 3 | GPIO | AlwaysON (PD0) | SwRstDisable | — |
| 4 | UHPI | AlwaysON (PD0) | SwRstDisable | — |
| 5 | — | — | — | — |
| 6 | DDR2 (and SCR_F3) | AlwaysON (PD0) | SwRstDisable | — |
| 7 | McASP0 ( + McASP0 FIFO) | AlwaysON (PD0) | SwRstDisable | — |
| 8 | — | — | — | — |
| 9 | — | — | — | — |
| 10 | SPI 1 | AlwaysON (PD0) | SwRstDisable | — |
| 11 | — | — | — | — |
| 12 | — | — | — | — |
| 13 | — | — | — | — |
| 14 | — | — | — | — |
| 15 | McBSP1 ( + McBSP1 FIFO) | AlwaysON (PD0) | SwRstDisable | — |
| 16 | — | — | — | — |
| 17 | eHRPWM0/1 | AlwaysON (PD0) | SwRstDisable | — |
| 18 | — | — | — | — |
| 19 | — | — | — | — |
| 20 | ECAP0/1/2 | AlwaysON (PD0) | SwRstDisable | — |
| 21 | EDMA3 Transfer Controller 2 | AlwaysON (PD0) | SwRstDisable | — |
| 22 | — | — | — | — |
| 23 | — | — | — | — |
| 24 | SCR_F0 (and bridge F0) | AlwaysON (PD0) | Enable | Yes |
| 25 | SCR_F1 (and bridge F1) | AlwaysON (PD0) | Enable | Yes |
| 26 | SCR_F2 (and bridge F2) | AlwaysON (PD0) | Enable | Yes |
| 27 | SCR_F6 (and bridge F3) | AlwaysON (PD0) | Enable | Yes |
| 28 | SCR_F7 (and bridge F4) | AlwaysON (PD0) | Enable | Yes |
| 29 | SCR_F8 (and bridge F5) | AlwaysON (PD0) | Enable | Yes |
| 30 | Bridge F7 (DDR Controller path) | AlwaysON (PD0) | Enable | Yes |
| 31 | — | — | — | — |


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#### 6.8.1.1 Power Domain States

A power domain can only be in one of the two states: ON or OFF, defined as follows:

- ON: power to the domain is on
- OFF: power to the domain is off

For both PSC0 and PSC1, the Always ON domain, or PD0 power domain, is always in the ON state when the chip is powered-on. This domain is not programmable to OFF state.

- On PSC0 PD1/PD_DSP Domain: Controls the sleep state for DSP L1 and L2 Memories

#### 6.8.1.2 Module States

The PSC defines several possible states for a module. This states are essentially a combination of the module reset asserted or de-asserted and module clock on/enabled or off/disabled. The module states are defined in Table 6-11.

**Table 6-11. Module States**

| Module State | Module Reset | Module Clock | Module State Definition |
|---|---|---|---|
| Enable | De-asserted | On | A module in the enable state has its module reset de-asserted and it has its clock on. This is the normal operational state for a given module |
| Disable | De-asserted | Off | A module in the disabled state has its module reset de-asserted and it has its module clock off. This state is typically used for disabling a module clock to save power. The device is designed in full static CMOS, so when you stop a module clock, it retains the module's state. When the clock is restarted, the module resumes operating from the stopping point. |
| SyncReset | Asserted | On | A module state in the SyncReset state has its module reset asserted and it has its clock on. Generally, software is not expected to initiate this state |
| SwRstDisable | Asserted | Off | A module in the SwResetDisable state has its module reset asserted and it has its clock disabled. After initial power-on, several modules come up in the SwRstDisable state. Generally, software is not expected to initiate this state |
| Auto Sleep | De-asserted | Off | A module in the Auto Sleep state also has its module reset de-asserted and its module clock disabled, similar to the Disable state. However this is a special state, once a module is configured in this state by software, it can "automatically" transition to "Enable" state whenever there is an internal read/write request made to it, and after servicing the request it will "automatically" transition into the sleep state (with module reset re de-asserted and module clock disabled), without any software intervention. The transition from sleep to enabled and back to sleep state has some cycle latency associated with it. It is not envisioned to use this mode when peripherals are fully operational and moving data. |
| Auto Wake | De-asserted | Off | A module in the Auto Wake state also has its module reset de-asserted and its module clock disabled, similar to the Disable state. However this is a special state, once a module is configured in this state by software, it will "automatically" transition to "Enable" state whenever there is an internal read/write request made to it, and will remain in the "Enabled" state from then on (with module reset re de-asserted and module clock on), without any software intervention. The transition from sleep to enabled state has some cycle latency associated with it. It is not envisioned to use this mode when peripherals are fully operational and moving data. |

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## 6.9 Enhanced Direct Memory Access Controller (EDMA3)

The EDMA3 controller handles all data transfers between memories and the device slave peripherals on the device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

### *6.9.1 EDMA3 Channel Synchronization Events*

Each EDMA3 channel controller supports up to 32 channels which service peripherals and memory. Table 6-12 lists the source of the EDMA3 synchronization events associated with each of the programmable EDMA channels.

**Table 6-12. EDMA Synchronization Events**

| EDMA3 Channel Controller 0 | | | |
|---|---|---|---|
| **Event** | **Event Name / Source** | **Event** | **Event Name / Source** |
| 0 | McASP0 Receive | 16 | Reserved |
| 1 | McASP0 Transmit | 17 | Reserved |
| 2 | Reserved | 18 | SPI1 Receive |
| 3 | Reserved | 19 | SPI1 Transmit |
| 4 | McBSP1 Receive | 20 | Reserved |
| 5 | McBSP1 Transmit | 21 | Reserved |
| 6 | GPIO Bank 0 Interrupt | 22 | GPIO Bank 2 Interrupt |
| 7 | GPIO Bank 1 Interrupt | 23 | GPIO Bank 3 Interrupt |
| 8 | UART0 Receive | 24 | I2C0 Receive |
| 9 | UART0 Transmit | 25 | I2C0 Transmit |
| 10 | Timer64P0 Event Out 12 | 26 | Reserved |
| 11 | Timer64P0 Event Out 34 | 27 | Reserved |
| 12 | Reserved | 28 | GPIO Bank 4 Interrupt |
| 13 | Reserved | 29 | GPIO Bank 5 Interrupt |
| 14-15 | Reserved | 30-31 | Reserved |
| **EDMA3 Channel Controller 1** | | | |
| Event | Event Name / Source | Event | Event Name / Source |
| 0 | Reserved | 16 | GPIO Bank 6 Interrupt |
| 1 | Reserved | 17 | GPIO Bank 7 Interrupt |
| 2 | Reserved | 18 | GPIO Bank 8 Interrupt |
| 3-15 | Reserved | 19-31 | Reserved |


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### 6.9.2 EDMA3 Peripheral Register Descriptions

Table 6-13 is the list of EDMA3 Channel Controller Registers and Table 6-14 is the list of EDMA3 Transfer Controller registers.

**Table 6-13. EDMA3 Channel Controller (EDMA3CC) Registers**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS | EDMA3_1 Channel Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C0 0000 | 0x01E3 0000 | PID | Peripheral Identification Register |
| 0x01C0 0004 | 0x01E3 0004 | CCCFG | EDMA3CC Configuration Register |
| **Global Registers** | | | |
| 0x01C0 0200 | 0x01E3 0200 | QCHMAP0 | QDMA Channel 0 Mapping Register |
| 0x01C0 0204 | 0x01E3 0204 | QCHMAP1 | QDMA Channel 1 Mapping Register |
| 0x01C0 0208 | 0x01E3 0208 | QCHMAP2 | QDMA Channel 2 Mapping Register |
| 0x01C0 020C | 0x01E3 020C | QCHMAP3 | QDMA Channel 3 Mapping Register |
| 0x01C0 0210 | 0x01E3 0210 | QCHMAP4 | QDMA Channel 4 Mapping Register |
| 0x01C0 0214 | 0x01E3 0214 | QCHMAP5 | QDMA Channel 5 Mapping Register |
| 0x01C0 0218 | 0x01E3 0218 | QCHMAP6 | QDMA Channel 6 Mapping Register |
| 0x01C0 021C | 0x01E3 021C | QCHMAP7 | QDMA Channel 7 Mapping Register |
| 0x01C0 0240 | 0x01E3 0240 | DMAQNUM0 | DMA Channel Queue Number Register 0 |
| 0x01C0 0244 | 0x01E3 0244 | DMAQNUM1 | DMA Channel Queue Number Register 1 |
| 0x01C0 0248 | 0x01E3 0248 | DMAQNUM2 | DMA Channel Queue Number Register 2 |
| 0x01C0 024C | 0x01E3 024C | DMAQNUM3 | DMA Channel Queue Number Register 3 |
| 0x01C0 0260 | 0x01E3 0260 | QDMAQNUM | QDMA Channel Queue Number Register |
| 0x01C0 0284 | 0x01E3 0284 | QUEPRI | Queue Priority Register(1) |
| 0x01C0 0300 | 0x01E3 0300 | EMR | Event Missed Register |
| 0x01C0 0308 | 0x01E3 0308 | EMCR | Event Missed Clear Register |
| 0x01C0 0310 | 0x01E3 0310 | QEMR | QDMA Event Missed Register |
| 0x01C0 0314 | 0x01E3 0314 | QEMCR | QDMA Event Missed Clear Register |
| 0x01C0 0318 | 0x01E3 0318 | CCERR | EDMA3CC Error Register |
| 0x01C0 031C | 0x01E3 031C | CCERRCLR | EDMA3CC Error Clear Register |
| 0x01C0 0320 | 0x01E3 0320 | EEVAL | Error Evaluate Register |
| 0x01C0 0340 | 0x01E3 0340 | DRAE0 | DMA Region Access Enable Register for Region 0 |
| 0x01C0 0348 | 0x01E3 0348 | DRAE1 | DMA Region Access Enable Register for Region 1 |
| 0x01C0 0350 | 0x01E3 0350 | DRAE2 | DMA Region Access Enable Register for Region 2 |
| 0x01C0 0358 | 0x01E3 0358 | DRAE3 | DMA Region Access Enable Register for Region 3 |
| 0x01C0 0380 | 0x01E3 0380 | QRAE0 | QDMA Region Access Enable Register for Region 0 |
| 0x01C0 0384 | 0x01E3 0384 | QRAE1 | QDMA Region Access Enable Register for Region 1 |
| 0x01C0 0388 | 0x01E3 0388 | QRAE2 | QDMA Region Access Enable Register for Region 2 |
| 0x01C0 038C | 0x01E3 038C | QRAE3 | QDMA Region Access Enable Register for Region 3 |
| 0x01C0 0400 - 0x01C0 043C | 0x01E3 0400 - 0x01E3 043C | Q0E0-Q0E15 | Event Queue Entry Registers Q0E0-Q0E15 |
| 0x01C0 0440 - 0x01C0 047C | 0x01E3 0440 - 0x01E3 047C | Q1E0-Q1E15 | Event Queue Entry Registers Q1E0-Q1E15 |
| 0x01C0 0600 | 0x01E3 0600 | QSTAT0 | Queue 0 Status Register |
| 0x01C0 0604 | 0x01E3 0604 | QSTAT1 | Queue 1 Status Register |
| 0x01C0 0620 | 0x01E3 0620 | QWMTHRA | Queue Watermark Threshold A Register |
| 0x01C0 0640 | 0x01E3 0640 | CCSTAT | EDMA3CC Status Register |

(1) On previous architectures, the EDMA3TC priority was controlled by the queue priority register (QUEPRI) in the EDMA3CC memory-map. However for this device, the priority control for the transfer controllers is controlled by the chip-level registers in the System Configuration Module. You should use the chip-level registers and not QUEPRI to configure the TC priority.

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**Table 6-13. EDMA3 Channel Controller (EDMA3CC) Registers (continued)**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS | EDMA3_1 Channel Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| **Global Channel Registers** | | | |
| 0x01C0 1000 | 0x01E3 1000 | ER | Event Register |
| 0x01C0 1008 | 0x01E3 1008 | ECR | Event Clear Register |
| 0x01C0 1010 | 0x01E3 1010 | ESR | Event Set Register |
| 0x01C0 1018 | 0x01E3 1018 | CER | Chained Event Register |
| 0x01C0 1020 | 0x01E3 1020 | EER | Event Enable Register |
| 0x01C0 1028 | 0x01E3 1028 | EECR | Event Enable Clear Register |
| 0x01C0 1030 | 0x01E3 1030 | EESR | Event Enable Set Register |
| 0x01C0 1038 | 0x01E3 1038 | SER | Secondary Event Register |
| 0x01C0 1040 | 0x01E3 1040 | SECR | Secondary Event Clear Register |
| 0x01C0 1050 | 0x01E3 1050 | IER | Interrupt Enable Register |
| 0x01C0 1058 | 0x01E3 1058 | IECR | Interrupt Enable Clear Register |
| 0x01C0 1060 | 0x01E3 1060 | IESR | Interrupt Enable Set Register |
| 0x01C0 1068 | 0x01E3 1068 | IPR | Interrupt Pending Register |
| 0x01C0 1070 | 0x01E3 1070 | ICR | Interrupt Clear Register |
| 0x01C0 1078 | 0x01E3 1078 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 1080 | 0x01E3 1080 | QER | QDMA Event Register |
| 0x01C0 1084 | 0x01E3 1084 | QEER | QDMA Event Enable Register |
| 0x01C0 1088 | 0x01E3 1088 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 108C | 0x01E3 108C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 1090 | 0x01E3 1090 | QSER | QDMA Secondary Event Register |
| 0x01C0 1094 | 0x01E3 1094 | QSECR | QDMA Secondary Event Clear Register |
| **Shadow Region 0 Channel Registers** | | | |
| 0x01C0 2000 | 0x01E3 2000 | ER | Event Register |
| 0x01C0 2008 | 0x01E3 2008 | ECR | Event Clear Register |
| 0x01C0 2010 | 0x01E3 2010 | ESR | Event Set Register |
| 0x01C0 2018 | 0x01E3 2018 | CER | Chained Event Register |
| 0x01C0 2020 | 0x01E3 2020 | EER | Event Enable Register |
| 0x01C0 2028 | 0x01E3 2028 | EECR | Event Enable Clear Register |
| 0x01C0 2030 | 0x01E3 2030 | EESR | Event Enable Set Register |
| 0x01C0 2038 | 0x01E3 2038 | SER | Secondary Event Register |
| 0x01C0 2040 | 0x01E3 2040 | SECR | Secondary Event Clear Register |
| 0x01C0 2050 | 0x01E3 2050 | IER | Interrupt Enable Register |
| 0x01C0 2058 | 0x01E3 2058 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2060 | 0x01E3 2060 | IESR | Interrupt Enable Set Register |
| 0x01C0 2068 | 0x01E3 2068 | IPR | Interrupt Pending Register |
| 0x01C0 2070 | 0x01E3 2070 | ICR | Interrupt Clear Register |
| 0x01C0 2078 | 0x01E3 2078 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2080 | 0x01E3 2080 | QER | QDMA Event Register |
| 0x01C0 2084 | 0x01E3 2084 | QEER | QDMA Event Enable Register |
| 0x01C0 2088 | 0x01E3 2088 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 208C | 0x01E3 208C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2090 | 0x01E3 2090 | QSER | QDMA Secondary Event Register |
| 0x01C0 2094 | 0x01E3 2094 | QSECR | QDMA Secondary Event Clear Register |


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**Table 6-13. EDMA3 Channel Controller (EDMA3CC) Registers (continued)**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS | EDMA3_1 Channel Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| **Shadow Region 1 Channel Registers** | | | |
| 0x01C0 2200 | 0x01E3 2200 | ER | Event Register |
| 0x01C0 2208 | 0x01E3 2208 | ECR | Event Clear Register |
| 0x01C0 2210 | 0x01E3 2210 | ESR | Event Set Register |
| 0x01C0 2218 | 0x01E3 2218 | CER | Chained Event Register |
| 0x01C0 2220 | 0x01E3 2220 | EER | Event Enable Register |
| 0x01C0 2228 | 0x01E3 2228 | EECR | Event Enable Clear Register |
| 0x01C0 2230 | 0x01E3 2230 | EESR | Event Enable Set Register |
| 0x01C0 2238 | 0x01E3 2238 | SER | Secondary Event Register |
| 0x01C0 2240 | 0x01E3 2240 | SECR | Secondary Event Clear Register |
| 0x01C0 2250 | 0x01E3 2250 | IER | Interrupt Enable Register |
| 0x01C0 2258 | 0x01E3 2258 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2260 | 0x01E3 2260 | IESR | Interrupt Enable Set Register |
| 0x01C0 2268 | 0x01E3 2268 | IPR | Interrupt Pending Register |
| 0x01C0 2270 | 0x01E3 2270 | ICR | Interrupt Clear Register |
| 0x01C0 2278 | 0x01E3 2278 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2280 | 0x01E3 2280 | QER | QDMA Event Register |
| 0x01C0 2284 | 0x01E3 2284 | QEER | QDMA Event Enable Register |
| 0x01C0 2288 | 0x01E3 2288 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 228C | 0x01E3 228C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2290 | 0x01E3 2290 | QSER | QDMA Secondary Event Register |
| 0x01C0 2294 | 0x01E3 2294 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 4000 - 0x01C0 4FFF | 0x01E3 4000 - 0x01E3 4FFF | — | Parameter RAM (PaRAM) |

**Table 6-14. EDMA3 Transfer Controller (EDMA3TC) Registers**

| EDMA3_0 Transfer Controller 0 BYTE ADDRESS | EDMA3_0 Transfer Controller 1 BYTE ADDRESS | EDMA3_1 Transfer Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|---|
| 0x01C0 8000 | 0x01C0 8400 | 0x01E3 8000 | PID | Peripheral Identification Register |
| 0x01C0 8004 | 0x01C0 8404 | 0x01E3 8004 | TCCFG | EDMA3TC Configuration Register |
| 0x01C0 8100 | 0x01C0 8500 | 0x01E3 8100 | TCSTAT | EDMA3TC Channel Status Register |
| 0x01C0 8120 | 0x01C0 8520 | 0x01E3 8120 | ERRSTAT | Error Status Register |
| 0x01C0 8124 | 0x01C0 8524 | 0x01E3 8124 | ERREN | Error Enable Register |
| 0x01C0 8128 | 0x01C0 8528 | 0x01E3 8128 | ERRCLR | Error Clear Register |
| 0x01C0 812C | 0x01C0 852C | 0x01E3 812C | ERRDET | Error Details Register |
| 0x01C0 8130 | 0x01C0 8530 | 0x01E3 8130 | ERRCMD | Error Interrupt Command Register |
| 0x01C0 8140 | 0x01C0 8540 | 0x01E3 8140 | RDRATE | Read Command Rate Register |
| 0x01C0 8240 | 0x01C0 8640 | 0x01E3 8240 | SAOPT | Source Active Options Register |
| 0x01C0 8244 | 0x01C0 8644 | 0x01E3 8244 | SASRC | Source Active Source Address Register |
| 0x01C0 8248 | 0x01C0 8648 | 0x01E3 8248 | SACNT | Source Active Count Register |
| 0x01C0 824C | 0x01C0 864C | 0x01E3 824C | SADST | Source Active Destination Address Register |
| 0x01C0 8250 | 0x01C0 8650 | 0x01E3 8250 | SABIDX | Source Active B-Index Register |
| 0x01C0 8254 | 0x01C0 8654 | 0x01E3 8254 | SAMPPRXY | Source Active Memory Protection Proxy Register |
| 0x01C0 8258 | 0x01C0 8658 | 0x01E3 8258 | SACNTRLD | Source Active Count Reload Register |
| 0x01C0 825C | 0x01C0 865C | 0x01E3 825C | SASRCBREF | Source Active Source Address B-Reference Register |
| 0x01C0 8260 | 0x01C0 8660 | 0x01E3 8260 | SADSTBREF | Source Active Destination Address B-Reference Register |

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**Table 6-14. EDMA3 Transfer Controller (EDMA3TC) Registers (continued)**

| EDMA3_0 Transfer Controller 0 BYTE ADDRESS | EDMA3_0 Transfer Controller 1 BYTE ADDRESS | EDMA3_1 Transfer Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|---|
| 0x01C0 8280 | 0x01C0 8680 | 0x01E3 8280 | DFCNTRLD | Destination FIFO Set Count Reload Register |
| 0x01C0 8284 | 0x01C0 8684 | 0x01E3 8284 | DFSRCBREF | Destination FIFO Set Source Address B-Reference Register |
| 0x01C0 8288 | 0x01C0 8688 | 0x01E3 8288 | DFDSTBREF | Destination FIFO Set Destination Address B-Reference Register |
| 0x01C0 8300 | 0x01C0 8700 | 0x01E3 8300 | DFOPT0 | Destination FIFO Options Register 0 |
| 0x01C0 8304 | 0x01C0 8704 | 0x01E3 8304 | DFSRC0 | Destination FIFO Source Address Register 0 |
| 0x01C0 8308 | 0x01C0 8708 | 0x01E3 8308 | DFCNT0 | Destination FIFO Count Register 0 |
| 0x01C0 830C | 0x01C0 870C | 0x01E3 830C | DFDST0 | Destination FIFO Destination Address Register 0 |
| 0x01C0 8310 | 0x01C0 8710 | 0x01E3 8310 | DFBIDX0 | Destination FIFO B-Index Register 0 |
| 0x01C0 8314 | 0x01C0 8714 | 0x01E3 8314 | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0 |
| 0x01C0 8340 | 0x01C0 8740 | 0x01E3 8340 | DFOPT1 | Destination FIFO Options Register 1 |
| 0x01C0 8344 | 0x01C0 8744 | 0x01E3 8344 | DFSRC1 | Destination FIFO Source Address Register 1 |
| 0x01C0 8348 | 0x01C0 8748 | 0x01E3 8348 | DFCNT1 | Destination FIFO Count Register 1 |
| 0x01C0 834C | 0x01C0 874C | 0x01E3 834C | DFDST1 | Destination FIFO Destination Address Register 1 |
| 0x01C0 8350 | 0x01C0 8750 | 0x01E3 8350 | DFBIDX1 | Destination FIFO B-Index Register 1 |
| 0x01C0 8354 | 0x01C0 8754 | 0x01E3 8354 | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1 |
| 0x01C0 8380 | 0x01C0 8780 | 0x01E3 8380 | DFOPT2 | Destination FIFO Options Register 2 |
| 0x01C0 8384 | 0x01C0 8784 | 0x01E3 8384 | DFSRC2 | Destination FIFO Source Address Register 2 |
| 0x01C0 8388 | 0x01C0 8788 | 0x01E3 8388 | DFCNT2 | Destination FIFO Count Register 2 |
| 0x01C0 838C | 0x01C0 878C | 0x01E3 838C | DFDST2 | Destination FIFO Destination Address Register 2 |
| 0x01C0 8390 | 0x01C0 8790 | 0x01E3 8390 | DFBIDX2 | Destination FIFO B-Index Register 2 |
| 0x01C0 8394 | 0x01C0 8794 | 0x01E3 8394 | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2 |
| 0x01C0 83C0 | 0x01C0 87C0 | 0x01E3 83C0 | DFOPT3 | Destination FIFO Options Register 3 |
| 0x01C0 83C4 | 0x01C0 87C4 | 0x01E3 83C4 | DFSRC3 | Destination FIFO Source Address Register 3 |
| 0x01C0 83C8 | 0x01C0 87C8 | 0x01E3 83C8 | DFCNT3 | Destination FIFO Count Register 3 |
| 0x01C0 83CC | 0x01C0 87CC | 0x01E3 83CC | DFDST3 | Destination FIFO Destination Address Register 3 |
| 0x01C0 83D0 | 0x01C0 87D0 | 0x01E3 83D0 | DFBIDX3 | Destination FIFO B-Index Register 3 |
| 0x01C0 83D4 | 0x01C0 87D4 | 0x01E3 83D4 | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3 |

Table 6-15 shows an abbreviation of the set of registers which make up the parameter set for each of 128 EDMA3 events. Each of the parameter register sets consist of 8 32-bit word entries. Table 6-16 shows the parameter set entry registers with relative memory address locations within each of the parameter sets.

**Table 6-15. EDMA3 Parameter Set RAM**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS RANGE | EDMA3_1 Channel Controller 0 BYTE ADDRESS RANGE | DESCRIPTION |
|---|---|---|
| 0x01C0 4000 - 0x01C0 401F | 0x01E3 4000 - 0x01E3 401F | Parameters Set 0 (8 32-bit words) |
| 0x01C0 4020 - 0x01C0 403F | 0x01E3 4020 - 0x01E3 403F | Parameters Set 1 (8 32-bit words) |
| 0x01C0 4040 - 0x01CC0 405F | 0x01E3 4040 - 0x01CE3 405F | Parameters Set 2 (8 32-bit words) |
| 0x01C0 4060 - 0x01C0 407F | 0x01E3 4060 - 0x01E3 407F | Parameters Set 3 (8 32-bit words) |
| 0x01C0 4080 - 0x01C0 409F | 0x01E3 4080 - 0x01E3 409F | Parameters Set 4 (8 32-bit words) |
| 0x01C0 40A0 - 0x01C0 40BF | 0x01E3 40A0 - 0x01E3 40BF | Parameters Set 5 (8 32-bit words) |
| ... | ... | ... |
| 0x01C0 4FC0 - 0x01C0 4FDF | 0x01E3 4FC0 - 0x01E3 4FDF | Parameters Set 126 (8 32-bit words) |
| 0x01C0 4FE0 - 0x01C0 4FFF | 0x01E3 4FE0 - 0x01E3 4FFF | Parameters Set 127 (8 32-bit words) |


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**Table 6-16. Parameter Set Entries**

| OFFSET BYTE ADDRESS WITHIN THE PARAMETER SET | ACRONYM | PARAMETER ENTRY |
|---|---|---|
| 0x0000 | OPT | Option |
| 0x0004 | SRC | Source Address |
| 0x0008 | A_B_CNT | A Count, B Count |
| 0x000C | DST | Destination Address |
| 0x0010 | SRC_DST_BIDX | Source B Index, Destination B Index |
| 0x0014 | LINK_BCNTRLD | Link Address, B Count Reload |
| 0x0018 | SRC_DST_CIDX | Source C Index, Destination C Index |
| 0x001C | CCNT | C Count |

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## 6.10 External Memory Interface A (EMIFA)

EMIFA is one of two external memory interfaces supported on the device. It is primarily intended to support asynchronous memory types, such as NAND and NOR flash and Asynchronous SRAM. However on this device, EMIFA also provides a secondary interface to SDRAM.

### *6.10.1 EMIFA Asynchronous Memory Support*

EMIFA supports asynchronous:

- SRAM memories
- NAND Flash memories
- NOR Flash memories

The EMIFA data bus width is up to 16-bits.The device supports up to 23 address lines and two external wait/interrupt inputs. Up to four asynchronous chip selects are supported by EMIFA ($\overline{\text{EMA_CS[5:2]}}$).

Each chip select has the following individually programmable attributes:

- Data Bus Width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Extended Wait Option With Programmable Timeout
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes.

### *6.10.2 EMIFA Synchronous DRAM Memory Support*

The device supports 16-bit SDRAM in addition to the asynchronous memories listed in Section 6.10.1. It has a single SDRAM chip select (EMA_CS[0]). SDRAM configurations that are supported are:

- One, Two, and Four Bank SDRAM devices
- Devices with Eight, Nine, Ten, and Eleven Column Address
- CAS Latency of two or three clock cycles
- Sixteen Bit Data Bus Width

Additionally, the SDRAM interface of EMIFA supports placing the SDRAM in Self Refresh and Powerdown Modes. Self Refresh mode allows the SDRAM to be put into a low power state while still retaining memory contents; since the SDRAM will continue to refresh itself even without clocks from the device. Powerdown mode achieves even lower power, except the device must periodically wake the SDRAM up and issue refreshes if data retention is required.

Finally, note that the EMIFA does not support Mobile SDRAM devices.

Table 6-17 shows the supported SDRAM configurations for EMIFA.


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**Table 6-17. EMIFA Supported SDRAM Configurations(1)**

| SDRAM Memory Data Bus Width (bits) | Number of Memories | EMIFA Data Bus Size (bits) | Rows | Columns | Banks | Total Memory (Mbits) | Total Memory (Mbytes) | Memory Density (Mbits) |
|---|---|---|---|---|---|---|---|---|
| 16 | 1 | 16 | 16 | 8 | 1 | 256 | 32 | 256 |
| | 1 | 16 | 16 | 8 | 2 | 512 | 64 | 512 |
| | 1 | 16 | 16 | 8 | 4 | 1024 | 128 | 1024 |
| | 1 | 16 | 16 | 9 | 1 | 512 | 64 | 512 |
| | 1 | 16 | 16 | 9 | 2 | 1024 | 128 | 1024 |
| | 1 | 16 | 16 | 9 | 4 | 2048 | 256 | 2048 |
| | 1 | 16 | 16 | 10 | 1 | 1024 | 128 | 1024 |
| | 1 | 16 | 16 | 10 | 2 | 2048 | 256 | 2048 |
| | 1 | 16 | 16 | 10 | 4 | 4096 | 512 | 4096 |
| | 1 | 16 | 16 | 11 | 1 | 2048 | 256 | 2048 |
| | 1 | 16 | 16 | 11 | 2 | 4096 | 512 | 4096 |
| | 1 | 16 | 15 | 11 | 4 | 4096 | 512 | 4096 |
| 8 | 2 | 16 | 16 | 8 | 1 | 256 | 32 | 128 |
| | 2 | 16 | 16 | 8 | 2 | 512 | 64 | 256 |
| | 2 | 16 | 16 | 8 | 4 | 1024 | 128 | 512 |
| | 2 | 16 | 16 | 9 | 1 | 512 | 64 | 256 |
| | 2 | 16 | 16 | 9 | 2 | 1024 | 128 | 512 |
| | 2 | 16 | 16 | 9 | 4 | 2048 | 256 | 1024 |
| | 2 | 16 | 16 | 10 | 1 | 1024 | 128 | 512 |
| | 2 | 16 | 16 | 10 | 2 | 2048 | 256 | 1024 |
| | 2 | 16 | 16 | 10 | 4 | 4096 | 512 | 2048 |
| | 2 | 16 | 16 | 11 | 1 | 2048 | 256 | 1024 |
| | 2 | 16 | 16 | 11 | 2 | 4096 | 512 | 2048 |
| | 2 | 16 | 15 | 11 | 4 | 4096 | 512 | 2048 |

(1) The shaded cells indicate configurations that are possible on the EMIFA interface but as of this writing SDRAM memories capable of supporting these densities are not available in the market.

### 6.10.3 EMIFA SDRAM Loading Limitations

EMIFA supports SDRAM up to 100 MHz with up to two SDRAM or asynchronous memory loads. Additional loads will limit the SDRAM operation to lower speeds and the maximum speed should be confirmed by board simulation using IBIS models.

### 6.10.4 EMIFA Connection Examples

Figure 6-10 illustrates an example of how SDRAM, NOR, and NAND flash devices might be connected to EMIFA simultaneously. The SDRAM chip select must be EMA_CS[0]. Note that the NOR flash is connected to EMA_CS[2] and the NAND flash is connected to EMA_CS[3] in this example. Note that any type of asynchronous memory may be connected to EMA_CS[5:2].

The on-chip bootloader makes some assumptions on which chip select the contains the boot image, and this depends on the boot mode. For NOR boot mode; the on-chip bootloader requires that the image be stored in NOR flash on EMA_CS[2]. For NAND boot mode, the bootloader requires that the boot image is stored in NAND flash on EMA_CS[3]. It is always possible to have the image span multiple chip selects, but this must be supported by second stage boot code stored in the external flash.

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A likely use case with more than one EMIFA chip select used for NAND flash is illustrated in Figure 6-11. This figure shows how two multiplane NAND flash devices with two chip selects each would connect to the EMIFA. In this case if NAND is the boot memory, then the boot image needs to be stored in the NAND area selected by EMA_CS[3]. Part of the application image could spill over into the NAND regions selected by other EMIFA chip selects; but would rely on the code stored in the EMA_CS[3] area to bootload it.

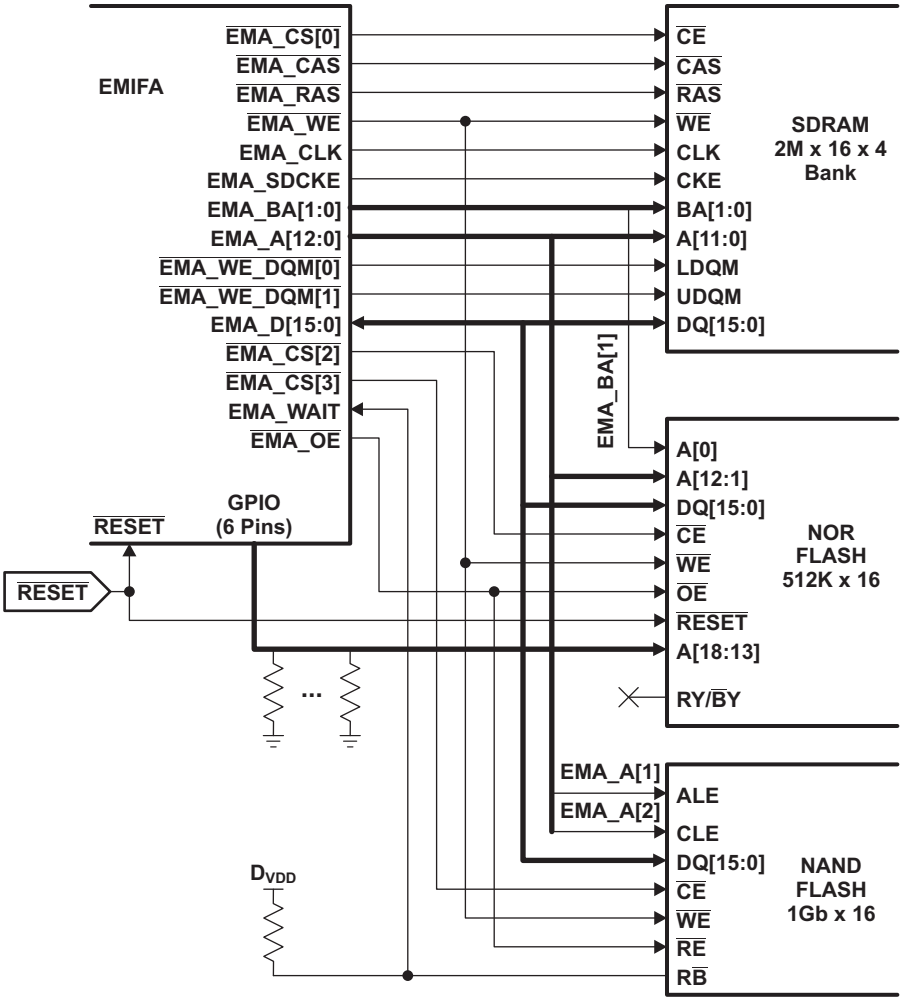



**Figure 6-10. Connection Diagram: SDRAM, NOR, NAND**


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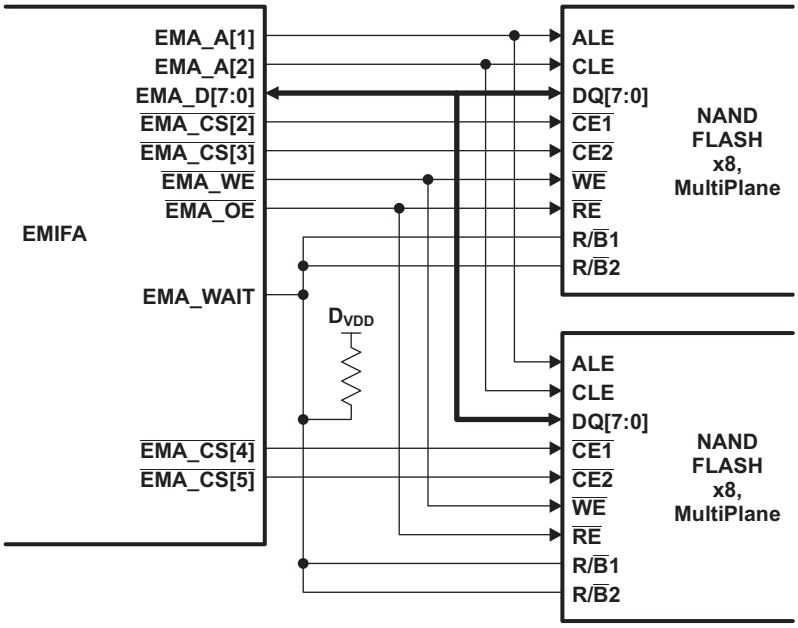



**Figure 6-11. EMIFA Connection Diagram: Multiple NAND Flash Planes**

### 6.10.5 External Memory Interface Register Descriptions

**Table 6-18. External Memory Interface (EMIFA) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x6800 0000 | MIDR | Module ID Register |
| 0x6800 0004 | AWCC | Asynchronous Wait Cycle Configuration Register |
| 0x6800 0008 | SDCR | SDRAM Configuration Register |
| 0x6800 000C | SDRCR | SDRAM Refresh Control Register |
| 0x6800 0010 | CE2CFG | Asynchronous 1 Configuration Register |
| 0x6800 0014 | CE3CFG | Asynchronous 2 Configuration Register |
| 0x6800 0018 | CE4CFG | Asynchronous 3 Configuration Register |
| 0x6800 001C | CE5CFG | Asynchronous 4 Configuration Register |
| 0x6800 0020 | SDTIMR | SDRAM Timing Register |
| 0x6800 003C | SDSRETR | SDRAM Self Refresh Exit Timing Register |
| 0x6800 0040 | INTRAW | EMIFA Interrupt Raw Register |
| 0x6800 0044 | INTMSK | EMIFA Interrupt Mask Register |
| 0x6800 0048 | INTMSKSET | EMIFA Interrupt Mask Set Register |
| 0x6800 004C | INTMSKCLR | EMIFA Interrupt Mask Clear Register |
| 0x6800 0060 | NANDFCR | NAND Flash Control Register |
| 0x6800 0064 | NANDFSR | NAND Flash Status Register |
| 0x6800 0070 | NANDF1ECC | NAND Flash 1 ECC Register (CS2 Space) |
| 0x6800 0074 | NANDF2ECC | NAND Flash 2 ECC Register (CS3 Space) |
| 0x6800 0078 | NANDF3ECC | NAND Flash 3 ECC Register (CS4 Space) |
| 0x6800 007C | NANDF4ECC | NAND Flash 4 ECC Register (CS5 Space) |
| 0x6800 00BC | NAND4BITECCLOAD | NAND Flash 4-Bit ECC Load Register |
| 0x6800 00C0 | NAND4BITECC1 | NAND Flash 4-Bit ECC Register 1 |
| 0x6800 00C4 | NAND4BITECC2 | NAND Flash 4-Bit ECC Register 2 |
| 0x6800 00C8 | NAND4BITECC3 | NAND Flash 4-Bit ECC Register 3 |
| 0x6800 00CC | NAND4BITECC4 | NAND Flash 4-Bit ECC Register 4 |
| 0x6800 00D0 | NANDERRADD1 | NAND Flash 4-Bit ECC Error Address Register 1 |
| 0x6800 00D4 | NANDERRADD2 | NAND Flash 4-Bit ECC Error Address Register 2 |
| 0x6800 00D8 | NANDERRVAL1 | NAND Flash 4-Bit ECC Error Value Register 1 |
| 0x6800 00DC | NANDERRVAL2 | NAND Flash 4-Bit ECC Error Value Register 2 |


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### 6.10.6 EMIFA Electrical Data/Timing

Table 6-19 through Table 6-22 assume testing over recommended operating conditions.

**Table 6-19. Timing Requirements for EMIFA SDRAM Interface**

| NO. | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 19 | $t_{su(EMA_DV-EM_CLKH)}$ | Input setup time, read data valid on EMA_D[15:0] before EMA_CLK rising | 2 | | 3 | | 3 | | ns |
| 20 | $t_{h(CLKH-DIV)}$ | Input hold time, read data valid on EMA_D[15:0] after EMA_CLK rising | 1.6 | | 1.6 | | 1.6 | | ns |

**Table 6-20. Switching Characteristics for EMIFA SDRAM Interface**

| NO. | PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, EMIF clock EMA_CLK | 10 | | 15 | | 20 | | ns |
| 2 | $t_{w(CLK)}$ | Pulse width, EMIF clock EMA_CLK high or low | 3 | | 5 | | 8 | | ns |
| 3 | $t_{d(CLKH-CSV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_CS[0]}$ valid | | 7 | | 9.5 | | 13 | ns |
| 4 | $t_{oh(CLKH-CSIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_CS[0]}$ invalid | 1 | | 1 | | 1 | | ns |
| 5 | $t_{d(CLKH-DQMV)}$ | Delay time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] valid | | 7 | | 9.5 | | 13 | ns |
| 6 | $t_{oh(CLKH-DQMIV)}$ | Output hold time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] invalid | 1 | | 1 | | 1 | | ns |
| 7 | $t_{d(CLKH-AV)}$ | Delay time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] valid | | 7 | | 9.5 | | 13 | ns |
| 8 | $t_{oh(CLKH-AIV)}$ | Output hold time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] invalid | 1 | | 1 | | 1 | | ns |
| 9 | $t_{d(CLKH-DV)}$ | Delay time, EMA_CLK rising to EMA_D[15:0] valid | | 7 | | 9.5 | | 13 | ns |
| 10 | $t_{oh(CLKH-DIV)}$ | Output hold time, EMA_CLK rising to EMA_D[15:0] invalid | 1 | | 1 | | 1 | | ns |
| 11 | $t_{d(CLKH-RASV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_RAS}$ valid | | 7 | | 9.5 | | 13 | ns |
| 12 | $t_{oh(CLKH-RASIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_RAS}$ invalid | 1 | | 1 | | 1 | | ns |
| 13 | $t_{d(CLKH-CASV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_CAS}$ valid | | 7 | | 9.5 | | 13 | ns |
| 14 | $t_{oh(CLKH-CASIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_CAS}$ invalid | 1 | | 1 | | 1 | | ns |
| 15 | $t_{d(CLKH-WEV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_WE}$ valid | | 7 | | 9.5 | | 13 | ns |
| 16 | $t_{oh(CLKH-WEIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_WE}$ invalid | 1 | | 1 | | 1 | | ns |
| 17 | $t_{dis(CLKH-DHZ)}$ | Delay time, EMA_CLK rising to EMA_D[15:0] tri-stated | | 7 | | 9.5 | | 13 | ns |
| 18 | $t_{ena(CLKH-DLZ)}$ | Output hold time, EMA_CLK rising to EMA_D[15:0] driving | 1 | | 1 | | 1 | | ns |

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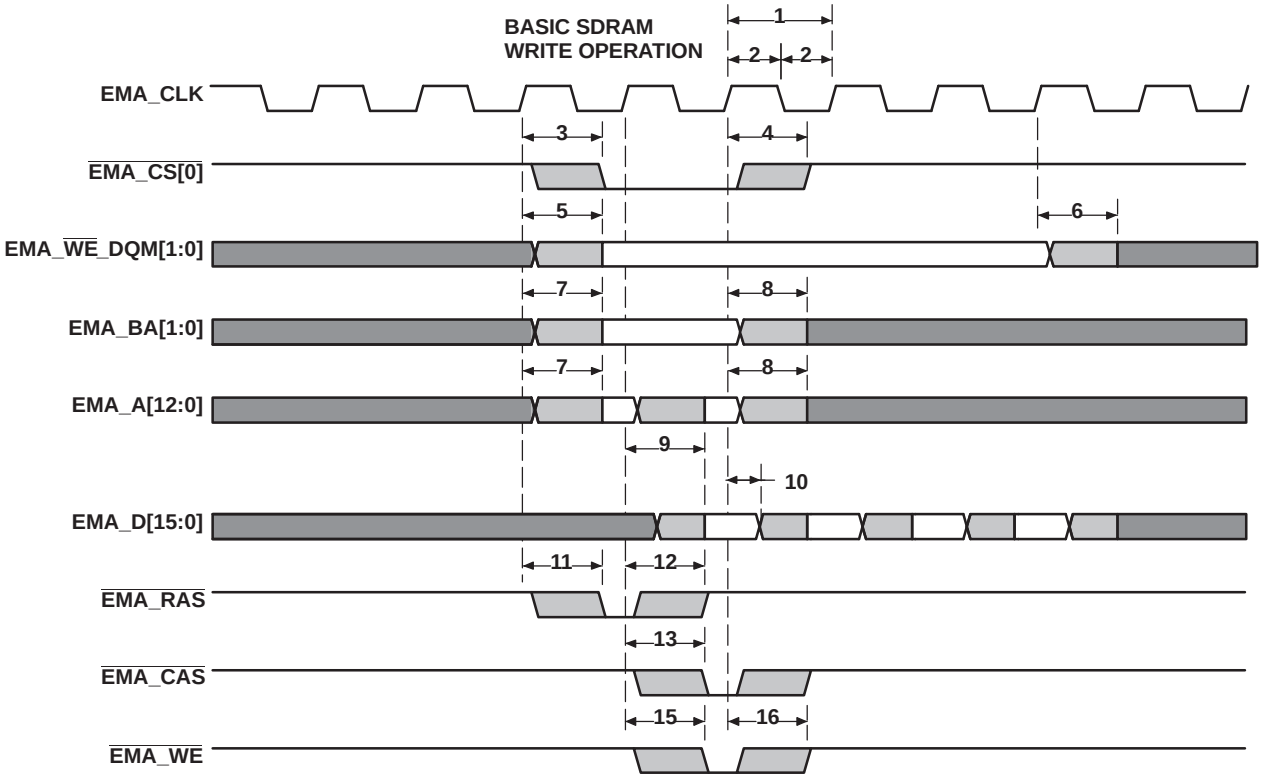



**Figure 6-12. EMIFA Basic SDRAM Write Operation**

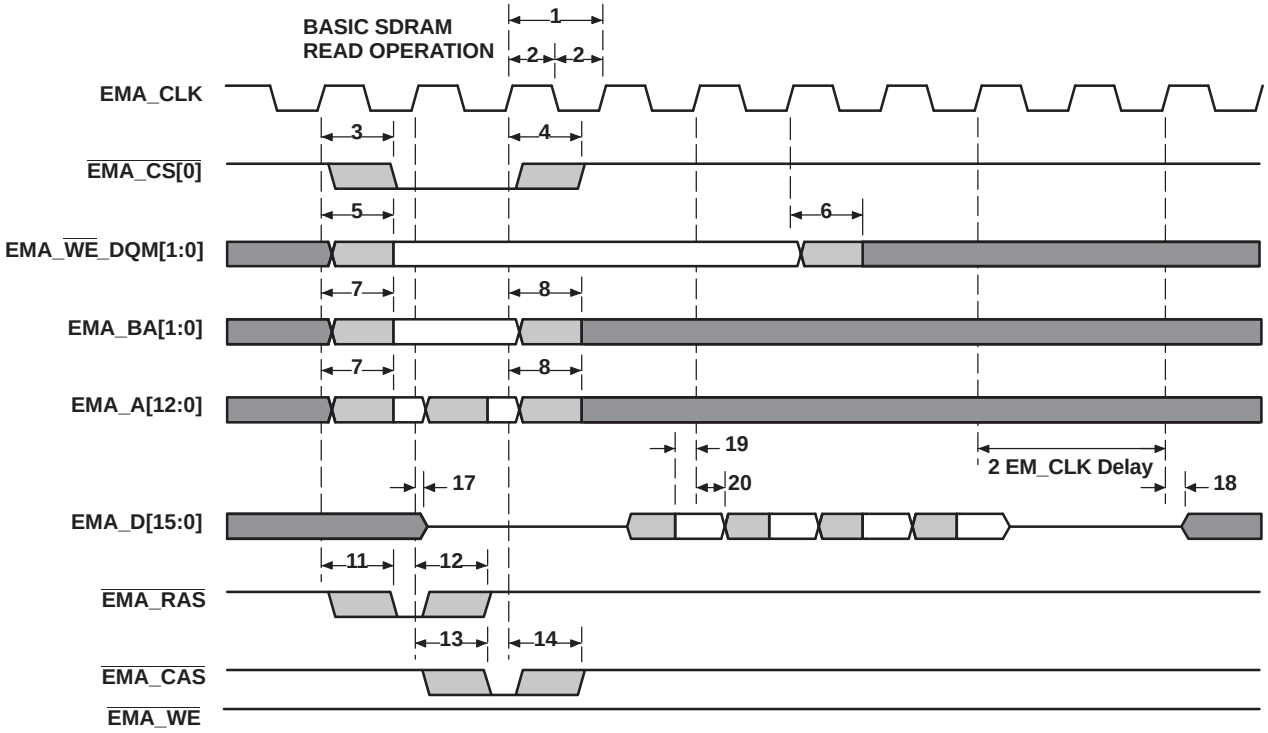



**Figure 6-13. EMIFA Basic SDRAM Read Operation**


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**Table 6-21. Timing Requirements for EMIFA Asynchronous Memory Interface (1)**

| NO. | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **READS and WRITES** | | | | | | | | | |
| E | $t_{c(CLK)}$ | Cycle time, EMIFA module clock | 6.75 | | 13.33 | | 20 | | ns |
| 2 | $t_{w(EM_WAIT)}$ | Pulse duration, EM_WAIT assertion and deassertion | 2E | | 2E | | 2E | | ns |
| **READS** | | | | | | | | | |
| 12 | $t_{su(EMDV-EMOEH)}$ | Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high | 3 | | 5 | | 7 | | ns |
| 13 | $t_{h(EMOEH-EMDIV)}$ | Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high | 0 | | 0 | | 0 | | ns |
| 14 | $t_{su\ (EMOEL-EMWAIT)}$ | Setup Time, EM_WAIT asserted before end of Strobe Phase (2) | 4E+3 | | 4E+3 | | 4E+3 | | ns |
| **WRITES** | | | | | | | | | |
| 28 | $t_{su\ (EMWEL-EMWAIT)}$ | Setup Time, EM_WAIT asserted before end of Strobe Phase (2) | 4E+3 | | 4E+3 | | 4E+3 | | ns |

(1) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL0 output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns

(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAIT must be asserted to add extended wait states. Figure 6-16 and Figure 6-17 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

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## Table 6-22. Switching Characteristics for EMIFA Asynchronous Memory Interface (1) (2) (3)

| NO. | PARAMETER | | 1.2V, 1.1V, 1.0V | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | Nom | MAX | |
| **READS and WRITES** | | | | | | |
| 1 | $t_{d(TURNAROUND)}$ | Turn around time | (TA)*E - 3 | (TA)*E | (TA)*E + 3 | ns |
| **READS** | | | | | | |
| 3 | $t_{c(EMRCYCLE)}$ | EMIF read cycle time (EW = 0) | (RS+RST+RH)*E - 3 | (RS+RST+RH)*E | (RS+RST+RH)*E + 3 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+EWC)*E - 3 | (RS+RST+RH+EWC)*E | (RS+RST+RH+EWC)*E + 3 | ns |
| 4 | $t_{su(EMCEL-EMOEL)}$ | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS = 0) | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| | | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS = 1) | -3 | 0 | +3 | ns |
| 5 | $t_{h(EMOEH-EMCEH)}$ | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 0) | (RH)*E - 3 | (RH)*E | (RH)*E + 3 | ns |
| | | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 1) | -3 | 0 | +3 | ns |
| 6 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_OE}$ low | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| 7 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_BA[1:0]}$ invalid | (RH)*E-3 | (RH)*E | (RH)*E+3 | ns |
| 8 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_OE}$ low | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| 9 | $t_{h(EMOEH-EMAIV)}$ | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_A[13:0]}$ invalid | (RH)*E-3 | (RH)*E | (RH)*E+3 | ns |
| 10 | $t_{w(EMOEL)}$ | $\overline{EMA_OE}$ active low width (EW = 0) | (RST)*E-3 | (RST)*E | (RST)*E+3 | ns |
| | | $\overline{EMA_OE}$ active low width (EW = 1) | (RST+EWC)*E-3 | (RST+EWC)*E | (RST+EWC)*E+3 | ns |
| 11 | $t_{d(EMWAITH-EMOEH)}$ | Delay time from EMA_WAIT deasserted to $\overline{EMA_OE}$ high | 3E-3 | 4E | 4E+3 | ns |
| 28 | $t_{su(EMARW-EMOEL)}$ | Output setup time, EMA_A_$\overline{RW}$ valid to $\overline{EMA_OE}$ low | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| 29 | $t_{h(EMOEH-EMARW)}$ | Output hold time, $\overline{EMA_OE}$ high to EMA_A_$\overline{RW}$ invalid | (RH)*E-3 | (RH)*E | (RH)*E+3 | ns |
| **WRITES** | | | | | | |
| 15 | $t_{c(EMWCYCLE)}$ | EMIF write cycle time (EW = 0) | (WS+WST+WH)*E-3 | (WS+WST+WH)*E | (WS+WST+WH)*E+3 | ns |
| | | EMIF write cycle time (EW = 1) | (WS+WST+WH+EWC)*E - 3 | (WS+WST+WH+EWC)*E | (WS+WST+WH+EWC)*E + 3 | ns |
| 16 | $t_{su(EMCEL-EMWEL)}$ | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS = 0) | (WS)*E - 3 | (WS)*E | (WS)*E + 3 | ns |
| | | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS = 1) | -3 | 0 | +3 | ns |
| 17 | $t_{h(EMWEH-EMCEH)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 0) | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| | | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 1) | -3 | 0 | +3 | ns |
| 18 | $t_{su(EMDQMV-EMWEL)}$ | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 19 | $t_{h(EMWEH-EMDQMIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 20 | $t_{su(EMBAV-EMWEL)}$ | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 21 | $t_{h(EMWEH-EMBAIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following range of values: TA[4-1], RS[16-1], RST[64-1], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEW[1-256].

(2) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL0 output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns.

(3) EWC = external wait cycles determined by EMA_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.


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**Table 6-22. Switching Characteristics for EMIFA Asynchronous Memory Interface (1) (2) (3) (continued)**

| NO. | PARAMETER | | 1.2V, 1.1V, 1.0V | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | Nom | MAX | |
| 22 | $t_{su(EMAV-EMWEL)}$ | Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 23 | $t_{h(EMWEH-EMAIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_A[13:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 24 | $t_{w(EMWEL)}$ | $\overline{EMA_WE}$ active low width (EW = 0) | (WST)*E-3 | (WST)*E | (WST)*E+3 | ns |
| | | $\overline{EMA_WE}$ active low width (EW = 1) | (WST+EWC)*E-3 | (WST+EWC)*E | (WST+EWC)*E+3 | ns |
| 25 | $t_{d(EMWAITH-EMWEH)}$ | Delay time from EMA_WAIT deasserted to $\overline{EMA_WE}$ high | 3E-3 | 4E | 4E+3 | ns |
| 26 | $t_{su(EMDV-EMWEL)}$ | Output setup time, $\overline{EMA_D[15:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 27 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_D[15:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 30 | $t_{su(EMARW-EMWEL)}$ | Output setup time, EMA_A_$\overline{RW}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 31 | $t_{h(EMWEH-EMARW)}$ | Output hold time, $\overline{EMA_WE}$ high to EMA_A_$\overline{RW}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |

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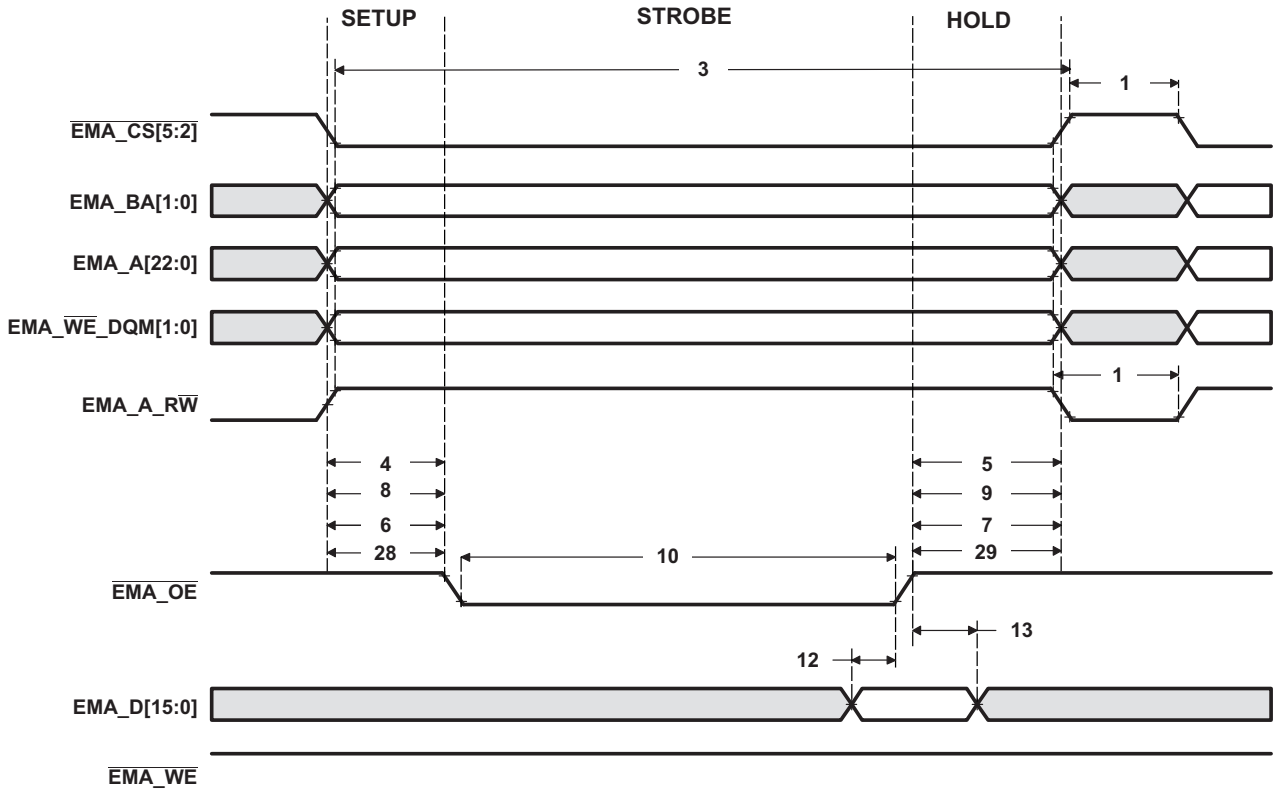



**Figure 6-14. Asynchronous Memory Read Timing for EMIFA**

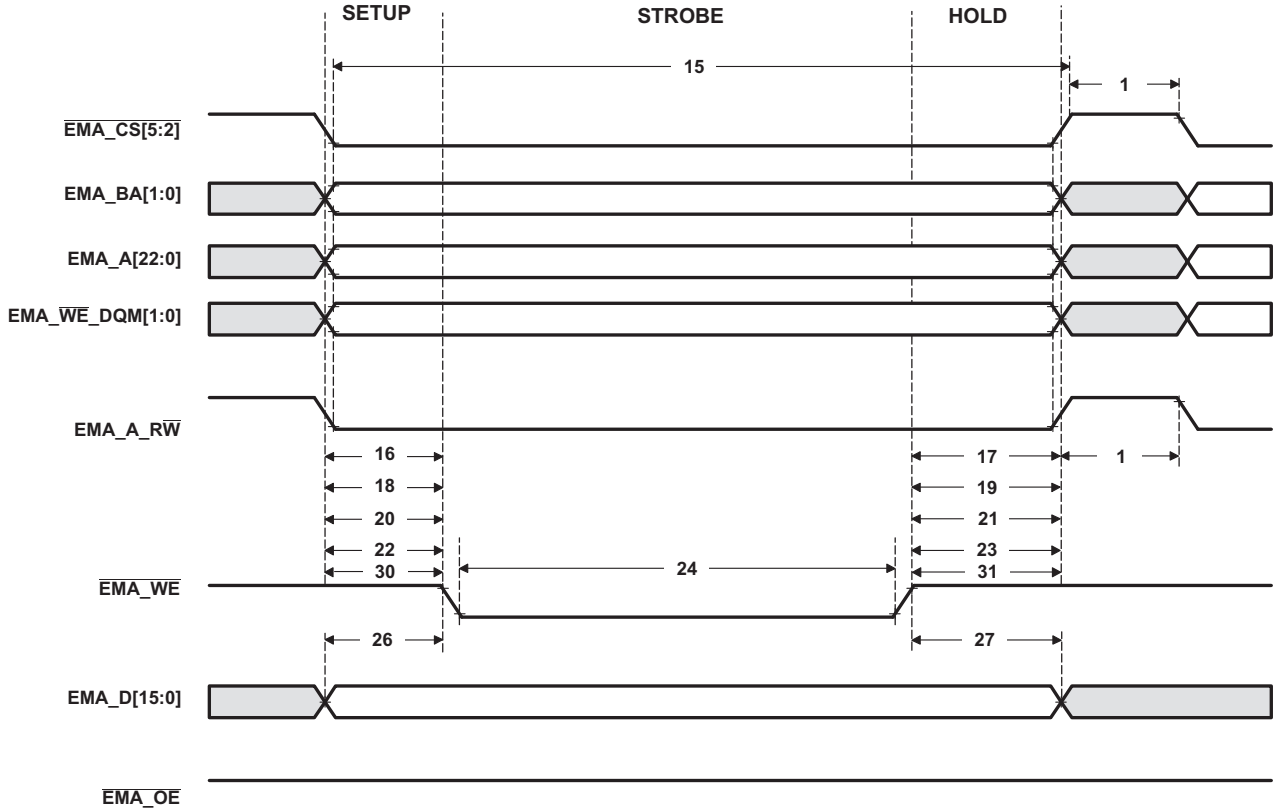



**Figure 6-15. Asynchronous Memory Write Timing for EMIFA**


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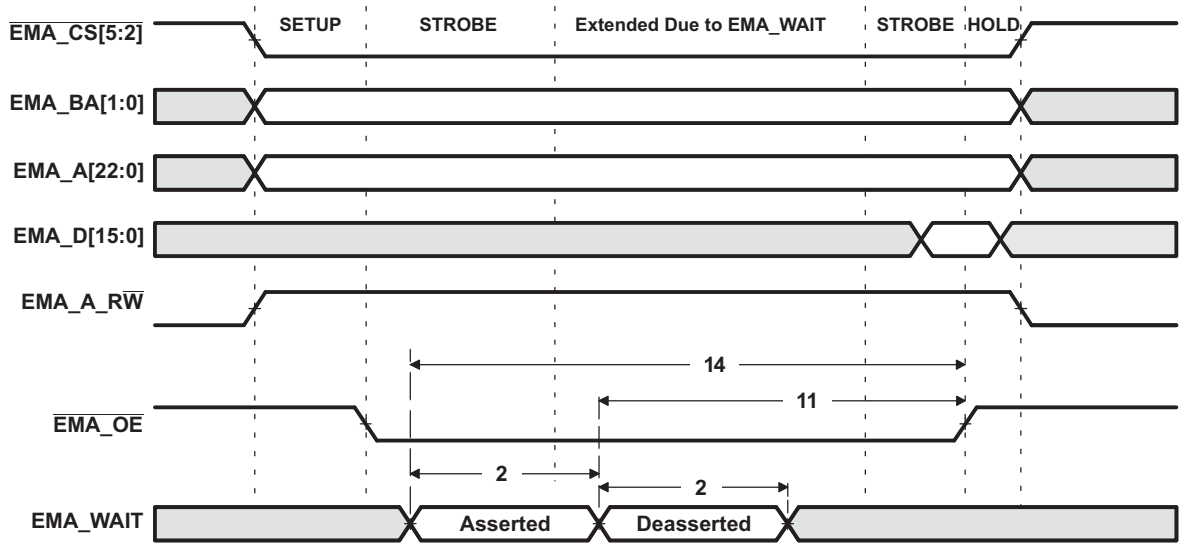



**Figure 6-16. EMA_WAIT Read Timing Requirements**

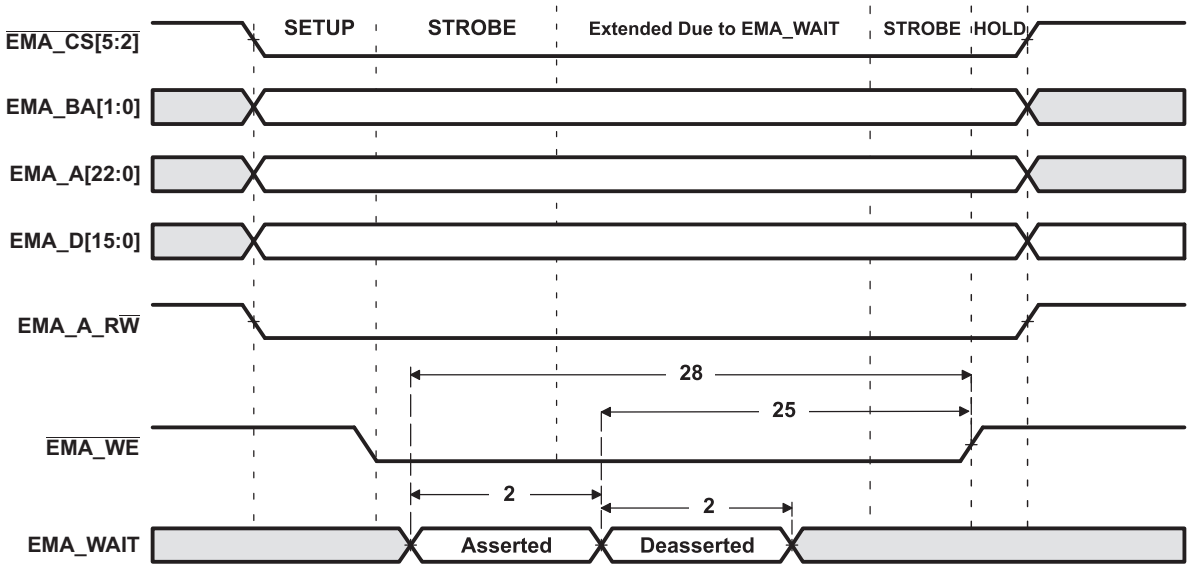



**Figure 6-17. EMA_WAIT Write Timing Requirements**

## 6.11 DDR2/mDDR Memory Controller

The DDR2/mDDR Memory Controller is a dedicated interface to DDR2/mDDR SDRAM. It supports JESD79-2A standard compliant DDR2 SDRAM devices and compliant Mobile DDR SDRAM devices.

The DDR2/mDDR Memory Controller support the following features:

- JESD79-2A standard compliant DDR2 SDRAM
- Mobile DDR SDRAM
- 256 MByte memory space for DDR2
- 256 MByte memory space for mDDR
- CAS latencies:
  - DDR2: 2, 3, 4 and 5
  - mDDR: 2 and 3
- Internal banks:
  - DDR2: 1, 2, 4 and 8
  - mDDR:1, 2 and 4
- Burst length: 8
- Burst type: sequential
- 1 chip select (CS) signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Partial array self-refresh (for mDDR)
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little endian

### *6.11.1 DDR2/mDDR Memory Controller Electrical Data/Timing*

**Table 6-23. Switching Characteristics Over Recommended Operating Conditions for DDR2/mDDR Memory Controller**

| No. | PARAMETER | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(DDR_CLK)}$ | Cycle time, DDR_CLKP / DDR_CLKN | DDR2 | 125 | 156 | 125 | 150 | —(1) | —(1) | MHz |
| | | | mDDR | 105 | 150 | 100 | 133 | 95 | 133 | |

(1) DDR2 is not supported at this voltage operating point.


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### 6.11.2 DDR2/mDDR Memory Controller Register Description(s)

**Table 6-24. DDR2/mDDR Memory Controller Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0xB000 0000 | REVID | Revision ID Register |
| 0xB000 0004 | SDRSTAT | SDRAM Status Register |
| 0xB000 0008 | SDCR | SDRAM Configuration Register |
| 0xB000 000C | SDRCR | SDRAM Refresh Control Register |
| 0xB000 0010 | SDTIMR1 | SDRAM Timing Register 1 |
| 0xB000 0014 | SDTIMR2 | SDRAM Timing Register 2 |
| 0xB000 001C | SDCR2 | SDRAM Configuration Register 2 |
| 0xB000 0020 | PBBPR | Peripheral Bus Burst Priority Register |
| 0xB000 0040 | PC1 | Performance Counter 1 Registers |
| 0xB000 0044 | PC2 | Performance Counter 2 Register |
| 0xB000 0048 | PCC | Performance Counter Configuration Register |
| 0xB000 004C | PCMRS | Performance Counter Master Region Select Register |
| 0xB000 0050 | PCT | Performance Counter Time Register |
| 0xB000 00C0 | IRR | Interrupt Raw Register |
| 0xB000 00C4 | IMR | Interrupt Mask Register |
| 0xB000 00C8 | IMSR | Interrupt Mask Set Register |
| 0xB000 00CC | IMCR | Interrupt Mask Clear Register |
| 0xB000 00E4 | DRPYC1R | DDR PHY Control Register 1 |
| 0x01E2 C000 | VTPIO_CTL | VTP IO Control Register |

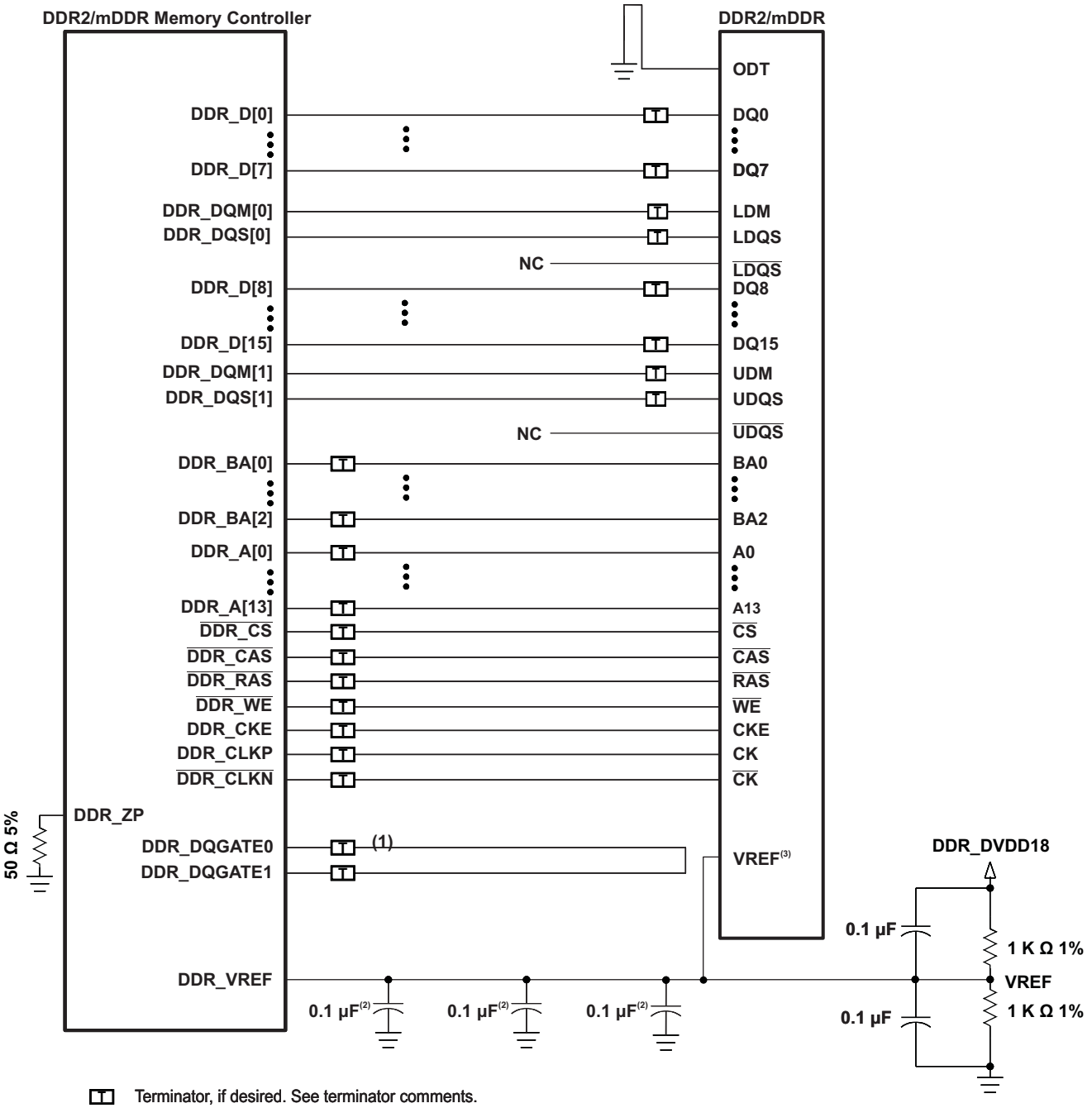
### 6.11.3 DDR2/mDDR Interface

This section provides the timing specification for the DDR2/mDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2/mDDR memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2/mDDR specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0).

#### 6.11.3.1 DDR2/mDDR Interface Schematic

Figure 6-18 shows the DDR2/mDDR interface schematic for a single-memory DDR2/mDDR system. The dual-memory system shown in Figure 6-19. Pin numbers for the device can be obtained from the pin description section.

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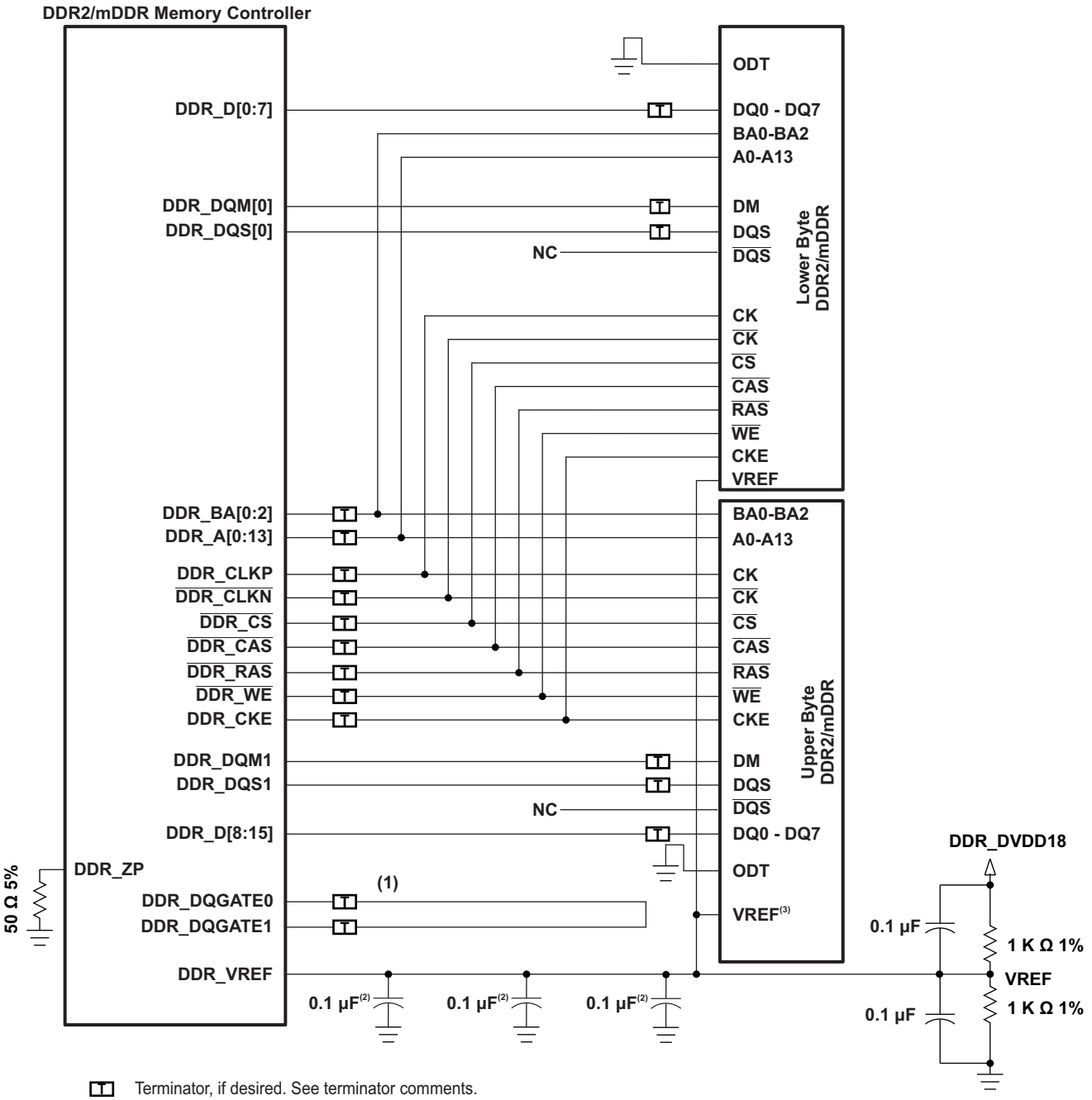

(1) See Figure 6-25 for DQGATE routing specifications.

(2) For DDR2, one of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin. For mDDR, these capacitors can be eliminated completely.

(3) VREF applies in the case of DDR2 memories. For mDDR, the DDR_VREF pin still needs to be connected to the divider circuit.

**Figure 6-18. DDR2/mDDR Single-Memory High Level Schematic**


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T Terminator, if desired. See terminator comments.

(1) See Figure 6-25 for DQGATE routing specifications.

(2) For DDR2, one of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin. For mDDR, these capacitors can be eliminated completely.

(3) VREF applies in the case of DDR2 memories. For mDDR, the DDR_VREF pin still needs to be connected to the divider circuit.

**Figure 6-19. DDR2/mDDR Dual-Memory High Level Schematic**

### 6.11.3.2 Compatible JEDEC DDR2/mDDR Devices

Table 6-25 shows the parameters of the JEDEC DDR2/mDDR devices that are compatible with this interface. Generally, the DDR2/mDDR interface is compatible with x16 DDR2-400/mDDR-200 speed grade DDR2/mDDR devices.

The device also supports JEDEC DDR2/mDDR x8 devices in the dual chip configuration. In this case, one chip supplies the upper byte and the second chip supplies the lower byte. Addresses and most control signals are shared just like regular dual chip memory configurations.

**Table 6-25. Compatible JEDEC DDR2/mDDR Devices**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | JEDEC DDR2/mDDR Device Speed Grade(1) | DDR2-400/mDDR-200 | | |
| 2 | JEDEC DDR2/mDDR Device Bit Width | x8 | x16 | Bits |
| 3 | JEDEC DDR2/mDDR Device Count(2) | 1 | 2 | Devices |

(1) Higher DDR2/mDDR speed grades are supported due to inherent JEDEC DDR2/mDDR backwards compatibility.
(2) Supported configurations are one 16-bit DDR2/mDDR memory or two 8-bit DDR2/mDDR memories

### 6.11.3.3 PCB Stackup

The minimum stackup required for routing the device is a six layer stack as shown in Table 6-26. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.Complete stack up specifications are provided in Table 6-27.

**Table 6-26. Device Minimum PCB Stack Up**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top Routing Mostly Horizontal |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Internal Routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom Routing Mostly Vertical |

**Table 6-27. PCB Stack Up Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB Routing/Plane Layers | 6 | | | |
| 2 | Signal Routing Layers | 3 | | | |
| 3 | Full ground layers under DDR2/mDDR routing region | 2 | | | |
| 4 | Number of ground plane cuts allowed within DDR routing region | | | 0 | |
| 5 | Number of ground reference planes required for each DDR2/mDDR routing layer | 1 | | | |
| 6 | Number of layers between DDR2/mDDR routing layer and reference ground plane | | | 0 | |
| 7 | PCB Routing Feature Size | | 4 | | Mils |
| 8 | PCB Trace Width w | | 4 | | Mils |
| 8 | PCB BGA escape via pad size | | 18 | | Mils |
| 9 | PCB BGA escape via hole size | | 8 | | Mils |
| 10 | Device BGA pad size(1) | | | | |
| 11 | DDR2/mDDR Device BGA pad size(2) | | | | |
| 12 | Single Ended Impedance, Zo | 50 | | 75 | Ω |
| 13 | Impedance Control(3) | Z-5 | Z | Z+5 | Ω |

(1) Please refer to the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) for device BGA pad size.
(2) Please refer to the DDR2/mDDR device manufacturer documentation for the DDR2/mDDR device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.


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### 6.11.3.4 Placement

Figure 6-19 shows the required placement for the device as well as the DDR2/mDDR devices. The dimensions for Figure 6-20 are defined in Table 6-28. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory DDR2/mDDR systems, the second DDR2/mDDR device is omitted from the placement.

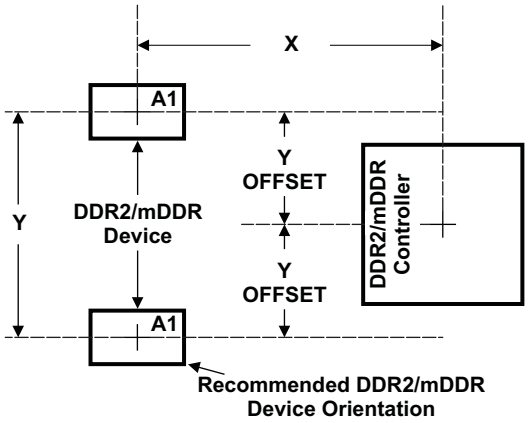



**Figure 6-20. C6742 and DDR2/mDDR Device Placement**

**Table 6-28. Placement Specifications(1)(2)**

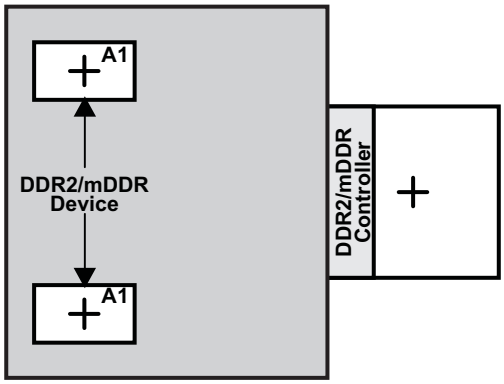
| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X | | 1750 | Mils |
| 2 | Y | | 1280 | Mils |
| 3 | Y Offset | | (3)650 | Mils |
| 4 | Clearance from non-DDR2/mDDR signal to DDR2/mDDR Keepout Region(4) | 4 | | w(5) |

(1) See Figure 6-20 for dimension definitions.
(2) Measurements from center of device to center of DDR2/mDDR device.
(3) For single memory systems it is recommended that Y Offset be as small as possible.
(4) Non-DDR2/mDDR signals allowed within DDR2/mDDR keepout region provided they are separated from DDR2/mDDR routing layers by a ground plane.
(5) w = PCB trace width as defined in Table 6-27.

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### 6.11.3.5 DDR2/mDDR Keep Out Region

The region of the PCB used for the DDR2/mDDR circuitry must be isolated from other signals. The DDR2/mDDR keep out region is defined for this purpose and is shown in Figure 6-21. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 6-28.




**Region should encompass all DDR2/mDDR circuitry and varies depending on placement. Non-DDR2/mDDR signals should not be routed on the DDR signal layers within the DDR2/mDDR keep out region. Non-DDR2/mDDR signals may be routed in the region provided they are routed on layers separated from DDR2/mDDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.**

**Figure 6-21. DDR2/mDDR Keepout Region**


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### 6.11.3.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2/mDDR and other circuitry. Table 6-29 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DSP and DDR2/mDDR interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 6-29. Bulk Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | DDR_DVDD18 Supply Bulk Bypass Capacitor Count(1) | 3 | | Devices |
| 2 | DDR_DVDD18 Supply Bulk Bypass Total Capacitance | 30 | | µF |
| 3 | DDR#1 Bulk Bypass Capacitor Count(1) | 1 | | Devices |
| 4 | DDR#1 Bulk Bypass Total Capacitance | 22 | | µF |
| 5 | DDR#2 Bulk Bypass Capacitor Count(1)(2) | 1 | | Devices |
| 6 | DDR#2 Bulk Bypass Total Capacitance(2) | 22 | | µF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.
(2) Only used on dual-memory systems.

### 6.11.3.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2/mDDR interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, DSP/DDR2/mDDR power, and DSP/DDR2/mDDR ground connections. Table 6-30 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

**Table 6-30. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | HS Bypass Capacitor Package Size(1) | | 0402 | 10 Mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | Mils |
| 3 | Number of connection vias for each HS bypass capacitor | 2(2) | | Vias |
| 4 | Trace length from bypass capacitor contact to connection via | 1 | 30 | Mils |
| 5 | Number of connection vias for each DDR2/mDDR device power or ground balls | 1 | | Vias |
| 6 | Trace length from DDR2/mDDR device power ball to connection via | | 35 | Mils |
| 7 | DDR_DVDD18 Supply HS Bypass Capacitor Count(3) | 10 | | Devices |
| 8 | DDR_DVDD18 Supply HS Bypass Capacitor Total Capacitance | 0.6 | | µF |
| 9 | DDR#1 HS Bypass Capacitor Count(3) | 8 | | Devices |
| 10 | DDR#1 HS Bypass Capacitor Total Capacitance | 0.4 | | µF |
| 11 | DDR#2 HS Bypass Capacitor Count(3)(4) | 8 | | Devices |
| 12 | DDR#2 HS Bypass Capacitor Total Capacitance(4) | 0.4 | | µF |

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Only used on dual-memory systems.

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### 6.11.3.8 Net Classes

Table 6-31 lists the clock net classes for the DDR2/mDDR interface. Table 6-32 lists the signal net classes, and associated clock net classes, for the signals in the DDR2/mDDR interface. These net classes are used for the termination and routing rules that follow.

**Table 6-31. Clock Net Class Definitions**

| CLOCK NET CLASS | DSP PIN NAMES |
|---|---|
| CK | DDR_CLKP / DDR_CLKN |
| DQS0 | DDR_DQS[0] |
| DQS1 | DDR_DQS[1] |

**Table 6-32. Signal Net Class Definitions**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | DSP PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_A[13:0], DDR_CS, DDR_CAS, DDR_RAS, DDR_WE, DDR_CKE |
| D0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| D1 | DQS1 | DDR_D[15:8], DDR_DQM1 |
| DQGATE | CK, DQS0, DQS1 | DDR_DQGATE0, DDR_DQGATE1 |

### 6.11.3.9 DDR2/mDDR Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 6-33 shows the specifications for the series terminators.

**Table 6-33. DDR2/mDDR Signal Terminations(1)(2)(3)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | CK Net Class | 0 | | 10 | Ω |
| 2 | ADDR_CTRL Net Class | 0 | 22 | Zo | Ω |
| 3 | Data Byte Net Classes (DQS[0], DQS[1], D0, D1)(4) | 0 | 22 | Zo | Ω |
| 4 | DQGATE Net Class (DQGATE) | 0 | 10 | Zo | Ω |

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ω), the DDR2/mDDR devices must be programmed to operate in 60% strength mode.


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### 6.11.3.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2/mDDR memories as well as the C6742 . VREF is intended to be half the DDR2/mDDR power supply voltage and should be created using a resistive divider as shown in Figure 6-18. Other methods of creating VREF are not recommended. Figure 6-22 shows the layout guidelines for VREF.

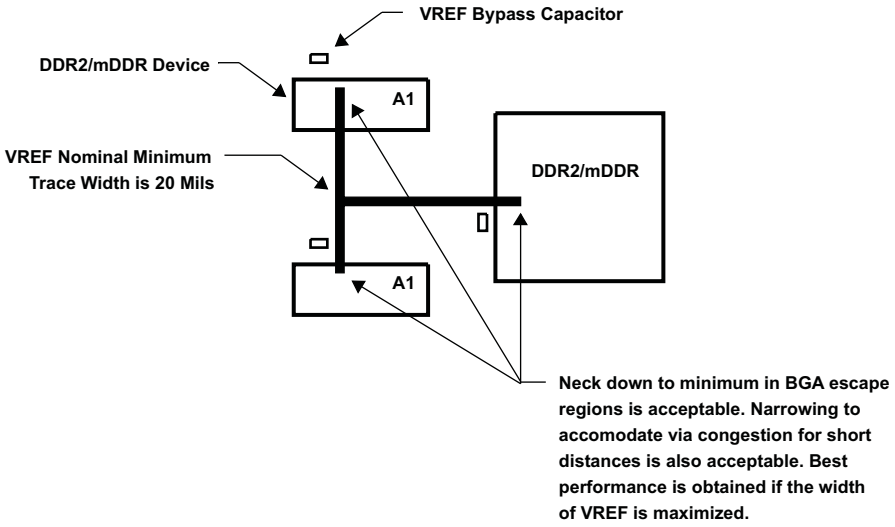



**Figure 6-22. VREF Routing and Topology**

### 6.11.3.11 DDR2/mDDR CK and ADDR_CTRL Routing

Figure 6-23 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

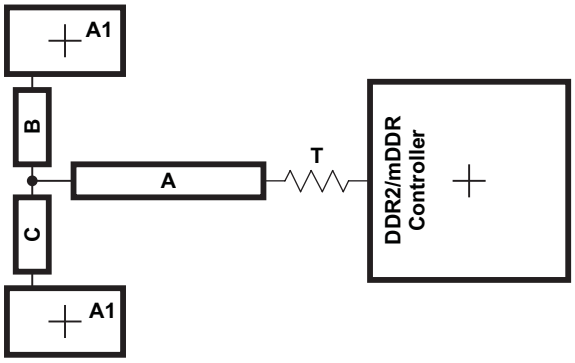



**Figure 6-23. CK and ADDR_CTRL Routing and Topology**

**Table 6-34. CK and ADDR_CTRL Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center to Center CK-CKN Spacing(1) | | | 2w(2) | |
| 2 | CK A to B/A to C Skew Length Mismatch(3) | | | 25 | Mils |
| 3 | CK B to C Skew Length Mismatch | | | 25 | Mils |
| 4 | Center to center CK to other DDR2/mDDR trace spacing(1) | 4w(2) | | | |
| 5 | CK/ADDR_CTRL nominal trace length(4) | CACLM-50 | CACLM | CACLM+50 | Mils |
| 6 | ADDR_CTRL to CK Skew Length Mismatch | | | 100 | Mils |
| 7 | ADDR_CTRL to ADDR_CTRL Skew Length Mismatch | | | 100 | Mils |
| 8 | Center to center ADDR_CTRL to other DDR2/mDDR trace spacing(1) | 4w(2) | | | |
| 9 | Center to center ADDR_CTRL to other ADDR_CTRL trace spacing(1) | 3w (2) | | | |
| 10 | ADDR_CTRL A to B/A to C Skew Length Mismatch(3) | | | 100 | Mils |
| 11 | ADDR_CTRL B to C Skew Length Mismatch | | | 100 | Mils |

(1) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) w = PCB trace width as defined in Table 6-27.
(3) Series terminator, if used, should be located closest to device.
(4) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.


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Figure 6-24 shows the topology and routing for the DQS and D net class; the routes are point to point. Skew matching across bytes is not needed nor recommended.

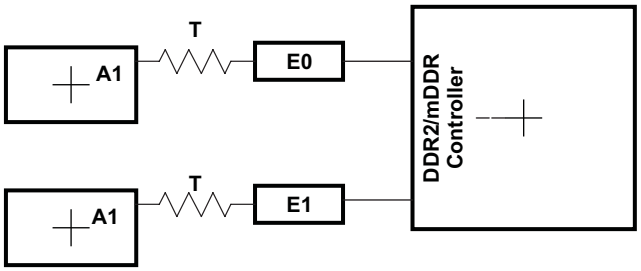



**Figure 6-24. DQS and D Routing and Topology**

**Table 6-35. DQS and D Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center to center DQS to other DDR2/mDDR trace spacing(1) | 4w(2) | | | |
| 2 | DQS/D nominal trace length(3)(4) | DQLM-50 | DQLM | DQLM+50 | Mils |
| 3 | D to DQS Skew Length Mismatch(4) | | | 100 | Mils |
| 4 | D to D Skew Length Mismatch(4) | | | 100 | Mils |
| 5 | Center to center D to other DDR2/mDDR trace spacing(1)(5) | 4w(2) | | | |
| 6 | Center to Center D to other D trace spacing(1)(6) | 3w(2) | | | |

(1) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) w = PCB trace width as defined in Table 6-27.
(3) Series terminator, if used, should be located closest to DDR.
(4) There is no need and it is not recommended to skew match across data bytes, i.e., from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) D's from other DQS domains are considered *other DDR2/mDDR trace*.
(6) DQLM is the longest Manhattan distance of each of the DQS and D net class.

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Figure 6-25 shows the routing for the DQGATE net class. Table 6-36 contains the routing specification.

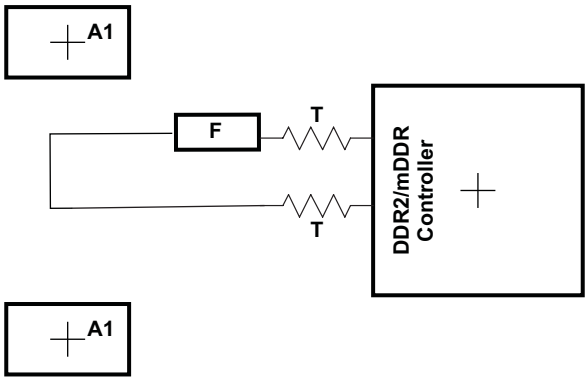



**Figure 6-25. DQGATE Routing**

**Table 6-36. DQGATE Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | DQGATE Length F | | CKB0B(1) | | |
| 2 | Center to center DQGATE to any other trace spacing | 4w(2) | | | |
| 3 | DQS/D nominal trace length | DQLM-50 | DQLM | DQLM+50 | Mils |
| 4 | DQGATE Skew(3) | | | 100 | Mils |

(1) CKB0B1 is the sum of the length of the CK net plus the average length of the DQS0 and DQS1 nets.
(2) w = PCB trace width as defined in Table 6-27.
(3) Skew from CKB0B1

### 6.11.3.12 DDR2/mDDR Boundary Scan Limitations

Due to DDR implementation and timing restrictions, it was not possible to place boundary scan cells between core logic and the IO like boundary scan cells for other IO. Instead, the boundary scan cells are tapped-off to the DDR PHY and there is the equivalent of a multiplexer inside the DDR PHY which selects between functional and boundary scan paths.

The implication for boundary scan is that the DDR pins will not support the SAMPLE function of the output enable cells on the DDR pins and this is a violation of IEEE 1149.1. Full EXTEST and PRELOAD capability is still available.


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## 6.12 Memory Protection Units

The MPU performs memory protection checking. It receives requests from a bus master in the system and checks the address against the fixed and programmable regions to see if the access is allowed. If allowed, the transfer is passed unmodified to its output bus (to the targeted address). If the transfer is illegal (fails the protection check) then the MPU does not pass the transfer to the output bus but rather services the transfer internally back to the input bus (to prevent a hang) returning the fault status to the requestor as well as generating an interrupt about the fault. The following features are supported by the MPU:

- Provides memory protection for fixed and programmable address ranges.
- Supports multiple programmable address region.
- Supports secure and debug access privileges.
- Supports read, write, and execute access privileges.
- Supports privid(8) associations with ranges.
- Generates an interrupt when there is a protection violation, and saves violating transfer parameters.
- MMR access is also protected.

**Table 6-37. MPU1 Configuration Registers**

| MPU1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 4000 | REVID | Revision ID |
| 0x01E1 4004 | CONFIG | Configuration |
| 0x01E1 4010 | IRAWSTAT | Interrupt raw status/set |
| 0x01E1 4014 | IENSTAT | Interrupt enable status/clear |
| 0x01E1 4018 | IENSET | Interrupt enable |
| 0x01E1 401C | IENCLR | Interrupt enable clear |
| 0x01E1 4020 - 0x01E1 41FF | - | Reserved |
| 0x01E1 4200 | PROG1_MPSAR | Programmable range 1, start address |
| 0x01E1 4204 | PROG1_MPEAR | Programmable range 1, end address |
| 0x01E1 4208 | PROG1_MPPA | Programmable range 1, memory page protection attributes |
| 0x01E1 420C - 0x01E1 420F | - | Reserved |
| 0x01E1 4210 | PROG2_MPSAR | Programmable range 2, start address |
| 0x01E1 4214 | PROG2_MPEAR | Programmable range 2, end address |
| 0x01E1 4218 | PROG2_MPPA | Programmable range 2, memory page protection attributes |
| 0x01E1 421C - 0x01E1 421F | - | Reserved |
| 0x01E1 4220 | PROG3_MPSAR | Programmable range 3, start address |
| 0x01E1 4224 | PROG3_MPEAR | Programmable range 3, end address |
| 0x01E1 4228 | PROG3_MPPA | Programmable range 3, memory page protection attributes |
| 0x01E1 422C - 0x01E1 422F | - | Reserved |
| 0x01E1 4230 | PROG4_MPSAR | Programmable range 4, start address |
| 0x01E1 4234 | PROG4_MPEAR | Programmable range 4, end address |
| 0x01E1 4238 | PROG4_MPPA | Programmable range 4, memory page protection attributes |
| 0x01E1 423C - 0x01E1 423F | - | Reserved |
| 0x01E1 4240 | PROG5_MPSAR | Programmable range 5, start address |
| 0x01E1 4244 | PROG5_MPEAR | Programmable range 5, end address |
| 0x01E1 4248 | PROG5_MPPA | Programmable range 5, memory page protection attributes |
| 0x01E1 424C - 0x01E1 424F | - | Reserved |
| 0x01E1 4250 | PROG6_MPSAR | Programmable range 6, start address |
| 0x01E1 4254 | PROG6_MPEAR | Programmable range 6, end address |
| 0x01E1 4258 | PROG6_MPPA | Programmable range 6, memory page protection attributes |
| 0x01E1 425C - 0x01E1 42FF | - | Reserved |

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**Table 6-37. MPU1 Configuration Registers (continued)**

| MPU1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 4300 | FLTADDRR | Fault address |
| 0x01E1 4304 | FLTSTAT | Fault status |
| 0x01E1 4308 | FLTCLR | Fault clear |
| 0x01E1 430C - 0x01E1 4FFF | - | Reserved |

**Table 6-38. MPU2 Configuration Registers**

| MPU2 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 5000 | REVID | Revision ID |
| 0x01E1 5004 | CONFIG | Configuration |
| 0x01E1 5010 | IRAWSTAT | Interrupt raw status/set |
| 0x01E1 5014 | IENSTAT | Interrupt enable status/clear |
| 0x01E1 5018 | IENSET | Interrupt enable |
| 0x01E1 501C | IENCLR | Interrupt enable clear |
| 0x01E1 5020 - 0x01E1 51FF | - | Reserved |
| 0x01E1 5200 | PROG1_MPSAR | Programmable range 1, start address |
| 0x01E1 5204 | PROG1_MPEAR | Programmable range 1, end address |
| 0x01E1 5208 | PROG1_MPPA | Programmable range 1, memory page protection attributes |
| 0x01E1 520C - 0x01E1 520F | - | Reserved |
| 0x01E1 5210 | PROG2_MPSAR | Programmable range 2, start address |
| 0x01E1 5214 | PROG2_MPEAR | Programmable range 2, end address |
| 0x01E1 5218 | PROG2_MPPA | Programmable range 2, memory page protection attributes |
| 0x01E1 521C - 0x01E1 521F | - | Reserved |
| 0x01E1 5220 | PROG3_MPSAR | Programmable range 3, start address |
| 0x01E1 5224 | PROG3_MPEAR | Programmable range 3, end address |
| 0x01E1 5228 | PROG3_MPPA | Programmable range 3, memory page protection attributes |
| 0x01E1 522C - 0x01E1 522F | - | Reserved |
| 0x01E1 5230 | PROG4_MPSAR | Programmable range 4, start address |
| 0x01E1 5234 | PROG4_MPEAR | Programmable range 4, end address |
| 0x01E1 5238 | PROG4_MPPA | Programmable range 4, memory page protection attributes |
| 0x01E1 523C - 0x01E1 523F | - | Reserved |
| 0x01E1 5240 | PROG5_MPSAR | Programmable range 5, start address |
| 0x01E1 5244 | PROG5_MPEAR | Programmable range 5, end address |
| 0x01E1 5248 | PROG5_MPPA | Programmable range 5, memory page protection attributes |
| 0x01E1 524C - 0x01E1 524F | - | Reserved |
| 0x01E1 5250 | PROG6_MPSAR | Programmable range 6, start address |
| 0x01E1 5254 | PROG6_MPEAR | Programmable range 6, end address |
| 0x01E1 5258 | PROG6_MPPA | Programmable range 6, memory page protection attributes |
| 0x01E1 525C - 0x01E1 525F | - | Reserved |
| 0x01E1 5260 | PROG7_MPSAR | Programmable range 7, start address |
| 0x01E1 5264 | PROG7_MPEAR | Programmable range 7, end address |
| 0x01E1 5268 | PROG7_MPPA | Programmable range 7, memory page protection attributes |
| 0x01E1 526C - 0x01E1 526F | - | Reserved |
| 0x01E1 5270 | PROG8_MPSAR | Programmable range 8, start address |
| 0x01E1 5274 | PROG8_MPEAR | Programmable range 8, end address |
| 0x01E1 5278 | PROG8_MPPA | Programmable range 8, memory page protection attributes |
| 0x01E1 527C - 0x01E1 527F | - | Reserved |


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**Table 6-38. MPU2 Configuration Registers (continued)**

| MPU2 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 5280 | PROG9_MPSAR | Programmable range 9, start address |
| 0x01E1 5284 | PROG9_MPEAR | Programmable range 9, end address |
| 0x01E1 5288 | PROG9_MPPA | Programmable range 9, memory page protection attributes |
| 0x01E1 528C - 0x01E1 528F | - | Reserved |
| 0x01E1 5290 | PROG10_MPSAR | Programmable range 10, start address |
| 0x01E1 5294 | PROG10_MPEAR | Programmable range 10, end address |
| 0x01E1 5298 | PROG10_MPPA | Programmable range 10, memory page protection attributes |
| 0x01E1 529C - 0x01E1 529F | - | Reserved |
| 0x01E1 52A0 | PROG11_MPSAR | Programmable range 11, start address |
| 0x01E1 52A4 | PROG11_MPEAR | Programmable range 11, end address |
| 0x01E1 52A8 | PROG11_MPPA | Programmable range 11, memory page protection attributes |
| 0x01E1 52AC - 0x01E1 52AF | - | Reserved |
| 0x01E1 52B0 | PROG12_MPSAR | Programmable range 12, start address |
| 0x01E1 52B4 | PROG12_MPEAR | Programmable range 12, end address |
| 0x01E1 52B8 | PROG12_MPPA | Programmable range 12, memory page protection attributes |
| 0x01E1 52BC - 0x01E1 52FF | - | Reserved |
| 0x01E1 5300 | FLTADDRR | Fault address |
| 0x01E1 5304 | FLTSTAT | Fault status |
| 0x01E1 5308 | FLTCLR | Fault clear |
| 0x01E1 530C - 0x01E1 5FFF | - | Reserved |

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## 6.13 Multichannel Audio Serial Port (McASP)

The McASP serial port is specifically designed for multichannel audio applications. Its key features are:

- Flexible clock and frame sync generation logic and on-chip dividers
- Up to sixteen transmit or receive data pins and serializers
- Large number of serial data format options, including:
  - TDM Frames with 2 to 32 time slots per frame (periodic) or 1 slot per frame (burst)
  - Time slots of 8,12,16, 20, 24, 28, and 32 bits
  - First bit delay 0, 1, or 2 clocks
  - MSB or LSB first bit order
  - Left- or right-aligned data words within time slots
- DIT Mode with 384-bit Channel Status and 384-bit User Data registers
- Extensive error checking and mute generation logic
- All unused pins GPIO-capable
- Transmit & Receive FIFO Buffers allow the McASP to operate at a higher sample rate by making it more tolerant to DMA latency.
- Dynamic Adjustment of Clock Dividers
  - Clock Divider Value may be changed without resetting the McASP

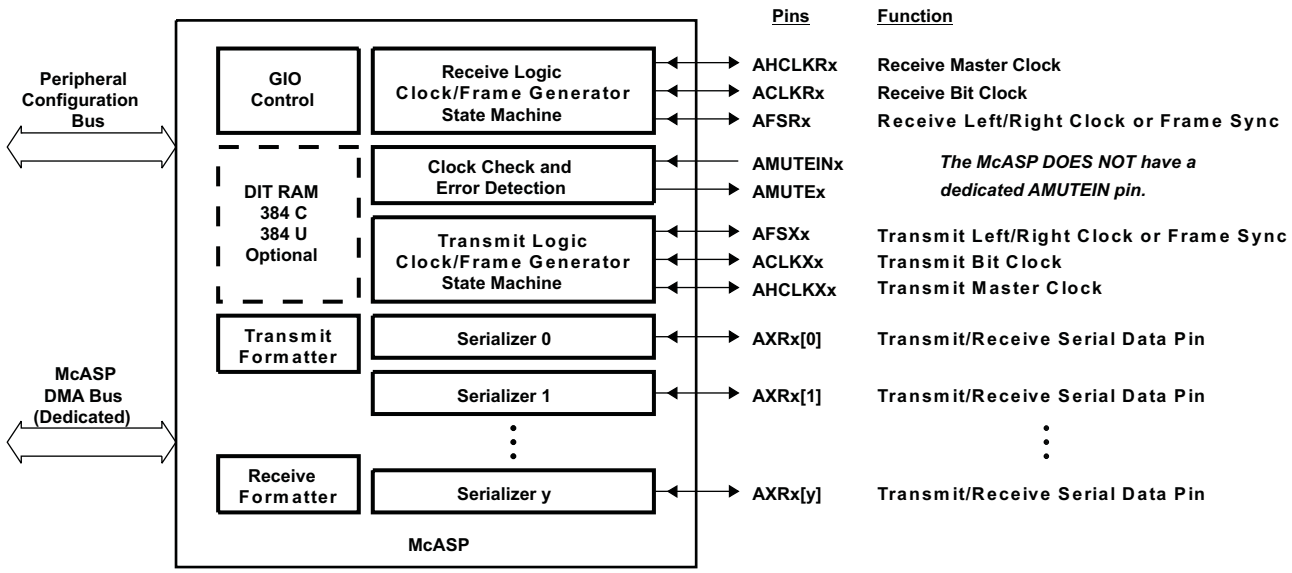



**Figure 6-26. McASP Block Diagram**


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### 6.13.1 McASP Peripheral Registers Description(s)

Registers for the McASP are summarized in Table 6-39. The registers are accessed through the peripheral configuration port. The receive buffer registers (RBUF) and transmit buffer registers (XBUF) can also be accessed through the DMA port, as listed in Table 6-40

Registers for the McASP Audio FIFO (AFIFO) are summarized in Table 6-41. Note that the AFIFO Write FIFO (WFIFO) and Read FIFO (RFIFO) have independent control and status registers. The AFIFO control registers are accessed through the peripheral configuration port.

**Table 6-39. McASP Registers Accessed Through Peripheral Configuration Port**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 0000 | REV | Revision identification register |
| 0x01D0 0010 | PFUNC | Pin function register |
| 0x01D0 0014 | PDIR | Pin direction register |
| 0x01D0 0018 | PDOUT | Pin data output register |
| 0x01D0 001C | PDIN | Read returns: Pin data input register |
| 0x01D0 001C | PDSET | Writes affect: Pin data set register (alternate write address: PDOUT) |
| 0x01D0 0020 | PDCLR | Pin data clear register (alternate write address: PDOUT) |
| 0x01D0 0044 | GBLCTL | Global control register |
| 0x01D0 0048 | AMUTE | Audio mute control register |
| 0x01D0 004C | DLBCTL | Digital loopback control register |
| 0x01D0 0050 | DITCTL | DIT mode control register |
| 0x01D0 0060 | RGBLCTL | Receiver global control register: Alias of GBLCTL, only receive bits are affected - allows receiver to be reset independently from transmitter |
| 0x01D0 0064 | RMASK | Receive format unit bit mask register |
| 0x01D0 0068 | RFMT | Receive bit stream format register |
| 0x01D0 006C | AFSRCTL | Receive frame sync control register |
| 0x01D0 0070 | ACLKRCTL | Receive clock control register |
| 0x01D0 0074 | AHCLKRCTL | Receive high-frequency clock control register |
| 0x01D0 0078 | RTDM | Receive TDM time slot 0-31 register |
| 0x01D0 007C | RINTCTL | Receiver interrupt control register |
| 0x01D0 0080 | RSTAT | Receiver status register |
| 0x01D0 0084 | RSLOT | Current receive TDM time slot register |
| 0x01D0 0088 | RCLKCHK | Receive clock check control register |
| 0x01D0 008C | REVTCTL | Receiver DMA event control register |
| 0x01D0 00A0 | XGBLCTL | Transmitter global control register. Alias of GBLCTL, only transmit bits are affected - allows transmitter to be reset independently from receiver |
| 0x01D0 00A4 | XMASK | Transmit format unit bit mask register |
| 0x01D0 00A8 | XFMT | Transmit bit stream format register |
| 0x01D0 00AC | AFSXCTL | Transmit frame sync control register |
| 0x01D0 00B0 | ACLKXCTL | Transmit clock control register |
| 0x01D0 00B4 | AHCLKXCTL | Transmit high-frequency clock control register |
| 0x01D0 00B8 | XTDM | Transmit TDM time slot 0-31 register |
| 0x01D0 00BC | XINTCTL | Transmitter interrupt control register |
| 0x01D0 00C0 | XSTAT | Transmitter status register |
| 0x01D0 00C4 | XSLOT | Current transmit TDM time slot register |
| 0x01D0 00C8 | XCLKCHK | Transmit clock check control register |
| 0x01D0 00CC | XEVTCTL | Transmitter DMA event control register |
| 0x01D0 0100 | DITCSRA0 | Left (even TDM time slot) channel status register (DIT mode) 0 |
| 0x01D0 0104 | DITCSRA1 | Left (even TDM time slot) channel status register (DIT mode) 1 |
| 0x01D0 0108 | DITCSRA2 | Left (even TDM time slot) channel status register (DIT mode) 2 |

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**Table 6-39. McASP Registers Accessed Through Peripheral Configuration Port (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 010C | DITCSRA3 | Left (even TDM time slot) channel status register (DIT mode) 3 |
| 0x01D0 0110 | DITCSRA4 | Left (even TDM time slot) channel status register (DIT mode) 4 |
| 0x01D0 0114 | DITCSRA5 | Left (even TDM time slot) channel status register (DIT mode) 5 |
| 0x01D0 0118 | DITCSRB0 | Right (odd TDM time slot) channel status register (DIT mode) 0 |
| 0x01D0 011C | DITCSRB1 | Right (odd TDM time slot) channel status register (DIT mode) 1 |
| 0x01D0 0120 | DITCSRB2 | Right (odd TDM time slot) channel status register (DIT mode) 2 |
| 0x01D0 0124 | DITCSRB3 | Right (odd TDM time slot) channel status register (DIT mode) 3 |
| 0x01D0 0128 | DITCSRB4 | Right (odd TDM time slot) channel status register (DIT mode) 4 |
| 0x01D0 012C | DITCSRB5 | Right (odd TDM time slot) channel status register (DIT mode) 5 |
| 0x01D0 0130 | DITUDRA0 | Left (even TDM time slot) channel user data register (DIT mode) 0 |
| 0x01D0 0134 | DITUDRA1 | Left (even TDM time slot) channel user data register (DIT mode) 1 |
| 0x01D0 0138 | DITUDRA2 | Left (even TDM time slot) channel user data register (DIT mode) 2 |
| 0x01D0 013C | DITUDRA3 | Left (even TDM time slot) channel user data register (DIT mode) 3 |
| 0x01D0 0140 | DITUDRA4 | Left (even TDM time slot) channel user data register (DIT mode) 4 |
| 0x01D0 0144 | DITUDRA5 | Left (even TDM time slot) channel user data register (DIT mode) 5 |
| 0x01D0 0148 | DITUDRB0 | Right (odd TDM time slot) channel user data register (DIT mode) 0 |
| 0x01D0 014C | DITUDRB1 | Right (odd TDM time slot) channel user data register (DIT mode) 1 |
| 0x01D0 0150 | DITUDRB2 | Right (odd TDM time slot) channel user data register (DIT mode) 2 |
| 0x01D0 0154 | DITUDRB3 | Right (odd TDM time slot) channel user data register (DIT mode) 3 |
| 0x01D0 0158 | DITUDRB4 | Right (odd TDM time slot) channel user data register (DIT mode) 4 |
| 0x01D0 015C | DITUDRB5 | Right (odd TDM time slot) channel user data register (DIT mode) 5 |
| 0x01D0 0180 | SRCTL0 | Serializer control register 0 |
| 0x01D0 0184 | SRCTL1 | Serializer control register 1 |
| 0x01D0 0188 | SRCTL2 | Serializer control register 2 |
| 0x01D0 018C | SRCTL3 | Serializer control register 3 |
| 0x01D0 0190 | SRCTL4 | Serializer control register 4 |
| 0x01D0 0194 | SRCTL5 | Serializer control register 5 |
| 0x01D0 0198 | SRCTL6 | Serializer control register 6 |
| 0x01D0 019C | SRCTL7 | Serializer control register 7 |
| 0x01D0 01A0 | SRCTL8 | Serializer control register 8 |
| 0x01D0 01A4 | SRCTL9 | Serializer control register 9 |
| 0x01D0 01A8 | SRCTL10 | Serializer control register 10 |
| 0x01D0 01AC | SRCTL11 | Serializer control register 11 |
| 0x01D0 01B0 | SRCTL12 | Serializer control register 12 |
| 0x01D0 01B4 | SRCTL13 | Serializer control register 13 |
| 0x01D0 01B8 | SRCTL14 | Serializer control register 14 |
| 0x01D0 01BC | SRCTL15 | Serializer control register 15 |


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**Table 6-39. McASP Registers Accessed Through Peripheral Configuration Port (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 0200 | XBUF0(1) | Transmit buffer register for serializer 0 |
| 0x01D0 0204 | XBUF1(1) | Transmit buffer register for serializer 1 |
| 0x01D0 0208 | XBUF2(1) | Transmit buffer register for serializer 2 |
| 0x01D0 020C | XBUF3(1) | Transmit buffer register for serializer 3 |
| 0x01D0 0210 | XBUF4(1) | Transmit buffer register for serializer 4 |
| 0x01D0 0214 | XBUF5(1) | Transmit buffer register for serializer 5 |
| 0x01D0 0218 | XBUF6(1) | Transmit buffer register for serializer 6 |
| 0x01D0 021C | XBUF7(1) | Transmit buffer register for serializer 7 |
| 0x01D0 0220 | XBUF8(1) | Transmit buffer register for serializer 8 |
| 0x01D0 0224 | XBUF9(1) | Transmit buffer register for serializer 9 |
| 0x01D0 0228 | XBUF10(1) | Transmit buffer register for serializer 10 |
| 0x01D0 022C | XBUF11(1) | Transmit buffer register for serializer 11 |
| 0x01D0 0230 | XBUF12(1) | Transmit buffer register for serializer 12 |
| 0x01D0 0234 | XBUF13(1) | Transmit buffer register for serializer 13 |
| 0x01D0 0238 | XBUF14(1) | Transmit buffer register for serializer 14 |
| 0x01D0 023C | XBUF15(1) | Transmit buffer register for serializer 15 |
| 0x01D0 0280 | RBUF0(2) | Receive buffer register for serializer 0 |
| 0x01D0 0284 | RBUF1(2) | Receive buffer register for serializer 1 |
| 0x01D0 0288 | RBUF2(2) | Receive buffer register for serializer 2 |
| 0x01D0 028C | RBUF3(2) | Receive buffer register for serializer 3 |
| 0x01D0 0290 | RBUF4(2) | Receive buffer register for serializer 4 |
| 0x01D0 0294 | RBUF5(2) | Receive buffer register for serializer 5 |
| 0x01D0 0298 | RBUF6(2) | Receive buffer register for serializer 6 |
| 0x01D0 029C | RBUF7(2) | Receive buffer register for serializer 7 |
| 0x01D0 02A0 | RBUF8(2) | Receive buffer register for serializer 8 |
| 0x01D0 02A4 | RBUF9(2) | Receive buffer register for serializer 9 |
| 0x01D0 02A8 | RBUF10(2) | Receive buffer register for serializer 10 |
| 0x01D0 02AC | RBUF11(2) | Receive buffer register for serializer 11 |
| 0x01D0 02B0 | RBUF12(2) | Receive buffer register for serializer 12 |
| 0x01D0 02B4 | RBUF13(2) | Receive buffer register for serializer 13 |
| 0x01D0 02B8 | RBUF14(2) | Receive buffer register for serializer 14 |
| 0x01D0 02BC | RBUF15(2) | Receive buffer register for serializer 15 |

(1) Writes to XRBUF originate from peripheral configuration port only when XBUSEL = 1 in XFMT.
(2) Reads from XRBUF originate on peripheral configuration port only when RBUSEL = 1 in RFMT.

**Table 6-40. McASP Registers Accessed Through DMA Port**

| ACCESS TYPE | BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| Read Accesses | 0x01D0 2000 | RBUF | Receive buffer DMA port address. Cycles through receive serializers, skipping over transmit serializers and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Reads from DMA port only if XBUSEL = 0 in XFMT. |
| Write Accesses | 0x01D0 2000 | XBUF | Transmit buffer DMA port address. Cycles through transmit serializers, skipping over receive and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Writes to DMA port only if RBUSEL = 0 in RFMT. |

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**Table 6-41. McASP AFIFO Registers Accessed Through Peripheral Configuration Port**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 1000 | AFIFOREV | AFIFO revision identification register |
| 0x01D0 1010 | WFIFOCTL | Write FIFO control register |
| 0x01D0 1014 | WFIFOSTS | Write FIFO status register |
| 0x01D0 1018 | RFIFOCTL | Read FIFO control register |
| 0x01D0 101C | RFIFOSTS | Read FIFO status register |

## *6.13.2 McASP Electrical Data/Timing*

### 6.13.2.1 Multichannel Audio Serial Port 0 (McASP0) Timing

Table 6-42 and Table 6-44 assume testing over recommended operating conditions (see Figure 6-27 and Figure 6-28).

**Table 6-42. Timing Requirements for McASP0 (1.2V, 1.1V)(1)(2)**

| NO. | | | | 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 25 | | 28 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 12.5 | | 14 | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | AHCLKR/X ext | 25(3) | | 28(3) | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/W high or low | AHCLKR/X ext | 12.5 | | 14 | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, AFSR/X input to ACLKR/X(4) | AHCLKR/X int | 11.5 | | 12 | | ns |
| | | | AHCLKR/X ext input | 4 | | 5 | | ns |
| | | | AHCLKR/X ext output | 4 | | 5 | | ns |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, AFSR/X input after ACLKR/X(4) | AHCLKR/X int | -1 | | -2 | | ns |
| | | | AHCLKR/X ext input | 1 | | 1 | | ns |
| | | | AHCLKR/X ext output | 1 | | 1 | | ns |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, AXR0[n] input to ACLKR/X(4)(5) | AHCLKR/X int | 11.5 | | 12 | | ns |
| | | | AHCLKR/X ext | 4 | | 5 | | ns |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, AXR0[n] input after ACLKR/X(4)(5) | AHCLKR/X int | -1 | | -2 | | ns |
| | | | AHCLKR/X ext input | 3 | | 4 | | ns |
| | | | AHCLKR/X ext output | 3 | | 4 | | ns |

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) This timing is limited by the timing shown or 2P, whichever is greater.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0


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**Table 6-43. Timing Requirements for McASP0 (1.0V)(1)(2)**

| NO. | | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 35 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 17.5 | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | AHCLKR/X ext | 35(3) | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/W high or low | AHCLKR/X ext | 17.5 | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, AFSR/X input to ACLKR/X(4) | AHCLKR/X int | 16 | | ns |
| | | | AHCLKR/X ext input | 5.5 | | ns |
| | | | AHCLKR/X ext output | 5.5 | | ns |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, AFSR/X input after ACLKR/X(4) | AHCLKR/X int | -2 | | ns |
| | | | AHCLKR/X ext input | 1 | | ns |
| | | | AHCLKR/X ext output | 1 | | ns |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, AXR0[n] input to ACLKR/X(4)(5) | AHCLKR/X int | 16 | | ns |
| | | | AHCLKR/X ext | 5.5 | | ns |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, AXR0[n] input after ACLKR/X(4)(5) | AHCLKR/X int | -2 | | ns |
| | | | AHCLKR/X ext input | 5 | | ns |
| | | | AHCLKR/X ext output | 5 | | ns |

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) This timing is limited by the timing shown or 2P, whichever is greater.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0

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### Table 6-44. Switching Characteristics for McASP0 (1.2V, 1.1V)(1)

| NO. | PARAMETER | | | 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 25 | | 28 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | AH – 2.5(2) | | AH – 2.5(2) | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | ACLKR/X int | 25(3)(4) | | 28(3)(4) | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X int | A – 2.5(5) | | A – 2.5(5) | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid(6) | ACLKR/X int | -1 | 6 | -1 | 8 | ns |
| | | | ACLKR/X ext input | 2 | 13.5 | 2 | 14.5 | ns |
| | | | ACLKR/X ext output | 2 | 13.5 | 2 | 14.5 | ns |
| 14 | $t_{d(ACLKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKR/X int | -1 | 6 | -1 | 8 | ns |
| | | | ACLKR/X ext input | 2 | 13.5 | 2 | 15 | ns |
| | | | ACLKR/X ext output | 2 | 13.5 | 2 | 15 | ns |
| 15 | $t_{dis(ACLKX-AXRHZ)}$ | Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit | ACLKR/X int | 0 | 6 | 0 | 8 | ns |
| | | | ACLKR/X ext | 2 | 13.5 | 2 | 15 | ns |

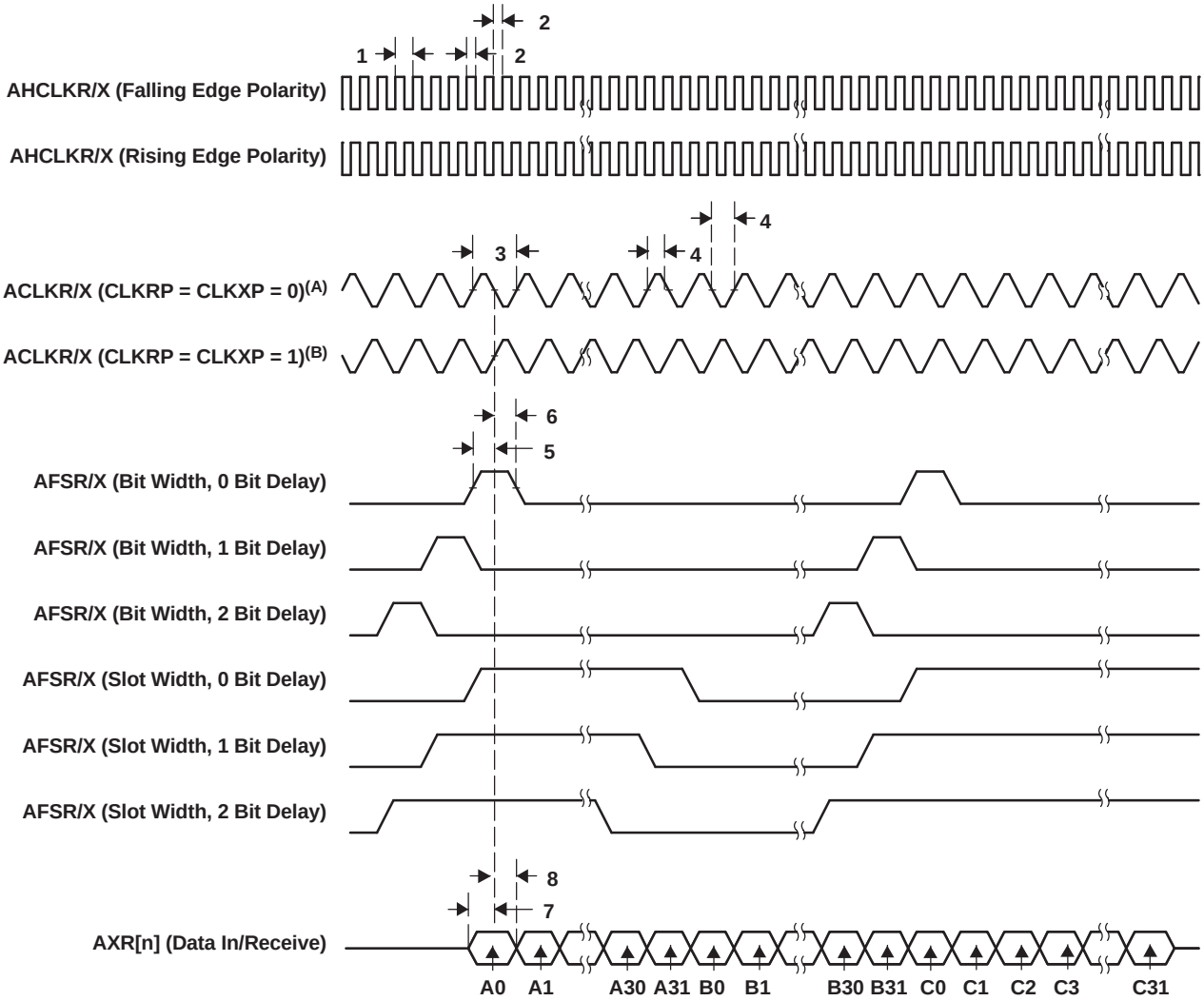
(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) P = SYSCLK2 period
(4) This timing is limited by the timing shown or 2P, whichever is greater.
(5) A = (ACLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(6) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0

### Table 6-45. Switching Characteristics for McASP0 (1.0V)(1)

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 35 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | AH – 2.5(2) | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | ACLKR/X int | 35(3)(4) | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X int | A – 2.5(5) | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid(6) | ACLKR/X int | -0.5 | 10 | ns |
| | | | ACLKR/X ext input | 2 | 19 | ns |
| | | | ACLKR/X ext output | 2 | 19 | ns |
| 14 | $t_{d(ACLKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKR/X int | -0.5 | 10 | ns |
| | | | ACLKR/X ext input | 2 | 19 | ns |
| | | | ACLKR/X ext output | 2 | 19 | ns |
| 15 | $t_{dis(ACLKX-AXRHZ)}$ | Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit | ACLKR/X int | 0 | 10 | ns |
| | | | ACLKR/X ext | 2 | 19 | ns |

(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) P = SYSCLK2 period
(4) This timing is limited by the timing shown or 2P, whichever is greater.
(5) A = (ACLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(6) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0

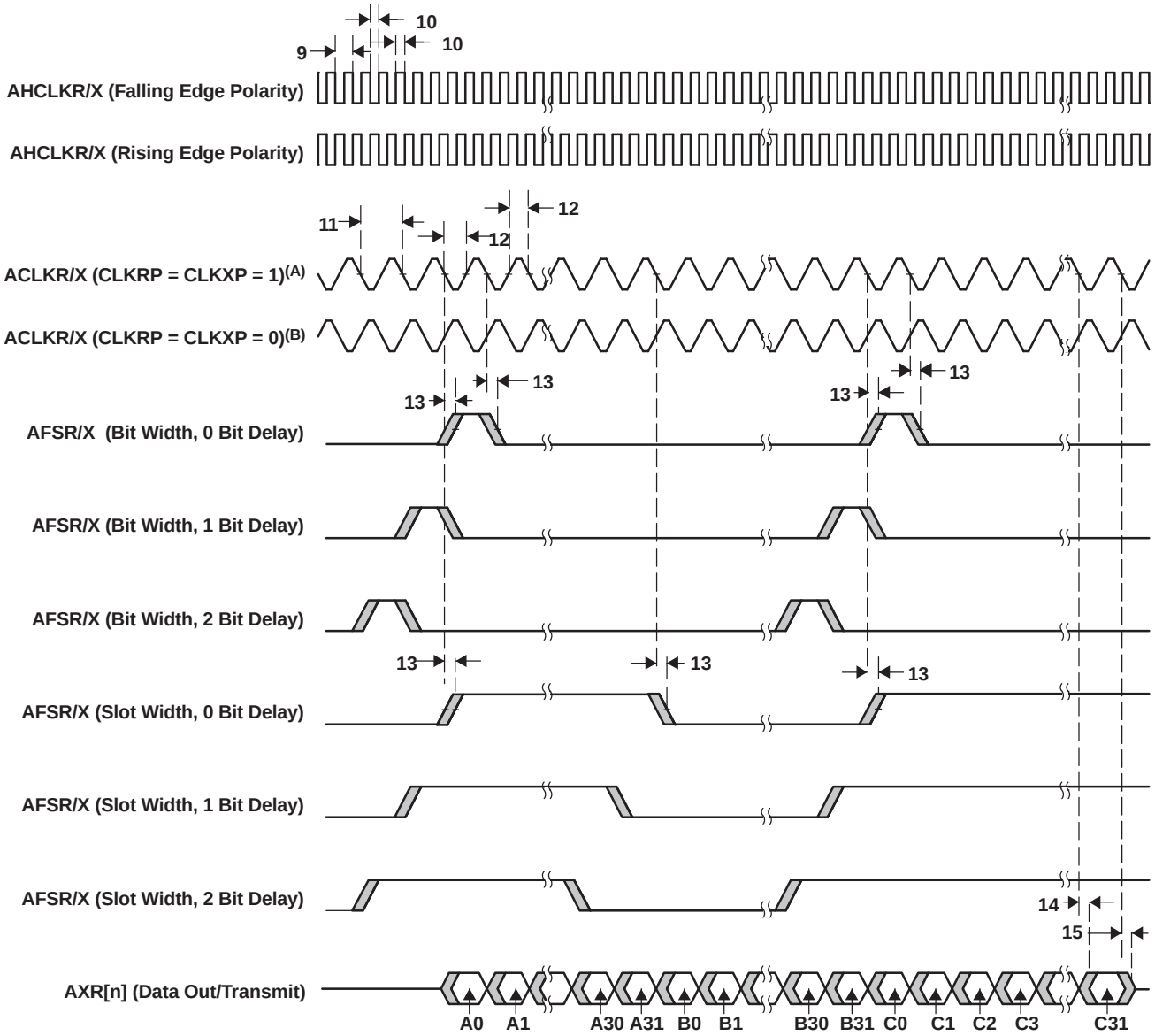

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A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**Figure 6-27. McASP Input Timings**




A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**Figure 6-28. McASP Output Timings**


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## 6.14 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer
- Transmit & Receive FIFO Buffers allow the McBSP to operate at a higher sample rate by making it more tolerant to DMA latency

If internal clock source is used, the CLKGDV field of the Sample Rate Generator Register (SRGR) must always be set to a value of 1 or greater.

### *6.14.1 McBSP Peripheral Register Description(s)*

**Table 6-46. McBSP/FIFO Registers**

| McBSP1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| **McBSP Registers** | | |
| 0x01D1 1000 | DRR | McBSP Data Receive Register (read-only) |
| 0x01D1 1004 | DXR | McBSP Data Transmit Register |
| 0x01D1 1008 | SPCR | McBSP Serial Port Control Register |
| 0x01D1 100C | RCR | McBSP Receive Control Register |
| 0x01D1 1010 | XCR | McBSP Transmit Control Register |
| 0x01D1 1014 | SRGR | McBSP Sample Rate Generator register |
| 0x01D1 1018 | MCR | McBSP Multichannel Control Register |
| 0x01D1 101C | RCERE0 | McBSP Enhanced Receive Channel Enable Register 0 Partition A/B |
| 0x01D1 1020 | XCERE0 | McBSP Enhanced Transmit Channel Enable Register 0 Partition A/B |
| 0x01D1 1024 | PCR | McBSP Pin Control Register |
| 0x01D1 1028 | RCERE1 | McBSP Enhanced Receive Channel Enable Register 1 Partition C/D |
| 0x01D1 102C | XCERE1 | McBSP Enhanced Transmit Channel Enable Register 1 Partition C/D |
| 0x01D1 1030 | RCERE2 | McBSP Enhanced Receive Channel Enable Register 2 Partition E/F |
| 0x01D1 1034 | XCERE2 | McBSP Enhanced Transmit Channel Enable Register 2 Partition E/F |
| 0x01D1 1038 | RCERE3 | McBSP Enhanced Receive Channel Enable Register 3 Partition G/H |
| 0x01D1 103C | XCERE3 | McBSP Enhanced Transmit Channel Enable Register 3 Partition G/H |
| **McBSP FIFO Control and Status Registers** | | |
| 0x01D1 1800 | BFIFOREV | BFIFO Revision Identification Register |
| 0x01D1 1810 | WFIFOCTL | Write FIFO Control Register |
| 0x01D1 1814 | WFIFOSTS | Write FIFO Status Register |
| 0x01D1 1818 | RFIFOCTL | Read FIFO Control Register |
| 0x01D1 181C | RFIFOSTS | Read FIFO Status Register |
| **McBSP FIFO Data Registers** | | |
| 0x01F1 1000 | RBUF | McBSP FIFO Receive Buffer |
| 0x01F1 1000 | XBUF | McBSP FIFO Transmit Buffer |

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### 6.14.2 McBSP Electrical Data/Timing

The following assume testing over recommended operating conditions.

#### 6.14.2.1 Multichannel Buffered Serial Port (McBSP) Timing

**Table 6-47. Timing Requirements for McBSP1 [1.2V, 1.1V](1) (see Figure 6-29)**

| NO. | | | | 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P or 20(2)(3) | | 2P or 25(2) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P - 1 | | P - 1(4) | | ns |
| 5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 15 | | 18 | | ns |
| | | | CLKR ext | 5 | | 5 | | |
| 6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | 6 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| 7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 15 | | 18 | | ns |
| | | | CLKR ext | 5 | | 5 | | |
| 8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | 3 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| 10 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 15 | | 18 | | ns |
| | | | CLKX ext | 5 | | 5 | | |
| 11 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 6 | | 6 | | ns |
| | | | CLKX ext | 3 | | 3 | | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = ASYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

**Table 6-48. Timing Requirements for McBSP1 [1.0V](1) (see Figure 6-29)**

| NO. | | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P or 26.6(2)(3) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P - 1(4) | | ns |
| 5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 21 | | ns |
| | | | CLKR ext | 10 | | |
| 6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | ns |
| | | | CLKR ext | 3 | | |
| 7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 21 | | ns |
| | | | CLKR ext | 10 | | |
| 8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | ns |
| | | | CLKR ext | 3 | | |
| 10 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 21 | | ns |
| | | | CLKX ext | 10 | | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = ASYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.


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**Table 6-48. Timing Requirements for McBSP1 [1.0V](1) (see Figure 6-29) (continued)**

| NO. | | | 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 11 | $t_{h(CKXL-FXH)}$ Hold time, external FSX high after CLKX low | CLKX int | 6 | | ns |
| | | CLKX ext | 3 | | |

**Table 6-49. Switching Characteristics for McBSP1 [1.2V, 1.1V](1) (2) (see Figure 6-29)**

| NO. | PARAMETER | | | 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | 0.5 | 16.5 | 1.5 | 18 | ns |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P or 20(3)(4) | | 2P or 25(3) (4) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C - 2(5) | C + 2(5) | C - 2(5) | C + 2(5) | ns |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | -4 | 6.5 | -4 | 13 | ns |
| | | | CLKR ext | 1 | 16.5 | 1 | 18 | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | -4 | 6.5 | -4 | 13 | ns |
| | | | CLKX ext | 1 | 16.5 | 1 | 18 | |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | -4 | 6.5 | -4 | 13 | ns |
| | | | CLKX ext | -2 | 16.5 | -2 | 18 | |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | -4 + D1(6) | 6.5 + D2(6) | -4 + D1(6) | 13 + D2(6) | ns |
| | | | CLKX ext | 1 + D1(6) | 16.5 + D2(6) | 1 + D1(6) | 18 + D2(6) | |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX int | -4(7) | 6.5(7) | -4(7) | 13(7) | ns |
| | | | FSX ext | -2(7) | 16.5(7) | -2(7) | 18 | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) P = ASYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(4) Use whichever value is greater.
(5) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(6) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(7) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

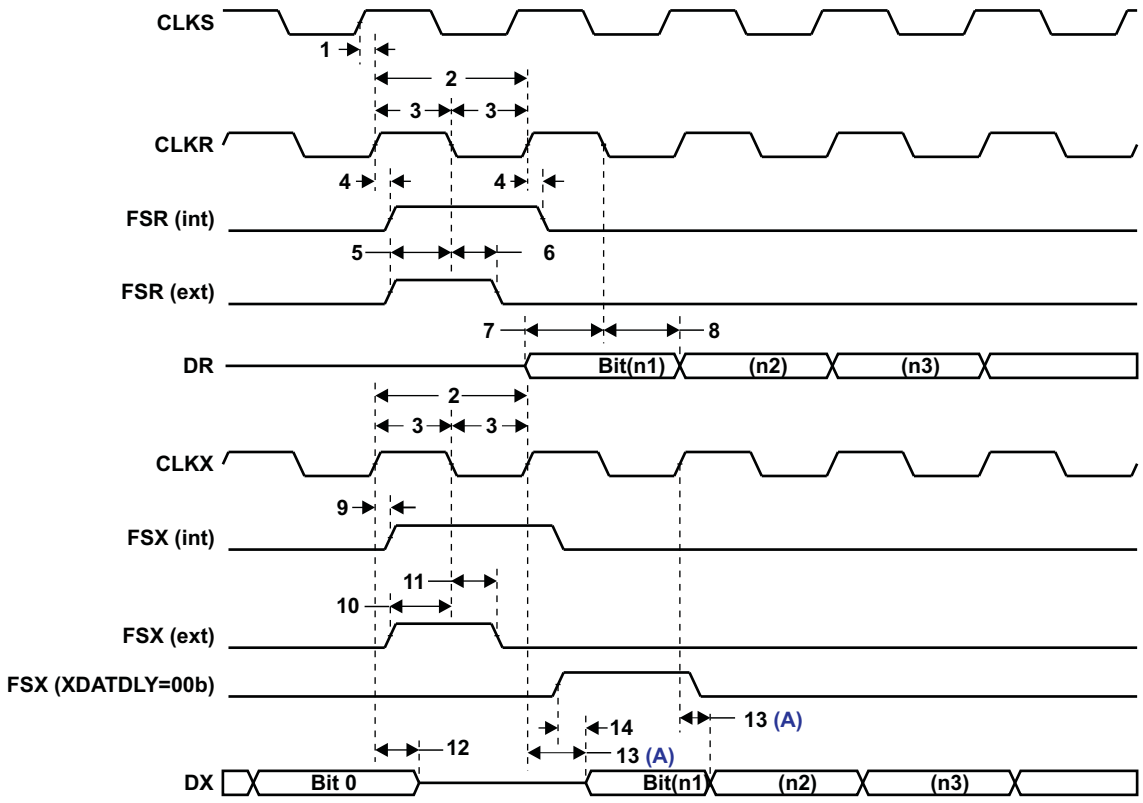

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**Table 6-50. Switching Characteristics for McBSP1 [1.0V](1) (2) (see Figure 6-29)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | 1.5 | 23 | ns |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P or 26.6(3)(4)(5) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C - 2(6) | C + 2(6) | ns |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | -4 | 13 | ns |
| | | | CLKR ext | 2.5 | 23 | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | -4 | 13 | ns |
| | | | CLKX ext | 1 | 23 | |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | -4 | 13 | ns |
| | | | CLKX ext | -2 | 23 | |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | -4 + D1 | 13 + D2(7) | ns |
| | | | CLKX ext | 1 + D1(7) | 23 + D2(7) | |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid | FSX int | -4(8) | 13(8) | ns |
| | | ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX ext | -2(8) | 23(8) | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = ASYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

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A. No. 13 applies to the first data bit only when XDATDLY ≠ 0.

**Figure 6-29. McBSP Timing**

**Table 6-51. Timing Requirements for McBSP1 FSR When GSYNC = 1 (see Figure 6-30)**

| NO. | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(FRH-CKSH)}$ | Setup time, FSR high before CLKS high | 5 | | 5 | | 10 | | ns |
| 2 | $t_{h(CKSH-FRH)}$ | Hold time, FSR high after CLKS high | 4 | | 4 | | 4 | | ns |

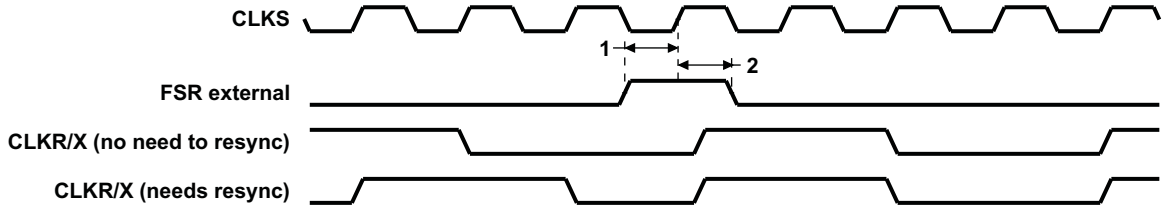



**Figure 6-30. FSR Timing When GSYNC = 1**


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## 6.15 Serial Peripheral Interface Ports (SPI1)

Figure 6-31 is a block diagram of the SPI module, which is a simple shift register and buffer plus control logic. Data is written to the shift register before transmission occurs and is read from the buffer at the end of transmission. The SPI can operate either as a master, in which case, it initiates a transfer and drives the SPIx_CLK pin, or as a slave. Four clock phase and polarity options are supported as well as many data formatting options.

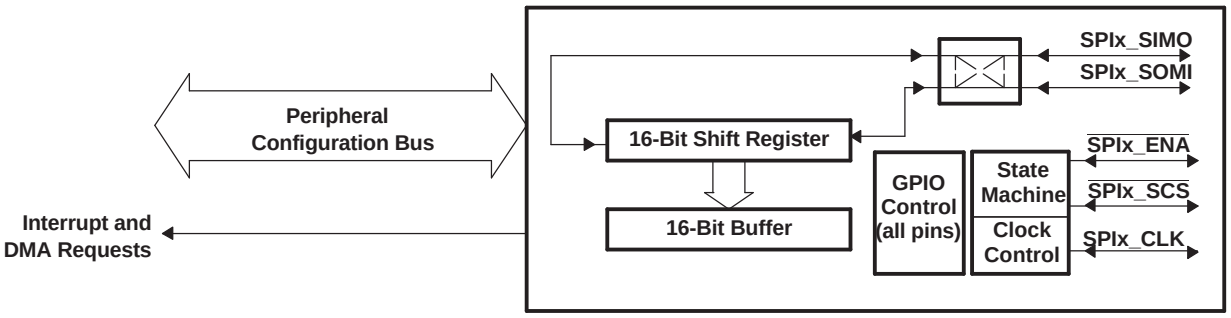



**Figure 6-31. Block Diagram of SPI Module**

The SPI supports 3-, 4-, and 5-pin operation with three basic pins (SPIx_CLK, SPIx_SIMO, and SPIx_SOMI) and two optional pins ($\overline{\text{SPIx_SCS}}$, $\overline{\text{SPIx_ENA}}$).

The optional $\overline{\text{SPIx_SCS}}$ (Slave Chip Select) pin is most useful to enable in slave mode when there are other slave devices on the same SPI port. The device will only shift data and drive the SPIx_SOMI pin when $\overline{\text{SPIx_SCS}}$ is held low.

In slave mode, $\overline{\text{SPIx_ENA}}$ is an optional output. The $\overline{\text{SPIx_ENA}}$ output provides the status of the internal transmit buffer (SPIDAT0/1 registers). In four-pin mode with the enable option, $\overline{\text{SPIx_ENA}}$ is asserted only when the transmit buffer is full, indicating that the slave is ready to begin another transfer. In five-pin mode, the $\overline{\text{SPIx_ENA}}$ is additionally qualified by $\overline{\text{SPIx_SCS}}$ being asserted. This allows a single handshake line to be shared by multiple slaves on the same SPI bus.

In master mode, the $\overline{\text{SPIx_ENA}}$ pin is an optional input and the master can be configured to delay the start of the next transfer until the slave asserts $\overline{\text{SPIx_ENA}}$. The addition of this handshake signal simplifies SPI communications and, on average, increases SPI bus throughput since the master does not need to delay each transfer long enough to allow for the worst-case latency of the slave device. Instead, each transfer can begin as soon as both the master and slave have actually serviced the previous SPI transfer.

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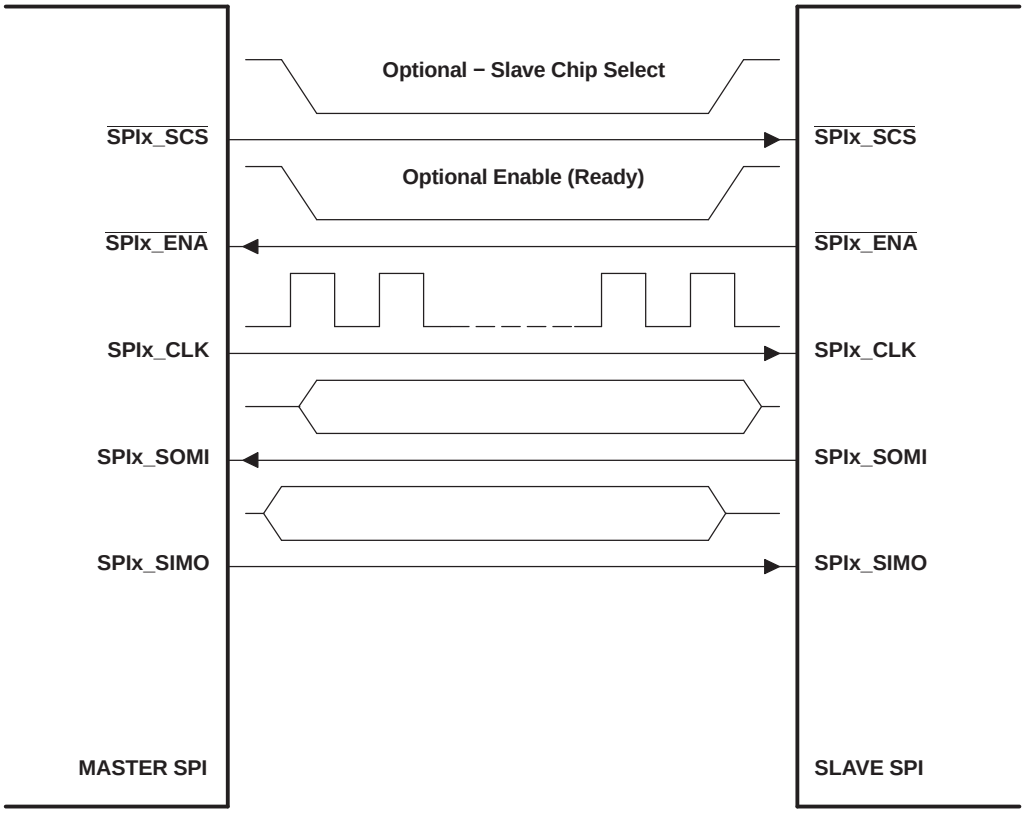



**Figure 6-32. Illustration of SPI Master-to-SPI Slave Connection**


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### 6.15.1 SPI Peripheral Registers Description(s)

Table 6-52is a list of the SPI registers.

**Table 6-52. SPIx Configuration Registers**

| SPI1 BYTE ADDRESS | REGISTER NAME | DESCRIPTION |
|---|---|---|
| 0x01F0 E000 | SPIGCR0 | Global Control Register 0 |
| 0x01F0 E004 | SPIGCR1 | Global Control Register 1 |
| 0x01F0 E008 | SPIINT0 | Interrupt Register |
| 0x01F0 E00C | SPILVL | Interrupt Level Register |
| 0x01F0 E010 | SPIFLG | Flag Register |
| 0x01F0 E014 | SPIPC0 | Pin Control Register 0 (Pin Function) |
| 0x01F0 E018 | SPIPC1 | Pin Control Register 1 (Pin Direction) |
| 0x01F0 E01C | SPIPC2 | Pin Control Register 2 (Pin Data In) |
| 0x01F0 E020 | SPIPC3 | Pin Control Register 3 (Pin Data Out) |
| 0x01F0 E024 | SPIPC4 | Pin Control Register 4 (Pin Data Set) |
| 0x01F0 E028 | SPIPC5 | Pin Control Register 5 (Pin Data Clear) |
| 0x01F0 E02C | Reserved | Reserved - Do not write to this register |
| 0x01F0 E030 | Reserved | Reserved - Do not write to this register |
| 0x01F0 E034 | Reserved | Reserved - Do not write to this register |
| 0x01F0 E038 | SPIDAT0 | Shift Register 0 (without format select) |
| 0x01F0 E03C | SPIDAT1 | Shift Register 1 (with format select) |
| 0x01F0 E040 | SPIBUF | Buffer Register |
| 0x01F0 E044 | SPIEMU | Emulation Register |
| 0x01F0 E048 | SPIDELAY | Delay Register |
| 0x01F0 E04C | SPIDEF | Default Chip Select Register |
| 0x01F0 E050 | SPIFMT0 | Format Register 0 |
| 0x01F0 E054 | SPIFMT1 | Format Register 1 |
| 0x01F0 E058 | SPIFMT2 | Format Register 2 |
| 0x01F0 E05C | SPIFMT3 | Format Register 3 |
| 0x01F0 E060 | INTVEC0 | Interrupt Vector for SPI INT0 |
| 0x01F0 E064 | INTVEC1 | Interrupt Vector for SPI INT1 |

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## 6.15.2 SPI Electrical Data/Timing

### 6.15.2.1 Serial Peripheral Interface (SPI) Timing

The following tables and timing diagrams assume testing over recommended operating conditions.

**Table 6-53. General Timing Requirements for SPI1 Master Modes(1)**

| NO. | | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPC)M}$ | Cycle Time, SPI1_CLK, All Master Modes | | 20(2) | 256P | 30(2) | 256P | 40(2) | 256P | ns |
| 2 | $t_{w(SPCH)M}$ | Pulse Width High, SPI1_CLK, All Master Modes | | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | ns |
| 3 | $t_{w(SPCL)M}$ | Pulse Width Low, SPI1_CLK, All Master Modes | | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | ns |
| 4 | $t_{d(SIMO_SPC)M}$ | Delay, initial data bit valid on SPI1_SIMO to initial edge on SPI1_CLK(3) | Polarity = 0, Phase = 0, to SPI1_CLK rising | | 5 | | 5 | | 6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | | -0.5M+5 | | -0.5M+5 | | -0.5M+6 | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | | -0.5M+5 | | -0.5M+5 | | -0.5M+6 | |
| 5 | $t_{d(SPC_SIMO)M}$ | Delay, subsequent bits valid on SPI1_SIMO after transmit edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK rising | | 5 | | 5 | | 6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | 5 | | 5 | | 6 | |
| 6 | $t_{oh(SPC_SIMO)M}$ | Output hold time, SPI1_SIMO valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| 7 | $t_{su(SOMI_SPC)M}$ | Input Setup Time, SPI1_SOMI valid before receive edge of SPI1_CLK | Polarity = 0, Phase = 0, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | |
| 8 | $t_{ih(SPC_SOMI)M}$ | Input Hold Time, SPI1_SOMI valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 4 | | 5 | | 6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 4 | | 5 | | 6 | | |

(1) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(2) This timing is limited by the timing shown or 3P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI1_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI1_SOMI.


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**Table 6-54. General Timing Requirements for SPI1 Slave Modes(1)**

| NO. | | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 9 | $t_{c(SPC)S}$ | Cycle Time, SPI1_CLK, All Slave Modes | | 40(2) | | 50(2) | | 60(2) | | ns |
| 10 | $t_{w(SPCH)S}$ | Pulse Width High, SPI1_CLK, All Slave Modes | | 18 | | 22 | | 27 | | ns |
| 11 | $t_{w(SPCL)S}$ | Pulse Width Low, SPI1_CLK, All Slave Modes | | 18 | | 22 | | 27 | | ns |
| 12 | $t_{su(SOMI_SPC)S}$ | Setup time, transmit data written to SPI before initial clock edge from master.(3)(4) | Polarity = 0, Phase = 0, to SPI1_CLK rising | 2P | | 2P | | 2P | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 2P | | 2P | | 2P | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 2P | | 2P | | 2P | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 2P | | 2P | | 2P | | |
| 13 | $t_{d(SPC_SOMI)S}$ | Delay, subsequent bits valid on SPI1_SOMI after transmit edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK rising | | 15 | | 17 | | 19 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | 15 | | 17 | | 19 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK falling | | 15 | | 17 | | 19 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | 15 | | 17 | | 19 | |
| 14 | $t_{oh(SPC_SOMI)S}$ | Output hold time, SPI1_SOMI valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | |
| 15 | $t_{su(SIMO_SPC)S}$ | Input Setup Time, SPI1_SIMO valid before receive edge of SPI1_CLK | Polarity = 0, Phase = 0, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | |
| 16 | $t_{ih(SPC_SIMO)S}$ | Input Hold Time, SPI1_SIMO valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 4 | | 5 | | 6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 4 | | 5 | | 6 | | |

(1) P = SYSCLK2 period; S = $t_{c(SPC)S}$ (SPI slave bit clock period)
(2) This timing is limited by the timing shown or 3P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI1_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI1_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by the CPU.

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**Table 6-55. Additional[1] SPI1 Master Timings, 4-Pin Enable Option[2][3]**

| NO. | PARAMETER | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 17 | $t_{d(EN\ A_SPC)M}$ | Delay from slave assertion of SPI1_ENA active to first SPI1_CLK from master.[4] | Polarity = 0, Phase = 0, to SPI1_CLK rising | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| 18 | $t_{d(SPC_ENA)M}$ | Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[5] | Polarity = 0, Phase = 0, from SPI1_CLK falling | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | P+5 | | P+5 | | P+6 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | P+5 | | P+5 | | P+6 | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-53).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_ENA assertion.
(5) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.

**Table 6-56. Additional[1] SPI1 Master Timings, 4-Pin Chip Select Option[2] [3]**

| NO. | PARAMETER | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 19 | $t_{d(SCS_SPC)M}$ | Delay from SPI1_SCS active to first SPI1_CLK[4] [5] | Polarity = 0, Phase = 0, to SPI1_CLK rising | 2P-1 | | 2P-5 | | 2P-6 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 2P-1 | | 2P-5 | | 2P-6 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |
| 20 | $t_{d(SPC_SCS)M}$ | Delay from final SPI1_CLK edge to master deasserting SPI1_SCS[6] [7] | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P-1 | | P-5 | | P-6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P-1 | | P-5 | | P-6 | | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-53).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(5) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].


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**Table 6-57. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3]**

| NO. | PARAMETER | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 18 | $t_{d(SPC_ENA)M}$ | Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[4] | Polarity = 0, Phase = 0, from SPI1_CLK falling | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | P+5 | | P+5 | | P+6 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | P+5 | | P+5 | | P+6 | |
| 20 | $t_{d(SPC_SCS)M}$ | Delay from final SPI1_CLK edge to master deasserting SPI1_SCS [5][6] | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P-1 | | P-5 | | P-6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P-1 | | P-5 | | P-6 | | |
| 21 | $t_{d(SCSL_ENAL)M}$ | Max delay for slave SPI to drive SPI1_ENA valid after master asserts SPI1_SCS to delay the master from beginning the next transfer, | | | C2TDELAY+P | | C2TDELAY+P | | C2TDELAY+P | ns |
| 22 | $t_{d(SCS_SPC)M}$ | Delay from SPI1_SCS active to first SPI1_CLK[7][8][9] | Polarity = 0, Phase = 0, to SPI1_CLK rising | 2P-1 | | 2P-5 | | 2P-6 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 2P-1 | | 2P-5 | | 2P-6 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 6-54).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.
(5) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(6) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
(7) If SPI1_ENA is asserted immediately such that the transmission is not delayed by SPI1_ENA.
(8) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(9) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].

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**Table 6-57. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3] (continued)**

| NO. | PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 23 | $t_{d(ENA_SPC)M}$ | Delay from assertion of $\overline{SPI1_ENA}$ low to first SPI1_CLK edge.[10] | Polarity = 0, Phase = 0, to SPI1_CLK rising | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 3P+5 | | 3P+5 | | 3P+6 | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |

(10) If $\overline{SPI1_ENA}$ was initially deasserted high and SPI1_CLK is delayed.

**Table 6-58. Additional[1] SPI1 Slave Timings, 4-Pin Enable Option[2][3]**

| NO. | PARAMETER | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 24 | $t_{d(SPC_ENAH)S}$ | Delay from final SPI1_CLK edge to slave deasserting $\overline{SPI1_ENA}$. | Polarity = 0, Phase = 0, from SPI1_CLK falling | 1.5P-3 | 2.5P+15 | 1.5P-10 | 2.5P+17 | 1.5P-12 | 2.5P+19 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | –0.5M+1.5P-3 | –0.5M+2.5P+15 | –0.5M+1.5P-10 | –0.5M+2.5P+17 | –0.5M+1.5P-12 | –0.5M+2.5P+19 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 1.5P-3 | 2.5P+15 | 1.5P-10 | 2.5P+17 | 1.5P-12 | 2.5P+19 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | –0.5M+1.5P-3 | –0.5M+2.5P+15 | –0.5M+1.5P-10 | –0.5M+2.5P+17 | –0.5M+1.5P-12 | –0.5M+2.5P+19 | |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-54).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.


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### Table 6-59. Additional(1) SPI1 Slave Timings, 4-Pin Chip Select Option(2)(3)

| NO. | PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 25 | $t_{d(SCSL_SPC)S}$ | Required delay from $\overline{SPI1_SCS}$ asserted at slave to first SPI1_CLK edge at slave. | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | $t_{d(SPC_SCSH)S}$ | Required delay from final SPI1_CLK edge before $\overline{SPI1_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | ns |
| | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P+4 | | P+5 | | P+6 | | |
| | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | |
| | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P+4 | | P+5 | | P+6 | | |
| 27 | $t_{ena(SCSL_SOMI)S}$ | Delay from master asserting $\overline{SPI1_SCS}$ to slave driving SPI1_SOMI valid | | P+15 | | P+17 | | P+19 | ns |
| 28 | $t_{dis(SCSH_SOMI)S}$ | Delay from master deasserting $\overline{SPI1_SCS}$ to slave 3-stating SPI1_SOMI | | P+15 | | P+17 | | P+19 | ns |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-54).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

### Table 6-60. Additional(1) SPI1 Slave Timings, 5-Pin Option(2)(3)

| NO. | PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 25 | $t_{d(SCSL_SPC)S}$ | Required delay from $\overline{SPI1_SCS}$ asserted at slave to first SPI1_CLK edge at slave. | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | $t_{d(SPC_SCSH)S}$ | Required delay from final SPI1_CLK edge before $\overline{SPI1_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | ns |
| | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P+4 | | P+5 | | P+6 | | |
| | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | |
| | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P+4 | | P+5 | | P+6 | | |
| 27 | $t_{ena(SCSL_SOMI)S}$ | Delay from master asserting $\overline{SPI1_SCS}$ to slave driving SPI1_SOMI valid | | P+15 | | P+17 | | P+19 | ns |
| 28 | $t_{dis(SCSH_SOMI)S}$ | Delay from master deasserting $\overline{SPI1_SCS}$ to slave 3-stating SPI1_SOMI | | P+15 | | P+17 | | P+19 | ns |
| 29 | $t_{ena(SCSL_ENA)S}$ | Delay from master deasserting $\overline{SPI1_SCS}$ to slave driving $\overline{SPI1_ENA}$ valid | | 15 | | 17 | | 19 | ns |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 6-54).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

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**Table 6-60. Additional[1] SPI1 Slave Timings, 5-Pin Option[2][3] (continued)**

| NO. | PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 30 | $t_{dis(SPC_ENA)S}$ | Delay from final clock receive edge on SPI1_CLK to slave 3-stating or driving high $\overline{SPI1_ENA}$.[4] Polarity = 0, Phase = 0, from SPI1_CLK falling | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | ns |
| | | Polarity = 0, Phase = 1, from SPI1_CLK rising | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | |
| | | Polarity = 1, Phase = 0, from SPI1_CLK rising | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | |
| | | Polarity = 1, Phase = 1, from SPI1_CLK falling | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | |

(4) $\overline{SPI1_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.


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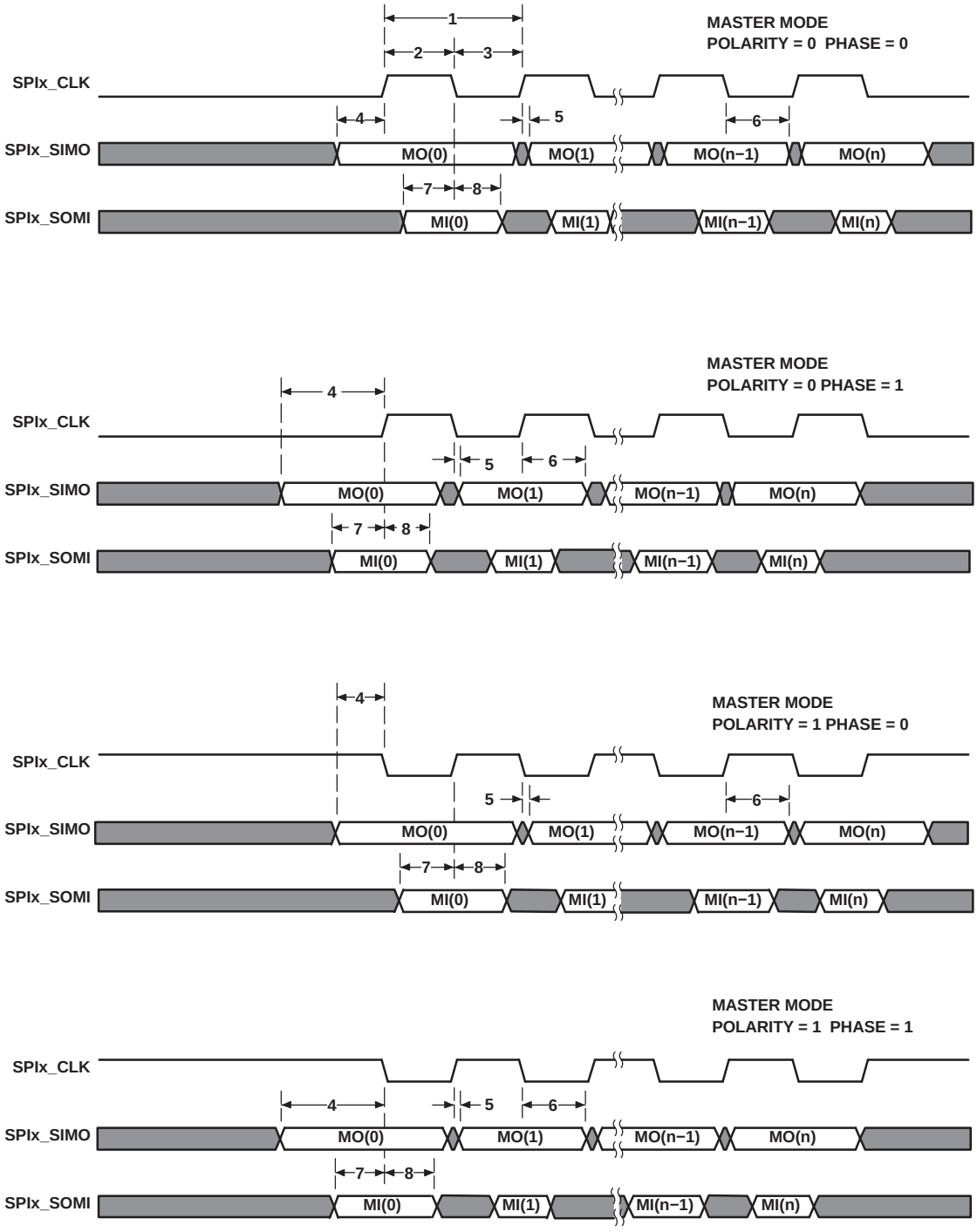



**Figure 6-33. SPI Timings—Master Mode**

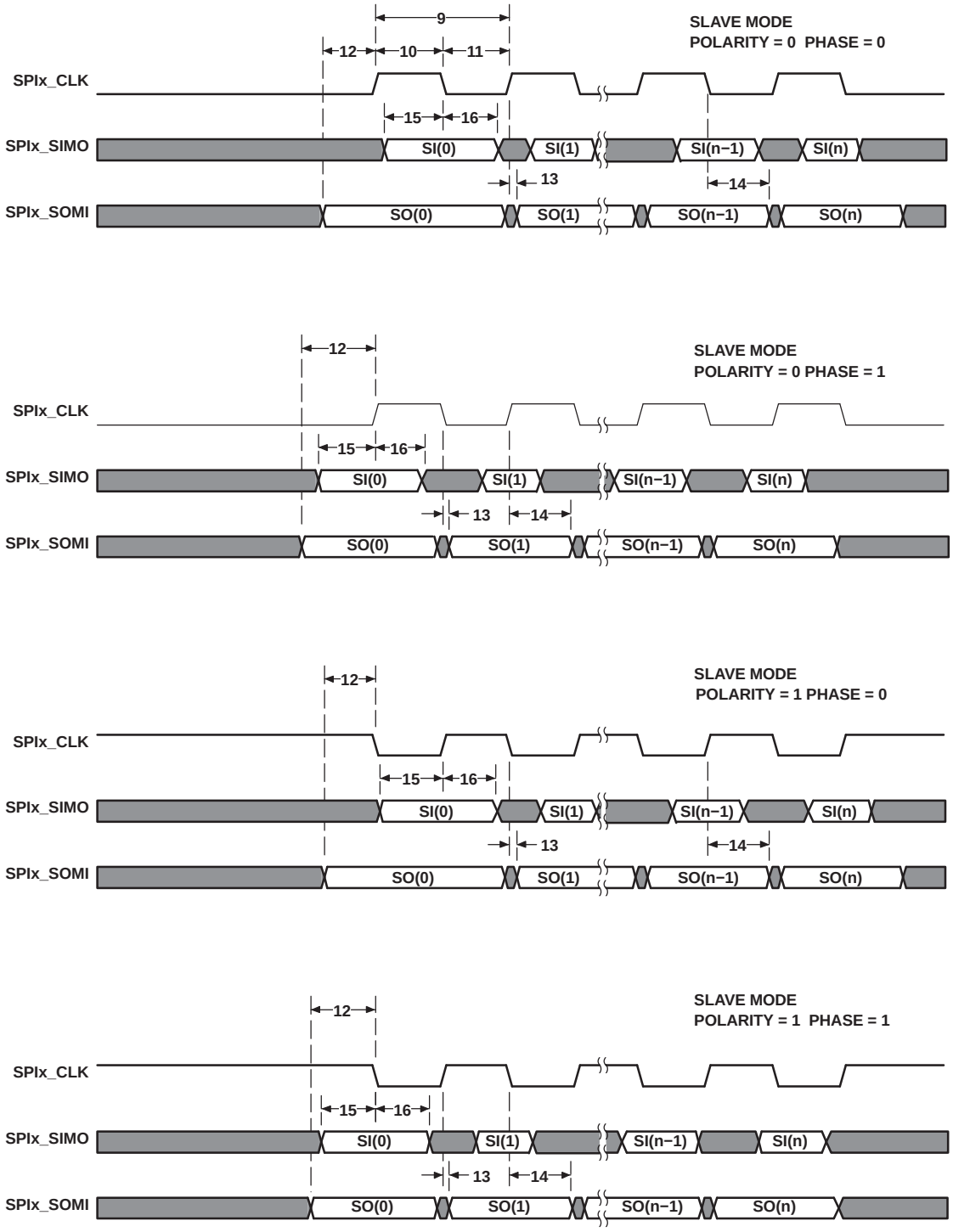
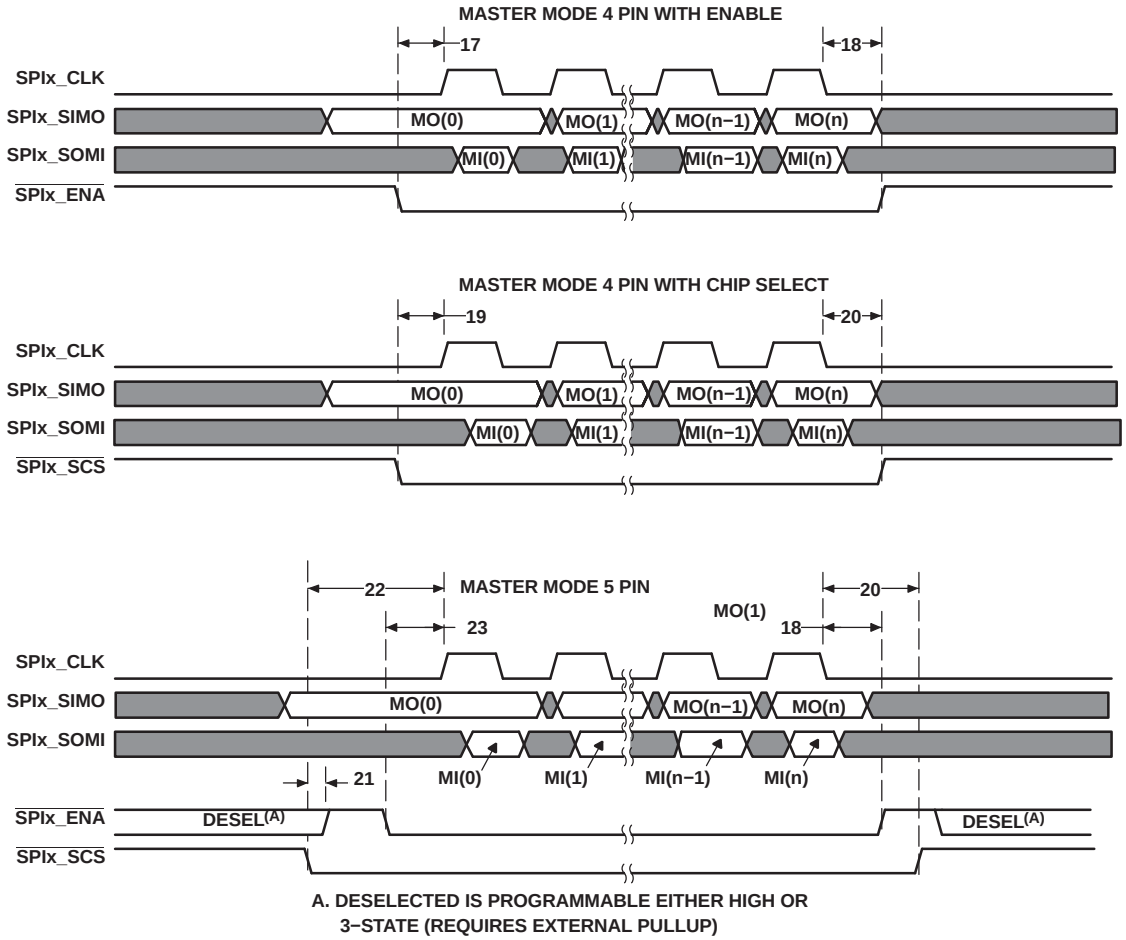



**Figure 6-34. SPI Timings—Slave Mode**


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A. DESELECTED IS PROGRAMMABLE EITHER HIGH OR 3−STATE (REQUIRES EXTERNAL PULLUP)

**Figure 6-35. SPI Timings—Master Mode (4-Pin and 5-Pin)**

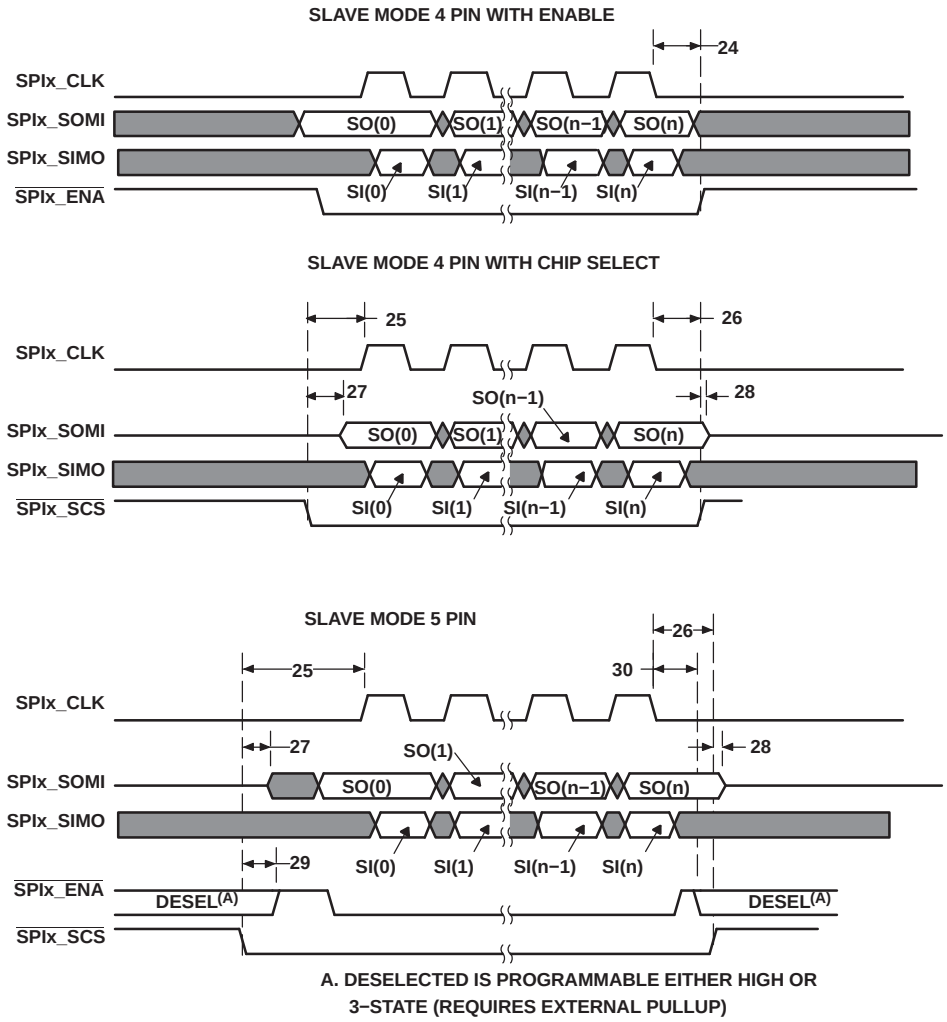



**Figure 6-36. SPI Timings—Slave Mode (4-Pin and 5-Pin)**


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## 6.16 Inter-Integrated Circuit Serial Ports (I2C)

### 6.16.1 I2C Device-Specific Information

I2C port supports:

- Compatible with Philips® I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- General-Purpose I/O Capability if not used as I2C

Figure 6-37 is block diagram of the device I2C Module.

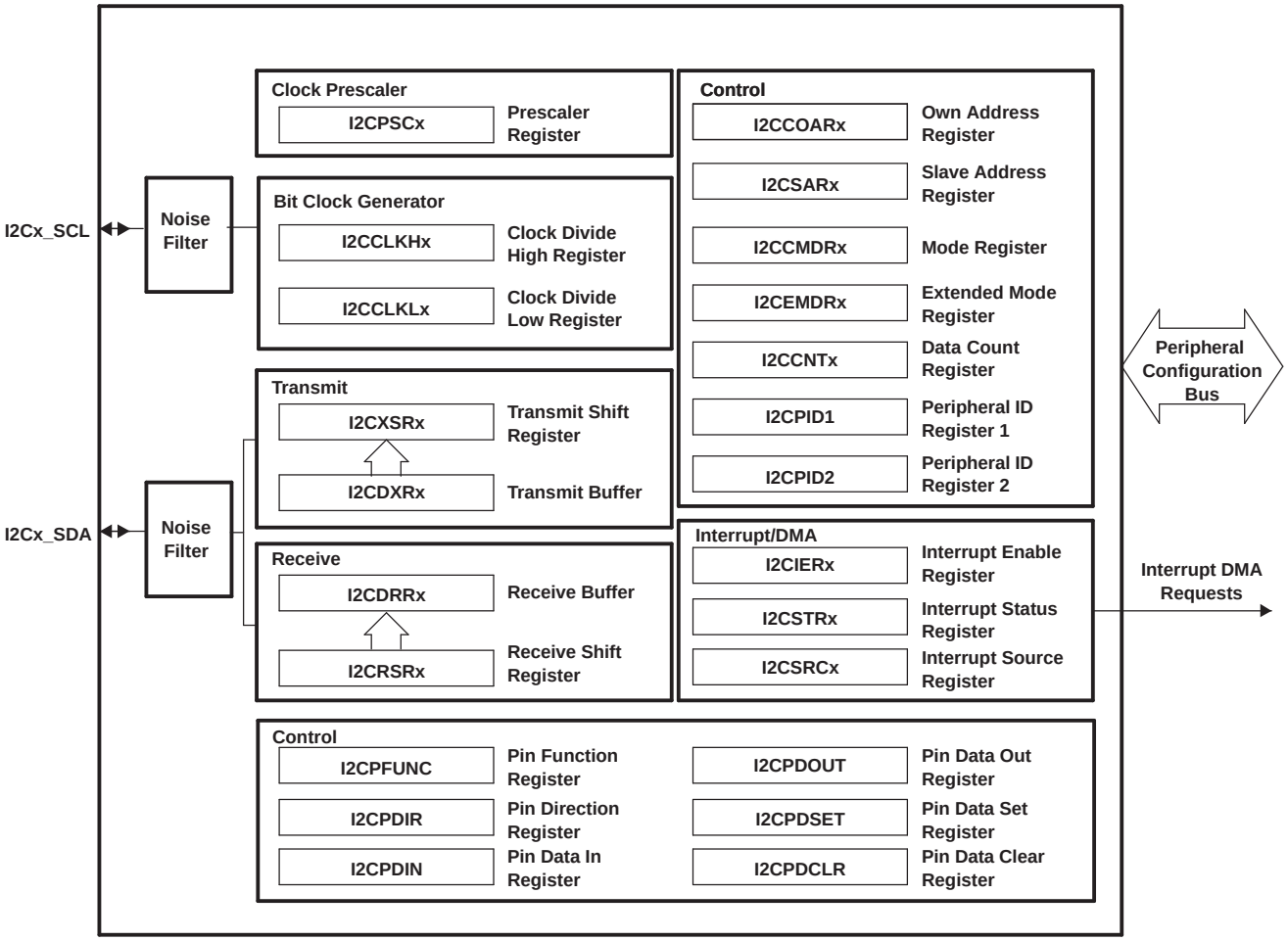



**Figure 6-37. I2C Module Block Diagram**

### 6.16.2 I2C Peripheral Registers Description(s)

Table 6-61 is the list of the I2C registers.

**Table 6-61. Inter-Integrated Circuit (I2C) Registers**

| I2C0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01C2 2000 | ICOAR | I2C Own Address Register |
| 0x01C2 2004 | ICIMR | I2C Interrupt Mask Register |
| 0x01C2 2008 | ICSTR | I2C Interrupt Status Register |
| 0x01C2 200C | ICCLKL | I2C Clock Low-Time Divider Register |
| 0x01C2 2010 | ICCLKH | I2C Clock High-Time Divider Register |
| 0x01C2 2014 | ICCNT | I2C Data Count Register |
| 0x01C2 2018 | ICDRR | I2C Data Receive Register |
| 0x01C2 201C | ICSAR | I2C Slave Address Register |
| 0x01C2 2020 | ICDXR | I2C Data Transmit Register |
| 0x01C2 2024 | ICMDR | I2C Mode Register |
| 0x01C2 2028 | ICIVR | I2C Interrupt Vector Register |
| 0x01C2 202C | ICEMDR | I2C Extended Mode Register |
| 0x01C2 2030 | ICPSC | I2C Prescaler Register |
| 0x01C2 2034 | REVID1 | I2C Revision Identification Register 1 |
| 0x01C2 2038 | REVID2 | I2C Revision Identification Register 2 |
| 0x01C2 2048 | ICPFUNC | I2C Pin Function Register |
| 0x01C2 204C | ICPDIR | I2C Pin Direction Register |
| 0x01C2 2050 | ICPDIN | I2C Pin Data In Register |
| 0x01C2 2054 | ICPDOUT | I2C Pin Data Out Register |
| 0x01C2 2058 | ICPDSET | I2C Pin Data Set Register |
| 0x01C2 205C | ICPDCLR | I2C Pin Data Clear Register |


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### 6.16.3 I2C Electrical Data/Timing

#### 6.16.3.1 Inter-Integrated Circuit (I2C) Timing

Table 6-62 and Table 6-63 assume testing over recommended operating conditions (see Figure 6-38 and Figure 6-39).

**Table 6-62. Timing Requirements for I2C Input**

| NO. | | | 1.2V, 1.1V, 1.0V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, I2Cx_SCL | 10 | | 2.5 | | µs |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA low | 4.7 | | 0.6 | | µs |
| 3 | $t_{h(SCLL-SDAL)}$ | Hold time, I2Cx_SCL low after I2Cx_SDA low | 4 | | 0.6 | | µs |
| 4 | $t_{w(SCLL)}$ | Pulse duration, I2Cx_SCL low | 4.7 | | 1.3 | | µs |
| 5 | $t_{w(SCLH)}$ | Pulse duration, I2Cx_SCL high | 4 | | 0.6 | | µs |
| 6 | $t_{su(SDA-SCLH)}$ | Setup time, I2Cx_SDA before I2Cx_SCL high | 250 | | 100 | | ns |
| 7 | $t_{h(SDA-SCLL)}$ | Hold time, I2Cx_SDA after I2Cx_SCL low | 0 | | 0 | 0.9 | µs |
| 8 | $t_{w(SDAH)}$ | Pulse duration, I2Cx_SDA high | 4.7 | | 1.3 | | µs |
| 9 | $t_{r(SDA)}$ | Rise time, I2Cx_SDA | | 1000 | $20 + 0.1C_b$ | 300 | ns |
| 10 | $t_{r(SCL)}$ | Rise time, I2Cx_SCL | | 1000 | $20 + 0.1C_b$ | 300 | ns |
| 11 | $t_{f(SDA)}$ | Fall time, I2Cx_SDA | | 300 | $20 + 0.1C_b$ | 300 | ns |
| 12 | $t_{f(SCL)}$ | Fall time, I2Cx_SCL | | 300 | $20 + 0.1C_b$ | 300 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA high | 4 | | 0.6 | | µs |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | N/A | | 0 | 50 | ns |
| 15 | $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

**Table 6-63. Switching Characteristics for I2C (1)**

| NO. | PARAMETER | | 1.2V, 1.1V, 1.0V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN | MAX | MIN | MAX | |
| 16 | $t_{c(SCL)}$ | Cycle time, I2Cx_SCL | 10 | | 2.5 | | µs |
| 17 | $t_{su(SCLH-SDAL)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA low | 4.7 | | 0.6 | | µs |
| 18 | $t_{h(SDAL-SCLL)}$ | Hold time, I2Cx_SCL low after I2Cx_SDA low | 4 | | 0.6 | | µs |
| 19 | $t_{w(SCLL)}$ | Pulse duration, I2Cx_SCL low | 4.7 | | 1.3 | | µs |
| 20 | $t_{w(SCLH)}$ | Pulse duration, I2Cx_SCL high | 4 | | 0.6 | | µs |
| 21 | $t_{su(SDAV-SCLH)}$ | Setup time, I2Cx_SDA valid before I2Cx_SCL high | 250 | | 100 | | ns |
| 22 | $t_{h(SCLL-SDAV)}$ | Hold time, I2Cx_SDA valid after I2Cx_SCL low | 0 | | 0 | 0.9 | µs |
| 23 | $t_{w(SDAH)}$ | Pulse duration, I2Cx_SDA high | 4.7 | | 1.3 | | µs |
| 28 | $t_{su(SCLH-SDAH)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA high | 4 | | 0.6 | | µs |

(1) I2C must be configured correctly to meet the timings in Table 6-63.

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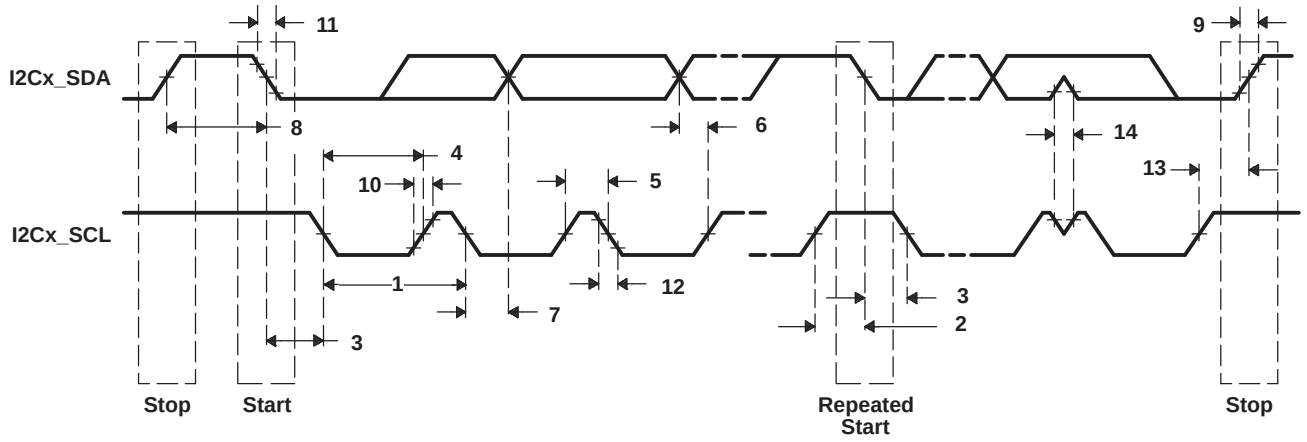



**Figure 6-38. I2C Receive Timings**

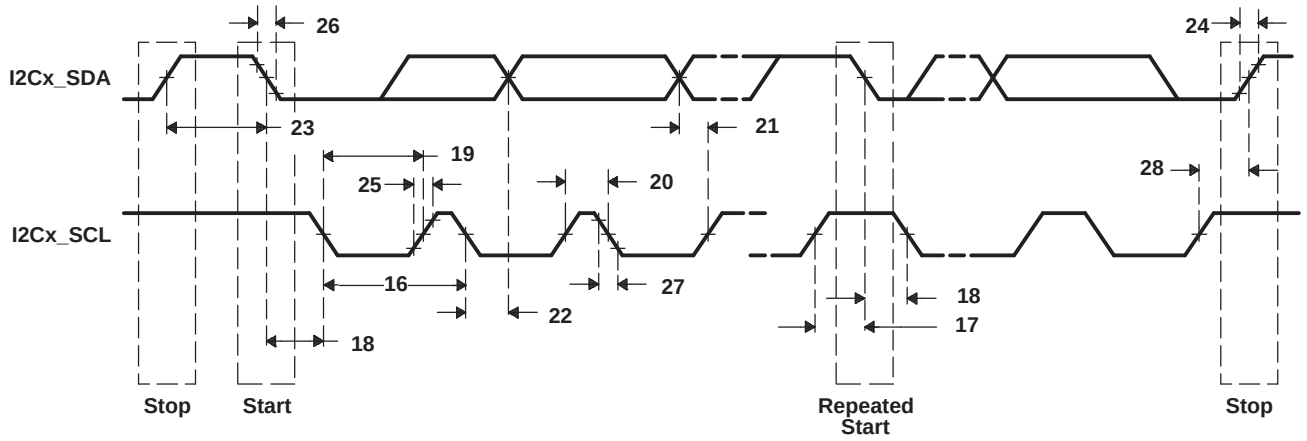



**Figure 6-39. I2C Transmit Timings**


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## 6.17 Universal Asynchronous Receiver/Transmitter (UART)

The UART has the following features:

- 16-byte storage space for both the transmitter and receiver FIFOs
- 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- Programmable auto-rts and auto-cts for autoflow control
- Programmable Baud Rate up to 12 MBaud
- Programmable Oversampling Options of x13 and x16
- Frequency pre-scale values from 1 to 65,535 to generate appropriate baud rates
- Prioritized interrupts
- Programmable serial data formats
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Modem control functions (CTS, RTS)

The UART registers are listed in Section 6.17.1

### *6.17.1 UART Peripheral Registers Description(s)*

Table 6-64 is the list of UART registers.

**Table 6-64. UART Registers**

| UART0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01C4 2000 | RBR | Receiver Buffer Register (read only) |
| 0x01C4 2000 | THR | Transmitter Holding Register (write only) |
| 0x01C4 2004 | IER | Interrupt Enable Register |
| 0x01C4 2008 | IIR | Interrupt Identification Register (read only) |
| 0x01C4 2008 | FCR | FIFO Control Register (write only) |
| 0x01C4 200C | LCR | Line Control Register |
| 0x01C4 2010 | MCR | Modem Control Register |
| 0x01C4 2014 | LSR | Line Status Register |
| 0x01C4 2018 | MSR | Modem Status Register |
| 0x01C4 201C | SCR | Scratchpad Register |
| 0x01C4 2020 | DLL | Divisor LSB Latch |
| 0x01C4 2024 | DLH | Divisor MSB Latch |
| 0x01C4 2028 | REVID1 | Revision Identification Register 1 |
| 0x01C4 2030 | PWREMU_MGMT | Power and Emulation Management Register |
| 0x01C4 2034 | MDR | Mode Definition Register |

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### 6.17.2 UART Electrical Data/Timing

**Table 6-65. Timing Requirements for UART Receive(1) (see Figure 6-40)**

| NO. | | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 4 | $t_{w(URXDB)}$ | Pulse duration, receive data bit (RXDn) | 0.96U | 1.05U | ns |
| 5 | $t_{w(URXSB)}$ | Pulse duration, receive start bit | 0.96U | 1.05U | ns |

(1) U = UART baud time = 1/programmed baud rate.

**Table 6-66. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit(1) (see Figure 6-40)**

| NO. | PARAMETER | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $f_{(baud)}$ | Maximum programmable baud rate | | D/E (2) (3) | MBaud (4) |
| 2 | $t_{w(UTXDB)}$ | Pulse duration, transmit data bit (TXDn) | U - 2 | U + 2 | ns |
| 3 | $t_{w(UTXSB)}$ | Pulse duration, transmit start bit | U - 2 | U + 2 | ns |

(1) U = UART baud time = 1/programmed baud rate.
(2) D = UART input clock in MHz.
(3) E = UART divisor x UART sampling rate. The UART divisor is set through the UART divisor latch registers (DLL and DLH). The UART sampling rate is set through the over-sampling mode select bit (OSM_SEL) of the UART mode definition register (MDR).
(4) Baud rate is not indicative of data rate. Actual data rate will be limited by system factors such as EDMA loading, EMIF/DDR loading, system frequency, etc.

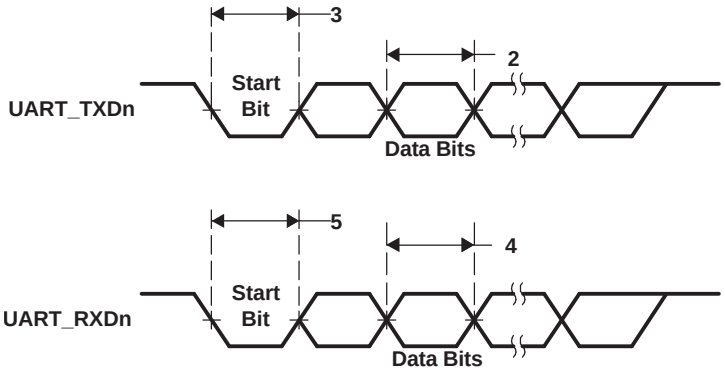



**Figure 6-40. UART Transmit/Receive Timing**


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## 6.18 Host-Port Interface (UHPI)

### 6.18.1 HPI Device-Specific Information

The device includes a user-configurable 16-bit Host-port interface (HPI16).

The host port interface (UHPI) provides a parallel port interface through which an external host processor can directly access the processor's resources (configuration and program/data memories). The external host device is asynchronous to the CPU clock and functions as a master to the HPI interface. The UHPI enables a host device and the processor to exchange information via internal or external memory. Dedicated address (HPIA) and data (HPID) registers within the UHPI provide the data path between the external host interface and the processor resources. A UHPI control register (HPIC) is available to the host and the CPU for various configuration and interrupt functions.

### 6.18.2 HPI Peripheral Register Description(s)

**Table 6-67. HPI Control Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | COMMENTS |
|---|---|---|---|
| 0x01E1 0000 | PID | Peripheral Identification Register | |
| 0x01E1 0004 | PWREMU_MGMT | HPI power and emulation management register | The CPU has read/write access to the PWREMU_MGMT register. |
| 0x01E1 0008 | - | Reserved | |
| 0x01E1 000C | GPIO_EN | General Purpose IO Enable Register | |
| 0x01E1 0010 | GPIO_DIR1 | General Purpose IO Direction Register 1 | |
| 0x01E1 0014 | GPIO_DAT1 | General Purpose IO Data Register 1 | |
| 0x01E1 0018 | GPIO_DIR2 | General Purpose IO Direction Register 2 | |
| 0x01E1 001C | GPIO_DAT2 | General Purpose IO Data Register 2 | |
| 0x01E1 0020 | GPIO_DIR3 | General Purpose IO Direction Register 3 | |
| 0x01E1 0024 | GPIO_DAT3 | General Purpose IO Data Register 3 | |
| 01E1 0028 | - | Reserved | |
| 01E1 002C | - | Reserved | |
| 01E1 0030 | HPIC | HPI control register | The Host and the CPU both have read/write access to the HPIC register. |
| 01E1 0034 | HPIA (HPIAW)(1) | HPI address register (Write) | The Host has read/write access to the HPIA registers. The CPU has only read access to the HPIA registers. |
| 01E1 0038 | HPIA (HPIAR)(1) | HPI address register (Read) | |
| 01E1 000C - 01E1 07FF | - | Reserved | |

(1) There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the Host. The CPU can access HPIAW and HPIAR independently.

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### 6.18.3 HPI Electrical Data/Timing

**Table 6-68. Timing Requirements for Host-Port Interface [1.2V, 1.1V](1) (2)**

| NO. | | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{su(SELV-HSTBL)}$ | Setup time, select signals(3) valid before $\overline{\text{UHPI_HSTROBE}}$ low | 5 | | ns |
| 2 | $t_{h(HSTBL-SELV)}$ | Hold time, select signals(3) valid after $\overline{\text{UHPI_HSTROBE}}$ low | 2 | | ns |
| 3 | $t_{w(HSTBL)}$ | Pulse duration, $\overline{\text{UHPI_HSTROBE}}$ active low | 15 | | ns |
| 4 | $t_{w(HSTBH)}$ | Pulse duration, $\overline{\text{UHPI_HSTROBE}}$ inactive high between consecutive accesses | 2M | | ns |
| 9 | $t_{su(SELV-HASL)}$ | Setup time, selects signals valid before $\overline{\text{UHPI_HAS}}$ low | 5 | | ns |
| 10 | $t_{h(HASL-SELV)}$ | Hold time, select signals valid after $\overline{\text{UHPI_HAS}}$ low | 2 | | ns |
| 11 | $t_{su(HDV-HSTBH)}$ | Setup time, host data valid before $\overline{\text{UHPI_HSTROBE}}$ high | 5 | | ns |
| 12 | $t_{h(HSTBH-HDV)}$ | Hold time, host data valid after $\overline{\text{UHPI_HSTROBE}}$ high | 2 | | ns |
| 13 | $t_{h(HRDYL-HSTBH)}$ | Hold time, $\overline{\text{UHPI_HSTROBE}}$ high after $\overline{\text{UHPI_HRDY}}$ low. $\overline{\text{UHPI_HSTROBE}}$ should not be inactivated until $\overline{\text{UHPI_HRDY}}$ is active (low); otherwise, HPI writes will not complete properly. | 2 | | ns |
| 16 | $t_{su(HASL-HSTBL)}$ | Setup time, $\overline{\text{UHPI_HAS}}$ low before $\overline{\text{UHPI_HSTROBE}}$ low | 5 | | ns |
| 17 | $t_{h(HSTBL-HASH)}$ | Hold time, $\overline{\text{UHPI_HAS}}$ low after $\overline{\text{UHPI_HSTROBE}}$ low | 2 | | ns |

(1) $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$: [NOT($\overline{\text{UHPI_HDS1}}$ XOR $\overline{\text{UHPI_HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.
(2) M=SYSCLK2 period in ns.
(3) Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$ and HHWIL.


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**Table 6-69. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface [1.2V, 1.1V](1) (2) (3)**

| NO. | PARAMETER | | | 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 5 | $t_{d(HSTBL-HRDYV)}$ | Delay time, HSTROBE low to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: Back-to-back HPIA writes (can be either first or second half-word)<br>*Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word)<br>*Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word)<br>*Case 4*: HPIA write and Write FIFO not empty<br><br>For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions:<br>*Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access)<br>*Case 2*: First half-word access of HPID Read without auto-increment<br>For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions:<br>*Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access)<br>*Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access)<br>*Case 3*: HPIC or HPIA read (applies to either half-word access) | | 15 | | 17 | ns |
| 5a | $t_{d(HASL-HRDYV)}$ | Delay time, HAS low to HRDY valid | | | 15 | | 17 | ns |
| 6 | $t_{en(HSTBL-HDLZ)}$ | Enable time, HD driven from HSTROBE low | | 1.5 | | 1.5 | | ns |
| 7 | $t_{d(HRDYL-HDV)}$ | Delay time, HRDY low to HD valid | | | 0 | | 0 | ns |
| 8 | $t_{oh(HSTBH-HDV)}$ | Output hold time, HD valid after HSTROBE high | | 1.5 | | 1.5 | | ns |
| 14 | $t_{dis(HSTBH-HDHZ)}$ | Disable time, HD high-impedance from HSTROBE high | | | 15 | | 17 | ns |
| 15 | $t_{d(HSTBL-HDV)}$ | Delay time, HSTROBE low to HD valid | For HPI Read. Applies to conditions where data is already residing in HPID/FIFO:<br>*Case 1*: HPIC or HPIA read<br>*Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO<br>*Case 3*: Second half-word of HPID read with or without auto-increment | | 15 | | 17 | ns |
| 18 | $t_{d(HSTBH-HRDYV)}$ | Delay time, HSTROBE high to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: HPID write when Write FIFO is full (can happen to either half-word)<br>*Case 2*: HPIA write (can happen to either half-word)<br>*Case 3*: HPID write without auto-increment (only happens to second half-word) | | 15 | | 17 | ns |

(1) M=SYSCLK2 period in ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).

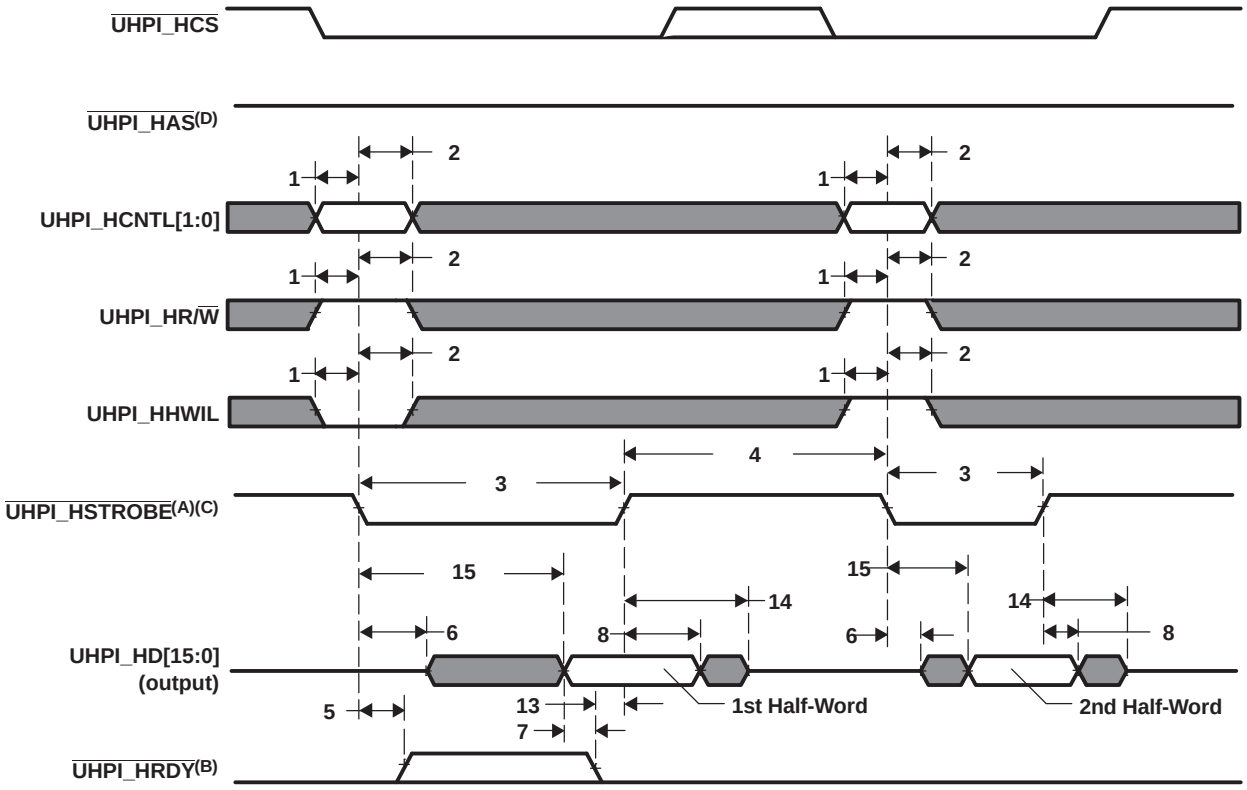
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**Table 6-70. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface [1.0V](1) (2) (3)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 5 | $t_{d(HSTBL-HRDYV)}$ | Delay time, HSTROBE low to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: Back-to-back HPIA writes (can be either first or second half-word)<br>*Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word)<br>*Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word)<br>*Case 4*: HPIA write and Write FIFO not empty<br><br>For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions:<br>*Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access)<br>*Case 2*: First half-word access of HPID Read without auto-increment<br>For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions:<br>*Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access)<br>*Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access)<br>*Case 3*: HPIC or HPIA read (applies to either half-word access) | | 22 | ns |
| 5a | $t_{d(HASL-HRDYV)}$ | Delay time, HAS low to HRDY valid | | | 22 | ns |
| 6 | $t_{en(HSTBL-HDLZ)}$ | Enable time, HD driven from HSTROBE low | | 1.5 | | ns |
| 7 | $t_{d(HRDYL-HDV)}$ | Delay time, HRDY low to HD valid | | | 0 | ns |
| 8 | $t_{oh(HSTBH-HDV)}$ | Output hold time, HD valid after HSTROBE high | | 1.5 | | ns |
| 14 | $t_{dis(HSTBH-HDHZ)}$ | Disable time, HD high-impedance from HSTROBE high | | | 22 | ns |
| 15 | $t_{d(HSTBL-HDV)}$ | Delay time, HSTROBE low to HD valid | For HPI Read. Applies to conditions where data is already residing in HPID/FIFO:<br>*Case 1*: HPIC or HPIA read<br>*Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO<br>*Case 3*: Second half-word of HPID read with or without auto-increment | | 22 | ns |
| 18 | $t_{d(HSTBH-HRDYV)}$ | Delay time, HSTROBE high to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: HPID write when Write FIFO is full (can happen to either half-word)<br>*Case 2*: HPIA write (can happen to either half-word)<br>*Case 3*: HPID write without auto-increment (only happens to second half-word) | | 22 | ns |

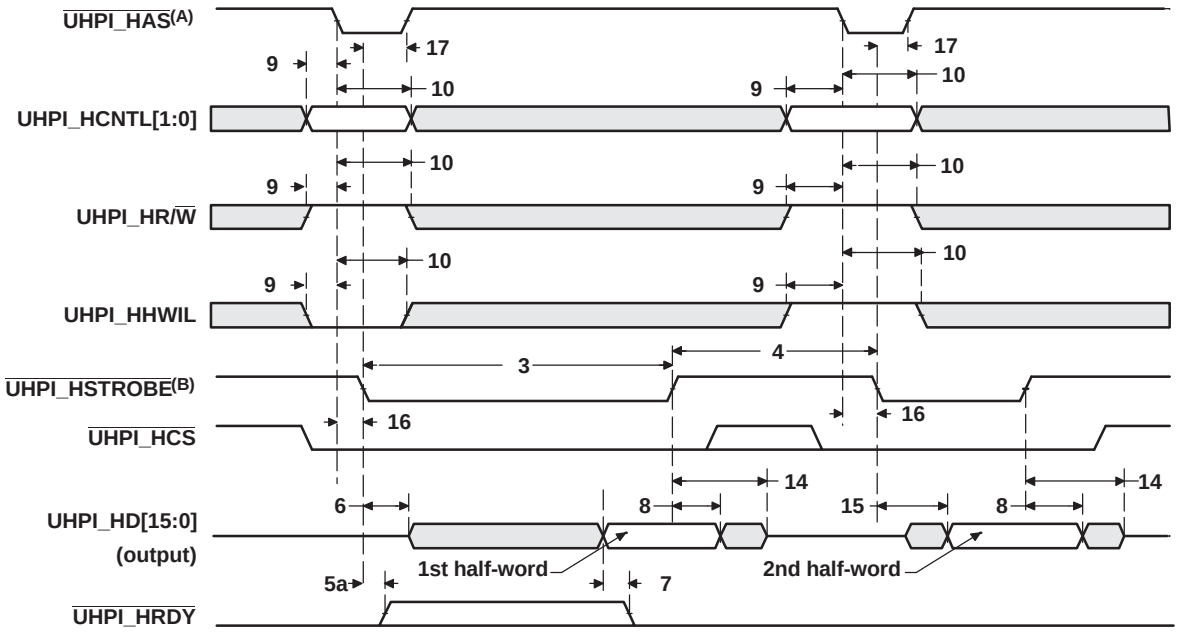
(1) M=SYSCLK2 period in ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).


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A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing)and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.
C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.
D The diagram above assumes UHPI_HAS has been pulled high.

**Figure 6-41. UHPI Read Timing (HAS Not Used, Tied High)**

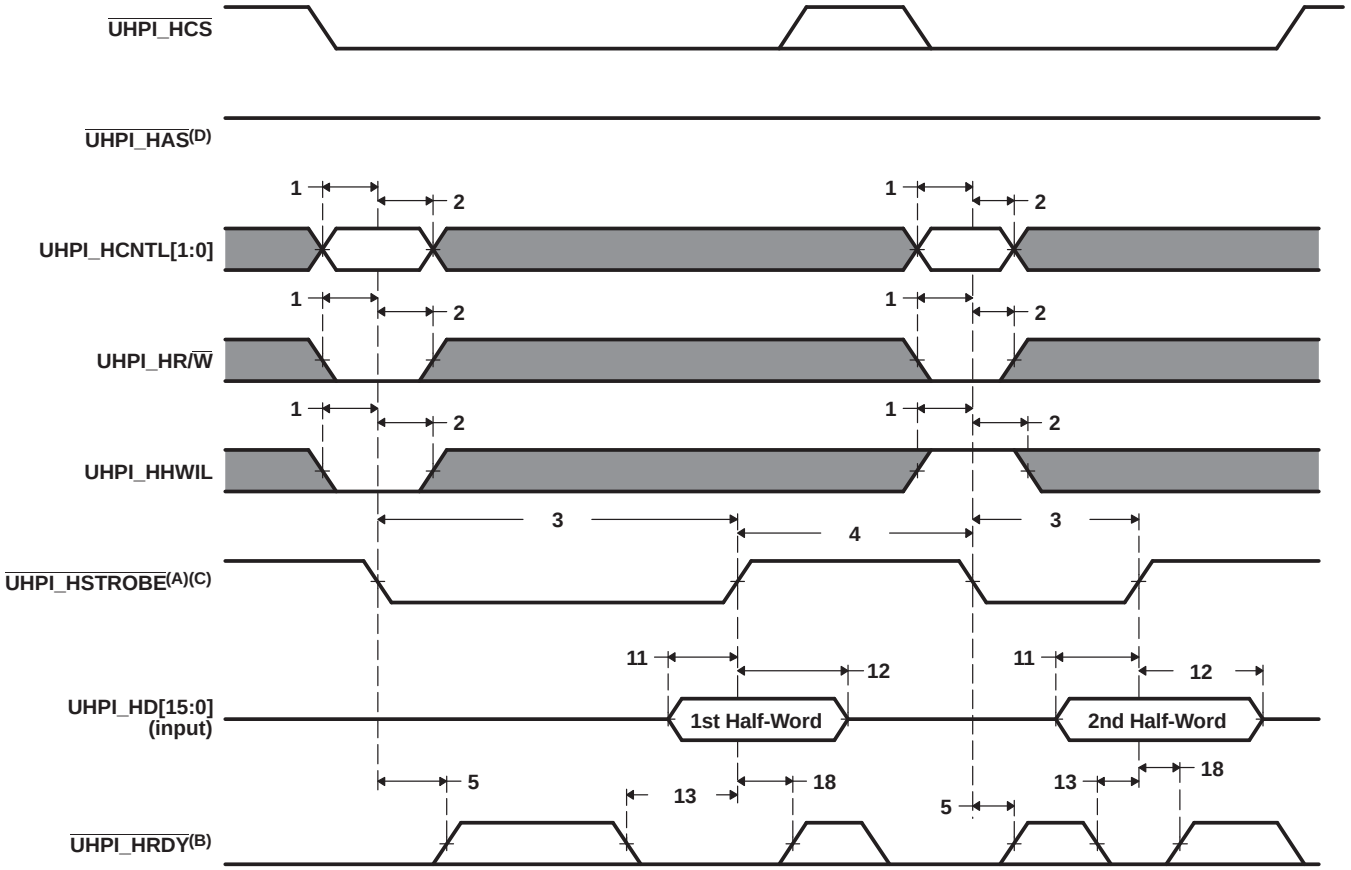



A. For correct operation, strobe the UHPI_HAS signal only once per UHPI_HSTROBE active cycle.

B. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

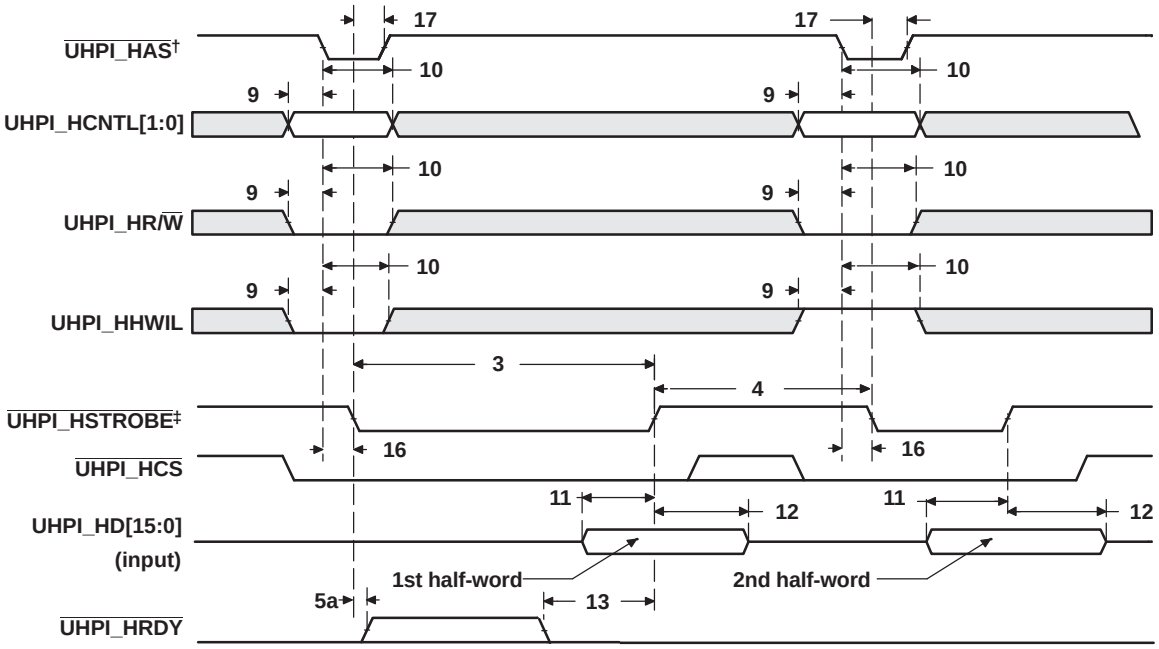
**Figure 6-42. UHPI Read Timing (HAS Used)**


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A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.
C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.
D The diagram above assumes UHPI_HAS has been pulled high.

**Figure 6-43. UHPI Write Timing (HAS Not Used, Tied High)**




A. For correct operation, strobe the $\overline{\text{UHPI_HAS}}$ signal only once per $\overline{\text{UHPI_HSTROBE}}$ active cycle.
B. $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$: [NOT($\overline{\text{UHPI_HDS1}}$ XOR $\overline{\text{UHPI_HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.

**Figure 6-44. UHPI Write Timing ($\overline{\text{HAS}}$ Used)**


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## 6.19 Enhanced Capture (eCAP) Peripheral

The device contains up to three enhanced capture (eCAP) modules. Figure 6-45 shows a functional block diagram of a module.

Uses for ECAP include:

- Speed measurements of rotating machinery (e.g. toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor triggers
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The ECAP module described in this specification includes the following features:

- 32 bit time base
- 4 event time-stamp registers (each 32 bits)
- Edge polarity selection for up to 4 sequenced time-stamp capture events
- Interrupt on either of the 4 events
- Single shot capture of up to 4 event time-stamps
- Continuous mode capture of time-stamps in a 4 deep circular buffer
- Absolute time-stamp capture
- Difference mode time-stamp capture
- All the above resources are dedicated to a single input pin

The eCAP modules are clocked at the ASYNC3 clock domain rate.

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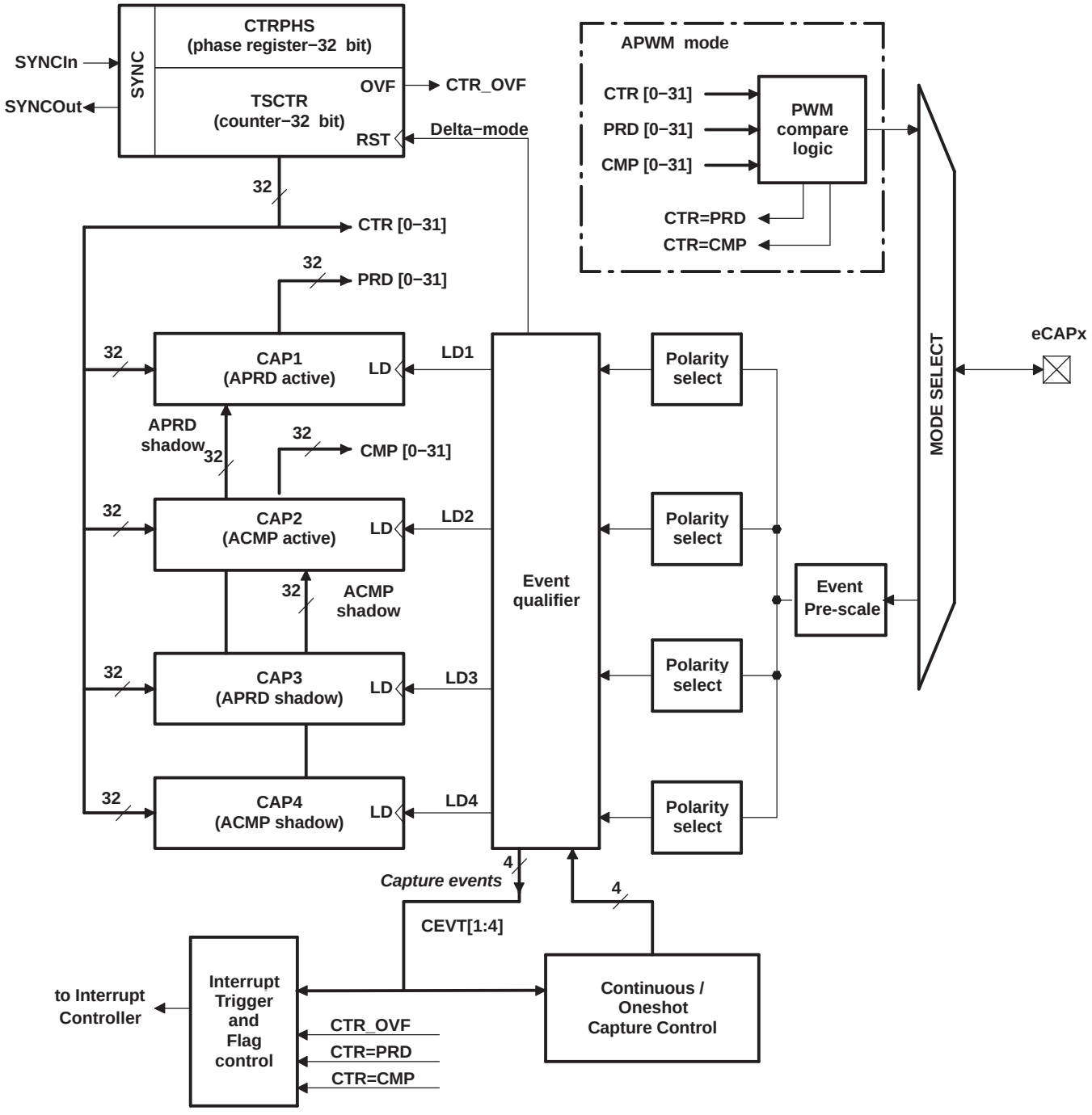



**Figure 6-45. eCAP Functional Block Diagram**


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Table 6-71 is the list of the ECAP registers.

**Table 6-71. ECAPx Configuration Registers**

| ECAP0 BYTE ADDRESS | ECAP1 BYTE ADDRESS | ECAP2 BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|---|---|
| 0x01F0 6000 | 0x01F0 7000 | 0x01F0 8000 | TSCTR | Time-Stamp Counter |
| 0x01F0 6004 | 0x01F0 7004 | 0x01F0 8004 | CTRPHS | Counter Phase Offset Value Register |
| 0x01F0 6008 | 0x01F0 7008 | 0x01F0 8008 | CAP1 | Capture 1 Register |
| 0x01F0 600C | 0x01F0 700C | 0x01F0 800C | CAP2 | Capture 2 Register |
| 0x01F0 6010 | 0x01F0 7010 | 0x01F0 8010 | CAP3 | Capture 3 Register |
| 0x01F0 6014 | 0x01F0 7014 | 0x01F0 8014 | CAP4 | Capture 4 Register |
| 0x01F0 6028 | 0x01F0 7028 | 0x01F0 8028 | ECCTL1 | Capture Control Register 1 |
| 0x01F0 602A | 0x01F0 702A | 0x01F0 802A | ECCTL2 | Capture Control Register 2 |
| 0x01F0 602C | 0x01F0 702C | 0x01F0 802C | ECEINT | Capture Interrupt Enable Register |
| 0x01F0 602E | 0x01F0 702E | 0x01F0 802E | ECFLG | Capture Interrupt Flag Register |
| 0x01F0 6030 | 0x01F0 7030 | 0x01F0 8030 | ECCLR | Capture Interrupt Clear Register |
| 0x01F0 6032 | 0x01F0 7032 | 0x01F0 8032 | ECFRC | Capture Interrupt Force Register |
| 0x01F0 605C | 0x01F0 705C | 0x01F0 805C | REVID | Revision ID |

Table 6-72 shows the eCAP timing requirement and Table 6-73 shows the eCAP switching characteristics.

**Table 6-72. Timing Requirements for Enhanced Capture (eCAP)**

| | | TEST CONDITIONS | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SCO)}$ | | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | | cycles |

**Table 6-73. Switching Characteristics Over Recommended Operating Conditions for eCAP**

| PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | 20 | | 20 | | ns |

## 6.20 Enhanced High-Resolution Pulse-Width Modulator (eHRPWM)

The device contains two enhanced PWM Modules (eHRPWM). Figure 6-46 shows a block diagram of multiple eHRPWM modules. Figure 6-46 shows the signal interconnections with the eHRPWM.

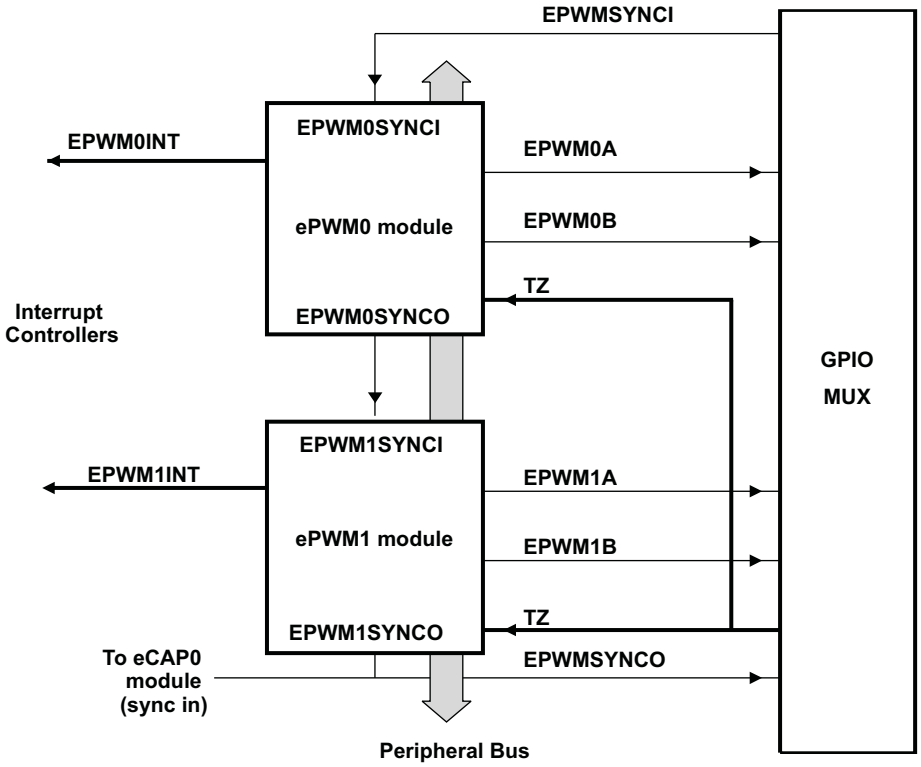



**Figure 6-46. Multiple PWM Modules in a C6742 System**


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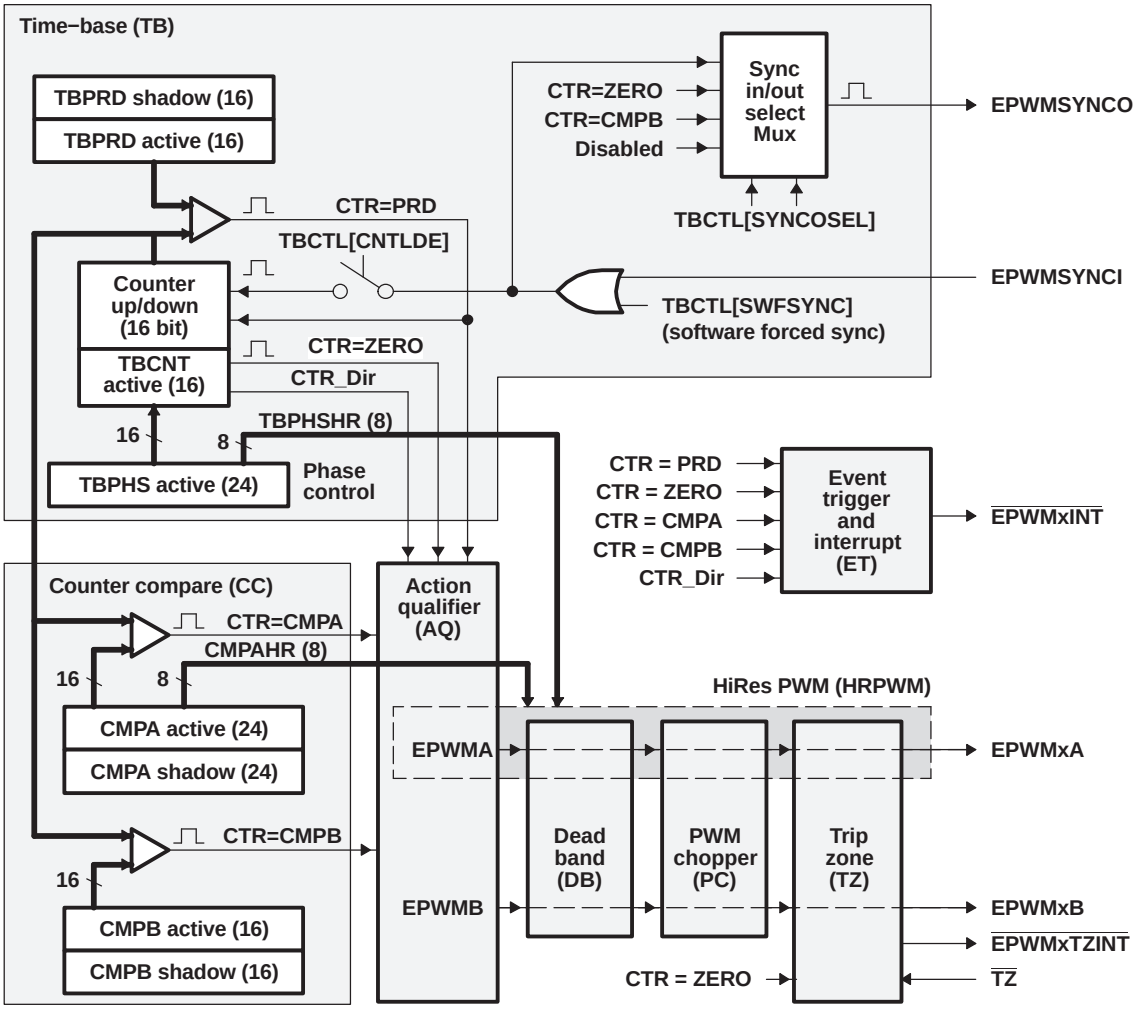



**Figure 6-47. eHRPWM Sub-Modules Showing Critical Internal Signal Interconnections**

**Table 6-74. eHRPWM Module Control and Status Registers Grouped by Submodule**

| eHRPWM0 BYTE ADDRESS | eHRPWM1 BYTE ADDRESS | ACRONYM | SHADOW | REGISTER DESCRIPTION |
|---|---|---|---|---|
| **Time-Base Submodule Registers** | | | | |
| 0x01F0 0000 | 0x01F0 2000 | TBCTL | No | Time-Base Control Register |
| 0x01F0 0002 | 0x01F0 2002 | TBSTS | No | Time-Base Status Register |
| 0x01F0 0004 | 0x01F0 2004 | TBPHSHR | No | Extension for HRPWM Phase Register(1) |
| 0x01F0 0006 | 0x01F0 2006 | TBPHS | No | Time-Base Phase Register |
| 0x01F0 0008 | 0x01F0 2008 | TBCNT | No | Time-Base Counter Register |
| 0x01F0 000A | 0x01F0 200A | TBPRD | Yes | Time-Base Period Register |
| **Counter-Compare Submodule Registers** | | | | |
| 0x01F0 000E | 0x01F0 200E | CMPCTL | No | Counter-Compare Control Register |
| 0x01F0 0010 | 0x01F0 2010 | CMPAHR | No | Extension for HRPWM Counter-Compare A Register(1) |
| 0x01F0 0012 | 0x01F0 2012 | CMPA | Yes | Counter-Compare A Register |
| 0x01F0 0014 | 0x01F0 2014 | CMPB | Yes | Counter-Compare B Register |
| **Action-Qualifier Submodule Registers** | | | | |
| 0x01F0 0016 | 0x01F0 2016 | AQCTLA | No | Action-Qualifier Control Register for Output A (eHRPWMxA) |
| 0x01F0 0018 | 0x01F0 2018 | AQCTLB | No | Action-Qualifier Control Register for Output B (eHRPWMxB) |
| 0x01F0 001A | 0x01F0 201A | AQSFRC | No | Action-Qualifier Software Force Register |
| 0x01F0 001C | 0x01F0 201C | AQCSFRC | Yes | Action-Qualifier Continuous S/W Force Register Set |
| **Dead-Band Generator Submodule Registers** | | | | |
| 0x01F0 001E | 0x01F0 201E | DBCTL | No | Dead-Band Generator Control Register |
| 0x01F0 0020 | 0x01F0 2020 | DBRED | No | Dead-Band Generator Rising Edge Delay Count Register |
| 0x01F0 0022 | 0x01F0 2022 | DBFED | No | Dead-Band Generator Falling Edge Delay Count Register |
| **PWM-Chopper Submodule Registers** | | | | |
| 0x01F0 003C | 0x01F0 203C | PCCTL | No | PWM-Chopper Control Register |
| **Trip-Zone Submodule Registers** | | | | |
| 0x01F0 0024 | 0x01F0 2024 | TZSEL | No | Trip-Zone Select Register |
| 0x01F0 0028 | 0x01F0 2028 | TZCTL | No | Trip-Zone Control Register |
| 0x01F0 002A | 0x01F0 202A | TZEINT | No | Trip-Zone Enable Interrupt Register |
| 0x01F0 002C | 0x01F0 202C | TZFLG | No | Trip-Zone Flag Register |
| 0x01F0 002E | 0x01F0 202E | TZCLR | No | Trip-Zone Clear Register |
| 0x01F0 0030 | 0x01F0 2030 | TZFRC | No | Trip-Zone Force Register |
| **Event-Trigger Submodule Registers** | | | | |
| 0x01F0 0032 | 0x01F0 2032 | ETSEL | No | Event-Trigger Selection Register |
| 0x01F0 0034 | 0x01F0 2034 | ETPS | No | Event-Trigger Pre-Scale Register |
| 0x01F0 0036 | 0x01F0 2036 | ETFLG | No | Event-Trigger Flag Register |
| 0x01F0 0038 | 0x01F0 2038 | ETCLR | No | Event-Trigger Clear Register |
| 0x01F0 003A | 0x01F0 203A | ETFRC | No | Event-Trigger Force Register |
| **High-Resolution PWM (HRPWM) Submodule Registers** | | | | |
| 0x01F0 1040 | 0x01F0 3040 | HRCNFG | No | HRPWM Configuration Register (1) |

(1) These registers are only available on eHRPWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, these locations are reserved.


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### 6.20.1 Enhanced Pulse Width Modulator (eHRPWM) Timing

PWM refers to PWM outputs on eHRPWM1-6. Table 6-75 shows the PWM timing requirements and Table 6-76, switching characteristics.

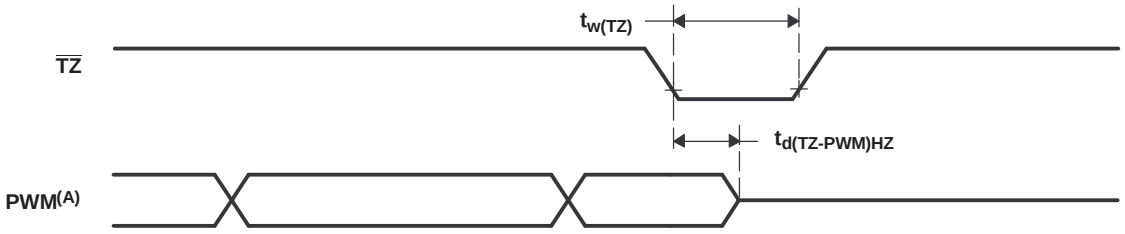
**Table 6-75. Timing Requirements for eHRPWM**

| | | TEST CONDITIONS | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{w(SYNCIN)}$ | Sync input pulse width | Asynchronous | $2t_{c(SCO)}$ | | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | | cycles |

**Table 6-76. Switching Characteristics Over Recommended Operating Conditions for eHRPWM**

| PARAMETER | | TEST CONDITIONS | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{w(PWM)}$ | Pulse duration, PWMx output high/low | | 20 | | 20 | | 26.6 | | ns |
| $t_{w(SYNCOUT)}$ | Sync output pulse width | | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | cycles |
| $t_{d(PWM)TZA}$ | Delay time, trip input active to PWM forced high<br>Delay time, trip input active to PWM forced low | no pin load; no additional programmable delay | | 25 | | 25 | | 25 | ns |
| $t_{d(TZ-PWM)HZ}$ | Delay time, trip input active to PWM Hi-Z | no additional programmable delay | | 20 | | 20 | | 20 | ns |

### 6.20.2 Trip-Zone Input Timing




A. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

**Figure 6-48. PWM Hi-Z Characteristics**

**Table 6-77. Trip-Zone input Timing Requirements**

| | | TEST CONDITIONS | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{w(TZ)}$ | Pulse duration, $\overline{TZ}$x input low | Asynchronous | $1t_{c(SCO)}$ | | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | | cycles |


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## 6.21 Timers

The timers support the following features:

- Configurable as single 64-bit timer or two 32-bit timers
- Period timeouts generate interrupts, DMA events or external pin events
- 8 32-bit compare registers
- Compare matches generate interrupt events
- Capture capability
- 64-bit Watchdog capability (Timer64P1 only)

Table 6-78 lists the timer registers.

**Table 6-78. Timer Registers**

| TIMER64P 0 BYTE ADDRESS | TIMER64P 1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C2 0000 | 0x01C2 1000 | REV | Revision Register |
| 0x01C2 0004 | 0x01C2 1004 | EMUMGT | Emulation Management Register |
| 0x01C2 0008 | 0x01C2 1008 | GPINTGPEN | GPIO Interrupt and GPIO Enable Register |
| 0x01C2 000C | 0x01C2 100C | GPDATGPDIR | GPIO Data and GPIO Direction Register |
| 0x01C2 0010 | 0x01C2 1010 | TIM12 | Timer Counter Register 12 |
| 0x01C2 0014 | 0x01C2 1014 | TIM34 | Timer Counter Register 34 |
| 0x01C2 0018 | 0x01C2 1018 | PRD12 | Timer Period Register 12 |
| 0x01C2 001C | 0x01C2 101C | PRD34 | Timer Period Register 34 |
| 0x01C2 0020 | 0x01C2 1020 | TCR | Timer Control Register |
| 0x01C2 0024 | 0x01C2 1024 | TGCR | Timer Global Control Register |
| 0x01C2 0028 | 0x01C2 1028 | WDTCR | Watchdog Timer Control Register |
| 0x01C2 0034 | 0x01C2 1034 | REL12 | Timer Reload Register 12 |
| 0x01C2 0038 | 0x01C2 1038 | REL34 | Timer Reload Register 34 |
| 0x01C2 003C | 0x01C2 103C | CAP12 | Timer Capture Register 12 |
| 0x01C2 0040 | 0x01C2 1040 | CAP34 | Timer Capture Register 34 |
| 0x01C2 0044 | 0x01C2 1044 | INTCTLSTAT | Timer Interrupt Control and Status Register |
| 0x01C2 0060 | 0x01C2 1060 | CMP0 | Compare Register 0 |
| 0x01C2 0064 | 0x01C2 1064 | CMP1 | Compare Register 1 |
| 0x01C2 0068 | 0x01C2 1068 | CMP2 | Compare Register 2 |
| 0x01C2 006C | 0x01C2 106C | CMP3 | Compare Register 3 |
| 0x01C2 0070 | 0x01C2 1070 | CMP4 | Compare Register 4 |
| 0x01C2 0074 | 0x01C2 1074 | CMP5 | Compare Register 5 |
| 0x01C2 0078 | 0x01C2 1078 | CMP6 | Compare Register 6 |
| 0x01C2 007C | 0x01C2 107C | CMP7 | Compare Register 7 |

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### 6.21.1 Timer Electrical Data/Timing

**Table 6-79. Timing Requirements for Timer Input(1) (2) (see Figure 6-49)**

| NO. | | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(TM64Px_IN12)}$ | Cycle time, TM64Px_IN12 | 4P | | ns |
| 2 | $t_{w(TINPH)}$ | Pulse duration, TM64Px_IN12 high | 0.45C | 0.55C | ns |
| 3 | $t_{w(TINPL)}$ | Pulse duration, TM64Px_IN12 low | 0.45C | 0.55C | ns |
| 4 | $t_{t(TM64Px_IN12)}$ | Transition time, TM64Px_IN12 | | 0.25P or 10 (3) | ns |

(1) P = OSCIN cycle time in ns.
(2) C = TM64P0_IN12 cycle time in ns.
(3) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

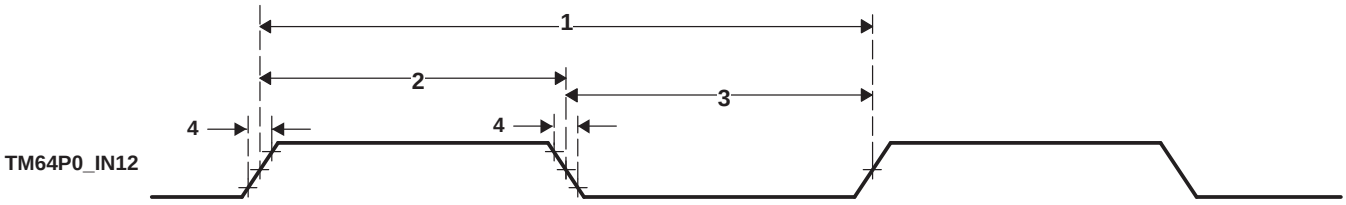



**Figure 6-49. Timer Timing**

**Table 6-80. Switching Characteristics Over Recommended Operating Conditions for Timer Output (1)**

| NO. | PARAMETER | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 5 | $t_{w(TOUTH)}$ | Pulse duration, TM64P0_OUT12 high | 4P | | ns |
| 6 | $t_{w(TOUTL)}$ | Pulse duration, TM64P0_OUT12 low | 4P | | ns |

(1) P = OSCIN cycle time in ns. For example, when OSCIN frequency is 27 MHz, use P = 37.0$\overline{37}$ ns.

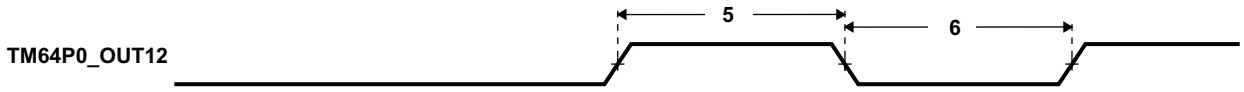



**Figure 6-50. Timer Timing**


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## 6.22 Real Time Clock (RTC)

The RTC provides a time reference to an application running on the device. The current date and time is tracked in a set of counter registers that update once per second. The time can be represented in 12-hour or 24-hour mode. The calendar and time registers are buffered during reads and writes so that updates do not interfere with the accuracy of the time and date.

Alarms are available to interrupt the CPU at a particular time, or at periodic time intervals, such as once per minute or once per day. In addition, the RTC can interrupt the CPU every time the calendar and time registers are updated, or at programmable periodic intervals.

The real-time clock (RTC) provides the following features:

- 100-year calendar (xx00 to xx99)
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 12-hour clock mode (with AM and PM) or 24-hour clock mode
- Alarm interrupt
- Periodic interrupt
- Single interrupt to the CPU
- Supports external 32.768-kHz crystal or external clock source of the same frequency
- Separate isolated power supply

Figure 6-51 shows a block diagram of the RTC.

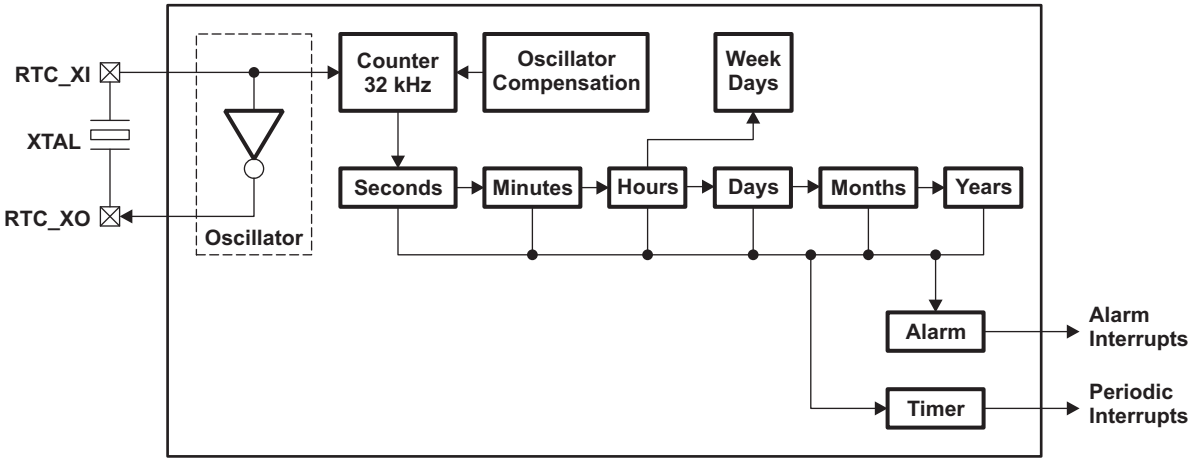



**Figure 6-51. Real-Time Clock Block Diagram**

### 6.22.1 Clock Source

The clock reference for the RTC is an external 32.768-kHz crystal or an external clock source of the same frequency. The RTC also has a separate power supply that is isolated from the rest of the system. When the CPU and other peripherals are without power, the RTC can remain powered to preserve the current time and calendar information. Even if the RTC is not used, it must remain powered when the rest of the device is powered.

The source for the RTC reference clock may be provided by a crystal or by an external clock source. The RTC has an internal oscillator buffer to support direct operation with a crystal. The crystal is connected between pins RTC_XI and RTC_XO. RTC_XI is the input to the on-chip oscillator and RTC_XO is the output from the oscillator back to the crystal.

An external 32.768-kHz clock source may be used instead of a crystal. In such a case, the clock source is connected to RTC_XI, and RTC_XO is left unconnected.

If the RTC is not used, the RTC_XI pin should be held either low or high, RTC_XO should be left unconnected, RTC_CVDD should be connected to the device CVDD, and RTC_VSS should remain grounded.

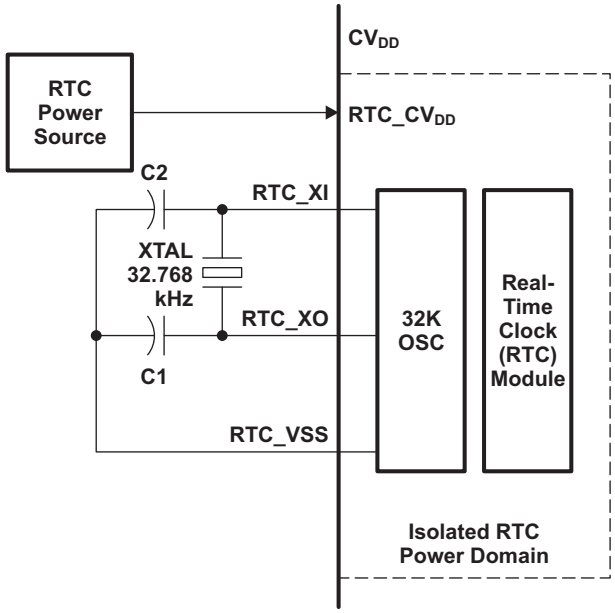



**Figure 6-52. Clock Source**


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### 6.22.2 Real-Time Clock Register Descriptions

**Table 6-81. Real-Time Clock (RTC) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01C2 3000 | SECOND | Seconds Register |
| 0x01C2 3004 | MINUTE | Minutes Register |
| 0x01C2 3008 | HOUR | Hours Register |
| 0x01C2 300C | DAY | Day of the Month Register |
| 0x01C2 3010 | MONTH | Month Register |
| 0x01C2 3014 | YEAR | Year Register |
| 0x01C2 3018 | DOTW | Day of the Week Register |
| 0x01C2 3020 | ALARMSECOND | Alarm Seconds Register |
| 0x01C2 3024 | ALARMMINUTE | Alarm Minutes Register |
| 0x01C2 3028 | ALARMHOUR | Alarm Hours Register |
| 0x01C2 302C | ALARMDAY | Alarm Days Register |
| 0x01C2 3030 | ALARMMONTH | Alarm Months Register |
| 0x01C2 3034 | ALARMYEAR | Alarm Years Register |
| 0x01C2 3040 | CTRL | Control Register |
| 0x01C2 3044 | STATUS | Status Register |
| 0x01C2 3048 | INTERRUPT | Interrupt Enable Register |
| 0x01C2 304C | COMPLSB | Compensation (LSB) Register |
| 0x01C2 3050 | COMPMSB | Compensation (MSB) Register |
| 0x01C2 3054 | OSC | Oscillator Register |
| 0x01C2 3060 | SCRATCH0 | Scratch 0 (General-Purpose) Register |
| 0x01C2 3064 | SCRATCH1 | Scratch 1 (General-Purpose) Register |
| 0x01C2 3068 | SCRATCH2 | Scratch 2 (General-Purpose) Register |
| 0x01C2 306C | KICK0 | Kick 0 (Write Protect) Register |
| 0x01C2 3070 | KICK1 | Kick 1 (Write Protect) Register |

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## 6.23 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GPIO [0:15]).

The device GPIO peripheral supports the following:

- Up to 144 Pins configurable as GPIO
- External Interrupt and DMA request Capability
  - Every GPIO pin may be configured to generate an interrupt request on detection of rising and/or falling edges on the pin.
  - The interrupt requests within each bank are combined (logical or) to create eight unique bank level interrupt requests.
  - The bank level interrupt service routine may poll the INTSTATx register for its bank to determine which pin(s) have triggered the interrupt.
  - GPIO Banks 0, 1, 2, 3, 4, 5, 6, 7, and 8 Interrupts assigned to DSP Events 65, 41, 49, 52, 54, 59, 62, 72, and 75 respectively
  - GPIO Banks 0, 1, 2, 3, 4, and 5 are assigned to EDMA events 6, 7, 22, 23, 28, 29, and 29 respectively on Channel Controller 0 and GPIO Banks 6, 7, and 8 are assigned to EDMA events 16, 17, and 18 respectively on Channel Controller 1.
- Set/clear functionality: Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

The memory map for the GPIO registers is shown in Table 6-82.


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### 6.23.1 GPIO Register Description(s)

**Table 6-82. GPIO Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 6000 | REV | Peripheral Revision Register |
| 0x01E2 6004 | RESERVED | Reserved |
| 0x01E2 6008 | BINTEN | GPIO Interrupt Per-Bank Enable Register |
| **GPIO Banks 0 and 1** | | |
| 0x01E2 6010 | DIR01 | GPIO Banks 0 and 1 Direction Register |
| 0x01E2 6014 | OUT_DATA01 | GPIO Banks 0 and 1 Output Data Register |
| 0x01E2 6018 | SET_DATA01 | GPIO Banks 0 and 1 Set Data Register |
| 0x01E2 601C | CLR_DATA01 | GPIO Banks 0 and 1 Clear Data Register |
| 0x01E2 6020 | IN_DATA01 | GPIO Banks 0 and 1 Input Data Register |
| 0x01E2 6024 | SET_RIS_TRIG01 | GPIO Banks 0 and 1 Set Rising Edge Interrupt Register |
| 0x01E2 6028 | CLR_RIS_TRIG01 | GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register |
| 0x01E2 602C | SET_FAL_TRIG01 | GPIO Banks 0 and 1 Set Falling Edge Interrupt Register |
| 0x01E2 6030 | CLR_FAL_TRIG01 | GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register |
| 0x01E2 6034 | INTSTAT01 | GPIO Banks 0 and 1 Interrupt Status Register |
| **GPIO Banks 2 and 3** | | |
| 0x01E2 6038 | DIR23 | GPIO Banks 2 and 3 Direction Register |
| 0x01E2 603C | OUT_DATA23 | GPIO Banks 2 and 3 Output Data Register |
| 0x01E2 6040 | SET_DATA23 | GPIO Banks 2 and 3 Set Data Register |
| 0x01E2 6044 | CLR_DATA23 | GPIO Banks 2 and 3 Clear Data Register |
| 0x01E2 6048 | IN_DATA23 | GPIO Banks 2 and 3 Input Data Register |
| 0x01E2 604C | SET_RIS_TRIG23 | GPIO Banks 2 and 3 Set Rising Edge Interrupt Register |
| 0x01E2 6050 | CLR_RIS_TRIG23 | GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register |
| 0x01E2 6054 | SET_FAL_TRIG23 | GPIO Banks 2 and 3 Set Falling Edge Interrupt Register |
| 0x01E2 6058 | CLR_FAL_TRIG23 | GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register |
| 0x01E2 605C | INTSTAT23 | GPIO Banks 2 and 3 Interrupt Status Register |
| **GPIO Banks 4 and 5** | | |
| 0x01E2 6060 | DIR45 | GPIO Banks 4 and 5 Direction Register |
| 0x01E2 6064 | OUT_DATA45 | GPIO Banks 4 and 5 Output Data Register |
| 0x01E2 6068 | SET_DATA45 | GPIO Banks 4 and 5 Set Data Register |
| 0x01E2 606C | CLR_DATA45 | GPIO Banks 4 and 5 Clear Data Register |
| 0x01E2 6070 | IN_DATA45 | GPIO Banks 4 and 5 Input Data Register |
| 0x01E2 6074 | SET_RIS_TRIG45 | GPIO Banks 4 and 5 Set Rising Edge Interrupt Register |
| 0x01E2 6078 | CLR_RIS_TRIG45 | GPIO Banks 4 and 5 Clear Rising Edge Interrupt Register |
| 0x01E2 607C | SET_FAL_TRIG45 | GPIO Banks 4 and 5 Set Falling Edge Interrupt Register |
| 0x01E2 6080 | CLR_FAL_TRIG45 | GPIO Banks 4 and 5 Clear Falling Edge Interrupt Register |
| 0x01E2 6084 | INTSTAT45 | GPIO Banks 4 and 5 Interrupt Status Register |

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**Table 6-82. GPIO Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| **GPIO Banks 6 and 7** | | |
| 0x01E2 6088 | DIR67 | GPIO Banks 6 and 7 Direction Register |
| 0x01E2 608C | OUT_DATA67 | GPIO Banks 6 and 7 Output Data Register |
| 0x01E2 6090 | SET_DATA67 | GPIO Banks 6 and 7 Set Data Register |
| 0x01E2 6094 | CLR_DATA67 | GPIO Banks 6 and 7 Clear Data Register |
| 0x01E2 6098 | IN_DATA67 | GPIO Banks 6 and 7 Input Data Register |
| 0x01E2 609C | SET_RIS_TRIG67 | GPIO Banks 6 and 7 Set Rising Edge Interrupt Register |
| 0x01E2 60A0 | CLR_RIS_TRIG67 | GPIO Banks 6 and 7 Clear Rising Edge Interrupt Register |
| 0x01E2 60A4 | SET_FAL_TRIG67 | GPIO Banks 6 and 7 Set Falling Edge Interrupt Register |
| 0x01E2 60A8 | CLR_FAL_TRIG67 | GPIO Banks 6 and 7 Clear Falling Edge Interrupt Register |
| 0x01E2 60AC | INTSTAT67 | GPIO Banks 6 and 7 Interrupt Status Register |
| **GPIO Bank 8** | | |
| 0x01E2 60B0 | DIR8 | GPIO Bank 8 Direction Register |
| 0x01E2 60B4 | OUT_DATA8 | GPIO Bank 8 Output Data Register |
| 0x01E2 60B8 | SET_DATA8 | GPIO Bank 8 Set Data Register |
| 0x01E2 60BC | CLR_DATA8 | GPIO Bank 8 Clear Data Register |
| 0x01E2 60C0 | IN_DATA8 | GPIO Bank 8 Input Data Register |
| 0x01E2 60C4 | SET_RIS_TRIG8 | GPIO Bank 8 Set Rising Edge Interrupt Register |
| 0x01E2 60C8 | CLR_RIS_TRIG8 | GPIO Bank 8 Clear Rising Edge Interrupt Register |
| 0x01E2 60CC | SET_FAL_TRIG8 | GPIO Bank 8 Set Falling Edge Interrupt Register |
| 0x01E2 60D0 | CLR_FAL_TRIG8 | GPIO Bank 8 Clear Falling Edge Interrupt Register |
| 0x01E2 60D4 | INTSTAT8 | GPIO Bank 8 Interrupt Status Register |


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### 6.23.2 GPIO Peripheral Input/Output Electrical Data/Timing

**Table 6-83. Timing Requirements for GPIO Inputs(1) (see Figure 6-53)**

| NO. | | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(GPIH)}$ | Pulse duration, GP*n*[*m*] as input high | 2C(1) (2) | | ns |
| 2 | $t_{w(GPIL)}$ | Pulse duration, GP*n*[*m*] as input low | 2C(1) (2) | | ns |

(1) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns.

**Table 6-84. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 6-53)**

| NO. | PARAMETER | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 3 | $t_{w(GPOH)}$ | Pulse duration, GP*n*[*m*] as output high | 2C(1) (2) | | ns |
| 4 | $t_{w(GPOL)}$ | Pulse duration, GP*n*[*m*] as output low | 2C(1) (2) | | ns |

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C=SYSCLK4 period in ns.

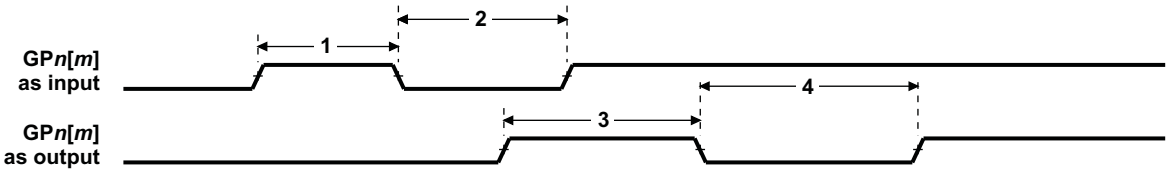



**Figure 6-53. GPIO Port Timing**

### 6.23.3 GPIO Peripheral External Interrupts Electrical Data/Timing

**Table 6-85. Timing Requirements for External Interrupts(1) (see Figure 6-54)**

| NO. | | | 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(ILOW)}$ | Width of the external interrupt pulse low | 2C(1) (2) | | ns |
| 2 | $t_{w(IHIGH)}$ | Width of the external interrupt pulse high | 2C(1) (2) | | ns |

(1) The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns.

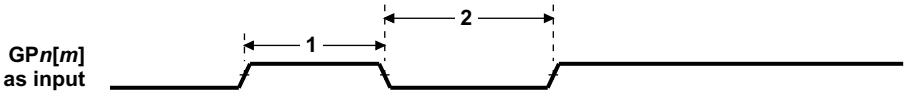



**Figure 6-54. GPIO External Interrupt Timing**

## 6.24 Emulation Logic

The debug capabilities and features for DSP are as shown below.

**DSP:**

- Basic Debug
  - Execution Control
  - System Visibility
- Real-Time Debug
  - Interrupts serviced while halted
  - Low/non-intrusive system visibility while running
- Advanced Debug
  - Global Start
  - Global Stop
  - Specify targeted memory level(s) during memory accesses
  - HSRTDX (High Speed Real Time Data eXchange)
- Advanced System Control
  - Subsystem reset via debug
  - Peripheral notification of debug events
  - Cache-coherent debug accesses
- Analysis Actions
  - Stop program execution
  - Generate debug interrupt
  - Benchmarking with counters
  - External trigger generation
  - Debug state machine state transition
  - Combinational and Sequential event generation
- Analysis Events
  - Program event detection
  - Data event detection
  - External trigger Detection
  - System event detection (i.e. cache miss)
  - Debug state machine state detection
- Analysis Configuration
  - Application access
  - Debugger access

**Table 6-86. DSP Debug Features**

| Category | Hardware Feature | Availability |
|---|---|---|
| Basic Debug | Software breakpoint | Unlimited |
| | Hardware breakpoint | Up to 10 HWBPs, including:<br>4 precise(1) HWBPs inside DSP core and one of them is associated with a counter.<br>2 imprecise(1) HWBPs from AET.<br>4 imprecise(1) HWBPs from AET which are shared for watch point. |

(1) Precise hardware breakpoints will halt the processor immediately prior to the execution of the selected instruction. Imprecise breakpoints will halt the processor some number of cycles after the selected instruction depending on device conditions.


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**Table 6-86. DSP Debug Features (continued)**

| Category | Hardware Feature | Availability |
|---|---|---|
| Analysis | Watch point | Up to 4 watch points, which are shared with HWBPs, and can also be used as 2 watch points with data (32 bits) |
| | Watch point with Data | Up to 2, Which can also be used as 4 watch points. |
| | Counters/timers | 1x64-bits (cycle only) + 2x32-bits (water mark counters) |
| | External Event Trigger In | 1 |
| | External Event Trigger Out | 1 |

### 6.24.1 JTAG Port Description

The device target debug interface uses the five standard IEEE 1149.1(JTAG) signals ($\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO).

$\overline{\text{TRST}}$ holds the debug and boundary scan logic in reset (normal DSP operation) when pulled low (its default state). Since $\overline{\text{TRST}}$ has an internal pull-down resistor, this ensures that at power up the device functions in its normal (non-test) operation mode if $\overline{\text{TRST}}$ is not connected. Otherwise, $\overline{\text{TRST}}$ should be driven inactive by the emulator or boundary scan controller. Boundary scan test cannot be performed while the $\overline{\text{TRST}}$ pin is pulled low.

**Table 6-87. JTAG Port Description**

| PIN | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| $\overline{\text{TRST}}$ | I | Test Logic Reset | When asserted (active low) causes all test and debug logic in the device to be reset along with the IEEE 1149.1 interface |
| TCK | I | Test Clock | This is the test clock used to drive an IEEE 1149.1 TAP state machine and logic. |
| TMS | I | Test Mode Select | Directs the next state of the IEEE 1149.1 test access port state machine |
| TDI | I | Test Data Input | Scan data input to the device |
| TDO | O | Test Data Output | Scan data output of the device |
| EMU0 | I/O | Emulation 0 | Channel 0 trigger + HSRTDX |
| EMU1 | I/O | Emulation 1 | Channel 1 trigger + HSRTDX |

### 6.24.2 Scan Chain Configuration Parameters

Table 6-88 shows the TAP configuration details required to configure the router/emulator for this device.

**Table 6-88. JTAG Port Description**

| Router Port ID | Default TAP | TAP Name | Tap IR Length |
|---|---|---|---|
| 17 | No | C674x | 38 |
| 19 | No | ETB | 4 |

The router is revision C and has a 6-bit IR length.

### 6.24.3 Initial Scan Chain Configuration

The first level of debug interface that sees the scan controller is the TAP router module. The debugger can configure the TAP router for serially linking up to 16 TAP controllers or individually scanning one of the TAP controllers without disrupting the IR state of the other TAPs.

### 6.24.4 IEEE 1149.1 JTAG

The JTAG (1) interface is used for BSDL testing and emulation of the device.

The device requires that both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ be asserted upon power up to be properly initialized. While $\overline{\text{RESET}}$ initializes the device, $\overline{\text{TRST}}$ initializes the device's emulation logic. Both resets are required for proper operation.

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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While both TRST and RESET need to be asserted upon power up, only RESET needs to be released for the device to boot properly. TRST may be asserted indefinitely for normal operation, keeping the JTAG port interface and device's emulation logic in the reset state.

TRST only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. Note: TRST is synchronous and ***must*** be clocked by TCK; otherwise, the boundary scan logic may not respond as expected after TRST is asserted.

RESET must be released only in order for boundary-scan JTAG to read the variant field of IDCODE correctly. Other boundary-scan instructions work correctly independent of current state of RESET.

For maximum reliability, the device includes an internal pulldown (IPD) on the TRST pin to ensure that TRST will always be asserted upon power up and the device's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of a pullup resistor on TRST.

When using this type of JTAG controller, assert TRST to initialize the device after powerup and externally drive TRST high before attempting any emulation or boundary scan operations.

### 6.24.4.1 JTAG Peripheral Register Description(s) – JTAG ID Register (DEVIDR0)

**Table 6-89. DEVIDR0 Register**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | COMMENTS |
|---|---|---|---|
| 0x01C1 4018 | DEVIDR0 | JTAG Identification Register | Read-only. Provides 32-bit JTAG ID of the device. |

The JTAG ID register is a read-only register that identifies the JTAG/Device ID. For the device, the JTAG ID register resides at address location 0x01C1 4018. The register hex value for each silicon revision is:

- 0x0B7D 102F for silicon revision 1.x
- 0x1B7D 102F for silicon revision 2.x

For the actual register bit names and their associated bit field descriptions, see Figure 6-55 and Table 6-90.

**Figure 6-55. JTAG ID (DEVIDR0) Register Description - Register Value**

| 31-28 | 27-12 | 11-1 | 0 |
|---|---|---|---|
| VARIANT (4-Bit) | PART NUMBER (16-Bit) | MANUFACTURER (11-Bit) | LSB |
| R-xxxx | R-1011 0111 1101 0001 | R-0000 0010 111 | R-1 |

LEGEND: R = Read, W = Write, n = value at reset

**Table 6-90. JTAG ID Register Selection Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:28 | VARIANT | Variant (4-Bit) value |
| 27:12 | PART NUMBER | Part Number (16-Bit) value |
| 11-1 | MANUFACTURER | Manufacturer (11-Bit) value |
| 0 | LSB | LSB. This bit is read as a "1". |


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#### 6.24.4.2 JTAG Test-Port Electrical Data/Timing

**Table 6-91. Timing Requirements for JTAG Test Port (see Figure 6-56)**

| No. | | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 40 | | 50 | | 66.6 | | ns |
| 2 | $t_{w(TCKH)}$ | Pulse duration, TCK high | 16 | | 20 | | 26.6 | | ns |
| 3 | $t_{w(TCKL)}$ | Pulse duration, TCK low | 16 | | 20 | | 26.6 | | ns |
| 4 | $t_{su(TDIV-TCKH)}$ | Setup time, TDI/TMS/$\overline{TRST}$ valid before TCK high | 4 | | 4 | | 4 | | ns |
| 5 | $t_{h(TCLKH-TDIV)}$ | Hold time, TDI/TMS/$\overline{TRST}$ valid after TCK high | 4 | | 6 | | 8 | | ns |

**Table 6-92. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 6-56)**

| No. | PARAMETER | | 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 6 | $t_{d(TCKL-TDOV)}$ | Delay time, TCK low to TDO valid | | 18 | | 23 | | 31 | ns |

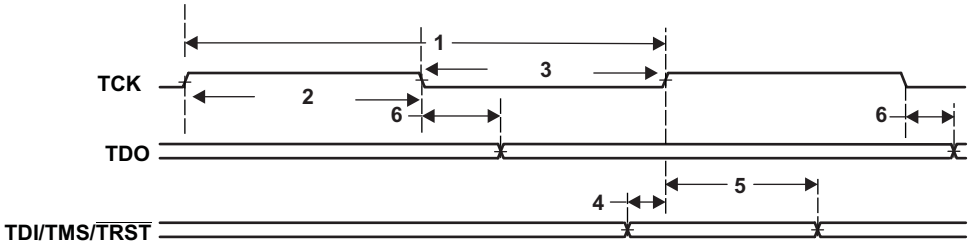



**Figure 6-56. JTAG Test-Port Timing**

### 6.24.5 JTAG 1149.1 Boundary Scan Considerations

To use boundary scan, the following sequence should be followed:

- Execute a valid reset sequence and exit reset
- Wait at least 6000 OSCIN clock cycles
- Enter boundary scan mode using the JTAG pins

No specific value is required on the EMU0 and EMU1 pins for boundary scan testing. If TRST is not driven by the boundary scan tool or tester, TRST should be externally pulled high during boundary scan testing.

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# 7 Device and Documentation Support

TI offers an extensive line of development tools for the device platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the device applications:

## 7.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320C6745). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications.

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**TMS** Fully-qualified production device.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

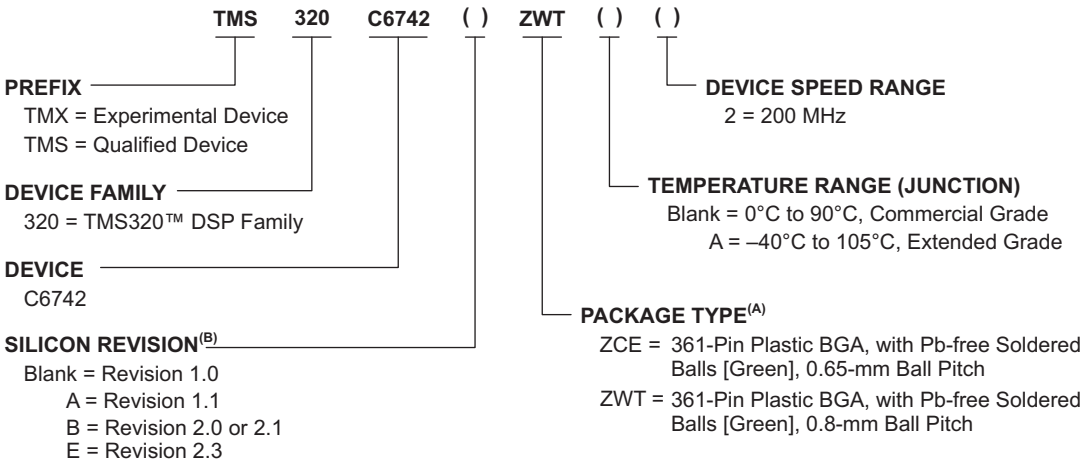
TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZWT), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "Blank" is the default).

Figure 7-1 provides a legend for reading the complete device.


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A. BGA = Ball Grid Array
B. Parts marked revision B are silicon revision 2.1 if '21' is marked on the package, and silicon revision 2.0 if there is no '21' marking.

**Figure 7-1. Device Nomenclature**

## 7.2 Tools and Software

### Software

**Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools**

**Scalable, Real-Time Foundation Software (DSP/BIOS™)** provides the basic run-time target software needed to support any application.

### Development Tools

**Extended Development System (XDS™) Emulator** For a complete listing of development-support tools for the device, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 7.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral is listed below.

### User's Guides

**SPRUG82** ***TMS320C674x DSP Cache User's Guide.*** Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C674x digital signal processor (DSP) can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C674x DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

**SPRUFE8** ***TMS320C674x DSP CPU and Instruction Set Reference Guide***. Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C674x digital signal processors (DSPs). The C674x DSP is an enhancement of the C64x+ and C67x+ DSPs with added functionality and an expanded instruction set.

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**SPRUFK5** ***TMS320C674x DSP Megamodule Reference Guide***. Describes the TMS320C674x digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

**SPRUFK9** ***TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide***. Provides an overview and briefly describes the peripherals available on the device.

**SPRUGM5** ***TMS320C6742 DSP System Reference Guide***. Describes the System-on-Chip (SoC) system. The SoC system includes TI's standard TMS320C674x Megamodule and several blocks of internal memory (L1P, L1D, and L2).

**Technical Reference Manuals**

## 7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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## 7.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.


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# 8 Mechanical Packaging and Orderable Information

This section describes the orderable part numbers, packaging options, materials, thermal and mechanical parameters.

## 8.1 Thermal Data for ZCE Package

The following table shows the thermal resistance characteristics for the PBGA–ZCE mechanical package.

**表 8-1. Thermal Resistance Characteristics (PBGA Package) [ZCE]**

| NO. | | | °C/W(1) | AIR FLOW (m/s)(2) |
|---|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 7.6 | N/A |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 11.3 | N /A |
| 3 | $R\Theta_{JA}$ | Junction-to-free air | 23.9 | 0.00 |
| 4 | $R\Theta_{JMA}$ | Junction-to-moving air | 21.2 | 0.50 |
| 5 | | | 20.3 | 1.00 |
| 6 | | | 19.5 | 2.00 |
| 7 | | | 18.6 | 4.00 |
| 8 | $Psi_{JT}$ | Junction-to-package top | 0.2 | 0.00 |
| 9 | | | 0.3 | 0.50 |
| 10 | | | 0.3 | 1.00 |
| 11 | | | 0.4 | 2.00 |
| 12 | | | 0.5 | 4.00 |
| 13 | $Psi_{JB}$ | Junction-to-board | 11.2 | 0.00 |
| 14 | | | 11.1 | 0.50 |
| 15 | | | 11.1 | 1.00 |
| 16 | | | 11.0 | 2.00 |
| 17 | | | 10.9 | 4.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. Power dissipation of 500 mW and ambient temp of 70C assumed. PCB with 2oz (70um) top and bottom copper thickness and 1.5oz (50um) inner copper thickness

(2) m/s = meters per second

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## 8.2 Thermal Data for ZWT Package

The following table shows the thermal resistance characteristics for the PBGA–ZWT mechanical package.

**表 8-2. Thermal Resistance Characteristics (PBGA Package) [ZWT]**

| NO. | | | °C/W(1) | AIR FLOW (m/s)(2) |
|---|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 7.3 | N/A |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 12.4 | N /A |
| 3 | $R\Theta_{JA}$ | Junction-to-free air | 23.7 | 0.00 |
| 4 | $R\Theta_{JMA}$ | Junction-to-moving air | 21.0 | 0.50 |
| 5 | | | 20.1 | 1.00 |
| 6 | | | 19.3 | 2.00 |
| 7 | | | 18.4 | 4.00 |
| 8 | $Psi_{JT}$ | Junction-to-package top | 0.2 | 0.00 |
| 9 | | | 0.3 | 0.50 |
| 10 | | | 0.3 | 1.00 |
| 11 | | | 0.4 | 2.00 |
| 12 | | | 0.5 | 4.00 |
| 13 | $Psi_{JB}$ | Junction-to-board | 12.3 | 0.00 |
| 14 | | | 12.2 | 0.50 |
| 15 | | | 12.1 | 1.00 |
| 16 | | | 12.0 | 2.00 |
| 17 | | | 11.9 | 4.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. Power dissipation of 1W and ambient temp of 70C assumed. PCB with 2oz (70um) top and bottom copper thickness and 1.5oz (50um) inner copper thickness

(2) m/s = meters per second

## 8.3 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMS320C6742EZWT2 | Active | Production | NFBGA (ZWT) \| 361 | 90 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | 0 to 90 | TMS320 C6742EZWT 200 |
| TMS320C6742EZWT2.B | Active | Production | NFBGA (ZWT) \| 361 | 90 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | 0 to 90 | TMS320 C6742EZWT 200 |
| TMS320C6742EZWTA2 | Active | Production | NFBGA (ZWT) \| 361 | 90 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 C6742EZWT A200 |
| TMS320C6742EZWTA2.B | Active | Production | NFBGA (ZWT) \| 361 | 90 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 105 | TMS320 C6742EZWT A200 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

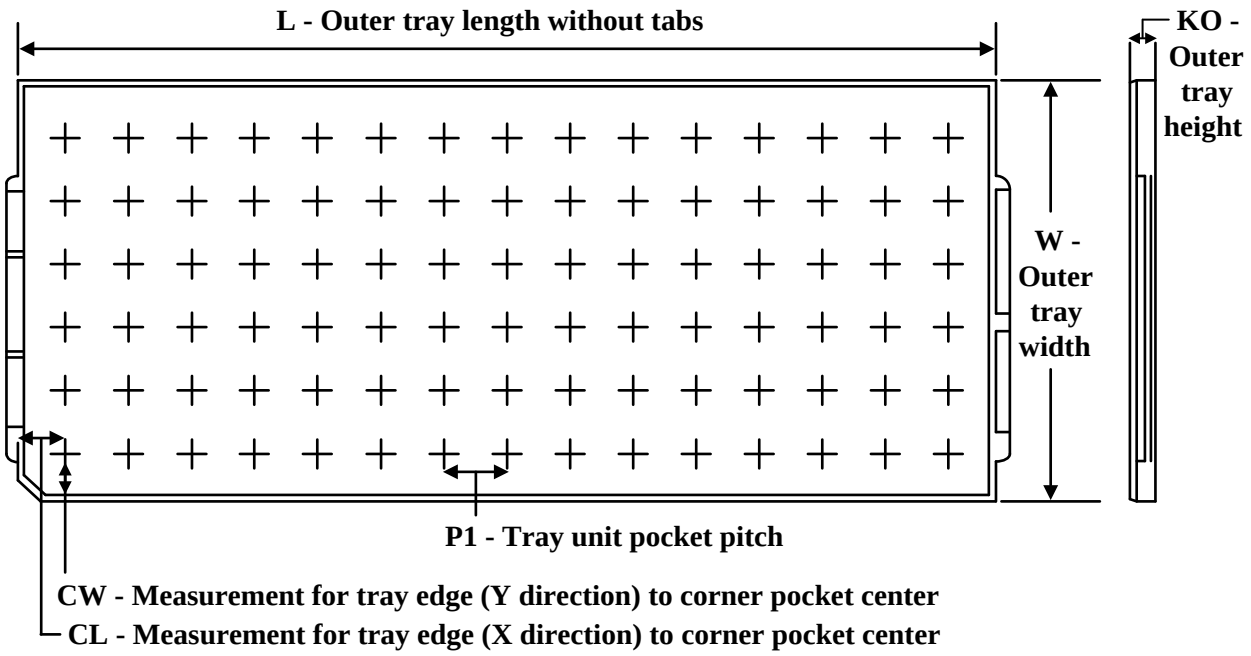
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TRAY

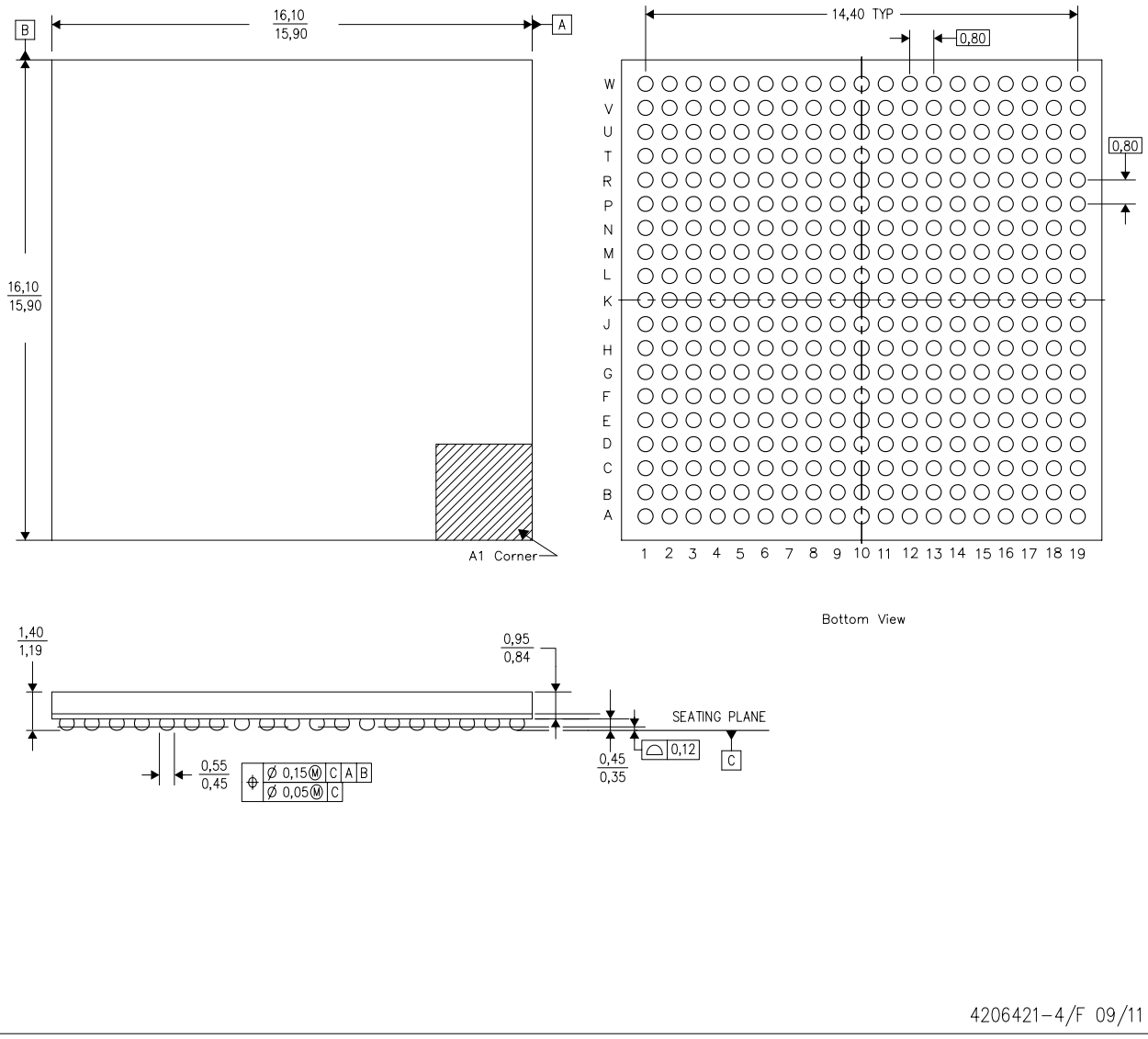



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320C6742EZWT2 | ZWT | NFBGA | 361 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| TMS320C6742EZWT2.B | ZWT | NFBGA | 361 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| TMS320C6742EZWTA2 | ZWT | NFBGA | 361 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| TMS320C6742EZWTA2.B | ZWT | NFBGA | 361 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |

ZWT (S–PBGA–N361) PLASTIC BALL GRID ARRAY



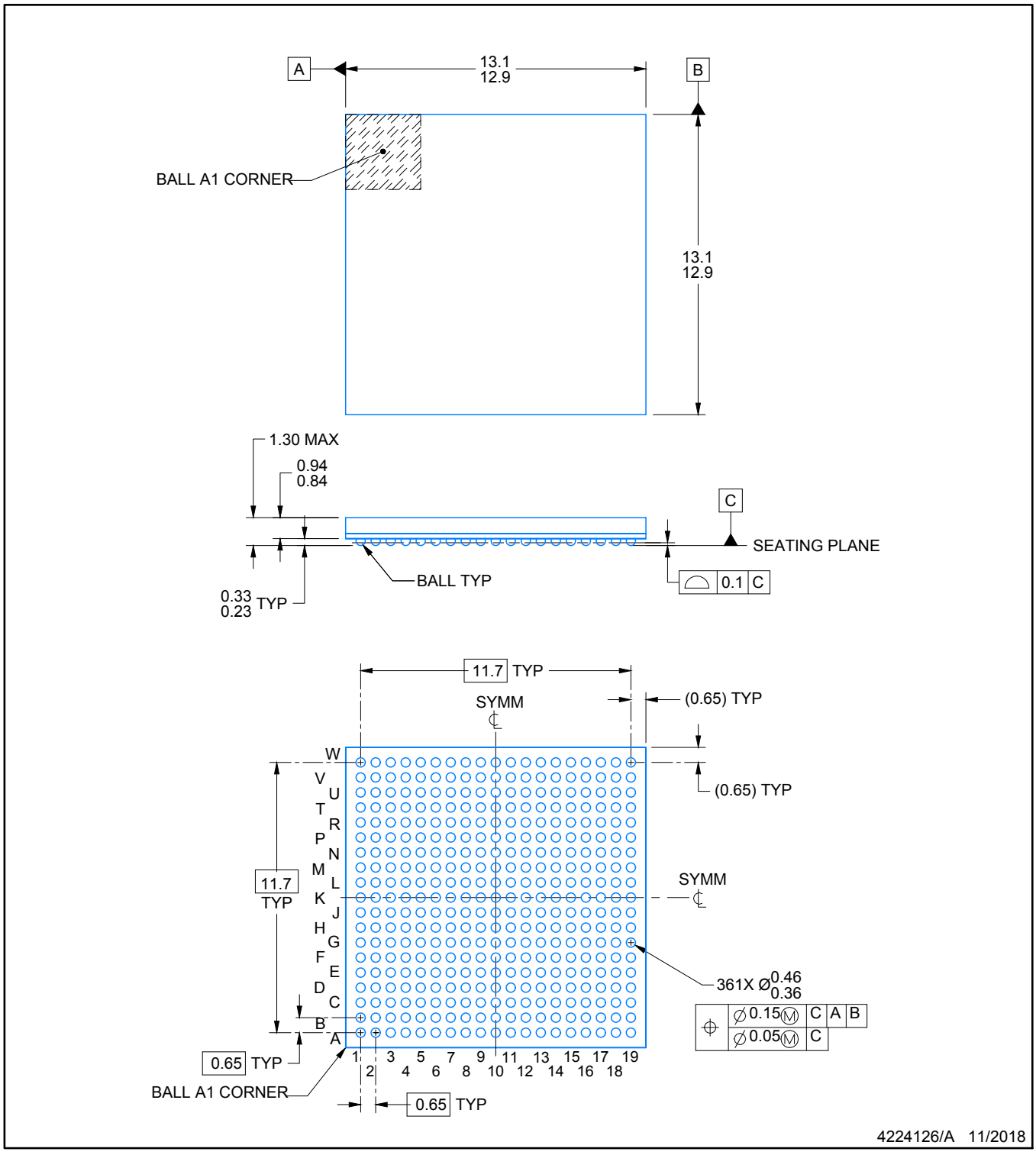

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.
D. Falls within JEDEC MO–275.

# PACKAGE OUTLINE

## ZCE0361A

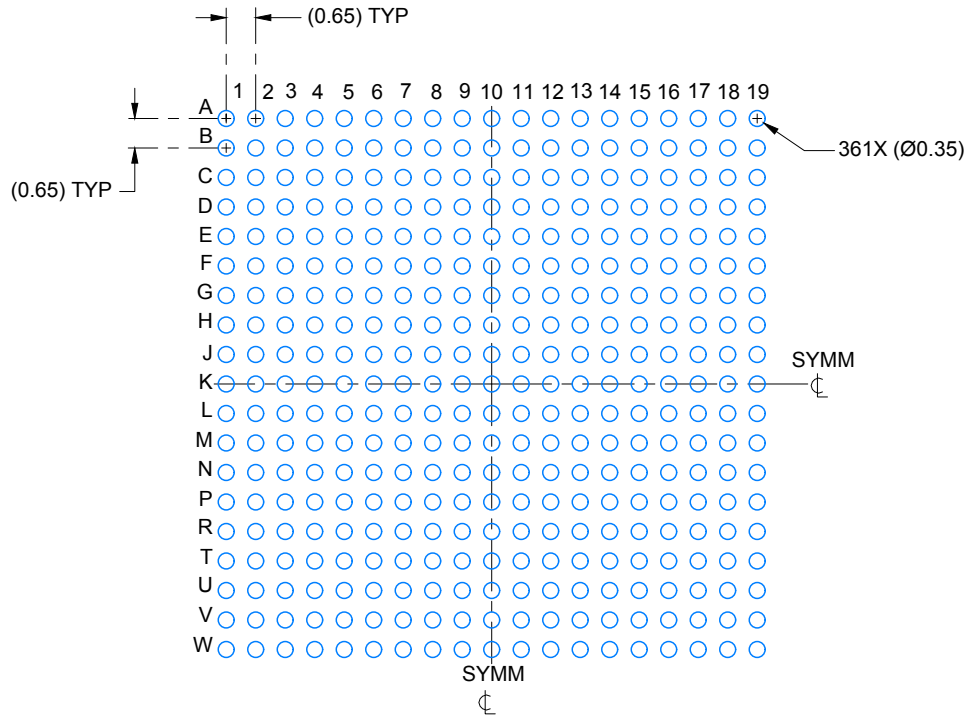
## NFBGA - 1.30 mm max height

PLASTIC BALL GRID ARRAY




NOTES:

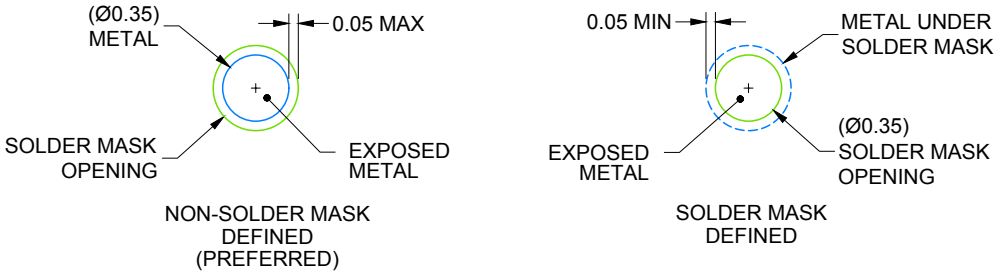
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 6X



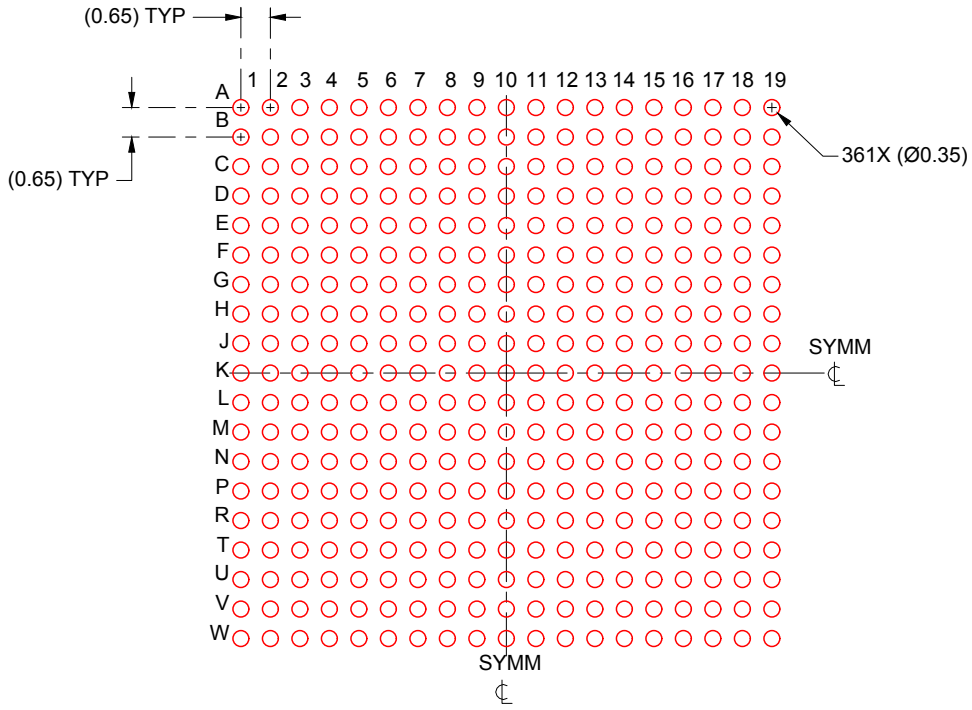

SOLDER MASK DETAILS

NOT TO SCALE

4224126/A 11/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4224126/A 11/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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