TMS320F28377D-EP デュアルコアDelfino™マイクロコントローラ

1 デバイスの概要

1.1 特長

- デュアルコアのアーキテクチャ
  - 2つのTMS320C28x 32ビットCPU
  - 200MHz
  - IEEE 754単精度浮動小数点ユニット(FPU)
  - 三角関数算術演算ユニット(TMU)
  - ビタビ/複素数演算ユニット(VCU-II)
- 2つのプログラム可能な制御補償器アクセラレータ(CLA)
  - 200MHz
  - IEEE 754単精度浮動小数点命令
  - メインCPUと独立にコードを実行
- オンチップ・メモリ
  - 512KB (256KW)または1MB (512KW)のフラッシュ(ECC保護)
  - 172KB (86KW)または204KB (102KW)のRAM (ECC保護またはパリティ保護)
  - デュアル・ゾーンのセキュリティでサードパーティーの開発をサポート
- クロックおよびシステム制御
  - 2つの内部ゼロ・ピン10MHz発振器
  - オンチップの水晶振動子
  - ウィンドウ付きウォッチドッグ・タイマ・モジュール
  - クロック消失検出回路
- コア1.2V、I/O 3.3Vの設計
- システム・ペリフェラル
  - ASRAMおよびSDRAMをサポートする2つの外部メモリ・インターフェイス(EMIF)
  - デュアル6チャネルのDMA (Direct Memory Access)コントローラ
  - 最大169の個別にプログラム可能な、多重化された、入力フィルタリング付き汎用入出力(GPIO)ピン
  - 拡張ペリフェラル割り込みコントローラ(ePIE)
  - 複数の低消費電力モード(LPM)サポートと外部的なウェークアップ
- 通信ペリフェラル
  - USB 2.0 (MAC + PHY)
  - 12ピンの3.3V互換ユニバーサル・パラレル・ポート(uPP)インターフェイスをサポート
  - 2つのCAN (Controller Area Network)モジュール(ピンでブート可能)
  - 3つの高速(最高50MHz) SPIポート(ピンでブート可能)
  - 2つのマルチチャネル・バッファ付きシリアル・ポート(McBSP)
  - 4つのシリアル通信インターフェイス(SCI/UART) (ピンでブート可能)
  - 2つのI2Cインターフェイス(ピンでブート可能)
- アナログ・サブシステム
  - 最大4つのアナログ/デジタル・コンバータ(ADC)
    - 16ビット・モード
      - 各1.1MSPS (最大4.4MSPSのシステム・スループット)
      - 差動入力
      - 最大12の外部チャネル
    - 12ビット・モード
      - 各3.5MSPS (最大14MSPSのシステム・スループット)
      - シングルエンド入力
      - 最大24の外部チャネル
    - 各ADCに単一のサンプルおよびホールド(S/H)
    - ADC変換の後処理をハードウェアに内蔵
      - 飽和オフセット較正
      - 設定ポイント計算からの誤差
      - 高、低、およびゼロクロス比較、割り込み機能付き
      - トリガからサンプルまでの遅延の捕捉
  - 8つのウィンドウ付きコンパレータ、12ビットのデジタル/アナログ・コンバータ(DAC)リファレンス付き
  - 3つのバッファ付き12ビットDAC出力
- 拡張制御ペリフェラル
  - 拡張機能付きの、24個のパルス幅変調器(PWM)チャネル
  - 16個の高分解能パルス幅変調器(HRPWM)チャネル
    - 8つのPWMモジュールのAおよびBチャネルの両方が高分解能
    - デッドバンドのサポート(標準と高分解能の両方)
  - 6つの拡張キャプチャ(eCAP)モジュール
  - 3つの拡張直交エンコーダ・パルス(eQEP)モジュール
  - 8つのシグマ-デルタ・フィルタ・モジュール(SDFM)入力チャネル(チャネルごとに2つのパラレル・フィルタ)
    - 標準SDFMデータ・フィルタリング
    - コンパレータ・フィルタによる範囲外への迅速なアクション

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- パッケージ・オプション
  - 337ボールの新ファイン・ピッチ・ボール・グリッド・アレイ(nFBGA) [接尾辞GWT]
  - 176ピン PowerPAD™の熱的に強化された薄型クワッド・フラットパック(HLQFP) [接尾辞PTP]
- 防衛、航空宇宙、医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ/テスト施設
  - 単一の製造施設
  - 拡張温度範囲(-55℃～125℃)で使用可能
  - 長期にわたる製品ライフ・サイクル
  - 長期にわたる製品変更通知
  - 製品のトレーサビリティ

1.2 アプリケーション

- 先進運転支援システム(ADAS)
- ビルディング・オートメーション
- 電子POS
- 電気自動車/ハイブリッド電気自動車(EV/HEV)のパワートレイン
- ファクトリ・オートメーション
- グリッド・インフラストラクチャ
- 産業用輸送
- 医療、ヘルスケア、フィットネス
- モータ駆動
- パワー・デリバリ
- 通信インフラストラクチャ
- 試験および測定機器

1.3 概要

Delfino™ TMS320F28377D-EPは強力な32ビットの浮動小数点マイクロコントローラ・ユニット(MCU)で、産業用ドライブやサーボ・モータ制御、ソーラー・インバータおよびコンバータ、デジタル電源、輸送、電源ライン通信など、高度なクローズド・ループ制御アプリケーション向けに設計されています。デジタル電源および産業用ドライブ向けの完全な開発パッケージが、powerSUITEおよびDesignDRIVEイニシアチブの一部として利用できます。Delfino製品ラインは TMS320C2000™ポートフォリオで新しいものではありませんが、F28377Dは新しいデュアルコアC28xアーキテクチャをサポートし、システム性能が大幅に向上しています。また、内蔵のアナログおよび制御ペリフェラルにより、設計者は制御アーキテクチャを統合し、ハイエンド・システムでマルチプロセッサを不要にできます。

デュアル・リアルタイム制御サブシステムは、TIの32ビットC28x浮動小数点CPUを基礎としており、コアごとに200MHzの信号処理能力があります。C28x CPUは、新しいTMUアクセラレータによってさらに高速化され、変換やトルク・ループ計算で一般的な三角法演算を含むアルゴリズムを高速に実行できます。また、VCUアクセラレータにより、エンコード・アプリケーションで一般的な複素数演算の時間が短縮されます。

F28377Dマイクロコントローラには、2つのCLAリアルタイム制御コプロセッサが搭載されています。これらのCLAは独立した32ビットの浮動小数点プロセッサで、メインCPUと同じ速度で動作します。これらのCLAは、ペリフェラルのトリガに応答し、メインのC28x CPUと同時にコードを実行します。この並列処理能力により、リアルタイム制御システムの計算能力を実質的に2倍にできます。CLAを使用してタイムクリティカルな機能へのサービスを行うことで、メインのC28x CPUは他のタスク、たとえば通信や診断を自由に実行できます。デュアルのC28x+CLAアーキテクチャにより、各種のシステム・タスクをインテリジェントに分割できます。たとえば、1つのC28x+CLAコアを速度と位置の追跡に使用し、もう1つのC28x+CLAコアはトルクと電流ループの制御に使用できます。

TMS320F28377D-EPは、ECC (Error Correction Code)付きの1MB (512KW)のオンボード・フラッシュ・メモリと、204KB (102KW)のSRAMをサポートしています。各CPUでは、コード保護のため、2つの128ビットのセキュア・ゾーンも使用できます。

高性能のアナログおよび制御ペリフェラルもF28377D MCUに内蔵されており、さらにシステムの統合が可能になります。4つの独立した16ビットADCにより、複数のアナログ信号を正確かつ効率的に管理でき、最終的にシステムのスループットが向上します。新しいシグマ-デルタ・フィルタ・モジュール(SDFM)は、シグマ-デルタ変調器との組み合わせで動作し、絶縁電流シャント測定を可能にします。ウィンドウ・コンパレータ付きのコンパレータ・サブシステム(CMPSS)により、電流制限条件を超過した、または条件が満たされていない場合に、電源段を保護できます。他のアナログおよび制御ペリフェラルとして、DAC、PWM、eCAP、eQEP、その他のペリフェラルがあります。

EMIF、CANモジュール(ISO 11898-1/CAN 2.0B準拠)、新しいuPPインターフェイスなどのペリフェラルにより、F28377Dの接続性が拡大されます。uPPインターフェイスは C2000™ MCUの新機能で、FPGAや他のプロセッサへの高速パラレル接続を、同様なuPPインターフェイスでサポートします。最後に、MACおよびPHY付きのUSB 2.0ポートにより、ユーザーはアプリケーションにUSB (Universal Serial Bus)接続を簡単に追加できます。

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製品情報(1)

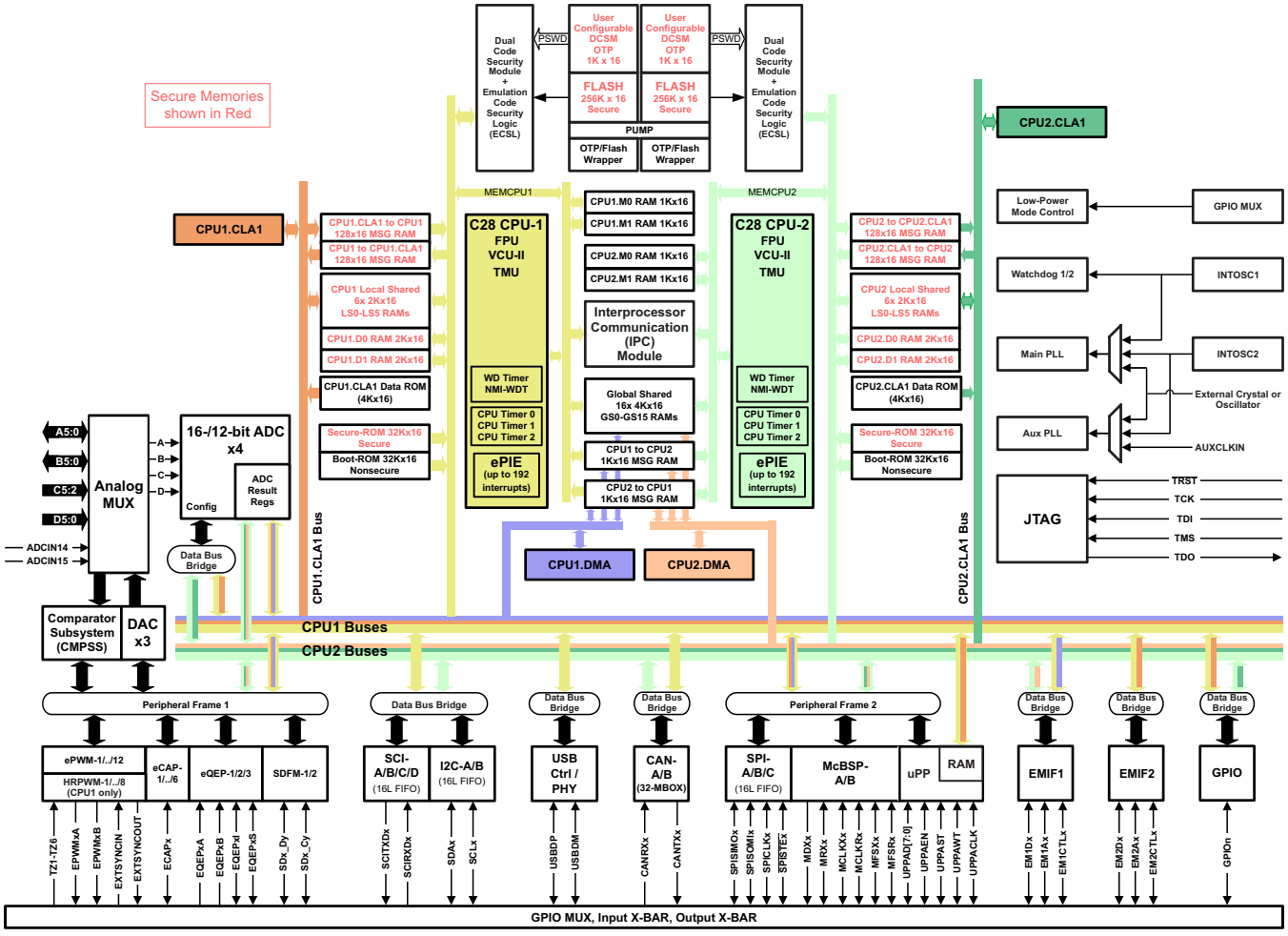
型番	パッケージ	本体サイズ
TMS320F28377D-EP	nFBGA (337)	16.0mm×16.0mm
	HLQFP (176)	24.0mm×24.0mm

(1) これらのデバイスの詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

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1.4 機能ブロック図

CPUシステムおよび関連ペリフェラルを、図 1-1に示します。



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図 1-1. 機能ブロック図

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年12月	*	初版

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3 Terminal Configuration and Functions

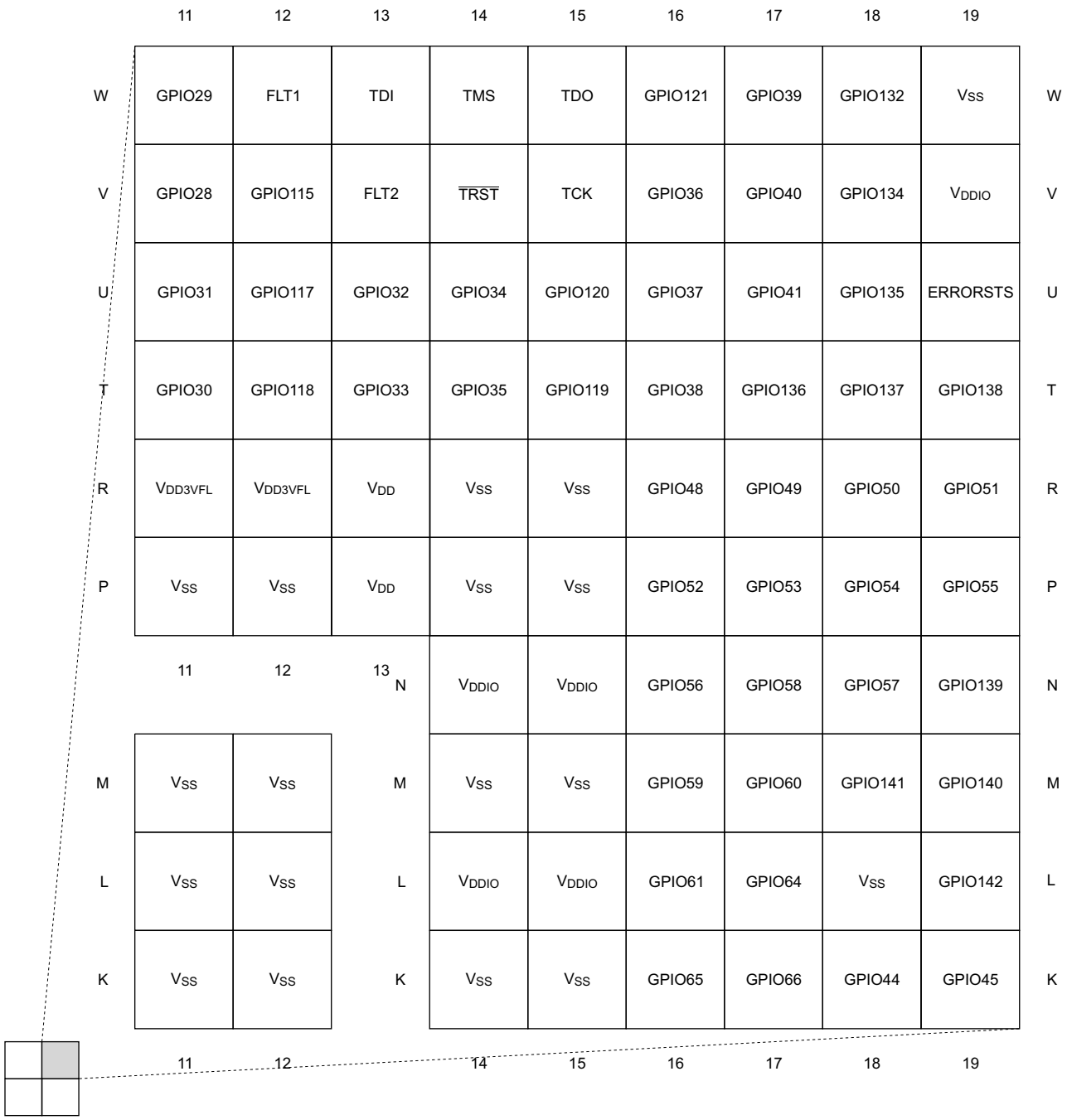
3.1 Pin Diagrams

Figure 3-1 to Figure 3-4 show the terminal assignments on the 337-ball ZWT New Fine Pitch Ball Grid Array. Each figure shows a quadrant of the terminal assignments. Figure 3-5 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack.

	1	2	3	4	5	6	7	8	9	10	
W	V_{SSA}	ADCINB1	ADCINB3	ADCINB5	V_{REFHIB}	V_{REFLOD}	V_{SS}	V_{DDIO}	GPIO128	GPIO116	W
V	V_{REFHIA}	ADCINB0	ADCINB2	ADCINB4	V_{REFHID}	V_{REFLOB}	V_{SSA}	GPIO124	GPIO127	GPIO131	V
U	ADCINA0	ADCINA2	ADCINA4	ADCIN15	ADCIND1	ADCIND3	ADCIND5	GPIO123	GPIO126	GPIO130	U
T	ADCINA1	ADCINA3	ADCINA5	ADCIN14	ADCIND0	ADCIND2	ADCIND4	GPIO122	GPIO125	GPIO129	T
R	V_{REFHIC}	V_{REFLOA}	ADCINC2	ADCINC4	V_{SSA}	V_{DDA}	V_{SS}	V_{SS}	V_{DDIO}	V_{DD}	R
P	V_{SSA}	V_{REFLOC}	ADCINC3	ADCINC5	V_{SSA}	V_{DDA}	V_{SS}	V_{SS}	V_{DDIO}	V_{DD}	P
N	V_{SS}	GPIO109	GPIO114	GPIO113	V_{SS}	V_{SS}	N				
M	V_{DDIO}	GPIO110	GPIO112	GPIO111	V_{DDIO}	V_{DDIO}	M	V_{SS}	V_{SS}	V_{SS}	M
L	GPIO27	GPIO106	GPIO107	GPIO108	V_{SS}	V_{SS}	L	V_{SS}	V_{SS}	V_{SS}	L
K	GPIO26	GPIO25	GPIO24	GPIO23	V_{DD}	V_{DD}	K	V_{SS}	V_{SS}	V_{SS}	K
	1	2	3	4	5	6	7	8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See Table 3-1 for the complete, muxed signal name.

Figure 3-1. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant A]

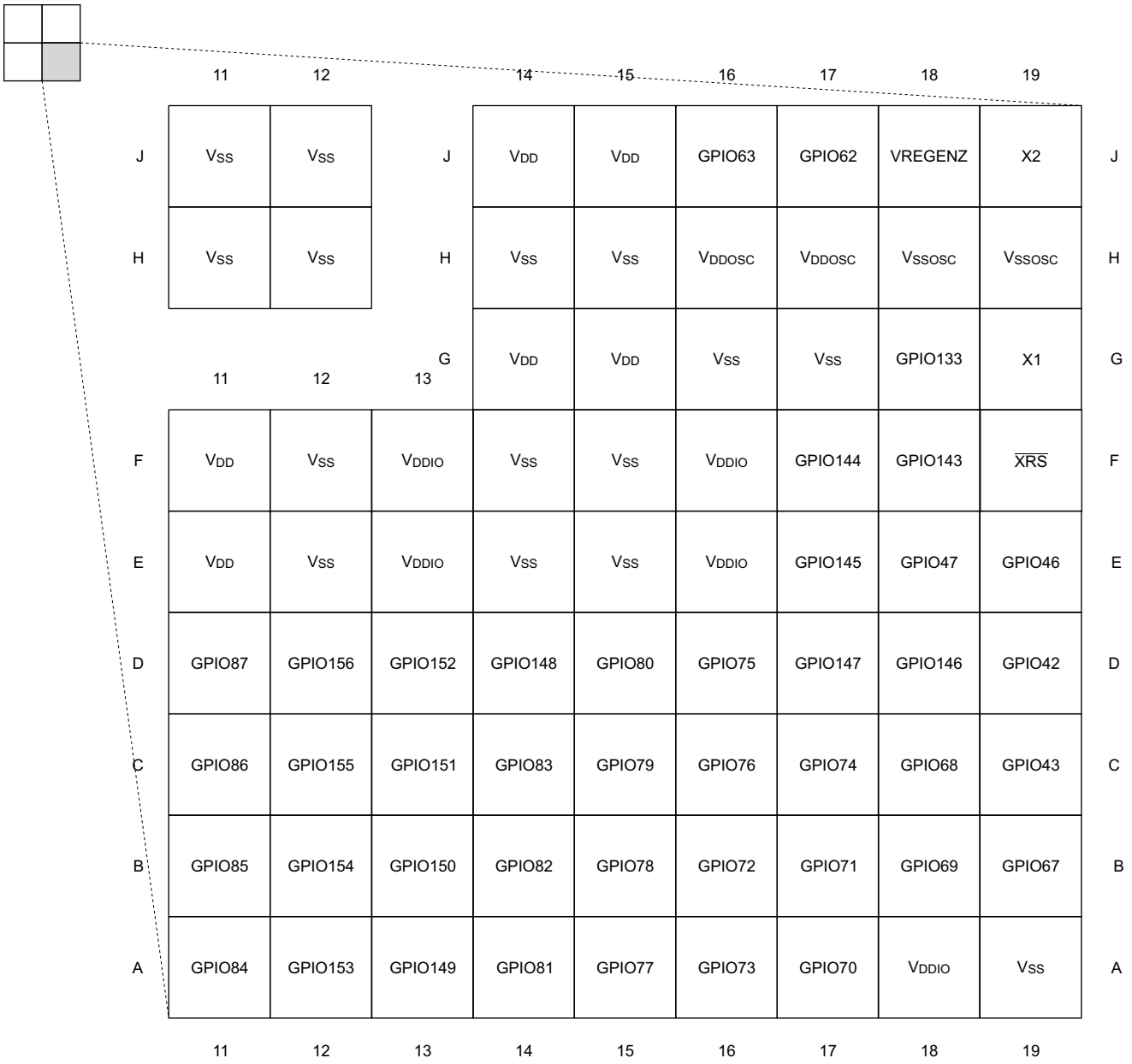


	11	12	13	14	15	16	17	18	19	
W	GPIO29	FLT1	TDI	TMS	TDO	GPIO121	GPIO39	GPIO132	V_{SS}	W
V	GPIO28	GPIO115	FLT2	$\overline{TRST}$	TCK	GPIO36	GPIO40	GPIO134	V_{DDIO}	V
U	GPIO31	GPIO117	GPIO32	GPIO34	GPIO120	GPIO37	GPIO41	GPIO135	ERRORSTS	U
T	GPIO30	GPIO118	GPIO33	GPIO35	GPIO119	GPIO38	GPIO136	GPIO137	GPIO138	T
R	V_{DD3VFL}	V_{DD3VFL}	V_{DD}	V_{SS}	V_{SS}	GPIO48	GPIO49	GPIO50	GPIO51	R
P	V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}	GPIO52	GPIO53	GPIO54	GPIO55	P
N	V_{DDIO}	V_{DDIO}	GPIO56	GPIO58	GPIO57	GPIO139				N
M	V_{SS}	V_{SS}	V_{SS}	V_{SS}	GPIO59	GPIO60	GPIO141	GPIO140		M
L	V_{SS}	V_{SS}	V_{DDIO}	V_{DDIO}	GPIO61	GPIO64	V_{SS}	GPIO142		L
K	V_{SS}	V_{SS}	V_{SS}	V_{SS}	GPIO65	GPIO66	GPIO44	GPIO45		K
	11	12	14	15	16	17	18	19		

A. Only the GPIO function is shown on GPIO terminals. See Table 3-1 for the complete, muxed signal name.

Figure 3-2. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant B]

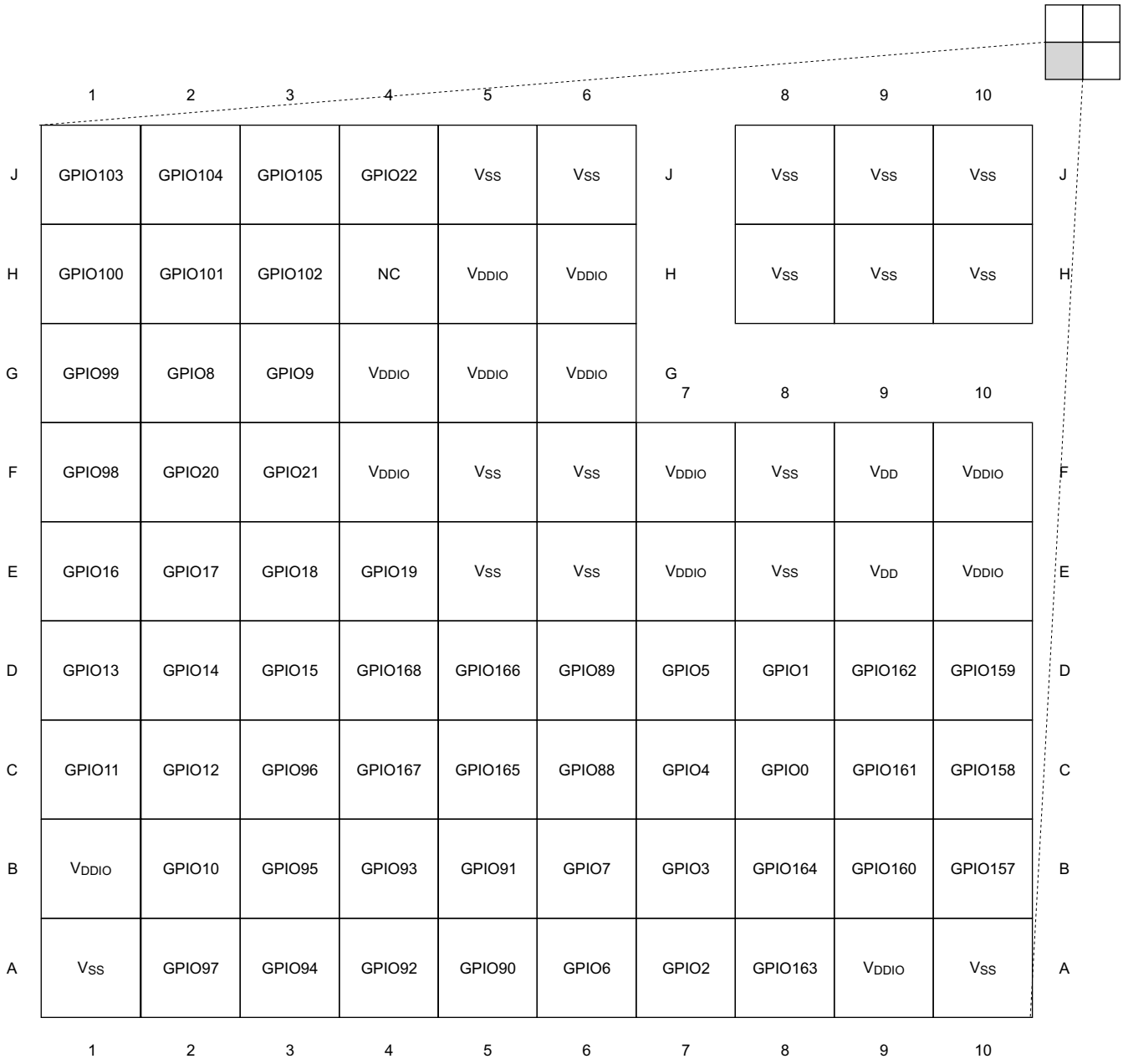
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	11	12	13	14	15	16	17	18	19	
J	V_{SS}	V_{SS}	J	V_{DD}	V_{DD}	GPIO63	GPIO62	VREGENZ	X2	J
H	V_{SS}	V_{SS}	H	V_{SS}	V_{SS}	V_{DDOSC}	V_{DDOSC}	V_{SSOSC}	V_{SSOSC}	H
	11	12	G 13	V_{DD}	V_{DD}	V_{SS}	V_{SS}	GPIO133	X1	G
F	V_{DD}	V_{SS}	V_{DDIO}	V_{SS}	V_{SS}	V_{DDIO}	GPIO144	GPIO143	$\overline{XRS}$	F
E	V_{DD}	V_{SS}	V_{DDIO}	V_{SS}	V_{SS}	V_{DDIO}	GPIO145	GPIO47	GPIO46	E
D	GPIO87	GPIO156	GPIO152	GPIO148	GPIO80	GPIO75	GPIO147	GPIO146	GPIO42	D
C	GPIO86	GPIO155	GPIO151	GPIO83	GPIO79	GPIO76	GPIO74	GPIO68	GPIO43	C
B	GPIO85	GPIO154	GPIO150	GPIO82	GPIO78	GPIO72	GPIO71	GPIO69	GPIO67	B
A	GPIO84	GPIO153	GPIO149	GPIO81	GPIO77	GPIO73	GPIO70	V_{DDIO}	V_{SS}	A
	11	12	13	14	15	16	17	18	19	

A. Only the GPIO function is shown on GPIO terminals. See Table 3-1 for the complete, muxed signal name.

Figure 3-3. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant C]

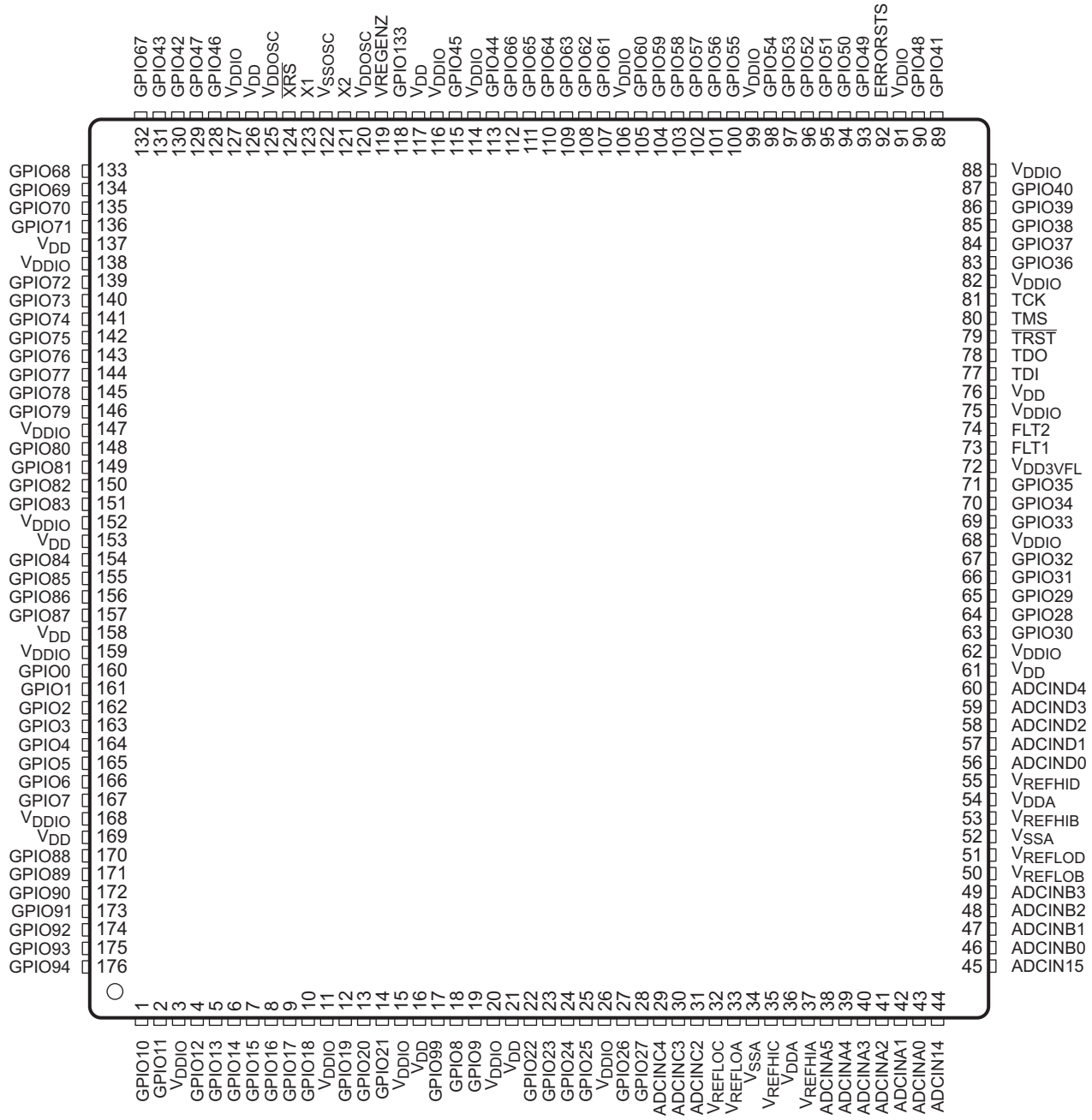


	1	2	3	4	5	6	7	8	9	10	
J	GPIO103	GPIO104	GPIO105	GPIO22	V_{SS}	V_{SS}		V_{SS}	V_{SS}	V_{SS}	J
H	GPIO100	GPIO101	GPIO102	NC	V_{DDIO}	V_{DDIO}		V_{SS}	V_{SS}	V_{SS}	H
G	GPIO99	GPIO8	GPIO9	V_{DDIO}	V_{DDIO}	V_{DDIO}					G
F	GPIO98	GPIO20	GPIO21	V_{DDIO}	V_{SS}	V_{SS}	V_{DDIO}	V_{SS}	V_{DD}	V_{DDIO}	F
E	GPIO16	GPIO17	GPIO18	GPIO19	V_{SS}	V_{SS}	V_{DDIO}	V_{SS}	V_{DD}	V_{DDIO}	E
D	GPIO13	GPIO14	GPIO15	GPIO168	GPIO166	GPIO89	GPIO5	GPIO1	GPIO162	GPIO159	D
C	GPIO11	GPIO12	GPIO96	GPIO167	GPIO165	GPIO88	GPIO4	GPIO0	GPIO161	GPIO158	C
B	V_{DDIO}	GPIO10	GPIO95	GPIO93	GPIO91	GPIO7	GPIO3	GPIO164	GPIO160	GPIO157	B
A	V_{SS}	GPIO97	GPIO94	GPIO92	GPIO90	GPIO6	GPIO2	GPIO163	V_{DDIO}	V_{SS}	A
	1	2	3	4	5	6	7	8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See Table 3-1 for the complete, muxed signal name.

Figure 3-4. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant D]

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A. Only the GPIO function is shown on GPIO pins. See Table 3-1 for the complete, muxed signal name.

Figure 3-5. 176-Pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack (Top View)

NOTE

The exposed lead frame die pad of the PowerPAD™ package serves two functions: to remove heat from the die and to provide ground path for the digital ground (analog ground is provided through dedicated pins). Thus, the PowerPAD should be soldered to the ground (GND) plane of the PCB because this will provide both the digital ground path and good thermal conduction path. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD. The thermal land should be soldered to the exposed lead frame die pad of the PowerPAD package; the thermal land should be as large as needed to dissipate the required heat. An array of thermal vias should be used to connect the thermal pad to the internal GND plane of the board. See *PowerPAD™ Thermally Enhanced Package* for more details on using the PowerPAD package.

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NOTE

PCB footprints and schematic symbols are available for download in a vendor-neutral format, which can be exported to the leading EDA CAD/CAE design tools. See the CAD/CAE Symbols section in the product folder for each device, under the Packaging section. These footprints and symbols can also be searched for at http://webench.ti.com/cad/.

3.2 Signal Descriptions

Table 3-1 describes the signals. The GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups are not enabled at reset.

Table 3-1. Signal Descriptions

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
ADC, DAC, AND COMPARATOR SIGNALS					
V_{REFHIA}		V1	37	I	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHIA} and V_{REFLOA} pins. **NOTE:** Do not load this pin externally.
V_{REFHIB}		W5	53	I	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHIB} and V_{REFLOB} pins. **NOTE:** Do not load this pin externally.
V_{REFHIC}		R1	35	I	ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHIC} and V_{REFLOC} pins. **NOTE:** Do not load this pin externally.
V_{REFHID}		V5	55	I	ADC-D high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHID} and V_{REFLOD} pins. **NOTE:** Do not load this pin externally.
V_{REFLOA}		R2	33	I	ADC-A low reference. On the PZP package, pin 17 is double-bonded to V_{SSA} and V_{REFLOA}. On the PZP package, pin 17 must be connected to V_{SSA} on the system board.
V_{REFLOB}		V6	50	I	ADC-B low reference
V_{REFLOC}		P2	32	I	ADC-C low reference
V_{REFLOD}		W6	51	I	ADC-D low reference
ADCIN14		T4	44	I	Input 14 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4P				I	Comparator 4 positive input
ADCIN15		U4	45	I	Input 15 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4N				I	Comparator 4 negative input

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
ADCINA0		U1	43	I	ADC-A input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTA				O	DAC-A output
ADCINA1		T1	42	I	ADC-A input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTB				O	DAC-B output
ADCINA2		U2	41	I	ADC-A input 2
CMPIN1P				I	Comparator 1 positive input
ADCINA3		T2	40	I	ADC-A input 3
CMPIN1N				I	Comparator 1 negative input
ADCINA4		U3	39	I	ADC-A input 4
CMPIN2P				I	Comparator 2 positive input
ADCINA5		T3	38	I	ADC-A input 5
CMPIN2N				I	Comparator 2 negative input
ADCINB0		V2	46	I	ADC-B input 0. There is a 100-pF capacitor to V_{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
VDAC				I	Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to V_{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
ADCINB1		W2	47	I	ADC-B input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTC				O	DAC-C output
ADCINB2		V3	48	I	ADC-B input 2
CMPIN3P				I	Comparator 3 positive input
ADCINB3		W3	49	I	ADC-B input 3
CMPIN3N				I	Comparator 3 negative input
ADCINB4		V4	–	I	ADC-B input 4
ADCINB5		W4	–	I	ADC-B input 5
ADCINC2		R3	31	I	ADC-C input 2
CMPIN6P				I	Comparator 6 positive input
ADCINC3		P3	30	I	ADC-C input 3
CMPIN6N				I	Comparator 6 negative input
ADCINC4		R4	29	I	ADC-C input 4
CMPIN5P				I	Comparator 5 positive input
ADCINC5		P4	–	I	ADC-C input 5
CMPIN5N				I	Comparator 5 negative input
ADCIND0		T5	56	I	ADC-D input 0
CMPIN7P				I	Comparator 7 positive input
ADCIND1		U5	57	I	ADC-D input 1
CMPIN7N				I	Comparator 7 negative input

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
ADCIND2		T6	58	I	ADC-D input 2
CMPIN8P				I	Comparator 8 positive input
ADCIND3		U6	59	I	ADC-D input 3
CMPIN8N				I	Comparator 8 negative input
ADCIND4		T7	60	I	ADC-D input 4
ADCIND5		U7	—	I	ADC-D input 5
GPIO AND PERIPHERAL SIGNALS					
GPIO0	0, 4, 8, 12	C8	160	I/O	General-purpose input/output 0
EPWM1A	1			O	Enhanced PWM1 output A (HRPWM-capable)
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
GPIO1	0, 4, 8, 12	D8	161	I/O	General-purpose input/output 1
EPWM1B	1			O	Enhanced PWM1 output B (HRPWM-capable)
MFSRB	3			I/O	McBSP-B receive frame synch
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
GPIO2	0, 4, 8, 12	A7	162	I/O	General-purpose input/output 2
EPWM2A	1			O	Enhanced PWM2 output A (HRPWM-capable)
OUTPUTXBAR1	5			O	Output 1 of the output XBAR
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO3	0, 4, 8, 12	B7	163	I/O	General-purpose input/output 3
EPWM2B	1			O	Enhanced PWM2 output B (HRPWM-capable)
OUTPUTXBAR2	2			O	Output 2 of the output XBAR
MCLKRB	3			I/O	McBSP-B receive clock
OUTPUTXBAR2	5			O	Output 2 of the output XBAR
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO4	0, 4, 8, 12	C7	164	I/O	General-purpose input/output 4
EPWM3A	1			O	Enhanced PWM3 output A (HRPWM-capable)
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
CANTXA	6			O	CAN-A transmit
GPIO5	0, 4, 8, 12	D7	165	I/O	General-purpose input/output 5
EPWM3B	1			O	Enhanced PWM3 output B (HRPWM-capable)
MFSRA	2			I/O	McBSP-A receive frame synch
OUTPUTXBAR3	3			O	Output 3 of the output XBAR
CANRXA	6			I	CAN-A receive
GPIO6	0, 4, 8, 12	A6	166	I/O	General-purpose input/output 6
EPWM4A	1			O	Enhanced PWM4 output A (HRPWM-capable)
OUTPUTXBAR4	2			O	Output 4 of the output XBAR
EXTSYNCOUT	3			O	External ePWM synch pulse output
EQEP3A	5			I	Enhanced QEP3 input A
CANTXB	6			O	CAN-B transmit
GPIO7	0, 4, 8, 12	B6	167	I/O	General-purpose input/output 7
EPWM4B	1			O	Enhanced PWM4 output B (HRPWM-capable)
MCLKRA	2			I/O	McBSP-A receive clock
OUTPUTXBAR5	3			O	Output 5 of the output XBAR
EQEP3B	5			I	Enhanced QEP3 input B
CANRXB	6			I	CAN-B receive

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO8	0, 4, 8, 12	G2	18	I/O	General-purpose input/output 8
EPWM5A	1			O	Enhanced PWM5 output A (HRPWM-capable)
CANTXB	2			O	CAN-B transmit
ADCSOCAO	3			O	ADC start-of-conversion A output for external ADC
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCITXDA	6			O	SCI-A transmit data
GPIO9	0, 4, 8, 12	G3	19	I/O	General-purpose input/output 9
EPWM5B	1			O	Enhanced PWM5 output B (HRPWM-capable)
SCITXDB	2			O	SCI-B transmit data
OUTPUTXBAR6	3			O	Output 6 of the output XBAR
EQEP3I	5			I/O	Enhanced QEP3 index
SCIRXDA	6			I	SCI-A receive data
GPIO10	0, 4, 8, 12	B2	1	I/O	General-purpose input/output 10
EPWM6A	1			O	Enhanced PWM6 output A (HRPWM-capable)
CANRXB	2			I	CAN-B receive
ADCSOCBO	3			O	ADC start-of-conversion B output for external ADC
EQEP1A	5			I	Enhanced QEP1 input A
SCITXDB	6			O	SCI-B transmit data
UPP-WAIT	15			I/O	Universal parallel port wait. Receiver asserts to request a pause in transfer.
GPIO11	0, 4, 8, 12	C1	2	I/O	General-purpose input/output 11
EPWM6B	1			O	Enhanced PWM6 output B (HRPWM-capable)
SCIRXDB	2, 6			I	SCI-B receive data
OUTPUTXBAR7	3			O	Output 7 of the output XBAR
EQEP1B	5			I	Enhanced QEP1 input B
UPP-START	15			I/O	Universal parallel port start. Transmitter asserts at start of DMA line.
GPIO12	0, 4, 8, 12	C2	4	I/O	General-purpose input/output 12
EPWM7A	1			O	Enhanced PWM7 output A (HRPWM-capable)
CANTXB	2			O	CAN-B transmit
MDXB	3			O	McBSP-B transmit serial data
EQEP1S	5			I/O	Enhanced QEP1 strobe
SCITXDC	6			O	SCI-C transmit data
UPP-ENA	15			I/O	Universal parallel port enable. Transmitter asserts while data bus is active.
GPIO13	0, 4, 8, 12	D1	5	I/O	General-purpose input/output 13
EPWM7B	1			O	Enhanced PWM7 output B (HRPWM-capable)
CANRXB	2			I	CAN-B receive
MDRB	3			I	McBSP-B receive serial data
EQEP1I	5			I/O	Enhanced QEP1 index
SCIRXDC	6			I	SCI-C receive data
UPP-D7	15			I/O	Universal parallel port data line 7

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO14	0, 4, 8, 12	D2	6	I/O	General-purpose input/output 14
EPWM8A	1			O	Enhanced PWM8 output A (HRPWM-capable)
SCITXDB	2			O	SCI-B transmit data
MCLKXB	3			I/O	McBSP-B transmit clock
OUTPUTXBAR3	6			O	Output 3 of the output XBAR
UPP-D6	15			I/O	Universal parallel port data line 6
GPIO15	0, 4, 8, 12	D3	7	I/O	General-purpose input/output 15
EPWM8B	1			O	Enhanced PWM8 output B (HRPWM-capable)
SCIRXDB	2			I	SCI-B receive data
MFSXB	3			I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	6			O	Output 4 of the output XBAR
UPP-D5	15			I/O	Universal parallel port data line 5
GPIO16	0, 4, 8, 12	E1	8	I/O	General-purpose input/output 16
SPISIMOA	1			I/O	SPI-A slave in, master out
CANTXB	2			O	CAN-B transmit
OUTPUTXBAR7	3			O	Output 7 of the output XBAR
EPWM9A	5			O	Enhanced PWM9 output A
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
UPP-D4	15			I/O	Universal parallel port data line 4
GPIO17	0, 4, 8, 12	E2	9	I/O	General-purpose input/output 17
SPISOMIA	1			I/O	SPI-A slave out, master in
CANRXB	2			I	CAN-B receive
OUTPUTXBAR8	3			O	Output 8 of the output XBAR
EPWM9B	5			O	Enhanced PWM9 output B
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
UPP-D3	15			I/O	Universal parallel port data line 3
GPIO18	0, 4, 8, 12	E3	10	I/O	General-purpose input/output 18
SPICLKA	1			I/O	SPI-A clock
SCITXDB	2			O	SCI-B transmit data
CANRXA	3			I	CAN-A receive
EPWM10A	5			O	Enhanced PWM10 output A
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
UPP-D2	15			I/O	Universal parallel port data line 2
GPIO19	0, 4, 8, 12	E4	12	I/O	General-purpose input/output 19
$\overline{\text{SPISTEA}}$	1			I/O	SPI-A slave transmit enable
SCIRXDB	2			I	SCI-B receive data
CANTXA	3			O	CAN-A transmit
EPWM10B	5			O	Enhanced PWM10 output B
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
UPP-D1	15			I/O	Universal parallel port data line 1

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO20	0, 4, 8, 12			I/O	General-purpose input/output 20
EQEP1A	1			I	Enhanced QEP1 input A
MDXA	2			O	McBSP-A transmit serial data
CANTXB	3	F2	13	O	CAN-B transmit
EPWM11A	5			O	Enhanced PWM11 output A
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
UPP-D0	15			I/O	Universal parallel port data line 0
GPIO21	0, 4, 8, 12			I/O	General-purpose input/output 21
EQEP1B	1			I	Enhanced QEP1 input B
MDRA	2			I	McBSP-A receive serial data
CANRXB	3	F3	14	I	CAN-B receive
EPWM11B	5			O	Enhanced PWM11 output B
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input
UPP-CLK	15			I/O	Universal parallel port transmit clock
GPIO22	0, 4, 8, 12			I/O	General-purpose input/output 22
EQEP1S	1			I/O	Enhanced QEP1 strobe
MCLKXA	2			I/O	McBSP-A transmit clock
SCITXDB	3	J4	22	O	SCI-B transmit data
EPWM12A	5			O	Enhanced PWM12 output A
SPICLKB	6			I/O	SPI-B clock
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO23	0, 4, 8, 12			I/O	General-purpose input/output 23
EQEP1I	1			I/O	Enhanced QEP1 index
MFSXA	2			I/O	McBSP-A transmit frame synch
SCIRXDB	3	K4	23	I	SCI-B receive data
EPWM12B	5			O	Enhanced PWM12 output B
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO24	0, 4, 8, 12			I/O	General-purpose input/output 24
OUTPUTXBAR1	1			O	Output 1 of the output XBAR
EQEP2A	2	K3	24	I	Enhanced QEP2 input A
MDXB	3			O	McBSP-B transmit serial data
SPISIMOB	6			I/O	SPI-B slave in, master out
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO25	0, 4, 8, 12			I/O	General-purpose input/output 25
OUTPUTXBAR2	1			O	Output 2 of the output XBAR
EQEP2B	2	K2	25	I	Enhanced QEP2 input B
MDRB	3			I	McBSP-B receive serial data
SPISOMIB	6			I/O	SPI-B slave out, master in
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO26	0, 4, 8, 12	K1	27	I/O	General-purpose input/output 26
OUTPUTXBAR3	1			O	Output 3 of the output XBAR
EQEP2I	2			I/O	Enhanced QEP2 index
MCLKXB	3			I/O	McBSP-B transmit clock
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
SPICLKB	6			I/O	SPI-B clock
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
GPIO27	0, 4, 8, 12	L1	28	I/O	General-purpose input/output 27
OUTPUTXBAR4	1			O	Output 4 of the output XBAR
EQEP2S	2			I/O	Enhanced QEP2 strobe
MFSXB	3			I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	5			O	Output 4 of the output XBAR
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
GPIO28	0, 4, 8, 12	V11	64	I/O	General-purpose input/output 28
SCIRXDA	1			I	SCI-A receive data
$\overline{\text{EM1CS4}}$	2			O	External memory interface 1 chip select 4
OUTPUTXBAR5	5			O	Output 5 of the output XBAR
EQEP3A	6			I	Enhanced QEP3 input A
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
GPIO29	0, 4, 8, 12	W11	65	I/O	General-purpose input/output 29
SCITXDA	1			O	SCI-A transmit data
EM1SDCKE	2			O	External memory interface 1 SDRAM clock enable
OUTPUTXBAR6	5			O	Output 6 of the output XBAR
EQEP3B	6			I	Enhanced QEP3 input B
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
GPIO30	0, 4, 8, 12	T11	63	I/O	General-purpose input/output 30
CANRXA	1			I	CAN-A receive
EM1CLK	2			O	External memory interface 1 clock
OUTPUTXBAR7	5			O	Output 7 of the output XBAR
EQEP3S	6			I/O	Enhanced QEP3 strobe
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO31	0, 4, 8, 12	U11	66	I/O	General-purpose input/output 31
CANTXA	1			O	CAN-A transmit
$\overline{\text{EM1WE}}$	2			O	External memory interface 1 write enable
OUTPUTXBAR8	5			O	Output 8 of the output XBAR
EQEP3I	6			I/O	Enhanced QEP3 index
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
GPIO32	0, 4, 8, 12	U13	67	I/O	General-purpose input/output 32
SDAA	1			I/OD	I2C-A data open-drain bidirectional port
$\overline{\text{EM1CS0}}$	2			O	External memory interface 1 chip select 0
GPIO33	0, 4, 8, 12	T13	69	I/O	General-purpose input/output 33
SCLA	1			I/OD	I2C-A clock open-drain bidirectional port
EM1RNW	2			O	External memory interface 1 read not write

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO34	0, 4, 8, 12	U14	70	I/O	General-purpose input/output 34
OUTPUTXBAR1	1			O	Output 1 of the output XBAR
$\overline{\text{EM1CS2}}$	2			O	External memory interface 1 chip select 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO35	0, 4, 8, 12	T14	71	I/O	General-purpose input/output 35
SCIRXDA	1			I	SCI-A receive data
$\overline{\text{EM1CS3}}$	2			O	External memory interface 1 chip select 3
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO36	0, 4, 8, 12	V16	83	I/O	General-purpose input/output 36
SCITXDA	1			O	SCI-A transmit data
EM1WAIT	2			I	External memory interface 1 Asynchronous SRAM WAIT
CANRXA	6			I	CAN-A receive
GPIO37	0, 4, 8, 12	U16	84	I/O	General-purpose input/output 37
OUTPUTXBAR2	1			O	Output 2 of the output XBAR
$\overline{\text{EM1OE}}$	2			O	External memory interface 1 output enable
CANTXA	6			O	CAN-A transmit
GPIO38	0, 4, 8, 12	T16	85	I/O	General-purpose input/output 38
EM1A0	2			O	External memory interface 1 address line 0
SCITXDC	5			O	SCI-C transmit data
CANTXB	6			O	CAN-B transmit
GPIO39	0, 4, 8, 12	W17	86	I/O	General-purpose input/output 39
EM1A1	2			O	External memory interface 1 address line 1
SCIRXDC	5			I	SCI-C receive data
CANRXB	6			I	CAN-B receive
GPIO40	0, 4, 8, 12	V17	87	I/O	General-purpose input/output 40
EM1A2	2			O	External memory interface 1 address line 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO41	0, 4, 8, 12	U17	89	I/O	General-purpose input/output 41. For applications using the Hibernate low-power mode, this pin serves as the $\overline{\text{GPIOHIBWAKE}}$ signal. For details, see the Low Power Modes section of the System Control chapter in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.
EM1A3	2			O	External memory interface 1 address line 3
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO42	0, 4, 8, 12	D19	130	I/O	General-purpose input/output 42
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
SCITXDA	15			O	SCI-A transmit data
USB0DM	Analog			I/O	USB PHY differential data
GPIO43	0, 4, 8, 12	C19	131	I/O	General-purpose input/output 43
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
SCIRXDA	15			I	SCI-A receive data
USB0DP	Analog			I/O	USB PHY differential data
GPIO44	0, 4, 8, 12	K18	113	I/O	General-purpose input/output 44
EM1A4	2			O	External memory interface 1 address line 4

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO45	0, 4, 8, 12	K19	115	I/O	General-purpose input/output 45
EM1A5	2			O	External memory interface 1 address line 5
GPIO46	0, 4, 8, 12	E19	128	I/O	General-purpose input/output 46
EM1A6	2			O	External memory interface 1 address line 6
SCIRXDD	6			I	SCI-D receive data
GPIO47	0, 4, 8, 12	E18	129	I/O	General-purpose input/output 47
EM1A7	2			O	External memory interface 1 address line 7
SCITXDD	6			O	SCI-D transmit data
GPIO48	0, 4, 8, 12	R16	90	I/O	General-purpose input/output 48
OUTPUTXBAR3	1			O	Output 3 of the output XBAR
EM1A8	2			O	External memory interface 1 address line 8
SCITXDA	6			O	SCI-A transmit data
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
GPIO49	0, 4, 8, 12	R17	93	I/O	General-purpose input/output 49
OUTPUTXBAR4	1			O	Output 4 of the output XBAR
EM1A9	2			O	External memory interface 1 address line 9
SCIRXDA	6			I	SCI-A receive data
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
GPIO50	0, 4, 8, 12	R18	94	I/O	General-purpose input/output 50
EQEP1A	1			I	Enhanced QEP1 input A
EM1A10	2			O	External memory interface 1 address line 10
SPISIMOC	6			I/O	SPI-C slave in, master out
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO51	0, 4, 8, 12	R19	95	I/O	General-purpose input/output 51
EQEP1B	1			I	Enhanced QEP1 input B
EM1A11	2			O	External memory interface 1 address line 11
SPISOMIC	6			I/O	SPI-C slave out, master in
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
GPIO52	0, 4, 8, 12	P16	96	I/O	General-purpose input/output 52
EQEP1S	1			I/O	Enhanced QEP1 strobe
EM1A12	2			O	External memory interface 1 address line 12
SPICLKC	6			I/O	SPI-C clock
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO53	0, 4, 8, 12	P17	97	I/O	General-purpose input/output 53
EQEP1I	1			I/O	Enhanced QEP1 index
EM1D31	2			I/O	External memory interface 1 data line 31
EM2D15	3			I/O	External memory interface 2 data line 15
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO54	0, 4, 8, 12			I/O	General-purpose input/output 54
SPISIMOA	1			I/O	SPI-A slave in, master out
EM1D30	2			I/O	External memory interface 1 data line 30
EM2D14	3	P18	98	I/O	External memory interface 2 data line 14
EQEP2A	5			I	Enhanced QEP2 input A
SCITXDB	6			O	SCI-B transmit data
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO55	0, 4, 8, 12			I/O	General-purpose input/output 55
SPISOMIA	1			I/O	SPI-A slave out, master in
EM1D29	2			I/O	External memory interface 1 data line 29
EM2D13	3	P19	100	I/O	External memory interface 2 data line 13
EQEP2B	5			I	Enhanced QEP2 input B
SCIRXDB	6			I	SCI-B receive data
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO56	0, 4, 8, 12			I/O	General-purpose input/output 56
SPICLKA	1			I/O	SPI-A clock
EM1D28	2			I/O	External memory interface 1 data line 28
EM2D12	3	N16	101	I/O	External memory interface 2 data line 12
EQEP2S	5			I/O	Enhanced QEP2 strobe
SCITXDC	6			O	SCI-C transmit data
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO57	0, 4, 8, 12			I/O	General-purpose input/output 57
$\overline{\text{SPISTEA}}$	1			I/O	SPI-A slave transmit enable
EM1D27	2			I/O	External memory interface 1 data line 27
EM2D11	3	N18	102	I/O	External memory interface 2 data line 11
EQEP2I	5			I/O	Enhanced QEP2 index
SCIRXDC	6			I	SCI-C receive data
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO58	0, 4, 8, 12			I/O	General-purpose input/output 58
MCLKRA	1			I/O	McBSP-A receive clock
EM1D26	2			I/O	External memory interface 1 data line 26
EM2D10	3	N17	103	I/O	External memory interface 2 data line 10
OUTPUTXBAR1	5			O	Output 1 of the output XBAR
SPICLKB	6			I/O	SPI-B clock
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
SPISIMOA	15			I/O	SPI-A slave in, master out[2]
GPIO59	0, 4, 8, 12			I/O	General-purpose input/output 59[3]
MFSRA	1			I/O	McBSP-A receive frame synch
EM1D25	2			I/O	External memory interface 1 data line 25
EM2D9	3	M16	104	I/O	External memory interface 2 data line 9
OUTPUTXBAR2	5			O	Output 2 of the output XBAR
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
SPISOMIA	15			I/O	SPI-A slave out, master in[2]

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO60	0, 4, 8, 12	M17	105	I/O	General-purpose input/output 60
MCLKRB	1			I/O	McBSP-B receive clock
EM1D24	2			I/O	External memory interface 1 data line 24
EM2D8	3			I/O	External memory interface 2 data line 8
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
SPISIMOB	6			I/O	SPI-B slave in, master out
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
SPICLKA	15			I/O	SPI-A clock[2]
GPIO61	0, 4, 8, 12	L16	107	I/O	General-purpose input/output 61[3]
MFSRB	1			I/O	McBSP-B receive frame synch
EM1D23	2			I/O	External memory interface 1 data line 23
EM2D7	3			I/O	External memory interface 2 data line 7
OUTPUTXBAR4	5			O	Output 4 of the output XBAR
SPISOMIB	6			I/O	SPI-B slave out, master in
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
$\overline{\text{SPISTEA}}$	15			I/O	SPI-A slave transmit enable[2]
GPIO62	0, 4, 8, 12	J17	108	I/O	General-purpose input/output 62
SCIRXDC	1			I	SCI-C receive data
EM1D22	2			I/O	External memory interface 1 data line 22
EM2D6	3			I/O	External memory interface 2 data line 6
EQEP3A	5			I	Enhanced QEP3 input A
CANRXA	6			I	CAN-A receive
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO63	0, 4, 8, 12	J16	109	I/O	General-purpose input/output 63
SCITXDC	1			O	SCI-C transmit data
EM1D21	2			I/O	External memory interface 1 data line 21
EM2D5	3			I/O	External memory interface 2 data line 5
EQEP3B	5			I	Enhanced QEP3 input B
CANTXA	6			O	CAN-A transmit
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
SPISIMOB	15			I/O	SPI-B slave in, master out[2]
GPIO64	0, 4, 8, 12	L17	110	I/O	General-purpose input/output 64[3]
EM1D20	2			I/O	External memory interface 1 data line 20
EM2D4	3			I/O	External memory interface 2 data line 4
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCIRXDA	6			I	SCI-A receive data
SPISOMIB	15			I/O	SPI-B slave out, master in[2]
GPIO65	0, 4, 8, 12	K16	111	I/O	General-purpose input/output 65
EM1D19	2			I/O	External memory interface 1 data line 19
EM2D3	3			I/O	External memory interface 2 data line 3
EQEP3I	5			I/O	Enhanced QEP3 index
SCITXDA	6			O	SCI-A transmit data
SPICLKB	15			I/O	SPI-B clock[2]

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO66	0, 4, 8, 12	K17	112	I/O	General-purpose input/output 66[3]
EM1D18	2			I/O	External memory interface 1 data line 18
EM2D2	3			I/O	External memory interface 2 data line 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
$\overline{\text{SPISTEB}}$	15			I/O	SPI-B slave transmit enable[2]
GPIO67	0, 4, 8, 12	B19	132	I/O	General-purpose input/output 67
EM1D17	2			I/O	External memory interface 1 data line 17
EM2D1	3			I/O	External memory interface 2 data line 1
GPIO68	0, 4, 8, 12	C18	133	I/O	General-purpose input/output 68
EM1D16	2			I/O	External memory interface 1 data line 16
EM2D0	3			I/O	External memory interface 2 data line 0
GPIO69	0, 4, 8, 12	B18	134	I/O	General-purpose input/output 69
EM1D15	2			I/O	External memory interface 1 data line 15
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
SPISIMOC	15			I/O	SPI-C slave in, master out[2]
GPIO70	0, 4, 8, 12	A17	135	I/O	General-purpose input/output 70[3]
EM1D14	2			I/O	External memory interface 1 data line 14
CANRXA	5			I	CAN-A receive
SCITXDB	6			O	SCI-B transmit data
SPISOMIC	15			I/O	SPI-C slave out, master in[2]
GPIO71	0, 4, 8, 12	B17	136	I/O	General-purpose input/output 71
EM1D13	2			I/O	External memory interface 1 data line 13
CANTXA	5			O	CAN-A transmit
SCIRXDB	6			I	SCI-B receive data
SPICLKC	15			I/O	SPI-C clock[2]
GPIO72	0, 4, 8, 12	B16	139	I/O	General-purpose input/output 72.[3] This is the factory default boot mode select pin 1.
EM1D12	2			I/O	External memory interface 1 data line 12
CANTXB	5			O	CAN-B transmit
SCITXDC	6			O	SCI-C transmit data
$\overline{\text{SPISTEC}}$	15			I/O	SPI-C slave transmit enable[2]
GPIO73	0, 4, 8, 12	A16	140	I/O	General-purpose input/output 73
EM1D11	2			I/O	External memory interface 1 data line 11
XCLKOUT	3			O/Z	External clock output. This pin outputs a divided-down version of a chosen clock signal from within the device. The clock signal is chosen using the CLKSRCCTL3.XCLKOUTSEL bit field while the divide ratio is chosen using the XCLKOUTDIVSEL.XCLKOUTDIV bit field.
CANRXB	5			I	CAN-B receive
SCIRXDC	6			I	SCI-C receive
GPIO74	0, 4, 8, 12	C17	141	I/O	General-purpose input/output 74
EM1D10	2			I/O	External memory interface 1 data line 10
GPIO75	0, 4, 8, 12	D16	142	I/O	General-purpose input/output 75
EM1D9	2			I/O	External memory interface 1 data line 9

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO76	0, 4, 8, 12	C16	143	I/O	General-purpose input/output 76
EM1D8	2			I/O	External memory interface 1 data line 8
SCITXDD	6			O	SCI-D transmit data
GPIO77	0, 4, 8, 12	A15	144	I/O	General-purpose input/output 77
EM1D7	2			I/O	External memory interface 1 data line 7
SCIRXDD	6			I	SCI-D receive data
GPIO78	0, 4, 8, 12	B15	145	I/O	General-purpose input/output 78
EM1D6	2			I/O	External memory interface 1 data line 6
EQEP2A	6			I	Enhanced QEP2 input A
GPIO79	0, 4, 8, 12	C15	146	I/O	General-purpose input/output 79
EM1D5	2			I/O	External memory interface 1 data line 5
EQEP2B	6			I	Enhanced QEP2 input B
GPIO80	0, 4, 8, 12	D15	148	I/O	General-purpose input/output 80
EM1D4	2			I/O	External memory interface 1 data line 4
EQEP2S	6			I/O	Enhanced QEP2 strobe
GPIO81	0, 4, 8, 12	A14	149	I/O	General-purpose input/output 81
EM1D3	2			I/O	External memory interface 1 data line 3
EQEP2I	6			I/O	Enhanced QEP2 index
GPIO82	0, 4, 8, 12	B14	150	I/O	General-purpose input/output 82
EM1D2	2			I/O	External memory interface 1 data line 2
GPIO83	0, 4, 8, 12	C14	151	I/O	General-purpose input/output 83
EM1D1	2			I/O	External memory interface 1 data line 1
GPIO84	0, 4, 8, 12	A11	154	I/O	General-purpose input/output 84. This is the factory default boot mode select pin 0.
SCITXDA	5			O	SCI-A transmit data
MDXB	6			O	McBSP-B transmit serial data
MDXA	15			O	McBSP-A transmit serial data
GPIO85	0, 4, 8, 12	B11	155	I/O	General-purpose input/output 85
EM1D0	2			I/O	External memory interface 1 data line 0
SCIRXDA	5			I	SCI-A receive data
MDRB	6			I	McBSP-B receive serial data
MDRA	15			I	McBSP-A receive serial data
GPIO86	0, 4, 8, 12	C11	156	I/O	General-purpose input/output 86
EM1A13	2			O	External memory interface 1 address line 13
EM1CAS	3			O	External memory interface 1 column address strobe
SCITXDB	5			O	SCI-B transmit data
MCLKXB	6			I/O	McBSP-B transmit clock
MCLKXA	15			I/O	McBSP-A transmit clock
GPIO87	0, 4, 8, 12	D11	157	I/O	General-purpose input/output 87
EM1A14	2			O	External memory interface 1 address line 14
EM1RAS	3			O	External memory interface 1 row address strobe
SCIRXDB	5			I	SCI-B receive data
MFSXB	6			I/O	McBSP-B transmit frame synch
MFSXA	15			I/O	McBSP-A transmit frame synch

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO88	0, 4, 8, 12	C6	170	I/O	General-purpose input/output 88
EM1A15	2			O	External memory interface 1 address line 15
EM1DQM0	3			O	External memory interface 1 Input/output mask for byte 0
GPIO89	0, 4, 8, 12	D6	171	I/O	General-purpose input/output 89
EM1A16	2			O	External memory interface 1 address line 16
EM1DQM1	3			O	External memory interface 1 Input/output mask for byte 1
SCITXDC	6			O	SCI-C transmit data
GPIO90	0, 4, 8, 12	A5	172	I/O	General-purpose input/output 90
EM1A17	2			O	External memory interface 1 address line 17
EM1DQM2	3			O	External memory interface 1 Input/output mask for byte 2
SCIRXDC	6			I	SCI-C receive data
GPIO91	0, 4, 8, 12	B5	173	I/O	General-purpose input/output 91
EM1A18	2			O	External memory interface 1 address line 18
EM1DQM3	3			O	External memory interface 1 Input/output mask for byte 3
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
GPIO92	0, 4, 8, 12	A4	174	I/O	General-purpose input/output 92
EM1A19	2			O	External memory interface 1 address line 19
EM1BA1	3			O	External memory interface 1 bank address 1
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
GPIO93	0, 4, 8, 12	B4	175	I/O	General-purpose input/output 93
EM1BA0	3			O	External memory interface 1 bank address 0
SCITXDD	6			O	SCI-D transmit data
GPIO94	0, 4, 8, 12	A3	176	I/O	General-purpose input/output 94
SCIRXDD	6			I	SCI-D receive data
GPIO95	0, 4, 8, 12	B3	—	I/O	General-purpose input/output 95
GPIO96	0, 4, 8, 12	C3	—	I/O	General-purpose input/output 96
EM2DQM1	3			O	External memory interface 2 Input/output mask for byte 1
EQEP1A	5			I	Enhanced QEP1 input A
GPIO97	0, 4, 8, 12	A2	—	I/O	General-purpose input/output 97
EM2DQM0	3			O	External memory interface 2 Input/output mask for byte 0
EQEP1B	5			I	Enhanced QEP1 input B
GPIO98	0, 4, 8, 12	F1	—	I/O	General-purpose input/output 98
EM2A0	3			O	External memory interface 2 address line 0
EQEP1S	5			I/O	Enhanced QEP1 strobe
GPIO99	0, 4, 8, 12	G1	17	I/O	General-purpose input/output 99
EM2A1	3			O	External memory interface 2 address line 1
EQEP1I	5			I/O	Enhanced QEP1 index
GPIO100	0, 4, 8, 12	H1	—	I/O	General-purpose input/output 100
EM2A2	3			O	External memory interface 2 address line 2
EQEP2A	5			I	Enhanced QEP2 input A
SPISIMOC	6			I/O	SPI-C slave in, master out
GPIO101	0, 4, 8, 12	H2	—	I/O	General-purpose input/output 101
EM2A3	3			O	External memory interface 2 address line 3
EQEP2B	5			I	Enhanced QEP2 input B
SPISOMIC	6			I/O	SPI-C slave out, master in

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO102	0, 4, 8, 12	H3	—	I/O	General-purpose input/output 102
EM2A4	3			O	External memory interface 2 address line 4
EQEP2S	5			I/O	Enhanced QEP2 strobe
SPICLKC	6			I/O	SPI-C clock
GPIO103	0, 4, 8, 12	J1	—	I/O	General-purpose input/output 103
EM2A5	3			O	External memory interface 2 address line 5
EQEP2I	5			I/O	Enhanced QEP2 index
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
GPIO104	0, 4, 8, 12	J2	—	I/O	General-purpose input/output 104
SDAA	1			I/OD	I2C-A data open-drain bidirectional port
EM2A6	3			O	External memory interface 2 address line 6
EQEP3A	5			I	Enhanced QEP3 input A
SCITXDD	6			O	SCI-D transmit data
GPIO105	0, 4, 8, 12	J3	—	I/O	General-purpose input/output 105
SCLA	1			I/OD	I2C-A clock open-drain bidirectional port
EM2A7	3			O	External memory interface 2 address line 7
EQEP3B	5			I	Enhanced QEP3 input B
SCIRXDD	6			I	SCI-D receive data
GPIO106	0, 4, 8, 12	L2	—	I/O	General-purpose input/output 106
EM2A8	3			O	External memory interface 2 address line 8
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCITXDC	6			O	SCI-C transmit data
GPIO107	0, 4, 8, 12	L3	—	I/O	General-purpose input/output 107
EM2A9	3			O	External memory interface 2 address line 9
EQEP3I	5			I/O	Enhanced QEP3 index
SCIRXDC	6			I	SCI-C receive data
GPIO108	0, 4, 8, 12	L4	—	I/O	General-purpose input/output 108
EM2A10	3			O	External memory interface 2 address line 10
GPIO109	0, 4, 8, 12	N2	—	I/O	General-purpose input/output 109
EM2A11	3			O	External memory interface 2 address line 11
GPIO110	0, 4, 8, 12	M2	—	I/O	General-purpose input/output 110
EM2WAIT	3			I	External memory interface 2 Asynchronous SRAM WAIT
GPIO111	0, 4, 8, 12	M4	—	I/O	General-purpose input/output 111
EM2BA0	3			O	External memory interface 2 bank address 0
GPIO112	0, 4, 8, 12	M3	—	I/O	General-purpose input/output 112
EM2BA1	3			O	External memory interface 2 bank address 1
GPIO113	0, 4, 8, 12	N4	—	I/O	General-purpose input/output 113
EM2CAS	3			O	External memory interface 2 column address strobe
GPIO114	0, 4, 8, 12	N3	—	I/O	General-purpose input/output 114
EM2RAS	3			O	External memory interface 2 row address strobe
GPIO115	0, 4, 8, 12	V12	—	I/O	General-purpose input/output 115
$\overline{\text{EM2CS0}}$	3			O	External memory interface 2 chip select 0
GPIO116	0, 4, 8, 12	W10	—	I/O	General-purpose input/output 116
$\overline{\text{EM2CS2}}$	3			O	External memory interface 2 chip select 2

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO117	0, 4, 8, 12	U12	—	I/O	General-purpose input/output 117
EM2SDCKE	3			O	External memory interface 2 SDRAM clock enable
GPIO118	0, 4, 8, 12	T12	—	I/O	General-purpose input/output 118
EM2CLK	3			O	External memory interface 2 clock
GPIO119	0, 4, 8, 12	T15	—	I/O	General-purpose input/output 119
EM2RNW	3			O	External memory interface 2 read not write
GPIO120	0, 4, 8, 12	U15	—	I/O	General-purpose input/output 120
$\overline{\text{EM2WE}}$	3			O	External memory interface 2 write enable
USB0PFLT	15			I/O	USB external regulator power fault indicator
GPIO121	0, 4, 8, 12	W16	—	I/O	General-purpose input/output 121
$\overline{\text{EM2OE}}$	3			O	External memory interface 2 output enable
USB0EPEN	15			I/O	USB external regulator enable
GPIO122	0, 4, 8, 12	T8	—	I/O	General-purpose input/output 122
SPISIMOC	6			I/O	SPI-C slave in, master out
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
GPIO123	0, 4, 8, 12	U8	—	I/O	General-purpose input/output 123
SPISOMIC	6			I/O	SPI-C slave out, master in
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
GPIO124	0, 4, 8, 12	V8	—	I/O	General-purpose input/output 124
SPICLKC	6			I/O	SPI-C clock
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO125	0, 4, 8, 12	T9	—	I/O	General-purpose input/output 125
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
GPIO126	0, 4, 8, 12	U9	—	I/O	General-purpose input/output 126
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO127	0, 4, 8, 12	V9	—	I/O	General-purpose input/output 127
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input
GPIO128	0, 4, 8, 12	W9	—	I/O	General-purpose input/output 128
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO129	0, 4, 8, 12	T10	—	I/O	General-purpose input/output 129
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO130	0, 4, 8, 12	U10	—	I/O	General-purpose input/output 130
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO131	0, 4, 8, 12	V10	—	I/O	General-purpose input/output 131
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO132	0, 4, 8, 12	W18	—	I/O	General-purpose input/output 132
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
GPIO133/AUXCLKIN	0, 4, 8, 12	G18	118	I/O	General-purpose input/output 133. The AUXCLKIN function of this GPIO pin could be used to provide a single-ended 3.3-V level clock signal to the Auxiliary Phase-Locked Loop (AUXPLL), whose output is used for the USB module. The AUXCLKIN clock may also be used for the CAN module.
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO134	0, 4, 8, 12	V18	—	I/O	General-purpose input/output 134
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
GPIO135	0, 4, 8, 12	U18	—	I/O	General-purpose input/output 135
SCITXDA	6			O	SCI-A transmit data
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
GPIO136	0, 4, 8, 12	T17	—	I/O	General-purpose input/output 136
SCIRXDA	6			I	SCI-A receive data
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO137	0, 4, 8, 12	T18	—	I/O	General-purpose input/output 137
SCITXDB	6			O	SCI-B transmit data
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
GPIO138	0, 4, 8, 12	T19	—	I/O	General-purpose input/output 138
SCIRXDB	6			I	SCI-B receive data
GPIO139	0, 4, 8, 12	N19	—	I/O	General-purpose input/output 139
SCIRXDC	6			I	SCI-C receive data
GPIO140	0, 4, 8, 12	M19	—	I/O	General-purpose input/output 140
SCITXDC	6			O	SCI-C transmit data
GPIO141	0, 4, 8, 12	M18	—	I/O	General-purpose input/output 141
SCIRXDD	6			I	SCI-D receive data
GPIO142	0, 4, 8, 12	L19	—	I/O	General-purpose input/output 142
SCITXDD	6			O	SCI-D transmit data
GPIO143	0, 4, 8, 12	F18	—	I/O	General-purpose input/output 143
GPIO144	0, 4, 8, 12	F17	—	I/O	General-purpose input/output 144
GPIO145	0, 4, 8, 12	E17	—	I/O	General-purpose input/output 145
EPWM1A	1			O	Enhanced PWM1 output A (HRPWM-capable)
GPIO146	0, 4, 8, 12	D18	—	I/O	General-purpose input/output 146
EPWM1B	1			O	Enhanced PWM1 output B (HRPWM-capable)
GPIO147	0, 4, 8, 12	D17	—	I/O	General-purpose input/output 147
EPWM2A	1			O	Enhanced PWM2 output A (HRPWM-capable)
GPIO148	0, 4, 8, 12	D14	—	I/O	General-purpose input/output 148
EPWM2B	1			O	Enhanced PWM2 output B (HRPWM-capable)
GPIO149	0, 4, 8, 12	A13	—	I/O	General-purpose input/output 149
EPWM3A	1			O	Enhanced PWM3 output A (HRPWM-capable)
GPIO150	0, 4, 8, 12	B13	—	I/O	General-purpose input/output 150
EPWM3B	1			O	Enhanced PWM3 output B (HRPWM-capable)
GPIO151	0, 4, 8, 12	C13	—	I/O	General-purpose input/output 151
EPWM4A	1			O	Enhanced PWM4 output A (HRPWM-capable)
GPIO152	0, 4, 8, 12	D13	—	I/O	General-purpose input/output 152
EPWM4B	1			O	Enhanced PWM4 output B (HRPWM-capable)
GPIO153	0, 4, 8, 12	A12	—	I/O	General-purpose input/output 153
EPWM5A	1			O	Enhanced PWM5 output A (HRPWM-capable)
GPIO154	0, 4, 8, 12	B12	—	I/O	General-purpose input/output 154
EPWM5B	1			O	Enhanced PWM5 output B (HRPWM-capable)
GPIO155	0, 4, 8, 12	C12	—	I/O	General-purpose input/output 155
EPWM6A	1			O	Enhanced PWM6 output A (HRPWM-capable)

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO156	0, 4, 8, 12	D12	—	I/O	General-purpose input/output 156
EPWM6B	1			O	Enhanced PWM6 output B (HRPWM-capable)
GPIO157	0, 4, 8, 12	B10	—	I/O	General-purpose input/output 157
EPWM7A	1			O	Enhanced PWM7 output A (HRPWM-capable)
GPIO158	0, 4, 8, 12	C10	—	I/O	General-purpose input/output 158
EPWM7B	1			O	Enhanced PWM7 output B (HRPWM-capable)
GPIO159	0, 4, 8, 12	D10	—	I/O	General-purpose input/output 159
EPWM8A	1			O	Enhanced PWM8 output A (HRPWM-capable)
GPIO160	0, 4, 8, 12	B9	—	I/O	General-purpose input/output 160
EPWM8B	1			O	Enhanced PWM8 output B (HRPWM-capable)
GPIO161	0, 4, 8, 12	C9	—	I/O	General-purpose input/output 161
EPWM9A	1			O	Enhanced PWM9 output A
GPIO162	0, 4, 8, 12	D9	—	I/O	General-purpose input/output 162
EPWM9B	1			O	Enhanced PWM9 output B
GPIO163	0, 4, 8, 12	A8	—	I/O	General-purpose input/output 163
EPWM10A	1			O	Enhanced PWM10 output A
GPIO164	0, 4, 8, 12	B8	—	I/O	General-purpose input/output 164
EPWM10B	1			O	Enhanced PWM10 output B
GPIO165	0, 4, 8, 12	C5	—	I/O	General-purpose input/output 165
EPWM11A	1			O	Enhanced PWM11 output A
GPIO166	0, 4, 8, 12	D5	—	I/O	General-purpose input/output 166
EPWM11B	1			O	Enhanced PWM11 output B
GPIO167	0, 4, 8, 12	C4	—	I/O	General-purpose input/output 167
EPWM12A	1			O	Enhanced PWM12 output A
GPIO168	0, 4, 8, 12	D4	—	I/O	General-purpose input/output 168
EPWM12B	1			O	Enhanced PWM12 output B
RESET					
$\overline{\text{XRS}}$		F19	124	I/OD	Device Reset (in) and Watchdog Reset (out). The devices have a built-in power-on reset (POR) circuit. During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset or NMI watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. If a capacitor is placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open drain with an internal pullup. If this pin is driven by an external device, an open-drain device is recommended.

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
CLOCKS					
X1		G19	123	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal must be connected across X1 and X2. If this pin is not used, it must be tied to GND. This pin can also be used to feed a single-ended 3.3-V level clock. In this case, X2 is a No Connect (NC).
X2		J19	121	O	On-chip crystal-oscillator output. A quartz crystal may be connected across X1 and X2. If X2 is not used, it must be left unconnected.
NO CONNECT					
NC		H4	—		No connect. BGA ball is electrically open and not connected to the die.
JTAG					
TCK		V15	81	I	JTAG test clock with internal pullup (see Section 4.5)
TDI		W13	77	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO		W15	78	O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.[3]
TMS		W14	80	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$		V14	79	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ or smaller resistor generally offers adequate protection. The value of the resistor is application-specific. TI recommends that each target board be validated for proper operation of the debugger and the application. This pin has an internal 50-ns (nominal) glitch filter.
INTERNAL VOLTAGE REGULATOR CONTROL					
VREGENZ		J18	119	I	Internal voltage regulator enable with internal pulldown. The internal VREG is not supported and must be disabled. Connect VREGENZ to V_{DDIO}.

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
ANALOG, DIGITAL, AND I/O POWER					
V_{DD}		E9	16		1.2-V digital logic power pins. TI recommends placing a decoupling capacitor near each V_{DD} pin with a minimum total capacitance of approximately 20 uF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.
		E11	21		
		F9	61		
		F11	76		
		G14	117		
		G15	126		
		J14	137		
		J15	153		
		K5	158		
		K6	169		
		P10	—		
		P13	—		
		R10	—		
		R13	—		
V_{DD3VFL}		R11	72		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin.
		R12	—		
V_{DDA}		P6	36		3.3-V analog power pins. Place a minimum 2.2-µF decoupling capacitor to V_{SSA} on each pin.
		R6	54		

Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
V_{DDIO}		A9	3		3.3-V digital I/O power pins. Place a minimum 0.1-µF decoupling capacitor on each pin. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.
		A18	11		
		B1	15		
		E7	20		
		E10	26		
		E13	62		
		E16	68		
		F4	75		
		F7	82		
		F10	88		
		F13	91		
		F16	99		
		G4	106		
		G5	114		
		G6	116		
		H5	127		
		H6	138		
		L14	147		
		L15	152		
		M1	159		
		M5	168		
		M6	—		
		N14	—		
		N15	—		
		P9	—		
		R9	—		
		V19	—		
		W8	—		
V_{DDOSC}		H16	120		Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-µF (minimum) decoupling capacitor on each pin.
		H17	125		

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
V_{SS}		A1	PWR PAD		Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB.
		A10			
		A19			
		E5			
		E6			
		E8			
		E12			
		E14			
		E15			
		F5			
		F6			
		F8			
		F12			
		F14			
		F15			
		G16			
		G17			
		H8			
		H9			
		H10			
		H11			
		H12			
		H14			
		H15			
		J5			
		J6			
		J8			
		J9			
		J10			
		J11			
		J12			
		K8			
		K9			
		K10			
		K11			
		K12			
		K14			
		K15			
		L5			
		L6			
		L8			
		L9			

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
V_{SS}		L10	PWR PAD		Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB.
		L11			
		L12			
		L18			
		M8			
		M9			
		M10			
		M11			
		M12			
		M14			
		M15			
		N1			
		N5			
		N6			
		P7			
		P8			
		P11			
		P12			
		P14			
		P15			
		R7			
		R8			
		R14			
		R15			
		W7			
		W19			
V_{SSOSC}		H18	122		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.
		H19	—		
V_{SSA}		P1	34		Analog ground. On the PZP package, pin 17 is double-bonded to V_{SSA} and V_{REFLOA}. This pin must be connect to V_{SSA}.
		P5	52		
		R5	—		
		V7	—		
		W1	—		

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Table 3-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
SPECIAL FUNCTIONS					
ERRORSTS		U19	92	O	Error status output. This pin has an internal pulldown.
TEST PINS					
FLT1		W12	73	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.
FLT2		V13	74	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.

(1) I = Input, O = Output, OD = Open Drain, Z = High Impedance

(2) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

(3) This pin has output impedance that can be as low as 22 Ω. This output could have fast edges and ringing depending on the system PCB characteristics. If this is a concern, the user should take precautions such as adding a 39 Ω (10% tolerance) series termination resistor or implement some other termination scheme. It is also recommended that a system-level signal integrity analysis be performed with the provided IBIS models. The termination is not required if this pin is used for input function.

3.3 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 3-2 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. In order to avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 3-2 with pullups and pulldowns are always on and cannot be disabled.

Table 3-2. Pins With Internal Pullup and Pulldown

PIN	RESET ($\overline{XRS}$ = 0)	DEVICE BOOT	APPLICATION SOFTWARE
GPIOx	Pullup disabled	Pullup disabled[1]	Pullup enable is application-defined
$\overline{TRST}$	Pulldown active		
TCK	Pullup active		
TMS	Pullup active		
TDI	Pullup active		
$\overline{XRS}$	Pullup active		
VREGENZ	Pulldown active		
ERRORSTS	Pulldown active		
Other pins	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

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3.4 Pin Multiplexing

3.4.1 GPIO Muxed Pins

Table 3-3 shows the GPIO muxed pins. The default for each pin is the GPIO function, secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured prior to the GPyMUXn to avoid transient pulses on GPIO's from alternate mux selections. Columns not shown and blank cells are reserved GPIO Mux settings.

Table 3-3. GPIO Muxed Pins(1)(2)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO0	EPWM1A (O)				SDAA (I/OD)		
	GPIO1	EPWM1B (O)		MFSRB (I/O)		SCLA (I/OD)		
	GPIO2	EPWM2A (O)			OUTPUTXBAR1 (O)	SDAB (I/OD)		
	GPIO3	EPWM2B (O)	OUTPUTXBAR2 (O)	MCLKRB (I/O)	OUTPUTXBAR2 (O)	SCLB (I/OD)		
	GPIO4	EPWM3A (O)			OUTPUTXBAR3 (O)	CANTXA (O)		
	GPIO5	EPWM3B (O)	MFSRA (I/O)	OUTPUTXBAR3 (O)		CANRXA (I)		
	GPIO6	EPWM4A (O)	OUTPUTXBAR4 (O)	EXTSYNCOUT (O)	EQEP3A (I)	CANTXB (O)		
	GPIO7	EPWM4B (O)	MCLKRA (I/O)	OUTPUTXBAR5 (O)	EQEP3B (I)	CANRXB (I)		
	GPIO8	EPWM5A (O)	CANTXB (O)	ADCSOCAO (O)	EQEP3S (I/O)	SCITXDA (O)		
	GPIO9	EPWM5B (O)	SCITXDB (O)	OUTPUTXBAR6 (O)	EQEP3I (I/O)	SCIRXDA (I)		
	GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCBO (O)	EQEP1A (I)	SCITXDB (O)		UPP-WAIT (I/O)
	GPIO11	EPWM6B (O)	SCIRXDB (I)	OUTPUTXBAR7 (O)	EQEP1B (I)	SCIRXDB (I)		UPP-START (I/O)
	GPIO12	EPWM7A (O)	CANTXB (O)	MDXB (O)	EQEP1S (I/O)	SCITXDC (O)		UPP-ENA (I/O)
	GPIO13	EPWM7B (O)	CANRXB (I)	MDRB (I)	EQEP1I (I/O)	SCIRXDC (I)		UPP-D7 (I/O)
	GPIO14	EPWM8A (O)	SCITXDB (O)	MCLKXB (I/O)		OUTPUTXBAR3 (O)		UPP-D6 (I/O)
	GPIO15	EPWM8B (O)	SCIRXDB (I)	MFSXB (I/O)		OUTPUTXBAR4 (O)		UPP-D5 (I/O)
	GPIO16	SPISIMOA (I/O)	CANTXB (O)	OUTPUTXBAR7 (O)	EPWM9A (O)		SD1_D1 (I)	UPP-D4 (I/O)
	GPIO17	SPISOMIA (I/O)	CANRXB (I)	OUTPUTXBAR8 (O)	EPWM9B (O)		SD1_C1 (I)	UPP-D3 (I/O)
	GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)	EPWM10A (O)		SD1_D2 (I)	UPP-D2 (I/O)
	GPIO19	$\overline{\text{SPISTEA}}$ (I/O)	SCIRXDB (I)	CANTXA (O)	EPWM10B (O)		SD1_C2 (I)	UPP-D1 (I/O)
	GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)	EPWM11A (O)		SD1_D3 (I)	UPP-D0 (I/O)
	GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)	EPWM11B (O)		SD1_C3 (I)	UPP-CLK (I/O)
	GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)	EPWM12A (O)	SPICLKB (I/O)	SD1_D4 (I)	
	GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)	EPWM12B (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD1_C4 (I)	
	GPIO24	OUTPUTXBAR1 (O)	EQEP2A (I)	MDXB (O)		SPISIMOB (I/O)	SD2_D1 (I)	
	GPIO25	OUTPUTXBAR2 (O)	EQEP2B (I)	MDRB (I)		SPISOMIB (I/O)	SD2_C1 (I)	
	GPIO26	OUTPUTXBAR3 (O)	EQEP2I (I/O)	MCLKXB (I/O)	OUTPUTXBAR3 (O)	SPICLKB (I/O)	SD2_D2 (I)	
	GPIO27	OUTPUTXBAR4 (O)	EQEP2S (I/O)	MFSXB (I/O)	OUTPUTXBAR4 (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD2_C2 (I)	
	GPIO28	SCIRXDA (I)	$\overline{\text{EM1CS4}}$ (O)		OUTPUTXBAR5 (O)	EQEP3A (I)	SD2_D3 (I)	
	GPIO29	SCITXDA (O)	EM1SDCKE (O)		OUTPUTXBAR6 (O)	EQEP3B (I)	SD2_C3 (I)	
	GPIO30	CANRXA (I)	EM1CLK (O)		OUTPUTXBAR7 (O)	EQEP3S (I/O)	SD2_D4 (I)	
	GPIO31	CANTXA (O)	$\overline{\text{EM1WE}}$ (O)		OUTPUTXBAR8 (O)	EQEP3I (I/O)	SD2_C4 (I)	
	GPIO32	SDAA (I/OD)	$\overline{\text{EM1CS0}}$ (O)					
	GPIO33	SCLA (I/OD)	EM1RNW (O)					
	GPIO34	OUTPUTXBAR1 (O)	$\overline{\text{EM1CS2}}$ (O)			SDAB (I/OD)		
	GPIO35	SCIRXDA (I)	$\overline{\text{EM1CS3}}$ (O)			SCLB (I/OD)		
	GPIO36	SCITXDA (O)	EM1WAIT (I)			CANRXA (I)		
	GPIO37	OUTPUTXBAR2 (O)	$\overline{\text{EM1OE}}$ (O)			CANTXA (O)		
	GPIO38		EM1A0 (O)		SCITXDC (O)	CANTXB (O)		
	GPIO39		EM1A1 (O)		SCIRXDC (I)	CANRXB (I)		

(1) I = Input, O = Output, OD = Open Drain
(2) GPIO Index settings of 9, 10, 11, 13, and 14 are reserved.

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Table 3-3. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO40		EM1A2 (O)			SDAB (I/OD)		
	GPIO41		EM1A3 (O)			SCLB (I/OD)		
	GPIO42					SDAA (I/OD)		SCITXDA (O)
	GPIO43					SCLA (I/OD)		SCIRXDA (I)
	GPIO44		EM1A4 (O)					
	GPIO45		EM1A5 (O)					
	GPIO46		EM1A6 (O)			SCIRXDD (I)		
	GPIO47		EM1A7 (O)			SCITXDD (O)		
	GPIO48	OUTPUTXBAR3 (O)	EM1A8 (O)			SCITXDA (O)	SD1_D1 (I)	
	GPIO49	OUTPUTXBAR4 (O)	EM1A9 (O)			SCIRXDA (I)	SD1_C1 (I)	
	GPIO50	EQEP1A (I)	EM1A10 (O)			SPISIMOC (I/O)	SD1_D2 (I)	
	GPIO51	EQEP1B (I)	EM1A11 (O)			SPISOMIC (I/O)	SD1_C2 (I)	
	GPIO52	EQEP1S (I/O)	EM1A12 (O)			SPICLKC (I/O)	SD1_D3 (I)	
	GPIO53	EQEP1I (I/O)	EM1D31 (I/O)	EM2D15 (I/O)		$\overline{\text{SPISTEC}}$ (I/O)	SD1_C3 (I)	
	GPIO54	SPISIMOA (I/O)	EM1D30 (I/O)	EM2D14 (I/O)	EQEP2A (I)	SCITXDB (O)	SD1_D4 (I)	
	GPIO55	SPISOMIA (I/O)	EM1D29 (I/O)	EM2D13 (I/O)	EQEP2B (I)	SCIRXDB (I)	SD1_C4 (I)	
	GPIO56	SPICLKA (I/O)	EM1D28 (I/O)	EM2D12 (I/O)	EQEP2S (I/O)	SCITXDC (O)	SD2_D1 (I)	
	GPIO57	$\overline{\text{SPISTEA}}$ (I/O)	EM1D27 (I/O)	EM2D11 (I/O)	EQEP2I (I/O)	SCIRXDC (I)	SD2_C1 (I)	
	GPIO58	MCLKRA (I/O)	EM1D26 (I/O)	EM2D10 (I/O)	OUTPUTXBAR1 (O)	SPICLKB (I/O)	SD2_D2 (I)	SPISIMOA[3] (I/O)
	GPIO59	MFSRA (I/O)	EM1D25 (I/O)	EM2D9 (I/O)	OUTPUTXBAR2 (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD2_C2 (I)	SPISOMIA[3] (I/O)
	GPIO60	MCLKRB (I/O)	EM1D24 (I/O)	EM2D8 (I/O)	OUTPUTXBAR3 (O)	SPISIMOB (I/O)	SD2_D3 (I)	SPICLKA[3] (I/O)
	GPIO61	MFSRB (I/O)	EM1D23 (I/O)	EM2D7 (I/O)	OUTPUTXBAR4 (O)	SPISOMIB (I/O)	SD2_C3 (I)	$\overline{\text{SPISTEA}}$[3] (I/O)
	GPIO62	SCIRXDC (I)	EM1D22 (I/O)	EM2D6 (I/O)	EQEP3A (I)	CANRXA (I)	SD2_D4 (I)	
	GPIO63	SCITXDC (O)	EM1D21 (I/O)	EM2D5 (I/O)	EQEP3B (I)	CANTXA (O)	SD2_C4 (I)	SPISIMOB[3] (I/O)
	GPIO64		EM1D20 (I/O)	EM2D4 (I/O)	EQEP3S (I/O)	SCIRXDA (I)		SPISOMIB[3] (I/O)
	GPIO65		EM1D19 (I/O)	EM2D3 (I/O)	EQEP3I (I/O)	SCITXDA (O)		SPICLKB[3] (I/O)
	GPIO66		EM1D18 (I/O)	EM2D2 (I/O)		SDAB (I/OD)		$\overline{\text{SPISTEB}}$[3] (I/O)
	GPIO67		EM1D17 (I/O)	EM2D1 (I/O)				
	GPIO68		EM1D16 (I/O)	EM2D0 (I/O)				
	GPIO69		EM1D15 (I/O)			SCLB (I/OD)		SPISIMOC[3] (I/O)
	GPIO70		EM1D14 (I/O)		CANRXA (I)	SCITXDB (O)		SPISOMIC[3] (I/O)
	GPIO71		EM1D13 (I/O)		CANTXA (O)	SCIRXDB (I)		SPICLKC[3] (I/O)
	GPIO72		EM1D12 (I/O)		CANTXB (O)	SCITXDC (O)		$\overline{\text{SPISTEC}}$[3] (I/O)
	GPIO73		EM1D11 (I/O)	XCLKOUT (O)	CANRXB (I)	SCIRXDC (I)		
	GPIO74		EM1D10 (I/O)					
	GPIO75		EM1D9 (I/O)					
	GPIO76		EM1D8 (I/O)			SCITXDD (O)		
	GPIO77		EM1D7 (I/O)			SCIRXDD (I)		
	GPIO78		EM1D6 (I/O)			EQEP2A (I)		
	GPIO79		EM1D5 (I/O)			EQEP2B (I)		
	GPIO80		EM1D4 (I/O)			EQEP2S (I/O)		
	GPIO81		EM1D3 (I/O)			EQEP2I (I/O)		
	GPIO82		EM1D2 (I/O)					
	GPIO83		EM1D1 (I/O)					
	GPIO84				SCITXDA (O)	MDXB (O)		MDXA (O)
	GPIO85		EM1D0 (I/O)		SCIRXDA (I)	MDRB (I)		MDRA (I)
	GPIO86		EM1A13 (O)	EM1CAS (O)	SCITXDB (O)	MCLKXB (I/O)		MCLKXA (I/O)
	GPIO87		EM1A14 (O)	EM1RAS (O)	SCIRXDB (I)	MFSXB (I/O)		MFSXA (I/O)
	GPIO88		EM1A15 (O)	EM1DQM0 (O)				
	GPIO89		EM1A16 (O)	EM1DQM1 (O)		SCITXDC (O)		

(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

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Table 3-3. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO90		EM1A17 (O)	EM1DQM2 (O)		SCIRXDC (I)		
	GPIO91		EM1A18 (O)	EM1DQM3 (O)		SDAA (I/OD)		
	GPIO92		EM1A19 (O)	EM1BA1 (O)		SCLA (I/OD)		
	GPIO93			EM1BA0 (O)		SCITXDD (O)		
	GPIO94					SCIRXDD (I)		
	GPIO95							
	GPIO96			EM2DQM1 (O)	EQEP1A (I)			
	GPIO97			EM2DQM0 (O)	EQEP1B (I)			
	GPIO98			EM2A0 (O)	EQEP1S (I/O)			
	GPIO99			EM2A1 (O)	EQEP1I (I/O)			
	GPIO100			EM2A2 (O)	EQEP2A (I)	SPISIMOC (I/O)		
	GPIO101			EM2A3 (O)	EQEP2B (I)	SPISOMIC (I/O)		
	GPIO102			EM2A4 (O)	EQEP2S (I/O)	SPICLKC (I/O)		
	GPIO103			EM2A5 (O)	EQEP2I (I/O)	$\overline{\text{SPISTEC}}$ (I/O)		
	GPIO104	SDAA (I/OD)		EM2A6 (O)	EQEP3A (I)	SCITXDD (O)		
	GPIO105	SCLA (I/OD)		EM2A7 (O)	EQEP3B (I)	SCIRXDD (I)		
	GPIO106			EM2A8 (O)	EQEP3S (I/O)	SCITXDC (O)		
	GPIO107			EM2A9 (O)	EQEP3I (I/O)	SCIRXDC (I)		
	GPIO108			EM2A10 (O)				
	GPIO109			EM2A11 (O)				
	GPIO110			EM2WAIT (I)				
	GPIO111			EM2BA0 (O)				
	GPIO112			EM2BA1 (O)				
	GPIO113			EM2CAS (O)				
	GPIO114			EM2RAS (O)				
	GPIO115			$\overline{\text{EM2CS0}}$ (O)				
	GPIO116			$\overline{\text{EM2CS2}}$ (O)				
	GPIO117			EM2SDCKE (O)				
	GPIO118			EM2CLK (O)				
	GPIO119			EM2RNW (O)				
	GPIO120			$\overline{\text{EM2WE}}$ (O)				USB0PFLT
	GPIO121			$\overline{\text{EM2OE}}$ (O)				USB0EPEN
	GPIO122					SPISIMOC (I/O)	SD1_D1 (I)	
	GPIO123					SPISOMIC (I/O)	SD1_C1 (I)	
	GPIO124					SPICLKC (I/O)	SD1_D2 (I)	
	GPIO125					$\overline{\text{SPISTEC}}$ (I/O)	SD1_C2 (I)	
	GPIO126						SD1_D3 (I)	
	GPIO127						SD1_C3 (I)	
	GPIO128						SD1_D4 (I)	
	GPIO129						SD1_C4 (I)	
	GPIO130						SD2_D1 (I)	
	GPIO131						SD2_C1 (I)	
	GPIO132						SD2_D2 (I)	
	GPIO133/ AUXCLKIN						SD2_C2 (I)	
	GPIO134						SD2_D3 (I)	
	GPIO135					SCITXDA (O)	SD2_C3 (I)	
	GPIO136					SCIRXDA (I)	SD2_D4 (I)	
	GPIO137					SCITXDB (O)	SD2_C4 (I)	
	GPIO138					SCIRXDB (I)		
	GPIO139					SCIRXDC (I)		
	GPIO140					SCITXDC (O)		

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Table 3-3. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO141					SCIRXDD (I)		
	GPIO142					SCITXDD (O)		
	GPIO143							
	GPIO144							
	GPIO145	EPWM1A (O)						
	GPIO146	EPWM1B (O)						
	GPIO147	EPWM2A (O)						
	GPIO148	EPWM2B (O)						
	GPIO149	EPWM3A (O)						
	GPIO150	EPWM3B (O)						
	GPIO151	EPWM4A (O)						
	GPIO152	EPWM4B (O)						
	GPIO153	EPWM5A (O)						
	GPIO154	EPWM5B (O)						
	GPIO155	EPWM6A (O)						
	GPIO156	EPWM6B (O)						
	GPIO157	EPWM7A (O)						
	GPIO158	EPWM7B (O)						
	GPIO159	EPWM8A (O)						
	GPIO160	EPWM8B (O)						
	GPIO161	EPWM9A (O)						
	GPIO162	EPWM9B (O)						
	GPIO163	EPWM10A (O)						
	GPIO164	EPWM10B (O)						
	GPIO165	EPWM11A (O)						
	GPIO166	EPWM11B (O)						
	GPIO167	EPWM12A (O)						
	GPIO168	EPWM12B (O)						

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3.4.2 Input X-BAR

The Input X-BAR is used to route any GPIO input to the ADC, eCAP, and ePWM peripherals as well as to external interrupts (XINT) (see Figure 3-6). Table 3-4 shows the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

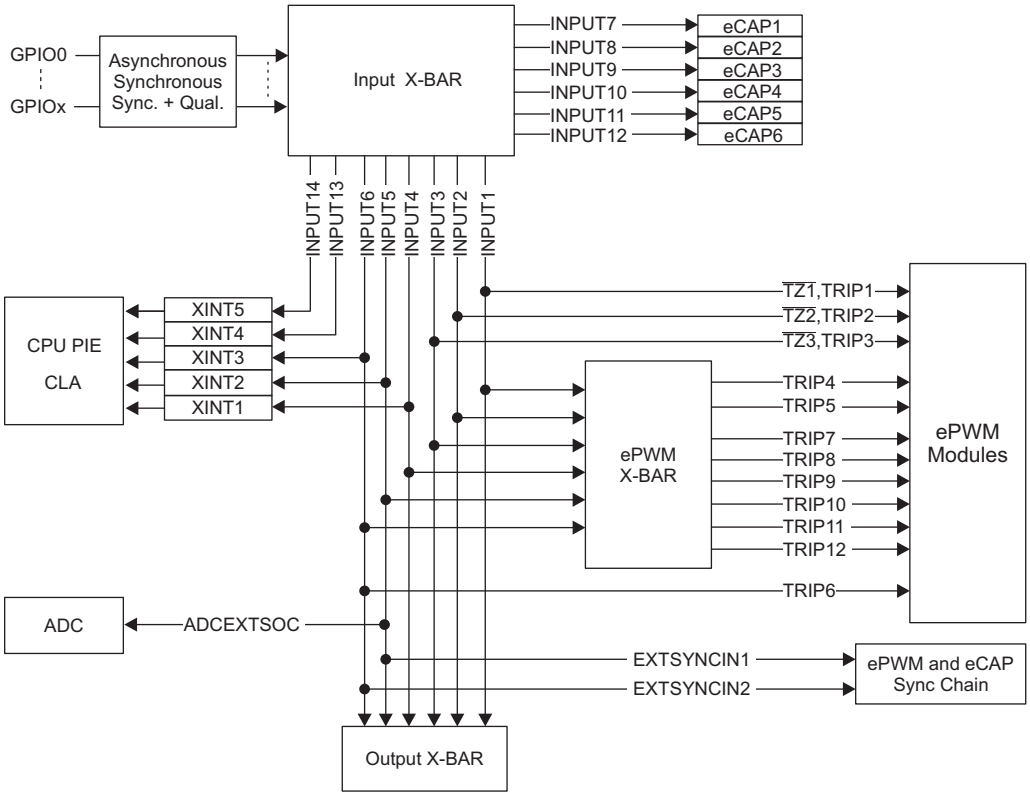


Figure 3-6. Input X-BAR

Table 3-4. Input X-BAR Destinations

INPUT	DESTINATIONS
INPUT1	EPWM[TZ1,TRIP1], EPWM X-BAR, Output X-BAR
INPUT2	EPWM[TZ2,TRIP2], EPWM X-BAR, Output X-BAR
INPUT3	EPWM[TZ3,TRIP3], EPWM X-BAR, Output X-BAR
INPUT4	XINT1, EPWM X-BAR, Output X-BAR
INPUT5	XINT2, ADCEXTSOC, EXTSYNCIN1, EPWM X-BAR, Output X-BAR
INPUT6	XINT3, EPWM[TRIP6], EXTSYNCIN2, EPWM X-BAR, Output X-BAR
INPUT7	ECAP1
INPUT8	ECAP2
INPUT9	ECAP3
INPUT10	ECAP4
INPUT11	ECAP5
INPUT12	ECAP6
INPUT13	XINT4
INPUT14	XINT5

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3.4.3 Output X-BAR and ePWM X-BAR

The Output X-BAR has eight outputs which can be selected on the GPIO mux as OUTPUTXBARx. The ePWM X-BAR has eight outputs which are connected to the TRIPx inputs of the ePWM. The sources for both the Output X-BAR and ePWM X-BAR are shown in Figure 3-7. For details on the Output X-BAR and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

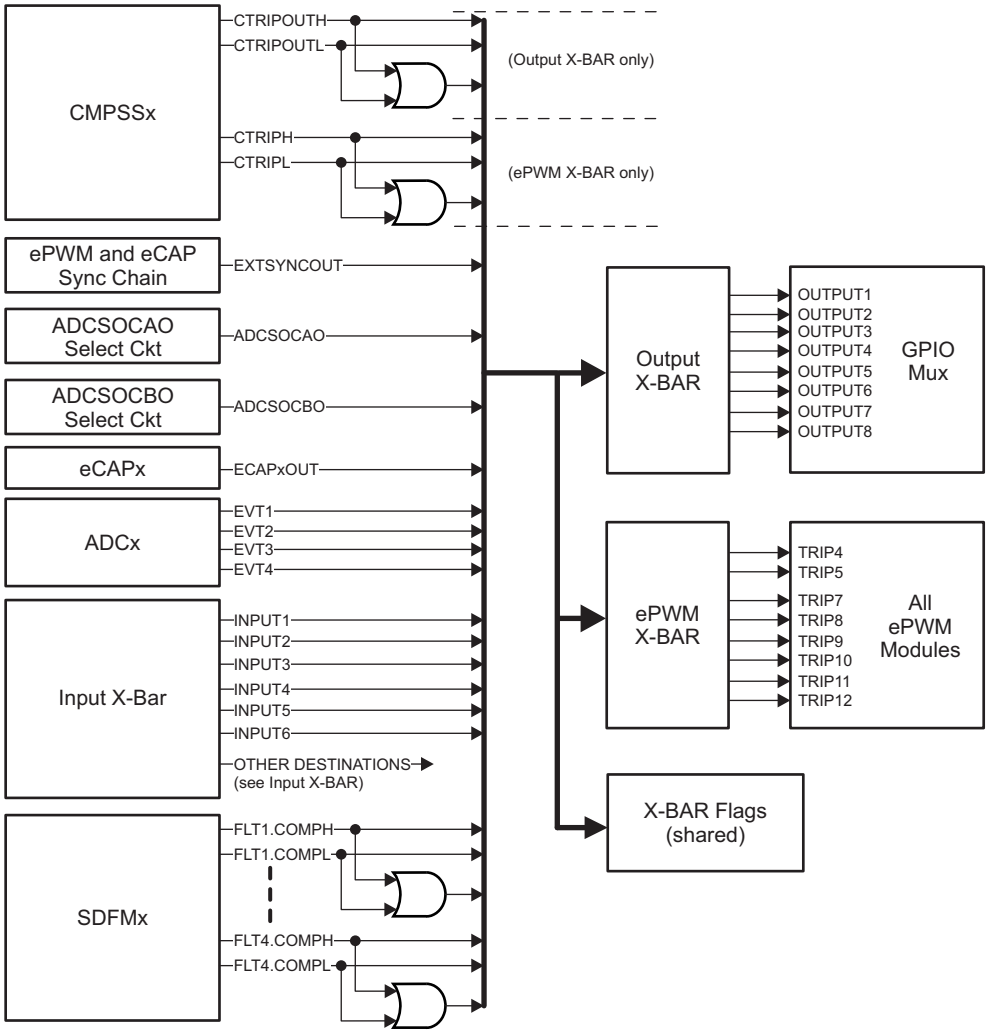


Figure 3-7. Output X-BAR and ePWM X-BAR

3.4.4 USB Pin Muxing

Table 3-5 shows assignment of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 3-5. Alternate USB Function

GPIO	GPBAMSEL SETTING	USB FUNCTION
GPIO42	GPBAMSEL[10] = 1b	USB0DM
GPIO43	GPBAMSEL[11] = 1b	USB0DP

3.4.5 High-Speed SPI Pin Muxing

The SPI module on this device has a high-speed mode. To achieve the highest possible speed, a special GPIO configuration is used on a single GPIO mux option for each SPI. These GPIOs may also be used by the SPI when not in high-speed mode (HS_MODE = 0).

To select the mux options that enable the SPI high-speed mode, configure the GPyGMUX and GPyMUX registers as shown in Table 3-6.

Table 3-6. GPIO Configuration for High-Speed SPI

GPIO	SPI SIGNAL	MUX CONFIGURATION	
SPIA			
GPIO58	SPISIMOA	GPBGMUX2[21:20]=11b	GPBMUX2[21:20]=11b
GPIO59	SPISOMIA	GPBGMUX2[23:22]=11b	GPBMUX2[23:22]=11b
GPIO60	SPICLKA	GPBGMUX2[25:24]=11b	GPBMUX2[25:24]=11b
GPIO61	$\overline{\text{SPISTEA}}$	GPBGMUX2[27:26]=11b	GPBMUX2[27:26]=11b
SPIB			
GPIO63	SPISIMOB	GPBGMUX2[31:30]=11b	GPBMUX2[31:30]=11b
GPIO64	SPISOMIB	GPCGMUX1[1:0]=11b	GPCMUX1[1:0]=11b
GPIO65	SPICLKB	GPCGMUX1[3:2]=11b	GPCMUX1[3:2]=11b
GPIO66	$\overline{\text{SPISTEB}}$	GPCGMUX1[5:4]=11b	GPCMUX1[5:4]=11b
SPIC			
GPIO69	SPISIMOC	GPCGMUX1[11:10]=11b	GPCMUX1[11:10]=11b
GPIO70	SPISOMIC	GPCGMUX1[13:12]=11b	GPCMUX1[13:12]=11b
GPIO71	SPICLKC	GPCGMUX1[15:14]=11b	GPCMUX1[15:14]=11b
GPIO72	$\overline{\text{SPISTEC}}$	GPCGMUX1[17:16]=11b	GPCMUX1[17:16]=11b

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3.5 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 3-7 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 3-7, any are acceptable. Pins not listed in Table 3-7 must be connected according to Table 3-1.

Table 3-7. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
Analog	
V_{REFHIx}	Tie to V_{DDA}
V_{REFLOx}	Tie to V_{SSA}
ADCINx	• No Connect • Tie to V_{SSA}
Digital	
GPIOx	• Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
X1	Tie to V_{SS}
X2	No Connect
TCK	• No Connect • Pullup resistor
TDI	• No Connect • Pullup resistor
TDO	No Connect
TMS	No Connect
$\overline{TRST}$	Pulldown resistor (2.2 kΩ or smaller)
VREGENZ	Tie to V_{DDIO}. VREG is not supported.
ERRORSTS	No Connect
FLT1	No Connect
FLT2	No Connect
Power and Ground	
V_{DD}	All V_{DD} pins must be connected per Table 3-1.
V_{DDA}	If a separate analog supply is not used, tie to V_{DDIO}.
V_{DDIO}	All V_{DDIO} pins must be connected per Table 3-1.
V_{DD3VFL}	Must be tied to V_{DDIO}
V_{DDOSC}	Must be tied to V_{DDIO}
V_{SS}	All V_{SS} pins must be connected to board ground.
V_{SSA}	If a separate analog ground is not used, tie to V_{SS}.
V_{SSOSC}	If an external crystal is not used, this pin may be connected to the board ground.

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4 Specifications

4.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{DDIO} with respect to V_{SS}	–0.3	4.6	V
	V_{DD3VFL} with respect to V_{SS}	–0.3	4.6	
	V_{DDOSC} with respect to V_{SS}	–0.3	4.6	
	V_{DD} with respect to V_{SS}	–0.3	1.5	
Analog voltage	V_{DDA} with respect to V_{SSA}	–0.3	4.6	V
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital input (per pin), I_{IK} ($V_{IN} < V_{SS}$ or $V_{IN} > V_{DDIO}$)	–20	20	mA
	Analog input (per pin), $I_{IKANALOG}$ ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$)	–20	20	
	Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Operating junction temperature	T_J	–55	150	°C
Storage temperature(3)	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *Semiconductor and IC Package Thermal Metrics*.

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4.2 ESD Ratings

			VALUE	UNIT
TMS320F28377D in 337-ball ZWT package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	
TMS320F28377D in 176-pin PTP package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

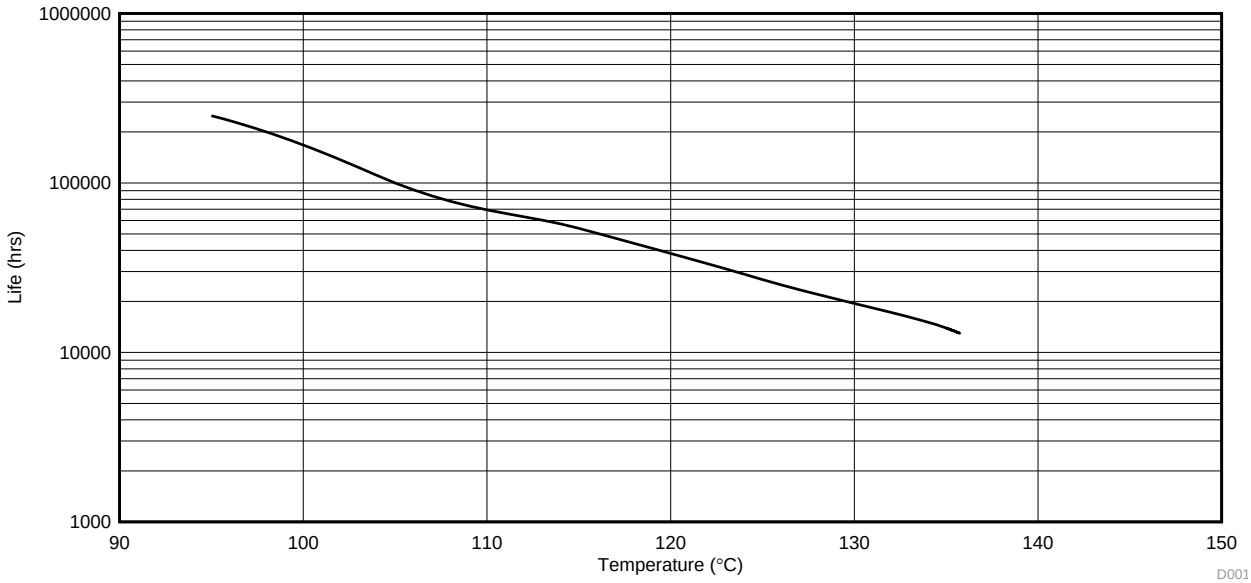
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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4.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO} (1)	3.14	3.3	3.47	V
Device supply voltage, V_{DD}	1.14	1.2	1.26	V
Supply ground, V_{SS}		0		V
Analog supply voltage, V_{DDA}	3.14	3.3	3.47	V
Analog ground, V_{SSA}		0		V
Junction temperature, T_J (2)	–55		125	°C

(1) V_{DDIO}, V_{DD3VFL}, and V_{DDOSC} should be maintained within 0.3 V of each other.
(2) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.



(1) Silicon operating life design goal is 100000 power-on hours (POH) at 105°C junction temperature (does not include package interconnect life).
(2) The predicted operating lifetime versus junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 4-1. TMS320F28377D-EP Operating Life Derating Chart

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4.4 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Table 4-1 shows the device current consumption at 200-MHz SYSCLK.

Table 4-1. Device Current Consumption at 200-MHz SYSCLK

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DDA}		I_{DD3VFL}	
		TYP (2)	MAX (3)	TYP (2)	MAX (3)	TYP (2)	MAX (3)	TYP (2)	MAX (3)
Operational (RAM)	• Code is running out of RAM. (4) • All I/O pins are left unconnected. • Peripherals not active have their clocks disabled. • FLASH is read and in active state. • XCLKOUT is enabled at SYSCLK/4.	325 mA	440 mA	30 mA		13 mA	20 mA	33 mA	40 mA
IDLE	• Both CPU1 and CPU2 are in IDLE mode. • Flash is powered down. • XCLKOUT is turned off.	105 mA	210 mA	3 mA	10 mA	10 µA	150 µA	10 µA	150 µA
STANDBY	• Both CPU1 and CPU2 are in STANDBY mode. • Flash is powered down. • XCLKOUT is turned off.	30 mA	135 mA	3 mA	10 mA	5 µA	150 µA	10 µA	150 µA
HALT (5)	• CPU1 watchdog is running. • Flash is powered down. • XCLKOUT is turned off.	1.5 mA	110 mA	750 µA	2 mA	5 µA	150 µA	10 µA	150 µA
HIBERNATE (6)	• CPU1.M0 and CPU1.M1 RAMs are in low-power data retention mode. • CPU2.M0 and CPU2.M1 RAMs are in low-power data retention mode.	300 µA	4 mA	750 µA	2 mA	5 µA	75 µA	1 µA	50 µA
Flash Erase/Program	• CPU1 is running from RAM. • CPU2 is running from Flash. • All I/O pins are left unconnected. • Peripheral clocks are disabled. • CPU1 is performing Flash Erase and Programming. • CPU2 is accessing Flash locations to keep bank active. • XCLKOUT is turned off.	242 mA	360 mA	3 mA	10 mA	10 µA	150 µA	53 mA	65 mA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) TYP: V_{nom}, 30°C
(3) MAX: V_{max}, 125°C
(4) The following is executed in a loop on CPU1:
- All of the communication peripherals are exercised in loop-back mode: CAN-A to CAN-B; SPI-A to SPI-C; SCI-A to SCI-D; I2C-A to I2C-B; McBSP-A to McBSP-B; USB
- SDFM1 to SDFM4 active
- ePWM1 to ePWM12 generate 400-kHz PWM output on 24 pins
- CPU TIMERs active
- DMA does 32-bit burst transfers
- CLA1 does multiply-accumulate tasks
- All ADCs perform continuous conversion
- All DACs ramp voltage up/down at 150 kHz
- CMPSS1 to CMPSS8 active

The following is executed in a loop on CPU2:
- CPU TIMERs active
- CLA1 does multiply-accumulate tasks
- VCU does complex multiply/accumulate with parallel load
- TMU calculates a cosine
- FPU does multiply/accumulate with parallel load

(5) CPU2 must go into IDLE mode before CPU1 enters HALT mode.
(6) CPU2 must go into reset/IDLE/STANDBY mode before CPU1 enters HIBERNATE mode.

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4.4.1 Current Consumption Graphs

Figure 4-2 and Figure 4-3 are a typical representation of the relationship between frequency and current consumption/power on the device. The operational test from Table 4-1 was run across frequency at V_{max} and high temperature. Actual results will vary based on the system implementation and conditions.

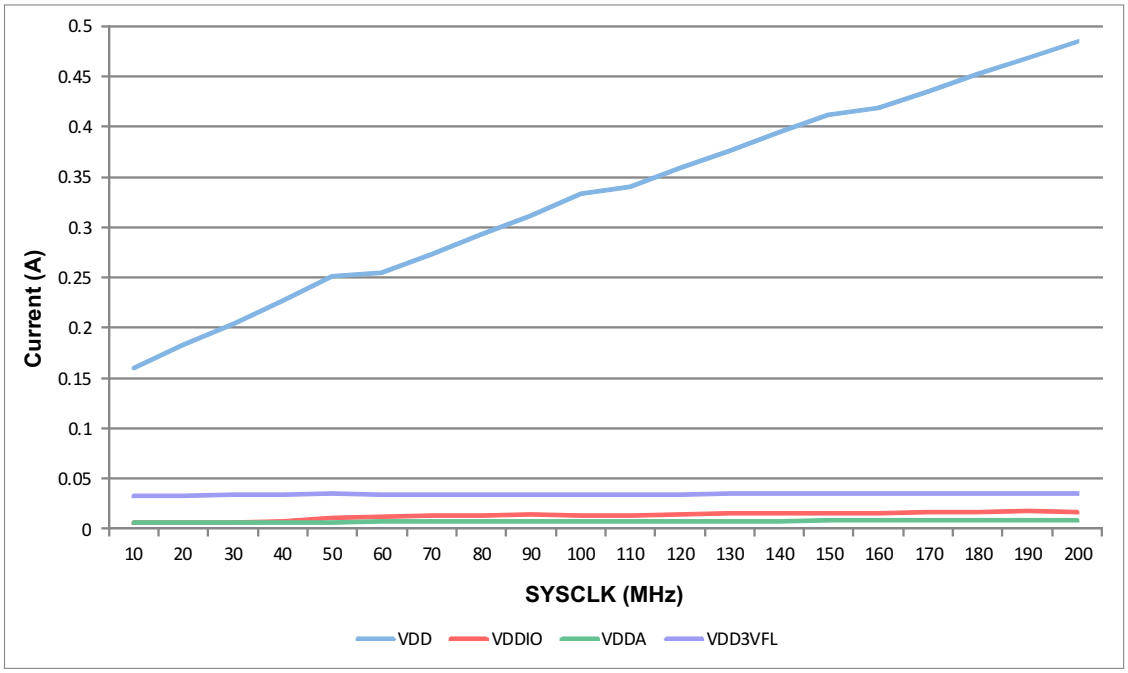


Figure 4-2. Operational Current Versus Frequency

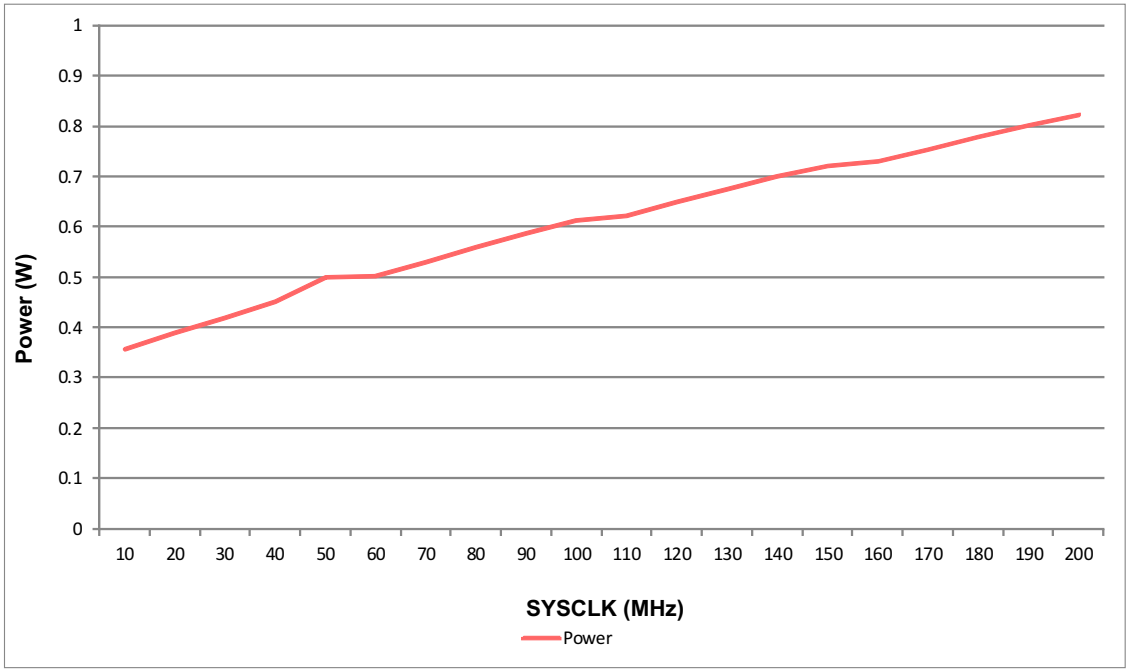


Figure 4-3. Power Versus Frequency

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Leakage current will increase with operating temperature in a nonlinear manner. The difference in V_{DD} current between TYP and MAX conditions can be seen in Figure 4-4. The current consumption in HALT mode is primarily leakage current as there is no active switching if the internal oscillator has been powered down.

Figure 4-4 shows the typical leakage current across temperature. The device was placed into HALT mode under nominal voltage conditions.

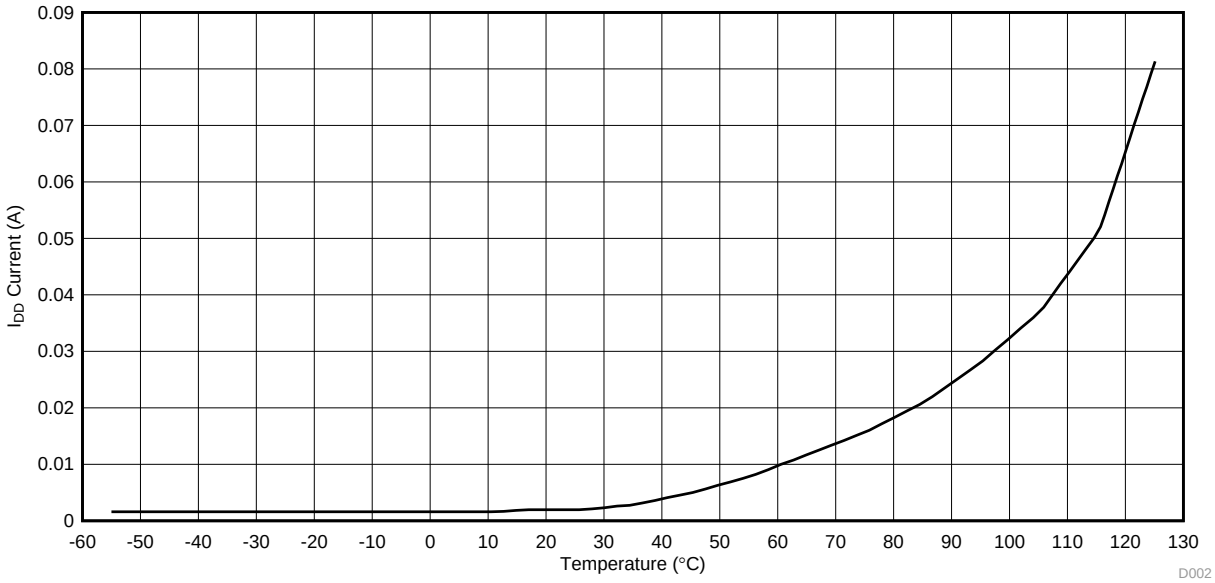


Figure 4-4. I_{DD} Leakage Current Versus Temperature

4.4.2 Reducing Current Consumption

The F28377D provides some methods to reduce the device current consumption:

- Any one of the four low-power modes—IDLE, STANDBY, HALT, and HIBERNATE—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. Table 4-2 indicates the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.

Table 4-2. Current on V_{DD} Supply by Various Peripherals (at 200 MHz)(1)

PERIPHERAL MODULE(2)	I_{DD} CURRENT REDUCTION (mA)
ADC(3)	3.3
CAN	3.3
CLA	1.4
CMPSS(3)	1.4
CPUTIMER	0.3
DAC(3)	0.6
DMA	2.9
eCAP	0.6
EMIF1	2.9
EMIF2	2.6
ePWM1 to ePWM4(4)	4.5
ePWM5 to ePWM12(4)	1.7
HRPWM(4)	1.7
I2C	1.3
McBSP	1.6
SCI	0.9
SDFM	2
SPI	0.5
uPP	7.3
USB and AUXPLL at 60 MHz	23.8

(1) At V_{max} and 125°C.
(2) All peripherals are disabled upon reset. Use the PCLKCRx register to individually enable peripherals. For peripherals with multiple instances, the current quoted is for a single module.
(3) This number represents the current drawn by the digital portion of the ADC, CMPSS, and DAC modules.
(4) The ePWM is at /2 of SYSCLK.

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4.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	V_{DDIO} * 0.8			V
			I_{OH} = –100 µA	V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100 µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
V_{IH}	High-level input voltage (3.3 V)	GPIO0–GPIO7, GPIO42–GPIO43, GPIO46–GPIO47		V_{DDIO} * 0.7		V_{DDIO} + 0.3	V
		All other pins		2.0		V_{DDIO} + 0.3	
V_{IL}	Low-level input voltage (3.3 V)			V_{SS} – 0.3		0.8	V
$I_{pulldown}$	Input current	Digital inputs with pulldown(1)	V_{DDIO} = 3.3 V V_{IN} = V_{DDIO}		120		µA
I_{pullup}	Input current	Digital inputs with pullup enabled(1)	V_{DDIO} = 3.3 V V_{IN} = 0 V		150		µA
I_{LEAK}	Pin leakage	Digital	Pullups disabled 0 V ≤ V_{IN} ≤ V_{DDIO}			2	µA
		Analog (except ADCINB0 or DACOUTx)	0 V ≤ V_{IN} ≤ V_{DDA}			2	
		ADCINB0			2	11(2)	
		DACOUTx			66		
C_I	Input capacitance				2		pF

(1) See Table 3-2 for a list of pins with a pullup or pulldown.
(2) The MAX input leakage shown on ADCINB0 is at high temperature.

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4.6 Thermal Resistance Characteristics

4.6.1 GWT Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	8.8	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	11.6	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	23.2	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	19.0	150
		17.8	250
		16.5	500
Psi_{JT}	Junction-to-package top	0.2	0
		0.3	150
		0.4	250
		0.5	500
Psi_{JB}	Junction-to-board	11.4	0
		11.3	150
		11.2	250
		11.0	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

4.6.2 PTP Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	10.2	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	7.9	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	19.4	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	12.8	150
		11.4	250
		10.1	500
Psi_{JT}	Junction-to-package top	0.11	0
		0.24	150
		0.33	250
		0.42	500
Psi_{JB}	Junction-to-board	6.1	0
		5.5	150
		5.4	250
		5.3	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

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4.7 System

4.7.1 Power Sequencing

An external power supply must be used to supply 3.3 V to V_{DDIO}, V_{DD3VFL}, V_{DDOSC}, and V_{DDA} and to provide 1.2 V to V_{DD}. The internal VREG is not supported; therefore, the VREGENZ pin must be tied high to 3.3 V. The supplies should ramp to full rail within 10 ms. Table 4-3 shows the supply ramp rate.

Table 4-3. Supply Ramp Rate

		MIN	MAX	UNIT
Supply ramp rate	V_{DDIO}, V_{DD}, V_{DDA}, V_{DD3VFL}, V_{DDOSC} with respect to V_{SS}	330	10^5	V/s

The voltage on V_{DDIO} should be greater than V_{DD} or no less than 0.3 V below V_{DD} at all times. V_{DDIO}, V_{DD3VFL}, V_{DDOSC}, and V_{DDA} should be powered up together and be kept within 0.3 V of each other during operation. Before powering the device, no voltage larger than 0.3 V above V_{DDIO} should be applied to any digital pin, and no voltage larger than 0.3 V above V_{DDA} should be applied to any analog pin. The V_{REFHI} voltage should not exceed V_{DDA} at any time.

An internal power-on-reset (POR) circuit holds the device in reset and keeps the I/Os in a high-impedance state during power up. External supply voltage supervisors (SVS) can be used to monitor the voltage on the 3.3-V and 1.2-V rails and drive $\overline{\text{XRS}}$ low should supplies fall outside operational specifications.

4.7.2 Reset Timing

$\overline{\text{XRS}}$ is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR). During power up, the POR circuit drives the $\overline{\text{XRS}}$ pin low. A watchdog or NMI watchdog reset also drives the pin low. An external circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. A capacitor should be placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering; the capacitance should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 4-5 shows the recommended reset circuit.

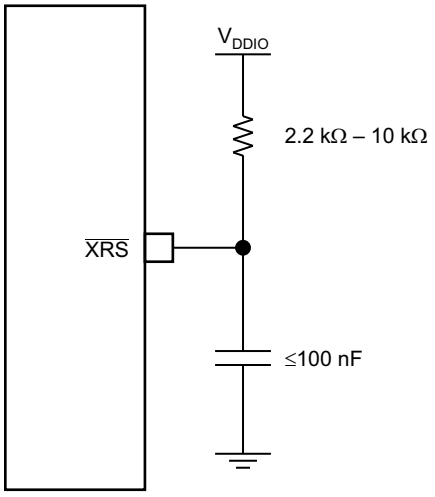


Figure 4-5. Reset Circuit

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4.7.2.1 Reset Sources

The following reset sources exist on this device: $\overline{\text{XRS}}$, $\overline{\text{WDRS}}$, $\overline{\text{NMIWDRS}}$, $\overline{\text{SYSRS}}$, $\overline{\text{SCCRESET}}$, and $\overline{\text{HIBRESET}}$. See the Reset Signals table in the System Control chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive $\overline{\text{XRS}}$ low. Use this to disable any other devices driving the boot pins. The $\overline{\text{SCCRESET}}$ and debugger reset sources do not drive $\overline{\text{XRS}}$; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP; for more details, see the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

4.7.2.2 Reset Electrical Data and Timing

Table 4-4 shows the reset ($\overline{\text{XRS}}$) timing requirements. Table 4-5 shows the reset ($\overline{\text{XRS}}$) switching characteristics. Figure 4-6 shows the power-on reset. Figure 4-7 shows the warm reset.

Table 4-4. Reset ($\overline{\text{XRS}}$) Timing Requirements

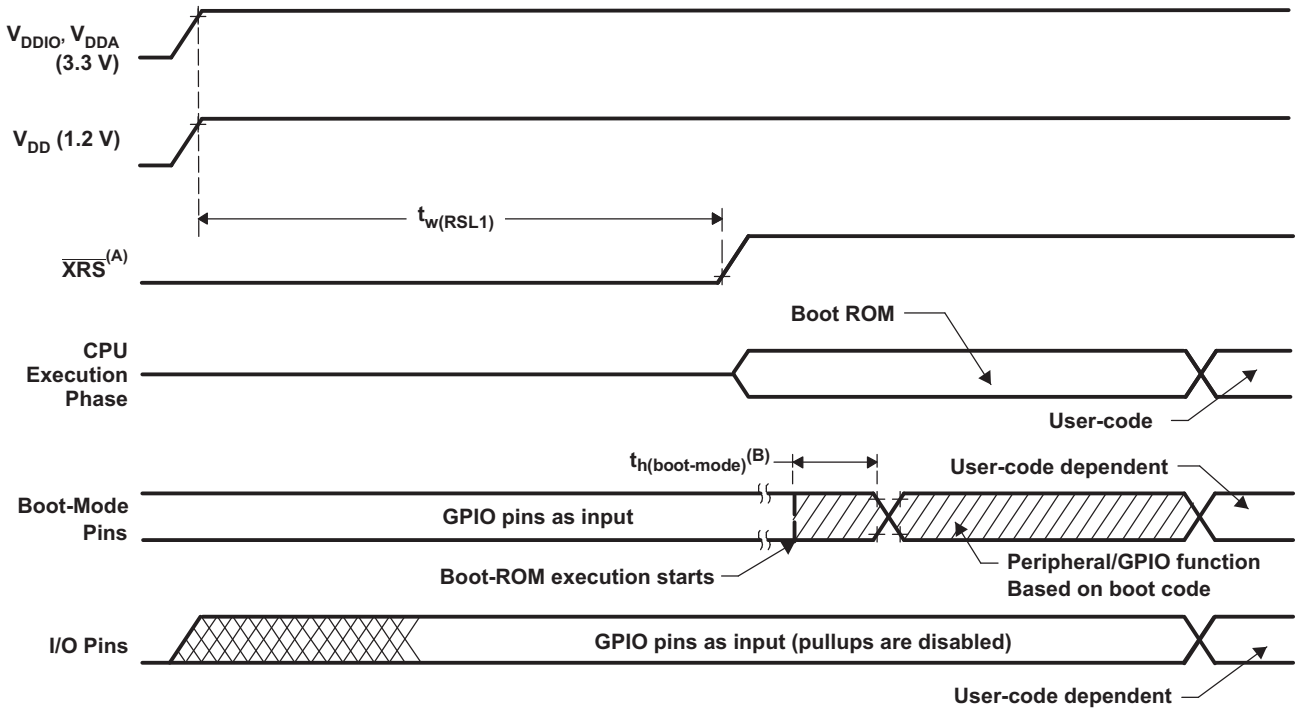
		MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, $\overline{\text{XRS}}$ low on warm reset	3.2		µs

Table 4-5. Reset ($\overline{\text{XRS}}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{\text{XRS}}$ driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles

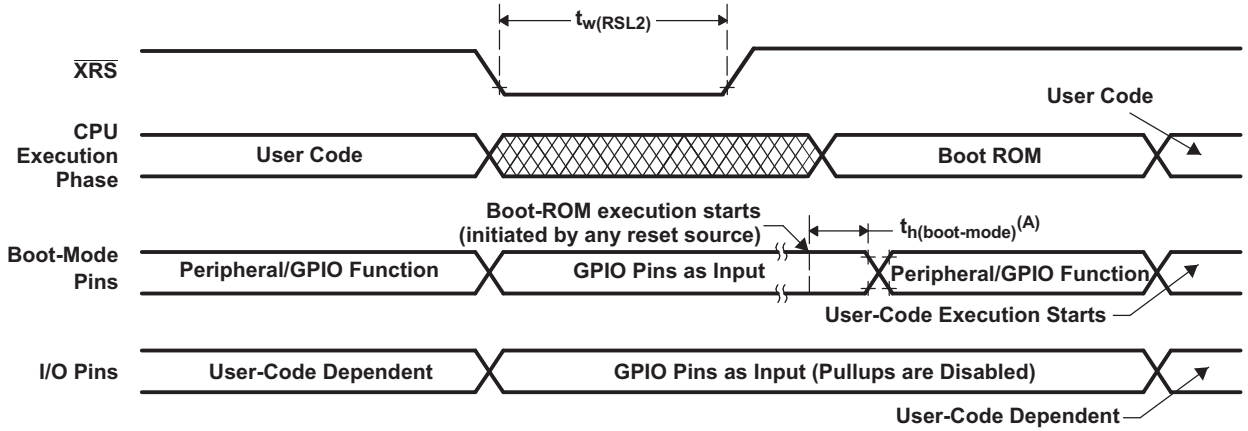
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A. The $\overline{XRS}$ pin can be driven externally by a supervisor or an external pullup resistor, see Table 3-1. On-chip POR logic will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see Section 4.7.2.1), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 4-6. Power-on Reset



A. After reset from any source (see Section 4.7.2.1), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 4-7. Warm Reset

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4.7.3 Clock Specifications

4.7.3.1 Clock Sources

表 4-6 lists four possible clock sources. 図 4-8 provides an overview of the device's clocking system.

表 4-6. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1	Can be used to provide clock for: • Watchdog block • Main PLL • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.
AUXCLKIN	Can be used to provide clock for: • Auxiliary PLL • CPU-Timer 2	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

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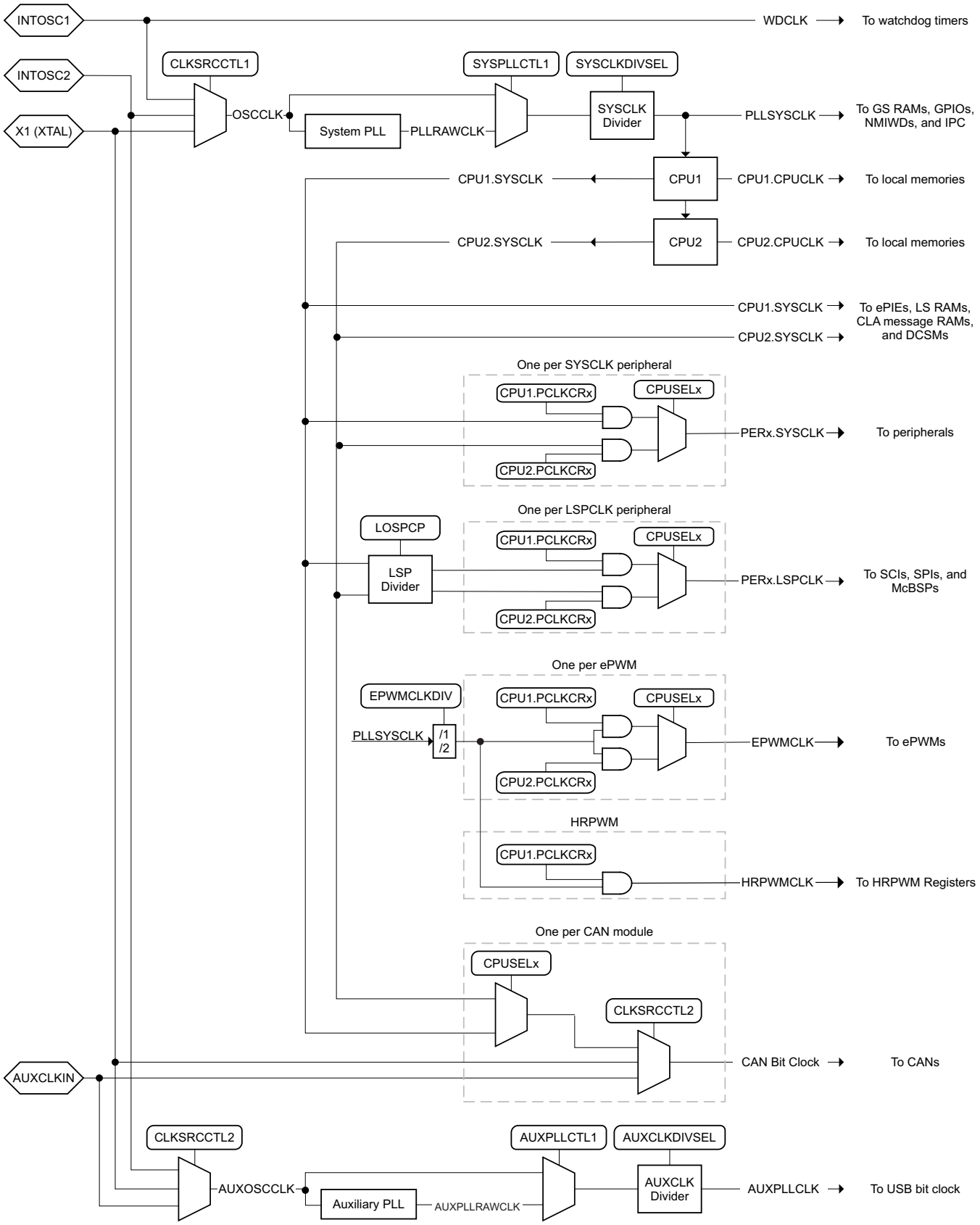


図 4-8. Clocking System

4.7.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

4.7.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

表 4-7 shows the frequency requirements for the input clocks. 表 4-16 shows the crystal equivalent series resistance requirements. 表 4-8 shows the X1 input level characteristics when using an external clock source. 表 4-9 and 表 4-10 show the timing requirements for the input clocks. 表 4-11 shows the PLL lock times for the Main PLL and the USB PLL.

表 4-7. Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator ***(PLL enabled)***	2	25	MHz
	Frequency, X1, from external oscillator ***(PLL disabled)***	2	100	MHz
$f_{(AUXI)}$	Frequency, AUXCLKIN, from external oscillator	2	60	MHz

表 4-8. X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3	0.3 * V_{DDIO}	V
X1 V_{IH}	Valid high-level input voltage	0.7 * V_{DDIO}	V_{DDIO} + 0.3	V

表 4-9. X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

表 4-10. AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(AUXI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(AUXI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(AUXL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(AUXH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

表 4-11. PLL Lock Times

		MIN	NOM	MAX	UNIT
$t_{(PLL)}$	Lock time, Main PLL (X1, from external oscillator)		50 µs + 2500 * $t_{c(OSCCLK)}$ (1)		µs
$t_{(USB)}$	Lock time, USB PLL (AUXCLKIN, from external oscillator)		50 µs + 2500 * $t_{c(OSCCLK)}$ (1)		µs

(1) The PLL lock time here includes the two required PLL lock sequences. Cycle count includes code execution of the PLL initialization routine, which could vary depending on compiler optimizations and flash wait states.

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4.7.3.2.2 Internal Clock Frequencies

表 4-12 provides the clock frequencies for the internal clocks.

表 4-12. Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		200(1)	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	5(1)		500	ns
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	120		400	MHz
$f_{(AUXPLLRAWCLK)}$	Frequency, auxiliary PLL output (before AUXCLK divider)	120		400	MHz
$f_{(AUXPLL)}$	Frequency, AUXPLLCLK	2	60	60	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200(1)	MHz
$f_{(LSP)}$	Frequency, LSPCLK(2)	2		200(1)	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	5(1)		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)	See respective clock			MHz
$f_{(EPWM)}$	Frequency, EPWMCLK(3)			100	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		100	MHz

(1) Using an external clock source. If INTOSC1 or INTOSC2 is used as the clock source, then the maximum frequency is 194 MHz and the minimum period is 5.15 ns.
(2) Lower LSPCLK will reduce device power consumption. The default at reset is SYSCLK/4.
(3) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

4.7.3.2.3 Output Clock Frequency and Switching Characteristics

表 4-13 provides the frequency of the output clock. 表 4-14 shows the switching characteristics of the output clock, XCLKOUT.

表 4-13. Output Clock Frequency

		MIN	MAX	UNIT
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

表 4-14. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1)(2)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

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4.7.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, multiple external clock source options are available. 図 4-9 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 (also referred to as XTAL) and AUXCLKIN.

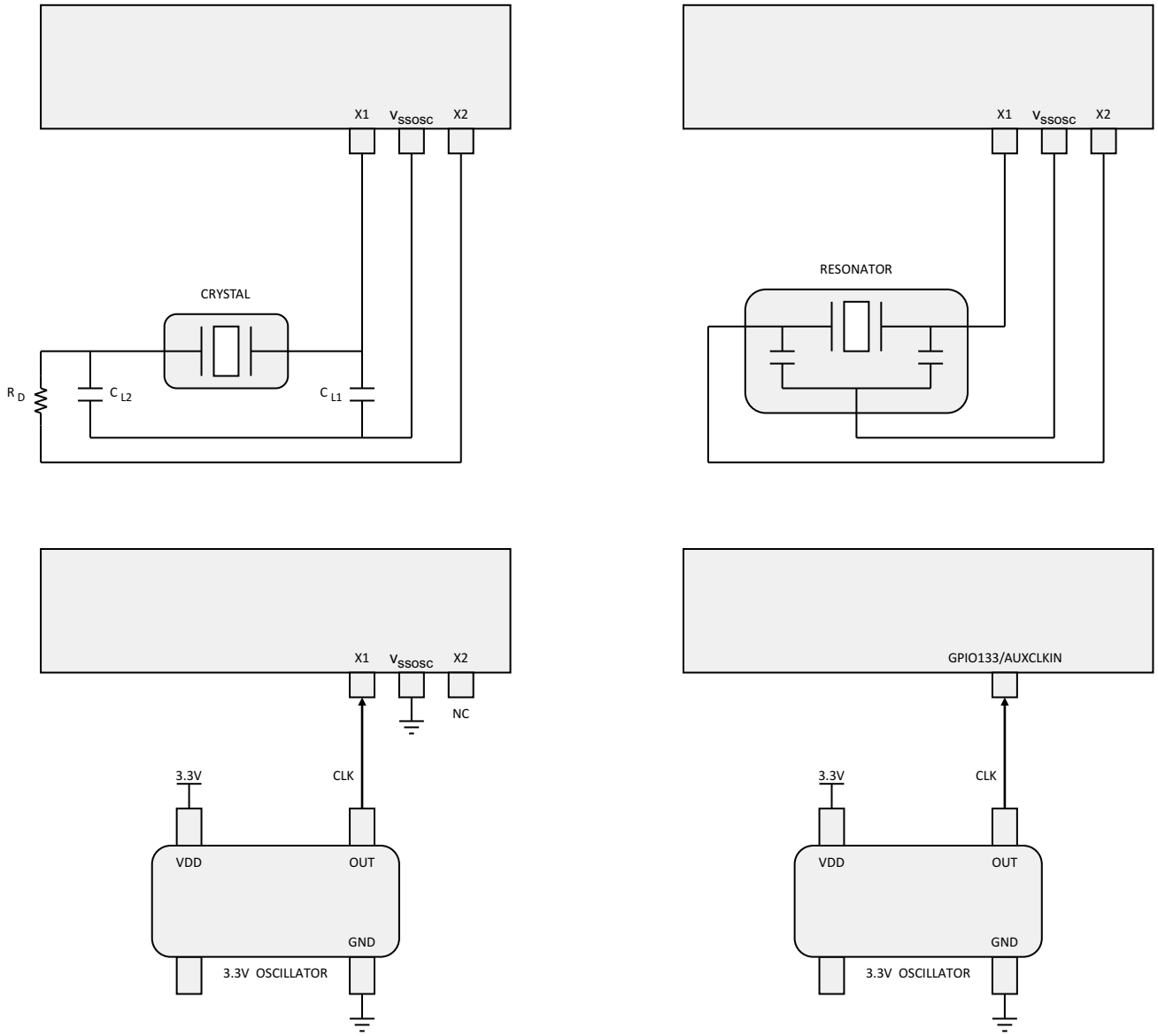


図 4-9. Connecting Input Clocks to a 2837xD Device

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4.7.3.4 Crystal Oscillator

When using a quartz crystal, it may be necessary to include a damping resistor (R_D) in the crystal circuit to prevent over-driving the crystal (drive level can be found in the crystal data sheet). In higher-frequency applications (10 MHz or greater), R_D is generally not required. If a damping resistor is required, R_D should be as small as possible because the size of the resistance affects start-up time (smaller R_D = faster start-up time). TI recommends that the crystal manufacturer characterize the crystal with the application board. 表 4-15 shows the crystal oscillator parameters. 表 4-16 shows the crystal equivalent series resistance (ESR) requirements. 表 4-17 shows the crystal oscillator electrical characteristics.

表 4-15. Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

表 4-16. Crystal Equivalent Series Resistance (ESR) Requirements(1)(2)

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

(1) Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
(2) ESR = Negative Resistance/3

表 4-17. Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 20 MHz ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)				1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

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4.7.3.5 Internal Oscillators

To reduce production board costs and application development time, the F28377D contains two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, both oscillators are enabled at power up. INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source. INTOSC1 can also be manually configured as the system reference clock (OSCCLK). 表 4-18 provides the electrical characteristics of the internal oscillators to determine if this module meets the clocking requirements of the application.

表 4-18 provides the electrical characteristics of the two internal oscillators.

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This oscillator cannot be used as the PLL source if the PLLSYSCLK is configured to frequencies above 194 MHz.

表 4-18. Internal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(INTOSC)}$	Frequency, INTOSC1 and INTOSC2		9.7	10.0	10.3	MHz
$f_{(INTOSC-STABILITY)}$	Frequency stability at room temperature	30ºC, Nominal V_{DD}		±0.1%		
	Frequency stability over V_{DD}	30ºC		±0.2%		
	Frequency stability		–3.0%		3.0%	
$f_{(INTOSC-ST)}$	Start-up and settling time				20	µs

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4.7.4 Flash Parameters

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 128-bit-wide prefetch reads and a pipeline buffer. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM. This flash efficiency lets designers realize a 2× improvement in performance when migrating from the previous generation Delfino MCUs.

This device also has an OTP (One-Time-Programmable) sector used for the dual code security module (DCSM), which cannot be erased after it is programmed.

表 4-19 shows the minimum required flash wait states at different frequencies. 表 4-20 shows the flash parameters.

表 4-19. Flash Wait States

CPUCLK (MHz)		MINIMUM WAIT STATES (1)
EXTERNAL OSCILLATOR OR CRYSTAL	INTOSC1 OR INTOSC2	
150 < CPUCLK ≤ 200	145 < CPUCLK ≤ 194	3
100 < CPUCLK ≤ 150	97 < CPUCLK ≤ 145	2
50 < CPUCLK ≤ 100	48 < CPUCLK ≤ 97	1
CPUCLK ≤ 50	CPUCLK ≤ 48	0

(1) Minimum required FRDCNTL[RWAIT].

表 4-20. Flash Parameters

PARAMETER			MIN	TYP	MAX	UNIT
	Program Time(1)	128 data bits + 16 ECC bits		40	300	µs
		8KW sector		90	180	ms
		32KW sector		360	720	ms
	Erase Time(2) at < 25 cycles	8KW sector		25	50	ms
		32KW sector		30	55	
	Erase Time(2) at 50k cycles	8KW sector		105	4000	ms
		32KW sector		110	4000	
N_{wec}	Write/erase cycles				20000	cycles
$t_{retention}$	Data retention duration at T_J = 85°C		20			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the emulator used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

注

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle. For more details, see the "Flash: Minimum Programming Word Size" advisory in the *TMS320F2837xD Dual-Core Delfino™ MCUs Silicon Errata*.

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4.7.5 Emulation/JTAG

The JTAG port has five dedicated pins: $\overline{\text{TRST}}$, TMS, TDI, TDO, and TCK. The $\overline{\text{TRST}}$ signal should always be pulled down through a 2.2-kΩ pulldown resistor on the board. This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

See 図 4-10 to see how the 14-pin JTAG header connects to the MCU's JTAG port signals. 図 4-11 shows how to connect to the 20-pin header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

The PD (Power Detect) terminal of the emulator header should be connected to the board 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the emulator). Header terminal $\overline{\text{RESET}}$ is an open-drain output from the emulator header that enables board components to be reset through emulator commands (available only through the 20-pin header).

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 in (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most emulator operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints for C28x in CCS.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

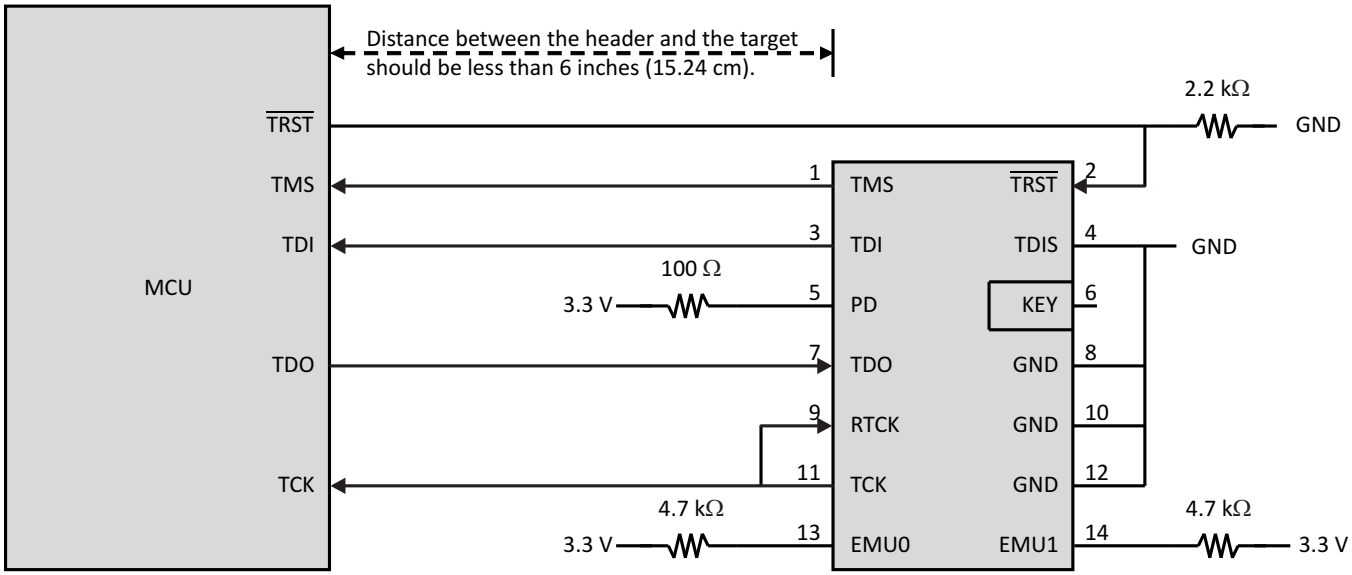


図 4-10. Connecting to the 14-Pin JTAG Header

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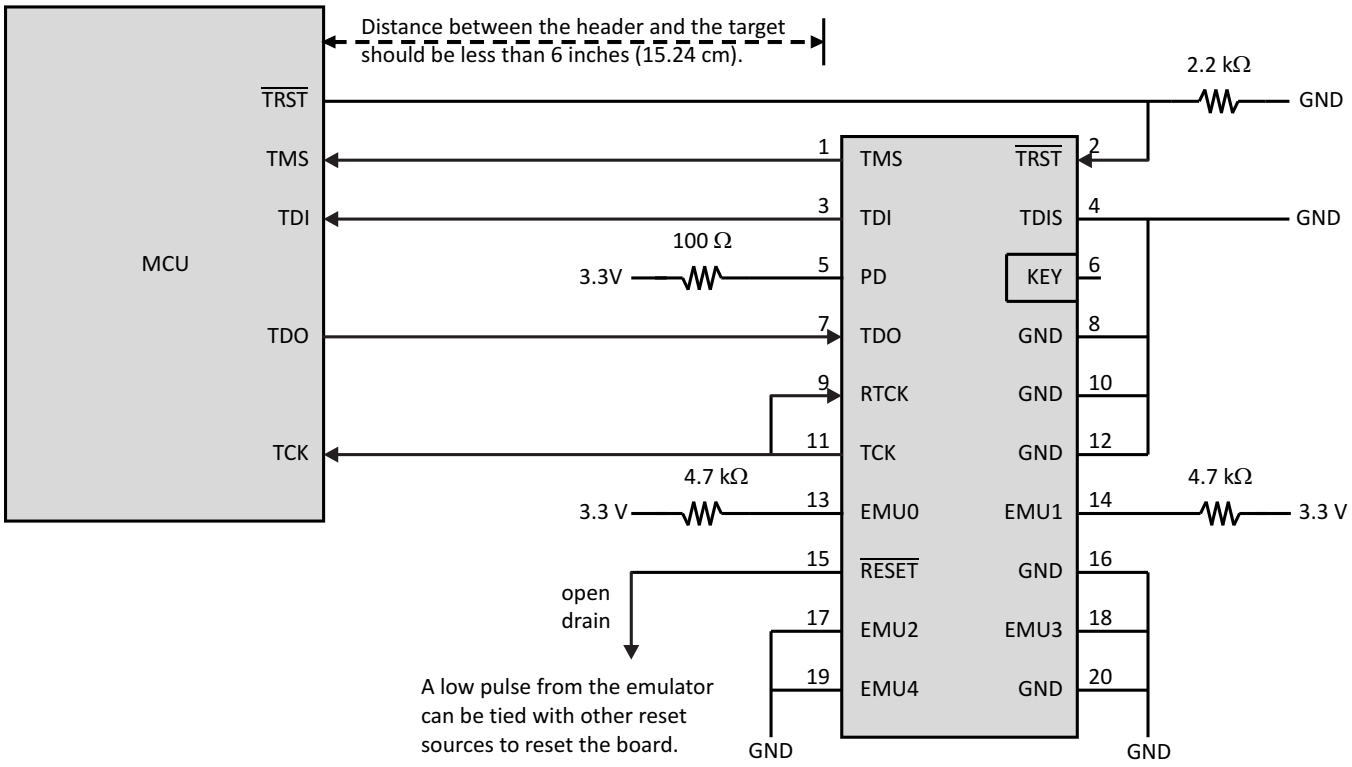


図 4-11. Connecting to the 20-Pin JTAG Header

4.7.5.1 JTAG Electrical Data and Timing

表 4-21 lists the JTAG timing requirements. 表 4-22 lists the JTAG switching characteristics. 図 4-12 shows the JTAG timing.

表 4-21. JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	13		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	13		ns
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		ns

表 4-22. JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	25	ns

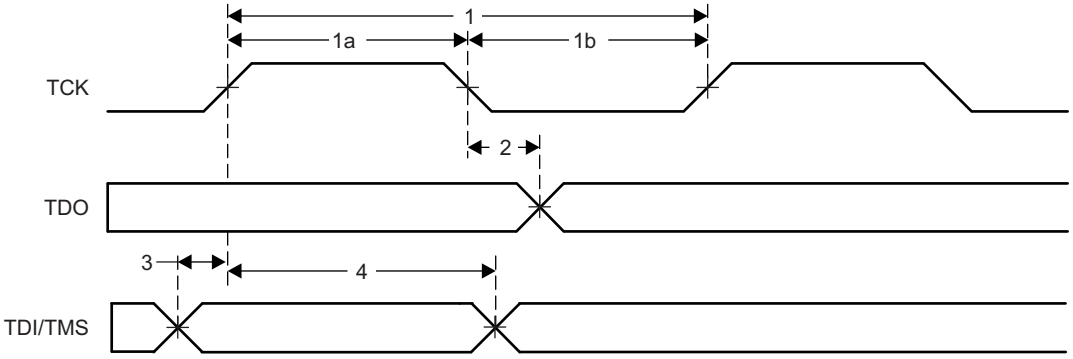


図 4-12. JTAG Timing

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4.7.6 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADC(s), eCAP(s), ePWM(s), and external interrupts. For more details, see the X-BAR chapter in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

4.7.6.1 GPIO - Output Timing

Table 4-23 shows the general-purpose output switching characteristics. Figure 4-13 shows the general-purpose output timing.

Table 4-23. General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8(1)	ns
t_{fGPO}	Toggling frequency, GPO pins			25	MHz

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

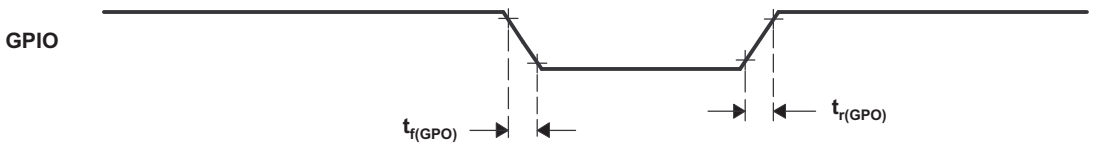


Figure 4-13. General-Purpose Output Timing

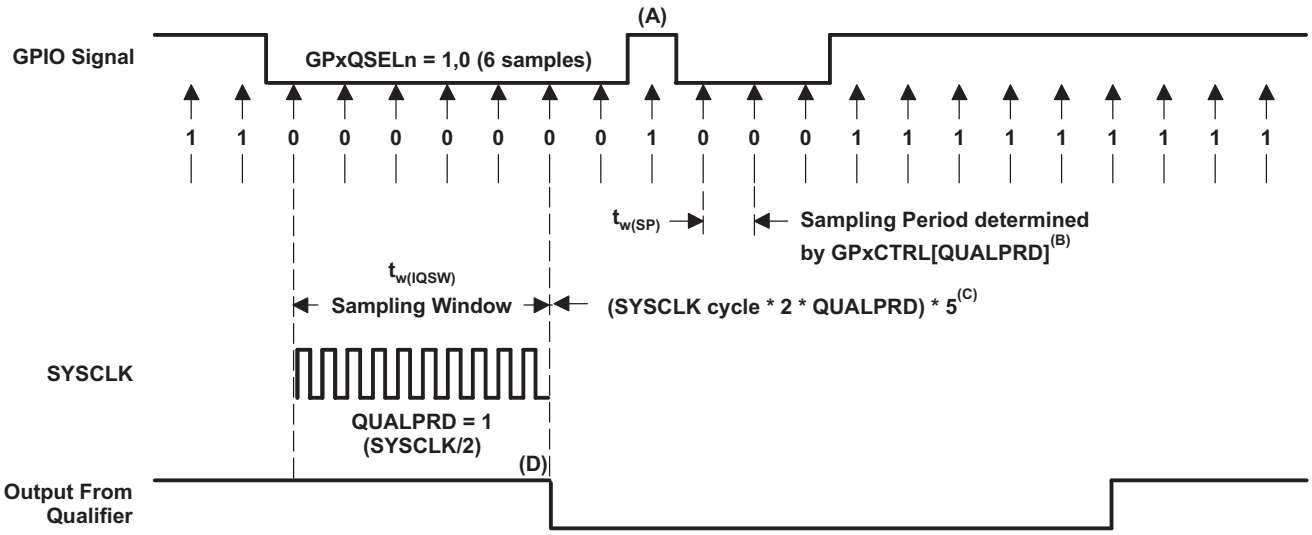
4.7.6.2 GPIO - Input Timing

Table 4-24 shows the general-purpose input timing requirements. Figure 4-14 shows the sampling mode.

Table 4-24. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).

B. The qualification period selected through the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 4-14. Sampling Mode

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4.7.6.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0 (1)

Sampling frequency = SYSCLK, if QUALPRD = 0 (2)

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0 (3)

In Equation 1, Equation 2, and Equation 3, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

Figure 4-15 shows the general-purpose input timing.

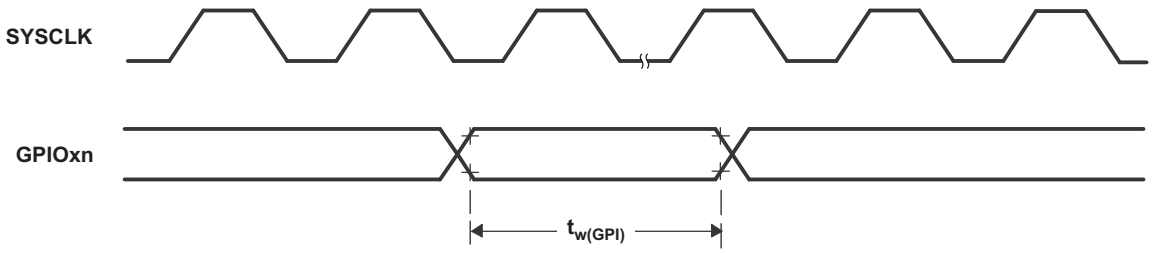


Figure 4-15. General-Purpose Input Timing

4.7.7 Interrupts

図 4-16 provides a high-level view of the interrupt architecture.

As shown in 図 4-16, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, 16 ePIE block interrupts are grouped into 1 CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

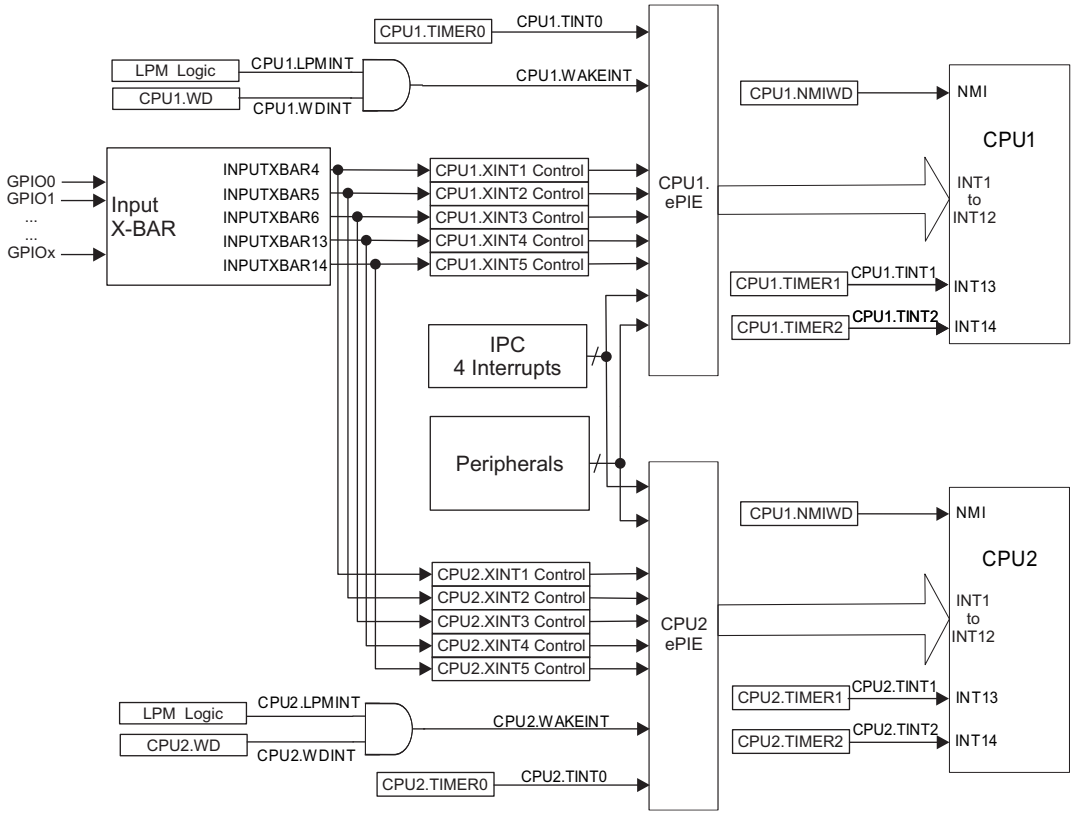


図 4-16. External and ePIE Interrupt Sources

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4.7.7.1 External Interrupt (XINT) Electrical Data and Timing

Table 4-25 lists the external interrupt timing requirements. Table 4-26 lists the external interrupt switching characteristics. Figure 4-17 shows the external interrupt timing.

Table 4-25. External Interrupt Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.

Table 4-26. External Interrupt Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch(2)	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.
(2) This assumes that the ISR is in a single-cycle memory.

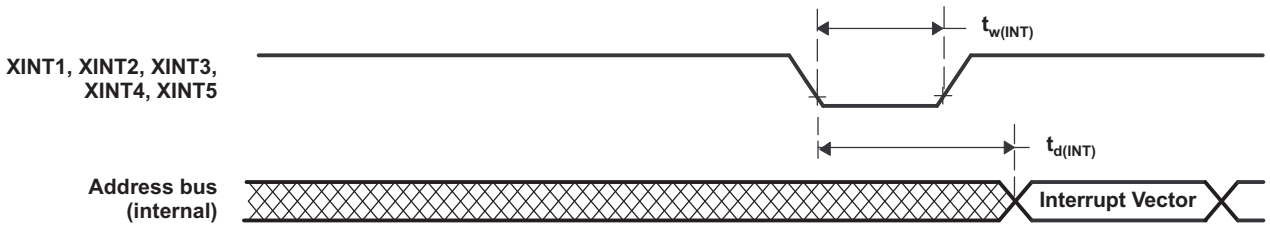


Figure 4-17. External Interrupt Timing

4.7.8 Low-Power Modes

This device has three clock-gating low-power modes and a special power-gating mode.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low Power Modes section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

4.7.8.1 Clock-Gating Low-Power Modes

IDLE, STANDBY, and HALT modes on this device are similar to those on other C28x devices. 表 4-27 describes the effect on the system when any of the clock-gating low-power modes are entered.

表 4-27. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	CPU1 IDLE	CPU1 STANDBY	CPU2 IDLE	CPU2 STANDBY	HALT
CPU1.CLKIN	Active	Gated	N/A	N/A	Gated
CPU1.SYSCLK	Active	Gated	N/A	N/A	Gated
CPU1.CPUCLK	Gated	Gated	N/A	N/A	Gated
CPU2.CLKIN	N/A	N/A	Active	Gated	Gated
CPU2.SYSCLK	N/A	N/A	Active	Gated	Gated
CPU2.CPUCLK	N/A	N/A	Gated	Gated	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Gated if CPUSEL.PERx = CPU1	Active	Gated if CPUSEL.PERx = CPU2	Gated
CPU1.WDCLK	Active	Active	N/A	N/A	Gated if CLKSRCCTL1.WDHALTI = 0
CPU2.WDCLK	N/A	N/A	Active	Active	Gated
AUXPLLCLK	Active	Active	Active	Active	Gated
PLL	Powered	Powered	Powered	Powered	Software must power down PLL before entering HALT
INTOSC1	Powered	Powered	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash	Powered	Powered	Powered	Powered	Software-Controlled
X1/X2 Crystal Oscillator	Powered	Powered	Powered	Powered	Powered-Down

4.7.8.2 Power-Gating Low-Power Modes

HIBERNATE mode is the lowest power mode on this device. It is a global low-power mode that gates the supply voltages to most of the system. HIBERNATE is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. 表 4-28 describes the effects on the system when the HIBERNATE mode is entered.

表 4-28. Effect of Power-Gating Low-Power Mode on the Device

MODULES/POWER DOMAINS	HIBERNATE
M0 and M1 memories	• Remain on with memory retention if LPMCR.M0M1MODE = 0x00 • Are off when LPMCR.M0M1MODE = 0x01
CPU1, CPU2 digital peripherals	Powered down
Dx, LSx, GSx memories	Power down, memory contents are lost
I/Os	On with output state preserved
Oscillators, PLL, analog peripherals, Flash	Enters Low-Power Mode

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4.7.8.3 Low-Power Mode Wakeup Timing

表 4-29 shows the IDLE mode timing requirements, 表 4-30 shows the switching characteristics, and 図 4-18 shows the timing diagram for IDLE mode.

表 4-29. IDLE Mode Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

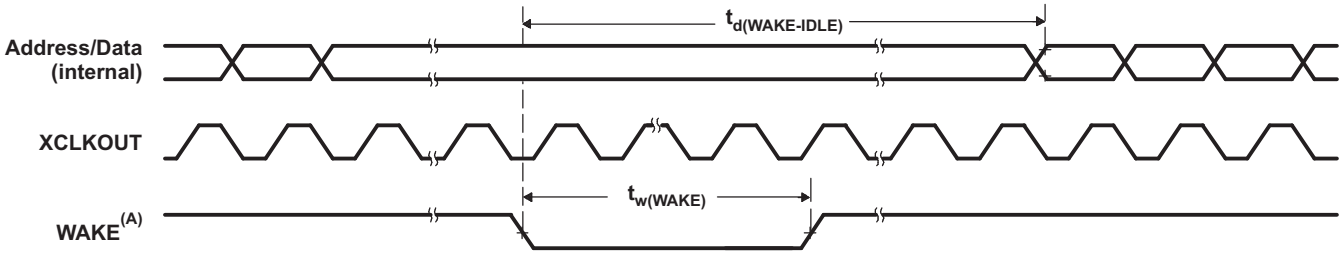
(1) For an explanation of the input qualifier parameters, see Table 4-24.

表 4-30. IDLE Mode Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)				cycles
	• Wakeup from Flash – Flash module in active state	Without input qualifier		$40t_{c(SYSCLK)}$	
		With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	
	• Wakeup from Flash – Flash module in sleep state	Without input qualifier		$6700t_{c(SYSCLK)}$ (3)	
		With input qualifier		$6700t_{c(SYSCLK)}$ (3) $+ t_{w(WAKE)}$	
	• Wakeup from RAM	Without input qualifier		$25t_{c(SYSCLK)}$	
		With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	

(1) For an explanation of the input qualifier parameters, see Table 4-24.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(3) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or $\overline{\text{XRS}}$. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

図 4-18. IDLE Entry and Exit Timing Diagram

表 4-31 shows the STANDBY mode timing requirements, 表 4-32 shows the switching characteristics, and 図 4-19 shows the timing diagram for STANDBY mode.

表 4-31. STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | $(2 + QUALSTDBY)t_{c(OSCCLK)}$ (1)	$(2 + QUALSTDBY) * t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

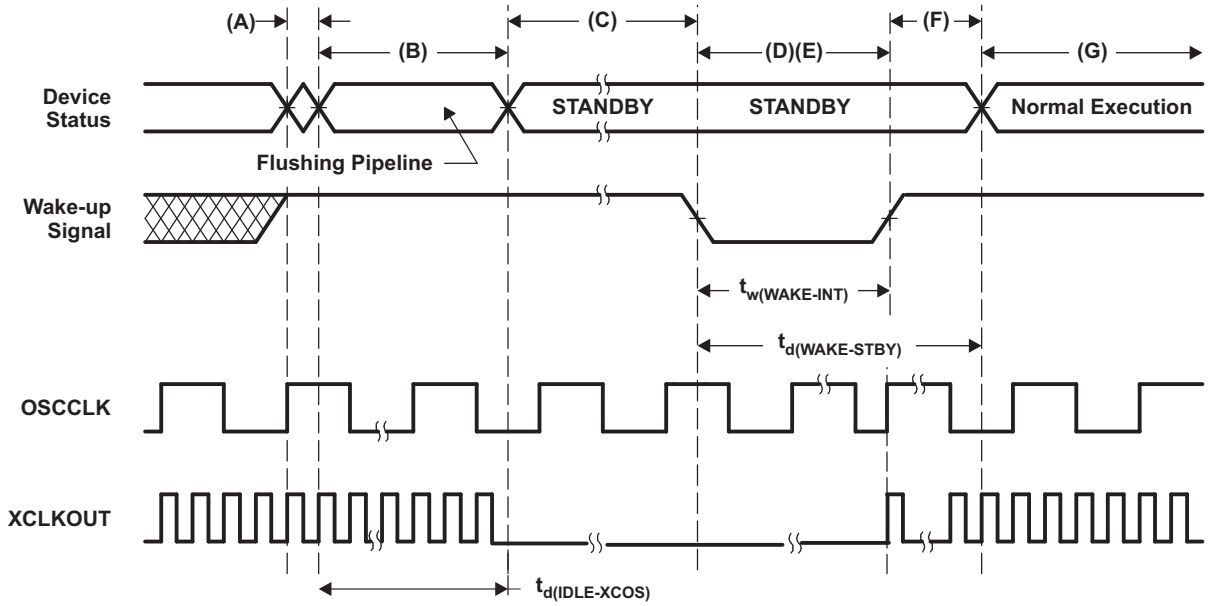
表 4-32. STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume (1)				cycles
	• Wakeup from flash – Flash module in active state			$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	
	• Wakeup from flash – Flash module in sleep state			$6700t_{c(SYSCLK)}$ (2) $+ t_{w(WAKE-INT)}$	
	• Wakeup from RAM			$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

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A. IDLE instruction is executed to put the device into STANDBY mode.

B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. The external wake-up signal is driven active.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.

F. After a latency period, the STANDBY mode is exited.

G. Normal execution resumes. The device will respond to the interrupt (if enabled).

図 4-19. STANDBY Entry and Exit Timing Diagram

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表 4-33 shows the HALT mode timing requirements, 表 4-34 shows the switching characteristics, and 図 4-20 shows the timing diagram for HALT mode.

表 4-33. HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal(1)	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal(1)	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See 表 4-17 for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see 4.7.3.5 for t_{oscst}. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

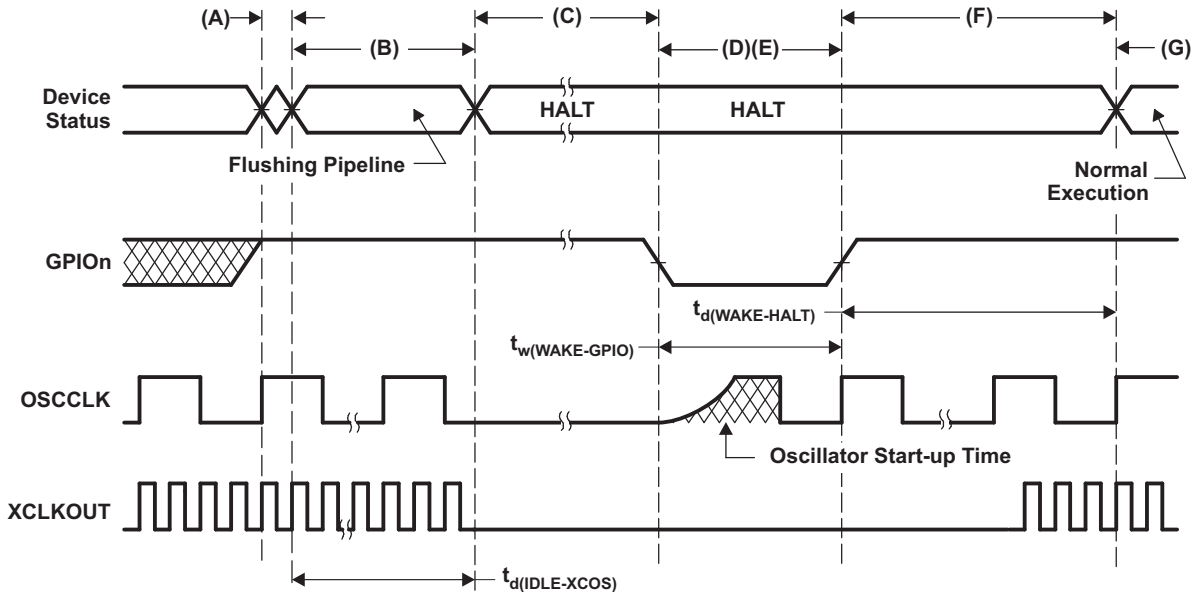
表 4-34. HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	• Wakeup from flash – Flash module in active state		$75t_{c(OSCCLK)}$	
	• Wakeup from flash – Flash module in sleep state		$17500t_{c(OSCCLK)}$ (1)	
	• Wakeup from RAM		$75t_{c(OSCCLK)}$	

(1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

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A. IDLE instruction is executed to put the device into HALT mode.

B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing a 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wakeup sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.

G. Normal operation resumes.

H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

図 4-20. HALT Entry and Exit Timing Diagram

注

CPU2 should enter IDLE mode before CPU1 puts the device into HALT mode. CPU1 should verify that CPU2 has entered IDLE mode using the LPMSTAT register before calling the IDLE instruction to enter HALT.

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表 4-35 shows the HIBERNATE mode timing requirements, 表 4-36 shows the switching characteristics, and 図 4-21 shows the timing diagram for HIBERNATE mode.

表 4-35. HIBERNATE Mode Timing Requirements

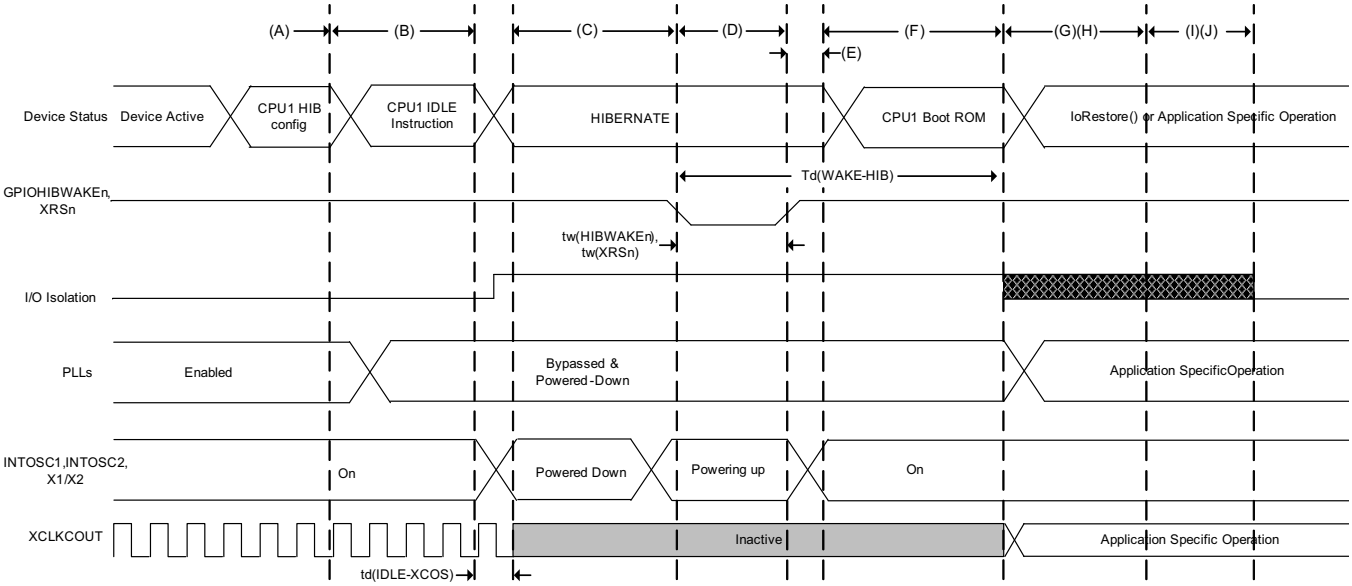
		MIN	MAX	UNIT
$t_{w(HIBWAKE)}$	Pulse duration, $\overline{HIBWAKE}$ signal	40		µs
$t_{w(WAKEXRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal	40		µs

表 4-36. HIBERNATE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$30t_{c(SYSCLK)}$	cycles
$t_{d(WAKE-HIB)}$	Delay time, external wake signal to IORestore function start		1.5	ms

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A. CPU1 does necessary application-specific context save to M0/M1 memories if required. This includes GPIO state if using I/O Isolation. Configures the LPMCR register of CPU1 for HIBERNATE mode. Powers down Flash Pump/Bank, USB-PHY, CMPSS, DAC, and ADC using their register configurations. The application should also power down the PLL and peripheral clocks before entering HIBERNATE. In dual-core applications, CPU1 should confirm that CPU2 has entered IDLE/STANDBY using the LPMSTAT register.

B. IDLE instruction is executed to put the device into HIBERNATE mode.

C. The device is now in HIBERNATE mode. If configured, I/O isolation is turned on, M0 and M1 memories are retained. CPU1 and CPU2 are powered down. Digital peripherals are powered down. The oscillators, PLLs, analog peripherals, and Flash are in their software-controlled Low-Power modes. Dx, LSx, and GSx memories are also powered down, and their memory contents lost.

D. A falling edge on the GPIOHIBWAKEn pin will drive the wakeup of the devices clock sources INTOSC1, INTOSC2, and X1/X2 OSC. The wakeup source must keep the GPIOHIBWAKEn pin low long enough to ensure full power-up of these clock sources.

E. After the clock sources are powered up, the GPIOHIBWAKEn must be driven high to trigger the wakeup sequence of the remainder of the device.

F. The BootROM will then begin to execute. The BootROM can distinguish a HIBERNATE wakeup by reading the CPU1.REC.HIBRESETn bit. After the TI OTP trims are loaded, the BootROM code will branch to the user-defined IoRestore function if it has been configured.

G. At this point, the device is out of HIBERNATE mode, and the application may continue.

H. The IoRestore function is a user-defined function where the application may reconfigure GPIO states, disable I/O isolation, reconfigure the PLL, restore peripheral configurations, or branch to application code. This is up to the application requirements.

I. If the application has not branched to application code, the BootROM will continue after completing IoRestore. It will disable I/O isolation automatically if it was not taken care of inside of IoRestore. CPU2 will be brought out of reset at this point as well.

J. BootROM will then boot as determined by the HIBBOOTMODE register. Refer to the ROM Code and Peripheral Booting chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for more information.

図 4-21. HIBERNATE Entry and Exit Timing Diagram

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1. If the IORESTOREADDR is configured as the default value, the BootROM will continue its execution to boot as determined by the HIBBOOTMODE register. Refer to the ROM Code and Peripheral Booting chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for more information.
2. The user may choose to disable I/O Isolation at any point in the IoRestore function. Regardless if the user has disabled Isolation in the IoRestore function or if IoRestore is not defined, the BootROM will automatically disable isolation before booting as determined by the HIBBOOTMODE register.

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For applications using both CPU1 and CPU2, TI recommends that the application puts CPU2 in either IDLE or STANDBY before entering HIBERNATE mode. If any GPIOs are used and the state is to be preserved, data can be stored in M0/M1 memory of CPU1 to be reconfigured upon wakeup. This should be done before step A of 図 4-21.

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4.7.9 External Memory Interface (EMIF)

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

4.7.9.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects (EMIF_CS[4:2]). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable time-out
- Select strobe option

4.7.9.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select (EMIF_CS[0]).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in controlSUITE™ (CONTROLSUITE) and the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with 8-, 9-, 10-, and 11-column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. The EMIF module does not support mobile SDRAM devices.

On this device, the EMIF does not support burst access for SDRAM configurations. This means every access to an external SDRAM device will have CAS latency.

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4.7.9.3 EMIF Electrical Data and Timing

4.7.9.3.1 Asynchronous RAM

Table 4-37 shows the EMIF asynchronous memory timing requirements. Table 4-38 shows the EMIF asynchronous memory switching characteristics. Figure 4-22 through Figure 4-25 show the EMIF asynchronous memory timing diagrams.

Table 4-37. EMIF Asynchronous Memory Timing Requirements(1)

NO.			MIN	MAX	UNIT
Reads and Writes					
	E	EMIF clock period	$t_{c(SYSCLK)}$		ns
2	$t_{w(EM_WAIT)}$	Pulse duration, EMxWAIT assertion and deassertion	2E		ns
Reads					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMxD[y:0] valid before $\overline{EMxOE}$ high	15		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMxD[y:0] valid after $\overline{EMxOE}$ high	0		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20		ns
Writes					
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20		ns

(1) E = EMxCLK period in ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. Figure 4-23 and Figure 4-25 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 4-38. EMIF Asynchronous Memory Switching Characteristics(1)(2)(3)

NO.	PARAMETER		MIN	MAX	UNIT
Reads and Writes					
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E–3	(TA)*E+2	ns
Reads					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH+2)*E–3	(RS+RST+RH+2)*E+2	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+2+ (EWC*16))*E–3	(RS+RST+RH+2+ (EWC*16))*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxOE}$ low (SS = 0)	(RS)*E–3	(RS)*E+2	ns
		Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxOE}$ low (SS = 1)	–3	2	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 0)	(RH)*E–3	(RH)*E	ns
		Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 1)	–3	0	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxBA[y:0] invalid	(RH)*E–3	(RH)*E	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–4], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for more information.
(2) E = EMxCLK period in ns.
(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256–1]. The maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for more information.

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Table 4-38. EMIF Asynchronous Memory Switching Characteristics[1][2][3] (continued)

NO.	PARAMETER		MIN	MAX	UNIT
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxA[y:0] invalid	(RH)*E–3	(RH)*E	ns
10	$t_{w(EMOEL)}$	$\overline{EMxOE}$ active low width (EW = 0)	(RST)*E–1	(RST)*E+1	ns
		$\overline{EMxOE}$ active low width (EW = 1)	(RST+(EWC*16))*E–1	(RST+(EWC*16))*E+1	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxOE}$ high	4E+10	5E+15	ns
29	$t_{su(EMDQMV-EMOEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
30	$t_{h(EMOEH-EMDQMIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxDQM[y:0] invalid	(RH)*E–3	(RH)*E	ns
Writes					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH+2)*E–3	(WS+WST+WH+2)*E+1	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+2+(EWC*16))*E–3	(WS+WST+WH+2+(EWC*16))*E+1	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxWE}$ low (SS = 0)	(WS)*E–3	(WS)*E+1	ns
		Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxWE}$ low (SS = 1)	–3	1	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 0)	(WH)*E–3	(WH)*E	ns
		Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 1)	–3	0	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxDQM[y:0] invalid	(WH)*E–3	(WH)*E	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxBA[y:0] invalid	(WH)*E–3	(WH)*E	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxA[y:0] invalid	(WH)*E–3	(WH)*E	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 0)	(WST)*E–1	(WST)*E+1	ns
		$\overline{EMxWE}$ active low width (EW = 1)	(WST+(EWC*16))*E–1	(WST+(EWC*16))*E+1	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxWE}$ high	4E+10	5E+15	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMxD[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxD[y:0] invalid	(WH)*E–3	(WH)*E	ns

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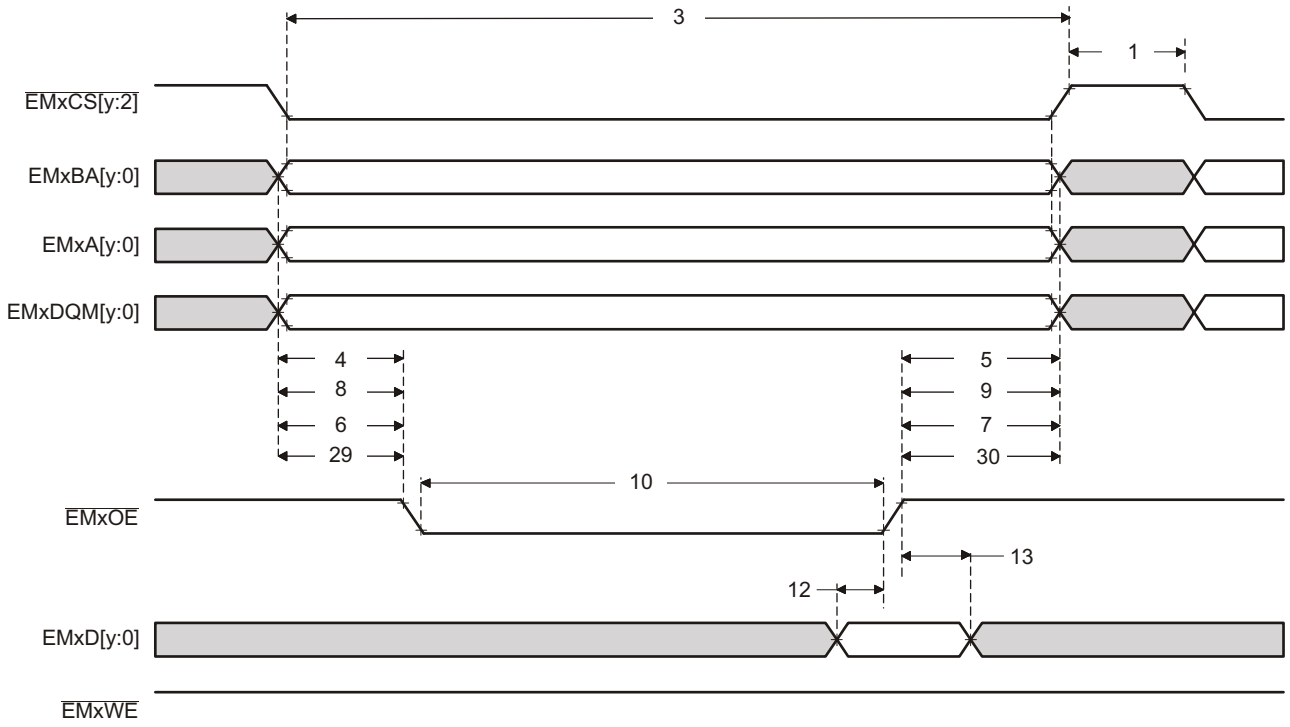


Figure 4-22. Asynchronous Memory Read Timing

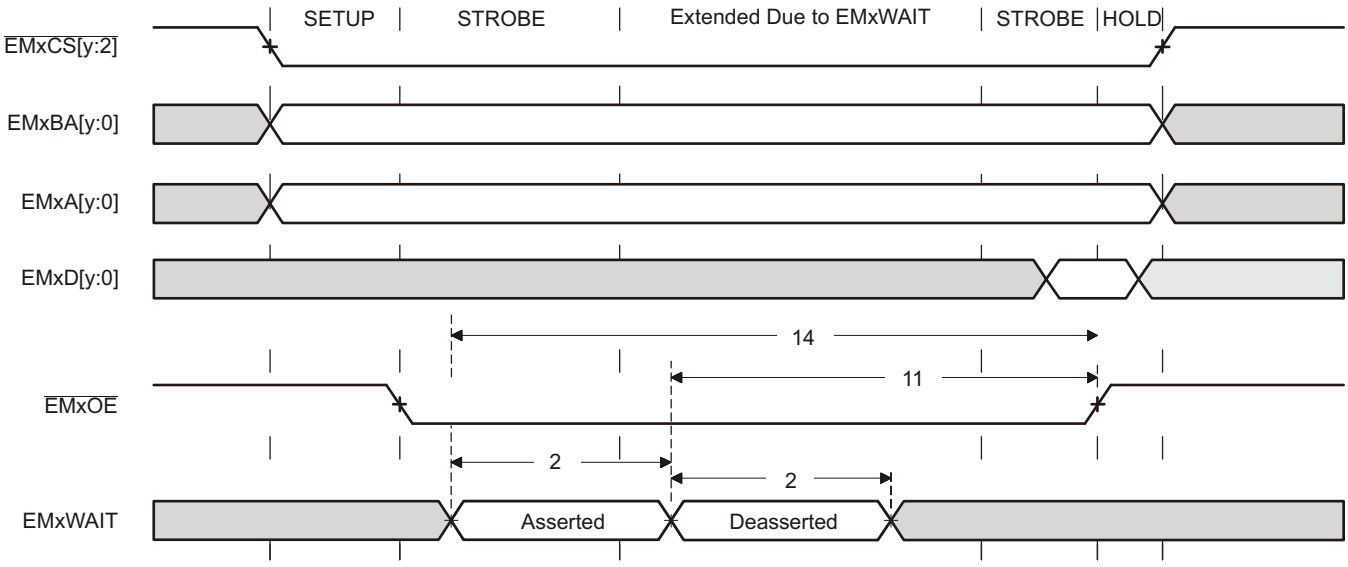


Figure 4-23. EMxWAIT Read Timing Requirements

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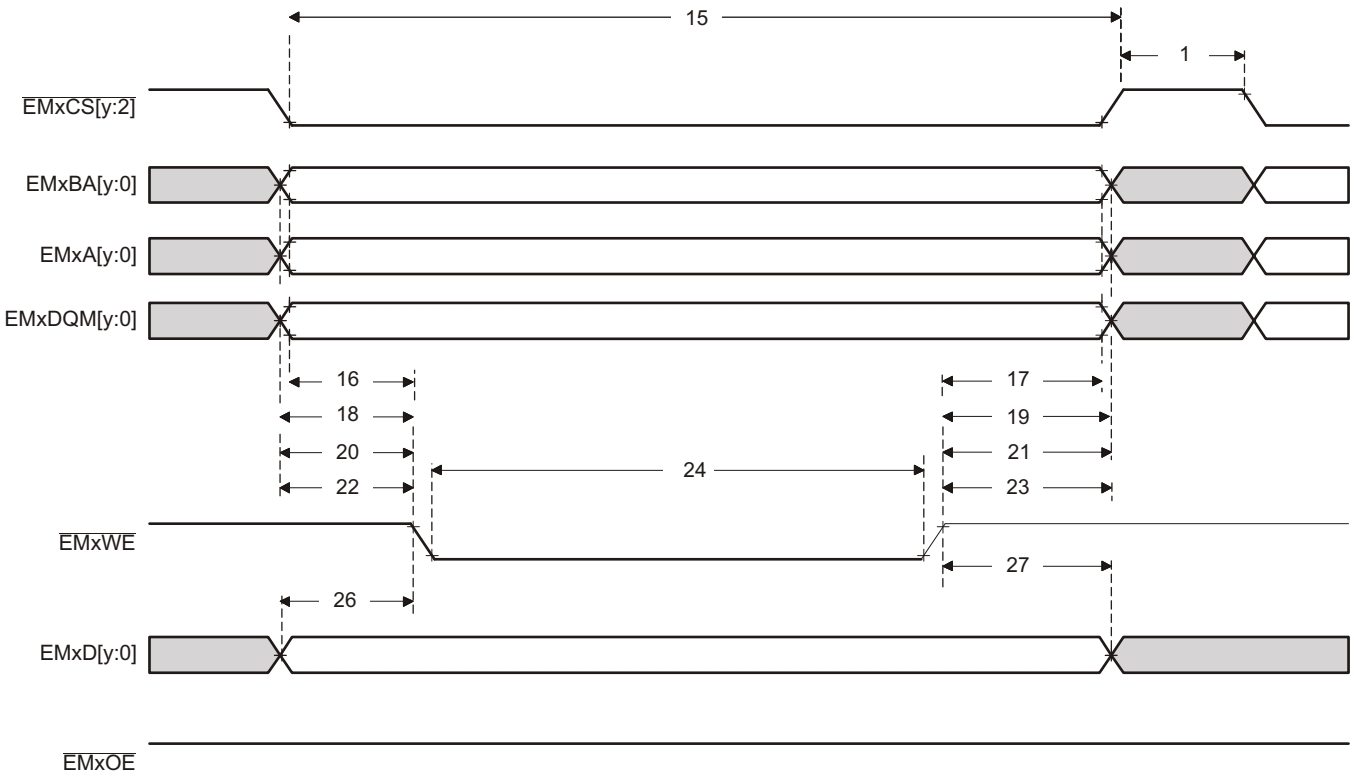


Figure 4-24. Asynchronous Memory Write Timing

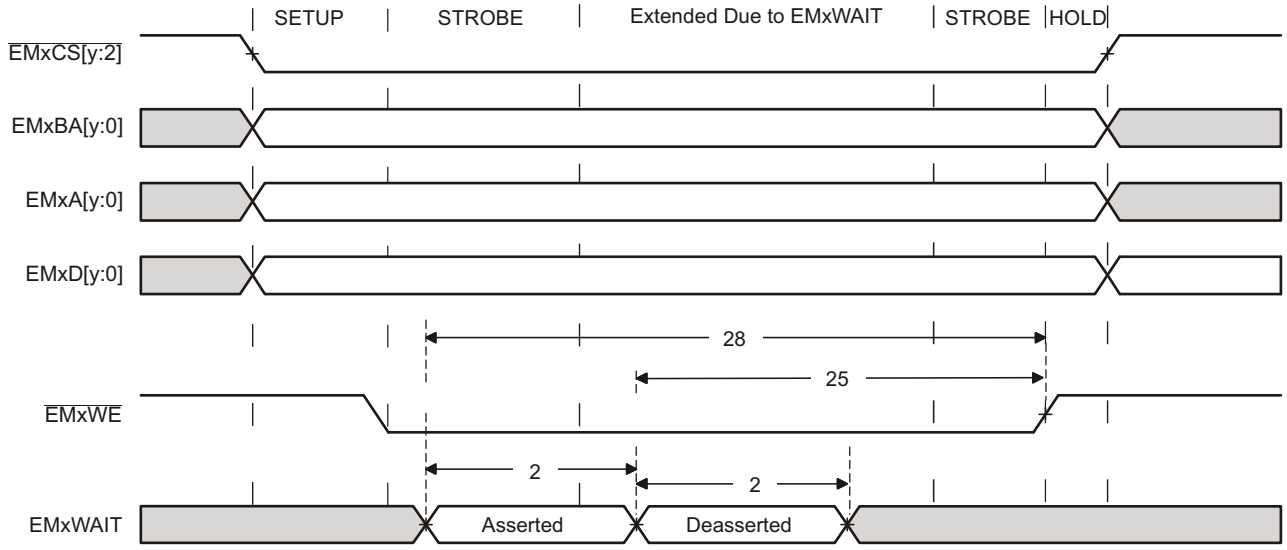


Figure 4-25. EMxWAIT Write Timing Requirements

4.7.9.3.2 Synchronous RAM

Table 4-39 shows the EMIF synchronous memory timing requirements. Table 4-40 shows the EMIF synchronous memory switching characteristics. Figure 4-26 and Figure 4-27 show the synchronous memory timing diagrams.

Table 4-39. EMIF Synchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EMIFDV-EM_CLKH)}$	Input setup time, read data valid on EMxD[y:0] before EMxCLK rising	2		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMxD[y:0] after EMxCLK rising	1.5		ns

Table 4-40. EMIF Synchronous Memory Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK	10		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMxCLK high or low	3		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ valid		8	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ invalid	1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMxCLK rising to EMxDQM[y:0] valid		8	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMxCLK rising to EMxDQM[y:0] invalid	1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid		8	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid	1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMxCLK rising to EMxD[y:0] valid		8	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMxCLK rising to EMxD[y:0] invalid	1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMxCLK rising to EMxRAS valid		8	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMxCLK rising to EMxRAS invalid	1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMxCLK rising to EMxCAS valid		8	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMxCLK rising to EMxCAS invalid	1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxWE}}$ valid		8	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxWE}}$ invalid	1		ns
17	$t_{d(CLKH-DHZ)}$	Delay time, EMxCLK rising to EMxD[y:0] tri-stated		8	ns
18	$t_{oh(CLKH-DLZ)}$	Output hold time, EMxCLK rising to EMxD[y:0] driving	1		ns

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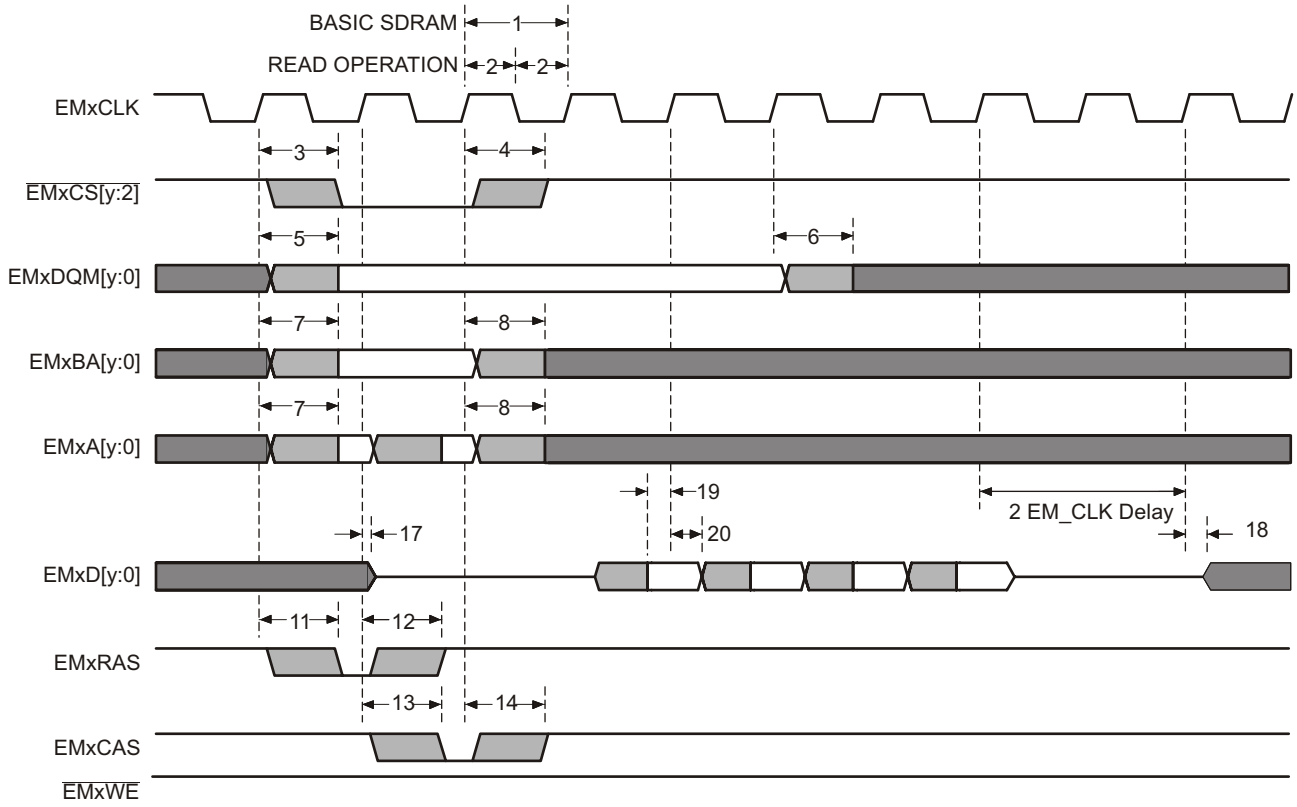


Figure 4-26. Basic SDRAM Read Operation

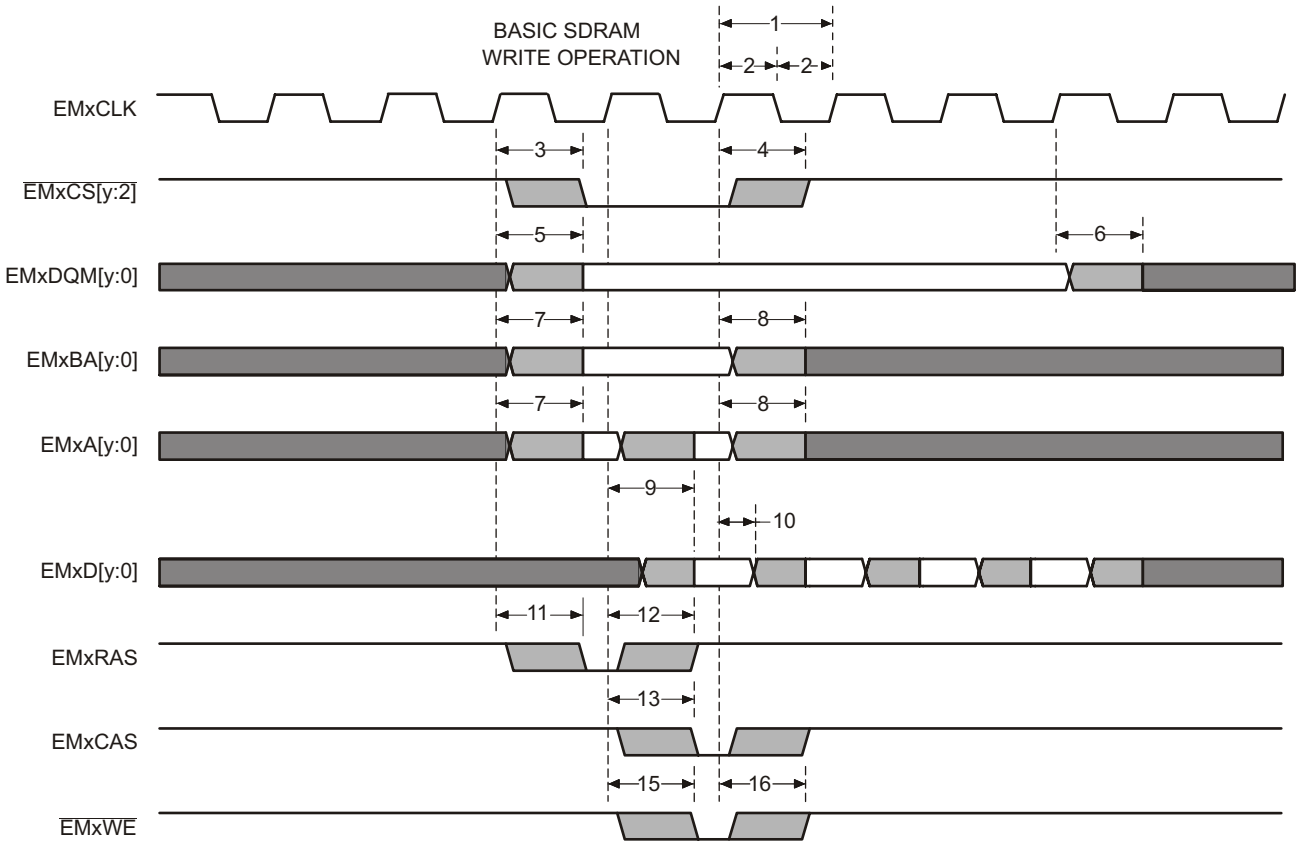


Figure 4-27. Basic SDRAM Write Operation

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4.8 Analog Peripherals

This analog subsystem module is described in this section.

The analog modules on this device include the ADC, temperature sensor, buffered DAC, and CMPSS.

The analog subsystem has the following features:

- Flexible voltage references
  - V_{REFHIA} and V_{REFLOA}, V_{REFHIB} and V_{REFLOB}, V_{REFHIC} and V_{REFLOC}, and V_{REFHID} and V_{REFLOD} externally supplied reference voltage pins
    - Selectable by ADCs and buffered DACs
  - VDAC externally supplied reference voltage pin
    - Selectable by buffered DACs and comparator subsystem DACs
    - Low reference is V_{SSA}
- Flexible pin usage
  - Buffered DAC and comparator subsystem functions multiplexed with ADC inputs
- Internal connection to V_{REFLO} on all ADCs for offset self-calibration

図 4-28 shows the Analog Subsystem Block Diagram for the 337-ball ZWT package. 図 4-29 shows the Analog Subsystem Block Diagram for the 176-pin PTP package. 図 4-30 shows the Analog Subsystem Block Diagram for the 100-pin PZP package.

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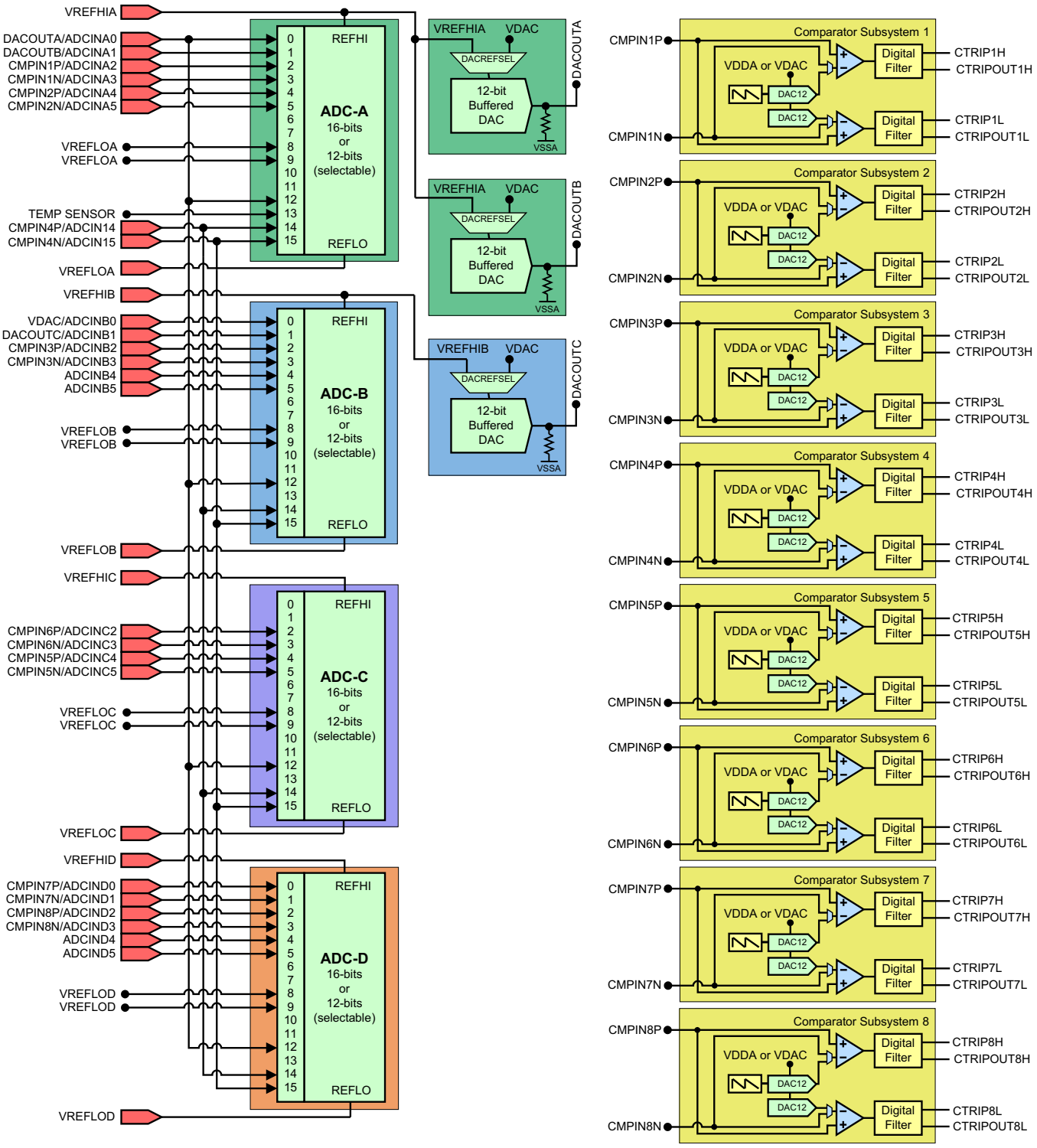


図 4-28. Analog Subsystem Block Diagram (337-Ball ZWT)

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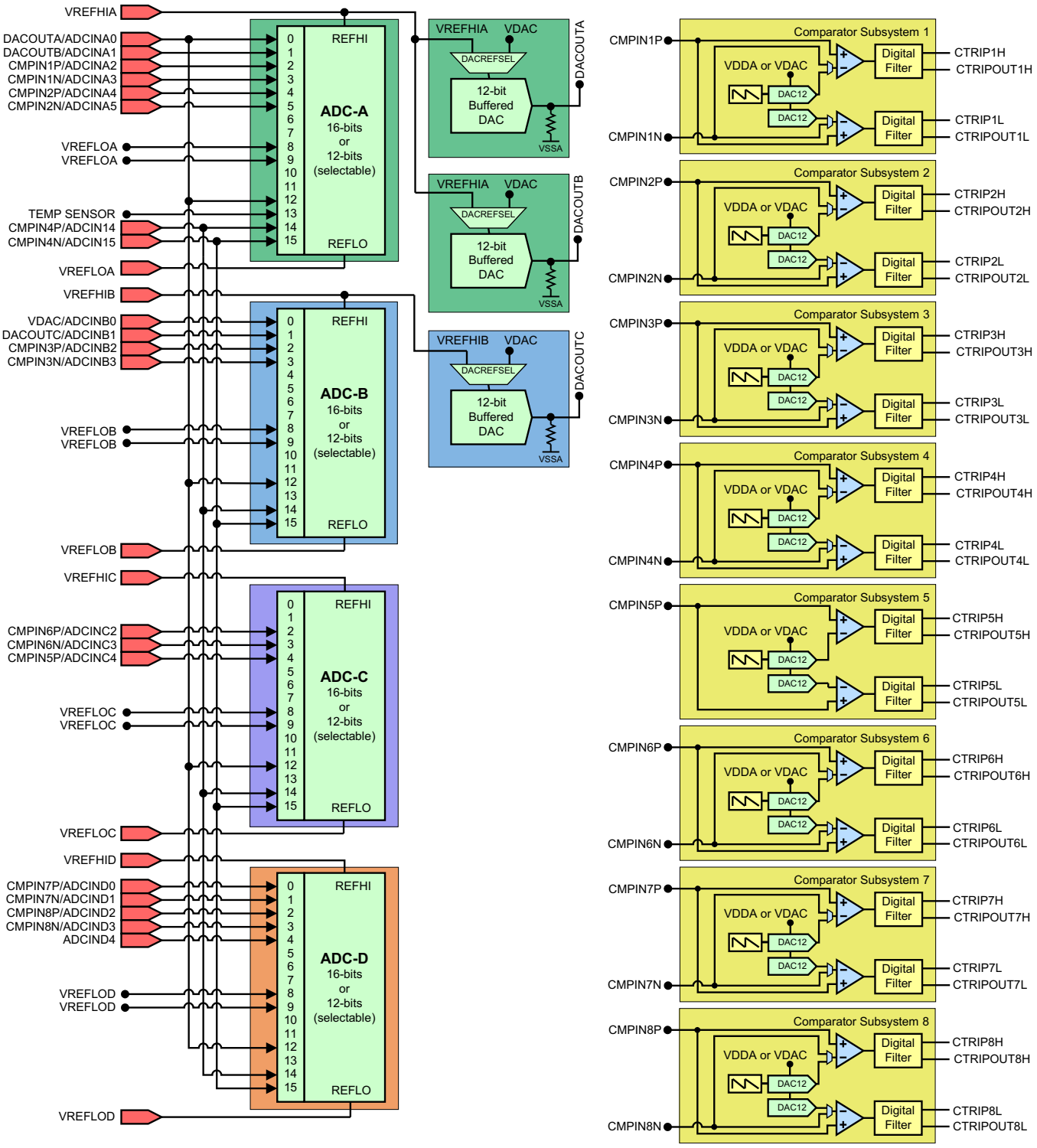


図 4-29. Analog Subsystem Block Diagram (176-Pin PTP)

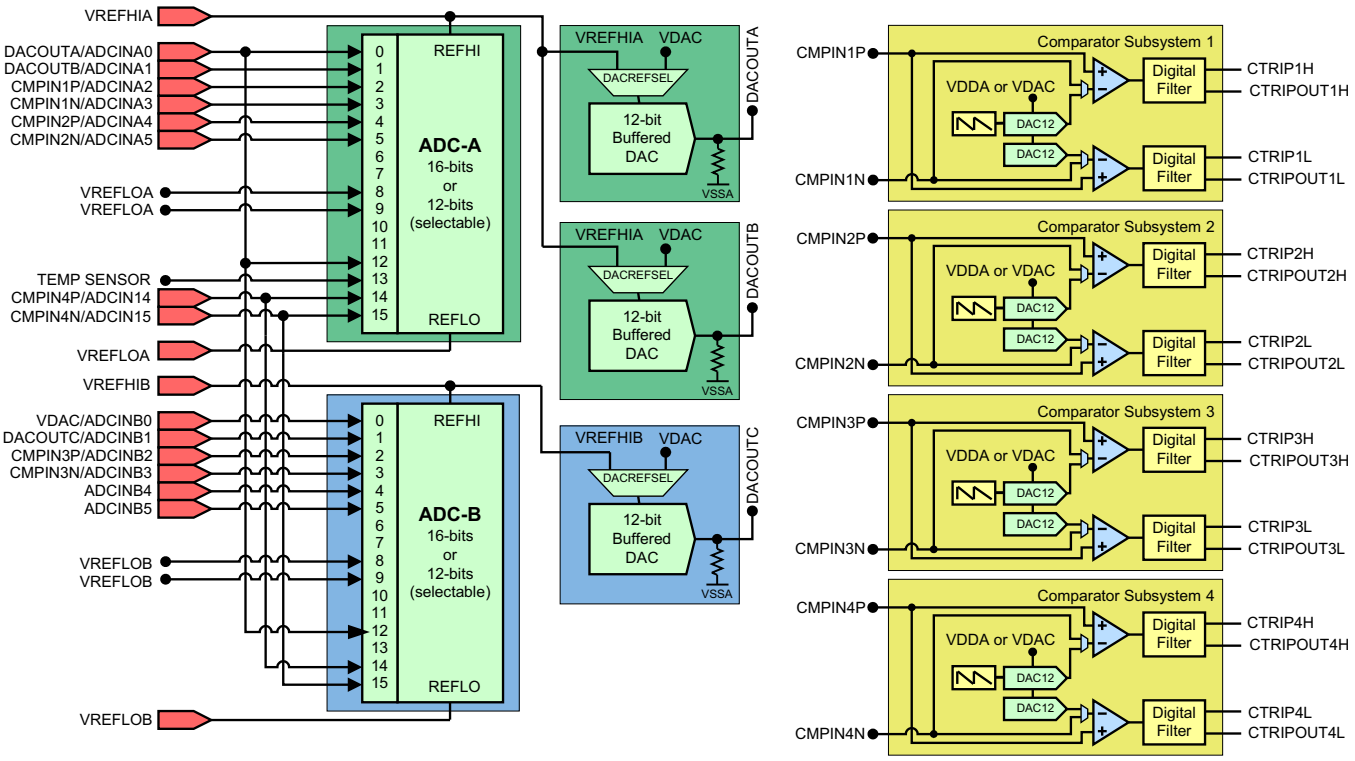


図 4-30. Analog Subsystem Block Diagram (100-Pin PZP)

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4.8.1 Analog-to-Digital Converter (ADC)

The ADCs on this device are successive approximation (SAR) style ADCs with selectable resolution of either 16 bits or 12 bits. There are multiple ADC modules which allow simultaneous sampling. The ADC wrapper is start-of-conversion (SOC) based [see the SOC Principle of Operation section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

Each ADC has the following features:

- Selectable resolution of 16 bits or 12 bits
- Ratiometric external reference set by V_{REFHI} and V_{REFLO}
- Differential signal conversions (16-bit mode only)
- Single-ended signal conversions (12-bit mode only)
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - Software immediate start
  - All ePWMs
  - GPIO XINT2
  - CPU timers
  - ADCINT1 or 2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

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図 4-31 shows the ADC module block diagram.

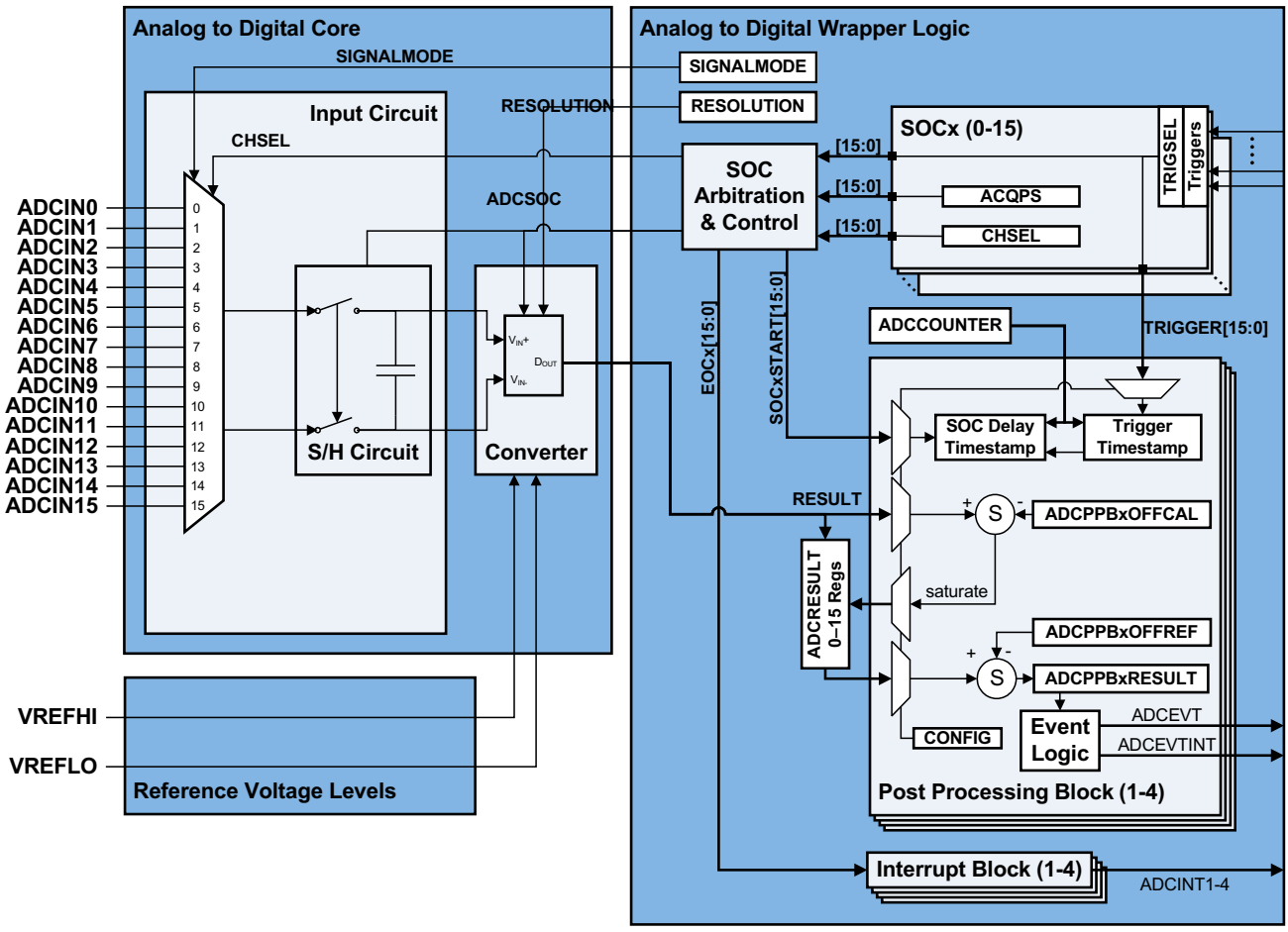


図 4-31. ADC Module Block Diagram

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4.8.1.1 ADC Electrical Data and Timing

Table 4-41 shows the ADC operating conditions for 16-bit differential mode. Table 4-42 shows the ADC characteristics for 16-bit differential mode. Table 4-43 shows the ADC operating conditions for 12-bit single-ended mode. Table 4-44 shows the ADC characteristics for 12-bit single-ended mode. Table 4-45 shows the ADCEXTSOC timing requirements.

Table 4-41. ADC Operating Conditions (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	5		50	MHz
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	320			ns
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
$V_{REFHI} - V_{REFLO}$	2.4		V_{DDA}	V
ADC input conversion range	V_{REFLO}		V_{REFHI}	V
ADC input signal common mode voltage(2)(3)	$V_{REFCM} - 50$	V_{REFCM}	$V_{REFCM} + 50$	mV

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$
(3) The V_{REFCM} requirements will not be met if the negative ADC input pin is connected to V_{SSA} or V_{REFLO}.

NOTE

The ADC inputs should be kept below V_{DDA} + 0.3 V during operation. If an ADC input exceeds this level, the V_{REF} internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same V_{REF}.

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Table 4-42. ADC Characteristics (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles(2)		29.6		31	ADCCLKs
Power-up time (after setting ADCPWDNZ to first conversion)				500	µs
Gain error		–64	±9	64	LSBs
Offset error(3)		–16	±9	16	LSBs
Channel-to-channel gain error			±6		LSBs
Channel-to-channel offset error			±3		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±6		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±3		LSBs
DNL(4)		> –1	±0.5	1	LSBs
INL		–3	±1.5	3	LSBs
SNR(5)(6)	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		87.6		dB
THD(5)(6)	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		–93.5		dB
SFDR(5)(6)	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		95.4		dB
SINAD(5)(6)	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		86.6		dB
ENOB(5)(6)	V_{REFHI} = 2.5 V, f_{in} = 10 kHz, single ADC(7)		14.1		bits
	V_{REFHI} = 2.5 V, f_{in} = 10 kHz, synchronous ADCs(8)		14.1		
	V_{REFHI} = 2.5 V, f_{in} = 10 kHz, asynchronous ADCs(9)		Not supported		
PSRR	V_{DDA} = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		77		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		74		dB
CMRR	DC to 1 MHz		60		dB
V_{REFHI} input current			190		µA
ADC-to-ADC isolation(6)(10)(11)	V_{REFHI} = 2.5 V, synchronous ADCs(8)	–2		2	LSBs
	V_{REFHI} = 2.5 V, asynchronous ADCs(9)		Not supported		

(1) Typical values are measured with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
(2) See 4.8.1.1.2.
(3) Difference from conversion result 32768 when ADCINp = ADCINn = V_{REFCM}.
(4) No missing codes.
(5) AC parameters will be impacted by clock source accuracy and jitter, this should be taken into account when selecting the clock source for the system. The clock source used for these parameters was a high-accuracy external clock fed through the PLL. The on-chip Internal Oscillator has higher jitter than an external crystal and these parameters will degrade if it is used as a clock source.
(6) I/O activity is minimized on pins adjacent to ADC input and V_{REFHI} pins as part of best practices to reduce capacitive coupling and crosstalk.
(7) One ADC operating while all other ADCs are idle.
(8) All ADCs operating with identical ADCCLK, S+H durations, triggers, and resolution.
(9) Any ADCs operating with heterogeneous ADCCLK, S+H durations, triggers, or resolution.
(10) Maximum DC code deviation due to operation of multiple ADCs simultaneously.
(11) Value based on characterization.

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Table 4-43. ADC Operating Conditions (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	5		50	MHz
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	75			ns
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
$V_{REFHI} - V_{REFLO}$	2.4		V_{DDA}	V
ADC input conversion range	V_{REFLO}		V_{REFHI}	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

NOTE

The ADC inputs should be kept below V_{DDA} + 0.3 V during operation. If an ADC input exceeds this level, the V_{REF} internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same V_{REF}.

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Table 4-44. ADC Characteristics (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles(2)		10.1		11	ADCCLKs
Power-up time				500	µs
Gain error		–5	±3	5	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±4		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±2		LSBs
DNL(3)		> –1	±0.5	1	LSBs
INL		–2	±1.0	2	LSBs
SNR(4)(5)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		68.8		dB
THD(4)(5)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		–78.4		dB
SFDR(4)(5)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		79.2		dB
SINAD(4)(5)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		68.4		dB
ENOB(4)(5)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, single ADC(6), all packages		11.1		bits
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, synchronous ADCs(7), all packages		11.1		
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, asynchronous ADCs(8), 100-pin PZP package		Not supported		
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, asynchronous ADCs(8), 176-pin PTP package		9.7		
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, asynchronous ADCs(8), 337-ball ZWT package		10.9		
PSRR	V_{DDA} = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		57		dB
ADC-to-ADC isolation(5)(9)(10)	V_{REFHI} = 2.5 V, synchronous ADCs(7), all packages	–1		1	LSBs
	V_{REFHI} = 2.5 V, asynchronous ADCs(8), 100-pin PZP package		Not supported		
	V_{REFHI} = 2.5 V, asynchronous ADCs(8), 176-pin PTP package	–9		9	
	V_{REFHI} = 2.5 V, asynchronous ADCs(8), 337-ball ZWT package	–2		2	
V_{REFHI} input current			130		µA

(1) Typical values are measured with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
(2) See 4.8.1.1.2.
(3) No missing codes.
(4) AC parameters will be impacted by clock source accuracy and jitter, this should be taken into account when selecting the clock source for the system. The clock source used for these parameters was a high-accuracy external clock fed through the PLL. The on-chip Internal Oscillator has higher jitter than an external crystal and these parameters will degrade if it is used as a clock source.
(5) I/O activity is minimized on pins adjacent to ADC input and V_{REFHI} pins as part of best practices to reduce capacitive coupling and crosstalk.
(6) One ADC operating while all other ADCs are idle.
(7) All ADCs operating with identical ADCCLK, S+H durations, triggers, and resolution.
(8) Any ADCs operating with heterogeneous ADCCLK, S+H durations, triggers, or resolution.
(9) Maximum DC code deviation due to operation of multiple ADCs simultaneously.
(10) Value based on characterization.

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Table 4-45. ADCEXTSOC Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.

4.8.1.1.1 ADC Input Models

注

ADC channels ADCINA0, ADCINA1, and ADCINB1 have a 50-kΩ pulldown resistor to V_{SSA}.

For single-ended operation, the ADC input characteristics are given by 表 4-46 and 図 4-32.

表 4-46. Single-Ended Input Model Parameters

	DESCRIPTION	VALUE (12-BIT MODE)
C_p	Parasitic input capacitance	See 表 4-48
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	14.5 pF
R_s	Nominal source impedance	50 Ω

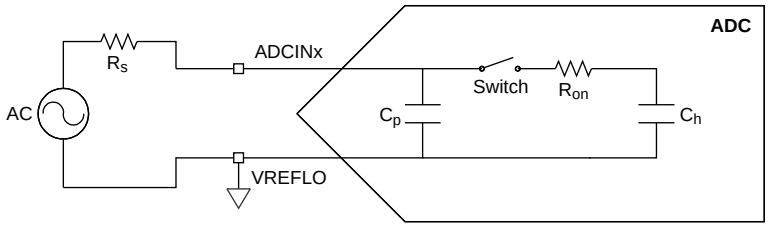


図 4-32. Single-Ended Input Model

For differential operation, the ADC input characteristics are given by 表 4-47 and 図 4-33.

表 4-47. Differential Input Model Parameters

	DESCRIPTION	VALUE (16-BIT MODE)
C_p	Parasitic input capacitance	See 表 4-48
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

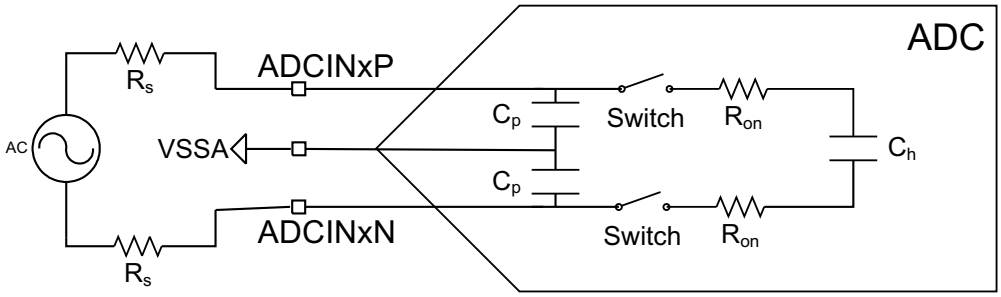


図 4-33. Differential Input Model

表 4-48 shows the parasitic capacitance on each channel. Also, enabling a comparator adds approximately 1.4 pF of capacitance on positive comparator inputs and 2.5 pF of capacitance on negative comparator inputs.

表 4-48. Per-Channel Parasitic Capacitance

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
ADCINA0	12.9	N/A
ADCINA1	10.3	N/A
ADCINA2	5.9	7.3
ADCINA3	6.3	8.8
ADCINA4	5.9	7.3
ADCINA5	6.3	8.8
ADCINB0(1)	117.0	N/A
ADCINB1	10.6	N/A
ADCINB2	5.9	7.3
ADCINB3	6.2	8.7
ADCINB4	5.2	N/A
ADCINB5	5.1	N/A
ADCINC2	5.5	6.9
ADCINC3	5.8	8.3
ADCINC4	5.0	6.4
ADCINC5	5.3	7.8
ADCIND0	5.3	6.7
ADCIND1	5.7	8.2
ADCIND2	5.3	6.7
ADCIND3	5.6	8.1
ADCIND4	4.3	N/A
ADCIND5	4.3	N/A
ADCIN14	8.6	10.0
ADCIN15	9.0	11.5

(1) The increased capacitance is due to VDAC functionality.

These input models should be used along with actual signal source impedance to determine the acquisition window duration. See the Choosing an Acquisition Window Duration section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for more information.

The user should analyze the ADC input setting assuming worst-case initial conditions on C_h. This will require assuming that C_h could start the S+H window completely charged to V_{REFHI} or completely discharged to V_{REFLO}. When the ADC transitions from an odd-numbered channel to an even-numbered channel, or vice-versa, the actual initial voltage on C_h will be close to being completely discharged to V_{REFLO}. For even-to-even or odd-to-odd channel transitions, the initial voltage on C_h will be close to the voltage of the previously converted channel.

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4.8.1.1.2 ADC Timing Diagrams

表 4-49 shows the ADC timings in 12-bit mode (SYSCLK cycles). 表 4-50 shows the ADC timings in 16-bit mode. 図 4-34 and 図 4-35 show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

The following parameters are identified in the timing diagrams:

- The parameter t_{SH} is the duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} will not necessarily be the same for different SOCs.
- The parameter t_{LAT} is the time from the end of the S+H window until the ADC conversion results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results will be returned.
- The parameter t_{EOC} is the time from the end of the S+H window until the next ADC conversion S+H window can begin. In 16-bit mode, this will coincide with the latching of the conversion results, while in 12-bit mode, the subsequent sample can start before the conversion results are latched.
- The parameter t_{INT} is the time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, this will coincide with the conversion results being latched into the result register. If the bit is cleared, this will coincide with the end of the S+H window.

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表 4-49. ADC Timings in 12-Bit Mode (SYSCLK Cycles)

ADCCLK PRESCALE		SYSCLK CYCLES				ADCCLK CYCLES
ADCCTL2 [PRESCALE]	RATIO ADCCLK:SYSCLK	t_{EOC}	t_{LAT}	$t_{INT(EARLY)}$	$t_{INT(LATE)}$	t_{EOC}
0	1	11	13	1	11	11.0
1	1.5	Invalid				
2	2	21	23	1	21	10.5
3	2.5	26	28	1	26	10.4
4	3	31	34	1	31	10.3
5	3.5	36	39	1	36	10.3
6	4	41	44	1	41	10.3
7	4.5	46	49	1	46	10.2
8	5	51	55	1	51	10.2
9	5.5	56	60	1	56	10.2
10	6	61	65	1	61	10.2
11	6.5	66	70	1	66	10.2
12	7	71	76	1	71	10.1
13	7.5	76	81	1	76	10.1
14	8	81	86	1	81	10.1
15	8.5	86	91	1	86	10.1

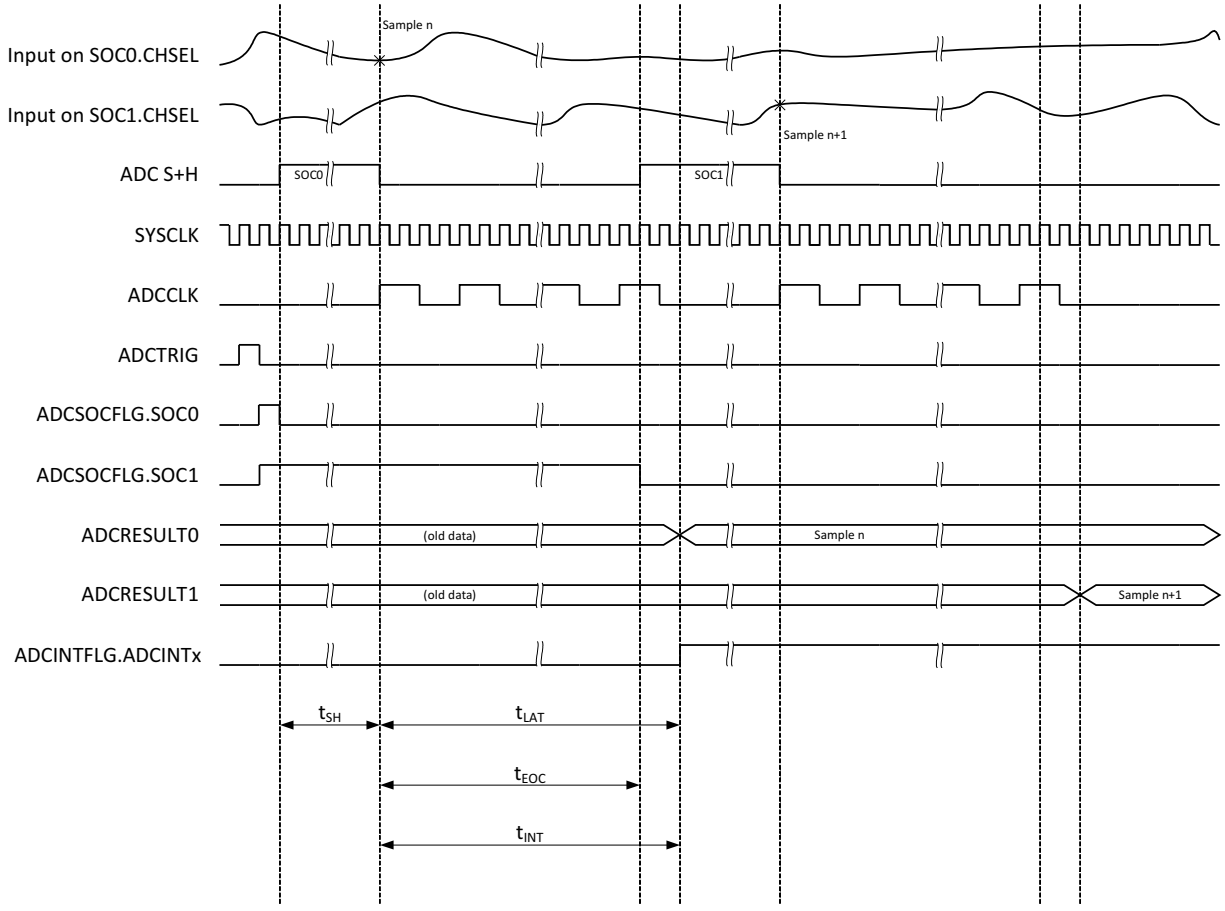


図 4-34. ADC Timings for 12-Bit Mode

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表 4-50. ADC Timings in 16-Bit Mode

ADCCLK PRESCALE		SYSCLK CYCLES				ADCCLK CYCLES
ADCCTL2 [PRESCALE]	RATIO ADCCLK:SYSCLK	t_{EOC}	t_{LAT}	$t_{INT(EARLY)}$	$t_{INT(LATE)}$	t_{EOC}
0	1	31	32	1	31	31.0
1	1.5	Invalid				
2	2	60	61	1	60	30.0
3	2.5	75	75	1	75	30.0
4	3	90	91	1	90	30.0
5	3.5	104	106	1	104	29.7
6	4	119	120	1	119	29.8
7	4.5	134	134	1	134	29.8
8	5	149	150	1	149	29.8
9	5.5	163	165	1	163	29.6
10	6	178	179	1	178	29.7
11	6.5	193	193	1	193	29.7
12	7	208	209	1	208	29.7
13	7.5	222	224	1	222	29.6
14	8	237	238	1	237	29.6
15	8.5	252	252	1	252	29.6

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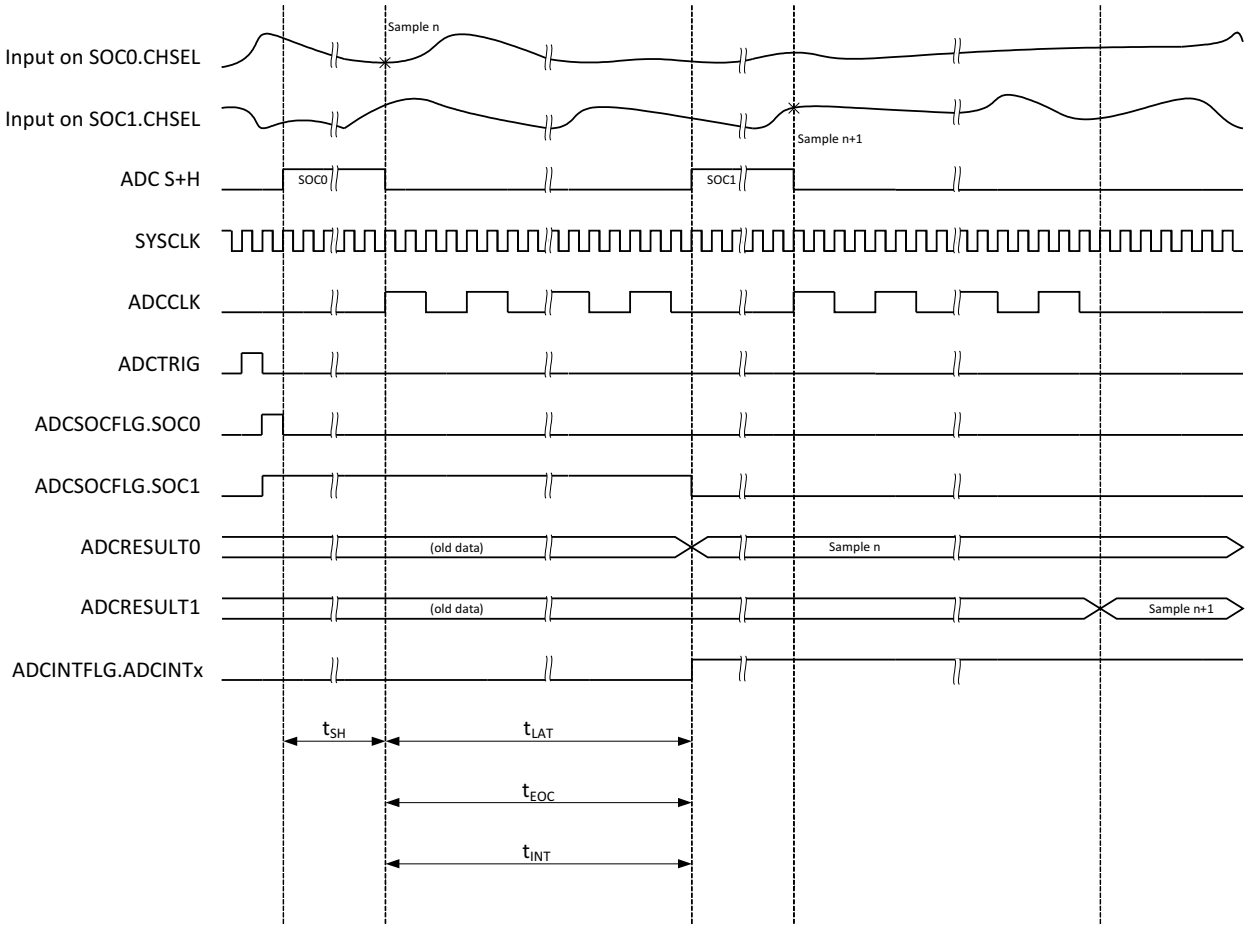


図 4-35. ADC Timings for 16-Bit Mode

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4.8.1.2 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in Table 4-51.

Table 4-51. Temperature Sensor Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Temperature accuracy		±15		°C
Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)		500		µs
ADC acquisition time	700			ns

4.8.2 Comparator Subsystem (CMPSS)

Each CMPSS module includes two comparators, two internal voltage reference DACs (CMPSS DACs), two digital glitch filters, and one ramp generator. There are two inputs, CMPINxP and CMPINxN. Each of these inputs will be internally connected to an ADCIN pin. The CMPINxP pin is always connected to the positive input of the CMPSS comparators. CMPINxN can be used instead of the DAC output to drive the negative comparator inputs. There are two comparators, and therefore two outputs from the CMPSS module, which are connected to the input of a digital filter module before being passed on to the Comparator TRIP crossbar and either PWM modules or directly to a GPIO pin. 図 4-36 shows the CMPSS connectivity on the 337-ball ZWT and 176-pin PTP packages. 図 4-37 shows CMPSS connectivity on the 100-pin PZP package.

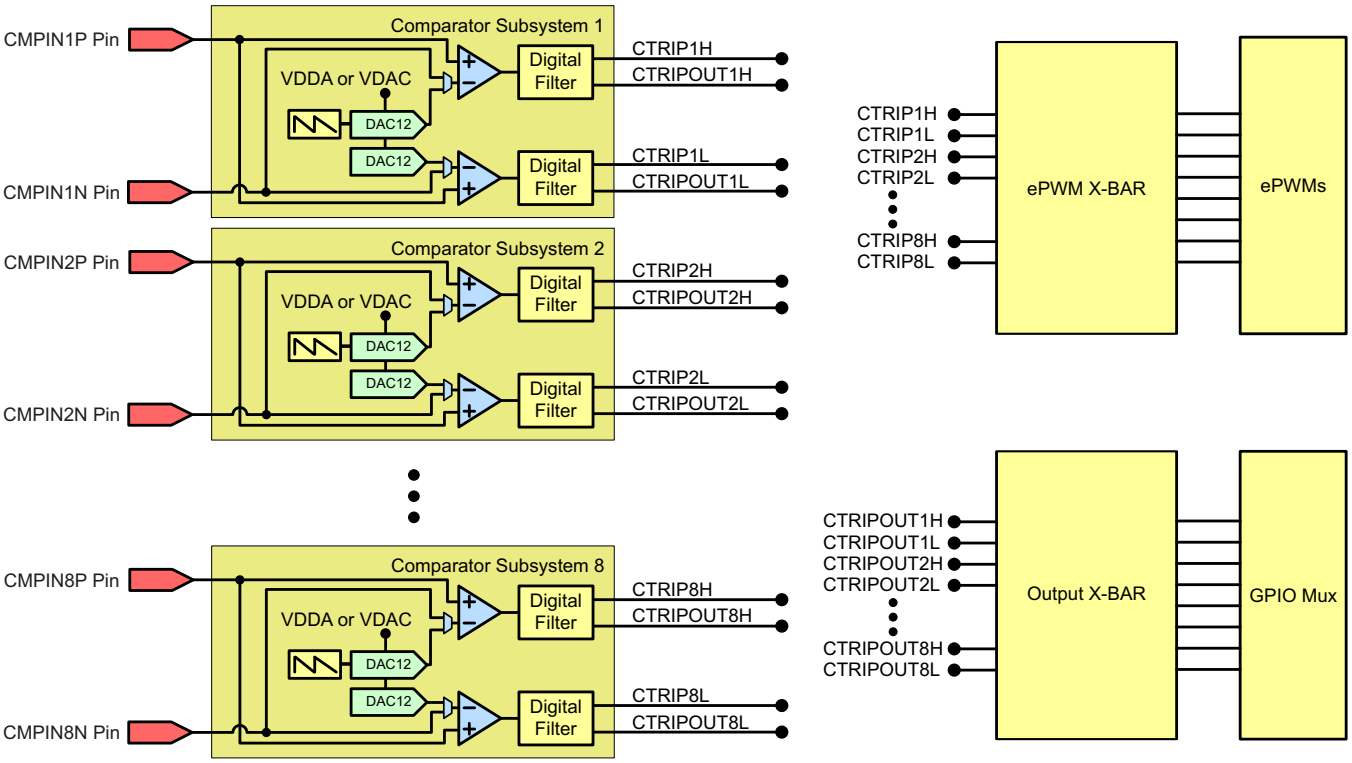


図 4-36. CMPSS Connectivity (337-Ball ZWT and 176-Pin PTP)

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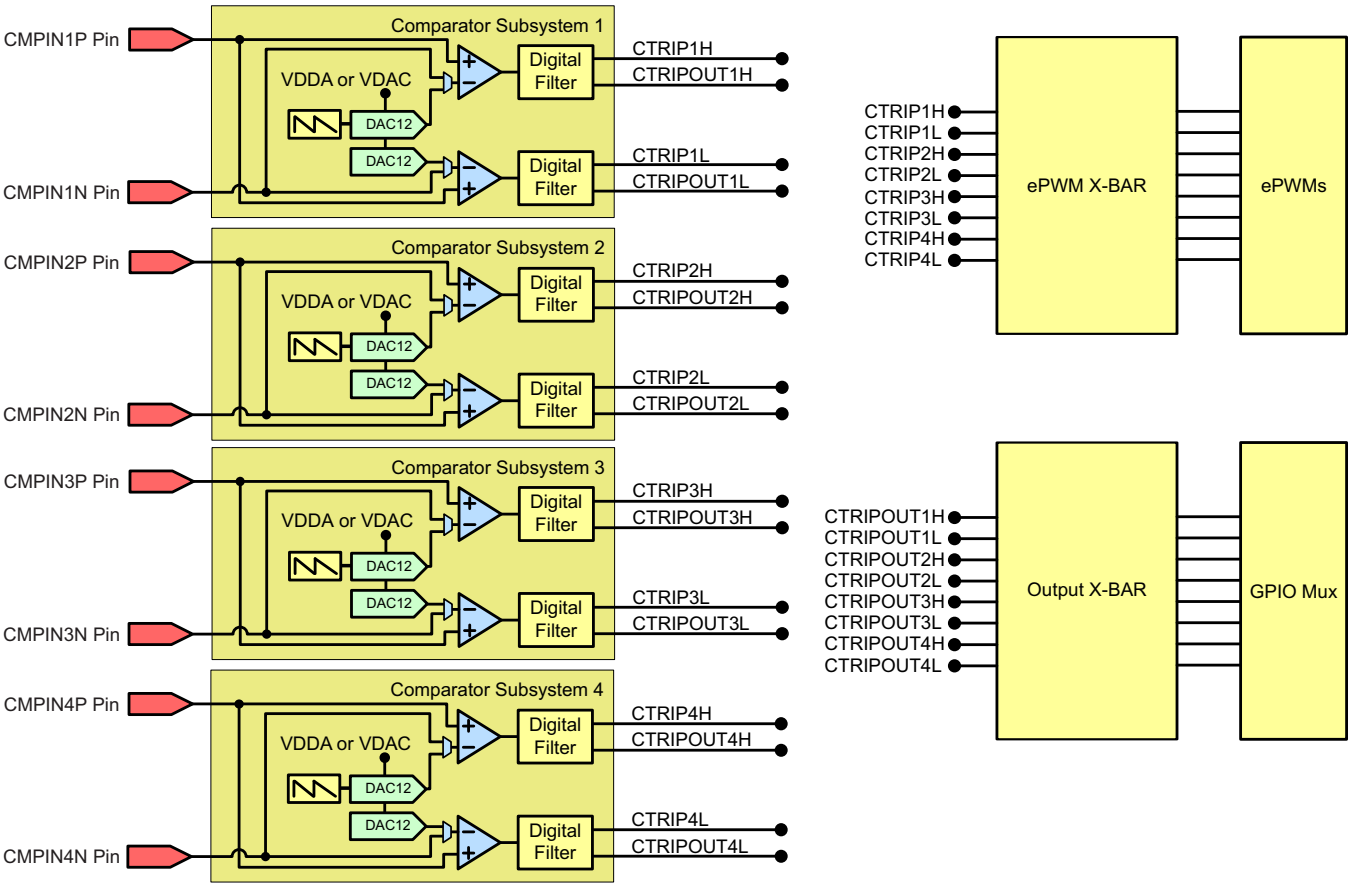


図 4-37. CMPSS Connectivity (100-Pin PZP)

4.8.2.1 CMPSS Electrical Data and Timing

Table 4-52 shows the comparator electrical characteristics. Figure 4-38 shows the CMPSS comparator input referred offset. Figure 4-39 shows the CMPSS comparator hysteresis.

Table 4-52. Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time (from COMPCTL[COMPDACE] to comparator ready)				10	µs
Comparator input (CMPINxx) range		0		V_{DDA}	V
Input referred offset error		–20		20	mV
Hysteresis (1)	1x		12		CMPSS DAC LSB
	2x		24		
	3x		36		
	4x		48		
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)	Step response		21	60	ns
	Ramp response (1.65 V/µs)		26		
	Ramp response (8.25 mV/µs)		30		

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

NOTE

The CMPSS inputs must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit will isolate the internal comparator from the external pin until the external pin voltage returns below V_{DDA} + 0.3 V. During this time, the internal comparator input will be floating and can decay below V_{DDA} within approximately 0.5 µs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

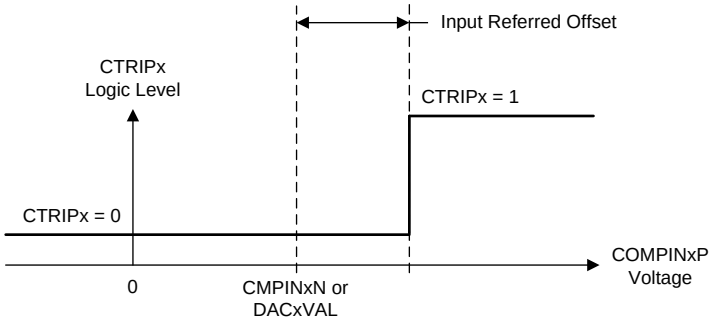


Figure 4-38. CMPSS Comparator Input Referred Offset

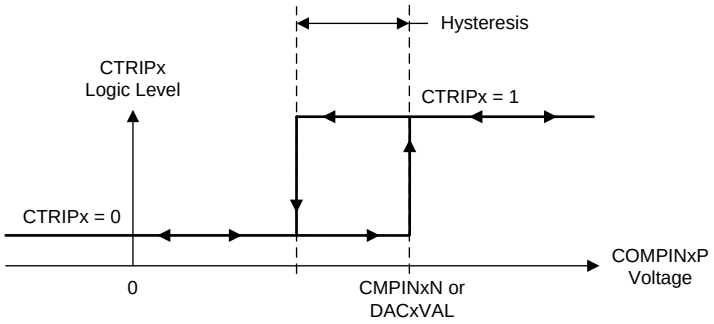


Figure 4-39. CMPSS Comparator Hysteresis

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Table 4-53 shows the CMPSS DAC static electrical characteristics. Figure 4-40 shows the CMPSS DAC static offset. Figure 4-41 shows the CMPSS DAC static gain. Figure 4-42 shows the CMPSS DAC static linearity.

Table 4-53. CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		V_{DDA}	V
	External reference	0		VDAC	
Static offset error(1)		–25		25	mV
Static gain error(1)		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1 LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance(2)	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time(2)			200		ns
VDAC reference voltage	When VDAC is reference	2.4	2.5 or 3.0	V_{DDA}	V
VDAC load(3)	When VDAC is reference		6		kΩ

(1) Includes comparator input referred errors.
(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(3) Per active CMPSS module.

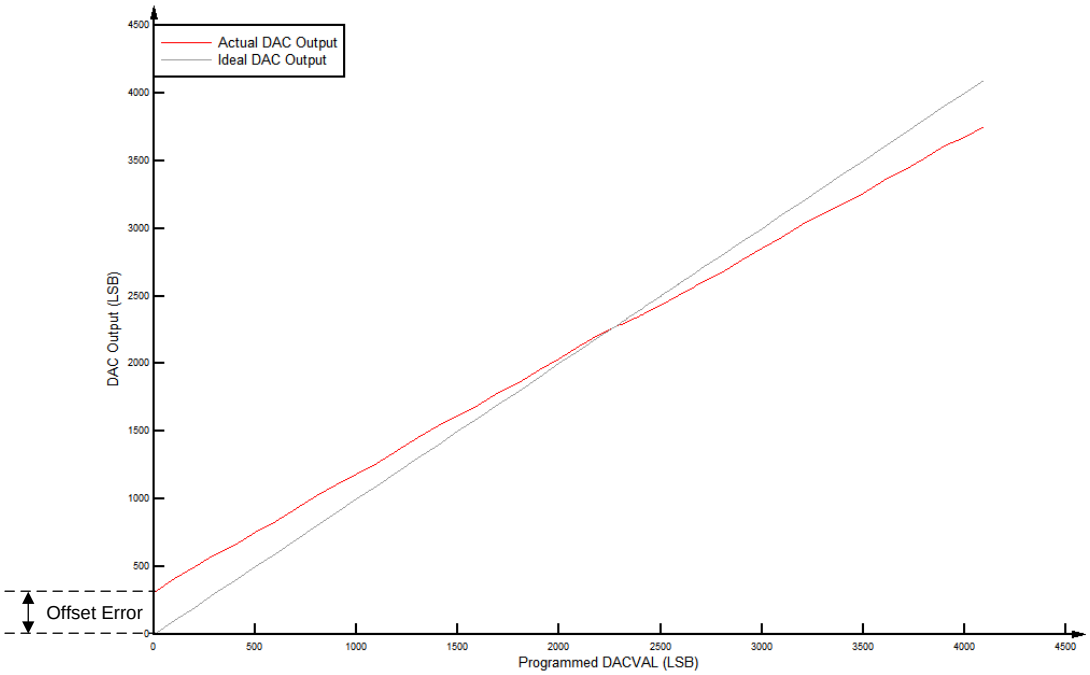


Figure 4-40. CMPSS DAC Static Offset

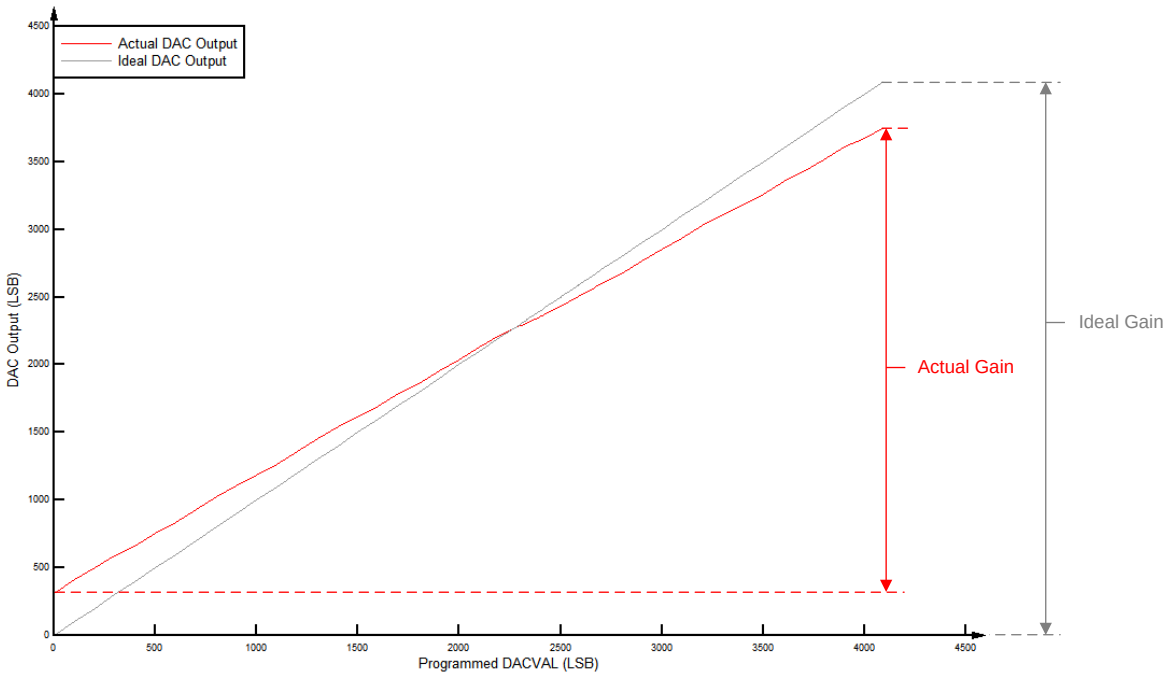


Figure 4-41. CMPSS DAC Static Gain

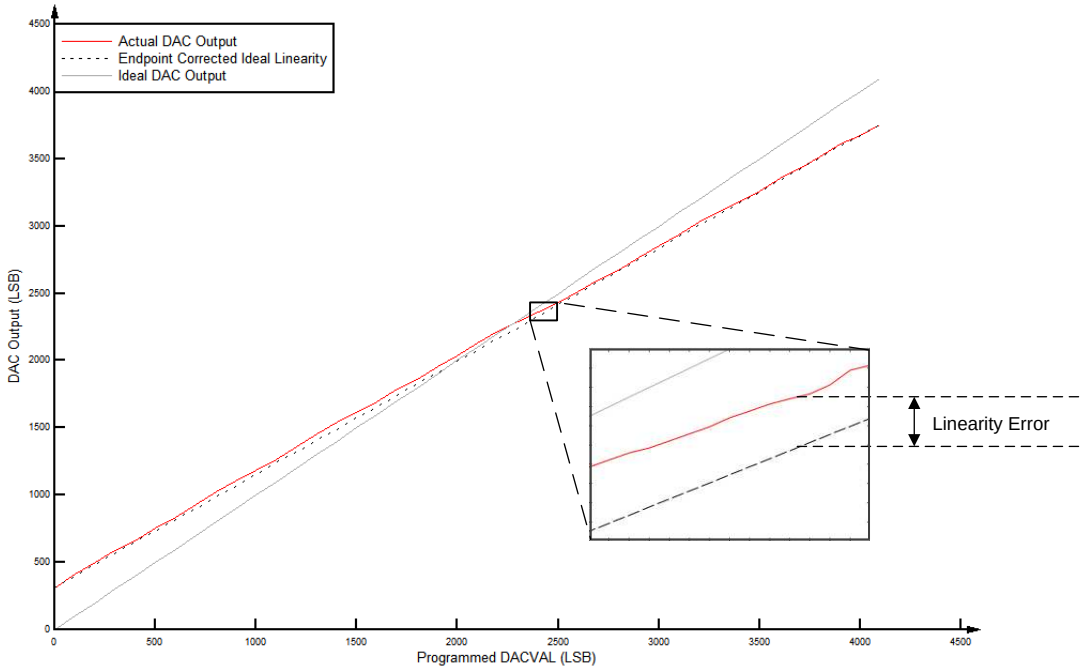


Figure 4-42. CMPSS DAC Static Linearity

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4.8.3 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal reference DAC and an analog output buffer that is capable of driving an external load. An integrated pulldown resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pulldown resistor cannot be disabled and remains as a passive component on the pin, even for other shared pin mux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with PWMSYNC events.

Each buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Pulldown resistor on output
- Ability to synchronize with PWMSYNC

The block diagram for the buffered DAC is shown in 図 4-43.

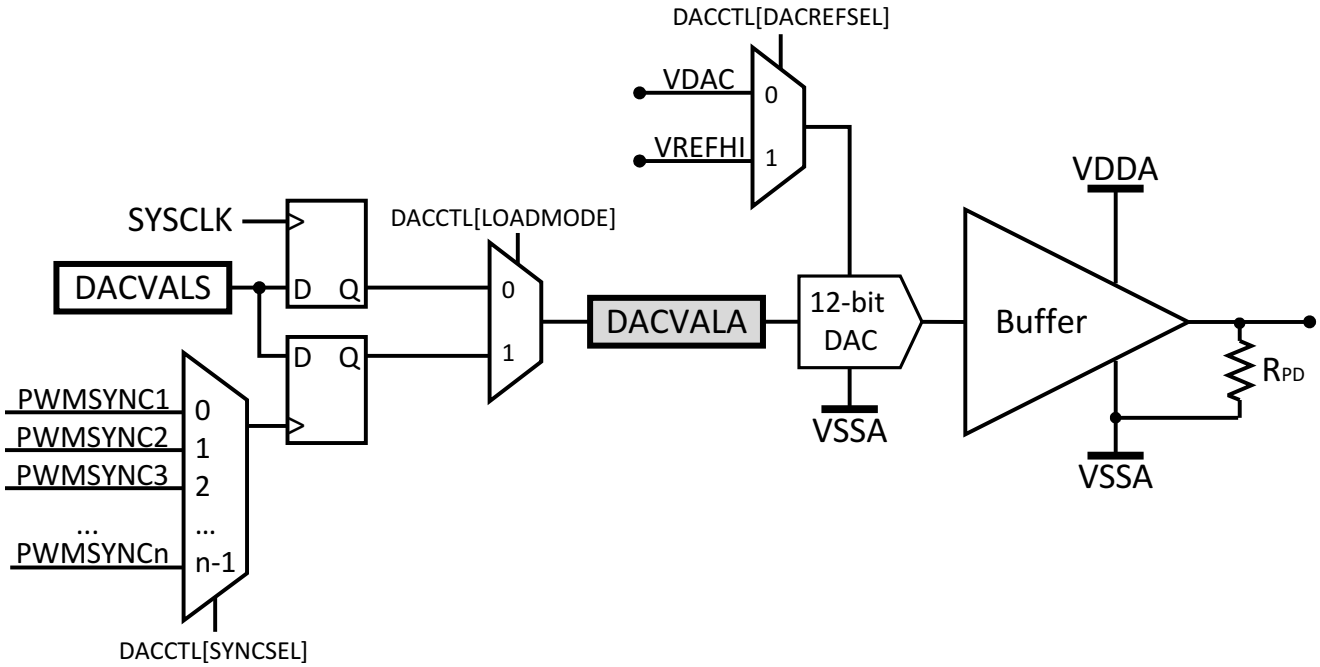


図 4-43. DAC Module Block Diagram

4.8.3.1 Buffered DAC Electrical Data and Timing

Table 4-54 shows the buffered DAC electrical characteristics. Figure 4-44 shows the buffered DAC offset. Figure 4-45 shows the buffered DAC gain. Figure 4-46 shows the buffered DAC linearity.

Table 4-54. Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time (DACOUTEN to DAC output valid)				10	µs
Trimmed offset error	Midpoint	–10		10	mV
Gain error(2)		–2.5		2.5	% of FSR
DNL(3)	Endpoint corrected	> –1		1	LSB
INL	Endpoint corrected	–5		5	LSB
DACOUTx settling time	Settling to 2 LSBs after 0.3V-to-3V transition		2		µs
Resolution			12		bits
Voltage output range(4)		0.3		V_{DDA} – 0.3	V
Capacitive load	Output drive capability			100	pF
Resistive load	Output drive capability	5			kΩ
R_{PD}			50		kΩ
Reference voltage(5)	VDAC or V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
Reference load(6)	VDAC or V_{REFHI}		170		kΩ
Output noise	Integrated noise from 100 Hz to 100 kHz		500		µVrms
	Noise density at 10 kHz		711		nVrms/√Hz
Glitch energy			1.5		V-ns
PSRR(7)	DC up to 1 kHz		70		dB
	100 kHz		30		
SNR	1020 Hz		67		dB
THD	1020 Hz		–63		dB
SFDR	1020 Hz, including harmonics and spurs		66		dBc
	1020 Hz, including only spurs		104		

(1) Typical values are measured with V_{REFHI} = 3.3 V and V_{REFLO} = 0 V unless otherwise noted. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
(2) Gain error is calculated for linear output range.
(3) The DAC output is monotonic.
(4) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(5) For best PSRR performance, VDAC or V_{REFHI} should be less than V_{DDA}.
(6) Per active Buffered DAC module.
(7) V_{REFHI} = 3.2 V, V_{DDA} = 3.3 V DC + 100 mV Sine.

NOTE

The VDAC pin must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If the VDAC pin exceeds this level, a blocking circuit may activate, and the internal value of VDAC may float to 0 V internally, giving improper DAC output.

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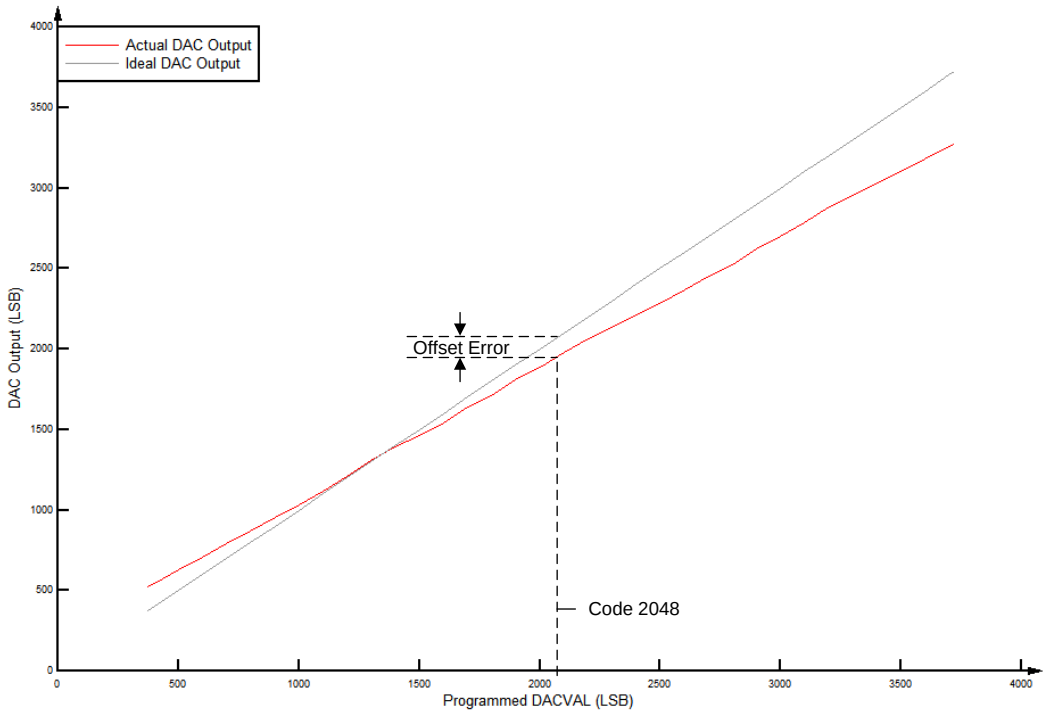


Figure 4-44. Buffered DAC Offset

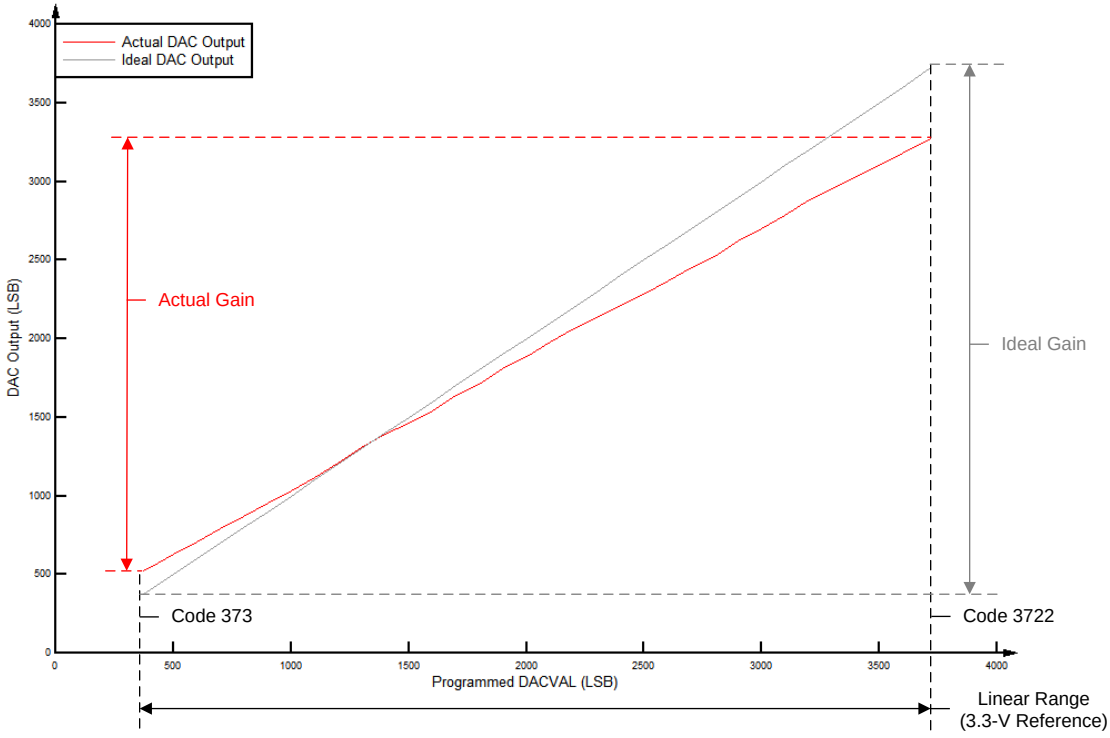


Figure 4-45. Buffered DAC Gain

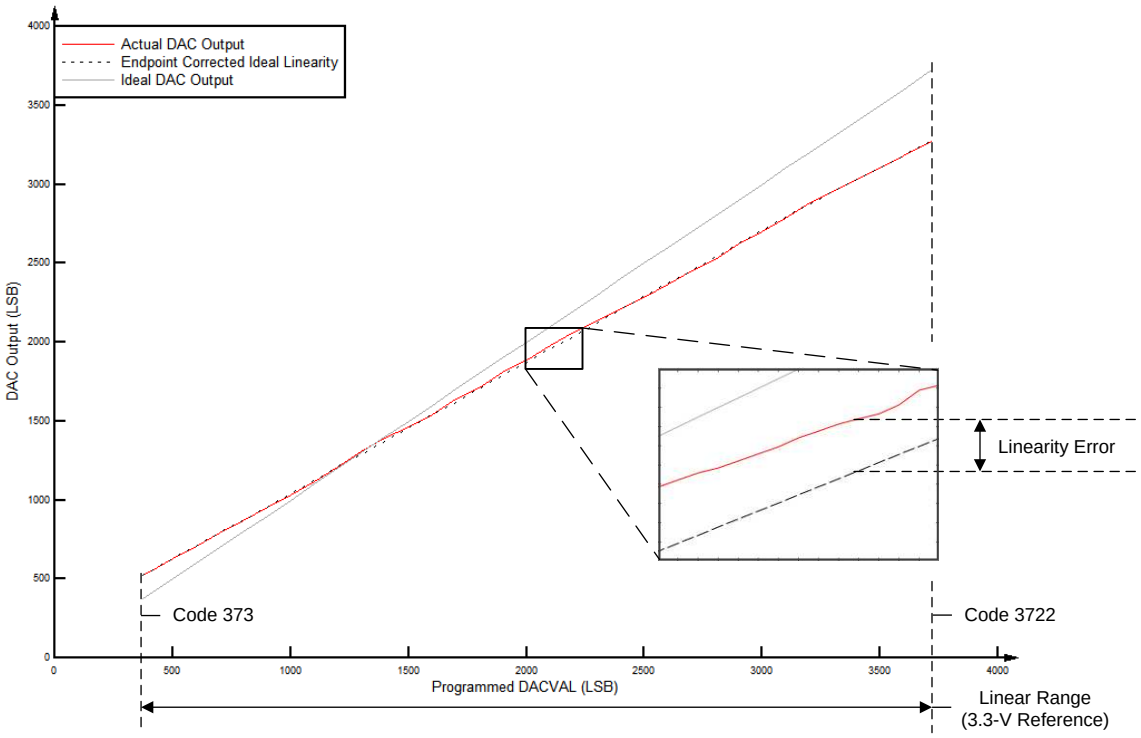


Figure 4-46. Buffered DAC Linearity

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4.9 Control Peripherals

4.9.1 Enhanced Capture (eCAP)

The eCAP module can be used in systems where accurate timing of external events is important.

Applications for eCAP include:

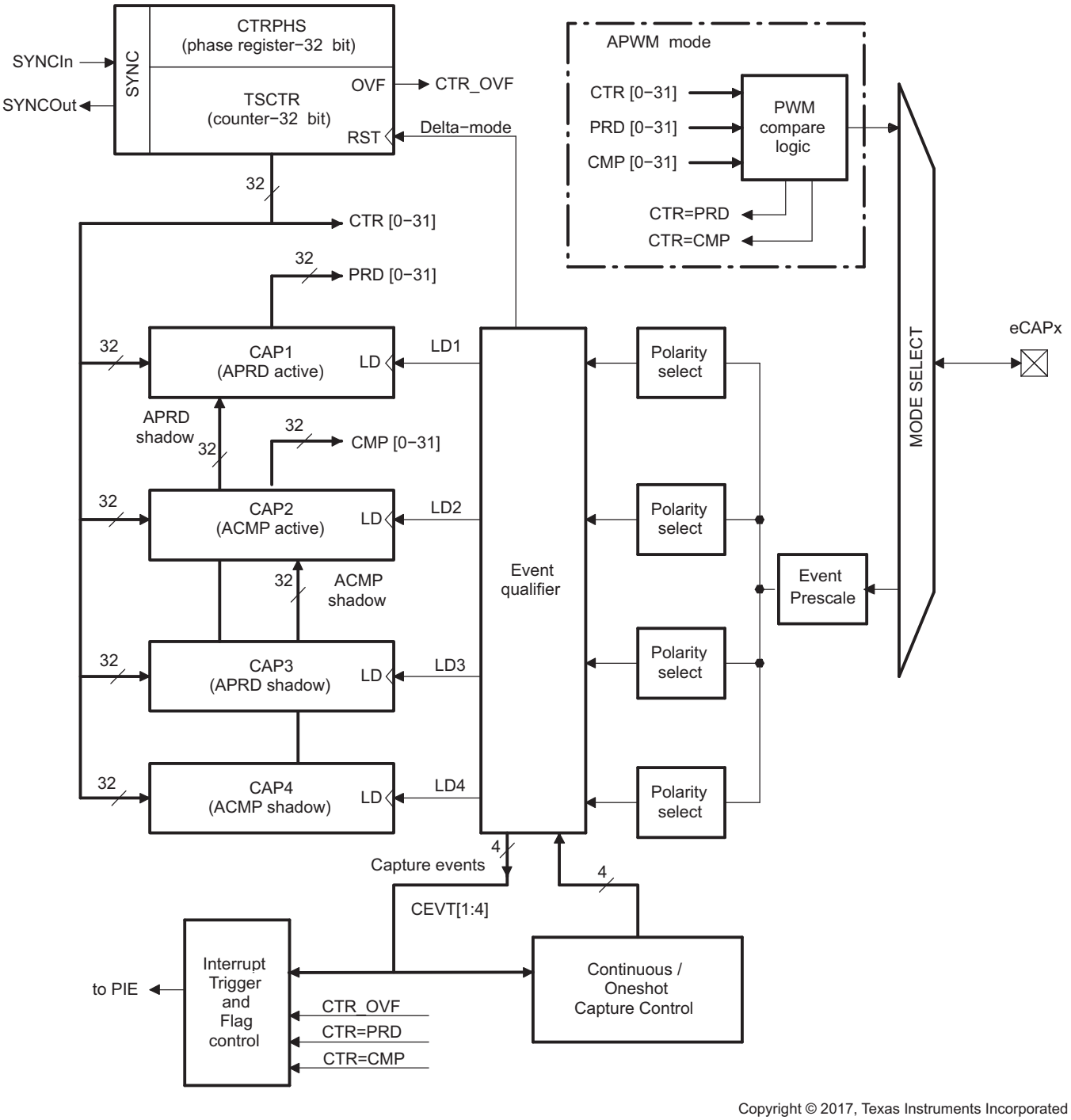
- Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 4-event time-stamp registers (each 32 bits)
- Edge-polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All of the above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).

The eCAP inputs connect to any GPIO input through the Input X-BAR. The APWM outputs connect to GPIO pins through the Output X-BAR to OUTPUTx positions in the GPIO mux. See Section 3.4.2 and Section 3.4.3.

図 4-47 shows the block diagram of an eCAP module.



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図 4-47. eCAP Block Diagram

The eCAP module is clocked by PERx.SYSCLK.

The clock enable bits (ECAP1–ECAP6) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

4.9.1.1 eCAP Electrical Data and Timing

Table 4-55 shows the eCAP timing requirement and Table 4-56 shows the eCAP switching characteristics.

Table 4-55. eCAP Timing Requirement(1)

			MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$		cycles
		Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$1t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.

Table 4-56. eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

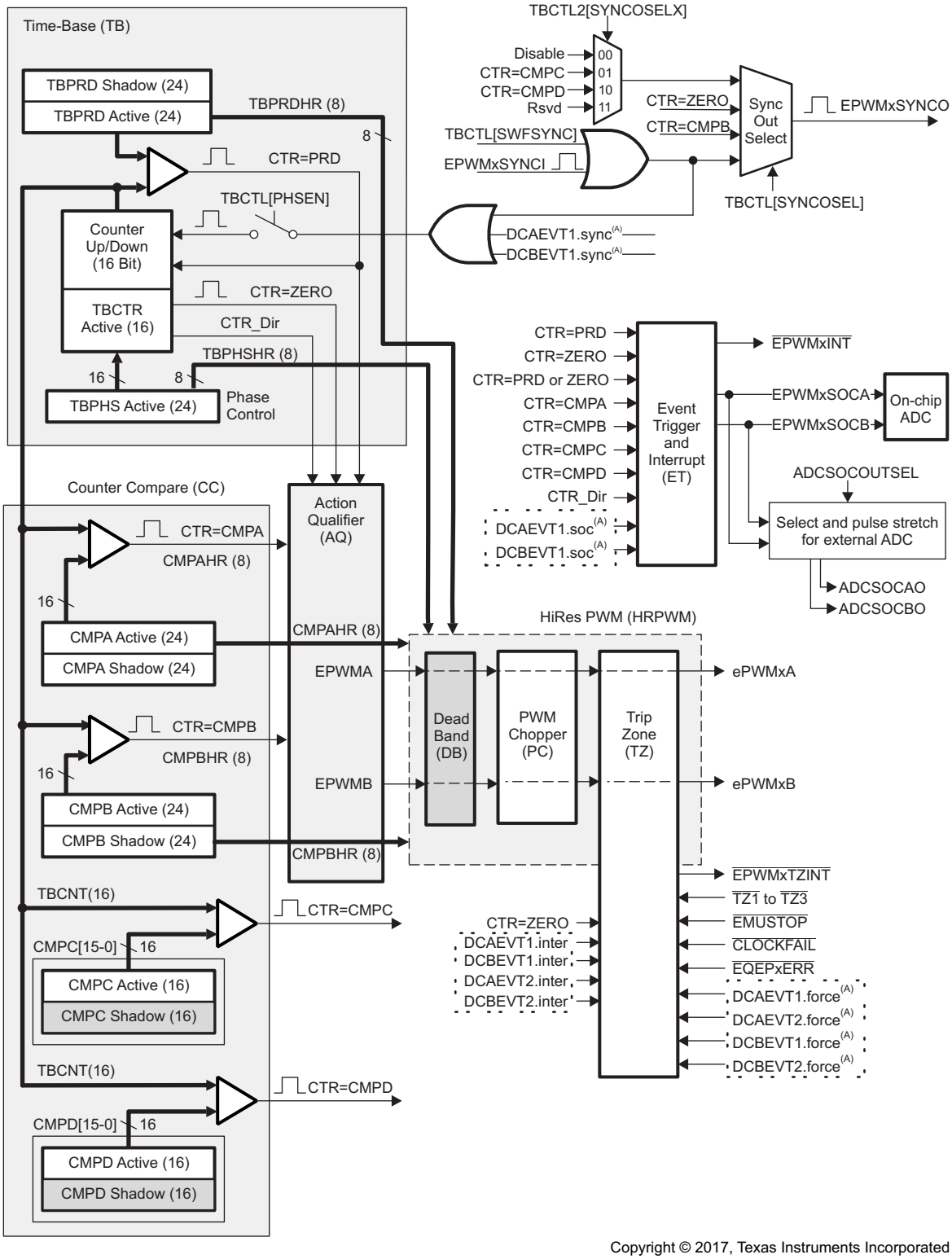
PARAMETER		MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20		ns

4.9.2 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

図 4-48 shows the signal interconnections with the ePWM. 図 4-49 shows the ePWM trip input connectivity.

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A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

図 4-48. ePWM Submodules and Critical Internal Signal Interconnects

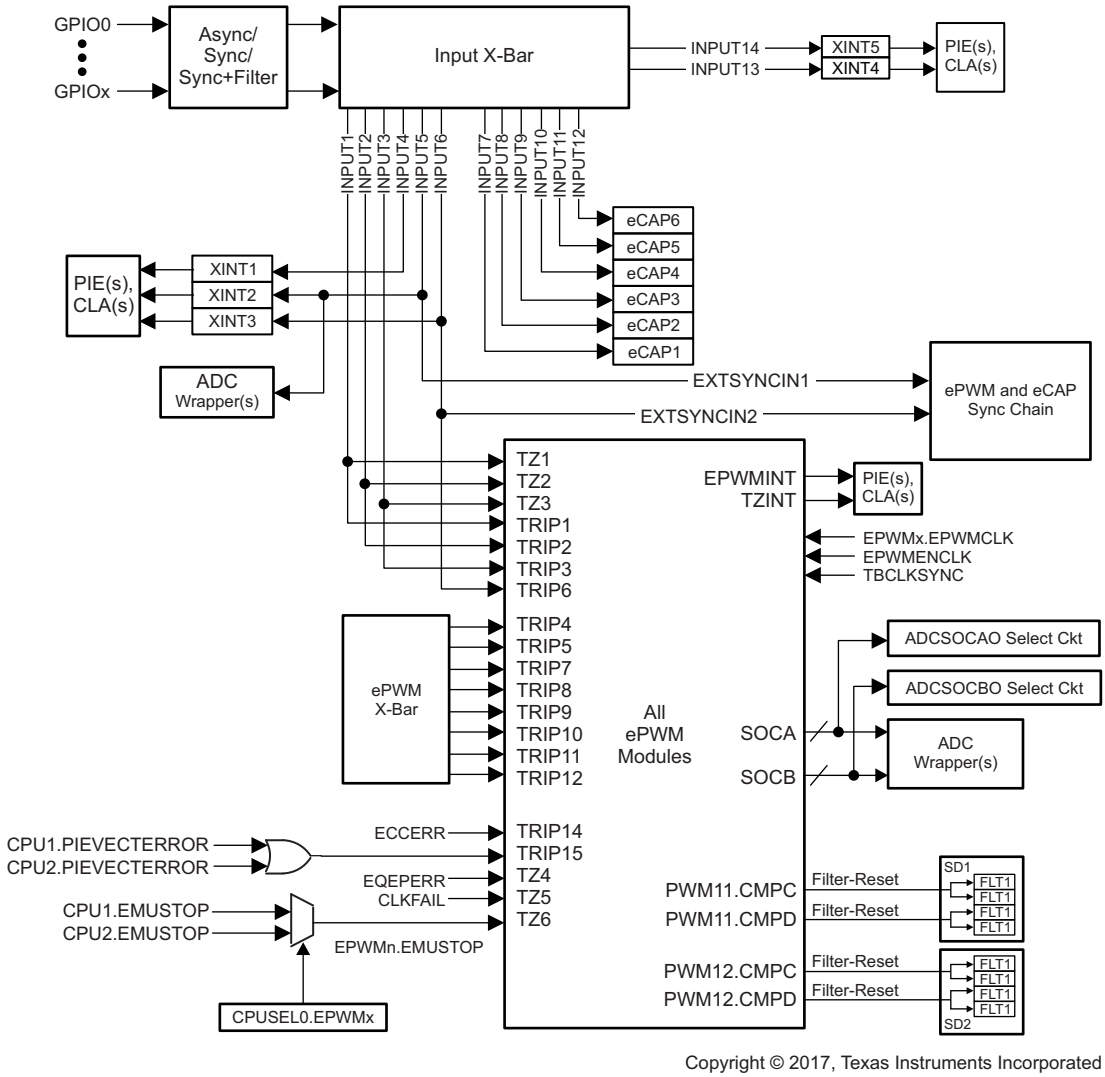


図 4-49. ePWM Trip Input Connectivity

4.9.2.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization chain on the device provides flexibility in partitioning the ePWM and eCAP modules between CPU1 and CPU2 and allows localized synchronization within the modules belonging to the same CPU. Like the other peripherals, the partitioning of the ePWM and eCAP modules needs to be done using the CPUSELx registers. 図 4-50 shows the synchronization chain architecture.

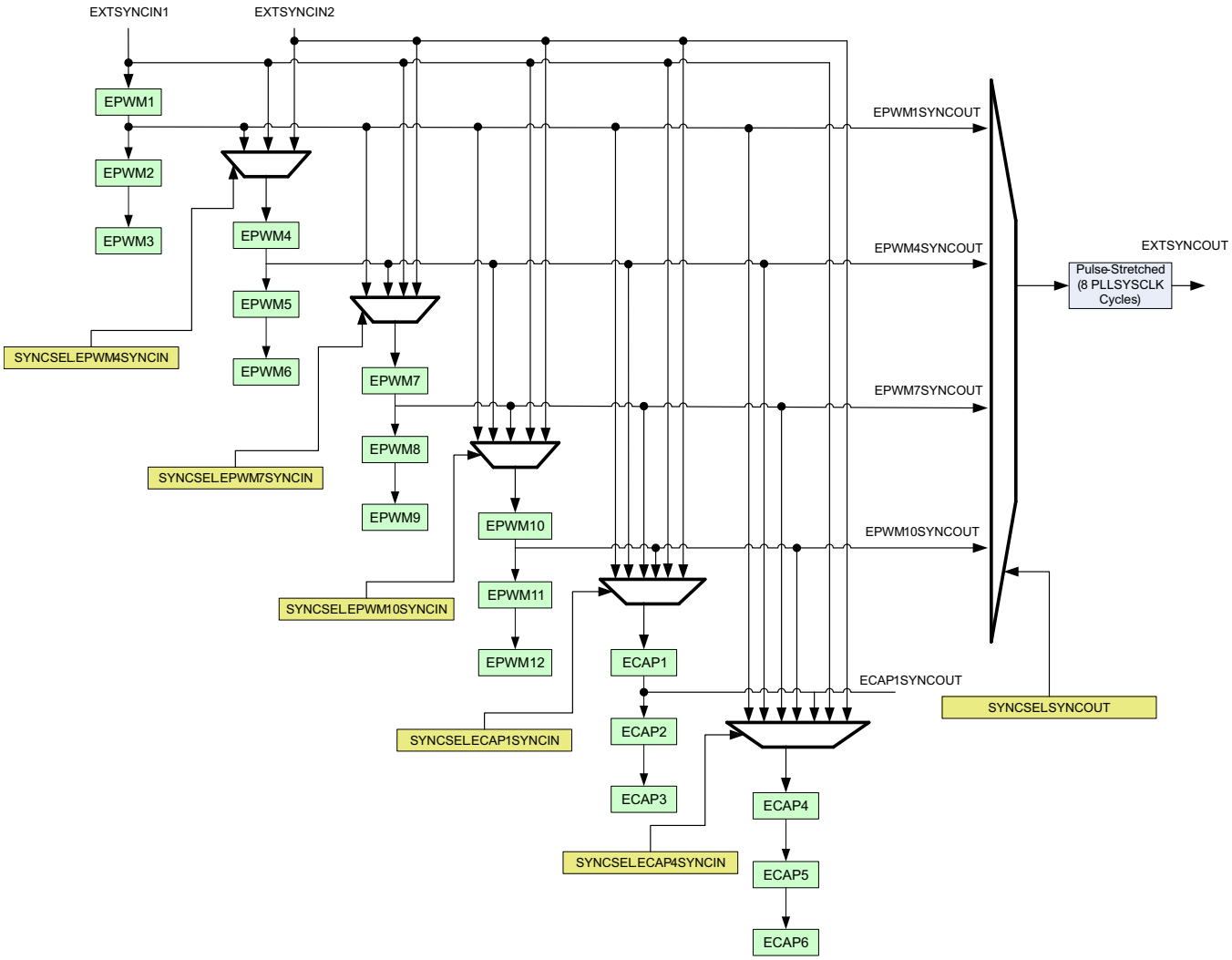


図 4-50. Synchronization Chain Architecture

4.9.2.2 ePWM Electrical Data and Timing

Table 4-57 shows the PWM timing requirements and Table 4-58 shows the PWM switching characteristics.

Table 4-57. ePWM Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.

Table 4-58. ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		25	ns

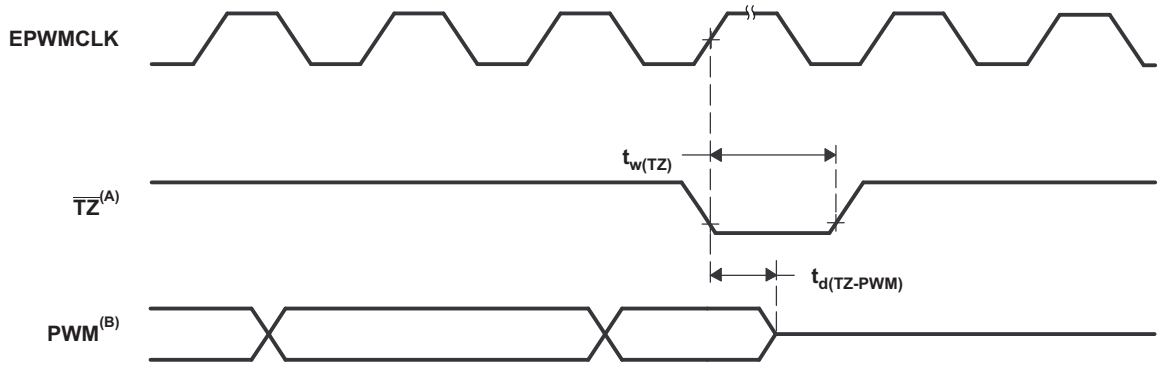
4.9.2.2.1 Trip-Zone Input Timing

Table 4-59 shows the trip-zone input timing requirements. Figure 4-51 shows the PWM Hi-Z characteristics.

Table 4-59. Trip-Zone Input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 4-51. PWM Hi-Z Characteristics

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4.9.2.3 External ADC Start-of-Conversion Electrical Data and Timing

表 4-60 shows the external ADC start-of-conversion switching characteristics. 図 4-52 shows the ADCSOCAO or ADCSOCBO timing.

表 4-60. External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, ADCSOCxO low	$32t_{c(SYSCLK)}$		cycles

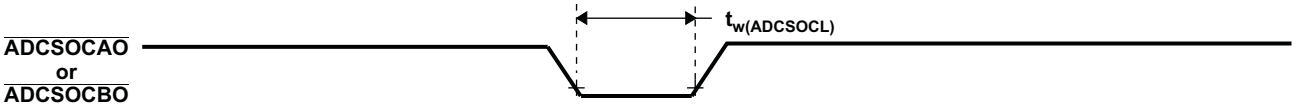


図 4-52. ADCSOCAO or ADCSOCBO Timing

4.9.3 Enhanced Quadrature Encoder Pulse (eQEP)

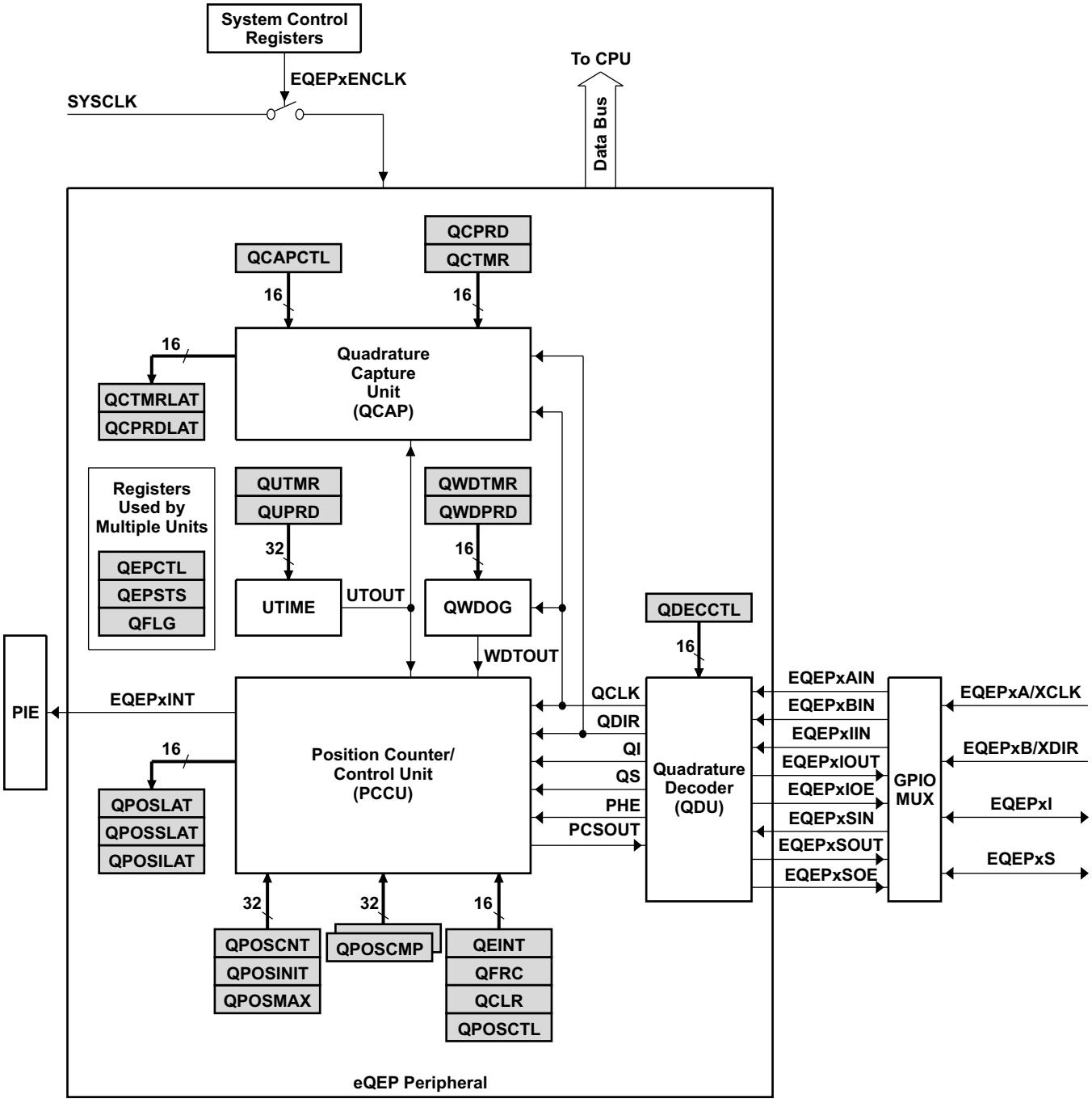
The eQEP module interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position-control systems.

Each eQEP peripheral comprises five major functional blocks:

- Quadrature Capture Unit (QCAP)
- Position Counter/Control Unit (PCCU)
- Quadrature Decoder Unit (QDU)
- Unit Time Base for speed and frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)

The eQEP peripherals are clocked by PERx.SYSCLK. 図 4-53 shows the eQEP block diagram.

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図 4-53. eQEP Block Diagram

4.9.3.1 eQEP Electrical Data and Timing

Table 4-61 lists the eQEP timing requirement and Table 4-62 lists the eQEP switching characteristics.

Table 4-61. eQEP Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 4-24.
(2) See the *TMS320F2837xD Dual-Core Delfino™ MCUs Silicon Errata* for limitations in the asynchronous mode.

Table 4-62. eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$4t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$6t_{c(SYSCLK)}$	cycles

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4.9.4 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

注

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

4.9.4.1 HRPWM Electrical Data and Timing

Table 4-63 lists the high-resolution PWM switching characteristics.

Table 4-63. High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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4.9.5 Sigma-Delta Filter Module (SDFM)

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta ($\Sigma\Delta$) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for overcurrent and undercurrent monitoring. 図 4-54 shows a block diagram of the SDFMs.

SDFM features include:

- Eight external pins per SDFM module:
  - Four sigma-delta data input pins per SDFM module (SDx_Dy, where x = 1 to 2 and y = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SDx_Cy, where x = 1 to 2 and y = 1 to 4)
- Four different configurable modulator clock modes:
  - Modulator clock rate equals modulator data rate
  - Modulator clock rate running at half the modulator data rate
  - Modulator data is Manchester encoded. Modulator clock not required.
  - Modulator clock rate is double that of modulator data rate
- Four independent configurable comparator units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to detect over-value and under-value conditions
  - Comparator Over-Sampling Ratio (COSR) value for comparator programmable from 1 to 32
- Four independent configurable data filter units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Data filter Over-Sampling Ratio (DOSR) value for data filter unit programmable from 1 to 256
  - Ability to enable or disable individual filter module
  - Ability to synchronize all four independent filters of a SDFM module using the Master Filter Enable (MFE) bit or the PWM signals.
- Filter data can be 16-bit or 32-bit representation
- PWMs can be used to generate modulator clock for sigma-delta modulators

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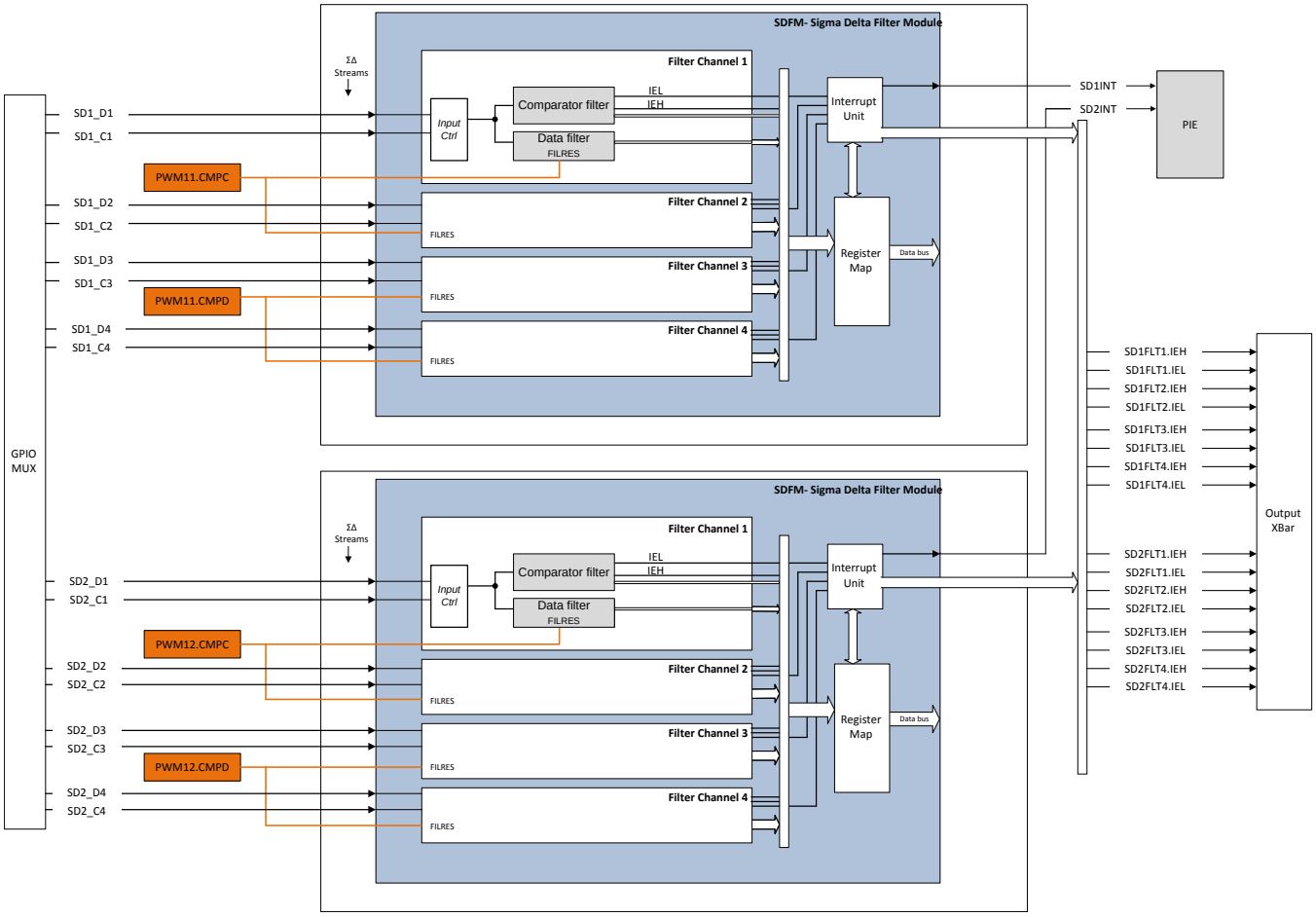


図 4-54. SDFM Block Diagram

4.9.5.1 SDFM Electrical Data and Timing

Table 4-64 shows the SDFM timing requirements. Figure 4-55 through Figure 4-58 show the SDFM timing diagrams.

Table 4-64. SDFM Timing Requirements

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	40	256 * SYSCLK period	ns
$t_{w(SDCH)M0}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M0}$ – 10	ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns
Mode 1				
$t_{c(SDC)M1}$	Cycle time, SDx_Cy	80	256 * SYSCLK period	ns
$t_{w(SDCH)M1}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M1}$ – 10	ns
$t_{su(SDDV-SDCL)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes low	5		ns
$t_{su(SDDV-SDCH)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCL-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes low	5		ns
$t_{h(SDCH-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns
Mode 2				
$t_{c(SDD)M2}$	Cycle time, SDx_Dy	8 * $t_{c(SYSCLK)}$	20 * $t_{c(SYSCLK)}$	ns
$t_{w(SDDH)M2}$	Pulse duration, SDx_Dy high	10		ns
Mode 3				
$t_{c(SDC)M3}$	Cycle time, SDx_Cy	40	256 * SYSCLK period	ns
$t_{w(SDCH)M3}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M3}$ – 5	ns
$t_{su(SDDV-SDCH)M3}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M3}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns

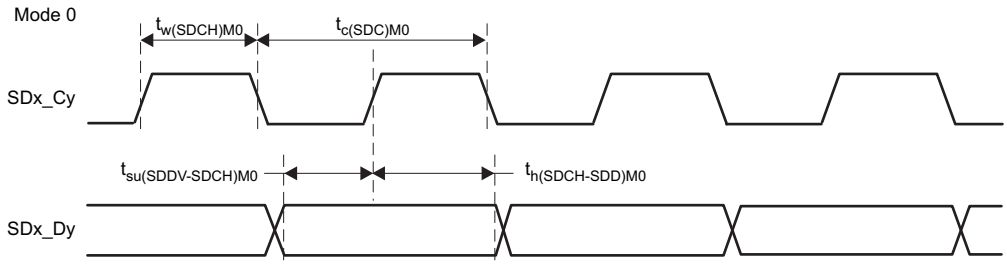


Figure 4-55. SDFM Timing Diagram – Mode 0

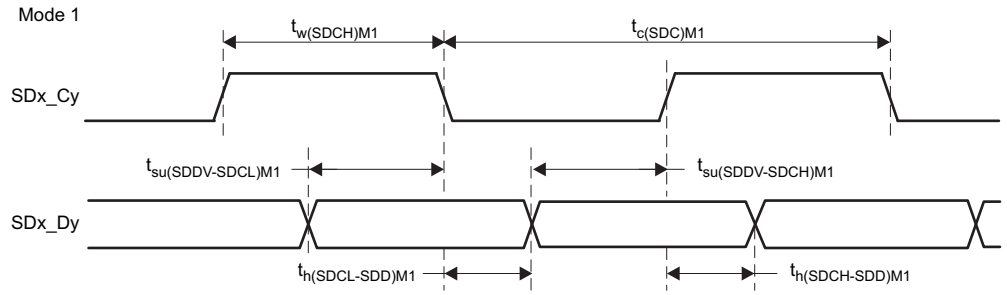


Figure 4-56. SDFM Timing Diagram – Mode 1

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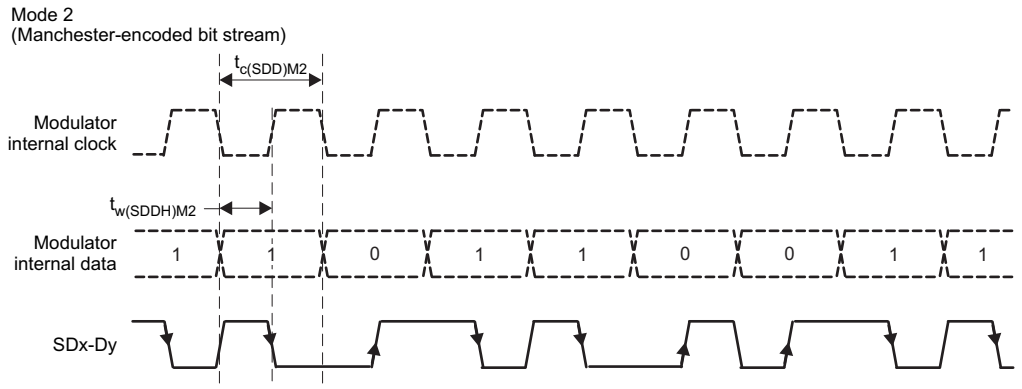


Figure 4-57. SDFM Timing Diagram – Mode 2

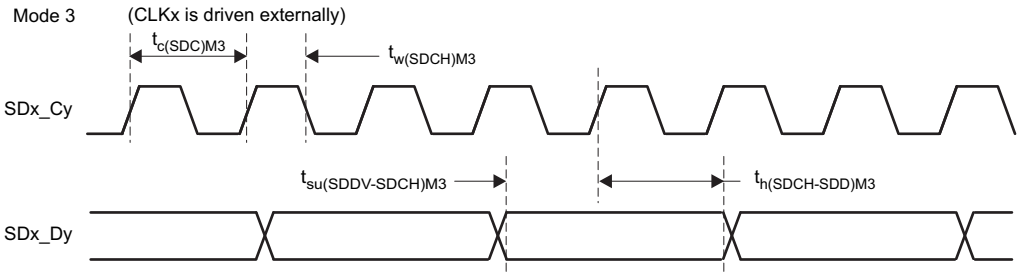


Figure 4-58. SDFM Timing Diagram – Mode 3

4.10 Communications Peripherals

4.10.1 Controller Area Network (CAN)

注

The CAN module uses the IP known as *D_CAN*. This document uses the names *CAN* and *D_CAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO 11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Programmable receive and identifier masks for each object
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for receive message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM parity check mechanism
- Two interrupt lines
- Global power down and wakeup support

注

For a CANx Bit-CLK of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

注

The accuracy of the on-chip zero-pin oscillator is in 表 4-18, Internal Oscillator Electrical Characteristics. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

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4.10.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

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図 4-59 shows how the I2C peripheral module interfaces within the device.

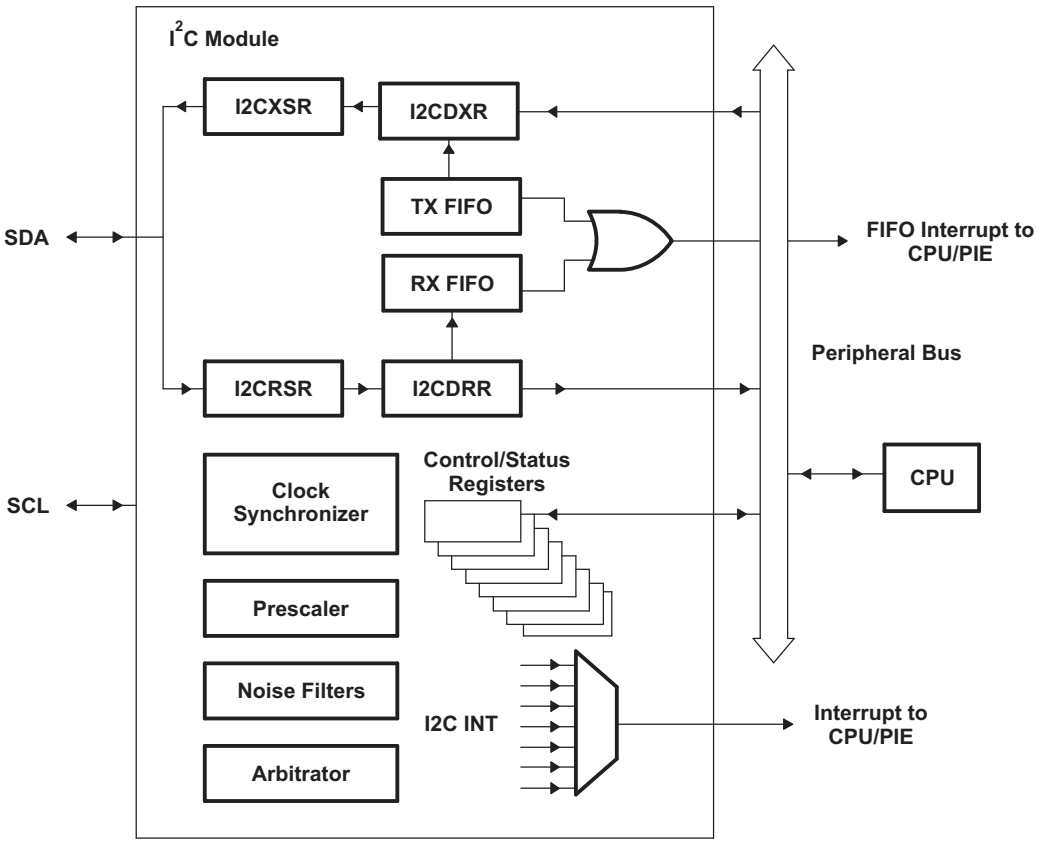


図 4-59. I2C Peripheral Module Interfaces

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4.10.2.1 I2C Electrical Data and Timing

Table 4-65 shows the I2C timing requirements. Table 4-66 shows the I2C switching characteristics.

Table 4-65. I2C Timing Requirements

			MIN	MAX	UNIT
$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall		0.6		µs
$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay		0.6		µs
$t_{h(SCL-DAT)}$	Hold time, data after SCL fall		0		µs
$t_{su(DAT-SCL)}$	Setup time, data before SCL rise		100		ns
$t_{r(SDA)}$	Rise time, SDA	Input tolerance	20	300	ns
$t_{r(SCL)}$	Rise time, SCL	Input tolerance	20	300	ns
$t_{f(SDA)}$	Fall time, SDA	Input tolerance	11.4	300	ns
$t_{f(SCL)}$	Fall time, SCL	Input tolerance	11.4	300	ns
$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay		0.6		µs

Table 4-66. I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		0	400	kHz
$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by the input filter		0	50	ns
t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
V_{IL}	Valid low-level input voltage		–0.3	0.3 * V_{DDIO}	V
V_{IH}	Valid high-level input voltage		0.7 * V_{DDIO}	V_{DDIO} + 0.3	V
V_{OL}	Low-level output voltage	Sinking 3 mA	0	0.4	V
I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA

NOTE

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured between 7 MHz to 12 MHz.

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4.10.3 Multichannel Buffered Serial Port (McBSP)

The McBSP module has the following features:

- Compatible with McBSP in TMS320C28x and TMS320F28x DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- 8-bit data transfer mode can be configured to transmit with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Supports AC97, I2S, and SPI protocols
- McBSP clock rate,

$$CLKG = \frac{CLKSRG}{(1 + CLKGDV)}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR.

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図 4-60 shows the block diagram of the McBSP module.

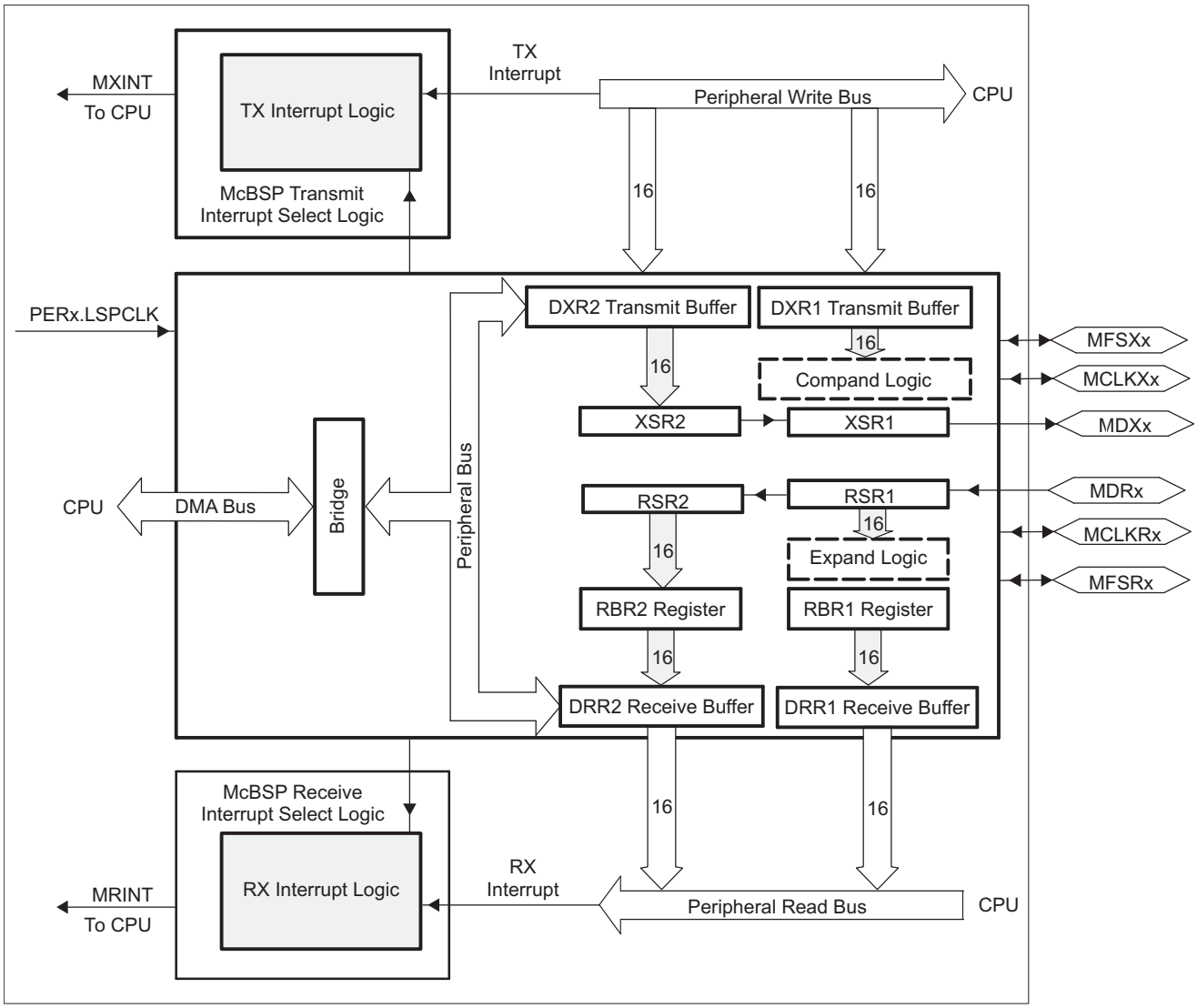


図 4-60. McBSP Block Diagram

4.10.3.1 McBSP Electrical Data and Timing

4.10.3.1.1 McBSP Transmit and Receive Timing

Table 4-67 shows the McBSP timing requirements. Table 4-68 shows the McBSP switching characteristics. Figure 4-61 and Figure 4-62 show the McBSP timing diagrams.

Table 4-67. McBSP Timing Requirements(1) (2)

NO.				MIN	MAX	UNIT
	McBSP module clock (CLKG, CLKX, CLKR) range			1		kHz
					25	MHz
	McBSP module cycle time (CLKG, CLKX, CLKR) range			40		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P – 7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18		ns
			CLKR ext	5		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	3		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	18		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = CLKSRG / (1 + CLKGDV). CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLK/2).

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Table 4-68. McBSP Switching Characteristics(1) (2)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D – 5 (3)	D + 5 (3)	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C – 5 (3)	C + 5 (3)	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	0	4	ns
				CLKR ext	3	27	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	0	4	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int		8	ns
				CLKX ext		14	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int		9	ns
				CLKX ext		28	
		Delay time, CLKX high to DX valid	DXENA = 0	CLKX int		8	
				CLKX ext		14	
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int		P + 8	
				CLKX ext		P + 14	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven	DXENA = 0	CLKX int	0		ns
				CLKX ext	6		
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P		
				CLKX ext	P + 6		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid	DXENA = 0	FSX int		8	ns
				FSX ext		14	
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 1	FSX int		P + 8	
				FSX ext		P + 14	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven	DXENA = 0	FSX int	0		ns
				FSX ext	6		
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 1	FSX int	P		
				FSX ext	P + 6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns.
(3) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

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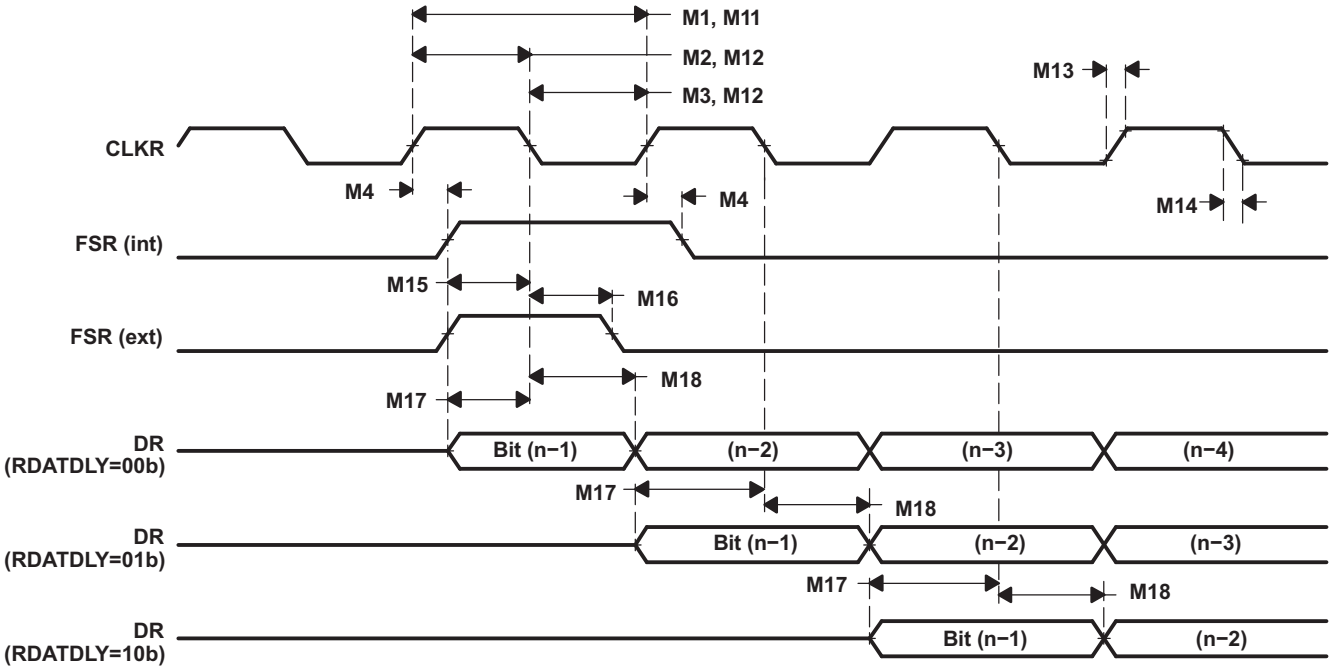


Figure 4-61. McBSP Receive Timing

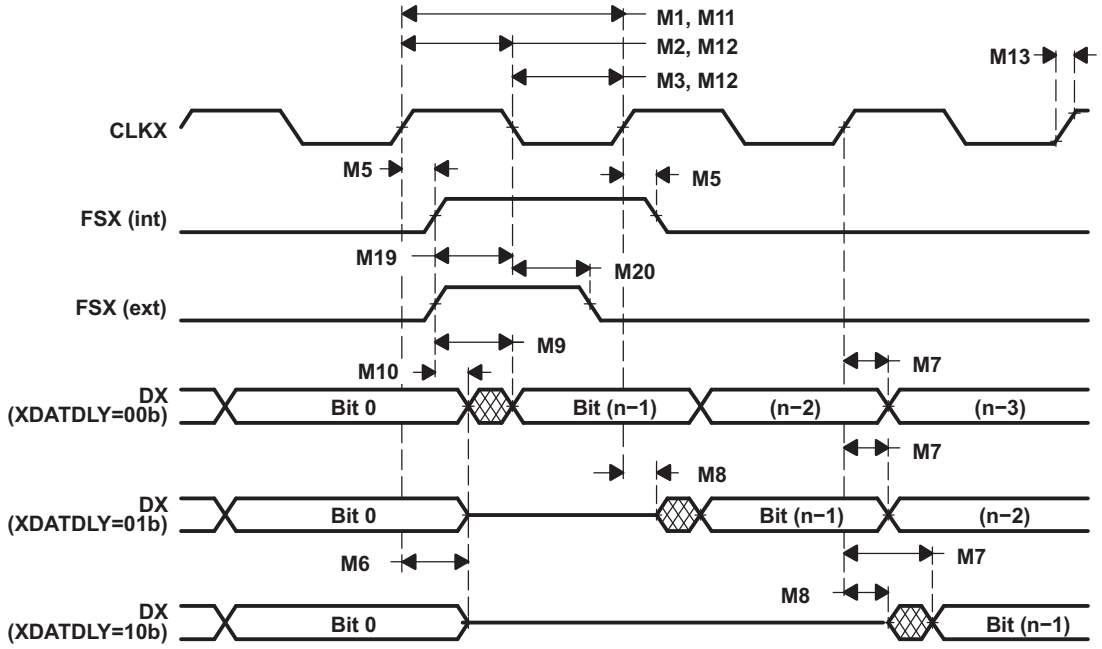


Figure 4-62. McBSP Transmit Timing

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4.10.3.1.2 McBSP as SPI Master or Slave Timing

For CLKSTP = 10b and CLKXP = 0, Table 4-69 shows the timing requirements, Table 4-70 shows the switching characteristics, and Figure 4-63 shows the timing diagram.

Table 4-69. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)(1)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high			8P + 10		ns
M33	$t_{c(CKX)}$	Cycle time, CLKX	2P(2)		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 4-70. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M24	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	2P(1)				ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P				ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

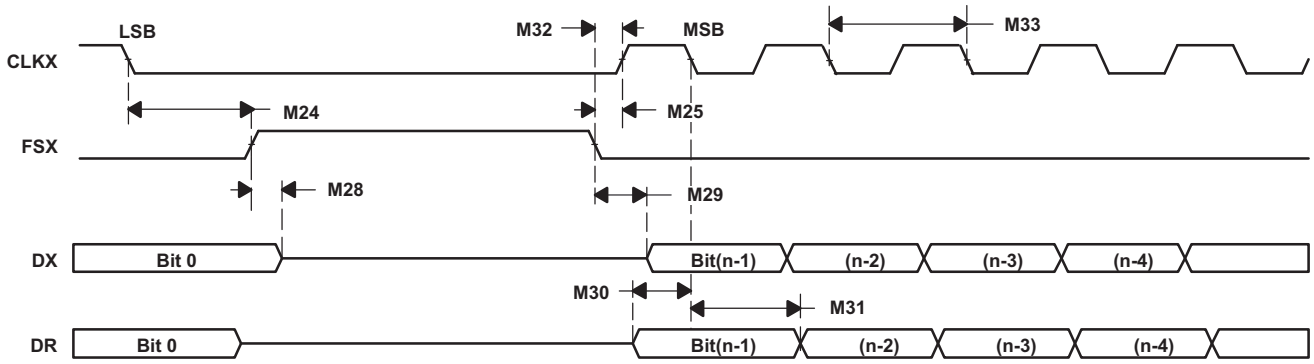


Figure 4-63. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

For CLKSTP = 11b and CLKXP = 0, Table 4-71 shows the timing requirements, Table 4-72 shows the switching characteristics, and Figure 4-64 shows the timing diagram.

Table 4-71. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)(1)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high			16P + 10		ns
M42	$t_{c(CKX)}$	Cycle time, CLKX	2P(2)		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 4-72. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M34	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	P				ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	2P(1)				ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P + 6		7P + 6		ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

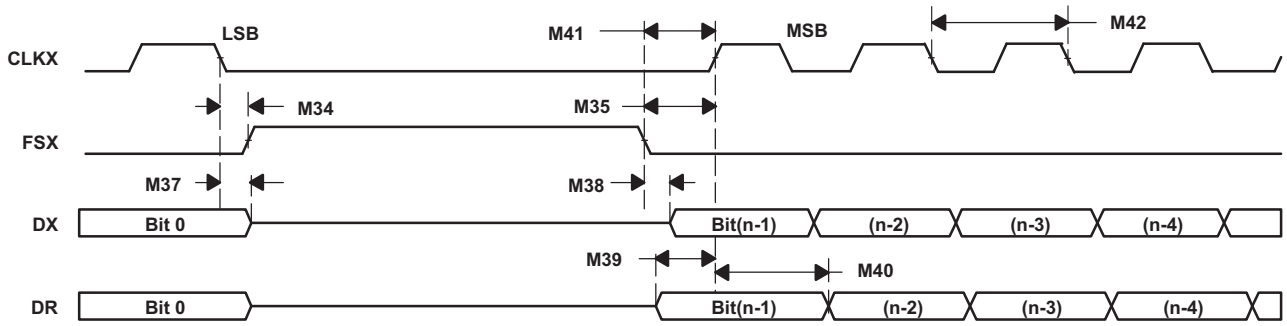


Figure 4-64. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

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For CLKSTP = 10b and CLKXP = 1, Table 4-73 shows the timing requirements, Table 4-74 shows the switching characteristics, and Figure 4-65 shows the timing diagram.

Table 4-73. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)(1)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			8P + 10		ns
M52	$t_{c(CKX)}$	Cycle time, CLKX	2P(2)		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 4-74. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M43	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	2P(1)				ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	P				ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

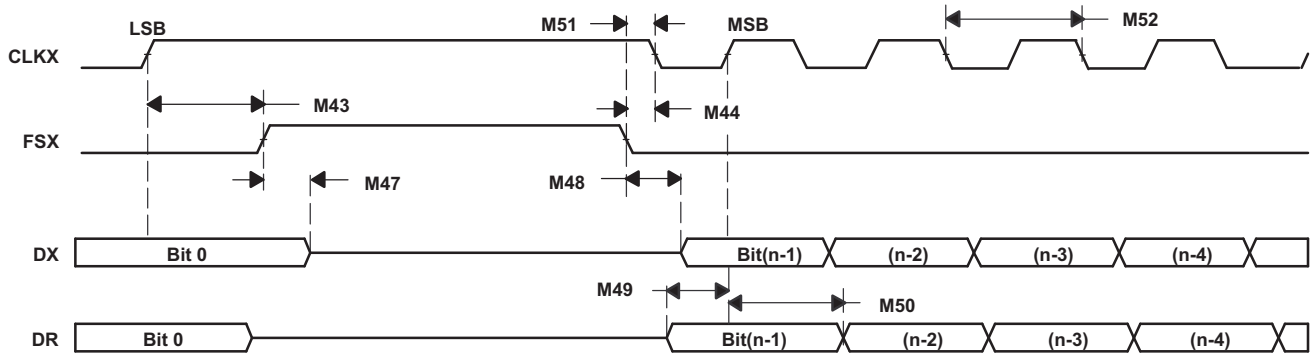


Figure 4-65. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

For CLKSTP = 11b and CLKXP = 1, Table 4-75 shows the timing requirements, Table 4-76 shows the switching characteristics, and Figure 4-66 shows the timing diagram.

Table 4-75. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)(1)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			16P + 10		ns
M61	$t_{c(CKX)}$	Cycle time, CLKX	2P(2)		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

Table 4-76. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)(1)

NO.	PARAMETER		MASTER(2)		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M53	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	P				ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	2P(1)				ns
M55	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	0	3P + 6	5P + 20	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P + 6		7P + 6		ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG
(2) C = CLKX low pulse width = P
D = CLKX high pulse width = P

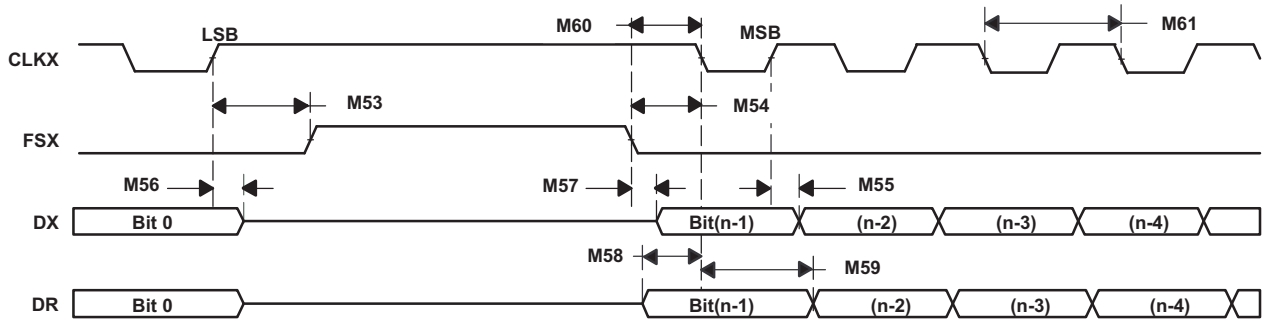


Figure 4-66. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

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4.10.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register. 図 4-67 shows the SCI block diagram.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates
- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wakeup multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

注

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

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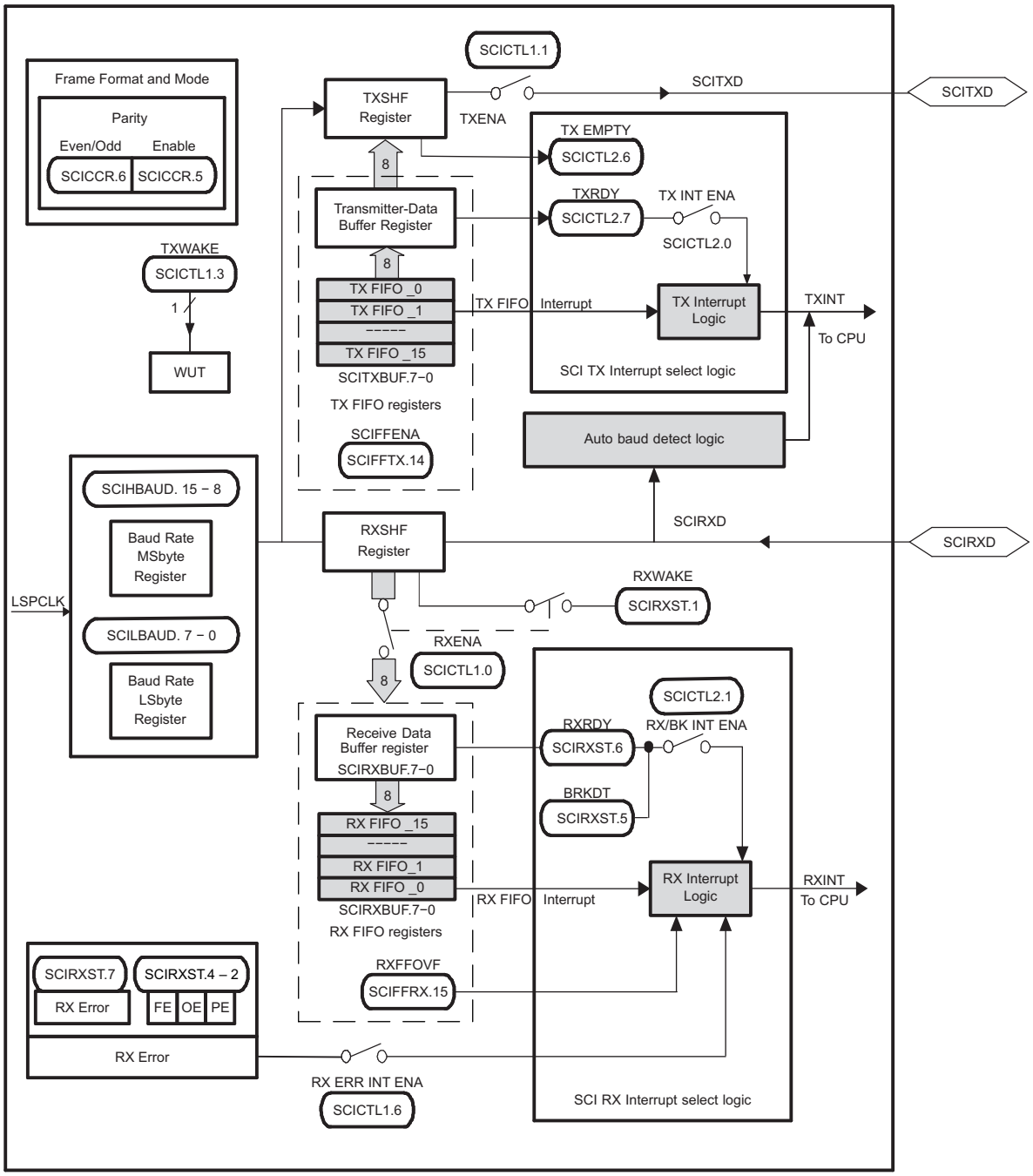


図 4-67. SCI Block Diagram

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The major elements used in full-duplex operation include:

- A transmitter (TX) and its major registers:
  - SCITXBUF register – Transmitter Data Buffer register. Contains data (loaded by the CPU) to be transmitted
  - TXSHF register – Transmitter Shift register. Accepts data from the SCITXBUF register and shifts data onto the SCITXD pin, 1 bit at a time
- A receiver (RX) and its major registers:
  - RXSHF register – Receiver Shift register. Shifts data in from the SCIRXD pin, 1 bit at a time
  - SCIRXBUF register – Receiver Data Buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into the RXSHF register and then into the SCIRXBUF and SCIRXEMU registers
- A programmable baud generator
- Data-memory-mapped control and status registers enable the CPU to access the I2C module registers and FIFOs.

The SCI receiver and transmitter operate independently.

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4.10.5 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The port supports 16-level receive and transmit FIFOs for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules
- DMA support
- High-speed mode for up to 50-MHz full-duplex communication

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The SPI operates in master or slave mode. The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICTL.3) is high, data is transmitted and received a half-cycle before the SPICLK transition. As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data
- Master sends data; slave sends data
- Master sends dummy data; slave sends data

The master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

図 4-68 shows the SPI CPU Interface.

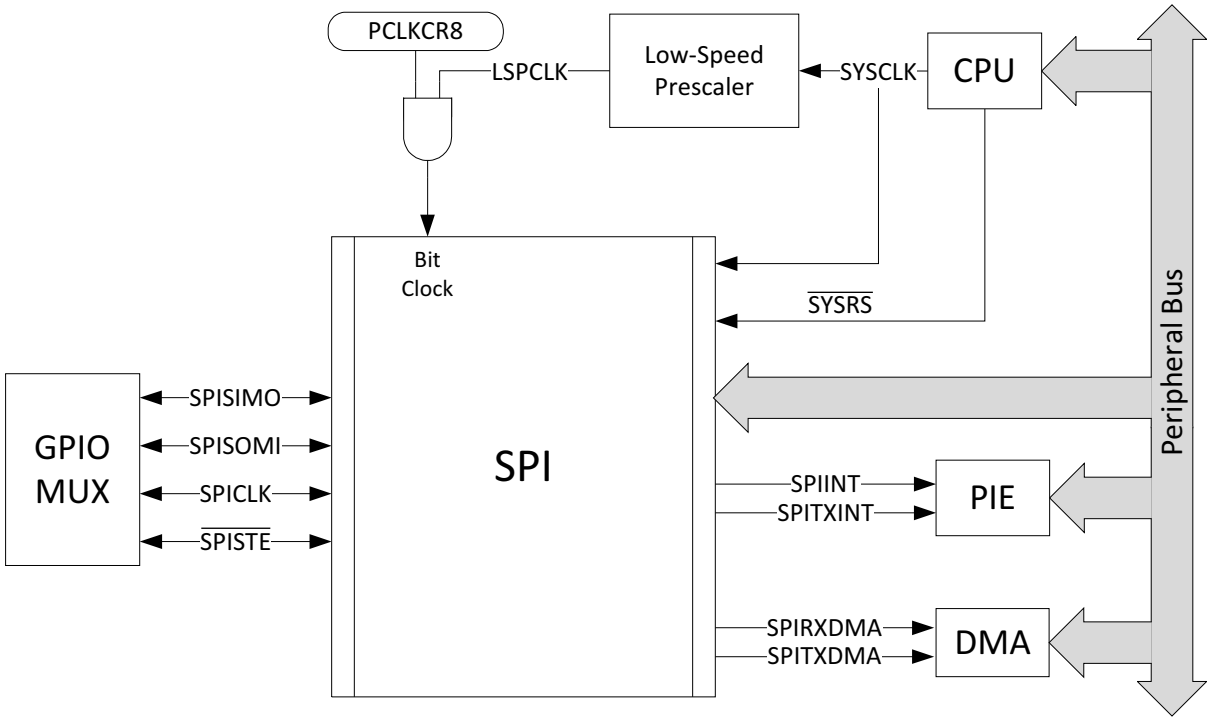


図 4-68. SPI CPU Interface

4.10.5.1 SPI Electrical Data and Timing

The following sections contain the SPI External Timings in Non-High-Speed Mode:

4.10.5.1.1 Non-High-Speed Master Mode Timings
4.10.5.1.2 Non-High-Speed Slave Mode Timings

The following sections contain the SPI External Timings in High-Speed Mode:

4.10.5.1.3 High-Speed Master Mode Timings
4.10.5.1.4 High-Speed Slave Mode Timings

注

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

To use the SPI in High-Speed mode, the application must use the high-speed enabled GPIOs (see Section 3.4.5).

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4.10.5.1.1 Non-High-Speed Master Mode Timings

Table 4-77 lists the SPI master mode switching characteristics where the clock phase = 0. 図 4-69 shows the SPI master mode external timing where the clock phase = 0.

Table 4-78 lists the SPI master mode switching characteristics where the clock phase = 1. 図 4-70 shows the SPI master mode external timing where the clock phase = 1.

Table 4-79 lists the SPI master mode timing requirements.

Table 4-77. SPI Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		3	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	Even	$t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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Table 4-78. SPI Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$	
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	Even, Odd	$t_{c(SPC)M} - 3$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

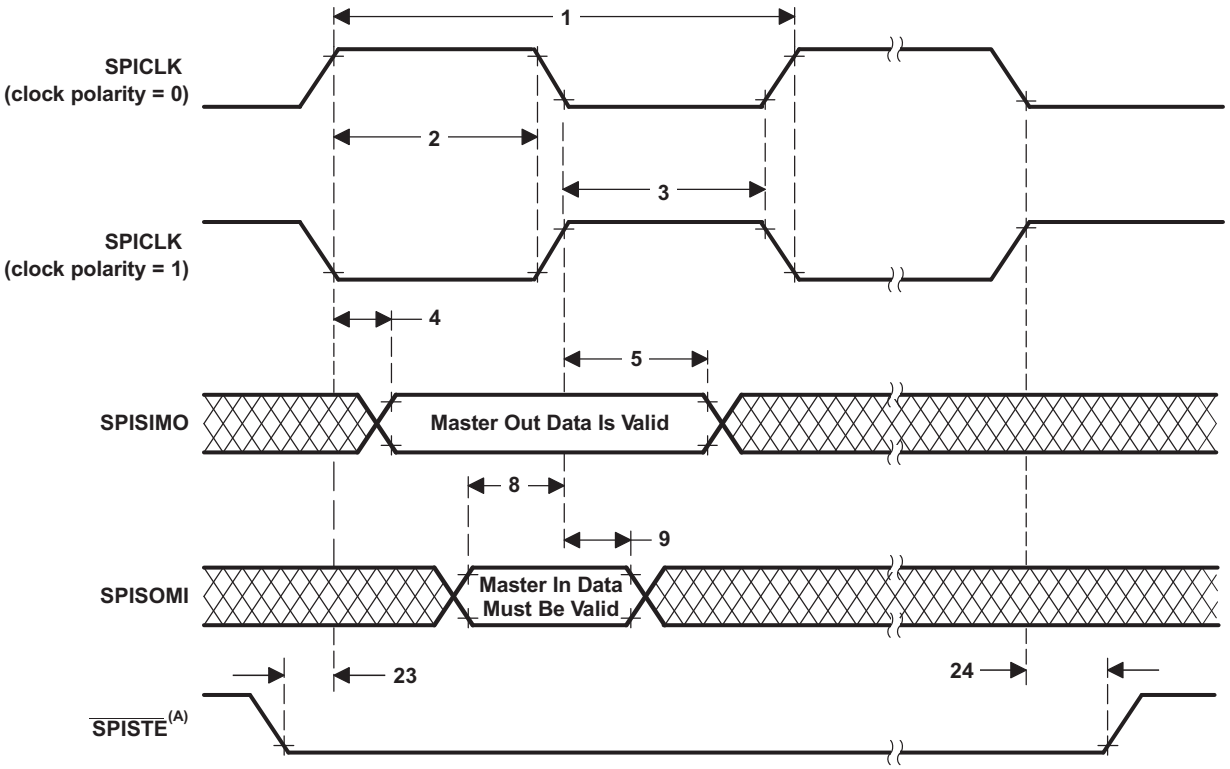
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

Table 4-79. SPI Master Mode Timing Requirements

NO.			(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	20		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	0		ns

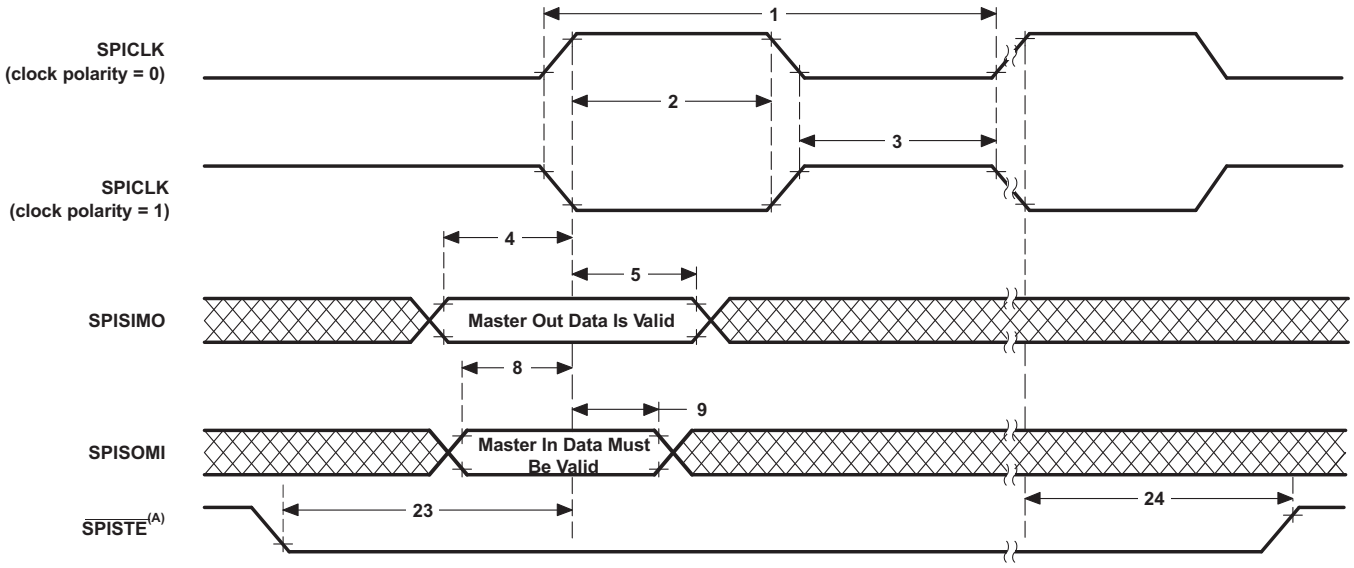
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

図 4-69. SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

図 4-70. SPI Master Mode External Timing (Clock Phase = 1)

4.10.5.1.2 Non-High-Speed Slave Mode Timings

Table 4-80 lists the SPI slave mode switching characteristics. Table 4-81 lists the SPI slave mode timing requirements.

図 4-71 shows the SPI slave mode external timing where the clock phase = 0. 図 4-72 shows the SPI slave mode external timing where the clock phase = 1.

Table 4-80. SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		20	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns

Table 4-81. SPI Slave Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

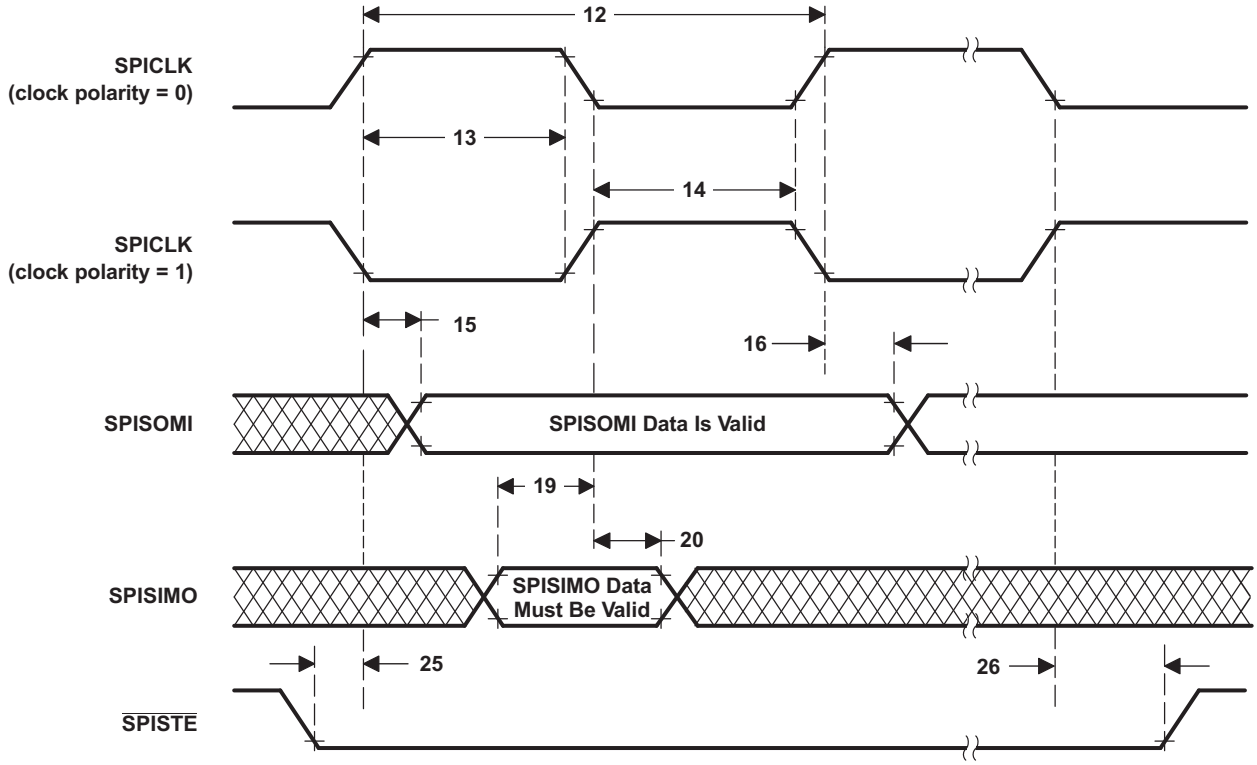


図 4-71. SPI Slave Mode External Timing (Clock Phase = 0)

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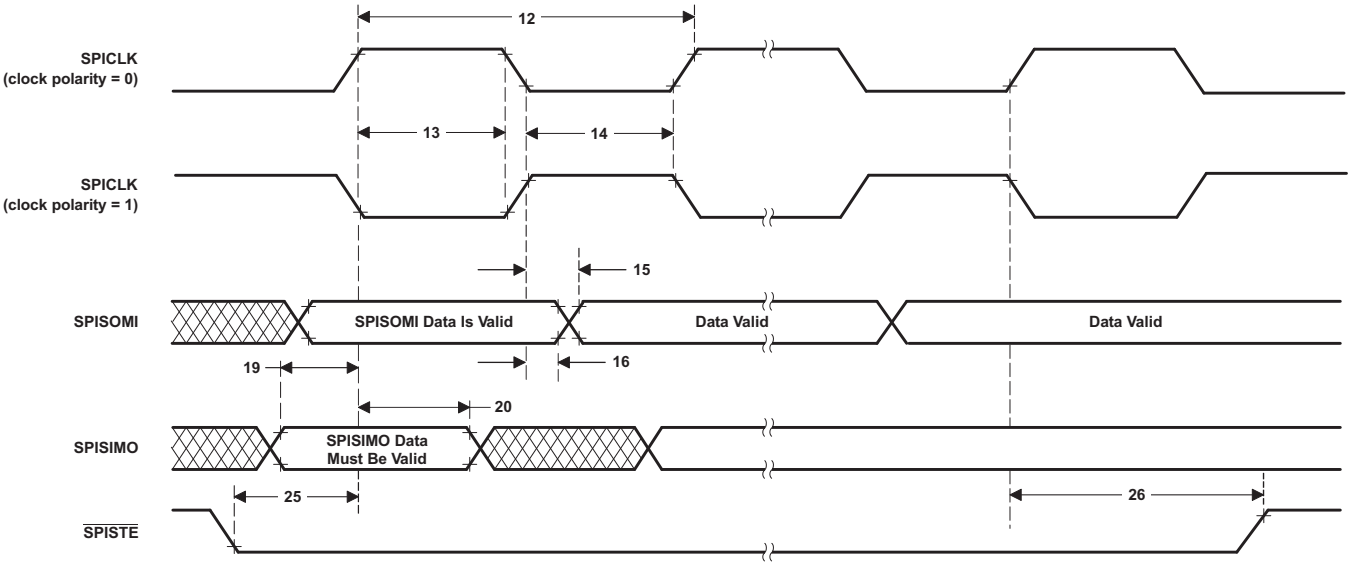


図 4-72. SPI Slave Mode External Timing (Clock Phase = 1)

4.10.5.1.3 High-Speed Master Mode Timings

Table 4-82 lists the SPI high-speed master mode switching characteristics where the clock phase = 0. 図 4-73 shows the high-speed SPI master mode external timing where the clock phase = 0.

Table 4-83 lists the SPI high-speed master mode switching characteristics where the clock phase = 1. 図 4-74 shows the high-speed SPI master mode external timing where the clock phase = 1.

Table 4-84 lists the SPI high-speed master mode timing requirements.

Table 4-82. SPI High-Speed Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		1	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ active to SPICLK	Even	$t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{SPISTE}$ inactive	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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Table 4-83. SPI High-Speed Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	Even, Odd	$t_{c(SPC)M} - 1$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		

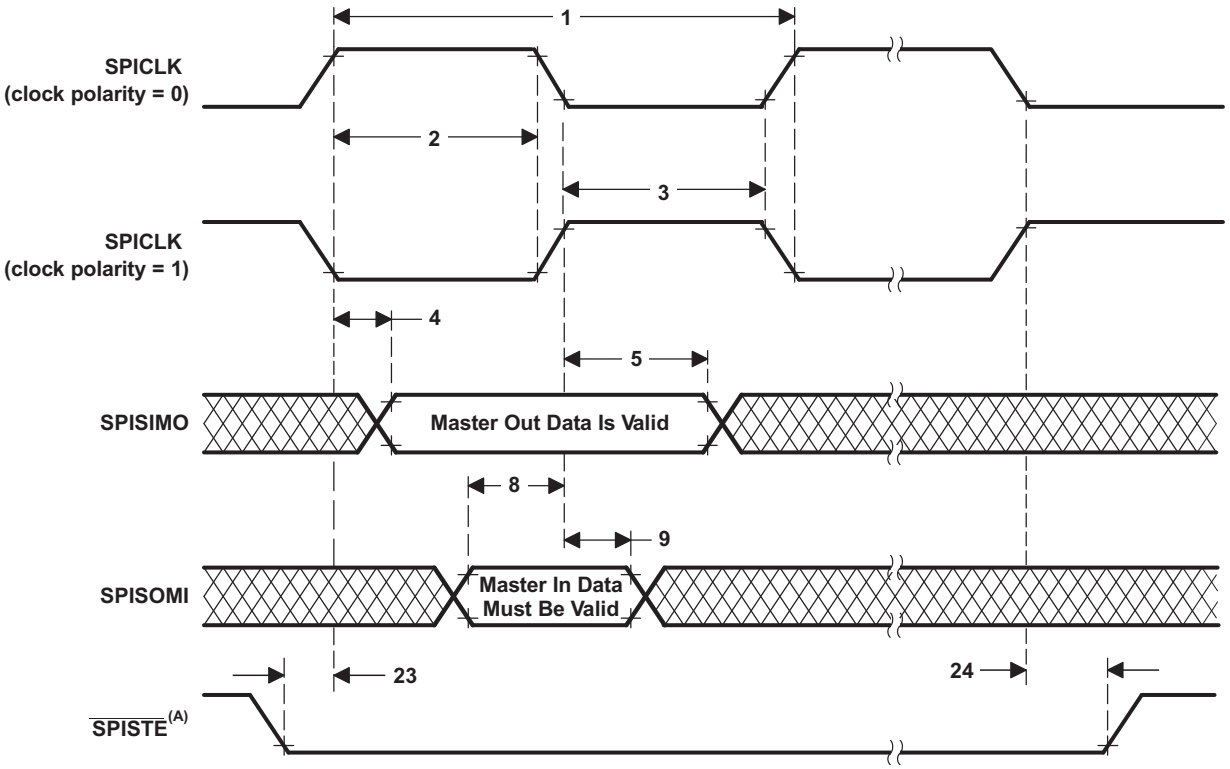
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

Table 4-84. SPI High-Speed Master Mode Timing Requirements

NO.			(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	5		ns

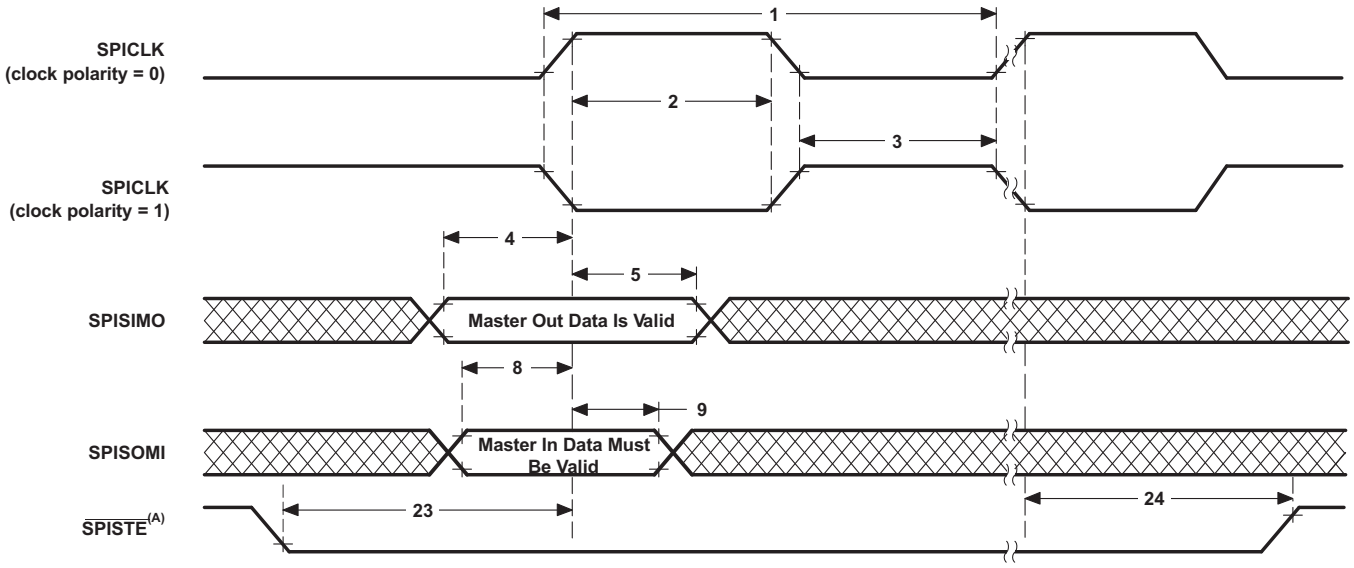
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

図 4-73. High-Speed SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

図 4-74. High-Speed SPI Master Mode External Timing (Clock Phase = 1)

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4.10.5.1.4 High-Speed Slave Mode Timings

Table 4-85 lists the SPI high-speed slave mode switching characteristics. Table 4-86 lists the SPI high-speed slave mode timing requirements.

図 4-75 shows the high-speed SPI slave mode external timing where the clock phase = 0. 図 4-76 shows the high-speed SPI slave mode external timing where the clock phase = 1.

Table 4-85. SPI High-Speed Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		9	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns

Table 4-86. SPI High-Speed Slave Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

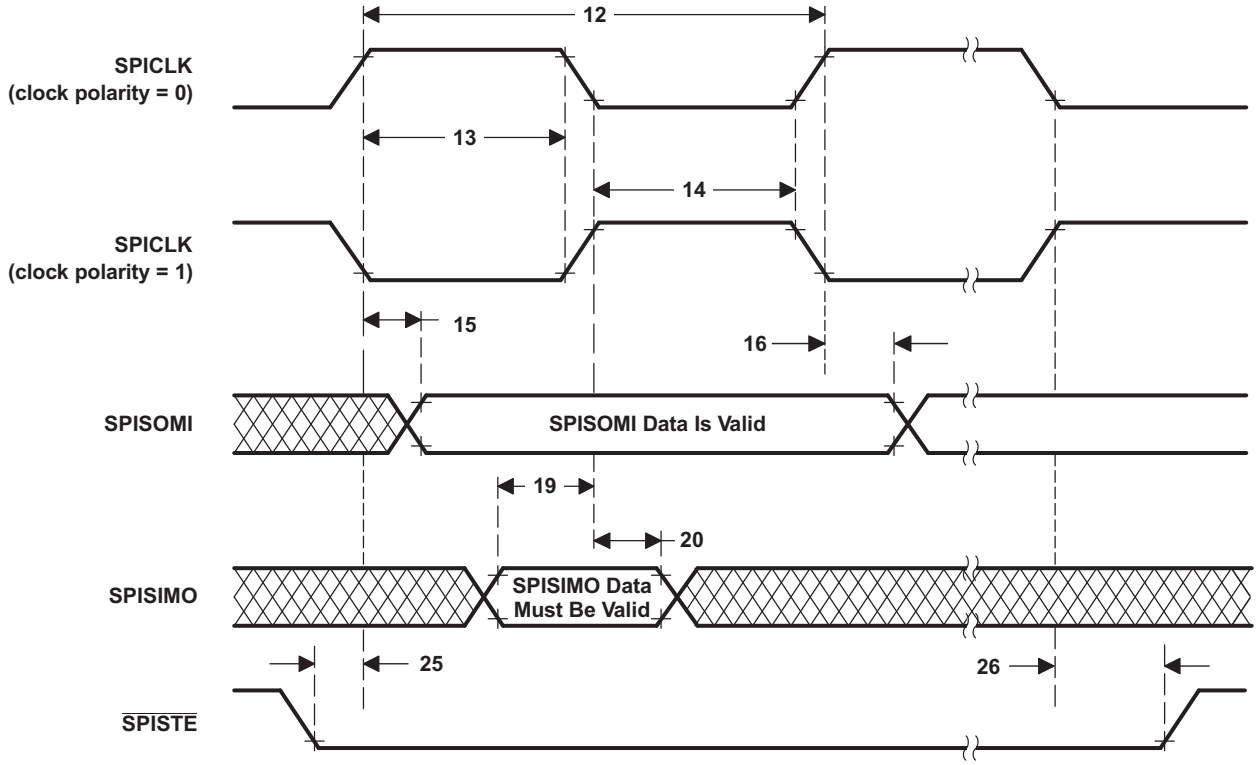


図 4-75. High-Speed SPI Slave Mode External Timing (Clock Phase = 0)

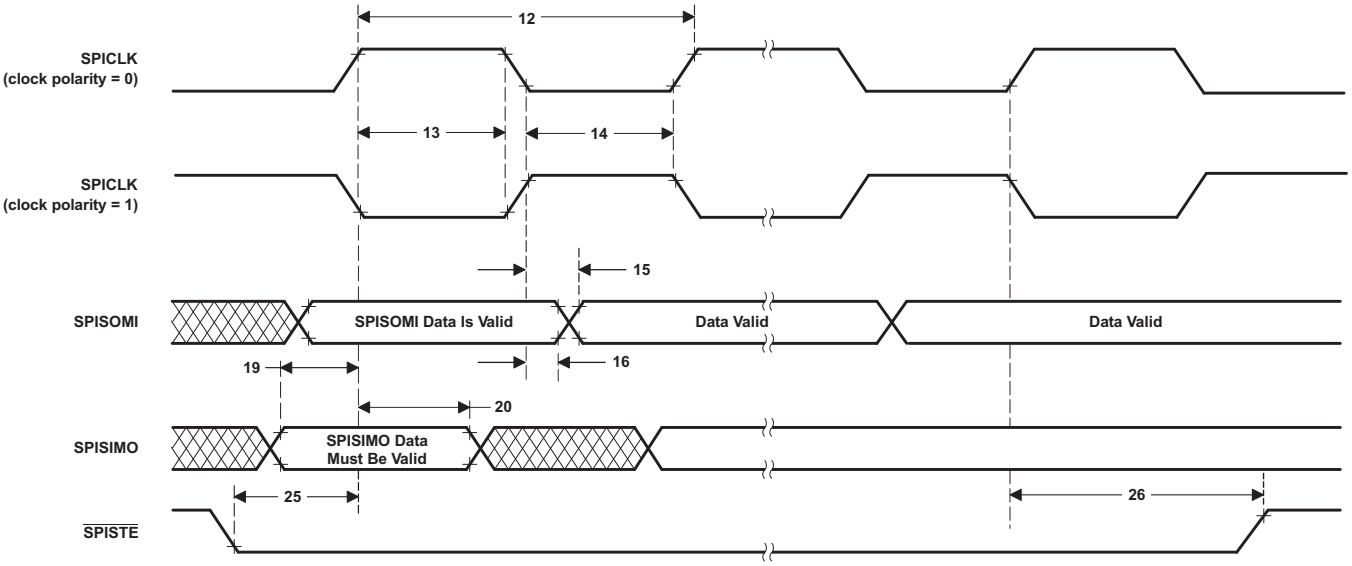


図 4-76. High-Speed SPI Slave Mode External Timing (Clock Phase = 1)

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4.10.6 Universal Serial Bus (USB) Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) operation
- Integrated PHY
- Three transfer types: control, interrupt, and bulk
- 32 endpoints
  - One dedicated control IN endpoint and one dedicated control OUT endpoint
  - 15 configurable IN endpoints and 15 configurable OUT endpoints
- 4KB of dedicated endpoint memory

図 4-77 shows the USB block diagram.

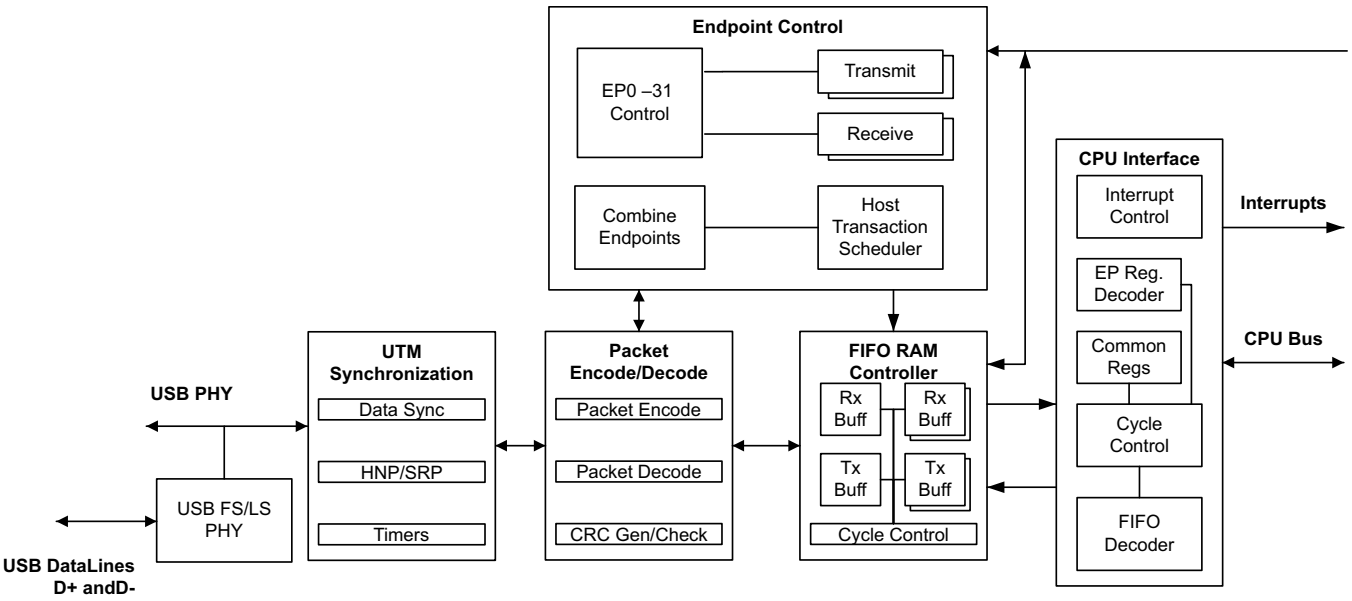


図 4-77. USB Block Diagram

注

The accuracy of the on-chip zero-pin oscillator (表 4-18, Internal Oscillator Electrical Characteristics) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB. For applications using the USB boot mode, see 5.10 (Boot ROM and Peripheral Booting) for clock frequency requirements.

4.10.6.1 USB Electrical Data and Timing

Table 4-87 shows the USB input ports DP and DM timing requirements. Table 4-88 shows the USB output ports DP and DM switching characteristics.

Table 4-87. USB Input Ports DP and DM Timing Requirements

		MIN	MAX	UNIT
V(CM)	Differential input common mode range	0.8	2.5	V
Z(IN)	Input impedance	300		kΩ
VCRS	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic-low level	0.8		V
V_{IH}	Static SE input logic-high level		2.0	V
VDI	Differential input voltage		0.2	V

Table 4-88. USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single-ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single-ended	USB 2.0 load conditions	0	0.3	V
Z(DRV)	D+, D– impedance		28	44	Ω
t_r	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_f	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

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4.10.7 Universal Parallel Port (uPP) Interface

The uPP interface is a high-speed parallel interface with dedicated data lines and minimal control signals. The uPP interface is designed to interface cleanly with high-speed ADCs or DACs with 8-bit data width. It can also be interconnected with field-programmable gate arrays (FPGAs) or other uPP devices to achieve high-speed digital data transfer. It can operate in receive mode or transmit mode (simplex mode).

The uPP interface includes an internal DMA controller to maximize throughput and minimize CPU overhead during high-speed data transmission. All uPP transactions use internal DMA to feed data to or retrieve data from the I/O channels. Even though there is only one I/O channel, the DMA controller includes two DMA channels to support data interleave mode, in which all DMA resources service a single I/O channel.

On this device, the uPP interface is the dedicated resource for the CPU1 subsystem. CPU1, CPU1.CLA1, and CPU1.DMA have access to this module. Two dedicated 512-byte data RAMs (also known as MSG RAMs) are tightly coupled with the uPP module (one for each, TX and RX). These data RAMs are used to store the bulk of data to avoid frequent interruptions to the CPU. Only CPU1 and CPU1.CLA1 have access to these data RAMs. 図 4-78 shows the integration of the uPP on this device.

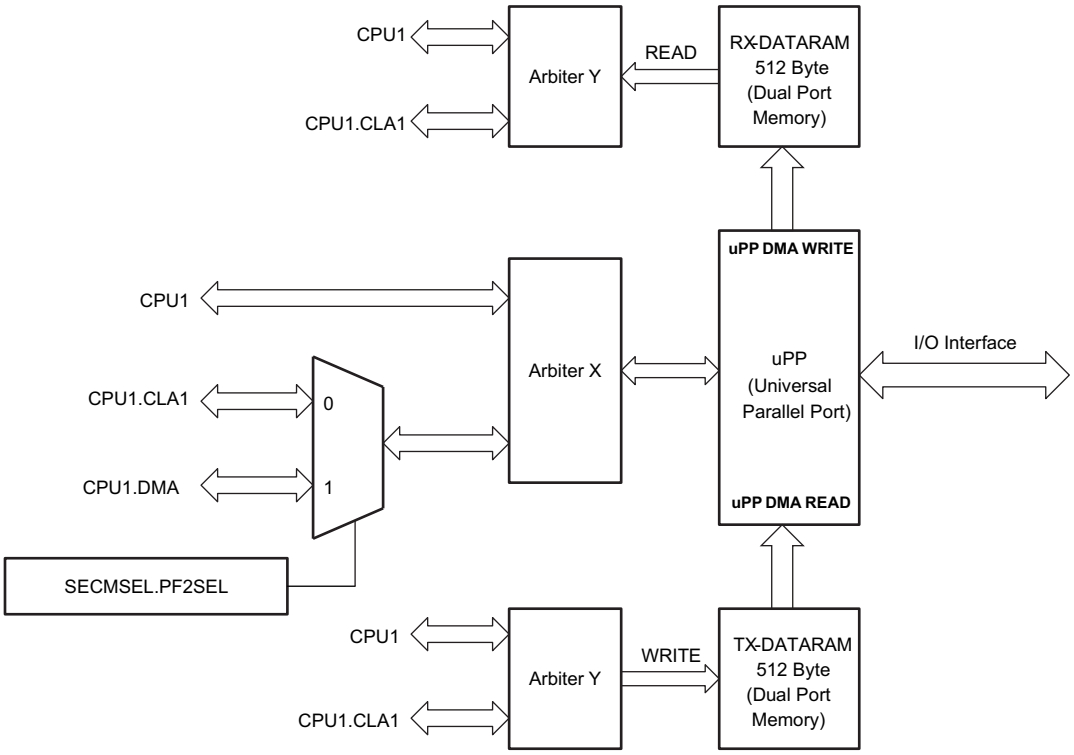


図 4-78. uPP Integration

注

On some TI devices, the uPP module is also called the Radio Peripheral Interface (RPI) module.

The uPP interface supports the following:

- Mainstream high-speed data converters with parallel conversion interface.
- Mainstream high-speed streaming interface with frame START indication.
- Mainstream high-speed streaming interface with data ENABLE indication.
- Mainstream high-speed streaming interface with synchronization WAIT signal.
- SDR (single-data-rate) or DDR (double-data-rate, interleaved) interface.
- Multiplexing of interleaved data in SDR transmit case.
- Demultiplexing and multiplexing of interleaved data in DDR case.
- I/O interface clock frequency up to 50 MHz for SDR, and 25 MHz for DDR.
- Single-channel 8-bit input receive or output transmit mode.
- Max throughput is 50MB/s for pure read or pure write.
- Available as a DSP to FPGA general-purpose streaming interface.

図 4-79 shows the uPP functional block diagram.

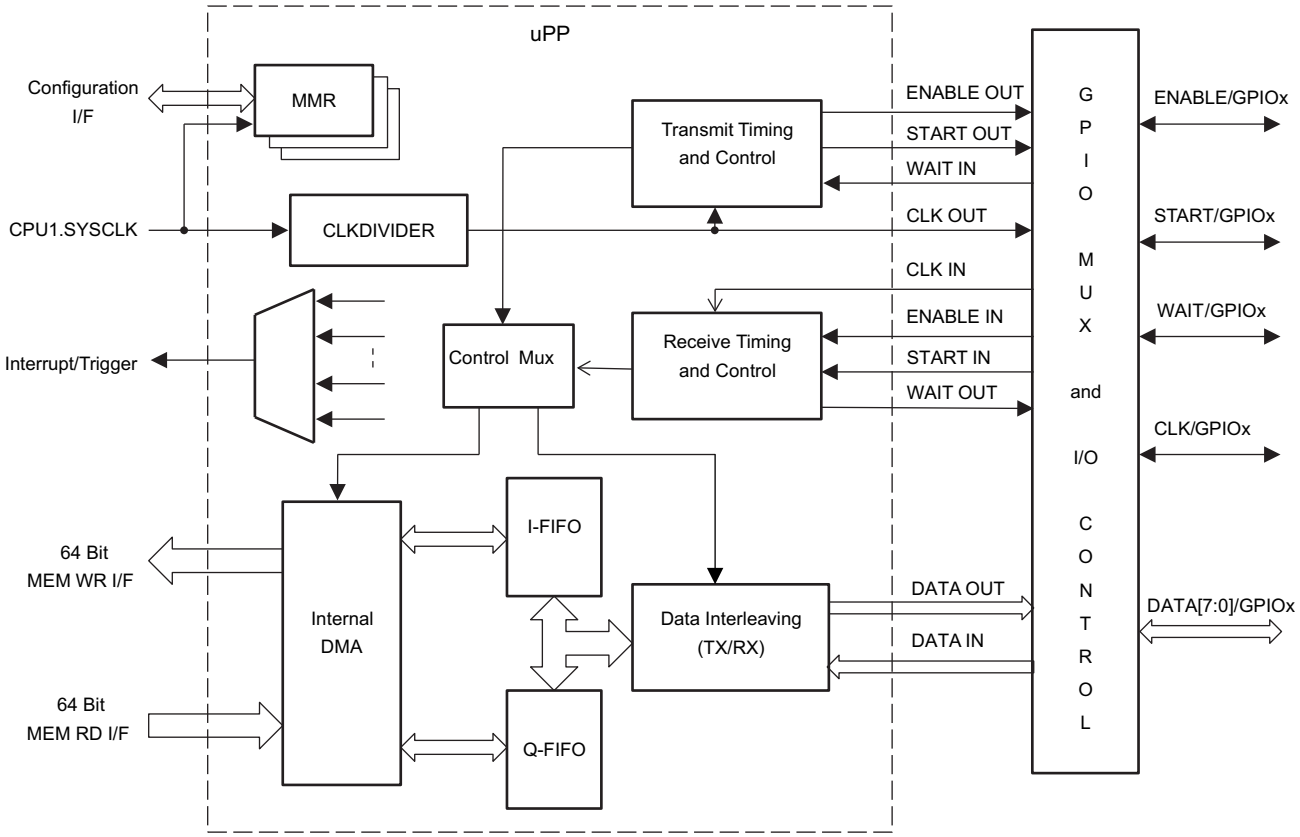


図 4-79. uPP Functional Block Diagram

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4.10.7.1 uPP Electrical Data and Timing

Table 4-89 shows the uPP timing requirements. Table 4-90 shows the uPP switching characteristics. Figure 4-80 through Figure 4-83 show the uPP timing diagrams.

Table 4-89. uPP Timing Requirements

NO.				MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, CLK	SDR mode	20		ns
			DDR mode	40		
2	$t_{w(CLKH)}$	Pulse width, CLK high	SDR mode	8		ns
			DDR mode	18		
3	$t_{w(CLKL)}$	Pulse width, CLK low	SDR mode	8		ns
			DDR mode	18		
4	$t_{su(STV-CLKH)}$	Setup time, START valid before CLK high		4		ns
5	$t_{h(CLKH-STV)}$	Hold time, START valid after CLK high		0.8		ns
6	$t_{su(ENV-CLKH)}$	Setup time, ENABLE valid before CLK high		4		ns
7	$t_{h(CLKH-ENV)}$	Hold time, ENABLE valid after CLK high		0.8		ns
8	$t_{su(DV-CLKH)}$	Setup time, DATA valid before CLK high		4		ns
9	$t_{h(CLKH-DV)}$	Hold time, DATA valid after CLK high		0.8		ns
10	$t_{su(DV-CLKL)}$	Setup time, DATA valid before CLK low		4		ns
11	$t_{h(CLKL-DV)}$	Hold time, DATA valid after CLK low		0.8		ns
19	$t_{su(WTV-CLKH)}$	Setup time, WAIT valid before CLK high	SDR mode	20		ns
20	$t_{h(CLKH-WTV)}$	Hold time, WAIT valid after CLK high	SDR mode	0		ns
21	$t_{su(WTV-CLKL)}$	Setup time, WAIT valid before CLK low	DDR mode	20		ns
22	$t_{h(CLKL-WTV)}$	Hold time, WAIT valid after CLK low	DDR mode	0		ns

Table 4-90. uPP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER			MIN	MAX	UNIT
12	$t_{c(CLK)}$	Cycle time, CLK	SDR mode	20		ns
			DDR mode	40		
13	$t_{w(CLKH)}$	Pulse width, CLK high	SDR mode	8		ns
			DDR mode	18		
14	$t_{w(CLKL)}$	Pulse width, CLK low	SDR mode	8		ns
			DDR mode	18		
15	$t_{d(CLKH-STV)}$	Delay time, START valid after CLK high		3	12	ns
16	$t_{d(CLKH-ENV)}$	Delay time, ENABLE valid after CLK high		3	12	ns
17	$t_{d(CLKH-DV)}$	Delay time, DATA valid after CLK high		3	12	ns
18	$t_{d(CLKL-DV)}$	Delay time, DATA valid after CLK low		3	12	ns

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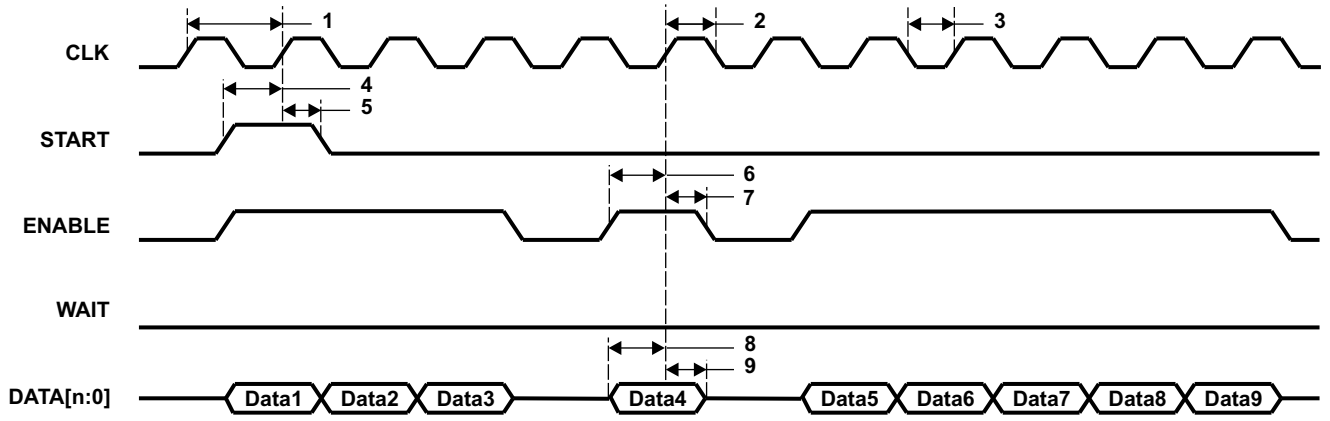


Figure 4-80. uPP Single Data Rate (SDR) Receive Timing

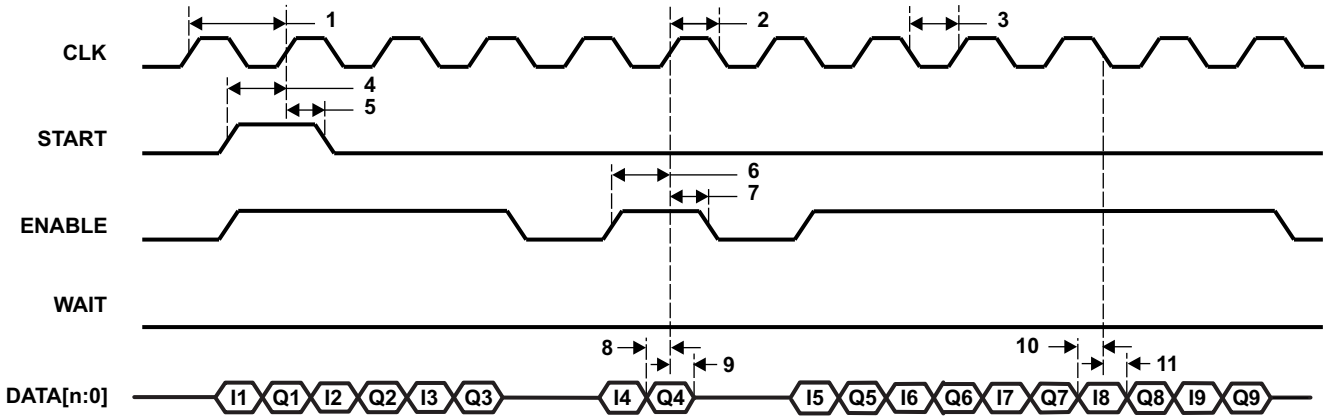


Figure 4-81. uPP Double Data Rate (DDR) Receive Timing

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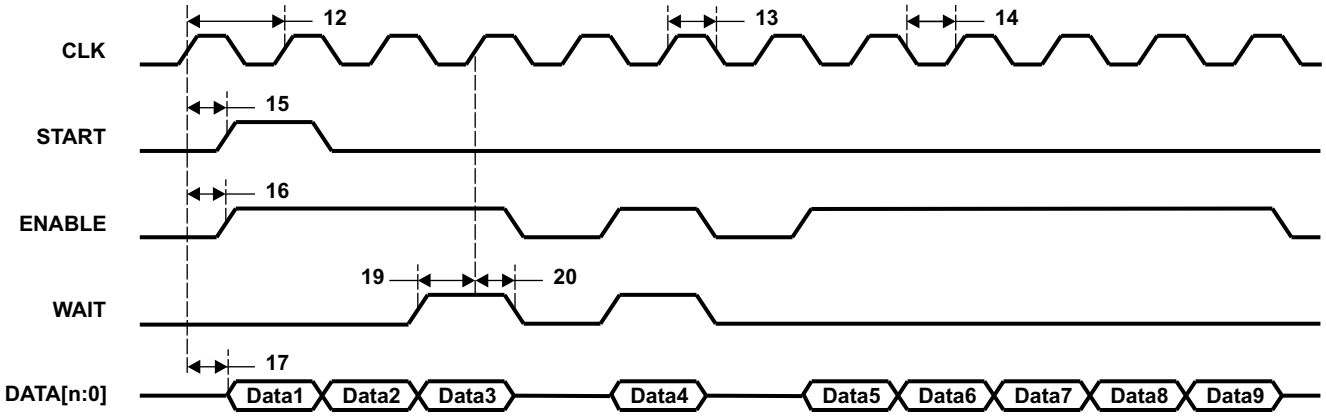


Figure 4-82. uPP Single Data Rate (SDR) Transmit Timing

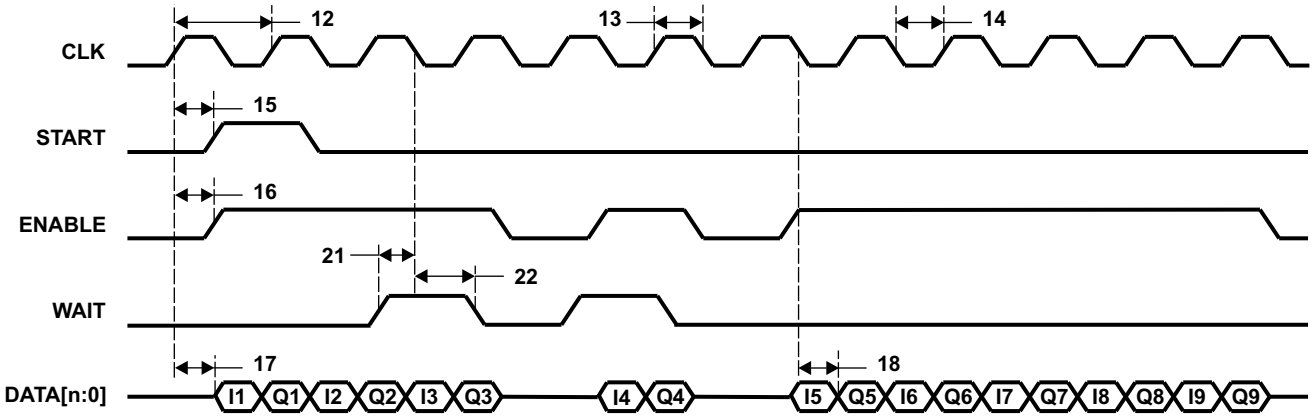


Figure 4-83. uPP Double Data Rate (DDR) Transmit Timing

5 Detailed Description

5.1 Overview

The Delfino TMS320F28377D-EP is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; transportation; and power line communications. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives. While the Delfino product line is not new to the TMS320C2000 portfolio, the F28377D supports a new dual-core C28x architecture that significantly boosts system performance. The integrated analog and control peripherals also let designers consolidate control architectures and eliminate multiprocessor use in high-end systems.

The dual real-time control subsystems are based on TI's 32-bit C28x floating-point CPUs, which provide 200 MHz of signal processing performance in each core. The C28x CPUs are further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations; and the VCU accelerator, which reduces the time for complex math operations common in encoded applications.

The F28377D microcontroller features two CLA real-time control coprocessors. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics. The dual C28x+CLA architecture enables intelligent partitioning between various system tasks. For example, one C28x+CLA core can be used to track speed and position, while the other C28x+CLA core can be used to control torque and current loops.

The TMS320F28377D-EP supports 1MB (512KW) of onboard flash memory with error correction code (ECC) and up to 204KB (102KW) of SRAM. Two 128-bit secure zones are also available on each CPU for code protection.

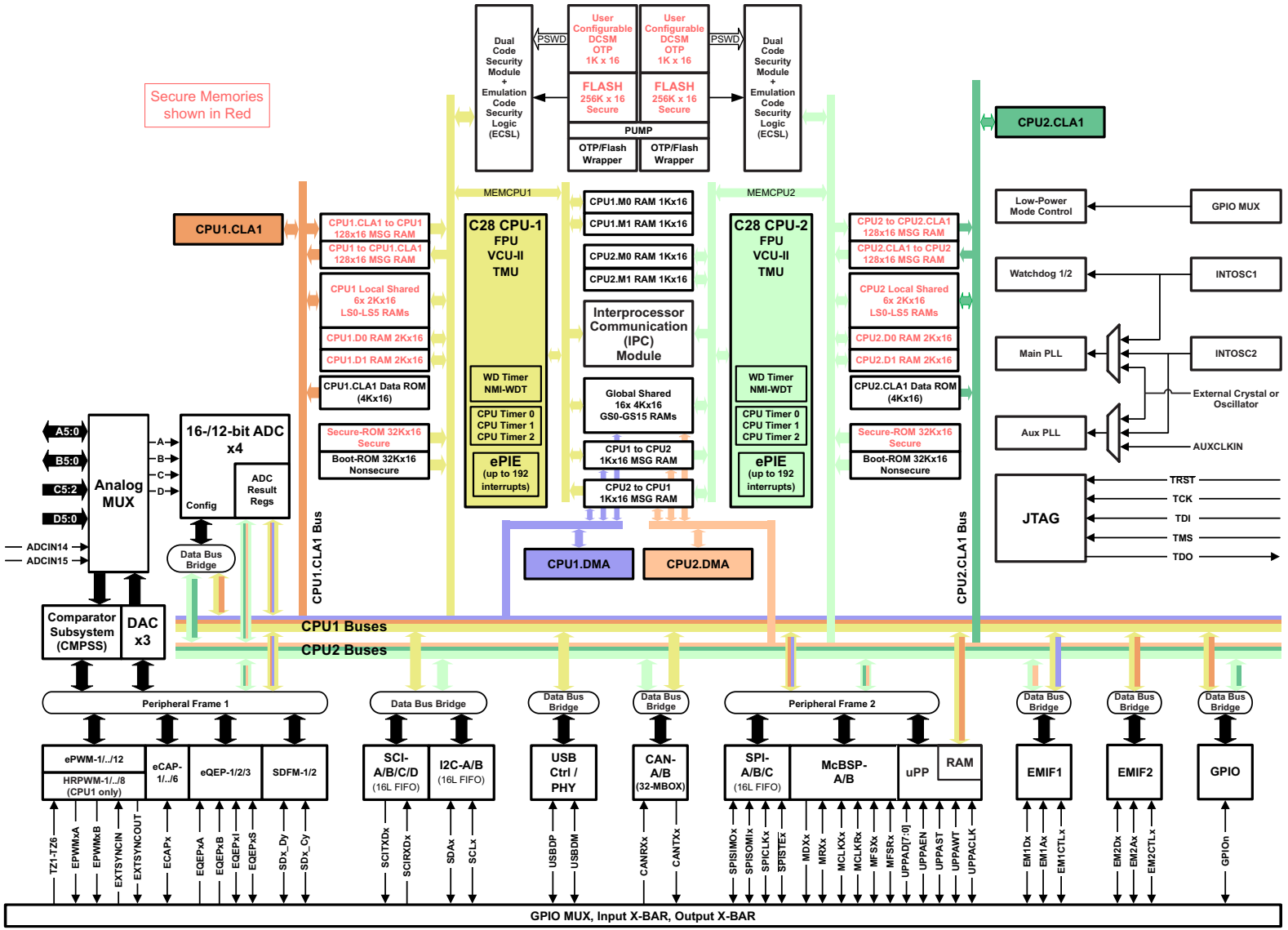
Performance analog and control peripherals are also integrated on the F28377D MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The new sigma-delta filter module (SDFM) works in conjunction with the sigma-delta modulator to enable isolated current shunt measurements. The Comparator Subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as EMIFs, CAN modules (ISO 11898-1/CAN 2.0B-compliant), and a new uPP interface extend the connectivity of the F28377D. The uPP interface is a new feature of the C2000 MCUs and supports high-speed parallel connection to FPGAs or other processors with similar uPP interfaces. Lastly, a USB 2.0 port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application.

5.2 Functional Block Diagram

図 5-1 shows the CPU system and associated peripherals.

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図 5-1. Functional Block Diagram

5.3 Memory

5.3.1 C28x Memory Map

Both C28x CPUs on the device have the same memory map except where noted in 表 5-1. The GSx_RAM (Global Shared RAM) should be assigned to either CPU by the GSxMSEL register. Memories accessible by the CLA or DMA (direct memory access) are noted as well.

表 5-1. C28x Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
M0 RAM	1K × 16	0x0000 0000	0x0000 03FF		
M1 RAM	1K × 16	0x0000 0400	0x0000 07FF		
PieVectTable	512 × 16	0x0000 0D00	0x0000 0EFF		
CPUx.CLA1 to CPUx MSGRAM	128 × 16	0x0000 1480	0x0000 14FF	Yes	
CPUx to CPUx.CLA1 MSGRAM	128 × 16	0x0000 1500	0x0000 157F	Yes	
UPP TX MSG RAM	512 × 16	0x0000 6C00	0x0000 6DFF	Yes	
UPP RX MSG RAM	512 × 16	0x0000 6E00	0x0000 6FFF	Yes	
LS0 RAM	2K × 16	0x0000 8000	0x0000 87FF	Yes	
LS1 RAM	2K × 16	0x0000 8800	0x0000 8FFF	Yes	
LS2 RAM	2K × 16	0x0000 9000	0x0000 97FF	Yes	
LS3 RAM	2K × 16	0x0000 9800	0x0000 9FFF	Yes	
LS4 RAM	2K × 16	0x0000 A000	0x0000 A7FF	Yes	
LS5 RAM	2K × 16	0x0000 A800	0x0000 AFFF	Yes	
D0 RAM	2K × 16	0x0000 B000	0x0000 B7FF		
D1 RAM	2K × 16	0x0000 B800	0x0000 BFFF		
GS0 RAM(1)	4K × 16	0x0000 C000	0x0000 CFFF		Yes
GS1 RAM(1)	4K × 16	0x0000 D000	0x0000 DFFF		Yes
GS2 RAM(1)	4K × 16	0x0000 E000	0x0000 EFFF		Yes
GS3 RAM(1)	4K × 16	0x0000 F000	0x0000 FFFF		Yes
GS4 RAM(1)	4K × 16	0x0001 0000	0x0001 0FFF		Yes
GS5 RAM(1)	4K × 16	0x0001 1000	0x0001 1FFF		Yes
GS6 RAM(1)	4K × 16	0x0001 2000	0x0001 2FFF		Yes
GS7 RAM(1)	4K × 16	0x0001 3000	0x0001 3FFF		Yes
GS8 RAM(1)	4K × 16	0x0001 4000	0x0001 4FFF		Yes
GS9 RAM(1)	4K × 16	0x0001 5000	0x0001 5FFF		Yes
GS10 RAM(1)	4K × 16	0x0001 6000	0x0001 6FFF		Yes
GS11 RAM(1)	4K × 16	0x0001 7000	0x0001 7FFF		Yes
GS12 RAM(1)(2)	4K × 16	0x0001 8000	0x0001 8FFF		Yes
GS13 RAM(1)(2)	4K × 16	0x0001 9000	0x0001 9FFF		Yes
GS14 RAM(1)(2)	4K × 16	0x0001 A000	0x0001 AFFF		Yes
GS15 RAM(1)(2)	4K × 16	0x0001 B000	0x0001 BFFF		Yes
CPU2 to CPU1 MSGRAM(1)	1K × 16	0x0003 F800	0x0003 FBFF		Yes
CPU1 to CPU2 MSGRAM(1)	1K × 16	0x0003 FC00	0x0003 FFFF		Yes
CAN A Message RAM(1)	2K × 16	0x0004 9000	0x0004 97FF		
CAN B Message RAM(1)	2K × 16	0x0004 B000	0x0004 B7FF		
Flash	256K × 16	0x0008 0000	0x000B FFFF		
Secure ROM	32K × 16	0x003F 0000	0x003F 7FFF		
Boot ROM	32K × 16	0x003F 8000	0x003F FFBF		
Vectors	64 × 16	0x003F FFC0	0x003F FFFF		

(1) Shared between CPU subsystems.
(2) Available only on F28379D, F28378D, F28377D, and F28375D.

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5.3.2 Flash Memory Map

On the F28377D device, each CPU has its own flash bank [512KB (256KW)], the total flash for each device is 1MB (512KW). Only one bank can be programmed or erased at a time and the code to program the flash should be executed out of RAM. 表 5-2 shows the addresses of flash sectors on CPU1 and CPU2 for F28377D.

表 5-2. Addresses of Flash Sectors on CPU1 and CPU2 for F28377D

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP	1K × 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP	1K × 16	0x0007 8000	0x0007 83FF
Sectors			
Sector A	8K × 16	0x0008 0000	0x0008 1FFF
Sector B	8K × 16	0x0008 2000	0x0008 3FFF
Sector C	8K × 16	0x0008 4000	0x0008 5FFF
Sector D	8K × 16	0x0008 6000	0x0008 7FFF
Sector E	32K × 16	0x0008 8000	0x0008 FFFF
Sector F	32K × 16	0x0009 0000	0x0009 7FFF
Sector G	32K × 16	0x0009 8000	0x0009 FFFF
Sector H	32K × 16	0x000A 0000	0x000A 7FFF
Sector I	32K × 16	0x000A 8000	0x000A FFFF
Sector J	32K × 16	0x000B 0000	0x000B 7FFF
Sector K	8K × 16	0x000B 8000	0x000B 9FFF
Sector L	8K × 16	0x000B A000	0x000B BFFF
Sector M	8K × 16	0x000B C000	0x000B DFFF
Sector N	8K ×16	0x000B E000	0x000B FFFF
Flash ECC Locations			
TI OTP ECC	128 × 16	0x0107 0000	0x0107 007F
User-configurable DCSM OTP ECC	128 × 16	0x0107 1000	0x0107 107F
Flash ECC	32K × 16	0x0108 0000	0x0108 7FFF

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5.3.3 EMIF Chip Select Memory Map

The EMIF1 memory map is the same for both CPU subsystems. EMIF2 is available only on the CPU1 subsystem. The EMIF memory map is shown in 表 5-3.

表 5-3. EMIF Chip Select Memory Map

EMIF CHIP SELECT	SIZE(1)	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EMIF1_CS0n - Data	256M × 16	0x8000 0000	0x8FFF FFFF		Yes
EMIF1_CS2n - Program + Data(2)	2M × 16	0x0010 0000	0x002F FFFF		Yes
EMIF1_CS3n - Program + Data	512K × 16	0x0030 0000	0x0037 FFFF		Yes
EMIF1_CS4n - Program + Data	393K × 16	0x0038 0000	0x003D FFFF		Yes
EMIF2_CS0n - Data(3)	3M × 16	0x9000 0000	0x91FF FFFF		
EMIF2_CS2n - Program + Data(3)	4K × 16	0x0000 2000	0x0000 2FFF	Yes (Data only)	

(1) Available memory size listed in this table is the maximum possible size assuming 32-bit memory. This may not apply to other memory sizes because of pin mux setting. See Section 3.4.1 to find the available address lines for your use case.
(2) The 2M × 16 size is for a 32-bit interface with the assumption that 16-bit accesses are not performed; hence, byte enables are not used (tied to active value on board). If byte enables are used, then the maximum size is smaller because byte enables are muxed with address pins (see Section 3.4.1). If 16-bit memory is used, then the maximum size is 1M × 16.
(3) Available only on the CPU1 subsystem.

5.3.4 Peripheral Registers Memory Map

The peripheral registers memory map can be found in 表 5-4. The peripheral registers can be assigned to either the CPU1 or CPU2 subsystems except where noted in 表 5-4. Registers in the peripheral frames share a secondary master (CLA or DMA) selection with all other registers within the same peripheral frame. See the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for details on the CPU subsystem and secondary master selection.

表 5-4. Peripheral Registers Memory Map

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	PROTECTED(1)	CLA ACCESS	DMA ACCESS
AdcaResultRegs	ADC_RESULT_REGS	0x0000 0B00	0x0000 0B1F		Yes	Yes
AdcbResultRegs	ADC_RESULT_REGS	0x0000 0B20	0x0000 0B3F		Yes	Yes
AdccResultRegs	ADC_RESULT_REGS	0x0000 0B40	0x0000 0B5F		Yes	Yes
AdcdResultRegs	ADC_RESULT_REGS	0x0000 0B60	0x0000 0B7F		Yes	Yes
CpuTimer0Regs(2)	CPUTIMER_REGS	0x0000 0C00	0x0000 0C07			
CpuTimer1Regs(2)	CPUTIMER_REGS	0x0000 0C08	0x0000 0C0F			
CpuTimer2Regs(2)	CPUTIMER_REGS	0x0000 0C10	0x0000 0C17			
PieCtrlRegs(2)	PIE_CTRL_REGS	0x0000 0CE0	0x0000 0CFF			
Cla1SoftIntRegs	CLA_SOFTINT_REGS	0x0000 0CE0	0x0000 0CFF		Yes – CLA only, no CPU access	
DmaRegs(2)	DMA_REGS	0x0000 1000	0x0000 11FF			
Cla1Regs(2)	CLA_REGS	0x0000 1400	0x0000 147F			
Peripheral Frame 1						
EPwm1Regs	EPWM_REGS	0x0000 4000	0x0000 40FF	Yes	Yes	Yes
EPwm2Regs	EPWM_REGS	0x0000 4100	0x0000 41FF	Yes	Yes	Yes
EPwm3Regs	EPWM_REGS	0x0000 4200	0x0000 42FF	Yes	Yes	Yes
EPwm4Regs	EPWM_REGS	0x0000 4300	0x0000 43FF	Yes	Yes	Yes
EPwm5Regs	EPWM_REGS	0x0000 4400	0x0000 44FF	Yes	Yes	Yes
EPwm6Regs	EPWM_REGS	0x0000 4500	0x0000 45FF	Yes	Yes	Yes
EPwm7Regs	EPWM_REGS	0x0000 4600	0x0000 46FF	Yes	Yes	Yes
EPwm8Regs	EPWM_REGS	0x0000 4700	0x0000 47FF	Yes	Yes	Yes
EPwm9Regs	EPWM_REGS	0x0000 4800	0x0000 48FF	Yes	Yes	Yes
EPwm10Regs	EPWM_REGS	0x0000 4900	0x0000 49FF	Yes	Yes	Yes

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表 5-4. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	PROTECTED[1]	CLA ACCESS	DMA ACCESS
EPwm11Regs	EPWM_REGS	0x0000 4A00	0x0000 4AFF	Yes	Yes	Yes
EPwm12Regs	EPWM_REGS	0x0000 4B00	0x0000 4BFF	Yes	Yes	Yes
ECap1Regs	ECAP_REGS	0x0000 5000	0x0000 501F	Yes	Yes	Yes
ECap2Regs	ECAP_REGS	0x0000 5020	0x0000 503F	Yes	Yes	Yes
ECap3Regs	ECAP_REGS	0x0000 5040	0x0000 505F	Yes	Yes	Yes
ECap4Regs	ECAP_REGS	0x0000 5060	0x0000 507F	Yes	Yes	Yes
ECap5Regs	ECAP_REGS	0x0000 5080	0x0000 509F	Yes	Yes	Yes
ECap6Regs	ECAP_REGS	0x0000 50A0	0x0000 50BF	Yes	Yes	Yes
EQep1Regs	EQEP_REGS	0x0000 5100	0x0000 513F	Yes	Yes	Yes
EQep2Regs	EQEP_REGS	0x0000 5140	0x0000 517F	Yes	Yes	Yes
EQep3Regs	EQEP_REGS	0x0000 5180	0x0000 51BF	Yes	Yes	Yes
DacaRegs	DAC_REGS	0x0000 5C00	0x0000 5C0F	Yes	Yes	Yes
DacbRegs	DAC_REGS	0x0000 5C10	0x0000 5C1F	Yes	Yes	Yes
DaccRegs	DAC_REGS	0x0000 5C20	0x0000 5C2F	Yes	Yes	Yes
Cmpss1Regs	CMPSS_REGS	0x0000 5C80	0x0000 5C9F	Yes	Yes	Yes
Cmpss2Regs	CMPSS_REGS	0x0000 5CA0	0x0000 5CBF	Yes	Yes	Yes
Cmpss3Regs	CMPSS_REGS	0x0000 5CC0	0x0000 5CDF	Yes	Yes	Yes
Cmpss4Regs	CMPSS_REGS	0x0000 5CE0	0x0000 5CFF	Yes	Yes	Yes
Cmpss5Regs	CMPSS_REGS	0x0000 5D00	0x0000 5D1F	Yes	Yes	Yes
Cmpss6Regs	CMPSS_REGS	0x0000 5D20	0x0000 5D3F	Yes	Yes	Yes
Cmpss7Regs	CMPSS_REGS	0x0000 5D40	0x0000 5D5F	Yes	Yes	Yes
Cmpss8Regs	CMPSS_REGS	0x0000 5D60	0x0000 5D7F	Yes	Yes	Yes
Sdfm1Regs	SDFM_REGS	0x0000 5E00	0x0000 5E7F	Yes	Yes	Yes
Sdfm2Regs	SDFM_REGS	0x0000 5E80	0x0000 5EFF	Yes	Yes	Yes
Peripheral Frame 2						
McbspaRegs	MCBSP_REGS	0x0000 6000	0x0000 603F	Yes	Yes	Yes
McbspbRegs	MCBSP_REGS	0x0000 6040	0x0000 607F	Yes	Yes	Yes
SpiaRegs	SPI_REGS	0x0000 6100	0x0000 610F	Yes	Yes	Yes
SpibRegs	SPI_REGS	0x0000 6110	0x0000 611F	Yes	Yes	Yes
SpicRegs	SPI_REGS	0x0000 6120	0x0000 612F	Yes	Yes	Yes
UppRegs[3]	UPP_REGS	0x0000 6200	0x0000 62FF	Yes	Yes	Yes
WdRegs[2]	WD_REGS	0x0000 7000	0x0000 703F	Yes		
NmiIntruptRegs[2]	NMI_INTRUPT_REGS	0x0000 7060	0x0000 706F	Yes		
XintRegs[2]	XINT_REGS	0x0000 7070	0x0000 707F	Yes		
SciaRegs	SCI_REGS	0x0000 7200	0x0000 720F	Yes		
ScibRegs	SCI_REGS	0x0000 7210	0x0000 721F	Yes		
ScicRegs	SCI_REGS	0x0000 7220	0x0000 722F	Yes		
ScidRegs	SCI_REGS	0x0000 7230	0x0000 723F	Yes		
I2caRegs	I2C_REGS	0x0000 7300	0x0000 733F	Yes		
I2cbRegs	I2C_REGS	0x0000 7340	0x0000 737F	Yes		
AdcaRegs	ADC_REGS	0x0000 7400	0x0000 747F	Yes	Yes	
AdcbRegs	ADC_REGS	0x0000 7480	0x0000 74FF	Yes	Yes	
AdccRegs	ADC_REGS	0x0000 7500	0x0000 757F	Yes	Yes	
AdcdRegs	ADC_REGS	0x0000 7580	0x0000 75FF	Yes	Yes	
InputXbarRegs[3]	INPUT_XBAR_REGS	0x0000 7900	0x0000 791F	Yes		
XbarRegs[3]	XBAR_REGS	0x0000 7920	0x0000 793F	Yes		
TrigRegs[3]	TRIG_REGS	0x0000 7940	0x0000 794F	Yes		
DmaClaSrcSelRegs[2]	DMA_CLA_SRC_SEL_REGS	0x0000 7980	0x0000 798F	Yes		
EPwmXbarRegs[3]	EPWM_XBAR_REGS	0x0000 7A00	0x0000 7A3F	Yes		

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表 5-4. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	PROTECTED(1)	CLA ACCESS	DMA ACCESS
OutputXbarRegs(3)	OUTPUT_XBAR_REGS	0x0000 7A80	0x0000 7ABF	Yes		
GpioCtrlRegs(3)	GPIO_CTRL_REGS	0x0000 7C00	0x0000 7D7F	Yes		
GpioDataRegs(2)	GPIO_DATA_REGS	0x0000 7F00	0x0000 7F2F	Yes	Yes	
UsbaRegs(3)	USB_REGS	0x0004 0000	0x0004 0FFF	Yes		
Emif1Regs	EMIF_REGS	0x0004 7000	0x0004 77FF	Yes		
Emif2Regs(3)	EMIF_REGS	0x0004 7800	0x0004 7FFF	Yes		
CanaRegs	CAN_REGS	0x0004 8000	0x0004 87FF	Yes		
CanbRegs	CAN_REGS	0x0004 A000	0x0004 A7FF	Yes		
IpcRegs(2)	IPC_REGS_CPU1 IPC_REGS_CPU2	0x0005 0000	0x0005 0023	Yes		
FlashPumpSemaphoreRegs(2)	FLASH_PUMP_SEMAPHORE_REGS	0x0005 0024	0x0005 0025	Yes		
DevCfgRegs(3)	DEV_CFG_REGS	0x0005 D000	0x0005 D17F	Yes		
AnalogSubsysRegs(3)	ANALOG_SUBSYS_REGS	0x0005 D180	0x0005 D1FF	Yes		
ClkCfgRegs(4)	CLK_CFG_REGS	0x0005 D200	0x0005 D2FF	Yes		
CpuSysRegs(2)	CPU_SYS_REGS	0x0005 D300	0x0005 D3FF	Yes		
RomPrefetchRegs(3)	ROM_PREFETCH_REGS	0x0005 E608	0x0005 E60B	Yes		
DcsmZ1Regs(2)	DCSM_Z1_REGS	0x0005 F000	0x0005 F02F	Yes		
DcsmZ2Regs(2)	DCSM_Z2_REGS	0x0005 F040	0x0005 F05F	Yes		
DcsmCommonRegs(2)	DCSM_COMMON_REGS	0x0005 F070	0x0005 F07F	Yes		
MemCfgRegs(2)	MEM_CFG_REGS	0x0005 F400	0x0005 F47F	Yes		
Emif1ConfigRegs(2)	EMIF1_CONFIG_REGS	0x0005 F480	0x0005 F49F	Yes		
Emif2ConfigRegs(3)	EMIF2_CONFIG_REGS	0x0005 F4A0	0x0005 F4BF	Yes		
AccessProtectionRegs(2)	ACCESS_PROTECTION_REGS	0x0005 F4C0	0x0005 F4FF	Yes		
MemoryErrorRegs(2)	MEMORY_ERROR_REGS	0x0005 F500	0x0005 F53F	Yes		
RomWaitStateRegs(3)	ROM_WAIT_STATE_REGS	0x0005 F540	0x0005 F541	Yes		
Flash0CtrlRegs(2)	FLASH_CTRL_REGS	0x0005 F800	0x0005 FAFF	Yes		
Flash0EccRegs(2)	FLASH_ECC_REGS	0x0005 FB00	0x0005 FB3F	Yes		

(1) The CPU (not applicable for CLA or DMA) contains a write followed by read protection mode to ensure that any read operation that follows a write operation within a protected address range is executed as written by delaying the read operation until the write is initiated.

(2) A unique copy of these registers exist on each CPU subsystem.

(3) These registers are available only on the CPU1 subsystem.

(4) These registers are mapped to either CPU1 or CPU2 based on a semaphore.

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5.3.5 Memory Types

表 5-5 provides more information about each memory type.

表 5-5. Memory Types

MEMORY TYPE	ECC-CAPABLE	PARITY	SECURITY	HIBERNATE RETENTION	ACCESS PROTECTION
M0, M1	Yes	–	–	Yes	–
D0, D1	Yes	–	Yes	–	Yes
LSx	–	Yes	Yes	–	Yes
GSx	–	Yes	–	–	Yes
CPU/CLA MSGRAM	–	Yes	Yes	–	Yes
Boot ROM	–	–	–	N/A	–
Secure ROM	–	–	Yes	N/A	–
Flash	Yes	–	Yes	N/A	N/A
User-configurable DCSM OTP	Yes	–	Yes	N/A	N/A

5.3.5.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has four dedicated ECC-capable RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). D0/D1 memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection).

5.3.5.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

表 5-6 shows the master access for the LSx RAM.

表 5-6. Master Access for LSx RAM (With Assumption That all Other Access Protections are Disabled)

MSEL_LSx	CLAPGM_LSx	CPU ALLOWED ACCESS	CLA ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

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5.3.5.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Each shared RAM block can be owned by either CPU subsystem based on the configuration of respective bits in the GSxMSEL register. Both the CPU and DMA have full read and write access to these memories.

All GSx RAM blocks have parity.

When a GSx RAM block is owned by a CPU subsystem, the CPUx and CPUx.DMA will have full access to that RAM block whereas the other CPUy and CPUy.DMA will only have read access (no fetch/write access).

表 5-7 shows the master access for the GSx RAM.

表 5-7. Master Access for GSx RAM
(With Assumption That all Other Access Protections are Disabled)

GSxMSEL	CPU	INSTRUCTION FETCH	READ	WRITE	CPUx.DMA READ	CPUx.DMA WRITE
0	CPU1	Yes	Yes	Yes	Yes	Yes
	CPU2	–	Yes	–	Yes	–
1	CPU1	–	Yes	–	Yes	–
	CPU2	Yes	Yes	Yes	Yes	Yes

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

5.3.5.4 CPU Message RAM (CPU MSGRAM)

These RAM blocks can be used to share data between CPU1 and CPU2. Since these RAMs are used for interprocessor communication, they are also called IPC RAMs. The CPU MSGRAMs have CPU/DMA read/write access from its own CPU subsystem, and CPU/DMA read only access from the other subsystem.

This RAM has parity.

5.3.5.5 CLA Message RAM (CLA MSGRAM)

These RAM blocks can be used to share data between the CPU and CLA. The CLA has read and write access to the "CLA to CPU MSGRAM." The CPU has read and write access to the "CPU to CLA MSGRAM." The CPU and CLA both have read access to both MSGRAMs.

This RAM has parity.

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5.4 Identification

表 5-8 shows the Device Identification Registers.

表 5-8. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDH (CPU1)	0x0005 D00A	2	Device part identification number	
PARTIDH (CPU2)	0x0007 0202		TMS320F28377D	0x00FF 0300
REVID	0x0005 D00C	2	Silicon revision number	
			Revision 0	0x0000 0000
			Revision A	0x0000 0000
			Revision B	0x0000 0002
			Revision C	0x0000 0003
UID_UNIQUE	0x0007 03C0	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This can be used as a serial number in the application. This number is present only on TMS Revision C devices.	
CPU ID	0x0007 026D	1	CPU identification number	
			CPU1	0xXX01
			CPU2	0xXX02
JTAG ID	N/A	N/A	JTAG Device ID	0x0B99 C02F

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5.5 Bus Architecture – Peripheral Connectivity

表 5-9 shows a broad view of the peripheral and configuration register accessibility from each bus master. Peripherals can be individually assigned to the CPU1 or CPU2 subsystem (for example, ePWM can be assigned to CPU1 and eQEP assigned to CPU2). Peripherals within peripheral frames 1 or 2 will all be mapped to the respective secondary master as a group (if SPI is assigned to CPUx.DMA, then McBSP is also assigned to CPUx.DMA).

表 5-9. Bus Master Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.CLA1	CPU2.DMA
Peripherals that can be assigned to CPU1 or CPU2 and have common selectable Secondary Masters						
Peripheral Frame 1: • ePWM • SDFM • eCAP(1) • eQEP(1) • CMPSS(1) • DAC(1)	Y	Y	Y	Y	Y	Y
Peripheral Frame 1: • HRPWM	Y	Y	Y			
Peripheral Frame 2: • SPI • McBSP	Y	Y	Y	Y	Y	Y
Peripheral Frame 2: • uPP Configuration(1)	Y	Y	Y			
Peripherals that can be assigned to CPU1 or CPU2 subsystems						
SCI			Y	Y		
I2C			Y	Y		
CAN			Y	Y		
ADC Configuration		Y	Y	Y	Y	
EMIF1	Y		Y	Y		Y
Peripherals and Device Configuration Registers only on CPU1 subsystem						
EMIF2		Y	Y			
USB			Y			
Device Capability, Peripheral Reset, Peripheral CPU Select			Y			
GPIO Pin Mapping and Configuration			Y			
Analog System Control			Y			
uPP Message RAMs		Y	Y			
Reset Configuration			Y			
Accessible by only one CPU at a time with Semaphore						
Clock and PLL Configuration			Y	Y		
Peripherals and Registers with Unique Copies of Registers for each CPU and CLA Master(2)						
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y	Y		
Flash Configuration(3)			Y	Y		
CPU Timers			Y	Y		
DMA and CLA Trigger Source Select			Y	Y		
GPIO Data(4)		Y	Y	Y	Y	
ADC Results	Y	Y	Y	Y	Y	Y

(1) These modules are on a Peripheral Frame with DMA access; however, they cannot trigger a DMA transfer.
(2) Each CPUx and CPUx.CLA1 can only access its own copy of these registers.
(3) At any given time, only one CPU can perform program or erase operations on the Flash.
(4) The GPIO Data Registers are unique for each CPUx and CPUx.CLAx. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the General-Purpose Input/Output (GPIO) chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* for more details.

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5.6 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*.

5.6.1 Floating-Point Unit

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

5.6.2 Trigonometric Math Unit

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in 表 5-10.

表 5-10. TMU Supported Instructions

INSTRUCTIONS	C EQUIVALENT OPERATION	PIPELINE CYCLES
MPY2PIF32 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32 RaH,RbH	a = b / 2pi	2/3
DIVF32 RaH,RbH,RcH	a = b / c	5
SQRTF32 RaH,RbH	a = sqrt(b)	5
SINPUF32 RaH,RbH	a = sin(b * 2pi)	4
COSPUF32 RaH,RbH	a = cos(b * 2pi)	4
ATANPUF32 RaH,RbH	a = atan(b) / 2pi	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. A detailed explanation of the workings of the FPU can be found in the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

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5.6.3 Viterbi, Complex Math, and CRC Unit II (VCU-II)

The VCU-II is the second-generation Viterbi, Complex Math, and CRC extension to the C28x CPU. The VCU-II extends the capabilities of the C28x CPU by adding registers and instructions to accelerate the performance of FFTs and communications-based algorithms. The C28x+VCU-II supports the following algorithm types:

- **Viterbi Decoding**

  Viterbi decoding is commonly used in baseband communications applications. The Viterbi decode algorithm consists of three main parts: branch metric calculations, compare-select (Viterbi butterfly), and a traceback operation. 表 5-11 shows a summary of the VCU performance for each of these operations.

表 5-11. Viterbi Decode Performance

VITERBI OPERATION	VCU CYCLES
Branch Metric Calculation (code rate = 1/2)	1
Branch Metric Calculation (code rate = 1/3)	2p
Viterbi Butterfly (add-compare-select)	2 (1)
Traceback per Stage	3 (2)

(1) C28x CPU takes 15 cycles per butterfly.
(2) C28x CPU takes 22 cycles per stage.

- **Cyclic Redundancy Check**

  Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCU can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCU can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

- **Complex Math**

  Complex math is used in many applications, a few of which are:

  – Fast Fourier Transform (FFT)

    The complex FFT is used in spread spectrum communications, as well as in many signal processing algorithms.

  – Complex filters

    Complex filters improve data reliability, transmission distance, and power efficiency. The C28x+VCU can perform a complex I and Q multiply with coefficients (four multiplies) in a single cycle. In addition, the C28x+VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.

  表 5-12 shows a summary of the VCU operations enabled by the VCU.

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表 5-12. Complex Math Performance

COMPLEX MATH OPERATION	VCU CYCLES	NOTES
Add or Subtract	1	32 +/- 32 = 32-bit (Useful for filters)
Add or Subtract	1	16 +/- 32 = 15-bit (Useful for FFT)
Multiply	2p	16 x 16 = 32-bit
Multiply and Accumulate (MAC)	2p	32 + 32 = 32-bit, 16 x 16 = 32-bit
RPT MAC	2p+N	Repeat MAC. Single cycle after the first operation.

For more information, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

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5.7 Control Law Accelerator

The CLA is an independent single-precision (32-bit) FPU processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

図 5-2 shows the CLA block diagram.

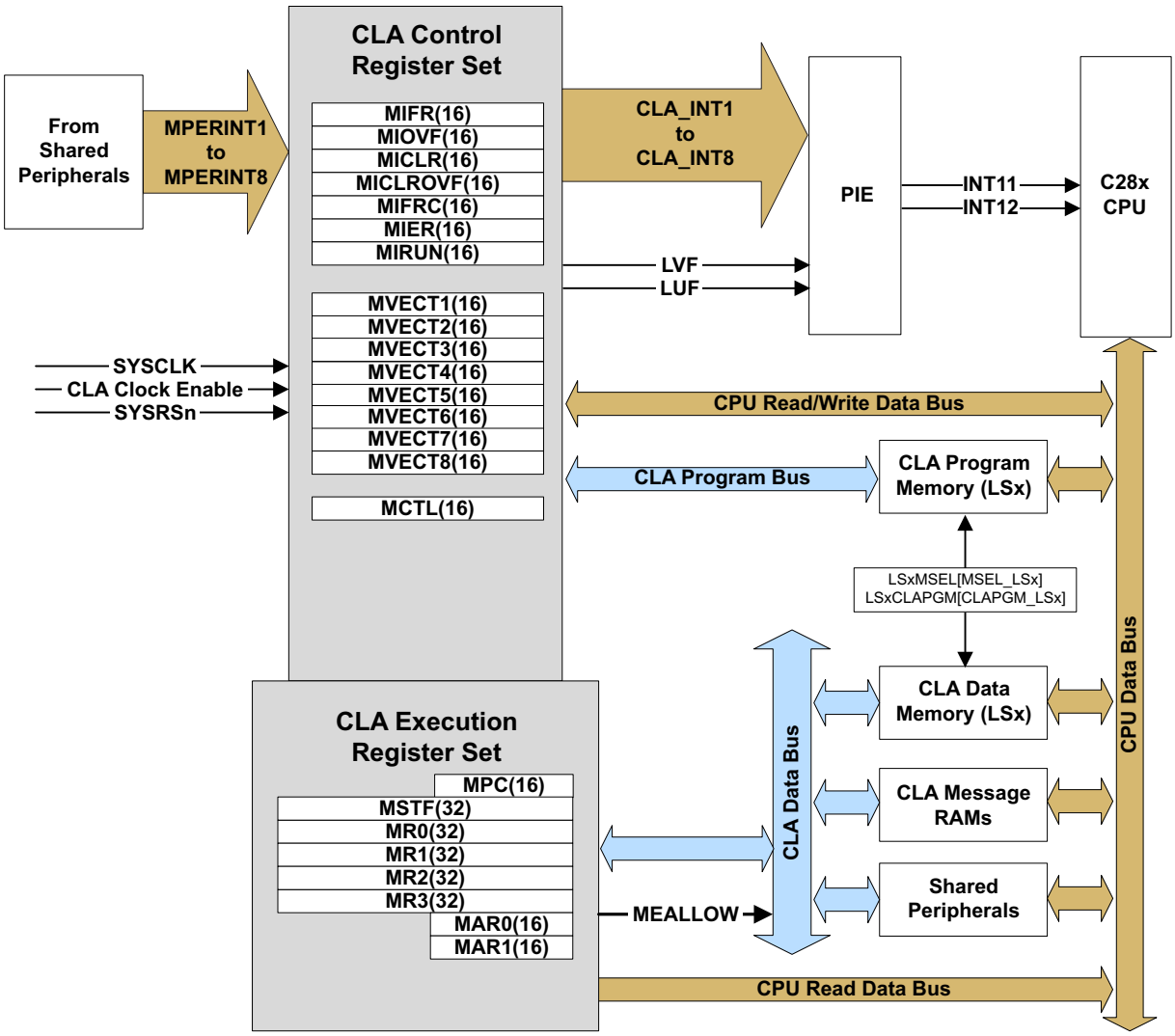


図 5-2. CLA Block Diagram

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5.8 Direct Memory Access

Each CPU has its own 6-channel DMA module. The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - Multichannel buffered serial port transmit and receive
  - External interrupts
  - CPU timers
  - EPWMxSOC signals
  - SPIx transmit and receive
  - SDFM
  - Software trigger
- Data sources and destinations:
  - GSx RAM
  - CPU message RAM (IPC RAM)
  - ADC result registers
  - ePWMx
  - SPI
  - McBSP
  - EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: four cycles/word (without arbitration)

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図 5-3 shows a device-level block diagram of the DMA.

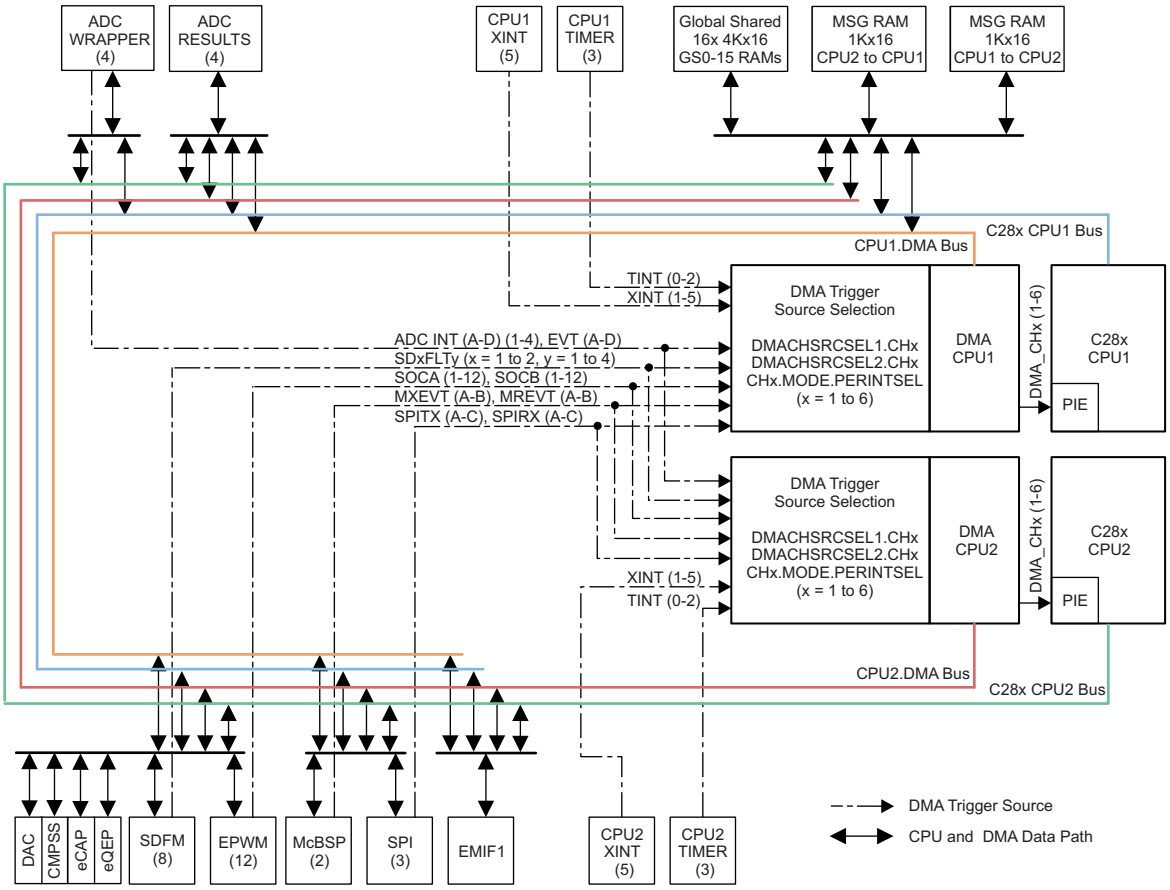


図 5-3. DMA Block Diagram

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5.9 Interprocessor Communication Module

The IPC module supports several methods of interprocessor communication:

- Thirty-two IPC flags per CPU, which can be used to signal events or indicate status through software polling. Four flags per CPU can generate interrupts.
- Shared data registers, which can be used to send commands or other small pieces of information between CPUs. Although the register names were chosen to support a command/response system, they can be used for any purpose as defined in software.
- Boot mode and status registers, which allow CPU1 to control the CPU2 boot process.
- A general-purpose free-running 64-bit counter.
- Two shared message RAMs, which can be used to transfer bulk data. Each RAM can be read by both CPUs. CPU1 can write to one RAM and CPU2 can write to the other.

図 5-4 shows the IPC architecture.

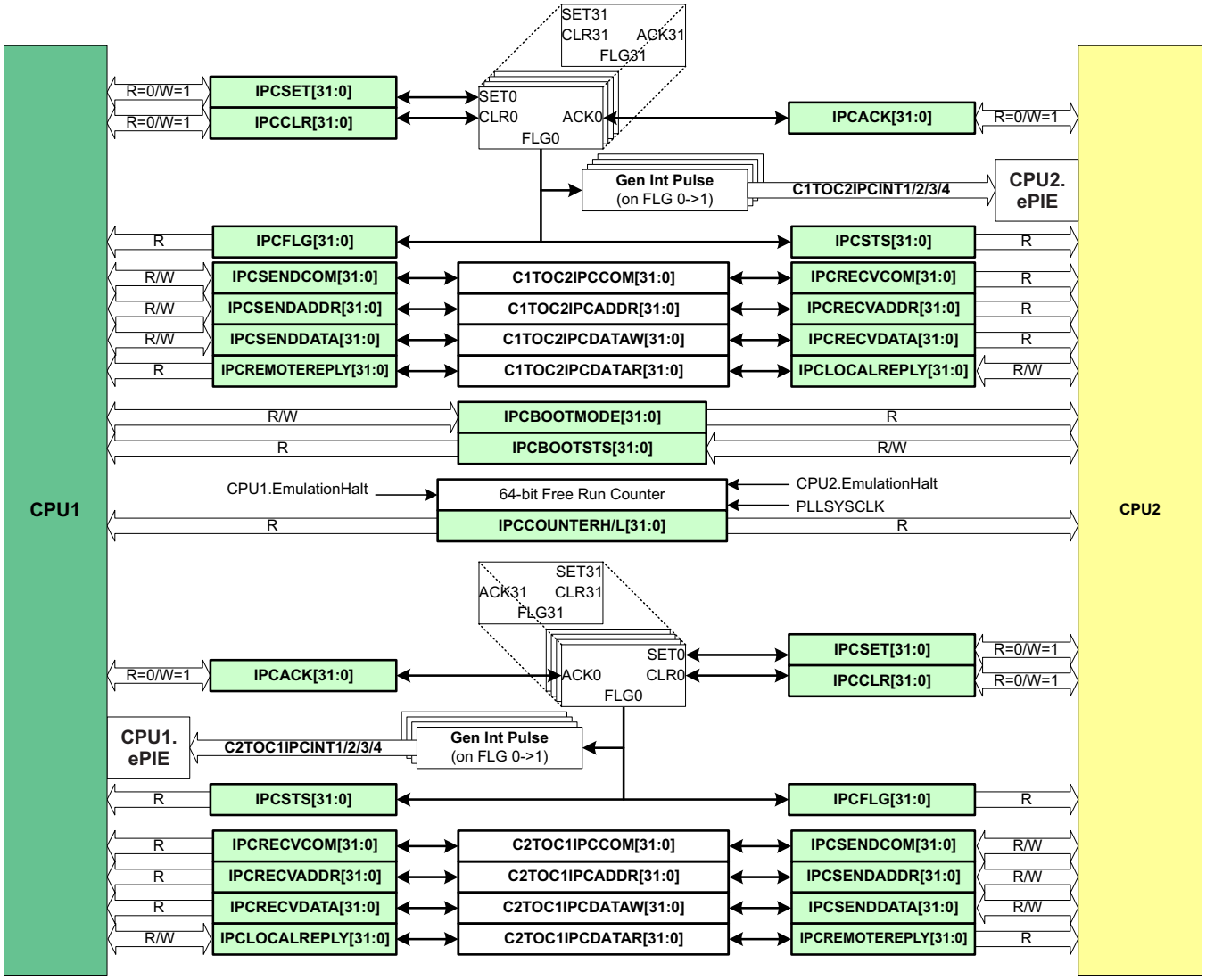


図 5-4. IPC Architecture

5.10 Boot ROM and Peripheral Booting

The device boot ROM (on both the CPUs) contains bootloading software. The CPU1 boot ROM does the system initialization before bringing CPU2 out of reset. The device boot ROM is executed each time the device comes out of reset. Users can configure the device to boot to flash (using GET mode) or choose to boot the device through one of the bootable peripherals by configuring the boot mode GPIO pins.

The CPU1 boot ROM, being master, owns the boot mode GPIO and boot configurations. The CPU2 boot ROM either boots to flash (if configured to do so through user configurable DCSM OTP) or enters a WAIT BOOT mode if no OTP is programmed. In WAIT BOOT mode, the CPU1 application instructs the CPU2 boot ROM on how to boot further using boot mode IPC commands supported by CPU2 boot ROM.

表 5-13 shows the possible boot modes supported on the device. The default boot mode pins are GPIO72 (boot mode pin 1) and GPIO 84 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user configurable DCSM OTP locations. This is recommended only for cases in which the factory default boot mode pins do not fit into the customer design. More details on the locations to be programmed is available in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

表 5-13. Device Boot Mode

MODE NO.	CPU1 BOOT MODE	CPU2 BOOT MODE	$\overline{\text{TRST}}$	GPIO72 (BOOT MODE PIN 1)	GPIO84 (BOOT MODE PIN 0)
0	Parallel I/O	Boot from Master	0	0	0
1	SCI Mode	Boot from Master	0	0	1
2	Wait Boot Mode	Boot from master	0	1	0
3	Get Mode	Boot from Master	0	1	1
4-7	EMU Boot Mode (Emulator Connected)	Boot from Master	1	X	X

注

The default behavior of Get mode is boot-to-flash. On unprogrammed devices, using Get mode will result in repeated watchdog resets, which may prevent proper JTAG connection and device initialization. Use Wait mode or another boot mode for unprogrammed devices.

注意

Some reset sources are internally driven by the device. The user must ensure the pins used for boot mode are not actively driven by other devices in the system for these cases. The boot configuration has a provision for changing the boot pins in OTP. For more details, see the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

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5.10.1 EMU Boot or Emulation Boot

The CPU enters this boot when it detects that $\overline{\text{TRST}}$ is HIGH (in other words, when an emulator/debugger is connected). In this mode, the user can program the EMUBOOTCTRL register (at location 0xD00) to instruct the device on how to boot. If the contents of the EMUBOOTCTRL locations are invalid, then the device would default into WAIT Boot mode. The emulation boot allows users to verify the device boot before programming the boot mode into OTP.

5.10.2 WAIT Boot Mode

The device in this boot mode loops in the boot ROM. This mode is useful if users want to connect a debugger on a secure device or if users do not want the device to execute an application in flash yet.

5.10.3 Get Mode

The default behavior of Get mode is boot-to-flash. This behavior can be changed by programming the Zx-OTPBOOTCTRL locations in user configurable DCSM OTP. The user configurable DCSM OTP on this device is divided in to two secure zones: Z1 and Z2. The Get mode function in boot ROM first checks if a valid OTPBOOTCTRL value is programmed in Z1. If the answer is yes, then the device boots as per the Z1-OTPBOOTCTRL location. The Z2-OTPBOOTCTRL location is read and decodes only if Z1-OTPBOOTCTRL is invalid or not programmed. If either Zx-OTPBOOTCTRL location is not programmed, then the device defaults to factory default operation, which is to use factory default boot mode pins to boot to flash if the boot mode pins are set to GET MODE. Users can choose the device through which to boot—SPI, I2C, CAN, and USB—by programming proper values into the user configurable DCSM OTP. More details on this can be found in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*.

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5.10.4 Peripheral Pins Used by Bootloaders

表 5-14 shows the GPIO pins used by each peripheral bootloader. This device supports two sets of GPIOs for each mode, as shown in 表 5-14.

表 5-14. GPIO Pins Used by Each Peripheral Bootloader

BOOTLOADER	GPIO PINS	NOTES
SCI-Boot0	SCITXDA: GPIO84 SCIRXDA: GPIO85	SCIA Boot I/O option 1 (default SCI option when chosen through Boot Mode GPIOs)
SCI-Boot1	SCITXDA: GPIO28 SCIRXDA: GPIO29	SCIA Boot option 2 – with alternate I/Os.
Parallel Boot	D0 – GPIO65 D1 – GPIO64 D2 – GPIO58 D3 – GPIO59 D4 – GPIO60 D5 – GPIO61 D6 – GPIO62 D7 – GPIO63 HOST_CTRL – GPIO70 DSP_CTRL – GPIO69	
CAN-Boot0	CANRXA: GPIO70 CANTXA: GPIO71	CAN-A Boot – I/O option 1
CAN-Boot1	CANRXA: GPIO62 CANTXA: GPIO63	CAN-A Boot – I/O option 2
I2C-Boot0	SDAA: GPIO91 SCLA: GPIO92	I2CA Boot – I/O option 1
I2C-Boot1	SDAA: GPIO32 SCLA: GPIO33	I2CA Boot – I/O option 2
SPI-Boot0	SPISIMOA - GPIO58 SPISOMIA - GPIO59 SPICLKA - GPIO60 SPISTEA - GPIO61	SPIA Boot – I/O option 1
SPI-Boot1	SPISIMOA – GPIO16 SPISOMIA – GPIO17 SPICLKA – GPIO18 SPISTEA – GPIO19	SPIA Boot – I/O option 2
USB Boot	USB0DM - GPIO42 USB0DP - GPIO43	The USB Bootloader will switch the clock source to the external crystal oscillator (X1 and X2 pins). A 20-MHz crystal should be present on the board if this boot mode is selected.

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5.11 Dual Code Security Module

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio™ (CSS).

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (CLA, LSx RAM, and flash sectors).

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP.

5.12 Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)
- AUXPLLCLK

5.13 Nonmaskable Interrupt With Watchdog Timer (NMIWD)

The NMIWD module is used to handle system-level errors. There is an NMIWD module for each CPU. The conditions monitored are:

- Missing system clock due to oscillator failure
- Uncorrectable ECC error on CPU access to flash memory
- Uncorrectable ECC error on CPU, CLA, or DMA access to RAM
- Vector fetch error on the other CPU
- CPU1 only: Watchdog or NMI watchdog reset on CPU2

If the CPU does not respond to the latched error condition, then the NMI watchdog will trigger a reset after a programmable time interval. The default time is 65536 SYSCLK cycles.

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5.14 Watchdog

The watchdog module is the same as the one on previous TMS320C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

図 5-5 shows the various functional blocks within the watchdog module.

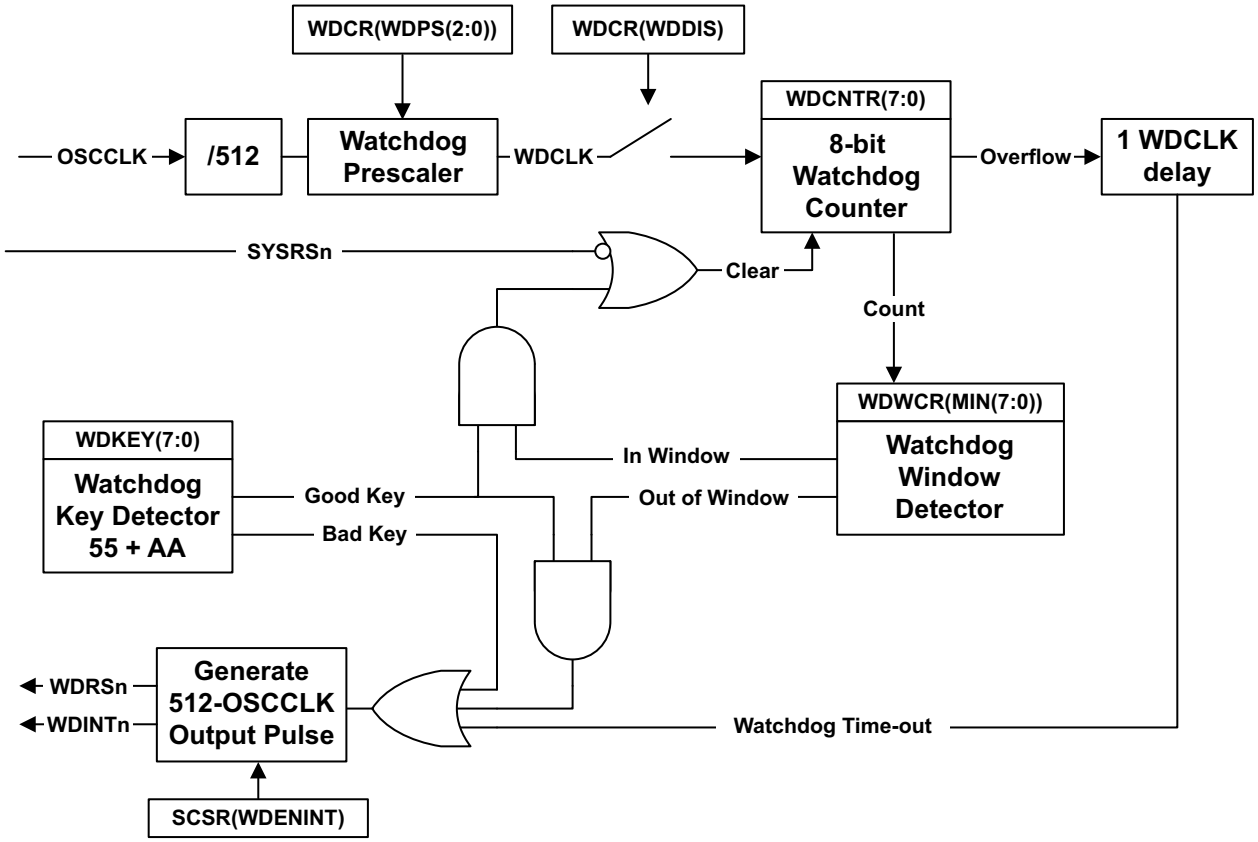


図 5-5. Windowed Watchdog

5.15 Configurable Logic Block (CLB)

TI uses the CLB to offer additional interfacing and control features for select C2000 devices. Functions that would otherwise be accomplished using external logic devices are now provided by on-chip TI solutions. For example, absolute encoder master protocol interfaces such as EnDat and BiSS are now provided as Position Manager solutions. Configuration files, application programmer's interface (API), and use examples for such solutions are provided with the C2000 controlSUITE software package. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality. In some cases, external communications transceivers may need to be added.

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6 Applications, Implementation, and Layout

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Information in the following sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 TI Design or Reference Design

TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at TIDesigns.

Industrial Servo Drive and AC Inverter Drive Reference Design

The DesignDRIVE Development Kit is a reference design for a complete industrial drive directly connecting to a three-phase ACI or PMSM motor. Many drive topologies can be created from the combined control, power, and communications technologies included on this single platform. This platform includes multiple position sensor interfaces, diverse current sensing techniques, hot-side partitioning options, and expansion for safety and industrial Ethernet.

Isolated Current Shunt and Voltage Measurement Reference Design for Motor Drives

This evaluation kit and reference design implement the AMC130x reinforced isolated delta-sigma modulators along with integrated Sinc filters in the C2000 TMS320F28377D Delfino microcontroller. The design provides an ability to evaluate the performance of these measurements: three motor currents, three inverter voltages, and the DC Link voltage. Provided in the kit is firmware to configure the Sinc filters, set the PLL frequency, and receive data from Sinc filters. A versatile run-time GUI is also provided to help the user validate the AMC130x performance and supports configuration changes to Sinc filter parameters in the Delfino controller.

Isolated, Shunt-Based Current Sensing Reference Design

This Verified TI Design implements an isolated current sensing data acqusition solution based on the AMC1304M25 isolated delta-sigma ($\Delta\Sigma$) modulator and a TMS320F28377D microcontroller. This circuit was designed for shunt-based current measurement applications, which require excellent galvanic isolation and accuracy, such as industrial motor drives, photovoltaic inverters, and energy metering. It is capable of measuring load currents from –10 A to +10 A with better than 0.3% uncalibrated accuracy, and it also provides dual functionality of a high-resolution channel and an additional overcurrent or short-circuit detection channel. The design's functionality and performance were verified against the circuit design goals by fabricating three PCBs and measuring results for dc and ac input signals.

Differential Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors

This design provides a 4-channel signal conditioning solution for differential ADCs integrated into a microcontroller measuring motor current using fluxgate sensors. Also provided is an alternative measurement circuit with external differential SAR ADCs as well as circuits for high-speed overcurrent and earth fault detection. Proper differential signal conditioning improves noise immunity on critical current measurements in motor drives. This reference design can help increase the effective resolution of the analog-to-digital conversion, improving motor drive efficiency.

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7 デバイスおよびドキュメントのサポート

TIでは、幅広い開発ツールを提供しています。デバイスの性能の評価、コードの生成、ソリューションの開発を行うためのツールとソフトウェアを、以下で紹介します。

7.1 デバイスおよび開発ツールの項目表記

製品開発サイクルの段階を示すために、TIでは TMS320™ MCUデバイスおよびサポートツールすべての型番に接頭辞が割り当てられます。それぞれのTMS320 MCUの商用ファミリ・メンバには、TMX、TMP、TMSのいずれかの接頭辞があります(たとえば、**TMS**320F28379D)。テキサス・インスツルメンツは、サポート・ツールの3つの可能な接頭辞のうち、TMDXおよびTMDSの2つを推奨しています。これらの接頭辞は、エンジニアリング・プロトタイプ(デバイスではTMX、ツールではTMDX)から、完全に認定済みの量産版デバイスとツール(デバイスではTMS、ツールではTMDS)まで、製品開発の段階を表しています。

デバイス開発の段階は次のとおりです。

TMX 実験的デバイスで、最終デバイスの電気的特性を必ずしも表しません。

TMP 最終的なシリコン・ダイで、デバイスの電気的特性に適合しますが、品質および信頼性の検証は完了していません。

TMS 完全に認定済みの量産版デバイスです。

サポート・ツール開発の段階は次のとおりです。

TMDX 開発サポート製品で、テキサス・インスツルメンツの社内認定試験はまだ完了していません。

TMDS 完全に認定済みの開発サポート製品です。

TMXおよびTMPデバイスと、TMDX開発サポート・ツールは、以下の免責事項の下で出荷されます。
「開発段階の製品は、社内での評価を目的としたものです」

TMSデバイスとTMDS開発サポート・ツールの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されてきました。TIの標準保証が適用されます。

プロトタイプ・デバイス(TMXまたはTMP)の方が標準的な製品版デバイスに比べて故障率が大きいと予測されます。これらのデバイスは予測される最終使用時の故障率が未定義であるため、テキサス・インスツルメンツではそれらのデバイスを本稼動システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、パッケージの種類 (例: PTP) と温度範囲 (例: T) を示しています。図 7-1に、任意のファミリ・メンバについて、完全なデバイス名を読み取るための凡例を示します。

デバイスの型番と詳しい注文情報については、TIのWebサイト(www.ti.com)を参照するか、TIの販売代理店にお問い合わせください。

ダイのデバイス項目表記マーキングについて、さらに詳しい説明は、『*TMS320F2837xD デュアルコア Delfino™ MCU シリコン正誤表*』をご覧ください。

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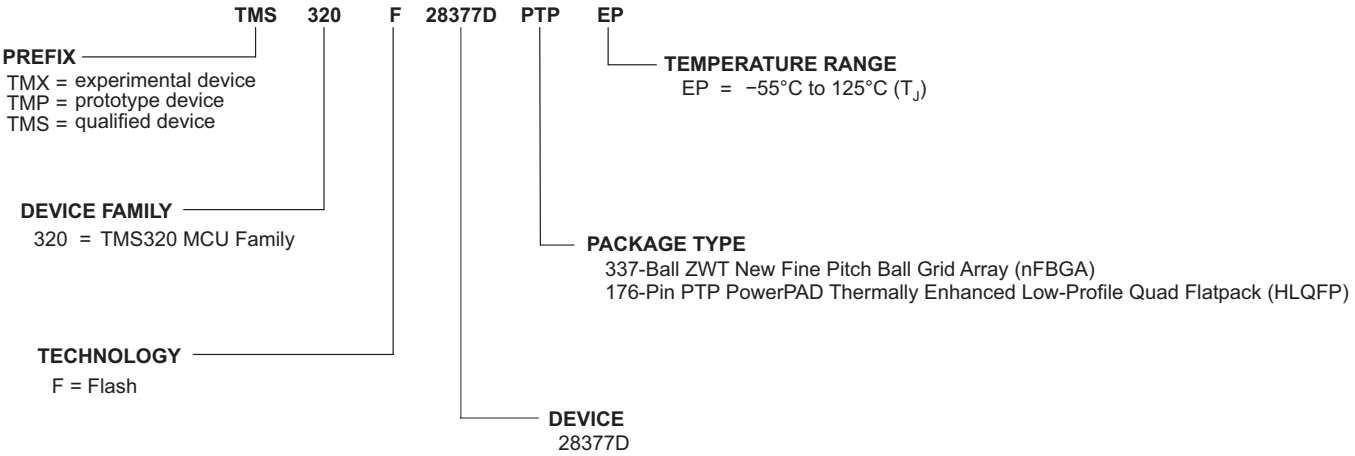


図 7-1. デバイスの項目表記

7.2 ツールとソフトウェア

TIでは、幅広い開発ツールを提供しています。ツールおよびソフトウェアの一部は、デバイスの性能評価や、コードの生成に使用され、以下に示すようなソリューションの開発が行われます。C2000™リアルタイム制御MCU用に利用できるすべてのツールおよびソフトウェアを参照するには、「C2000　MCUのツールとソフトウェア」ページをご覧ください。

開発ツール

C2000用のF28379D controlCARDリアルタイム制御開発キット
テキサス・インスツルメンツ製のDelfino F28379D controlCARDはPosition Manager対応で、システム・プロトタイプ、テスト・スタンド、その他高性能コントローラに簡単にアクセスする必要がある多くのプロジェクト用の、初期ソフトウェア開発および短期使用ビルドに理想的な製品です。すべての C2000 controlCARD は包括的なボードレベル・モジュールで、HSEC180またはDIMM100フォーム・ファクタを利用して、薄型のシングルボード・コントローラ・ソリューションを実現します。ホスト・システムが5Vの単一電源レールをcontrolCARDに供給するだけで、controlCARDのすべての機能を使用できます。

F28379D Delfino実験キット
C2000™ MCU実験キットは、テキサス・インスツルメンツのC2000 32ビットマイクロコントローラ・ファミリを使用して、リアルタイム、閉ループ制御開発を行うための、堅牢なハードウェア・プロトタイプ作成プラットフォームです。このプラットフォームは、モータ制御、デジタル電源、ソーラー・インバータ、デジタルLED照明、高精度センシングなど、多くのパワー・エレクトロニクス・アプリケーション用のソリューションをカスタマイズして実証するための、優れたツールです。

ソフトウェア・ツール

C2000 MCU用C2000Ware
C2000™マイクロコントローラ用のC2000Wareは、開発ソフトウェアおよびドキュメントの総合的なセットで、ソフトウェア開発時間を最小化できるよう設計されています。特定デバイスのドライバやライブラリから、デバイス・ペリフェラルのサンプルに至るまで、C2000Wareは開発と評価を開始するための堅牢な土台を提供します。C2000Wareは現在、controlSUITE™に対して推奨されるコンテンツ配信ツールです。

controlSUITE™ソフトウェア・スイート
C2000マイクロコントローラ用のcontrolSUITE™は、ソフトウェアの開発期間を最短にするように設計された、ソフトウェア・インフラとソフトウェア・ツールの総合的なセットです。

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C2000マイクロコントローラ用の Code Composer Studio™ (CCS)統合開発環境(IDE)
Code Composer Studioは、TIのマイクロコントローラおよび組み込みプロセッサ・ポートフォリオをサポートする統合開発環境(IDE)です。Code Composer Studioは、組み込みアプリケーションの開発およびデバッグに必要な一連のツールで構成されています。最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。IDEは直感的で、アプリケーションの開発フローの各段階を、すべて同一のユーザー・インターフェイスで実行できます。使い慣れたツールとインターフェイスにより、ユーザーは従来より迅速に作業を開始できます。Code Composer Studioは、Eclipseソフトウェア・フレームワークの利点と、TIの先進的な組み込みデバッグ機能の利点を組み合わせ、組み込み製品の開発者向けの魅力的な、豊富な機能を持つ開発環境を実現します。

Pin Muxツール
Pin Muxユーティリティは、TI MPUのピン多重化設定を構成し、競合を解決し、I/Oセルの特性を指定するためのグラフィカル・ユーザー・インターフェイスを提供する、ソフトウェア・ツールです。

F021フラッシュ・アプリケーション・プログラミング・インターフェイス(API)
F021フラッシュ・アプリケーション・プログラミング・インターフェイス(API)は、F021オンチップ・フラッシュ・メモリをプログラム、消去、および確認するための機能を含むソフトウェア・ライブラリを提供します。

トレーニング

設計エンジニアがC2000マイクロコントローラの機能および性能を十分に活用できるよう、TIは各種のトレーニング・リソースを開発しました。オンライン・トレーニング資料や、ダウンロード可能な実践的ワークショップを活用することで、C2000マイクロコントローラ・ファミリの完全な動作の知識を簡単に習得できます。これらのトレーニング資料は、習得を容易にし、開発期間を短縮し、製品を短期間で開発できるよう設計されています。各種のトレーニング資料の詳細については、C2000™リアルタイム制御MCUのサポートおよびトレーニングサイトをご覧ください。

F2837xD/F2837xS/F2807x固有の実践的トレーニング資料は、次のサイトにあります。

- C2000の複数日ワークショップ
- C2000の1日ワークショップ

7.3 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではマイクロプロセッサ(MPU)とサポート・ツールのすべての型番に接頭辞が割り当てられています。各デバイスには、X、P、null (接頭辞なし)のいずれかの接頭辞があります(例: *ご利用のデバイス*)。テキサス・インスツルメンツは、サポート・ツールの3つの可能な接頭辞のうち、TMDXおよびTMDSの2つを推奨しています。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(TMDX)から、完全認定済みの量産デバイス/ツール(TMDS)まであります。

デバイス開発の段階は次のとおりです。

X 実験的デバイス。最終デバイスの電気的特性を必ずしも表さず、量産アセンブリ・フローを使用しない可能性があります。

P プロトタイプ・デバイス。最終的なシリコン・ダイとは限らず、最終的な電気的特性を満たさない可能性があります。

空白 認定済みのシリコン・ダイの量産バージョン。

サポート・ツール開発の段階は次のとおりです。

TMDX 開発サポート製品。テキサス・インスツルメンツの社内認定試験はまだ完了していません。

TMDS 完全に認定済みの開発サポート製品です。

XおよびPデバイスとTMDX開発サポート・ツールは、以下の免責事項の下で出荷されます。

製品開発サイクルの段階を示すために、TIではDSPデバイスとサポート・ツールすべての型番に接頭辞を割り当てます。それぞれのDSP商用ファミリ・メンバには、TMX、TMP、TMSのいずれかの接頭辞があります(例: *ご利用のデバイス*)。テキサス・インスツルメンツは、サポート・ツールの3つの可能な接頭辞のうち、TMDXおよびTMDSの2つを推奨しています。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(TMXおよびTMDX)から、完全認定済みの量産デバイス/ツール(TMSおよびTMDS)まであります。

デバイス開発の段階は次のとおりです。

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TMX 実験的デバイス。最終デバイスの電気的特性を必ずしも表さず、量産アセンブリ・フローを使用しない可能性があります。

TMP プロトタイプ・デバイス。最終的なシリコン・ダイとは限らず、最終的な電気的特性を満たさない可能性があります。

TMS 認定済みのシリコン・ダイの量産バージョン。

サポート・ツール開発の段階は次のとおりです。

TMDX 開発サポート製品。テキサス・インスツルメンツの社内認定試験はまだ完了していません。

TMDS 完全に認定済みの開発サポート製品です。

TMXおよびTMPデバイスとTMDX開発サポート・ツールは、以下の免責事項の下で出荷されます。

「開発中の製品は、社内での評価用です。」

量産デバイスおよびTMDS開発サポート・ツールの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XまたはP)の方が標準的な量産デバイスに比べて故障率が大きいと予測されます。これらのデバイスは予測される最終使用時の故障率が未定義であるため、テキサス・インスツルメンツではそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、パッケージのタイプ(例: *ご利用のパッケージ*)、温度範囲(たとえば、空白はデフォルトの商業用温度範囲)、およびデバイスの速度範囲をMHz単位で表します(例: *ご利用のデバイスの速度範囲*)。任意の*ご利用のデバイス*について、完全なデバイス名の読み方の凡例を、図 7-2に示します。

*ご利用のパッケージタイプのご利用のデバイス*の注文可能な部品番号については、このドキュメントにあるパッケージ・オプションについての付録またはti.comをご覧になるか、御社のTI販売代理店にお問い合わせください。

ダイにあるデバイスの項目表記マーキングの詳細な説明については、*シリコン正誤表*を参照してください。

図 7-2. デバイスの項目表記

7.4 ドキュメントのサポート

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

プロセッサおよび関連ペリフェラルに関する最新ドキュメント、その他の技術資料を以下に示します。

正誤表

『TMS320F2837xD デュアルコアDelfino™ MCUのシリコン正誤表』には、シリコンについての既知の勧告事項と対策が記載されています。

テクニカル・リファレンス・マニュアル

『TMS320F2837xD デュアルコアDelfinoマイクロコントローラ・テクニカル・リファレンス・マニュアル』には、2837xDマイクロコントローラの各ペリフェラルおよびサブシステムについて、統合、環境、機能説明、プログラミング・モデルの詳細が記載されています。

CPUユーザー・ガイド

『TMS320C28x CPU および命令セット・リファレンス・ガイド』には、TMS320C28x固定小数点デジタル信号プロセッサ(DSP)のCPU (Central Processing Unit)およびアセンブリ言語命令について記述されています。このリファレンス・ガイドには、これらのDSPで利用可能なエミュレーション機能についても解説されています。

『TMS320C28x拡張命令セット・テクニカル・リファレンス・マニュアル』には、TMU、VCU-II、およびFPUアクセラレータのアーキテクチャ、パイプライン、および命令セットについて記述されています。

ペリフェラル・ガイド

『C2000リアルタイム制御ペリフェラル・リファレンス・ガイド』には、28x DSPのペリフェラル・リファレンス・ガイドが記載されています。

ツール・ガイド

『TMS320C28xアセンブリ言語ツールv17.6.0.STSユーザー・ガイド』には、TMS320C28xデバイス用のアセンブリ言語ツール(アセンブリ言語コードを開発するためのアセンブラや他のツール)、アセンブラのディレクティブ、マクロ、一般的なオブジェクト・ファイルのフォーマット、およびシンボリック・デバッグ・ディレクティブについて記述されています。

『TMS320C28x最適化C/C++コンパイラv17.6.0.STSユーザー・ガイド』には、TMS320C28x C/C++コンパイラについて記述されています。このコンパイラは、ANSI標準C/C++ソースコードを受け付け、TMS320C28xデバイス用のTMS320 DSPアセンブリ言語ソースコードを生成します。

『TMS320C28x命令セット・シミュレータの技術的概要』には、TMS320C2000 IDE用のCode Composer Studio内で利用可能な、C28xコアの命令セットをシミュレートするシミュレータについて記述されています。

アプリケーション・レポート

『半導体のパッキング手法』には、半導体デバイスをエンド・ユーザーへの配送用に準備するためのパッキング手法について記述されています。

『組み込みプロセッサの有効寿命の計算』には、TIの組み込みプロセッサ(EP)を電子機器システムで、電力を供給して使用したときの有効寿命を計算するための手法が解説されています。これは、TI EPの信頼性が最終システムの信頼性要件を満たすかどうかを判定したい一般的なエンジニアを対象としています。

『TMS320C28xデジタル信号コントローラの基礎』には、TMS320C28x DSPのソフトウェアおよびハードウェアの開発を開始するとき、最初の設計やデバッグ作業に役立つヒントが紹介されています。

7.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.6 商標

PowerPAD, Delfino, TMS320C2000, C2000, controlSUITE, Code Composer Studio, TMS320, E2E are trademarks of Texas Instruments.
Bosch is a registered trademark of Robert Bosch GmbH Corporation.
All other trademarks are the property of their respective owners.

7.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。



静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

7.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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8 メカニカル、パッケージ、および注文情報

8.1 ビア・チャネル

ご利用のパッケージは、ビア・チャネル・テクノロジを使用して特別に設計されたものです。これにより、通常より大きなPCBビアおよびトレース・サイズが可能になり、0.65mmピッチのパッケージでのPCB設計に使用されるPCB信号レイヤ数が減少し、PCBのコストが大幅に削減されています。ビア・チャネルBGAテクノロジのレイヤ効率向上により、わずか2つの信号レイヤ(合計4レイヤ)でPCBの配線が可能です。

[ご*利用のパッケージ*]パッケージに実装されているビア・チャネル・テクノロジにより、[ご*利用のデバイス*]ベースの製品を4レイヤのPCBで構築できますが、4レイヤのPCBがシステムの性能目標を満たすとは限りません。このため、製品設計の段階で4レイヤPCB設計のシステム性能を評価する必要があります。

8.2 パッケージ情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320F28377DGWTEP	Active	Production	NFBGA (GWT) | 337	90 | JEDEC TRAY (10+1)	No	SNPB	Level-3-220C-168 HR	-55 to 125	TMS320 F28377DGWTEP
TMS320F28377DPTPEP	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TMS320 F28377DPTPEP
V62/18601-01XF	Active	Production	NFBGA (GWT) | 337	90 | JEDEC TRAY (10+1)	No	SNPB	Level-3-220C-168 HR	-55 to 125	TMS320 F28377DGWTEP
V62/18601-01YE	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TMS320 F28377DPTPEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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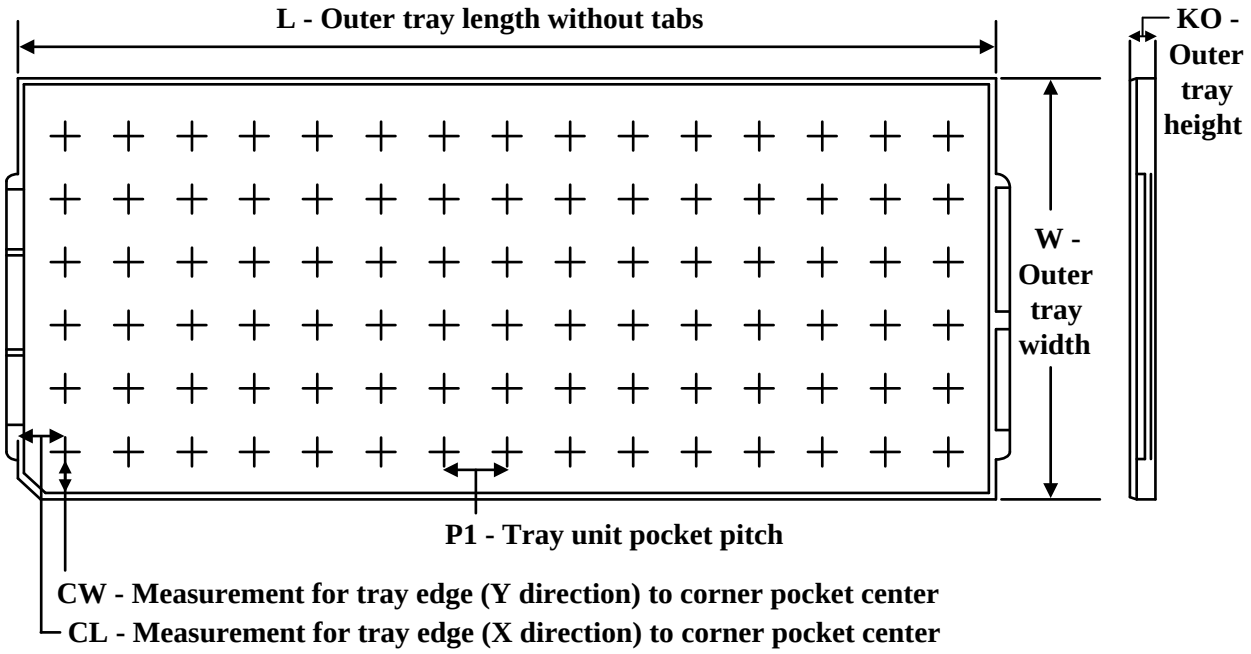
OTHER QUALIFIED VERSIONS OF TMS320F28377D-EP :

- Catalog : TMS320F28377D
- Automotive : TMS320F28377D-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F28377DGWTEP	GWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
TMS320F28377DPTPEP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
V62/18601-01XF	GWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
V62/18601-01YE	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7

GENERIC PACKAGE VIEW

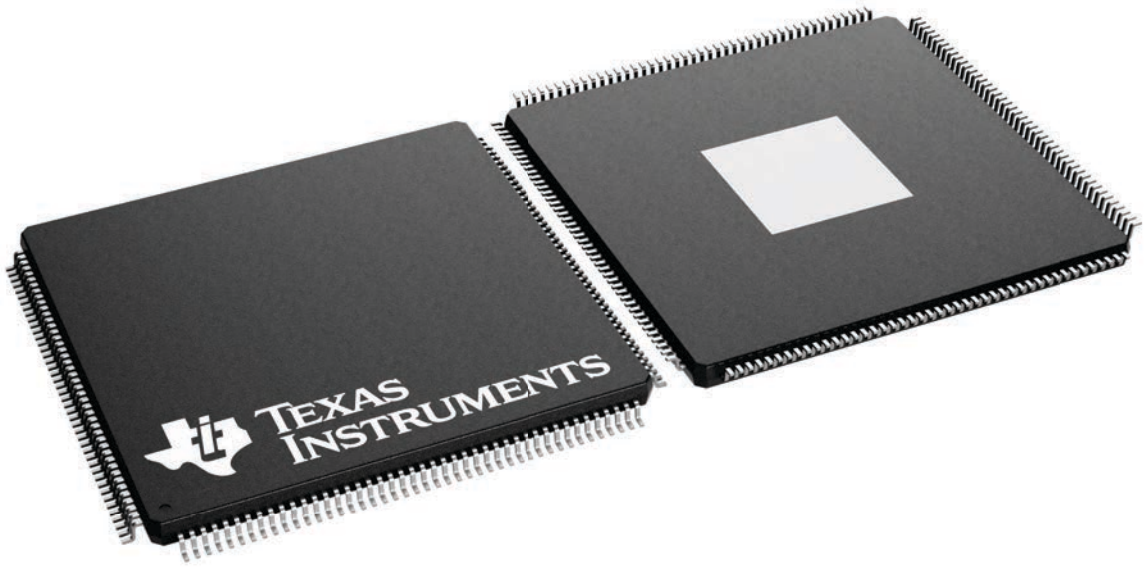
PTP 176

HLQFP - 1.6 mm max height

24 x 24, 0.5 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



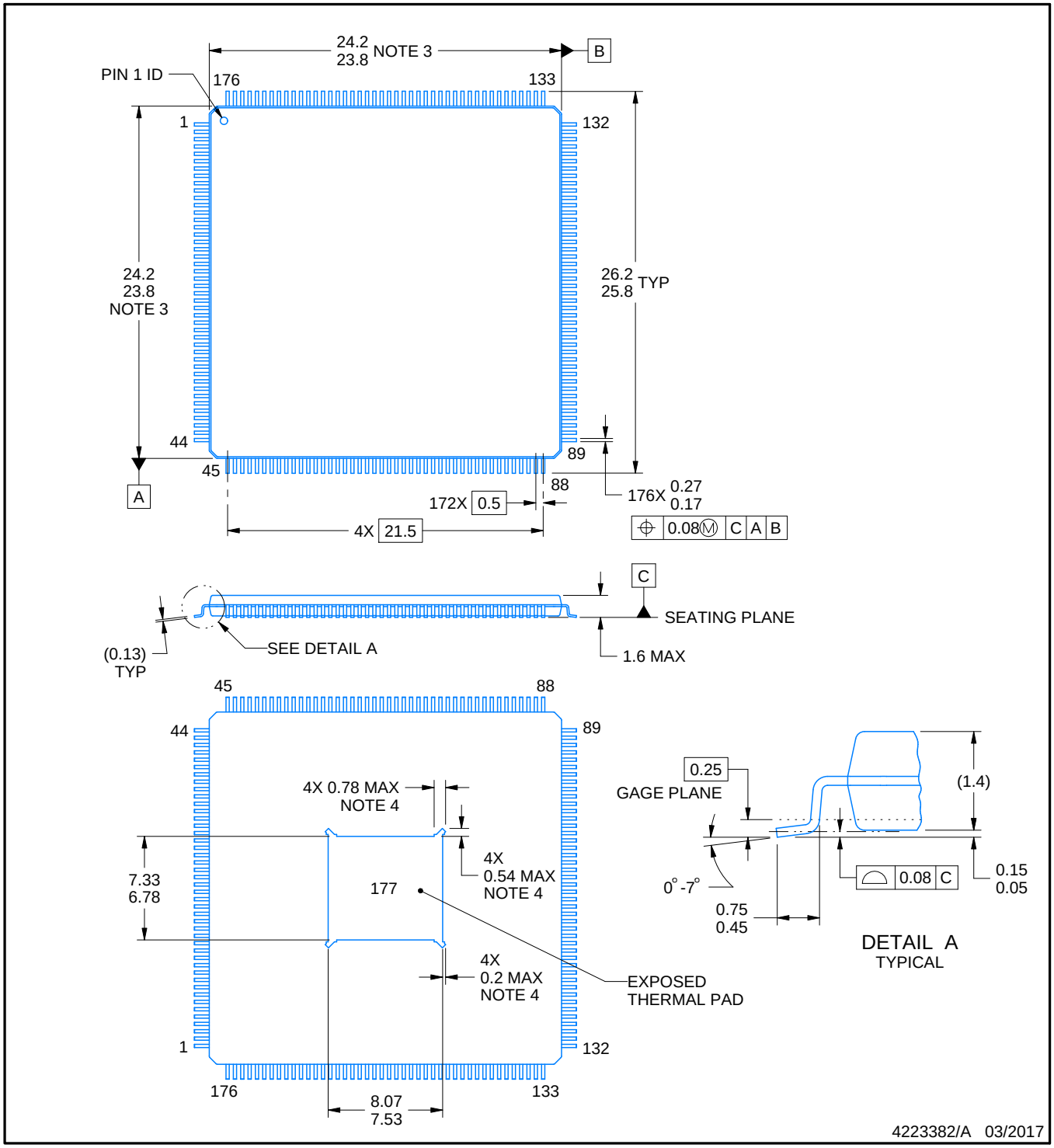
4226435/A

PACKAGE OUTLINE

PTP0176F

PowerPAD™ HLQFP - 1.6 mm max height

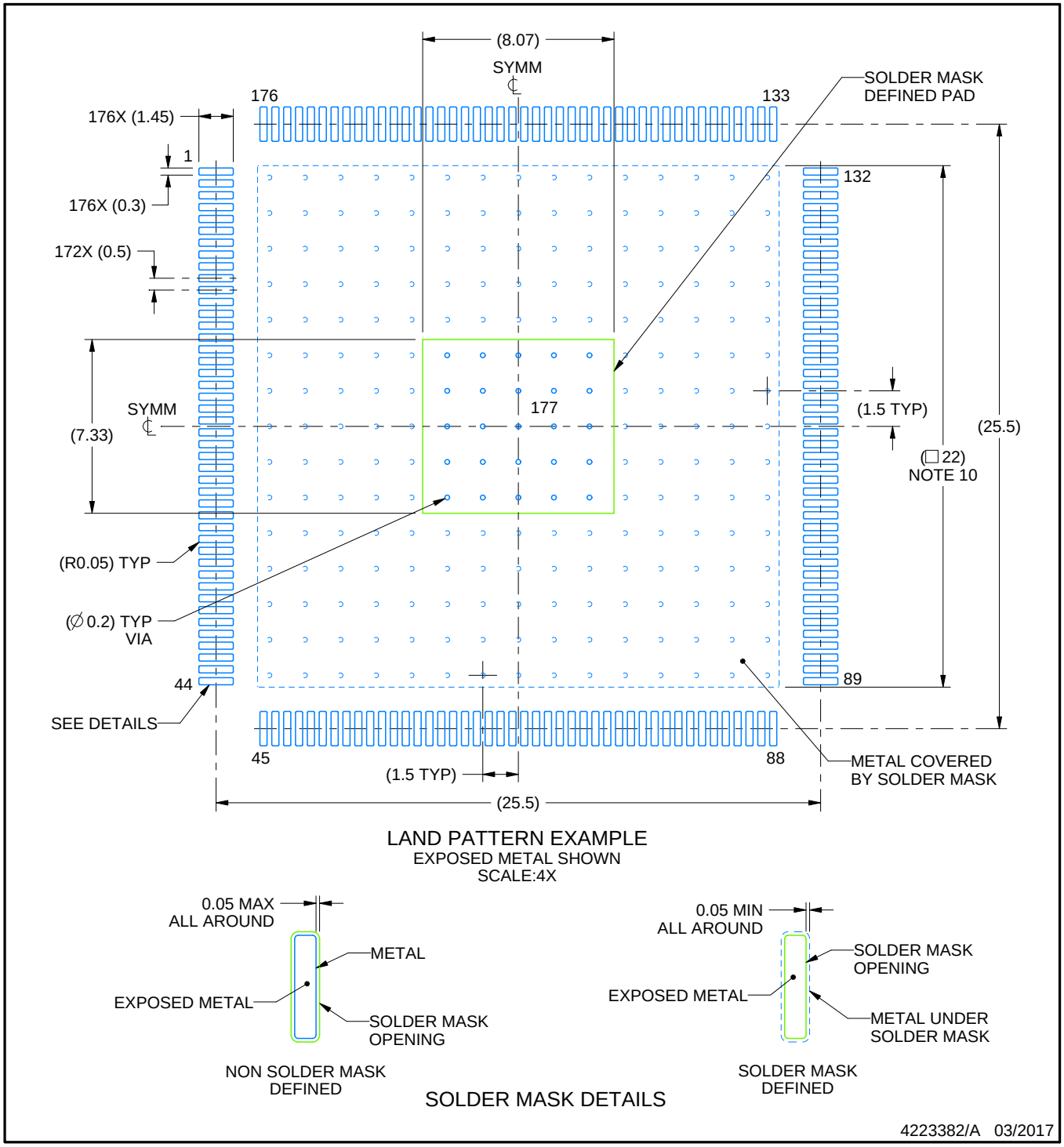
PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

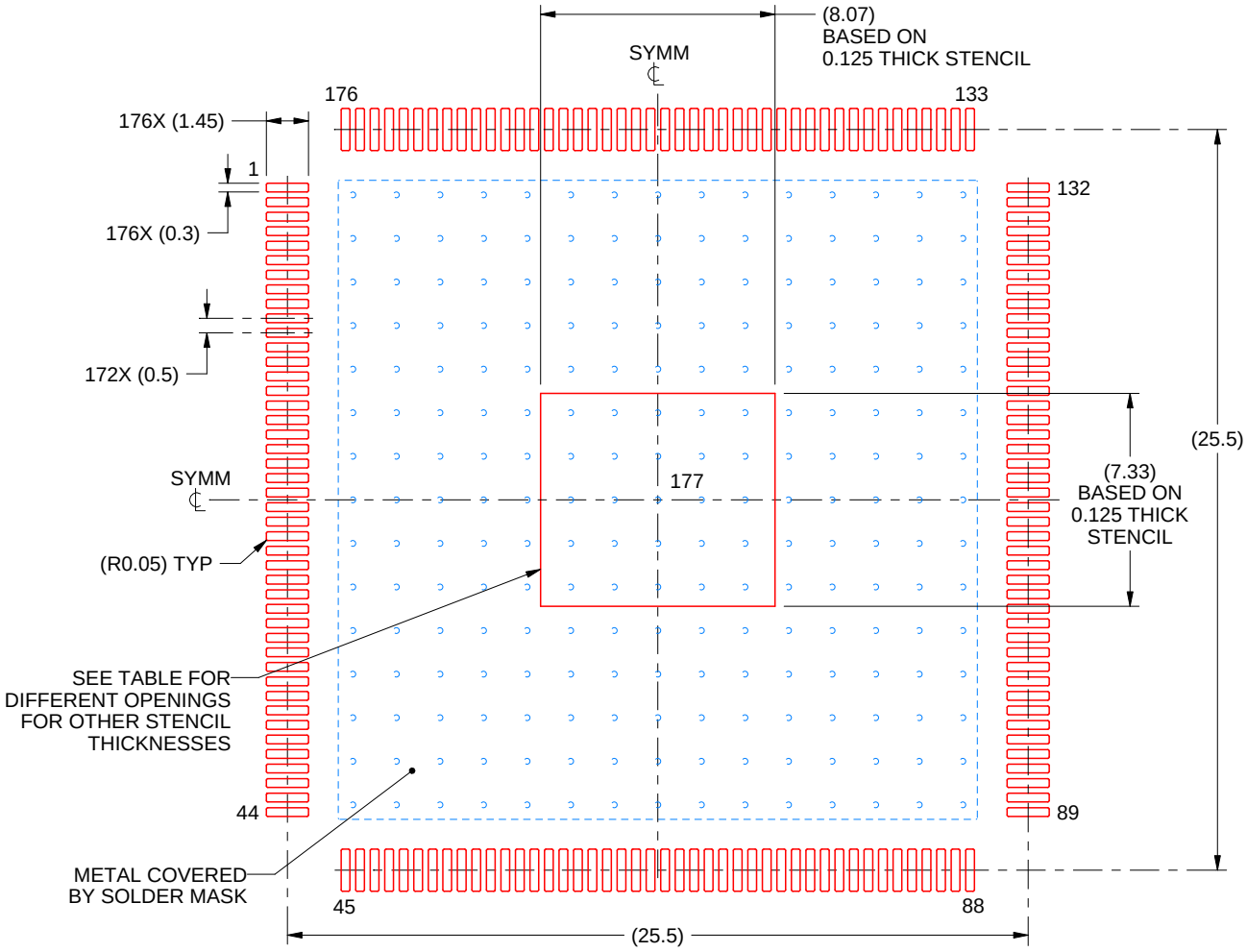
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features my not present.
5. Reference JEDEC registration MS-026.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:4X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	9.02 X 8.2
0.125	8.07 X 7.33 (SHOWN)
0.150	7.37 X 6.69
0.175	6.82 X 6.2

4223382/A 03/2017

NOTES: (continued)

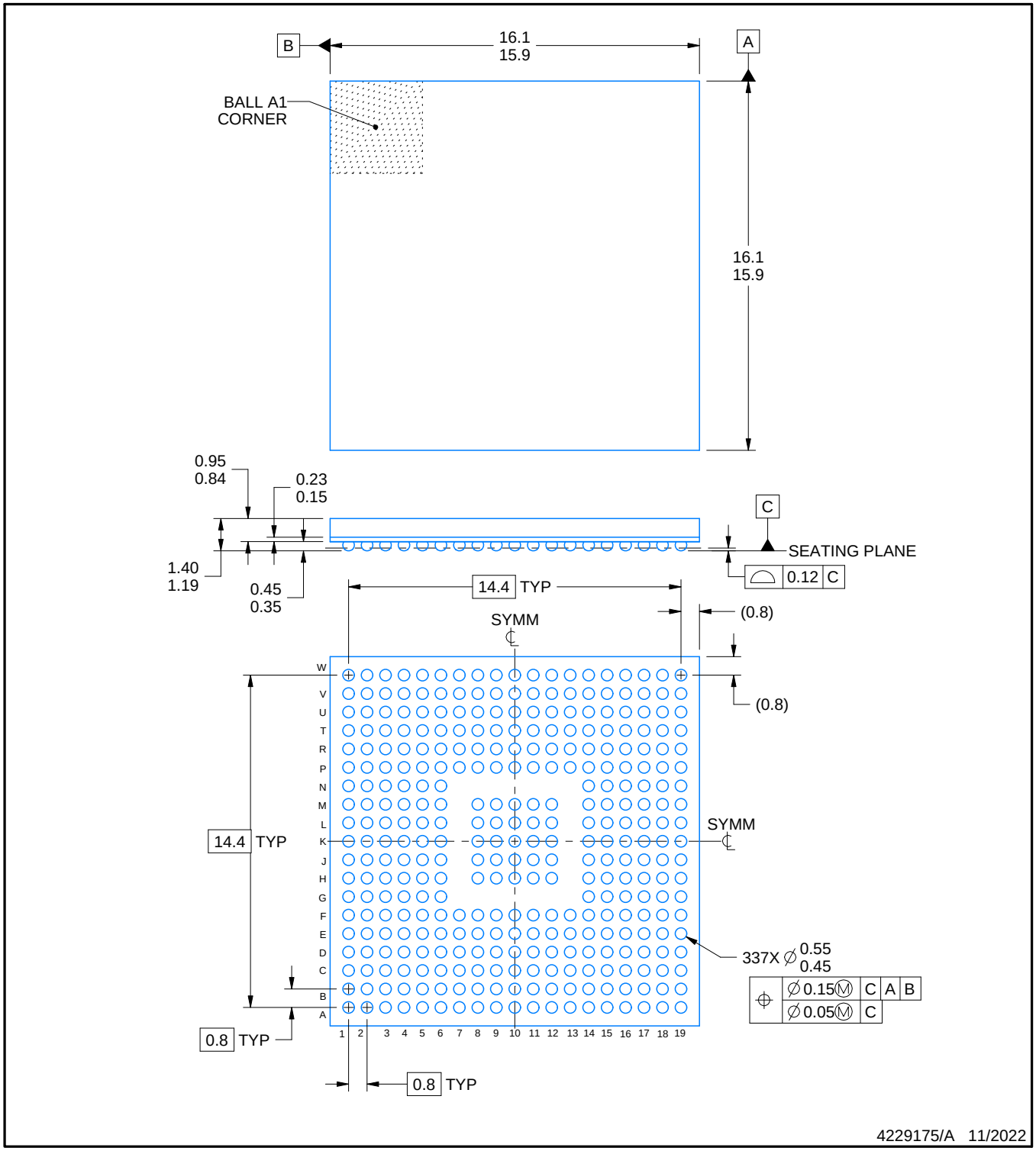
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

GWT0337A

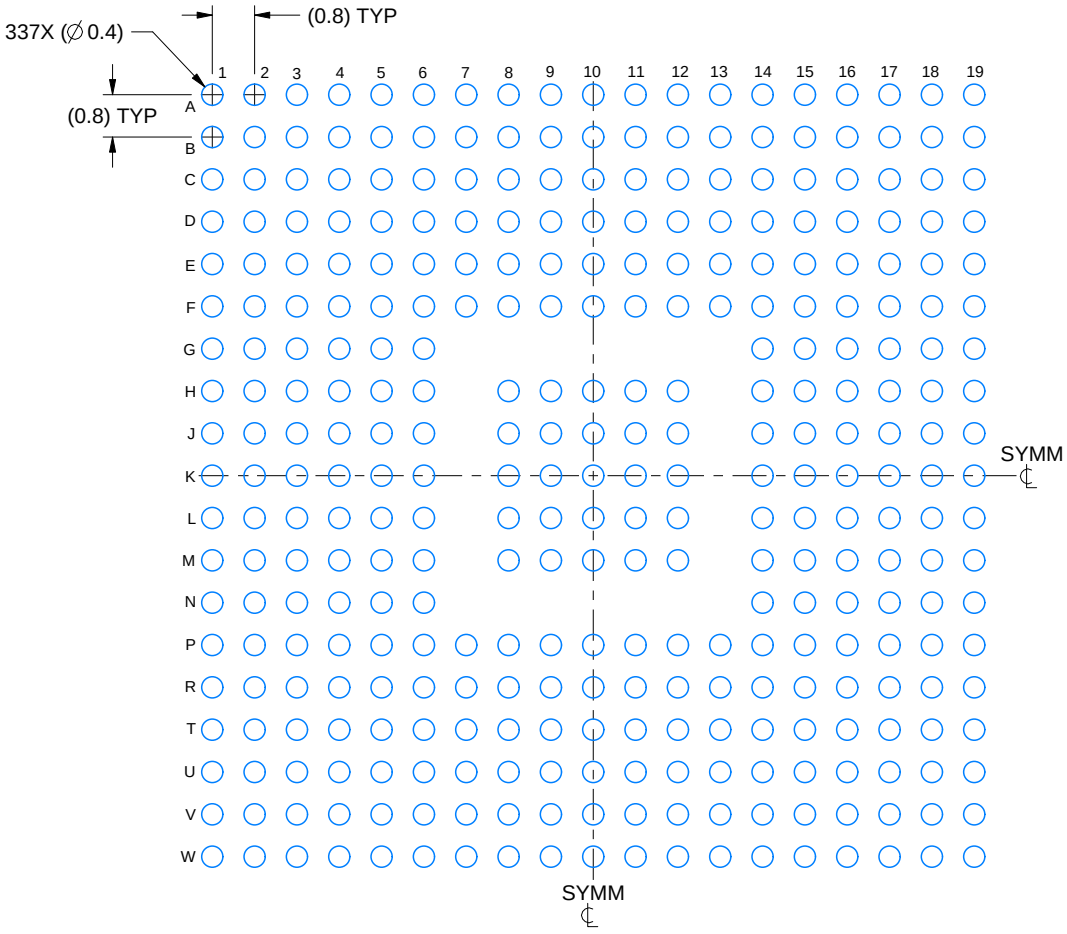
NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X

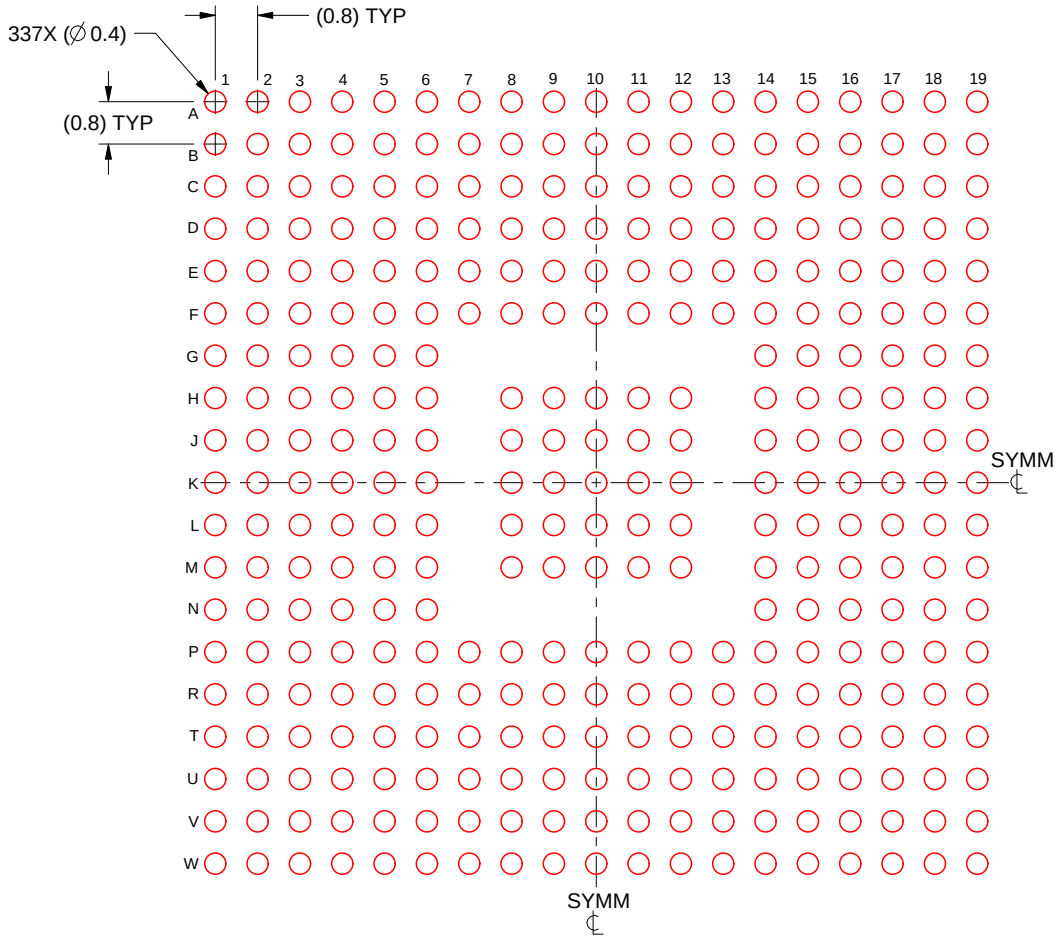


SOLDER MASK DETAILS
NOT TO SCALE

4229175/A 11/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 7X

4229175/A 11/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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