

TMUX110x 5V、低リーク電流、1:1 (SPST) 高精度スイッチ

1 特長

- 幅広い電源電圧範囲: 1.08V～5.5V
- 小さいリーク電流: 3pA
- 少ない電荷注入: -1.5pC
- 低いオン抵抗: 1.8Ω
- 40°C～+125°Cの動作温度範囲
- 1.8V ロジック互換
- フェイルセーフ ロジック
- レールツーレールの動作
- 双方向の信号パス
- ブレイクビフォー メイクのスイッチング動作
- ESD 保護 (HBM): 2000V

2 アプリケーション

- サンプル アンド ホールド回路
- 帰還ゲイン スイッチング
- 信号絶縁
- フィールドトランシミッタ
- プログラマブル ロジック コントローラ (PLC)
- ファクトリ オートメーション / 制御
- 超音波スキャナ
- メディカル モニタと診断
- 心電図 (ECG)
- データ アクイジション システム (DAQ)
- 半導体試験機器
- バッテリ テスト機器
- 計測機器: ラボ、分析、ポータブル
- 超音波スマート メータ: 水道およびガス
- 光ネットワーク
- 光学テスト機器

3 概要

TMUX1101 および TMUX1102 は、高精度の CMOS (相補型金属酸化膜半導体) 単極单投 (SPST) スイッチです。1.08V～5.5V の広い電源電圧範囲で動作するため、医療機器から産業システムまで、幅広い用途に適しています。このデバイスは、ソース (S) ピンおよびドレイン (D) ピンで、GND から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。

ロジック制御入力 (SEL) には 1.8V ロジック互換のスレッショルドがあり、有効な電源電圧範囲で動作していれば、TTL と CMOS 両方のロジックとの互換性が確保されます。TMUX1101 のスイッチは SEL がロジック 1 のときにオンになり、TMUX1102 は SEL がロジック 0 のときにオンになります。フェイルセーフ ロジック回路により、電源ピンよりも前に SEL ピンに電圧が印加されるため、デバイスの損傷を防ぐことができます。

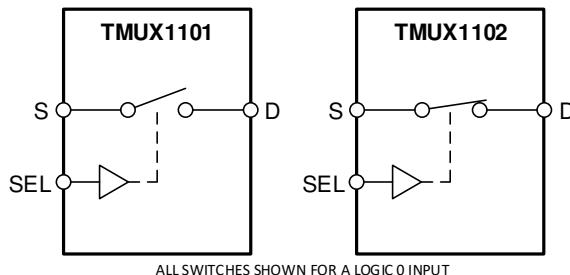
TMUX110x デバイスは、高精度スイッチおよびマルチプレクサのファミリーの製品です。これらのデバイスは、オンおよびオフ時のリーク電流が非常に小さく、電荷注入も少ないため、高精度の測定アプリケーションに使用できます。消費電流が 3nA と低く、小さいパッケージ オプションが存在するため、携帯型アプリケーションでも使用できます。

製品情報

部品番号	制御ロジック ⁽¹⁾	パッケージ ⁽²⁾
TMUX1101	アクティブ HIGH	DCK (SC70, 5)
TMUX1102	アクティブ LOW	DBV (SOT-23, 5)

(1) 製品比較表を参照してください。

(2) 詳細については、セクション 12 を参照してください。



TMUX110x ブロック図



このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX1101	Low-Leakage-Current, 1:1 (SPST), Precision Switch (Logic High)
TMUX1102	Low-Leakage-Current, 1:1 (SPST), Precision Switch (Logic Low)

5 Pin Configuration and Functions

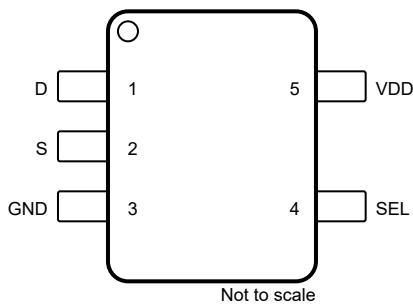


図 5-1. DCK Package 5-Pin SC70 (Top View)

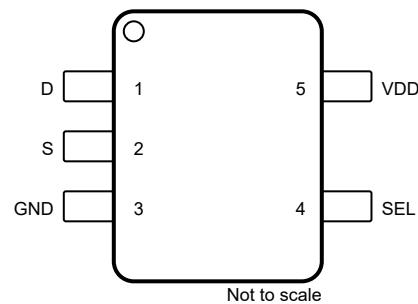


図 5-2. DBV Package 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
D	1	I/O	Drain pin. Can be an input or output.
S	2	I/O	Source pin. Can be an input or output.
GND	3	P	Ground (0V) reference
SEL	4	I	Logic control input. Controls the switch state as shown in セクション 8.4.1 .
VDD	5	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.

(1) I = input, O = output, I/O = input and output, and P = power.

(2) Refer to [セクション 8.4](#) for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾

		MIN	MAX	UNIT
V_{DD}	Supply voltage	-0.5	6	V
V_{SEL}	Logic control input pin voltage (SELx)	-0.5	6	V
I_{SEL}	Logic control input pin current (SELx)	-30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	-0.5	$V_{DD}+0.5$	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, Dx)	$I_{DC} \pm 10\%^{(4)}$	$I_{DC} \pm 10\%^{(4)}$	mA
I_S or I_D (PEAK)	Source and drain peak current: (1 ms period max, 10% duty cycle maximum) (Sx, Dx)	$I_{peak} \pm 10\%^{(4)}$	$I_{peak} \pm 10\%^{(4)}$	mA
T_{stg}	Storage temperature	-65	150	°C
P_{tot}	Total power dissipation ⁽⁵⁾ ⁽⁶⁾		250	mW
T_J	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) Refer to Recommended Operating Conditions for I_{DC} and I_{Peak} ratings.
- (5) For DBV(SOT-23) package: P_{tot} derates linearly above $TA = 93^\circ\text{C}$ by $4.45\text{mW/}^\circ\text{C}$.
- (6) For DCK(SC70) package: P_{tot} derates linearly above $TA = 62^\circ\text{C}$ by $2.87\text{mW/}^\circ\text{C}$.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	± 750

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.08	5.5	V	
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, Dx)	0	V_{DD}	V	
V_{SEL}	Logic control input pin voltage (SELx)	0	5.5	V	
T_A	Ambient temperature	-40	125	°C	
I_{DC}	Continuous current through switch	$T_J = 25^\circ\text{C}$	150	mA	
		$T_J = 85^\circ\text{C}$	120	mA	
		$T_J = 125^\circ\text{C}$	60	mA	
		$T_J = 130^\circ\text{C}$	50	mA	
I_{peak}	Peak current through switch (1 ms period max, 10% duty cycle maximum)	$T_J = 25^\circ\text{C}$	300	mA	
		$T_J = 85^\circ\text{C}$	300	mA	
		$T_J = 125^\circ\text{C}$	180	mA	
		$T_J = 130^\circ\text{C}$	160	mA	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX1101 / TMUX1102		UNIT
		DCK (SC70)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	348.5	224.9	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	238.3	150.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	205.7	130.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	141.4	74.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	204.7	129.3	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics ($V_{DD} = 5V \pm 10\%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH						
R_{ON}	On-resistance Refer to On-resistance	$V_S = 0\text{V}$ to V_{DD} $I_{SD} = 10\text{mA}$	25°C	1.8	4	Ω
			-40°C to +85°C		4.5	Ω
			-40°C to +125°C		4.9	Ω
$R_{ON\text{ FLAT}}$	On-resistance flatness Refer to On-resistance	$V_S = 0\text{V}$ to V_{DD} $I_{SD} = 10\text{mA}$	25°C	0.85		Ω
			-40°C to +85°C		1.6	Ω
			-40°C to +125°C		1.6	Ω
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾ Refer to Off-leakage current	$V_{DD} = 5\text{V}$ Switch Off $V_D = 4.5\text{V} / 1.5\text{V}$ $V_S = 1.5\text{V} / 4.5\text{V}$	25°C	-0.08	± 0.005	0.08
			-40°C to +85°C	-0.3		nA
			-40°C to +125°C	-0.9		nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾ Refer to Off-leakage current	$V_{DD} = 5\text{V}$ Switch Off $V_D = 4.5\text{V} / 1.5\text{V}$ $V_S = 1.5\text{V} / 4.5\text{V}$	25°C	-0.08	± 0.005	0.08
			-40°C to +85°C	-0.3		nA
			-40°C to +125°C	-0.9		nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current Refer to On-leakage current	$V_{DD} = 5\text{V}$ Switch On $V_D = V_S = 2.5\text{V}$	25°C	-0.025	± 0.003	0.025
			-40°C to +85°C	-0.2		nA
			-40°C to +125°C	-0.95		nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current Refer to On-leakage current	$V_{DD} = 5\text{V}$ Switch On $V_D = V_S = 4.5\text{V} / 1.5\text{V}$	25°C	-0.1	± 0.01	0.1
			-40°C to +85°C	-0.35		nA
			-40°C to +125°C	-2		nA
LOGIC INPUTS (SEL)						
V_{IH}	Input logic high		-40°C to +125°C	1.49	5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0	0.87	V
I_{IH} I_{IL}	Input leakage current		25°C	± 0.005		µA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C	± 0.06		µA
C_{IN}	Logic input capacitance		25°C	1		pF
C_{IN}	Logic input capacitance		-40°C to +125°C		2	pF

6.5 Electrical Characteristics ($V_{DD} = 5V \pm 10\%$) (続き)

at $T_A = 25^\circ C$, $V_{DD} = 5V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V _{DD} supply current	Logic inputs = 0V or 5.5V	25°C	0.003		μA	
			-40°C to +125°C	1		μA	
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 3V$ $R_L = 200\Omega$, $C_L = 15pF$ Refer to Transition time	25°C	12		ns	
			-40°C to +85°C	17		ns	
			-40°C to +125°C	18		ns	
Q_C	Charge Injection	$V_S = 1V$ $R_S = 0\Omega$, $C_L = 1nF$ Refer to Charge injection	25°C	-1.5		pC	
O_{ISO}	Off Isolation	$R_L = 50\Omega$, $C_L = 5pF$ $f = 1MHz$ Refer to Off isolation	25°C	-62		dB	
		$R_L = 50\Omega$, $C_L = 5pF$ $f = 10MHz$ Refer to Off isolation	25°C	-40		dB	
BW	Bandwidth	$R_L = 50\Omega$, $C_L = 5pF$ Refer to Bandwidth	25°C	300		MHz	
C_{SOFF}	Source off capacitance	$f = 1MHz$	25°C	6		pF	
C_{DOFF}	Drain off capacitance	$f = 1MHz$	25°C	10		pF	
C_{SON} C_{DON}	On capacitance	$f = 1MHz$	25°C	17		pF	

(1) When V_S is 4.5V, V_D is 1.5V or when V_S is 1.5V, V_D is 4.5V.

6.6 Electrical Characteristics ($V_{DD} = 3.3V \pm 10\%$)

at $T_A = 25^\circ C$, $V_{DD} = 3.3V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0V$ to V_{DD} $I_{SD} = 10mA$ Refer to On-resistance	25°C	3.7		8.8	Ω
			-40°C to +85°C	9.5		Ω	
			-40°C to +125°C	9.8		Ω	
$R_{ON,FLAT}$	On-resistance flatness	$V_S = 0V$ to V_{DD} $I_{SD} = 10mA$ Refer to On-resistance	25°C	1.9		Ω	
			-40°C to +85°C	2		Ω	
			-40°C to +125°C	2.2		Ω	
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 3.3V$ Switch Off $V_D = 3V / 1V$ $V_S = 1V / 3V$ Refer to Off-leakage current	25°C	-0.05		±0.001	0.05
			-40°C to +85°C	-0.2		0.2	nA
			-40°C to +125°C	-0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 3.3V$ Switch Off $V_D = 3V / 1V$ $V_S = 1V / 3V$ Refer to Off-leakage current	25°C	-0.05		±0.001	0.05
			-40°C to +85°C	-0.2		0.2	nA
			-40°C to +125°C	-0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 3.3V$ Switch On $V_D = V_S = 3V / 1V$ Refer to On-leakage current	25°C	-0.1		±0.005	0.1
			-40°C to +85°C	-0.35		0.35	nA
			-40°C to +125°C	-2		2	nA

6.6 Electrical Characteristics ($V_{DD} = 3.3V \pm 10\%$) (続き)

at $T_A = 25^\circ C$, $V_{DD} = 3.3V$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
LOGIC INPUTS (SEL)						
V_{IH}	Input logic high		-40°C to +125°C	1.35	5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0	0.8	V
I_{IH} I_{IL}	Input leakage current		25°C	± 0.005		μA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C	± 0.05		μA
C_{IN}	Logic input capacitance		25°C	1		pF
C_{IN}	Logic input capacitance		-40°C to +125°C	2		pF
POWER SUPPLY						
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C	0.002		μA
			-40°C to +125°C	0.65		μA
DYNAMIC CHARACTERISTICS						
t_{TRAN}	Transition time from control input	$V_S = 2V$ $R_L = 200\Omega$, $C_L = 15pF$ Refer to Transition time	25°C	14		ns
			-40°C to +85°C	20		ns
			-40°C to +125°C	22		ns
Q_C	Charge Injection	$V_S = 1V$ $R_S = 0\Omega$, $C_L = 1nF$ Refer to Charge injection	25°C	-1.5		pC
O_{ISO}	Off Isolation	$R_L = 50\Omega$, $C_L = 5pF$ $f = 1MHz$ Refer to Off isolation	25°C	-62		dB
		$R_L = 50\Omega$, $C_L = 5pF$ $f = 10MHz$ Refer to Off isolation	25°C	-40		dB
BW	Bandwidth	$R_L = 50\Omega$, $C_L = 5pF$ Refer to Bandwidth	25°C	300		MHz
C_{SOFF}	Source off capacitance	$f = 1MHz$	25°C	6		pF
C_{DOFF}	Drain off capacitance	$f = 1MHz$	25°C	10		pF
C_{SON} C_{DON}	On capacitance	$f = 1MHz$	25°C	17		pF

(1) When V_S is 3V, V_D is 1V or when V_S is 1V, V_D is 3V.

6.7 Electrical Characteristics ($V_{DD} = 1.8V \pm 10\%$)

at $T_A = 25^\circ C$, $V_{DD} = 1.8V$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT	
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0V$ to V_{DD} $I_{SD} = 10mA$ Refer to On-resistance	25°C	40		Ω	
			-40°C to +85°C	80		Ω	
			-40°C to +125°C	80		Ω	
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 1.98V$ Switch Off $V_D = 1.62V$ / 1V $V_S = 1V$ / 1.62V Refer to Off-leakage current	25°C	-0.05	± 0.001	nA	
			-40°C to +85°C	-0.2	0.2		nA
			-40°C to +125°C	-0.9	0.9		nA

6.7 Electrical Characteristics ($V_{DD} = 1.8V \pm 10\%$) (続き)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 1.98\text{V}$ Switch Off $V_D = 1.62\text{V} / 1\text{V}$ $V_S = 1\text{V} / 1.62\text{V}$ Refer to Off-leakage current	25°C	-0.05	± 0.001	0.05	nA
			-40°C to +85°C	-0.2		0.2	nA
			-40°C to +125°C	-0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 1.98\text{V}$ Switch On $V_D = V_S = 1.62\text{V} / 1\text{V}$ Refer to On-leakage current	25°C	-0.1	± 0.005	0.1	nA
			-40°C to +85°C	-0.35		0.35	nA
			-40°C to +125°C	-2		2	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		-40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		± 0.005		μA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C			± 0.05	μA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		μA
			-40°C to +125°C			0.45	μA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 1\text{V}$ $R_L = 200\Omega$, $C_L = 15\text{pF}$ Refer to Transition time	25°C		25		ns
			-40°C to +85°C			44	ns
			-40°C to +125°C			44	ns
Q_C	Charge Injection	$V_S = 1\text{V}$ $R_S = 0\Omega$, $C_L = 1\text{nF}$ Refer to Charge injection	25°C		-1.5		pC
O_{ISO}	Off Isolation	$R_L = 50\Omega$, $C_L = 5\text{pF}$ $f = 1\text{MHz}$ Refer to Off isolation	25°C		-62		dB
		$R_L = 50\Omega$, $C_L = 5\text{pF}$ $f = 10\text{MHz}$ Refer to Off isolation	25°C		-40		dB
BW	Bandwidth	$R_L = 50\Omega$, $C_L = 5\text{pF}$ Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	$f = 1\text{MHz}$	25°C		6		pF
C_{DOFF}	Drain off capacitance	$f = 1\text{MHz}$	25°C		10		pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{MHz}$	25°C		17		pF

(1) When V_S is 1.62V, V_D is 1V or when V_S is 1V, V_D is 1.62V.

6.8 Electrical Characteristics ($V_{DD} = 1.2V \pm 10\%$)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0\text{V to } V_{DD}$ $I_{SD} = 10\text{mA}$ Refer to On-resistance	25°C		70		Ω
			-40°C to +85°C			105	Ω
			-40°C to +125°C			105	Ω

6.8 Electrical Characteristics ($V_{DD} = 1.2V \pm 10\%$) (続き)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 1.32V$ Switch Off $V_D = 1V / 0.8V$ $V_S = 0.8V / 1V$ Refer to Off-leakage current	25°C	-0.05	± 0.001	0.05	nA
			-40°C to +85°C	-0.2		0.2	nA
			-40°C to +125°C	-0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 1.32V$ Switch Off $V_D = 1V / 0.8V$ $V_S = 0.8V / 1V$ Refer to Off-leakage current	25°C	-0.05	± 0.001	0.05	nA
			-40°C to +85°C	-0.2		0.2	nA
			-40°C to +125°C	-0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 1.32V$ Switch On $V_D = V_S = 1V / 0.8V$ Refer to On-leakage current	25°C	-0.1	± 0.005	0.1	nA
			-40°C to +85°C	-0.35		0.35	nA
			-40°C to +125°C	-2		2	nA
LOGIC INPUTS (SEL)							
V_{IH}	Input logic high		-40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		± 0.005		μA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C			± 0.05	μA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		μA
			-40°C to +125°C			0.38	μA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 1V$ $R_L = 200\Omega$, $C_L = 15pF$ Refer to Transition time	25°C		55		ns
			-40°C to +85°C			190	ns
			-40°C to +125°C			190	ns
Q_C	Charge Injection	$V_S = 1V$ $R_S = 0\Omega$, $C_L = 1nF$ Refer to Charge injection	25°C		-1.5		pC
O_{ISO}	Off Isolation	$R_L = 50\Omega$, $C_L = 5pF$ $f = 1MHz$ Refer to Off isolation	25°C		-62		dB
		$R_L = 50\Omega$, $C_L = 5pF$ $f = 10MHz$ Refer to Off isolation	25°C		-42		dB
BW	Bandwidth	$R_L = 50\Omega$, $C_L = 5pF$ Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	$f = 1MHz$	25°C		6		pF
C_{DOFF}	Drain off capacitance	$f = 1MHz$	25°C		10		pF
C_{SON} C_{DON}	On capacitance	$f = 1MHz$	25°C		17		pF

(1) When V_S is 1V, V_D is 0.8V or when V_S is 0.8V, V_D is 1V.

6.9 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted).

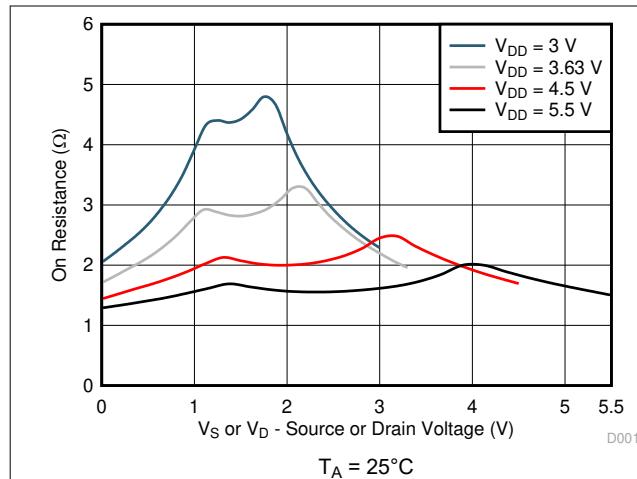


図 6-1. On-Resistance vs Source or Drain Voltage

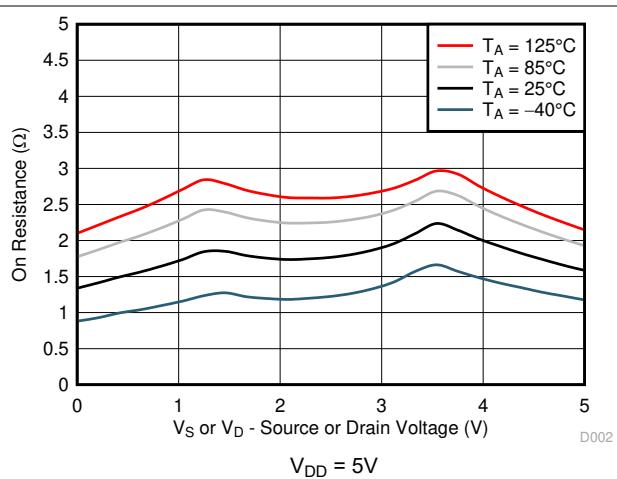


図 6-2. On-Resistance vs Temperature

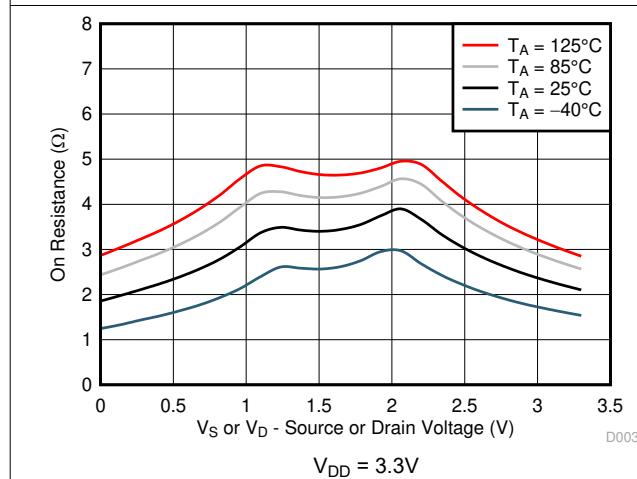


図 6-3. On-Resistance vs Temperature

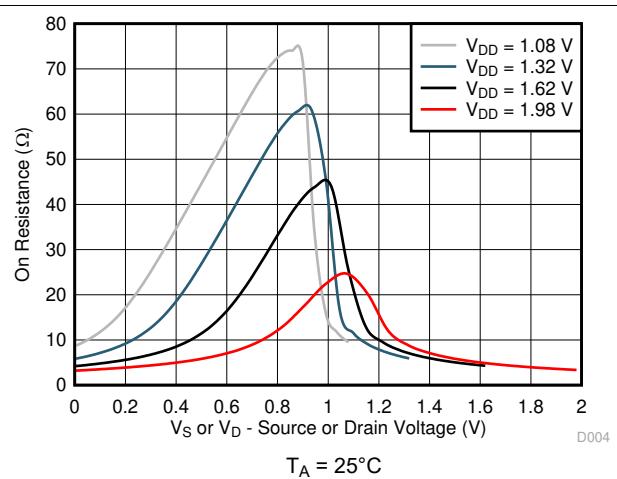


図 6-4. On-Resistance vs Source or Drain Voltage

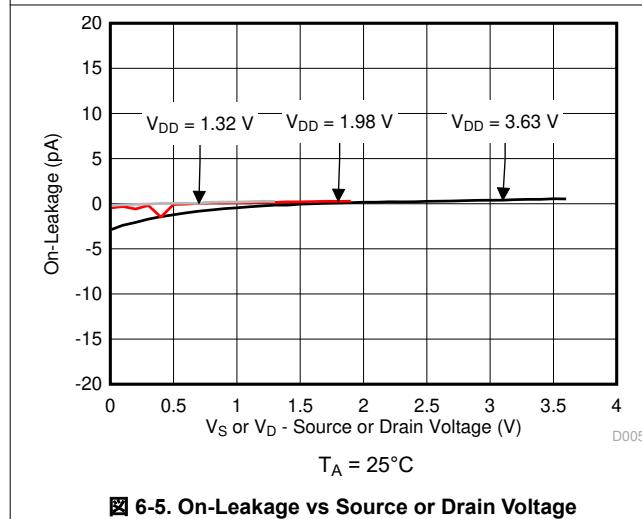


図 6-5. On-Leakage vs Source or Drain Voltage

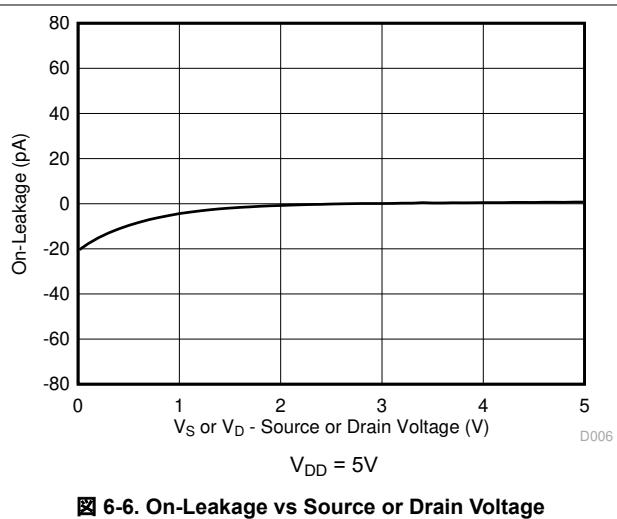


図 6-6. On-Leakage vs Source or Drain Voltage

6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted).

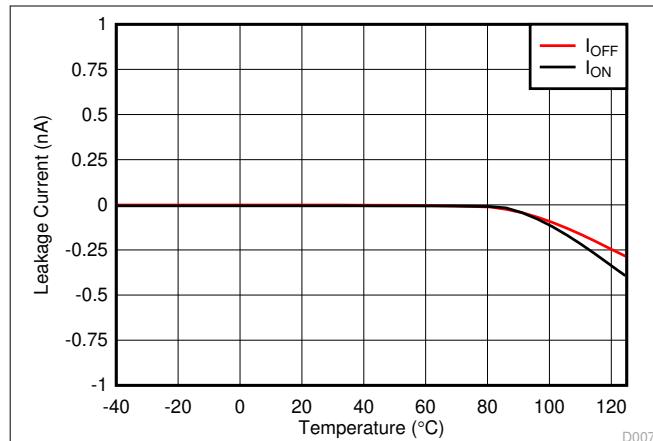


図 6-7. Leakage Current vs Temperature

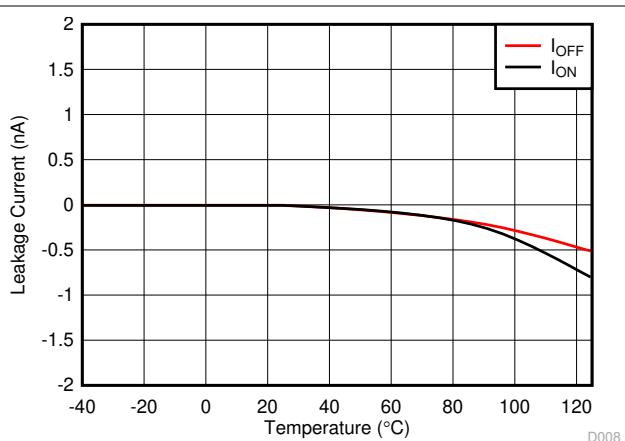


図 6-8. Leakage Current vs Temperature

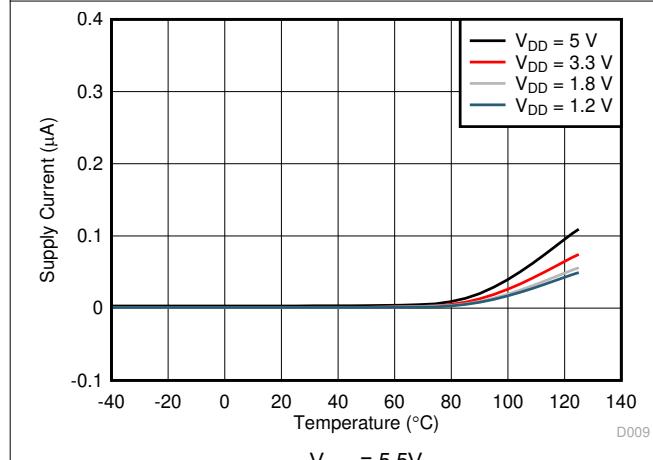


図 6-9. Supply Current vs Temperature

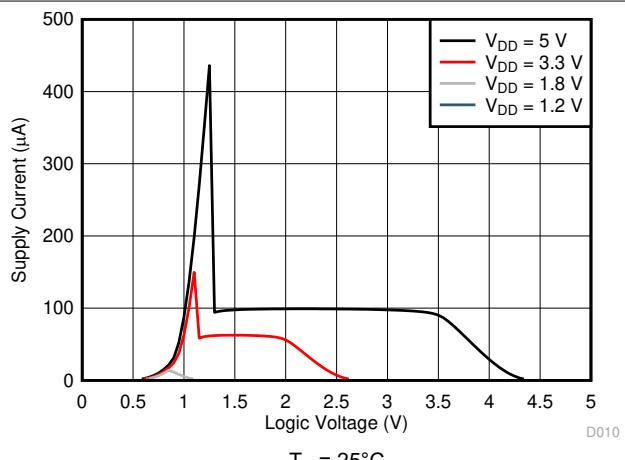


図 6-10. Supply Current vs Logic Voltage

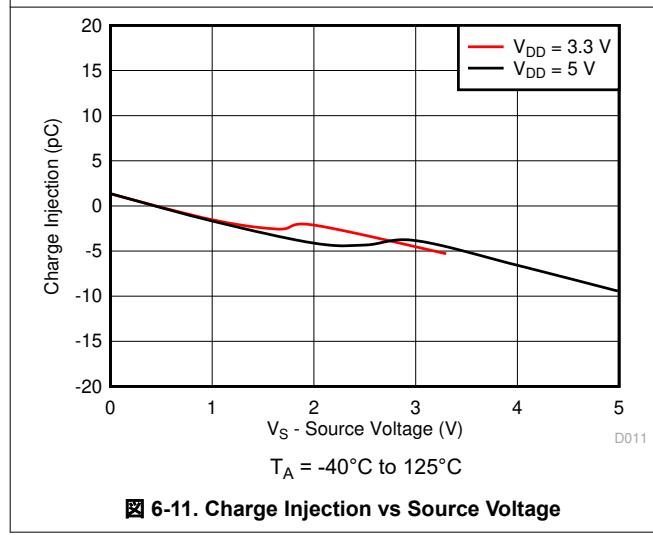


図 6-11. Charge Injection vs Source Voltage

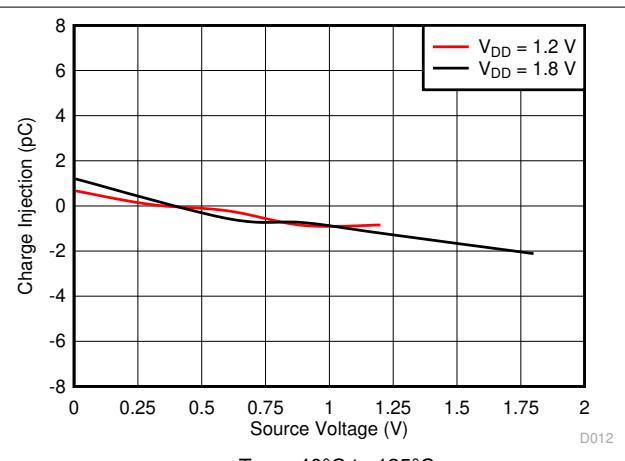
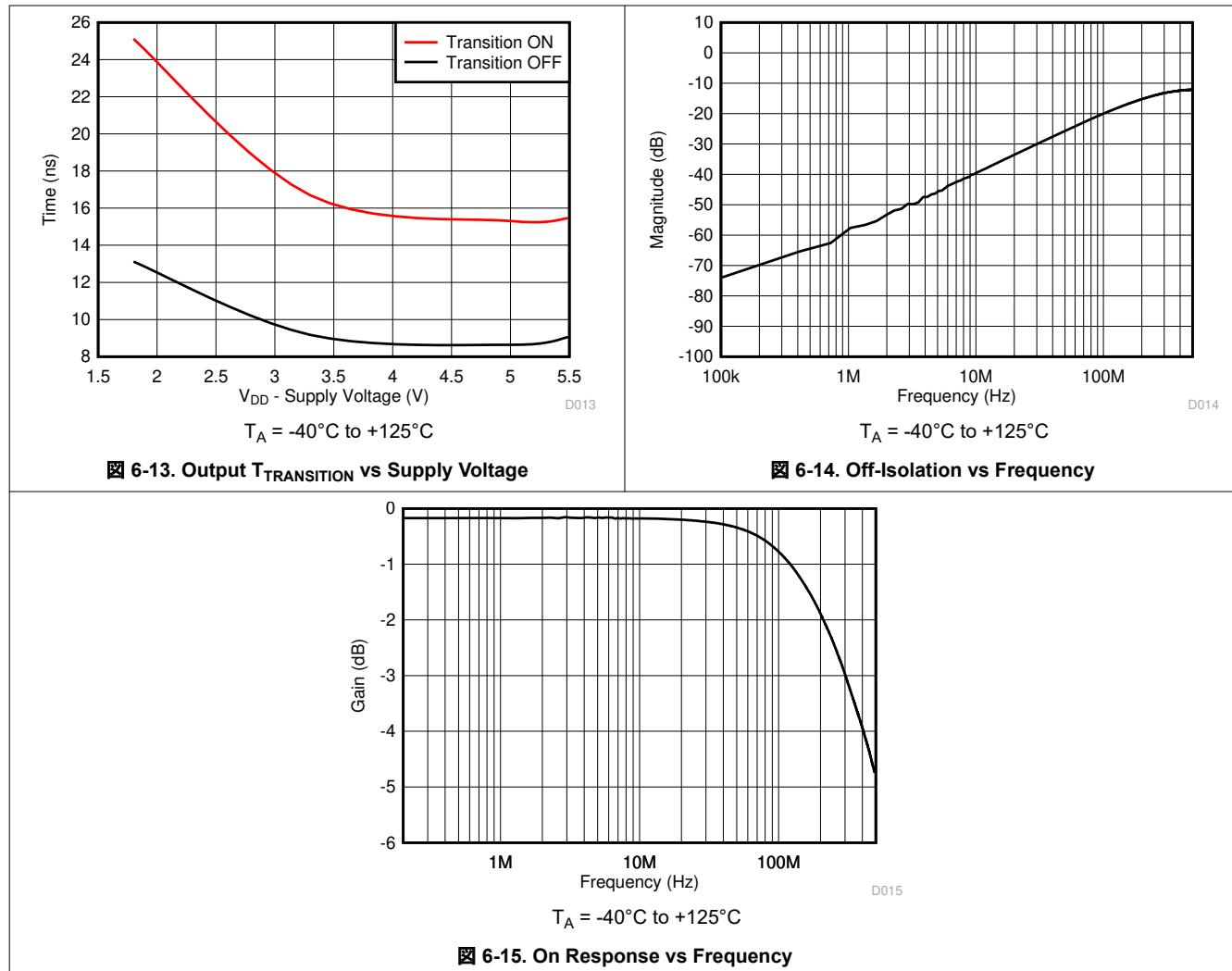


図 6-12. Charge Injection vs Source Voltage

6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted).



7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (S) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in [図 7-1](#). Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

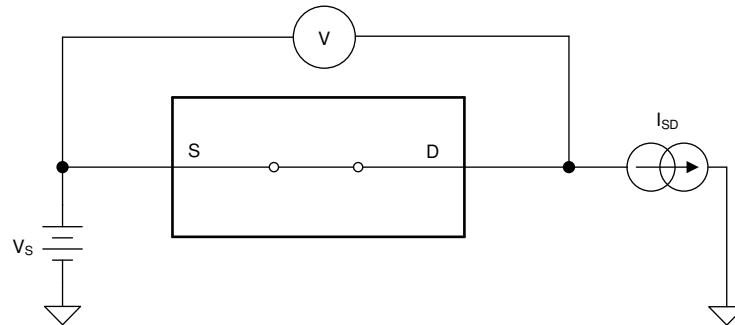


図 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in [図 7-2](#).

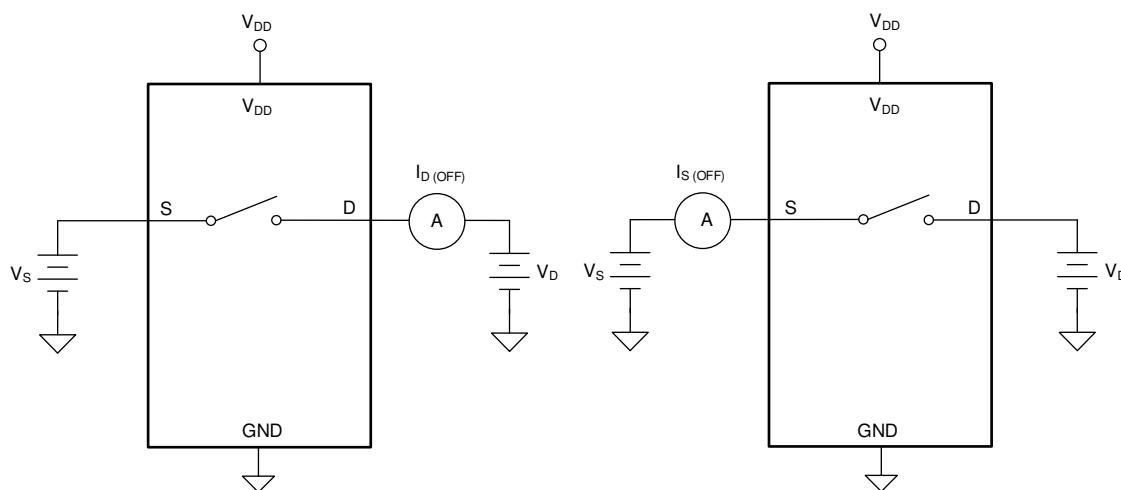


図 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. [図 7-3](#) shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

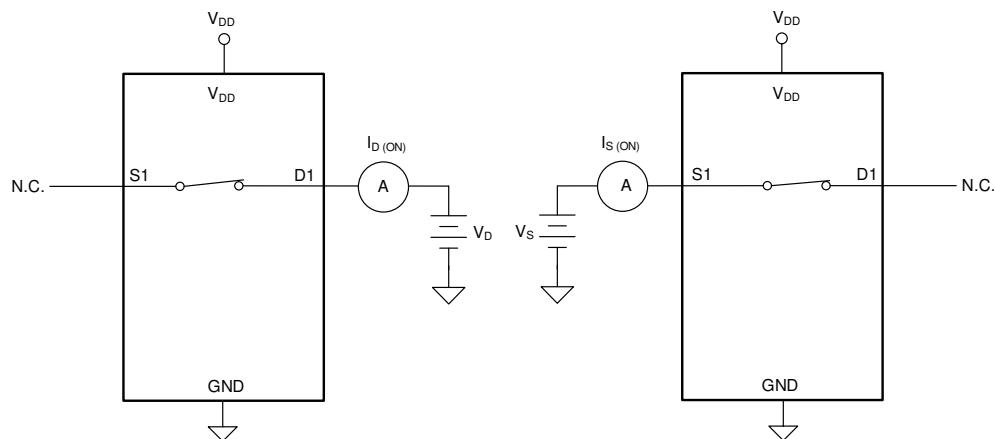


図 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. [図 7-4](#) shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

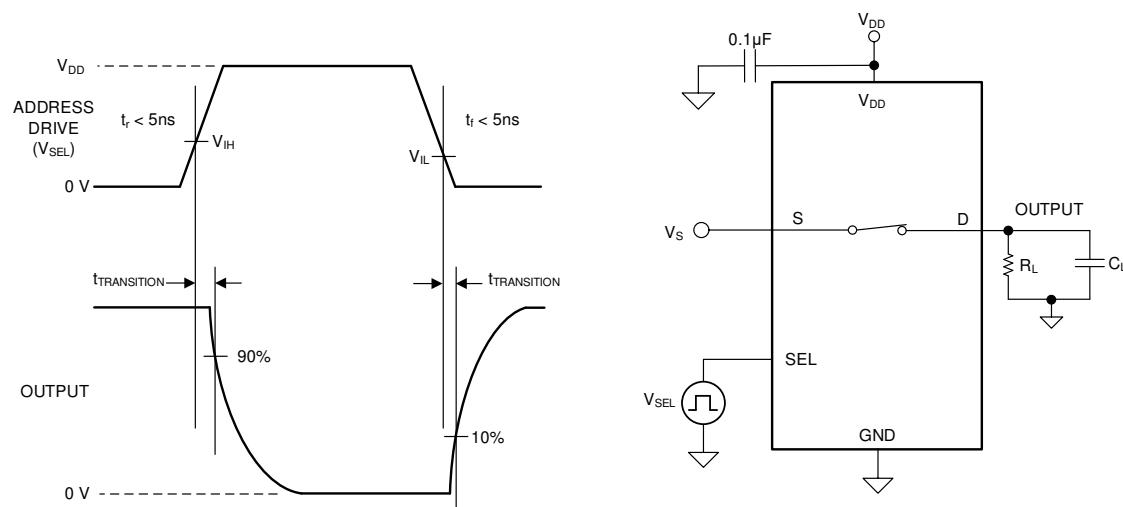


図 7-4. Transition-Time Measurement Setup

7.5 Charge Injection

The TMUX110x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C . [図 7-5](#) shows the setup used to measure charge injection from source (S) to drain (D).

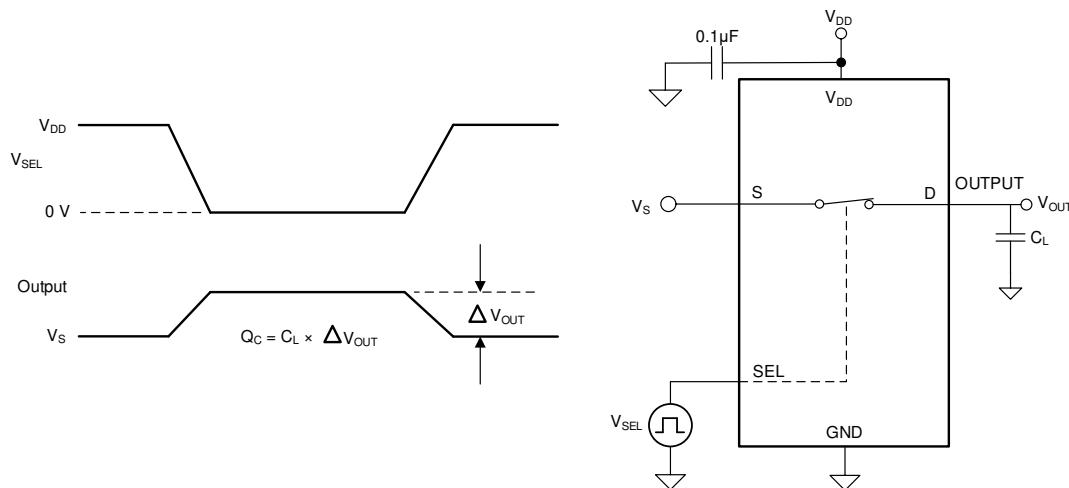


図 7-5. Charge-Injection Measurement Setup

7.6 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (S) of an off-channel. The characteristic impedance, Z_0 , for the measurement is 50Ω . [図 7-6](#) shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

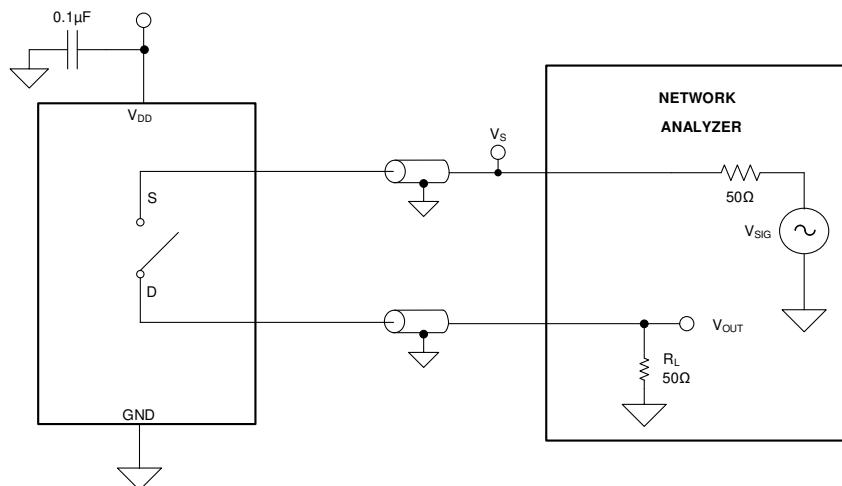


図 7-6. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \log\left(\frac{V_{\text{OUT}}}{V_S}\right) \quad (1)$$

7.7 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (S) of an on-channel, and the output is measured at the drain pin (D) of the device. The characteristic impedance, Z_0 , for the measurement is 50Ω . [图 7-7](#) shows the setup used to measure bandwidth.

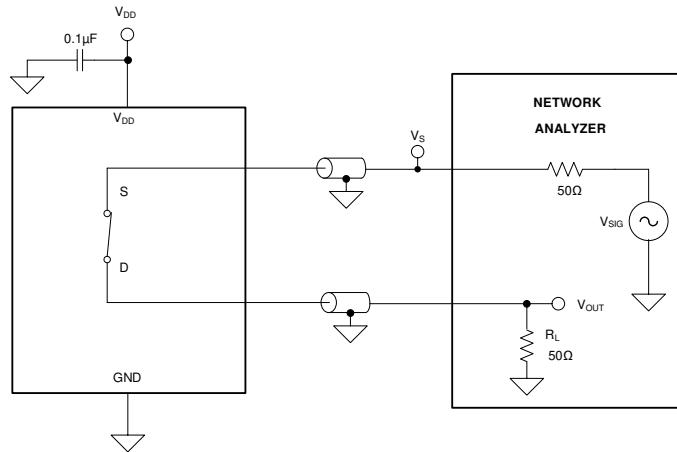


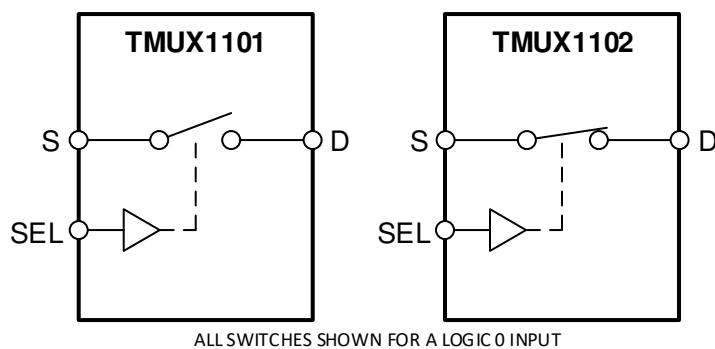
图 7-7. Bandwidth Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX1101 and TMUX1102 are 1:1 (SPST) switches. The TMUX110x devices have a controllable single-pole, single-throw switch that is turned on or off based on the state of the select pin. The switch of the TMUX1101 is turned on with a Logic 1 on the select pin, while a Logic 0 is required to turn on switch in the TMUX1102. The following figure shows the functional block diagram for the TMUX110x devices.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX110x conducts equally well from source (S) to drain (D) or from drain (D) to source (S). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input/output voltage for TMUX110x ranges from GND to V_{DD} .

8.3.3 1.8V Logic Compatible Inputs

The TMUX110x devices have 1.8V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allows the TMUX110x devices to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. The current consumption of the TMUX110x devices increase when using 1.8V logic with higher supply voltage as shown in [図 6-10](#). For more information on 1.8V logic implementations refer to [Simplifying Design with 1.8V logic Muxes and Switches](#).

8.3.4 Fail-Safe Logic

The TMUX110x supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pin. For example, the Fail-Safe Logic feature allows the select pin of the TMUX110x devices to be ramped to 5.5V while $V_{DD} = 0V$. Additionally, the feature enables operation of the TMUX110x with $V_{DD} = 1.2V$ while allowing the select pin to interface with a logic level of another device up to 5.5V.

8.3.5 Ultra-Low Leakage Current

The TMUX110x devices provide extremely low on-leakage and off-leakage currents. The TMUX110x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. [図 8-1](#) shows typical leakage currents of the TMUX110x devices versus temperature at $V_{DD} = 5V$.

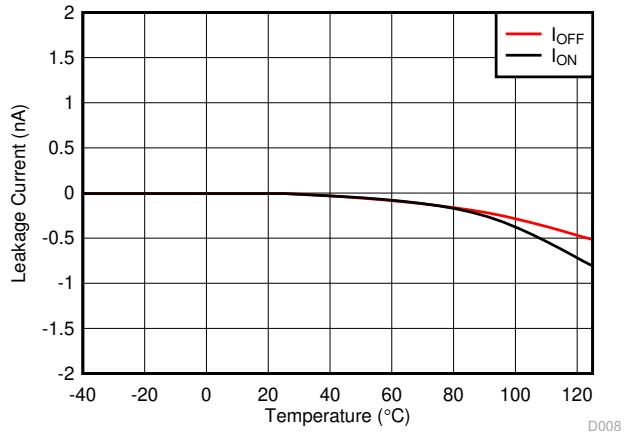


図 8-1. Leakage Current vs Temperature

8.3.6 Ultra-Low Charge Injection

The TMUX110x devices have a transmission gate topology, as shown in [図 8-2](#). Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

The TMUX110x devices have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to $-1.5pC$ at $V_S = 1V$ as shown in [図 8-3](#).

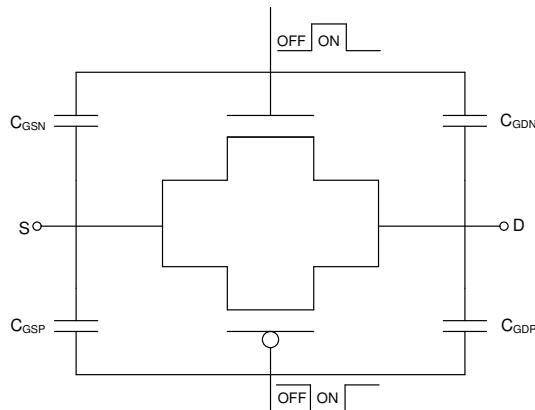


図 8-2. Transmission Gate Topology

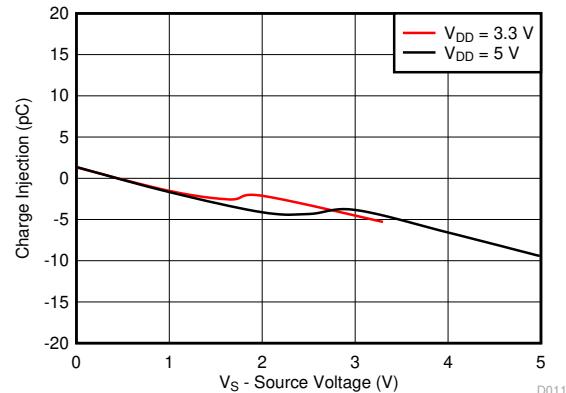


図 8-3. Charge Injection vs Source Voltage

8.4 Device Functional Modes

The TMUX110x devices have a controllable single-pole, single-throw switch that is turned on or turned off based on the state of the corresponding select pin. The control pin can be as high as 5.5V.

The TMUX110x devices can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connection to GND.

8.4.1 Truth Tables

表 8-1 和 表 8-2 列出了 TMUX1101 和 TMUX1102 的真值表。

表 8-1. TMUX1101 Truth Table

SEL	SWITCH STATE
0	OFF (HI-Z)
1	ON

表 8-2. TMUX1102 Truth Table

SEL	SWITCH STATE
0	ON
1	OFF (HI-Z)

9 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インストルメンツの製品仕様に含まれるものではなく、テキサス・インストルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TMUX11xx family offers ultra-low input and output leakage currents and low charge injection. These devices operate up to 5.5V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX110x have a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

9.2 Typical Application - Sample-and-Hold Circuit

One useful application to take advantage of the TMUX1101 and TMUX1102's performance is the sample-and-hold circuit. A sample-and-hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample-and-hold circuit can be realized using an analog switch such as the TMUX1101, and TMUX1102 analog switches. [図 9-1](#) shows a single channel sample-and hold circuit using either of the TMUX110x devices.

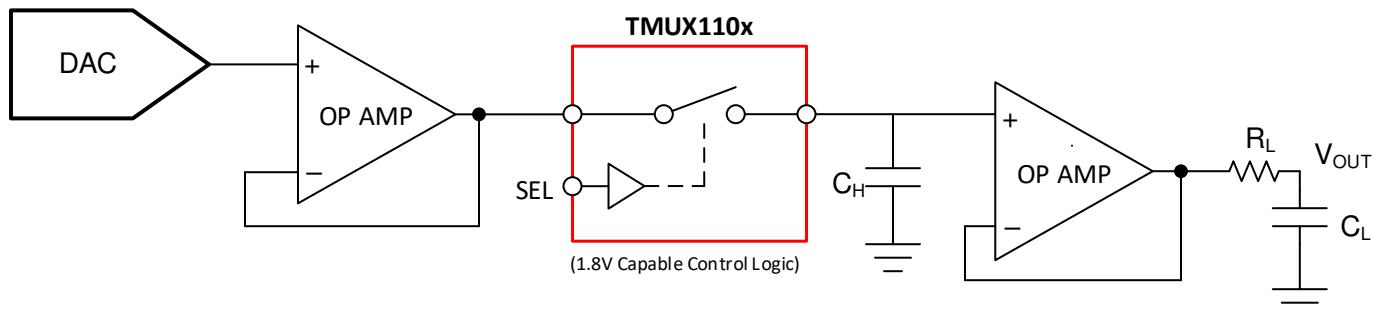


図 9-1. Single Channel Sample-and-Hold Circuit Example

An optional op amp is used before the switch since driving large capacitive loads is a typical limitation of buffered DACs. The additional buffer stage is included following the DAC to prevent potential stability problems from driving a large capacitive load.

Generally, the switch delivers only the input signals to the holding capacitors. However, when the switch is toggled, some amount of charge is transferred to the switch output in the form of charge injection, resulting in a pedestal sampling error. The TMUX1101 and TMUX1102 switches have excellent charge injection performance of only -1.5pC, making them excellent choices for this implementation to minimize sampling error. The pedestal error voltage is indirectly related to the size of the capacitance on the output, for better precision a larger capacitor is required due to charge injection.

9.2.1 Design Requirements

The purpose of this precision design is to implement an optimized single channel sample-and-hold circuit using a precision 1:1 (SPST) CMOS switch. The sample-and-hold circuit needs to be capable of supporting high accuracy with minimized pedestal error and fast settling time.

9.2.2 Detailed Design Procedure

The TMUX1101 or TMUX1102 switch is used in conjunction with the voltage holding capacitors (C_H) to implement the sample-and-hold circuit. The basic operation is:

1. When the switch is closed, it samples the input voltage and charges the holding capacitors (C_H) to the input voltage values.
2. When the switch is open, the holding capacitors (C_H) holds its previous value, maintaining stable voltage at the amplifier output (V_{OUT}).

Due to switch and capacitor leakage current, as well as amplifier bias current, the voltage on the hold capacitors droops with time. The TMUX1101 and TMUX1102 minimize the droops due to its ultra-low leakage performance. At 25°C, the TMUX1101 and TMUX1102 have extremely low leakage current of 3pA typical.

Refer to [Sample and Hold Glitch Reduction for Precision Outputs Reference Design](#) for more information on sample-and-hold circuits.

9.2.3 Application Curve

TMUX1101 and TMUX1102 have excellent charge injection performance and ultra-low leakage current, making them excellent choices to minimize sampling error for the sample-and-hold application. The charge injection and leakage performance are shown in [図 9-2](#) and [図 9-3](#) respectively.

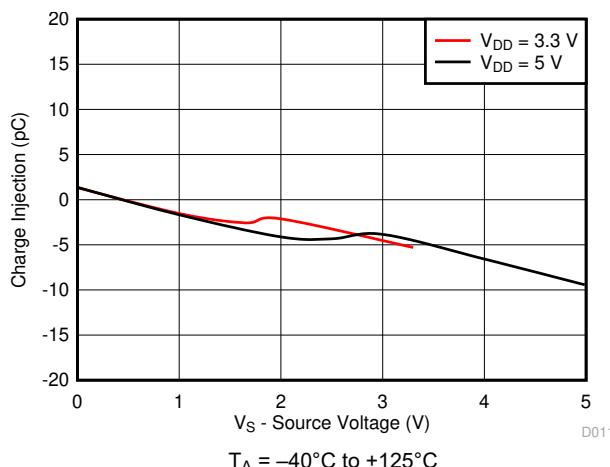


図 9-2. Charge Injection vs Source Voltage

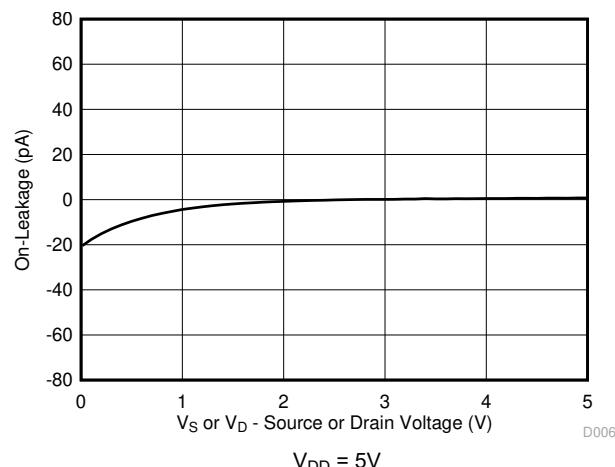
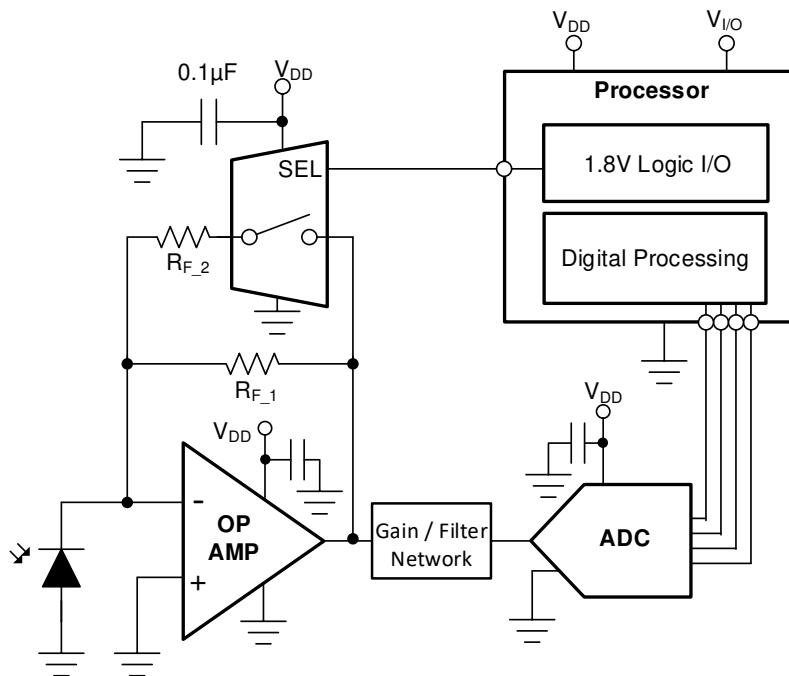


図 9-3. On-Leakage vs Source or Drain Voltage

9.3 Typical Application - Switched Gain Amplifier

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on the switch path, the TMUX110x allows the system to have multiple gain settings. An external resistor ensures the amplifier is not operating in an open loop configuration. A transimpedance amplifier (TIA) for photodiode inputs is a common circuit that requires gain control using a switch to convert the output current of the photodiode into a voltage for the MCU or processor. The amount of light present during a photodiode measurement is dependent on the time of day and available light source. An external switch such as the TMUX110x can be utilized to increase the gain when a smaller photodiode current is present. The leakage current, capacitance, and charge injection performance of the TMUX110x are key specifications to evaluate when selecting a device for gain control. An example switched gain amplifier circuit is shown in [図 9-4](#).



[図 9-4. Configurable Gain Setting of a TIA Circuit](#)

9.3.1 Design Requirements

For this design example, use the parameters listed in [表 9-1](#).

表 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3V
Input / Output signal range	0μA to 10μA
Control logic thresholds	1.8V compatible

9.3.2 Detailed Design Procedure

The TMUX110x devices can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommended operating conditions of the TMUX110x, including signal range and continuous current. For this design example, with a supply of 3.3V, the signals can range from 0V to 3.3V when the device is powered. The maximum continuous current can be 30mA.

Photodiodes commonly have a current output that ranges from a few hundred picoamps to tens of microamps based on the amount of light being absorbed. The TMUX110x devices have a typical On-leakage current of less than 10pA, which would lead to an accuracy well within 1% of a full scale 10 μ A signal. The low ON and OFF capacitance of the TMUX110x improves system stability by minimizing the total capacitance on the output of the amplifier. Lower capacitance leads to less overshoot and ringing in the system, which can cause the amplifier circuit to become unstable if the phase margin is not at least 45°. Refer to [Improve Stability Issues with Low \$C_{\text{ON}}\$ Multiplexers](#) for more information on calculating the phase margin versus percent overshoot.

9.3.3 Application Curve

The TMUX110x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents.

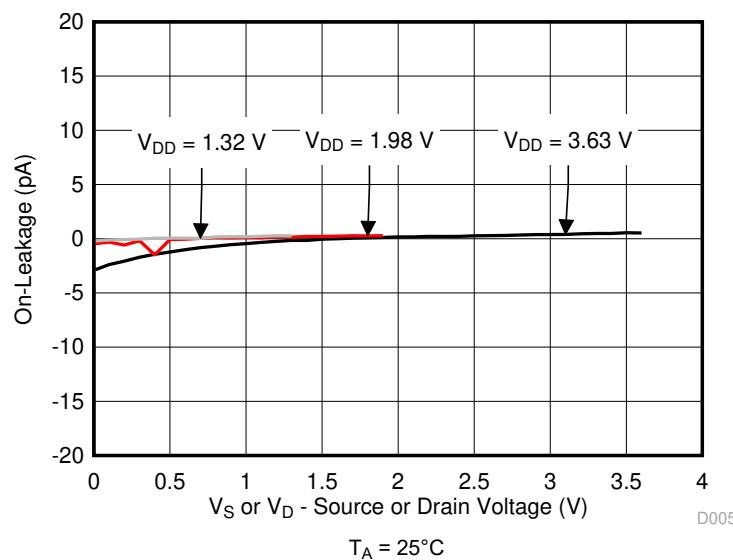


图 9-5. On-Leakage vs Source or Drain Voltage

9.4 Power Supply Recommendations

The TMUX110x devices operate across a wide supply range of 1.08V to 5.5V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from $0.1\mu F$ to $10\mu F$ from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

9.5 Layout

9.5.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. **图 9-6** shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

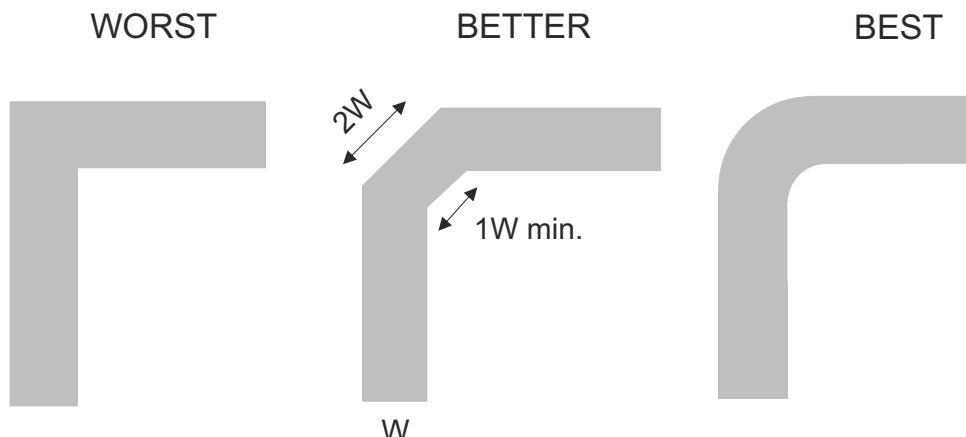


图 9-6. Trace example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

図 9-7 shows an example of a PCB layout with the TMUX110x. Some key considerations are as follows:

- Decouple the V_{DD} pin with a $0.1\mu F$ capacitor, placed as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.5.2 Layout Example

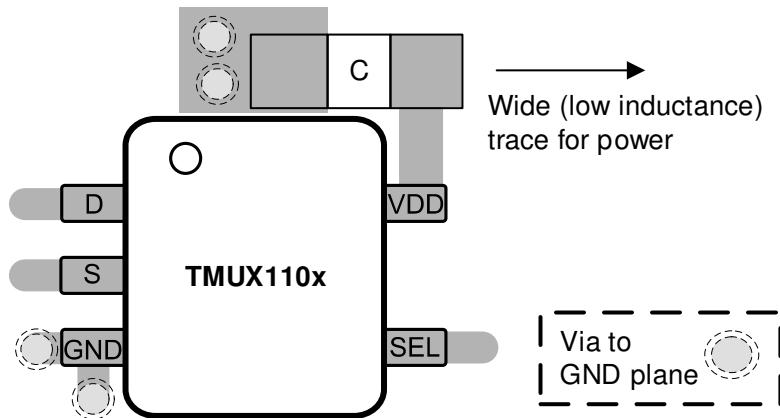


図 9-7. TMUX110x Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Sample and Hold Glitch Reduction for Precision Outputs Reference Design](#).
- Texas Instruments, [True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit](#).
- Texas Instruments, [Improve Stability Issues with Low CON Multiplexers](#).
- Texas Instruments, [Simplifying Design with 1.8V logic Muxes and Switches](#).
- Texas Instruments, [Eliminate Power Sequencing with Powered-off Protection Signal Switches](#).
- Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers](#).

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.4 Trademarks

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10.6 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (November 2019) to Revision D (February 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated I_s or I_d (Continuous Current) values.....	4
• Added I_{peak} values to Recommended Operating Conditions table.....	4

Changes from Revision B (August 2019) to Revision C (November 2019)	Page
• 「アプリケーション」セクションにリンクを追加.....	1

- TMUX1101 および TMUX1102 DBV パッケージ RTM の設定を追加。 1

Changes from Revision A (March 2019) to Revision B (August 2019)	Page
• 「製品情報」表から製品プレビューの注を削除	1
• Deleted the <i>Product Preview</i> note from the <i>Device Comparison</i> table.....	2
• Added DBV (SOT-23) thermal values to <i>Thermal Information</i>	5

Changes from Revision * (March 2019) to Revision A (July 2019)	Page
• ドキュメントのステータスを「事前情報」から「混合ステータス」に変更。	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1101DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1W1F
TMUX1101DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1W1F
TMUX1101DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1W1F
TMUX1101DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1W1F
TMUX1101DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	101
TMUX1101DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	101
TMUX1101DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	101
TMUX1101DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	101
TMUX1102DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1W3F
TMUX1102DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1W3F
TMUX1102DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	102
TMUX1102DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	102

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

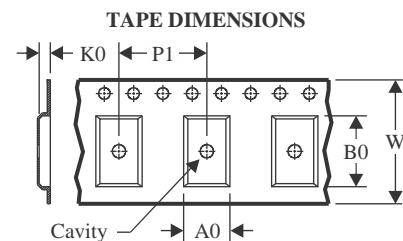
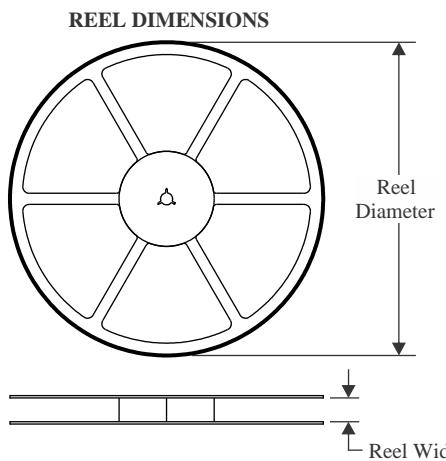
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

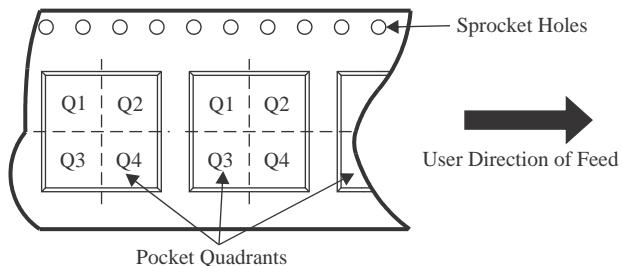
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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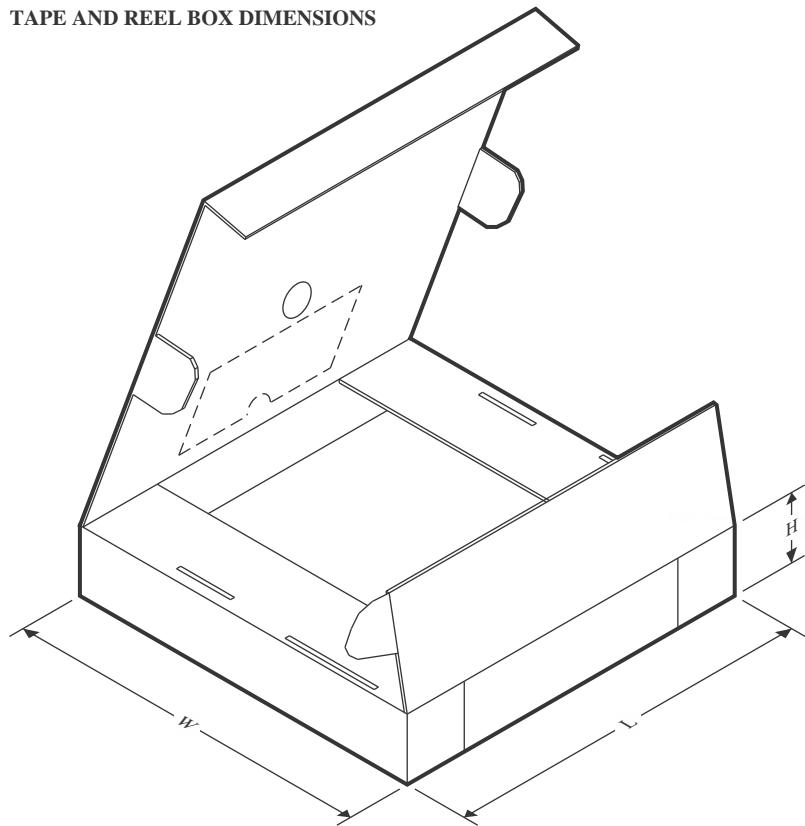
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1101DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMUX1101DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMUX1101DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TMUX1101DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1102DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMUX1102DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1101DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TMUX1101DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TMUX1101DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TMUX1101DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
TMUX1102DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TMUX1102DCKR	SC70	DCK	5	3000	210.0	185.0	35.0

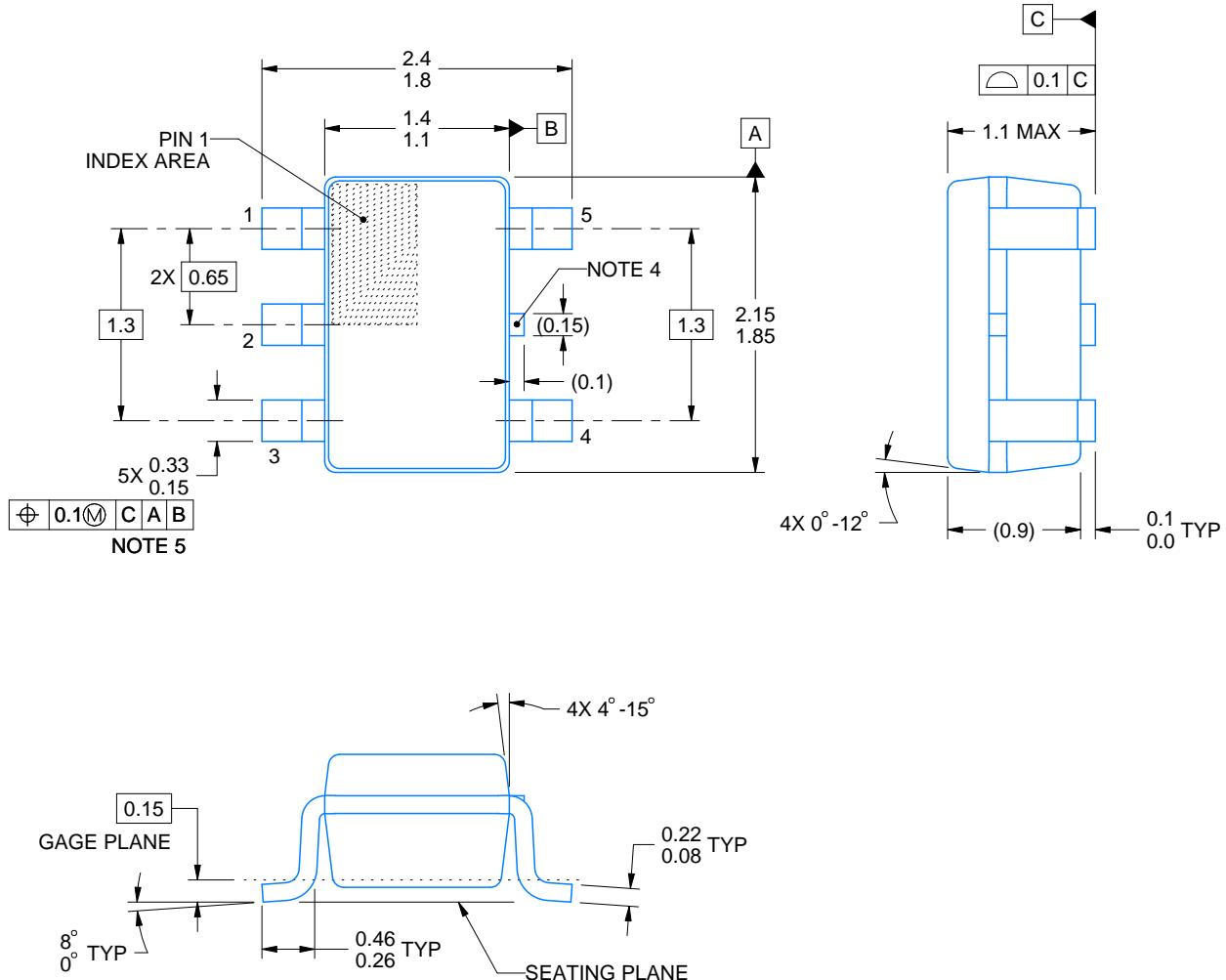
PACKAGE OUTLINE

DCK0005A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

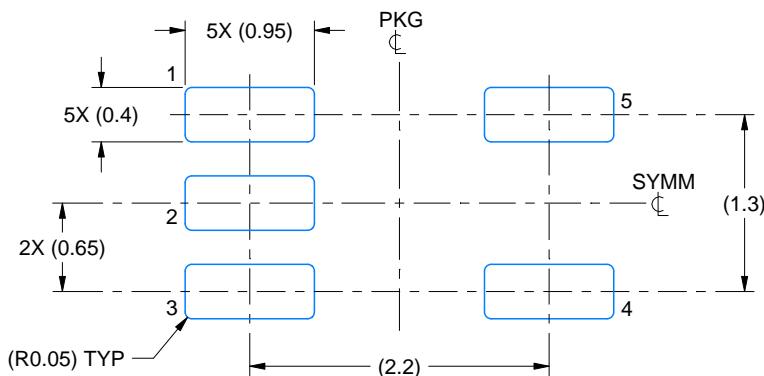
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

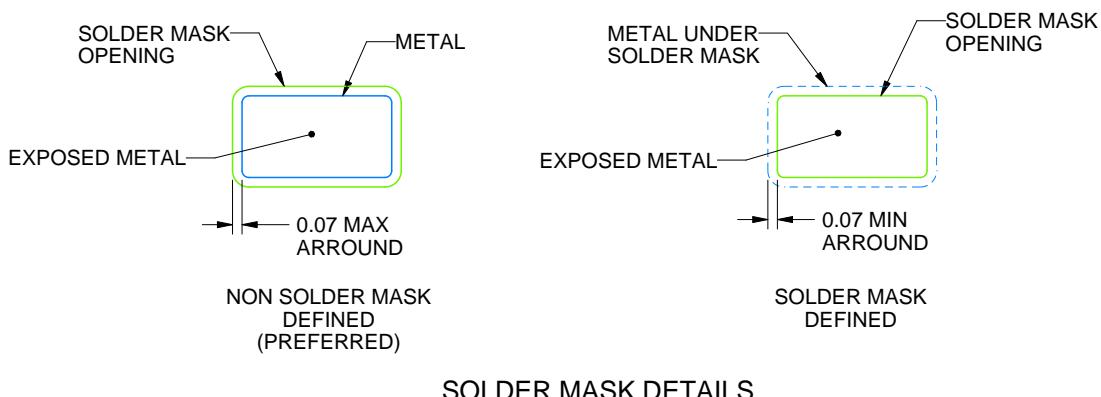
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

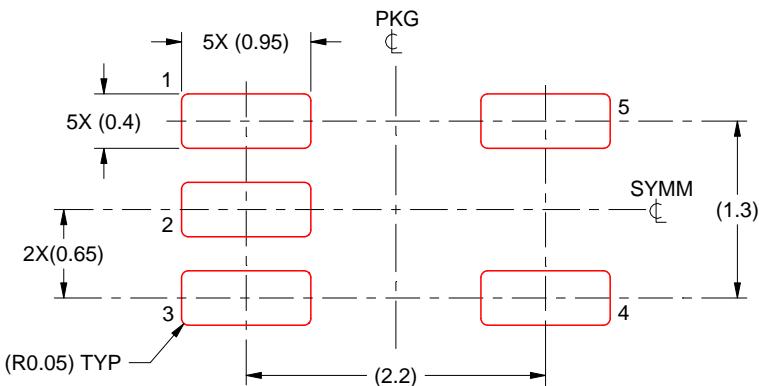
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

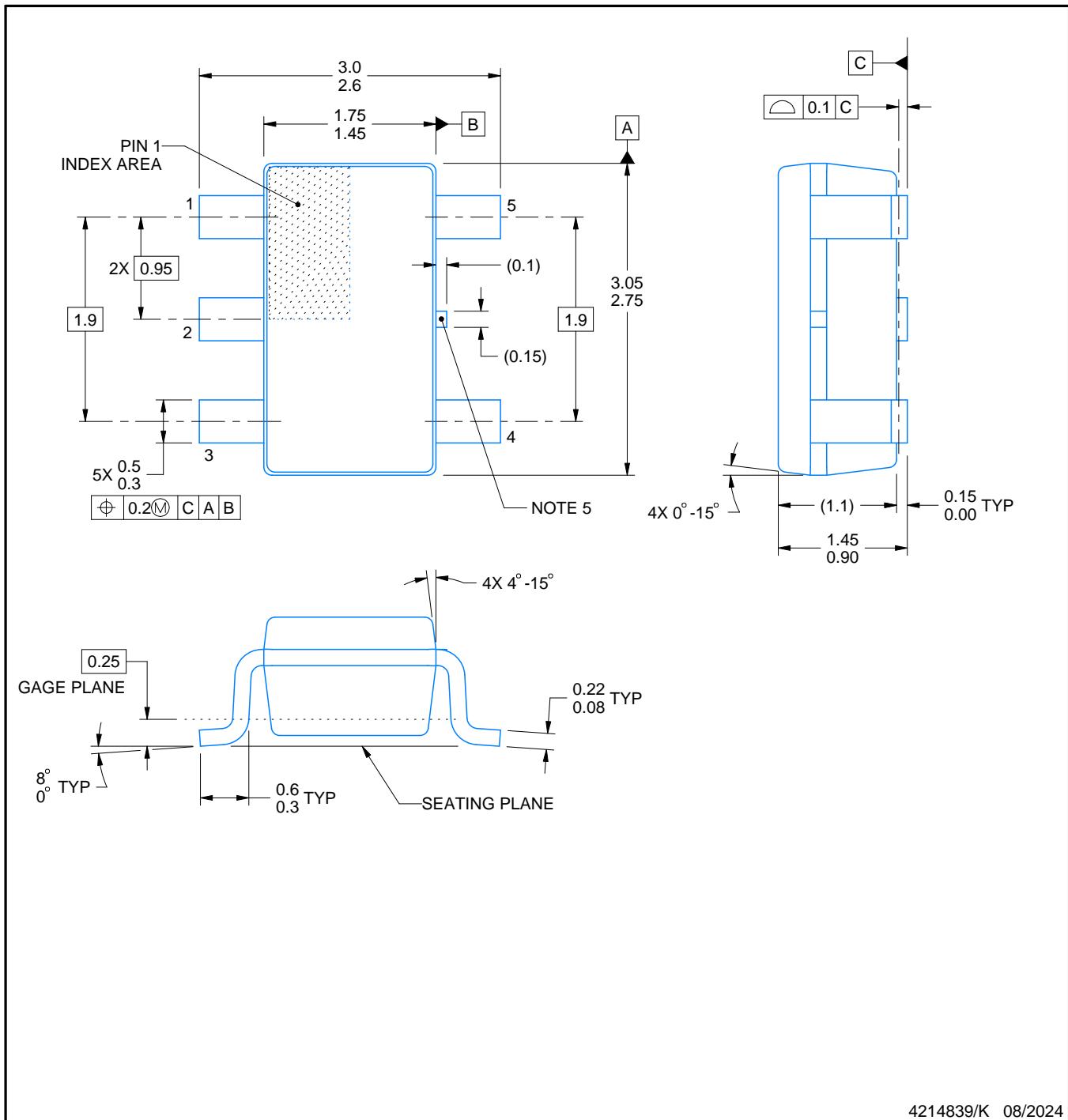
PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

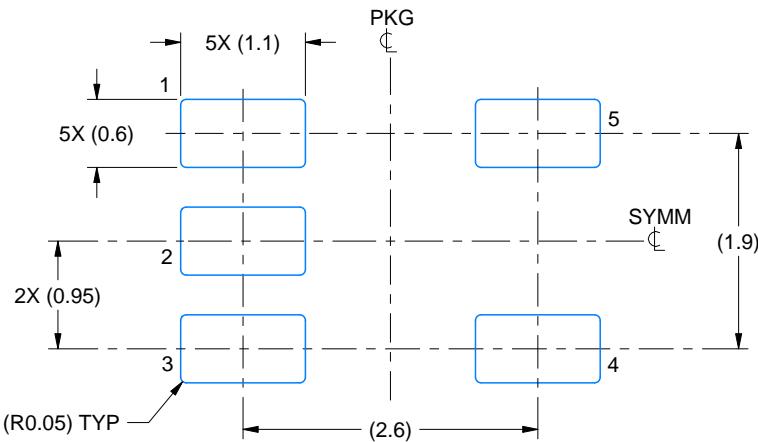
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

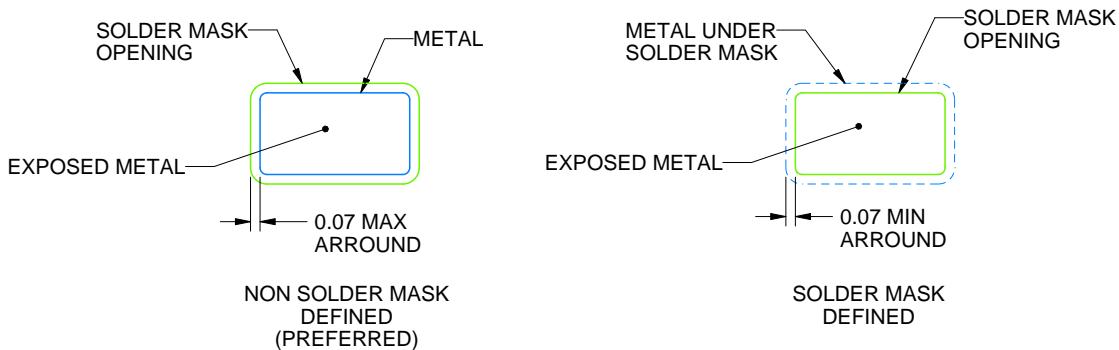
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

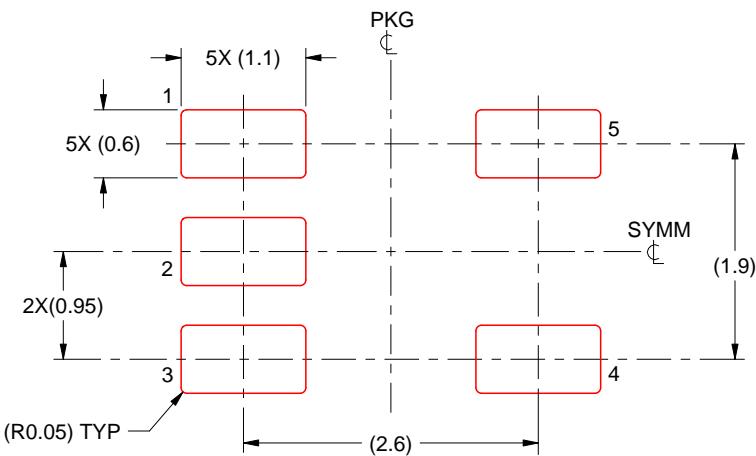
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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