TMUX6104 36V、低容量、低リーク電流、高精度の4:1アナログ・マルチプレクサ

1 特長

- 低いオン容量: 5pF
- 低入力リーク電流: 5pA
- 低電荷注入: 0.35pC
- レール・ツー・レール動作
- 広い電源電圧範囲: ±5V～±16.5V (デュアル電源)、または10V～16.5V (シングル電源)
- 低オン抵抗: 125Ω
- 遷移時間: 88ns
- Break-Before-Makeの切り替え動作
- V_{DD}に接続可能なENピン 、プルダウン内蔵
- ロジック・レベル: 2V～V_{DD}
- 低い消費電流: 17µA
- ESD保護(HBM): 2000V
- 業界標準のTSSOPパッケージ

2 アプリケーション

- ファクトリ・オートメーションと産業プロセス制御
- プログラマブル・ロジック・コントローラ（PLC）
- アナログ入力モジュール
- ATE試験装置
- デジタル・マルチメータ
- バッテリ・モニタリング・システム

3 概要

TMUX6104は新型の相補型金属酸化膜半導体(CMOS)アナログ・マルチプレクサ(MUX)で、4:1のシングルエンド多重化を行います。これらのデバイスはデュアル電源(±5V～±16.5V)、シングル電源(10V～16.5V)、または非対称電源(V_{DD} = 12V、V_{SS} = -5Vなど)で適切に動作します。すべてのデジタル入力はスレッショルドがTTL (Transistor-Transistor Logic)互換で、TTLおよびCMOS両方のロジックとの互換性が保証されています。

TMUX6104は、アドレス・ピン(A0/A1)とイネーブル・ピン(EN)のステータスに従い、4つの入力の1つ(Sx)を共通の出力(D)に多重化します。各スイッチはオン位置において、どちらの方向にも同程度に伝導性が高く、電源電圧までの入力信号範囲をサポートします。オフ状態では、電源電圧までの信号レベルがブロックされます。すべてのスイッチは、Break-Before-Make (BBM)スイッチング動作を行います。

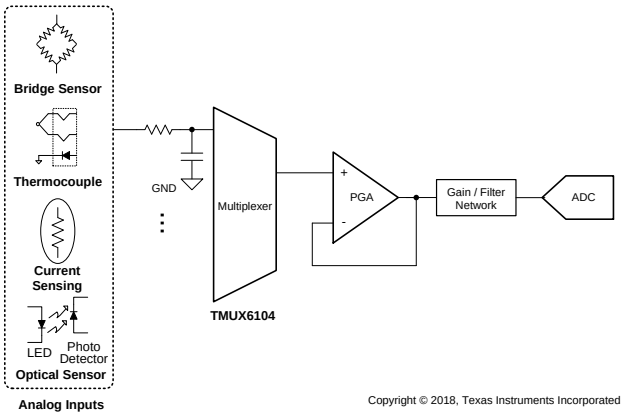
TMUX6104デバイスは、テキサス・インスツルメンツの高精度スイッチおよびマルチプレクサ・ファミリの製品です。このファミリのデバイスはリーク電流と電荷注入が非常に小さいため、高精度の測定アプリケーションに使用可能です。消費電流が17µAと低いため、携帯型アプリケーションにも使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TMUX6104	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年2月発行のものから更新 **Page**

- デバイスのステータスを「*事前情報*」から「*量産データ*」に変更 ... 1

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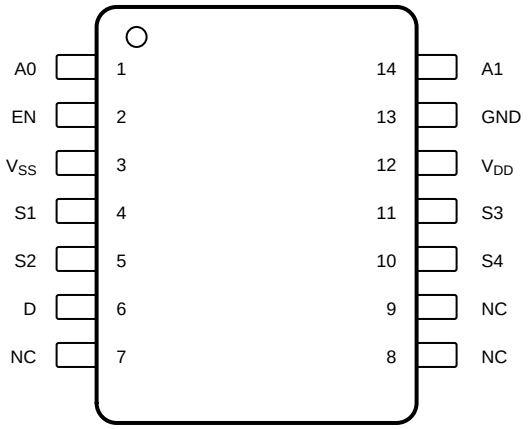
5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	I	Address line 0
A1	14	I	Address line 1
D	6	I/O	Drain pin. Can be an input or output.
EN	2	I	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A0 and A1 logic inputs determine which switch is turned on.
GND	13	P	Ground (0 V) reference
NC	7, 8, 9	No Connect	No internal connection
S1	4	I/O	Source pin 1. Can be an input or output.
S2	5	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	10	I/O	Source pin 4. Can be an input or output.
V_{DD}	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
V_{SS}	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (EN, A0, A1) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (EN, A0, A1) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	–30	30	mA
T_A	Ambient temperature	–55	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX6104 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} (1)	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	–5		–16.5	V

(1) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 33 V.

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S (2)	Source pins voltage	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (EN, A0, A1) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	–25		25	mA
T_A	Ambient temperature	–40		125	°C

(2) V_S is the voltage on all the S pins.

6.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			125	170	Ω
		V_S = ±10 V, I_S = 1 mA			145	200	Ω
			T_A = –40°C to +85°C			230	Ω
			T_A = –40°C to +125°C			250	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			1.5	6	Ω
			T_A = –40°C to +85°C			9	Ω
			T_A = –40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = –10 V, 0 V, +10 V, I_S = 1 mA			26	45	Ω
			T_A = –40°C to +85°C			53	Ω
			T_A = –40°C to +125°C			58	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.5		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.13		0.05	nA
			T_A = –40°C to +125°C	–1		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.05	0.01	0.05	nA
			T_A = –40°C to +85°C	–0.14		0.1	nA
			T_A = –40°C to +125°C	–1		0.5	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.07	0.01	0.07	nA
			T_A = –40°C to +85°C	–0.27		0.15	nA
			T_A = –40°C to +125°C	–2		1	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high		T_A = –40°C to +125°C	2			V
V_{IL}	Logic voltage low		T_A = –40°C to +125°C			0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			17	24	µA
			T_A = –40°C to +85°C			25	µA
			T_A = –40°C to +125°C			27	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			7	12	µA
			T_A = –40°C to +85°C			13	µA
			T_A = –40°C to +125°C			15	µA

(1) When V_S is positive, V_D is negative, and vice versa.

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6.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		85	120	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			130	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			140	ns
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		53	65	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			70	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			75	ns
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF		88	125	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			135	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			145	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	30	50		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		–0.35		pC
		V_S = –15 V to 15 V, R_S = 0 Ω , C_L = 1 nF		–0.41		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–86		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, non-adjacent channels		–105		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, adjacent channels		–87		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–7		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–52		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–49		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		500		MHz
THD + N	Total harmonic distortion + noise	R_L = 10k Ω , C_L = 5 pF, f= 20Hz to 20kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.2		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz		1.6	2.3	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 0 V, f = 1 MHz		3.8	4.2	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		5.0	6.5	pF

6.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	T_A = –40°C to +125°C	T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			235	345	Ω
			T_A = –40°C to +85°C			400	Ω
			T_A = –40°C to +125°C			440	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			2.4	12	Ω
			T_A = –40°C to +85°C			19	Ω
			T_A = –40°C to +125°C			23	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.47		%/°C

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Electrical Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.1		0.05	nA
			T_A = –40°C to +125°C	–0.8		0.4	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.03	0.01	0.03	nA
			T_A = –40°C to +85°C	–0.1		0.08	nA
			T_A = –40°C to +125°C	–0.8		0.4	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.05	0.01	0.05	nA
			T_A = –40°C to +85°C	–0.2		0.15	nA
			T_A = –40°C to +125°C	–1.6		0.8	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high		T_A = –40°C to +125°C	2			V
V_{IL}	Logic voltage low		T_A = –40°C to +125°C			0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V , V_{EN} = 3.3 V			12	18	µA
			T_A = –40°C to +85°C			19	µA
			T_A = –40°C to +125°C			21	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		91	125	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			135	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			145	ns
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		52	60	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			70	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			77	ns
t_{TRAN}	Transition time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		94	127	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			140	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			150	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	30	55		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω , C_L = 1 nF		–0.2		pC
		V_S = 0 V to 12 V, R_S = 0 Ω , C_L = 1 nF		–0.2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–86		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, non-adjacent channels		–107		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, adjacent channels		–87		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–14		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L= 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–51		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		400		MHz

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Switching Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.2		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz		1.9	2.3	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 6 V, f = 1 MHz		4.6	5.3	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		6.3	7.5	pF

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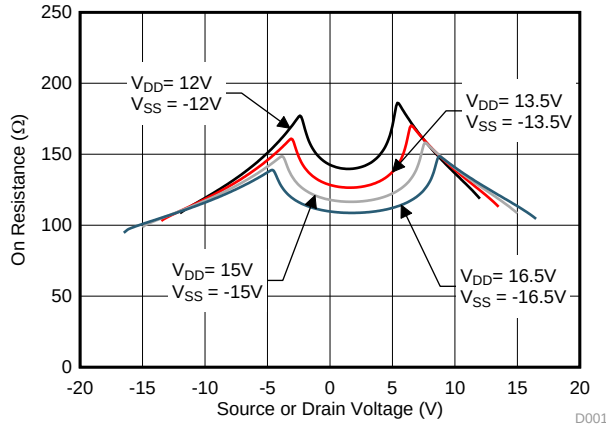
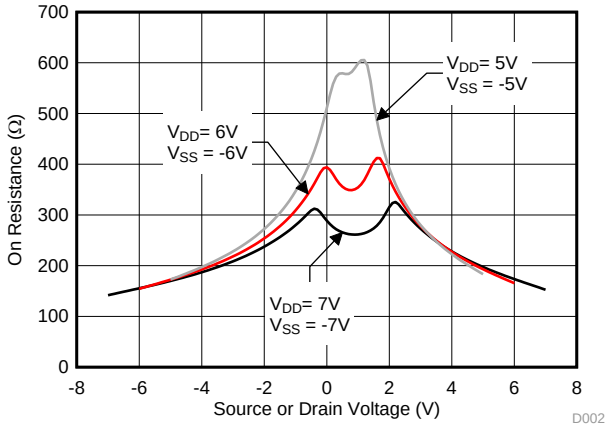
6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



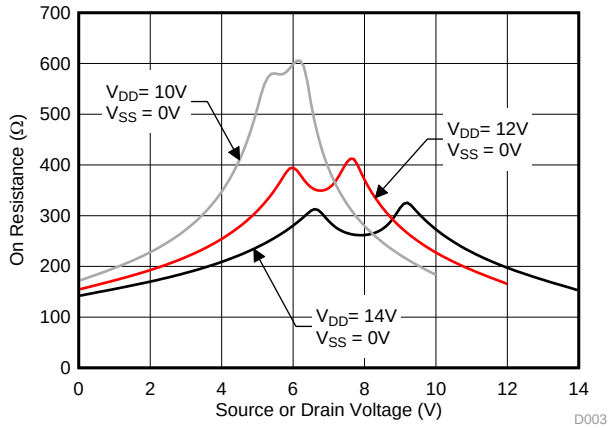
T_A = 25°C

図 1. On-Resistance vs Source or Drain Voltage



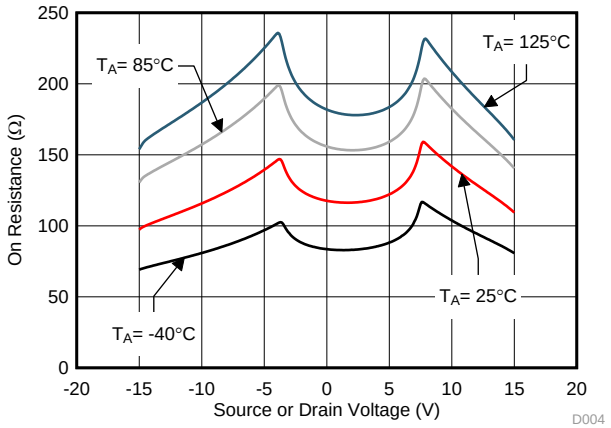
T_A = 25°C

図 2. On-Resistance vs Source or Drain Voltage



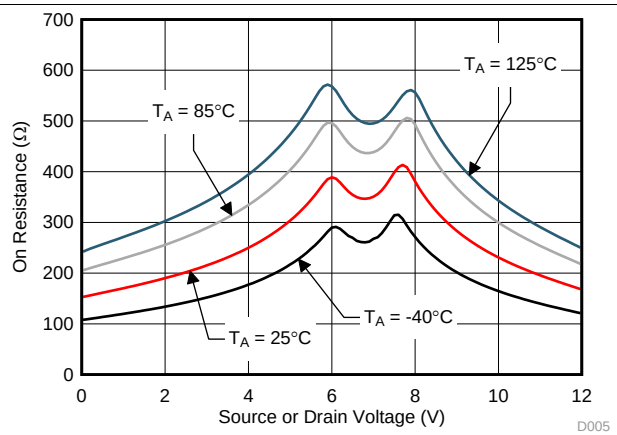
T_A = 25°C

図 3. On-Resistance vs Source or Drain Voltage



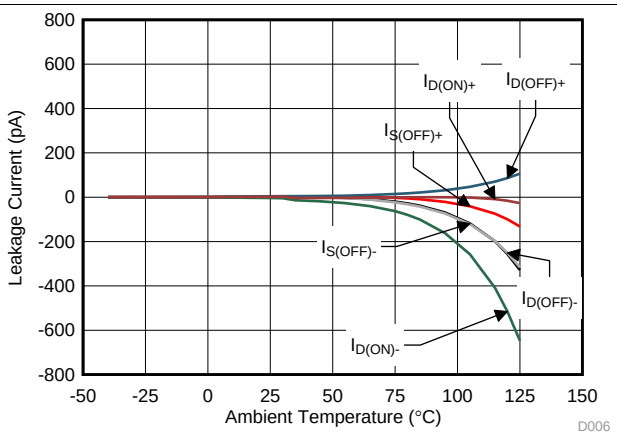
V_{DD} = 15 V, V_{SS} = –15 V

図 4. On-Resistance vs Source or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

図 5. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

図 6. Leakage Current vs Temperature

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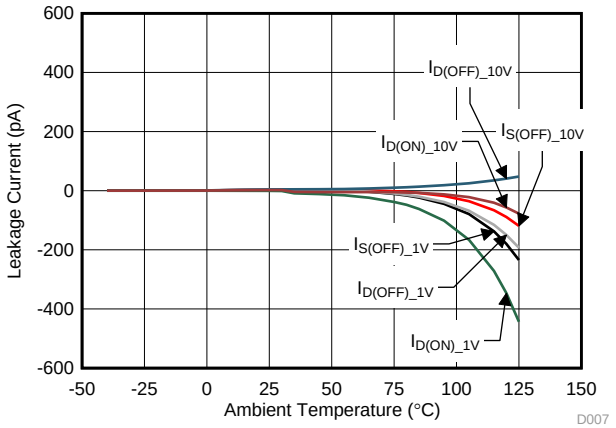
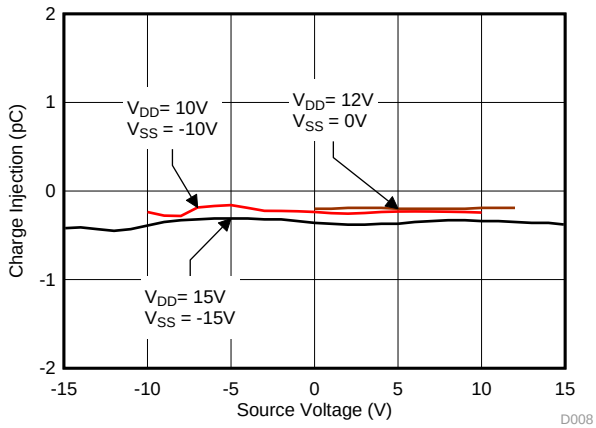
Typical Characteristics (continued)



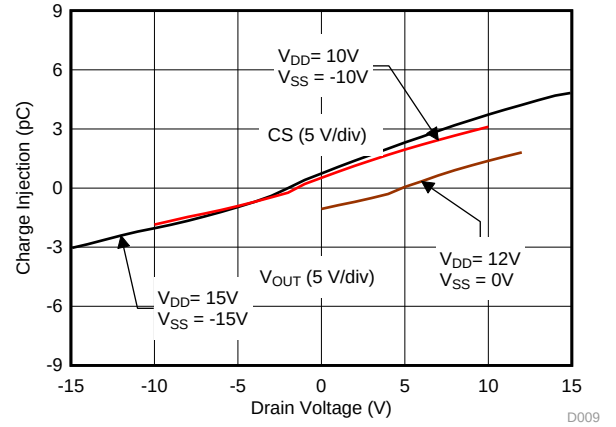
V_{DD} = 12 V, V_{SS} = 0 V

図 7. Leakage Current vs Temperature



Source-to-drain, T_A = 25°C

図 8. Charge Injection vs Source Voltage



Drain-to-source, T_A = 25°C

図 9. Charge Injection vs Drain Voltage

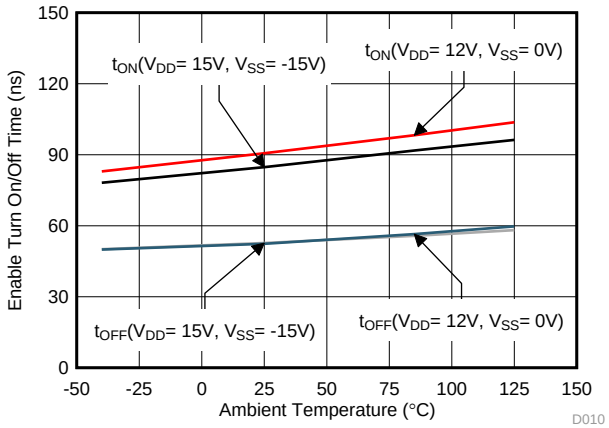
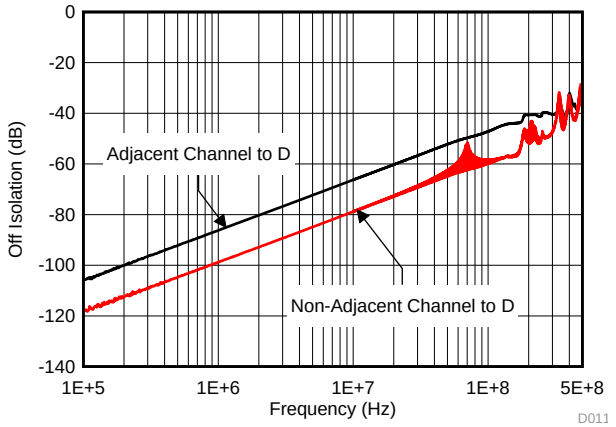
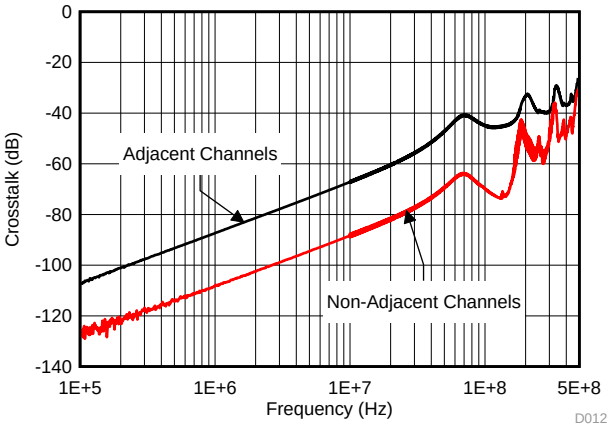


図 10. Turn-On and Turn-Off Times vs Temperature



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 11. Off Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 12. Crosstalk vs Frequency

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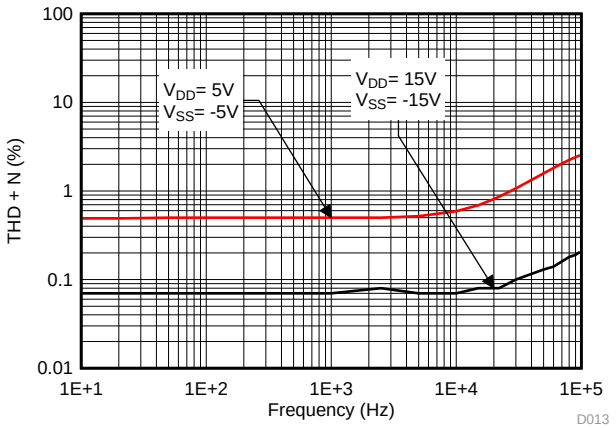
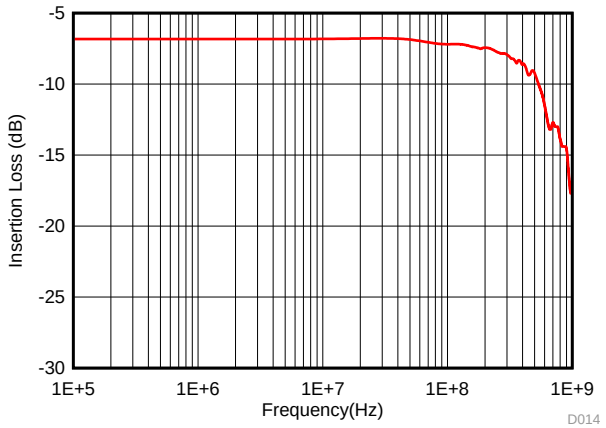
Typical Characteristics (continued)



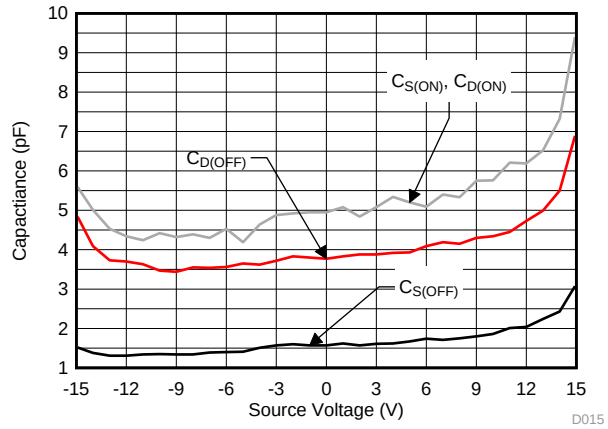
T_A = 25°C

図 13. THD+N vs Frequency



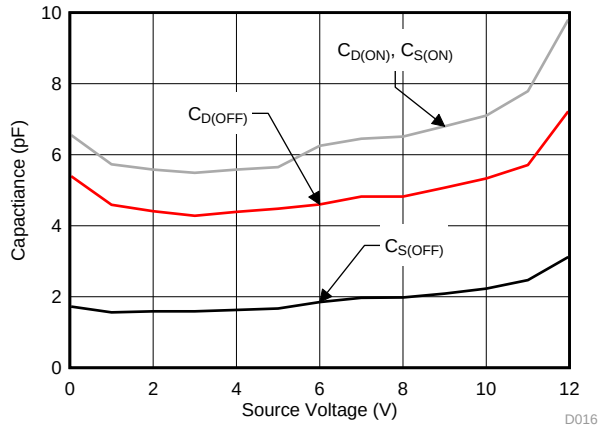
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 14. On Response vs. Frequency



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 15. Capacitance vs Source Voltage



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

図 16. Capacitance vs Source Voltage

7 Parameter Measurement Information

7.1 Truth Table

表 1. TMUX6104 Truth Table

EN	A1	A0	STATE
0	X(1)	X(1)	All channels are off
1	0	0	Channel 1
1	0	1	Channel 2
1	1	0	Channel 3
1	1	1	Channel 4

(1) X denotes *don't care*..

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8 Detailed Description

8.1 Overview

8.1.1 On-Resistance

The on-resistance of the TMUX6104 is the ohmic resistance across the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 17. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 式 1:

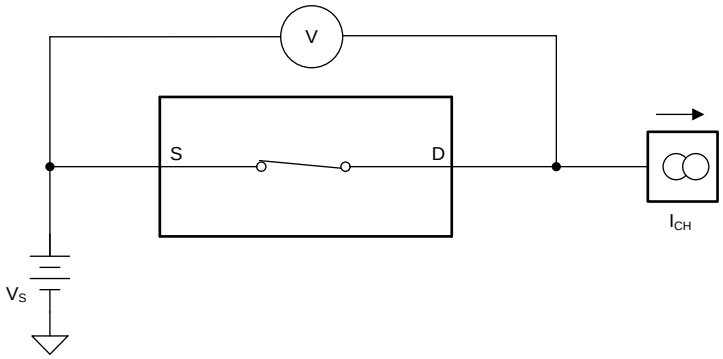

図 17. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

8.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 図 18

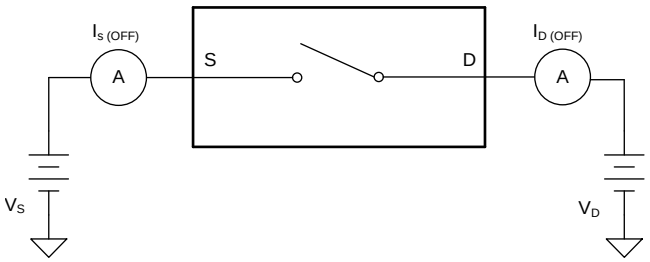

図 18. Off-Leakage Measurement Setup

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Overview (continued)

8.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 図 19 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

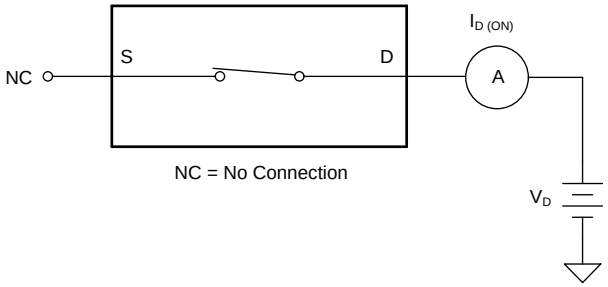

図 19. On-Leakage Measurement Setup

8.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6104 to rise (to 90% of the transition) or fall (to 10% of the transition) after the digital address signal has fallen or risen to 50% of the transition. 図 20 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

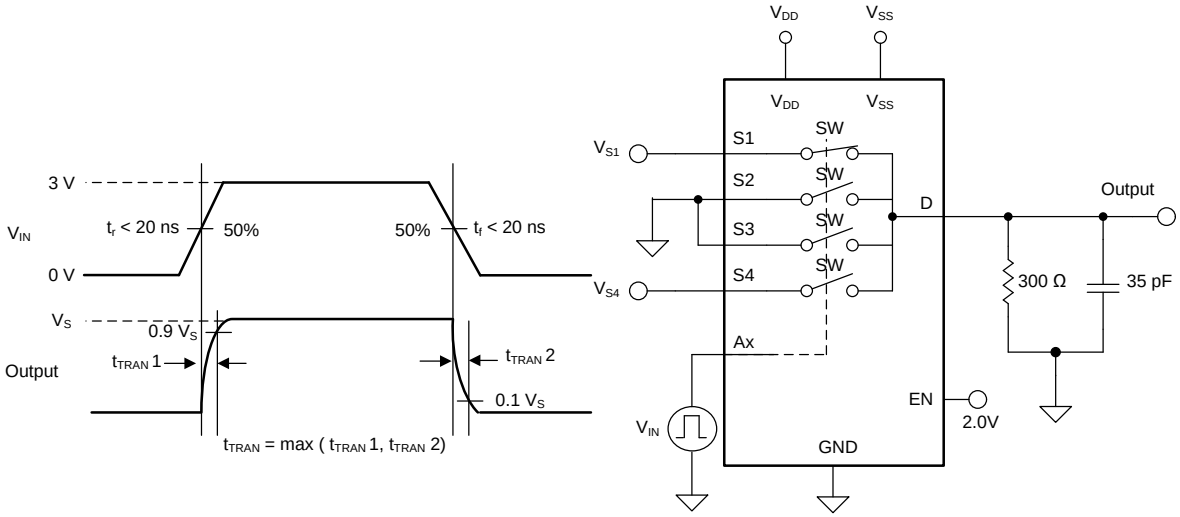

図 20. Transition-Time Measurement Setup

Overview (continued)

8.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6104 is switching. The TMUX6104 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 21 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

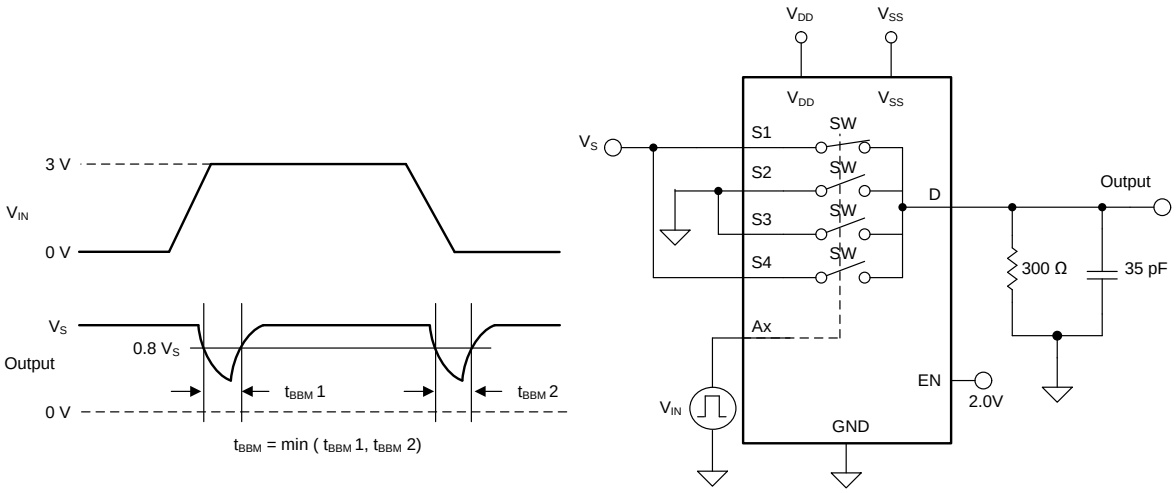

図 21. Break-Before-Make Delay Measurement Setup

8.1.6 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the TMUX6104 to rise to a 90% final value after the enable signal has risen to a 50% final value. 図 22 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol $t_{ON\ (EN)}$.

Turn off time is defined as the time taken by the output of the TMUX6104 to fall to a 10% initial value after the enable signal has fallen to a 50% initial value. 図 22 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol $t_{OFF\ (EN)}$.

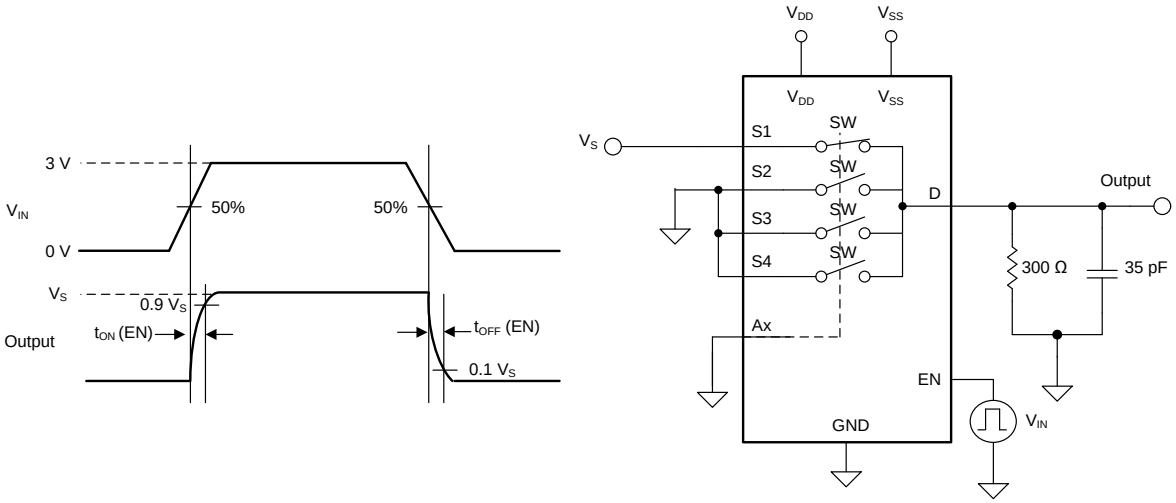

図 22. Turn-On and Turn-Off Time Measurement Setup

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Overview (continued)

8.1.7 Charge Injection

The TMUX6104 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 図 23 shows the setup used to measure charge injection from source (Sx) to drain (D).

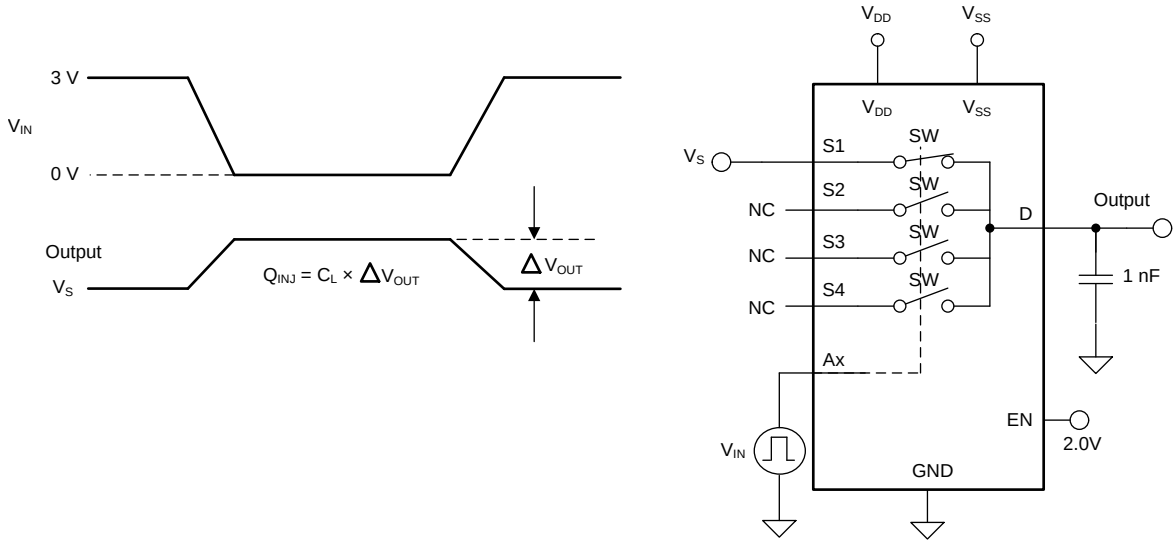

図 23. Charge-Injection Measurement Setup

8.1.8 Off Isolation

Off isolation is defined as the voltage at the drain pin (D) of the TMUX6104 when a 1-V_{RMS} signal is applied to the source pin (Sx) of an off-channel. 図 24 shows the setup used to measure off isolation. Use 式 2 to compute off isolation.

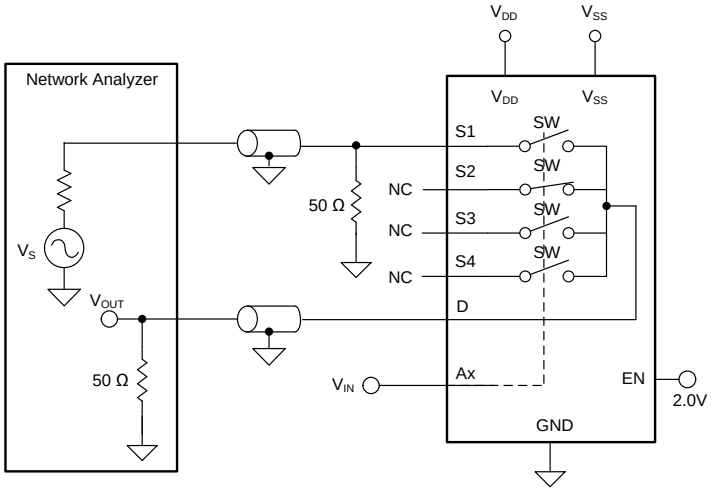

図 24. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

Overview (continued)

8.1.9 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin (Sx) of an on-channel. 図 25 shows the setup used to measure, and 式 3 is the equation used to compute, channel-to-channel crosstalk.

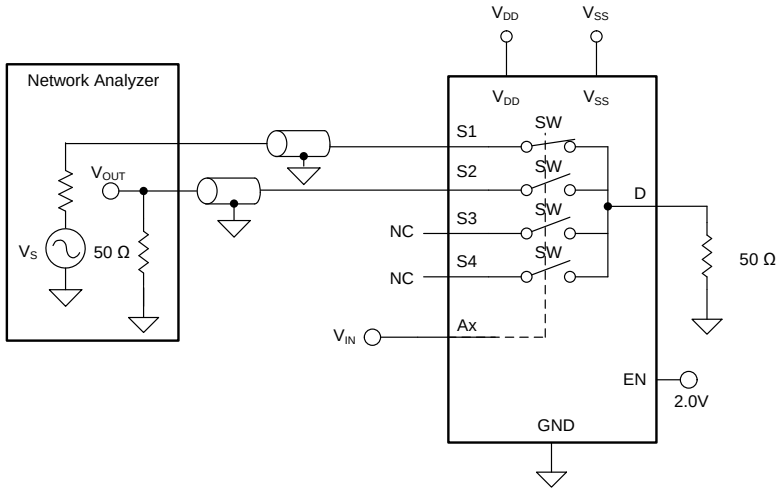

図 25. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

8.1.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the TMUX6104. 図 26 shows the setup used to measure bandwidth of the mux. Use 式 4 to compute the attenuation.

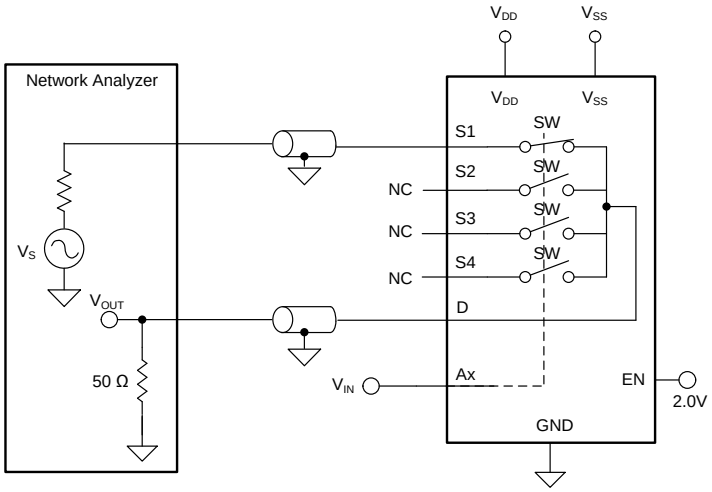

図 26. Bandwidth Measurement Setup

$$Attenuation = 20 \times Log\left(\frac{V_{OUT}}{V_S}\right) \quad (4)$$

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Overview (continued)

8.1.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6104 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.

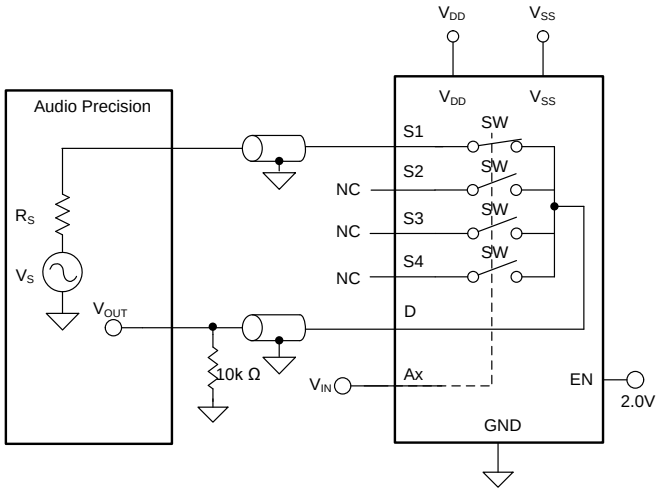


図 27. THD+N Measurement Setup

8.1.12 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

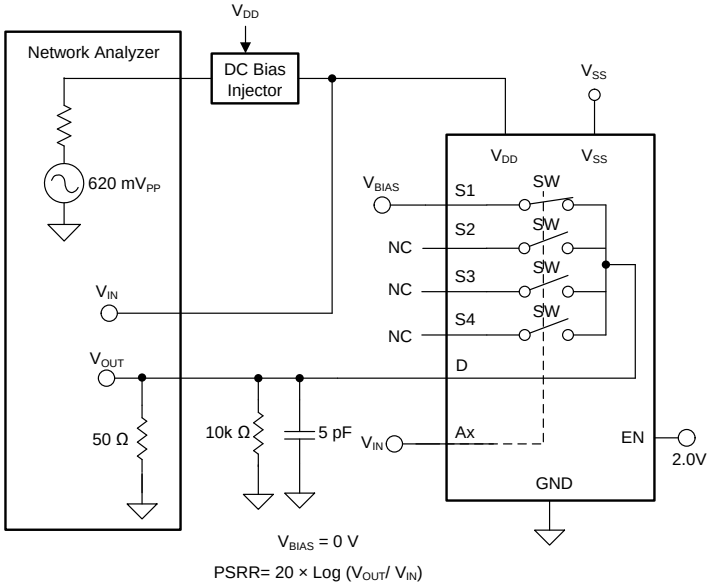
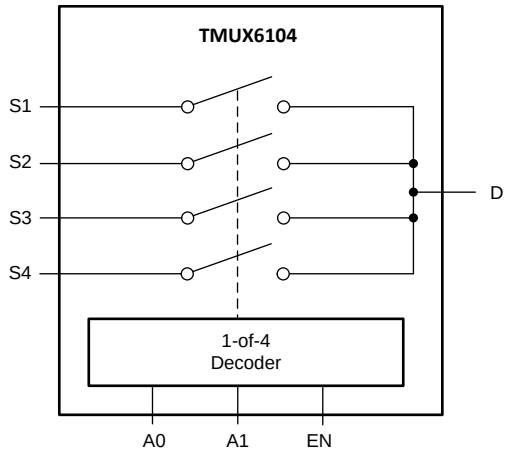


図 28. AC PSRR Measurement Setup

Overview (continued)

The *Functional Block Diagram* section provides a top-level block diagram of the TMUX6104. The TMUX6104 is a 4-channel, single-ended, analog multiplexer. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Ultralow Leakage Current

The TMUX6104 provide extremely low on- and off-leakage currents. The TMUX6104 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 図 29 shows typical leakage currents of the TMUX6104 versus temperature.

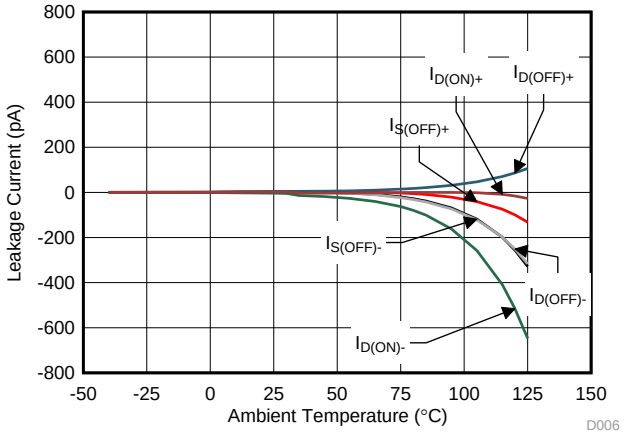

図 29. Leakage Current vs Temperature

8.3.2 Ultralow Charge Injection

The TMUX6104 is implemented with simple transmission gate topology, as shown in 図 30. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

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Feature Description (continued)

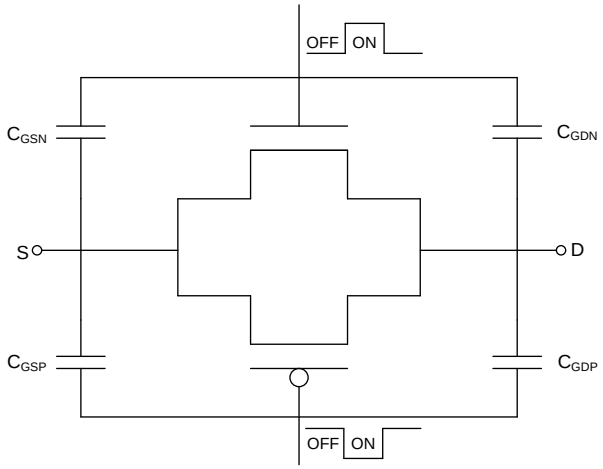

図 30. Transmission Gate Topology

The TMUX6119 utilizes special charge-injection cancellation circuitry that reduces the source (Sx) to drain (D) charge injection to as low as –0.35 pC at V_S = 0 V, and –0.41 pC in the full signal range, as shown in 図 31.

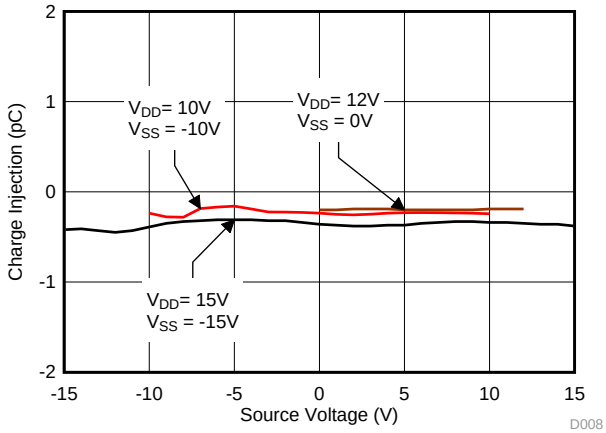

図 31. Source-to-Drain Charge Injection vs Source Voltage

The drain (D)-to-source (Sx) charge injection becomes important when the device is used as a demultiplexer (demux), where the drain (D) becomes the input and the source (Sx) becomes the output. 図 32 shows the drain-to-source charge injection across the full signal range.

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Feature Description (continued)

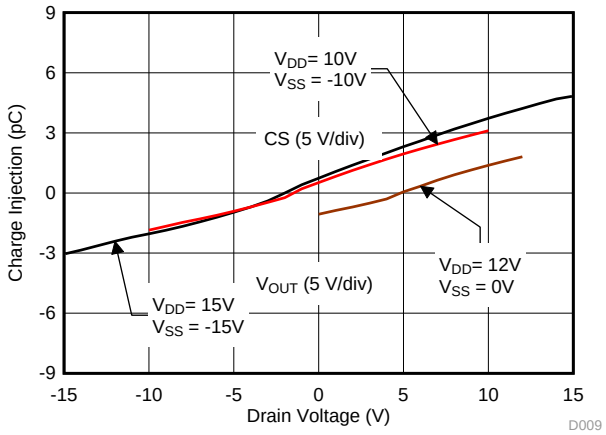

図 32. Drain-to-Source Charge Injection vs Drain Voltage

8.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6104 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each TMUX6104 channel has very similar characteristics in both directions. The valid analog signal for TMUX6104 ranges from V_{SS} to V_{DD}. The input signal to the TMUX6104 swings from V_{SS} to V_{DD} without any significant degradation in performance.

8.4 Device Functional Modes

When the EN pin of the TMUX6104 is pulled high, one of the four switches is closed based on the state of the address pins (A0 and A1). When the EN pin is pulled low, all four switches remain open irrespective of the state of the address pins. The EN pin is weakly pull-down internally through a 6 MΩ resistor; thereby, setting each channel to the open state if the EN pin is not actively driven. The address pins are also weakly pulled-down through an internal 6 MΩ resistor, allowing channel 1 (S1 to D) to be selected by default when EN pin is driven high. Both the EN pin and the address pins can be connected to V_{DD} (as high as 16.5 V).

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX6104 offers outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 33 V, and offer true rail-to-rail input and output. The on-capacitance of the TMUX6104 is very low. These features makes the TMUX6104 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

9.2 Typical Application

図 33 shows a 16-bit, differential, 4-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel single-ended mux. This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the TMUX6104 and OPA192 to achieve excellent dynamic performance and linearity with the ADS8864.

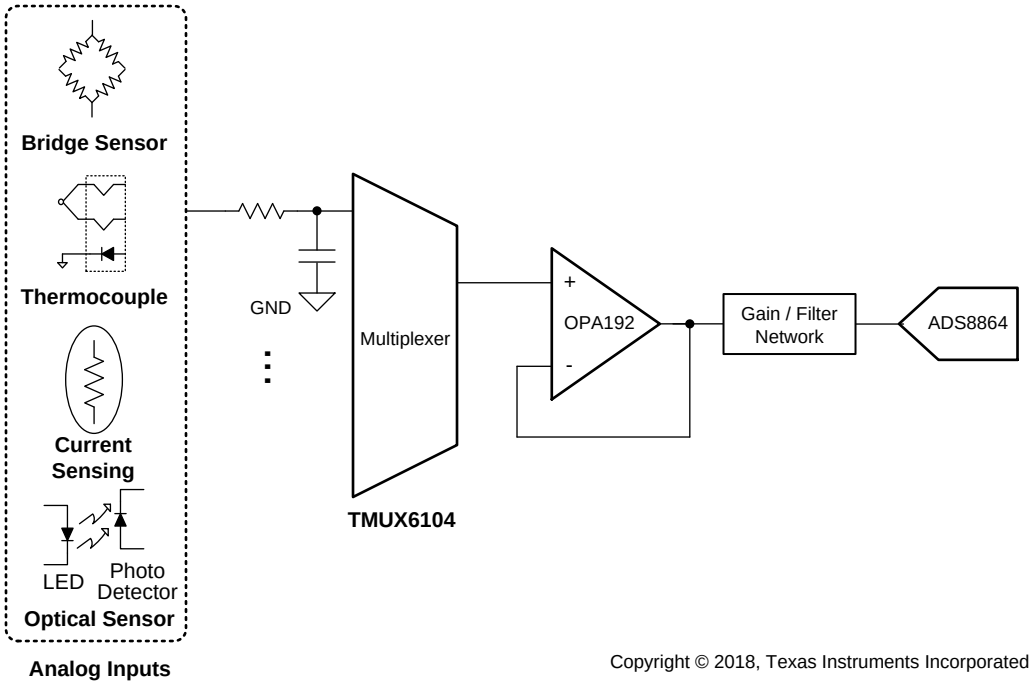

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図 33. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

Typical Application (continued)

9.2.1 Design Requirements

The primary objective is to design a ±15 V, single-ended, 4-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 15 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

9.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in 図 33. The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, and attenuating SAR ADC driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel.

9.2.3 Application Curve

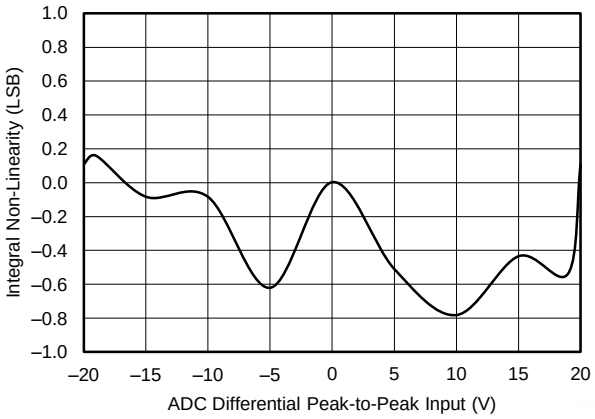

図 34. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

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10 Power Supply Recommendations

The TMUX6104 operates across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). The device also perform well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground.

The on-resistance of the TMUX6104 varies with supply voltage, as illustrated in 図 35

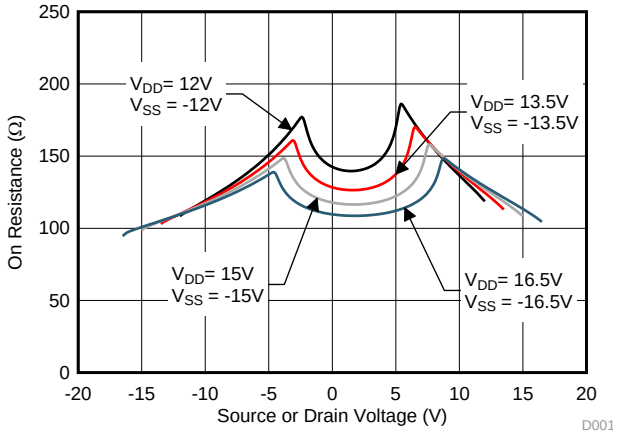

図 35. On-Resistance Variation With Supply and Input Voltage

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11 Layout

11.1 Layout Guidelines

図 36 illustrates an example of a PCB layout with the TMUX6104.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

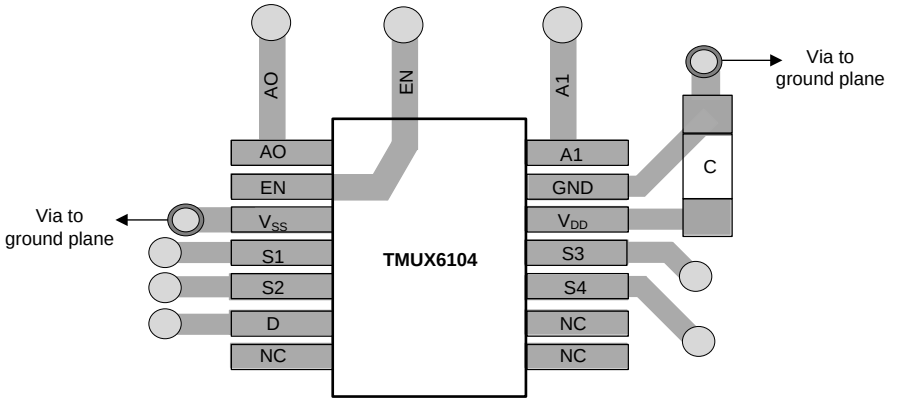

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図 36. TMUX6104 Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

- 『ADS8664 12ビット、500kSPS、4および8チャネル、シングル電源、バイポーラ入力範囲のSAR ADC』(SBAS492)
- 『OPA192　36V、高精度、レール・ツー・レール入力/出力、低オフセット電圧、低入力バイアス電流、e-trim™搭載のオペアンプ』(SBOS620)

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX6104PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	MUX6104
TMUX6104PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6104
TMUX6104PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6104
TMUX6104PWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6104

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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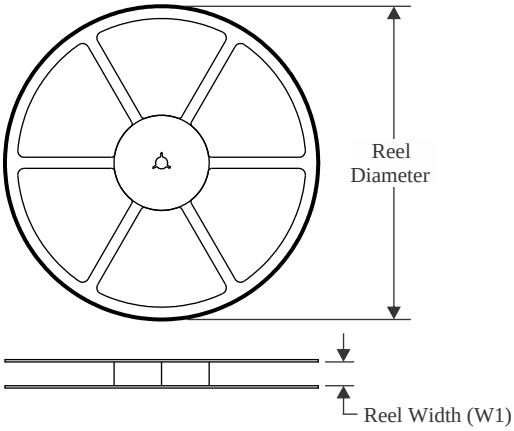
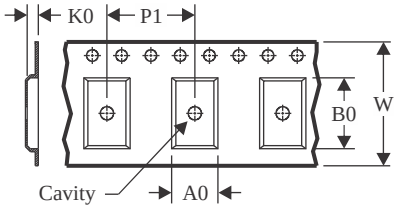
TAPE AND REEL INFORMATION

REEL DIMENSIONS

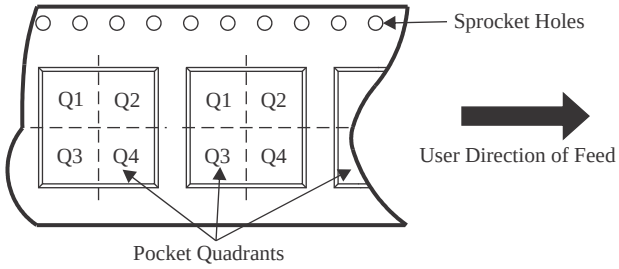


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

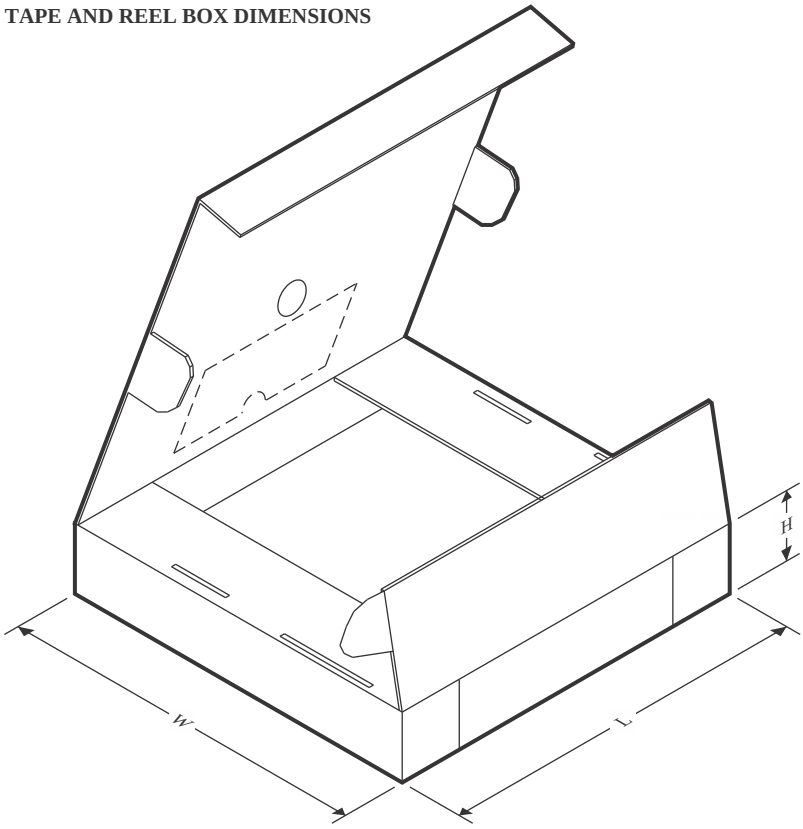
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6104PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

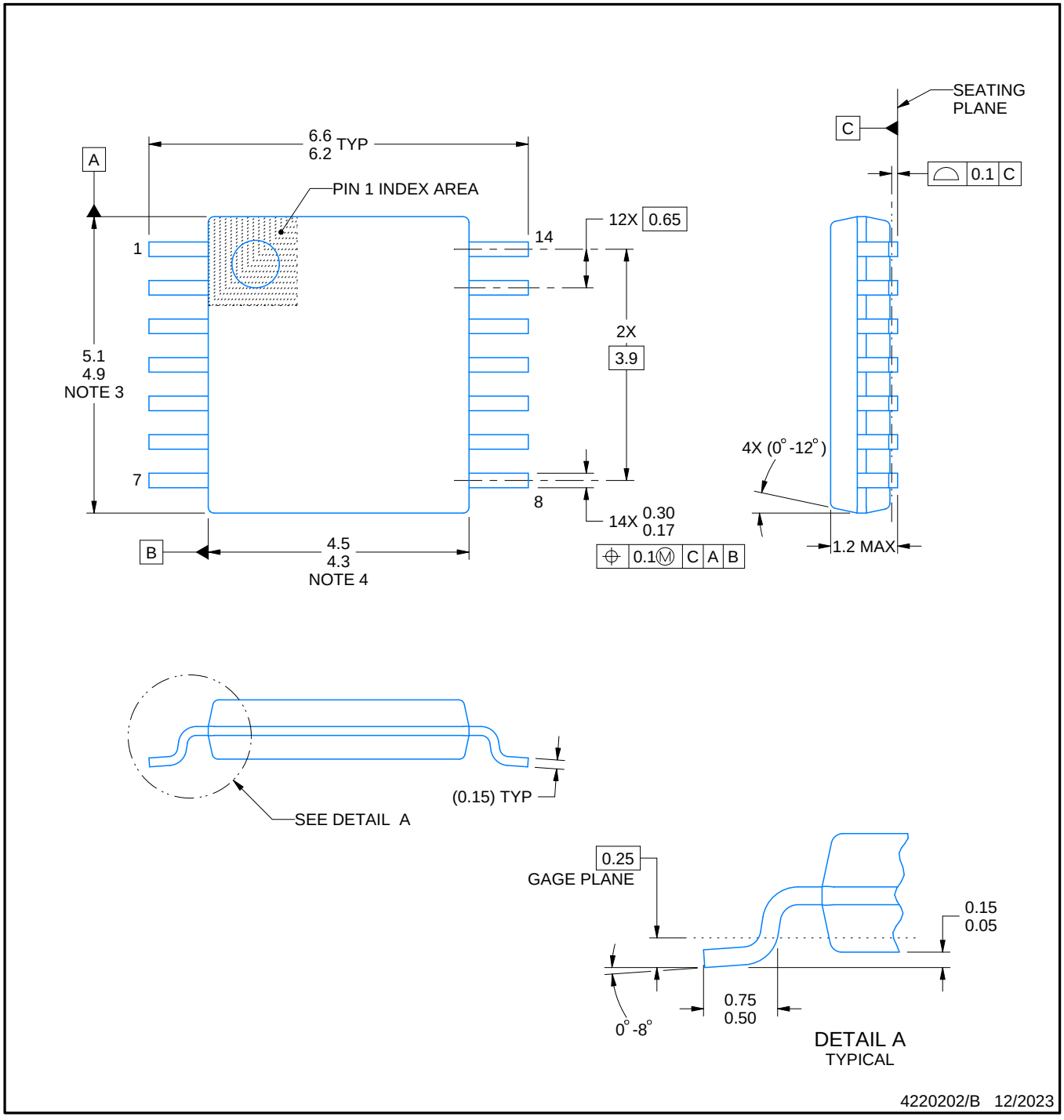
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6104PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TMUX6104PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TMUX6104PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0014A

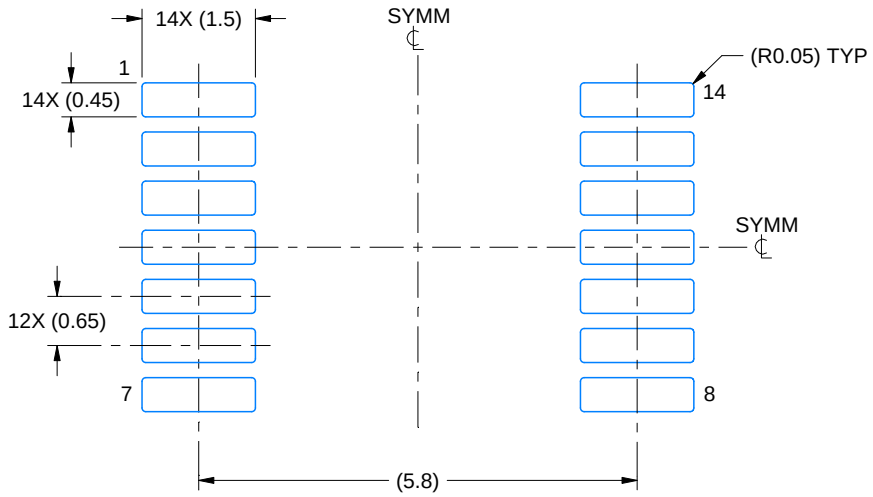
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

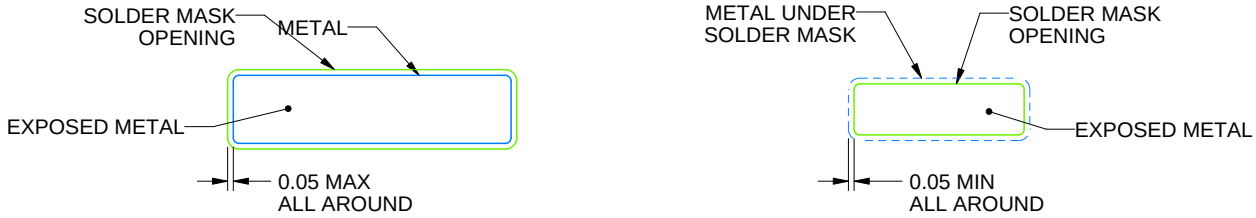


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

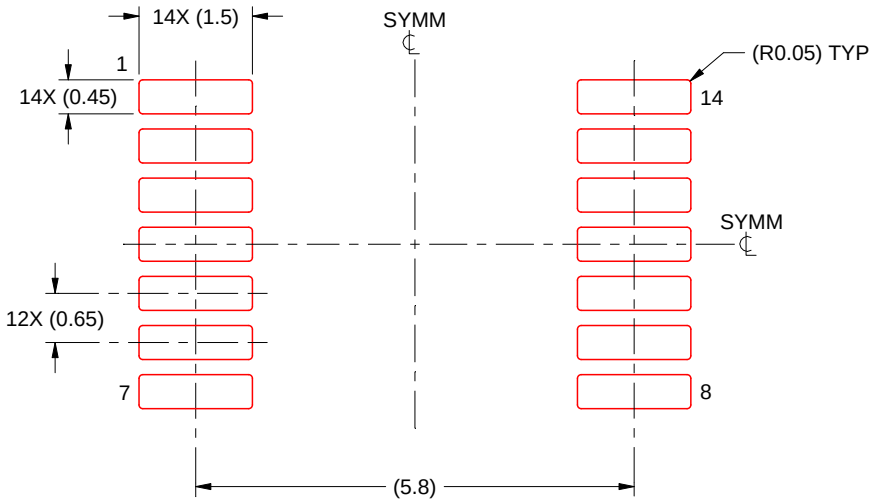


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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