TPD2E2U06-Q1 車載用デュアル・チャネル高速 ESD 保護デバイス

1 特長

- AEC-Q101 準拠
- IEC 61000-4-2 レベル 4 ESD 保護
  - ±25kV (接触放電)
  - ±30kV (空中放電)
- ISO 10605 (330pF、330Ω) ESD 保護
  - ±20kV (接触放電)
  - ±25kV (空中放電)
- IO 容量:1.5pF (標準値)
- DC ブレークダウン電圧:6.5V (最小値)
- 超低リーク電流:10nA (最大値)
- 低 ESD クランプ電圧
- 産業用温度範囲:-40℃～+125℃
- 配線が容易な小型 DBZ および DCK パッケージ

2 アプリケーション

- 最終製品:
  - ヘッド・ユニット
  - 後部座席用エンターテインメント
  - テレマティクス
  - ナビゲーション・モジュール
  - メディア・インターフェイス
- インターフェイス:
  - USB 2.0
  - イーサネット™
  - アンテナ
  - LVDS
  - I^2C

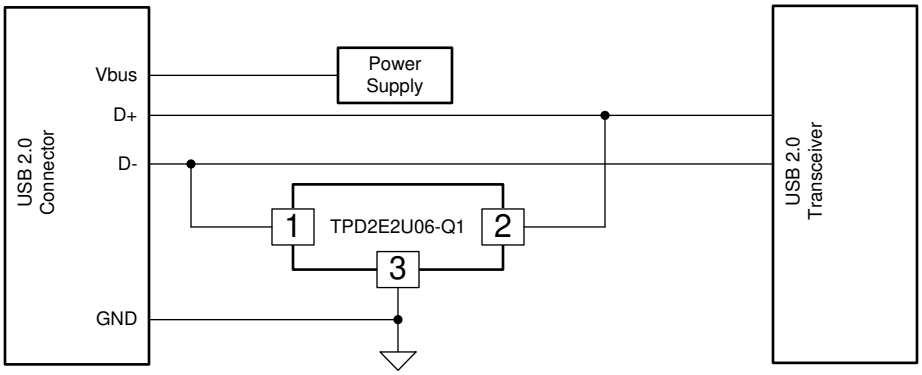
3 概要

TPD2E2U06-Q1 は低キャパシタンスの過渡電圧サプレッサ (TVS)、静電気放電 (ESD) 保護ダイオード・アレイです。このデュアル・チャネル ESD 保護ダイオードは、IEC 61000-4-2 国際規格で規定されている最大レベルを上回る ESD のエネルギーを吸収するように定格が設定されています。1.5pF のライン・キャパシタンスにより、TPD2E2U06-Q1 は USB 2.0、イーサネット、LVDS、アンテナ、I^2C などのインターフェイス保護に理想的です。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPD2E2U06-Q1	DBZ (SOT23、3)	2.92mm × 1.30mm
	DCK (SC70、3)	2.00mm × 1.25mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (May 2016) to Revision E (October 2022) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated the *Surge Curve (t_p = 8/20 µs) IO to GND* figure ... 6

Changes from Revision C (March 2016) to Revision D (May 2016) — **Page**

- 「*特長*」、「*アプリケーション*」、「*概要*」を更新 ... 1
- 「*ESD 定格 — AEC 仕様*」の表を更新 ... 1

Changes from Revision B (December 2014) to Revision C (March 2016) — **Page**

- DCK パッケージを追加 ... 1
- 「*熱に関する情報*」の表の DCK の熱データを追加 ... 1

Changes from Revision A (December 2014) to Revision B (December 2014) — **Page**

- Added temperature specification to V_{BR} TEST CONDITIONS. ... 5

Changes from Revision * (December 2014) to Revision A (December 2014) — **Page**

- 完全版の初回リリース ... 1

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5 Pin Configuration and Functions

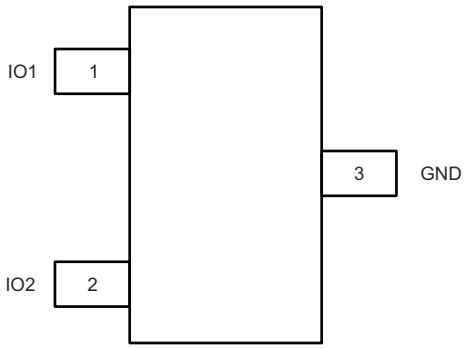


図 5-1. DBZ Package, 3-Pin SOT23 (Top View)

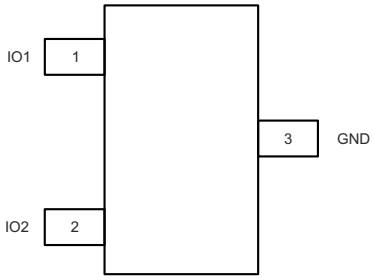


図 5-2. DCK Package, 3-Pin SC70 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO1	1	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	2	I/O	
GND	3	G	The GND (ground) pin is connected to ground.

(1) I = input, O = output, G = ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
I_{PP}	Peak pulse current (t_p = 8/20 µs)		5.5(2)	A
P_{PP}	Peak pulse power (t_p = 8/20 µs)		75(2)	W
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured at 25°C.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±10000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AAEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2	Contact discharge	±25000	V
			Air-gap discharge	±30000	

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω)	Contact discharge	±20000	V
			Air-gap discharge	±25000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free air temperature	–40	125	℃

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6.6 Thermal Information

THERMAL METRIC[1]		TPD2E2U06-Q1		UNIT
		DBZ (SOT23)	DCK (SC70)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	439.5	308.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	194.9	170.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	173.9	89.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	53.7	34.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	172	88.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA			5.5	V
V_{CLAMP}	IO to GND	I_{PP} = 1 A, TLP[1] [3]		9.7		V
		I_{PP} = 5 A, TLP[1] [3]		12.4		
V_{CLAMP}	GND to IO	I_{PP} = 1 A, TLP[1] [3]		1.9		V
		I_{PP} = 5 A, TLP[1] [3]		4		
R_{DYN}	Dynamic resistance	IO to GND[2] [3]		0.6		Ω
		GND to IO[2] [3]		0.4		
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V[3]		1.5	1.9	pF
C_{CROSS}	Channel-to-channel input capacitance	Pin 3 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins[3]		0.02	0.03	pF
Δ_{CL}	Variation of channel input capacitance	Pin 3 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, Pin 1 to GND – Pin 2 to GND[3]		0.03	0.1	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA[3]	6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V		1	10	nA

(1) Transmission Line Pulse with 10-ns rise time, 100-ns width.
(2) Extraction of R_{DYN} Using least squares fit of TLP characteristics between I = 20 A and I = 30 A.
(3) Measured at 25°C.

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6.8 Typical Characteristics

Measured at T_A = 25°C unless otherwise specified

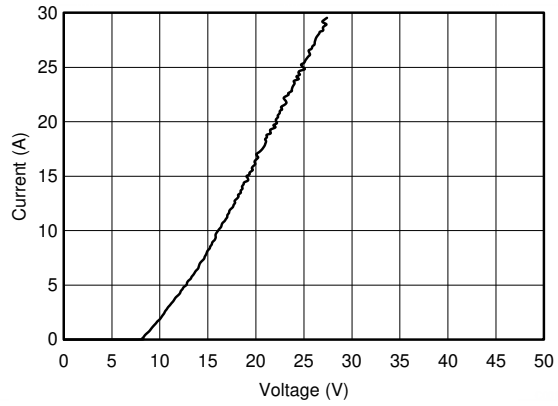


図 6-1. TLP, Data to GND

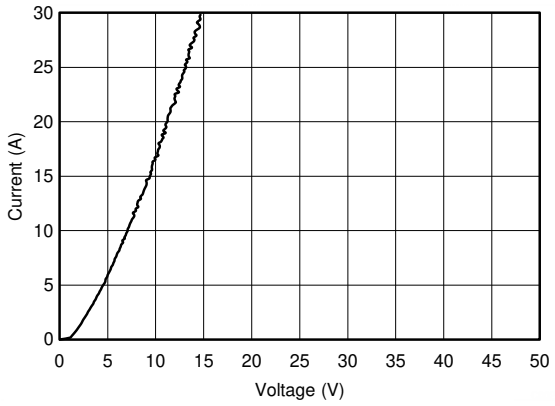


図 6-2. TLP, GND to Data

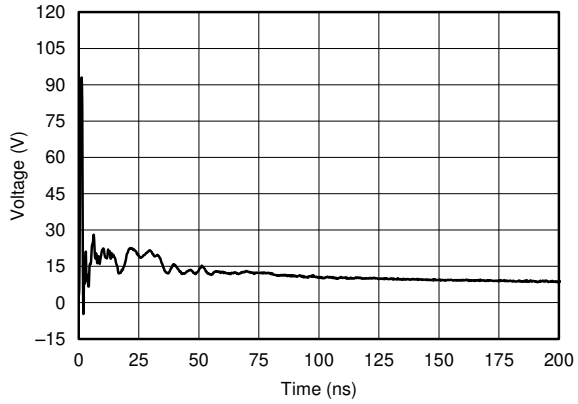


図 6-3. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

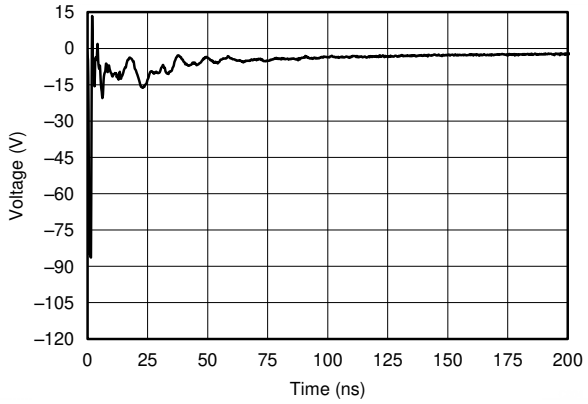


図 6-4. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

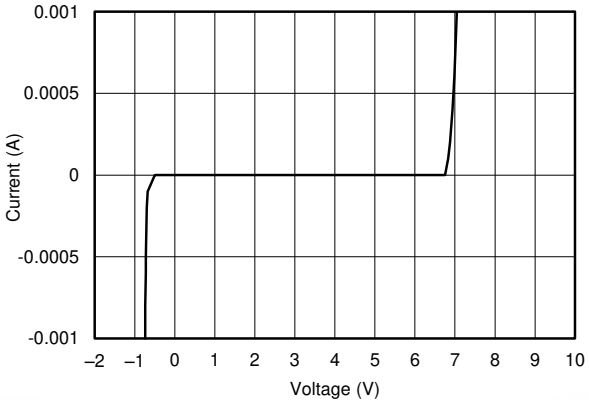


図 6-5. IV Curve, T_A = 25°C

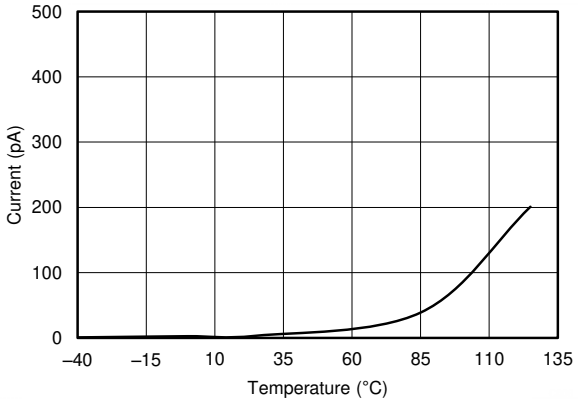


図 6-6. I_{LEAK} vs Temperature, V_{IN} = 2.5 V

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6.8 Typical Characteristics (continued)

Measured at T_A = 25°C unless otherwise specified

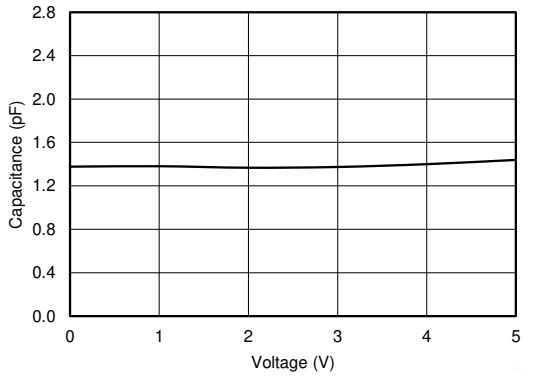


図 6-7. Capacitance Across V_{BIAS} f = 1 MHz

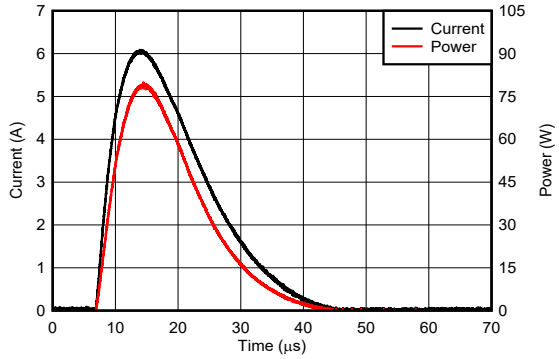


図 6-8. Surge Curve (t_p = 8/20 µs) IO to GND

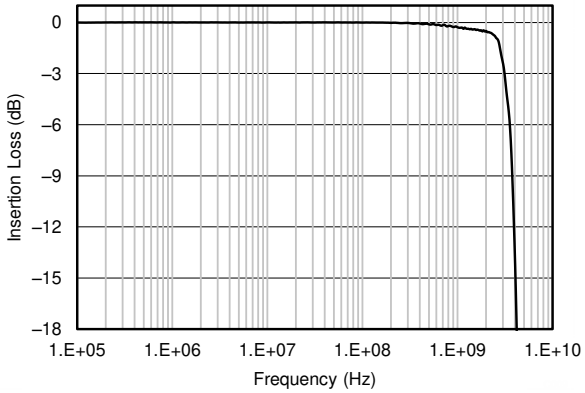


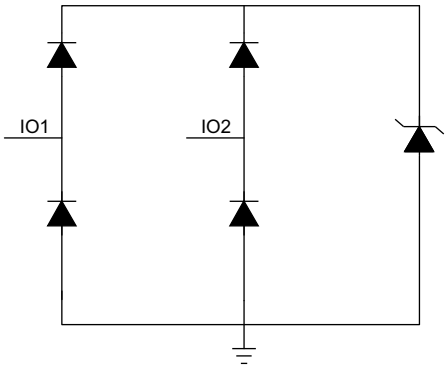
図 6-9. Insertion Loss

7 Detailed Description

7.1 Overview

The TPD2E2U06-Q1 device is a TVS ESD protection diode array with low capacitance. It is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The 1.5-pF line capacitance makes it ideal for protecting interfaces such as USB 2.0, LVDS, antenna, and I^2C.

7.2 Functional Block Diagram



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7.3 Feature Description

The TPD2E2U06-Q1 device is a TVS ESD protection diode array with low capacitance. It is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The 1.5-pF line capacitance makes it ideal for protecting interfaces such as USB 2.0, LVDS, antenna, and I^2C.

7.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards. It passes HBM H3B (±8 kV) and CDM C5 (±1 kV) ESD ratings and is qualified to operate from –40°C to +125°C.

7.3.2 IEC 61000-4-2 Level 4

The I/O pins can withstand ESD events up to ±25-kV contact and ±30-kV air. An ESD-surge clamp diverts the current to ground.

7.3.3 IO Capacitance

The capacitance between each I/O pin to ground is 1.5 pF. These capacitances support data rates in excess of 1.5 Gbps.

7.3.4 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

7.3.5 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Maximum) with a bias of 2.5 V.

7.3.6 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.7 V (I_{PP} = 1 A).

7.3.7 Industrial Temperature Range

This device is designed to operate from –40°C to +125°C.

7.3.8 Small Easy-to-Route Packages

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offer flow-through routing, requiring minimal modification to an existing layout.

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7.4 Device Functional Modes

The TPD2E2U06-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±30 kV (air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of the TPD2E2U06-Q1 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

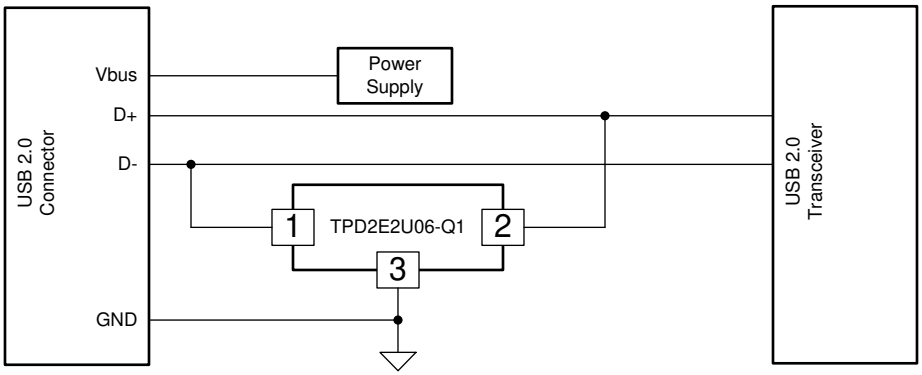
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8.1 Application Information

The TPD2E2U06-Q1 device is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application



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図 8-1. Typical USB Application Diagram

8.2.1 Design Requirements

For this design example, one TPD2E2U06-Q1 device will be used in a USB 2.0 application. This will provide complete port protection.

Given the USB 2.0 application, the parameters listed in 表 8-1 are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1 or 2	0 V to 3.3 V
Operating frequency	240 MHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD2E2U06-Q1 device has 2 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 2 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD2E2U06-Q1 device has a capacitance of 1.5 pF (typical), supporting USB 2.0 data rates.

8.2.3 Application Curve

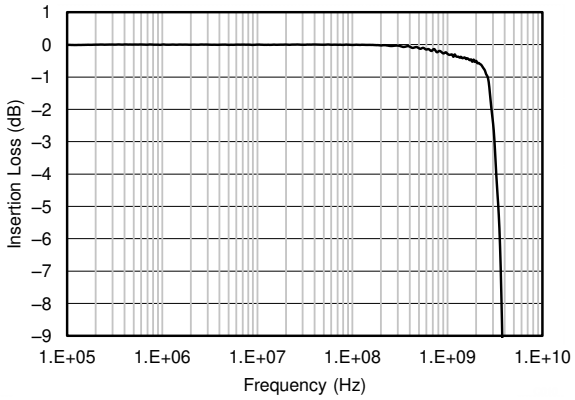


図 8-2. Insertion Loss Graph

9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Make sure that the maximum voltage specifications for each line are not violated.

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10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

This application is typical of a differential data pair application, such as USB 2.0.

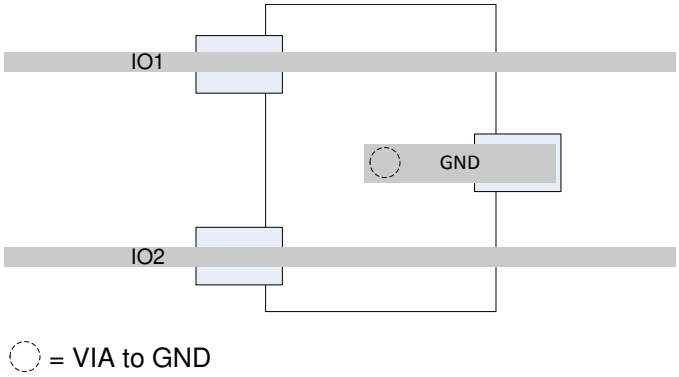


図 10-1. Routing with DBZ Package

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet* application report
- Texas Instruments, *ESD Protection Layout Guide* application report
- Texas Instruments, *TPD4E02B04EVM* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD2E2U06QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	22U6Q
TPD2E2U06QDBZRQ1.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22U6Q
TPD2E2U06QDBZRQ1G4	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22U6Q
TPD2E2U06QDBZRQ1G4.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22U6Q
TPD2E2U06QDCKRQ1	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	11X
TPD2E2U06QDCKRQ1.B	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11X

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD2E2U06-Q1 :

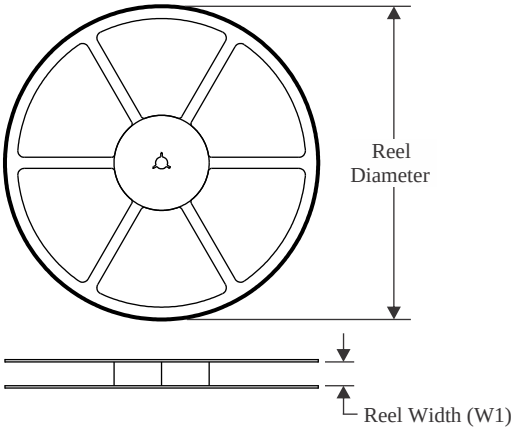
- Catalog : TPD2E2U06

NOTE: Qualified Version Definitions:

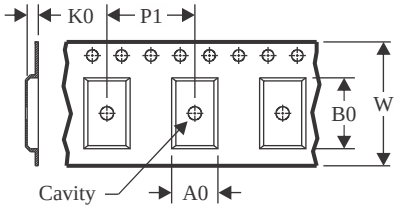
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

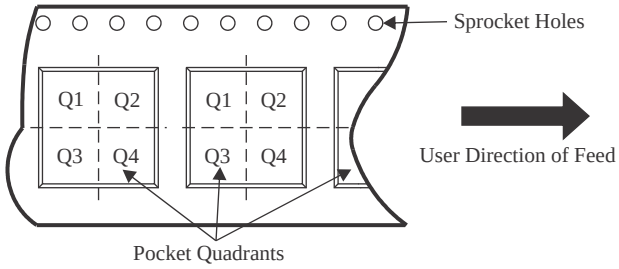


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

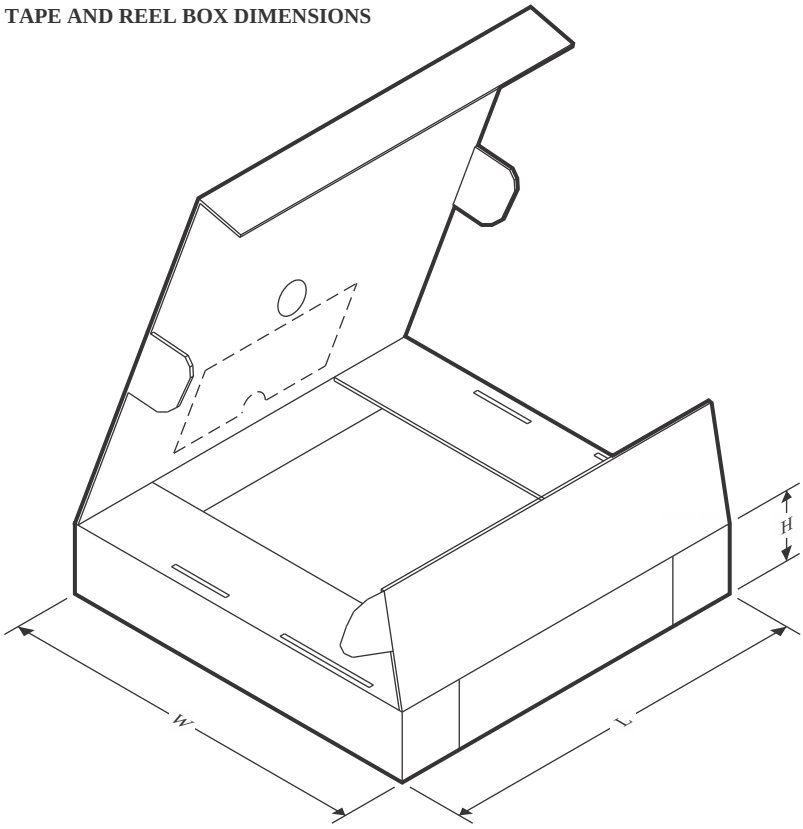
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
TPD2E2U06QDBZRQ1G4	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TPD2E2U06QDBZRQ1G4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TPD2E2U06QDCKRQ1	SC70	DCK	3	3000	180.0	8.4	2.3	2.75	1.2	4.0	8.0	Q3
TPD2E2U06QDCKRQ1	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

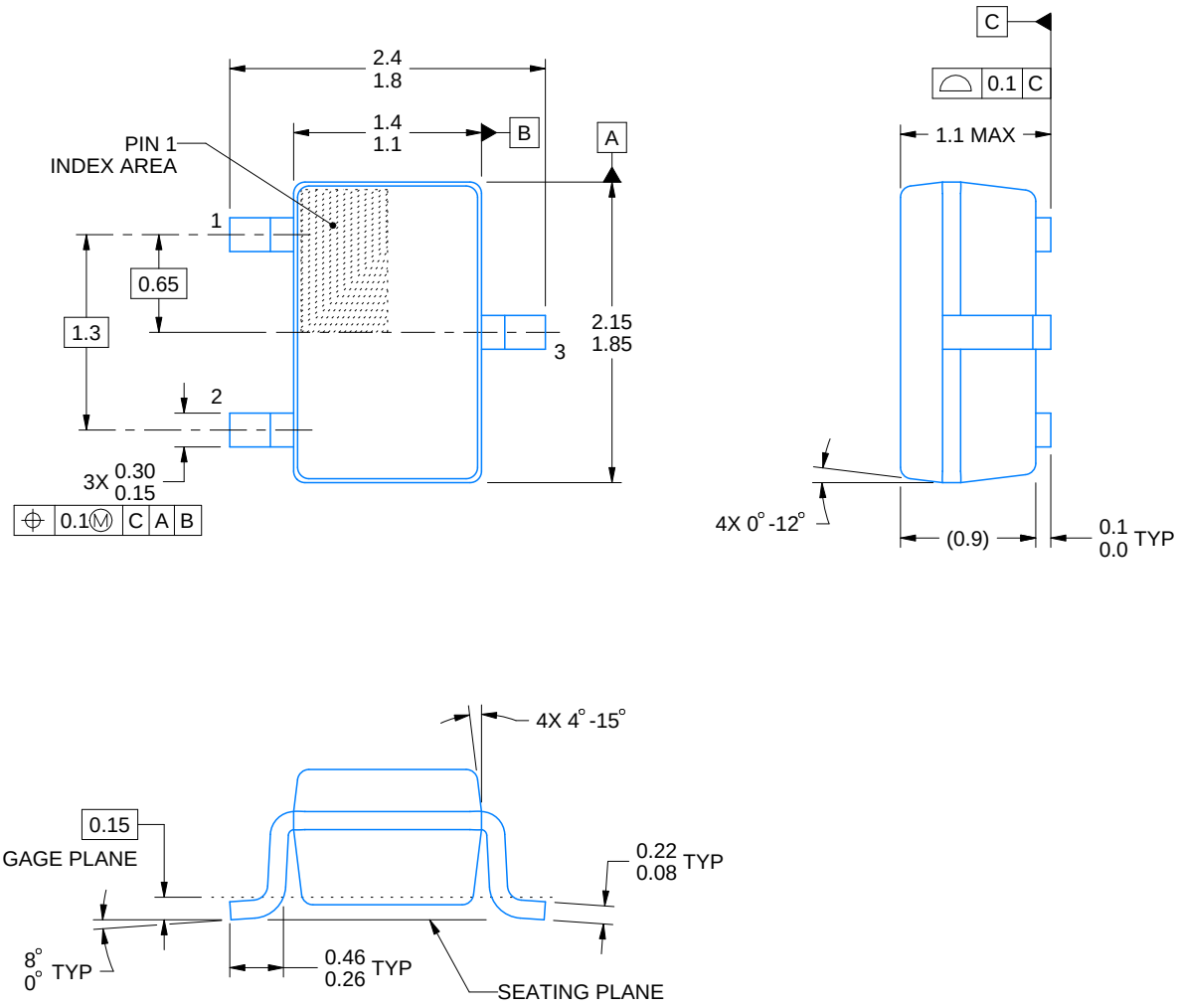
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TPD2E2U06QDBZRQ1G4	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TPD2E2U06QDBZRQ1G4	SOT-23	DBZ	3	3000	213.0	191.0	35.0
TPD2E2U06QDCKRQ1	SC70	DCK	3	3000	210.0	185.0	35.0
TPD2E2U06QDCKRQ1	SC70	DCK	3	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

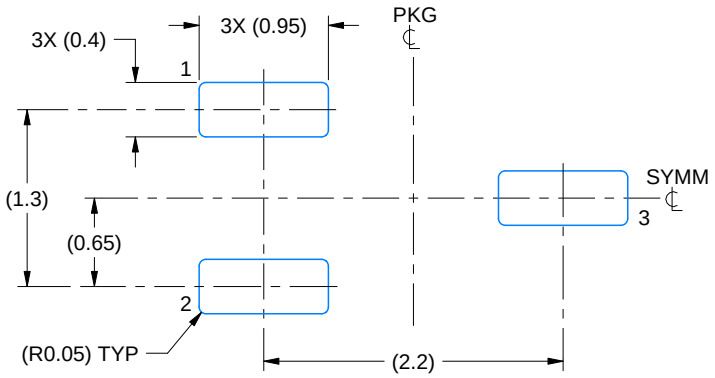
SMALL OUTLINE TRANSISTOR SC70



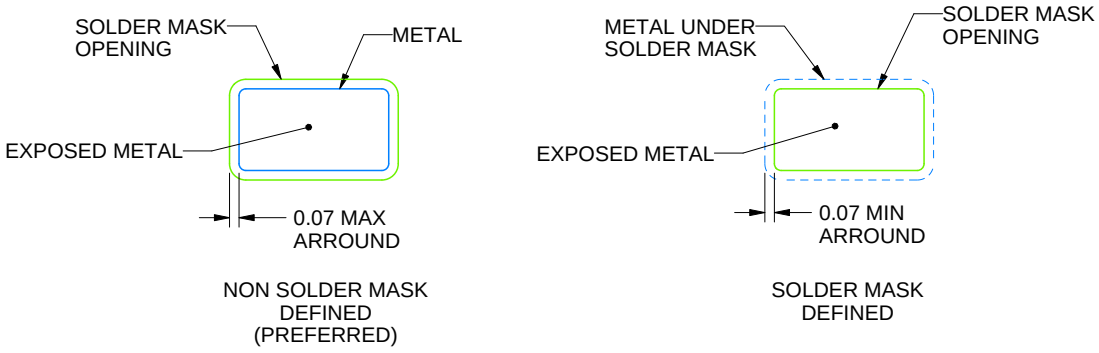
4220745/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

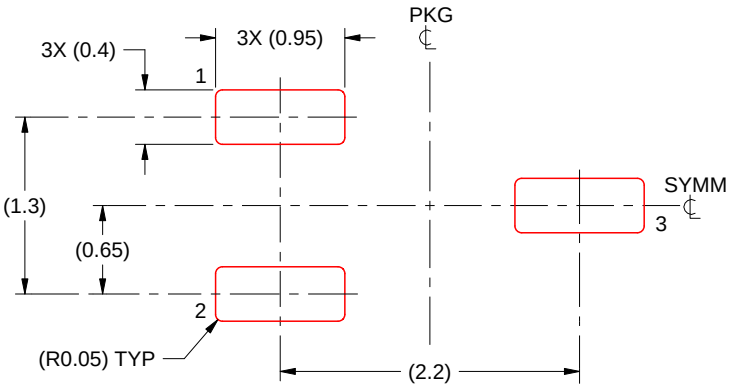


SOLDER MASK DETAILS

4220745/F 11/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

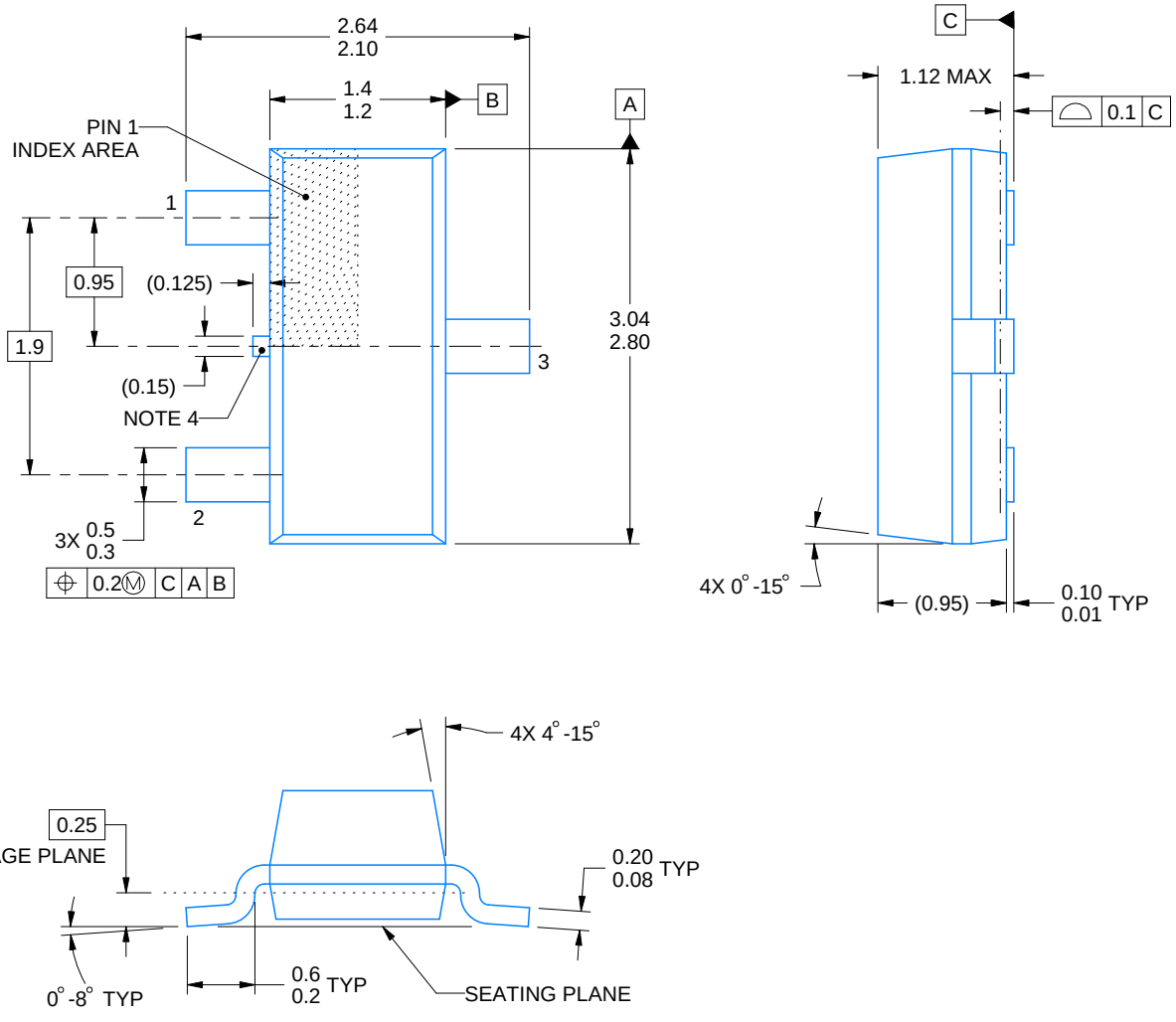
PACKAGE OUTLINE

DBZ0003A



SOT-23 - 1.12 mm max height

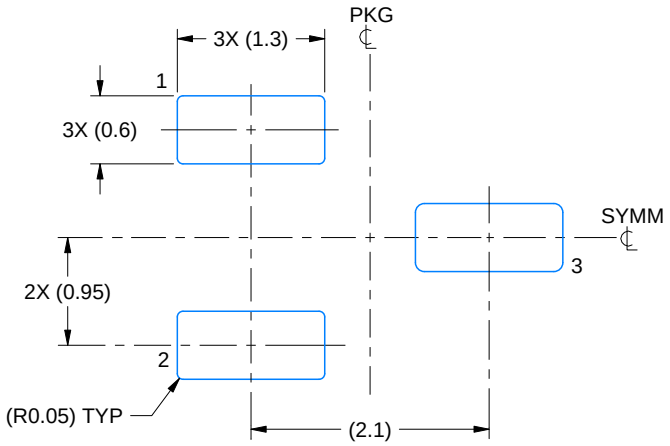
SMALL OUTLINE TRANSISTOR



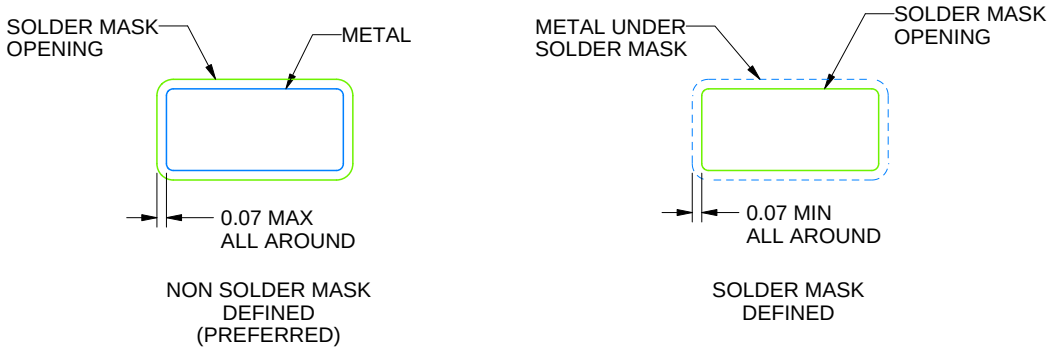
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

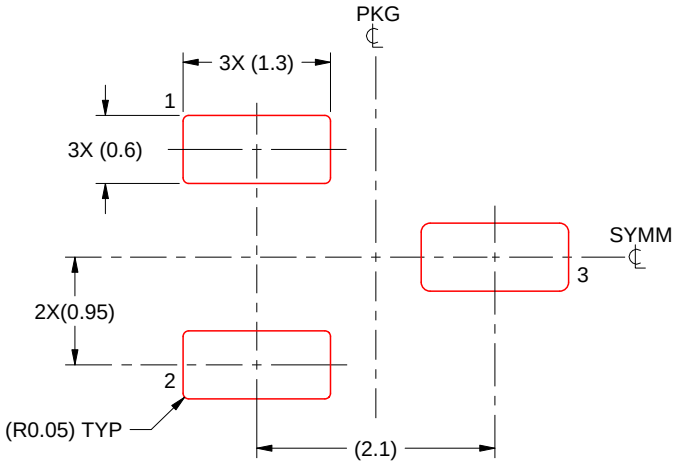


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月