TPD4E001 高速データ インターフェイス用の低容量、4 チャネル ESD 保護

1 特長

- IEC 61000-4-2 ESD 保護 (レベル 4)
  - 接触放電:±8kV
  - 空中放電:±15kV
- 5.5A ピーク パルス電流 (8/20µs のパルス)
- IO 容量 1.5pF (標準値)
- 低リーク電流:1nA (最大値)
- 低消費電流:1nA
- 0.9V ～ 5.5V の動作電源電圧範囲
- 省スペースの DRL、DBV、DCK、DPK、DRS パッケージ オプション
- 2、3、6 チャネルの代替オプションを利用可能:
  TPD2E001、TPD3E001、TPD6E001

2 アプリケーション

- USB 2.0
- イーサネット
- FireWire™ シリアル バス
- LVDS
- SVGA ビデオ接続
- 血糖値測定器

3 概要

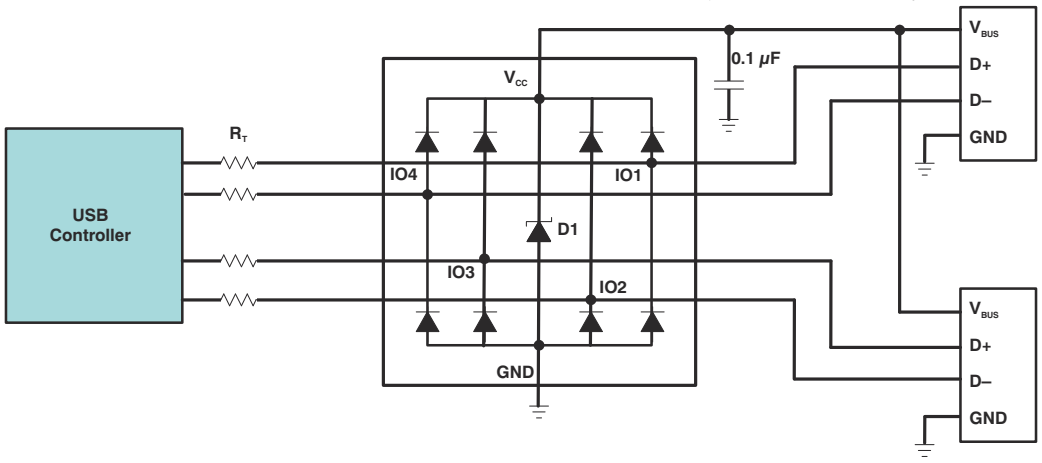
TPD4E001 は、静電放電(ESD)保護ダイオード アレイをベースとする、4 チャネルの過渡電圧サプレッサ(TVS)です。TPD4E001 は、IEC 61000-4-2 国際規格で規定されている最大レベル(レベル 4)の ESD 耐性を備えています。このデバイスにはチャネルごとに 1.5pF IO の容量があり、高速データ IO インターフェイスでの使用に理想的です。リーク電流が非常に低いため (最大値 1nA 未満)、血糖値計や心拍数モニタなどのアプリケーションでの高精度アナログ測定に適しています。

TPD4E001 は DRL (SOT)、DBV (SOT-23)、DCK (SC-70)、DRS (QFN)、DPK (PUSON) パッケージで供給され、–40°C ～ 85°C までの動作が規定されています。PD4E1U06DCKR および TPD4E1U06DBVR も参照してください。これらは、TPD4E001DCKR および TPD4E001DBVR のピン互換品です。これらのデバイスは IEC 保護がより高く、容量が低く、クランピング電圧が低いため、入力コンデンサが必要ありません。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPD4E001	SOT (6)	1.60mm × 1.20mm
		2.90mm × 1.60mm
	SC70 (6)	2.00mm × 1.25mm
	USON (6)	1.60mm × 1.60mm
	SON (6)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



アプリケーション回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
Pin Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings—JEDEC Specification ... 4
5.3 ESD Ratings—IEC Specification ... 4
5.4 Recommended Operating Conditions ... 4
5.5 Thermal Information ... 5
5.6 Electrical Characteristics ... 5
5.7 Typical Characteristics ... 6
6 Detailed Description ... 7
6.1 Overview ... 7
6.2 Functional Block Diagram ... 7
6.3 Feature Description ... 7
6.4 Device Functional Modes ... 7
7 Application and Implementation ... 8
7.1 Application Information ... 8
7.2 Typical Application ... 8
8 Layout ... 9
8.1 Layout Guidelines ... 9
8.2 Layout Example ... 10
9 Device and Documentation Support ... 11
9.1 サード・パーティ製品に関する免責事項 ... 11
9.2 Documentation Support ... 11
9.3 Receiving Notification of Documentation Updates ... 11
9.4 サポート・リソース ... 11
9.5 Trademarks ... 11
9.6 静電気放電に関する注意事項 ... 11
9.7 用語集 ... 11
10 Revision History ... 11
11 Mechanical, Packaging, and Orderable Information ... 13

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4 Pin Configuration and Functions

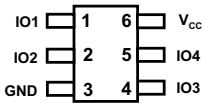


図 4-1. DRL Package 6-Pin SOT Top View

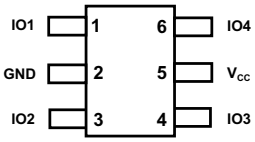


図 4-2. DBV or DCK Package 6-Pin SOT or SC70 Top View

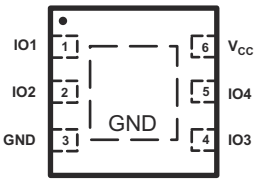


図 4-3. DRS Package 6-Pin SON Top View

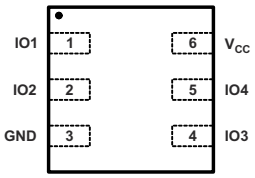


図 4-4. DPK Package 6-Pin USON Top View

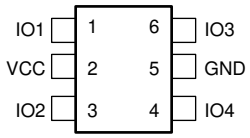


図 4-5. TPD4E001R DBV Package 6-Pin SOT Top View

Pin Functions

PIN				I/O	DESCRIPTION
NAME	DRS, DRL, DPK	DBV, DCK	TPD4E001R		
GND	3	2	5	—	Ground
IOx	1	1	1	I	ESD-protected channel
	2	3	3		
	4	4	4		
	5	6	6		
V_{CC}	6	5	2	I	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor
Exposed thermal pad (DRS package only)				—	Exposed thermal pad. Connect to GND or leave floating

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
$V_{I/O}$	IO voltage tolerance		–0.3	V_{CC} + 0.3	V
$I_{(Surge)}$	IEC 61000-4-5 peak pulse current (T_P = 8/20µs), IOx pins			5.5	A
$P_{(Surge)}$	IEC 61000-4-5 peak pulse power (T_P = 8/20µs), IOx pins			100	W
T_J	Junction temperature			150	°C
	Bump temperature (soldering)	Infrared (15s)		220	°C
		Vapor phase (60s)		215	
	Lead temperature (soldering, 10s)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings—JEDEC Specification

				VALUE	UNIT
TPD4E001 in DRS, DRL, and DPK Packages					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 1, 2, 4, and 5	±2000	V
			Pins 1, 2, 4, and 5	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1000	
TPD4E001 in DBV and DCK Packages					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 1, 3, 4, and 6	±2000	V
			Pins 1, 3, 4, and 6	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

				VALUE	UNIT
TPD4E001 in DRS, DRL, and DPK Packages					
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	All pins	±8000	V
		IEC 61000-4-2 air-gap discharge	All pins	±15000	
TPD4E001 in DBV and DCK Packages					
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	All pins	±8000	V
		IEC 61000-4-2 air-gap discharge	All pins	±15000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_A	Operating free-air temperature		–40	85	°C
	Operating voltage	V_{CC} pin	0.9	5.5	V
		IO1, IO2 pins	0	V_{CC}	

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5.5 Thermal Information

THERMAL METRIC[1]		TPD4E001					UNIT
		DRL (SOT)	DBV (SOT)	DCK (SC70)	DPK (USON)	DRS (SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226.4	259.7	251.1	247.6	91.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.3	186.5	88.1	124.8	106.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.2	107.6	54.8	204.2	64.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.7	71.4	1.7	19.2	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61	107.1	54.1	209.3	64.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	29.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted), V_{CC} = 5 V ± 10%

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	I_F = 10mA		0.65		0.95	V
V_{BR}	Breakdown Voltage	I_{BR} = 10mA		11			V
V_C	Channel clamp voltage	T_A = 25°C, ±15kV HBM, I_F = 10A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	
		T_A = 25°C, ±8kV contact discharge (IEC 61000-4-2), I_F = 24A	Positive transients			V_{CC} + 60	
			Negative transients			–60	
		T_A = 25°C, ±15kV air-gap discharge (IEC 61000-4-2), I_F = 45A	Positive transients			V_{CC} + 100	
			Negative transients			–100	
		Surge strike on IO pin, GND pin grounded, I_{PP} = 5A, 8/20µs[2]	Positive transients		17		
V_{RWM}	Reverse stand-off voltage	IO pin to GND pin				5.5	V
$I_{I/O}$	Channel leakage current	$V_{i/o}$ = GND to V_{CC}				±1	nA
$C_{I/O}$	Channel input capacitance	V_{CC} = 5V, bias of V_{CC}/2; f = 10MHz			1.5		pF

(1) Typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Non-repetitive current pulse 8/20µs exponentially decaying waveform according to ICE61000-4-5.

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5.7 Typical Characteristics

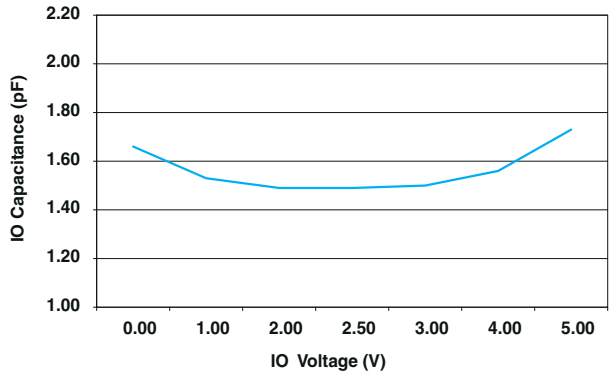


図 5-1. IO Capacitance vs IO Voltage (V_{CC} = 5V)

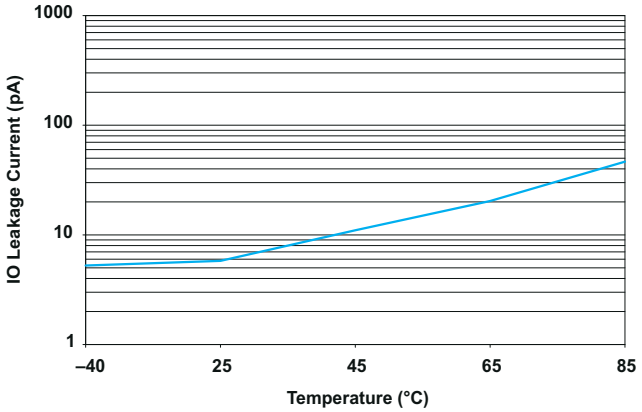


図 5-2. IO Leakage Current vs Temperature (V_{CC} = 5.5V)

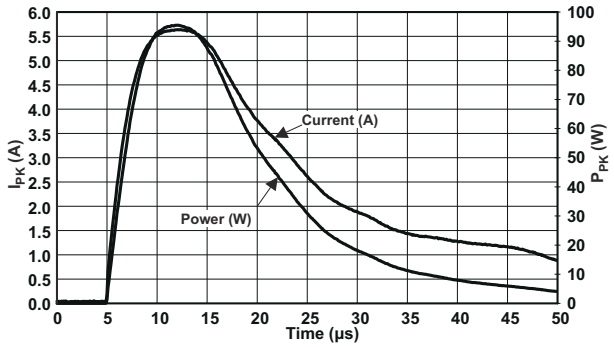


図 5-3. Peak Pulse Waveform, V_{CC} = 5.5V

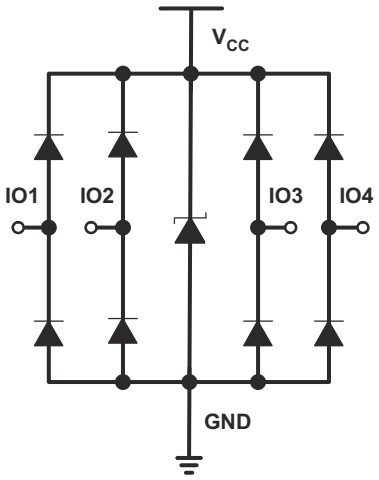
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6 Detailed Description

6.1 Overview

The TPD4E001 is a four-channel transient voltage suppressor (TVS) based ESD protection diode array. The TPD4E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra-low leakage current (<1nA maximum) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

6.2 Functional Block Diagram



6.3 Feature Description

The TPD4E001 is a uni-directional ESD protection device with low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to V_{CC} to provide protection for the V_{CC} line. Each IO line is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard. The TPD4E001's low loading capacitance makes it ideal for protection high-speed signal terminals.

6.4 Device Functional Modes

The TPD4E001 is a passive-integrated circuit that activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±15kV can be directed to ground and V_{CC} via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD4E001 (usually within 10s of nano-seconds) the device reverts back to a high-impedance state.

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7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TPD4E001 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

7.2 Typical Application

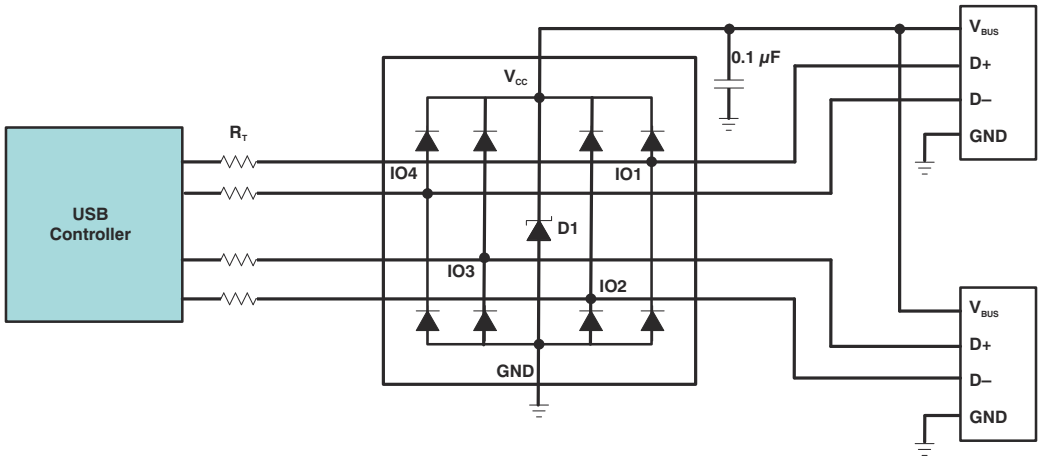


図 7-1. Typical Application Schematic

7.2.1 Design Requirements

For this design example, a single TPD4E001 is used to protect all the pins of two USB2.0 connectors.

Given the USB application, the following parameters in 表 7-1 are known.

表 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, and IO4	0V to 3.6V
Signal voltage range on V_{CC}	0V to 5.25V
Operating Frequency	240MHz

7.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD4E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD4E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines must be followed:

1. Place the TPD4E001 solution close to the connectors. This allows the TPD4E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.

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2. Place a 0.1µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15A to 30A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting two USB ports, none of the IO pins are left unused.
5. The V_{CC} pin can be connected in two different ways:
   a. If the V_{CC} pin is connected to the system power supply, the TPD4E001 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1µF capacitor on the device V_{CC} pin is recommended for ESD bypass.
   b. If the V_{CC} pin is not connected to the system power supply, the TPD4E001 can tolerate higher signal swing in the range up to 10V. Please note that a 0.1µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

7.2.3 Application Curve

図 7-2 is a capture of the voltage clamping waveform of TPD4E001DRL on IO3 during an 8kV Contact IEC61000-4-2 ESD strike.

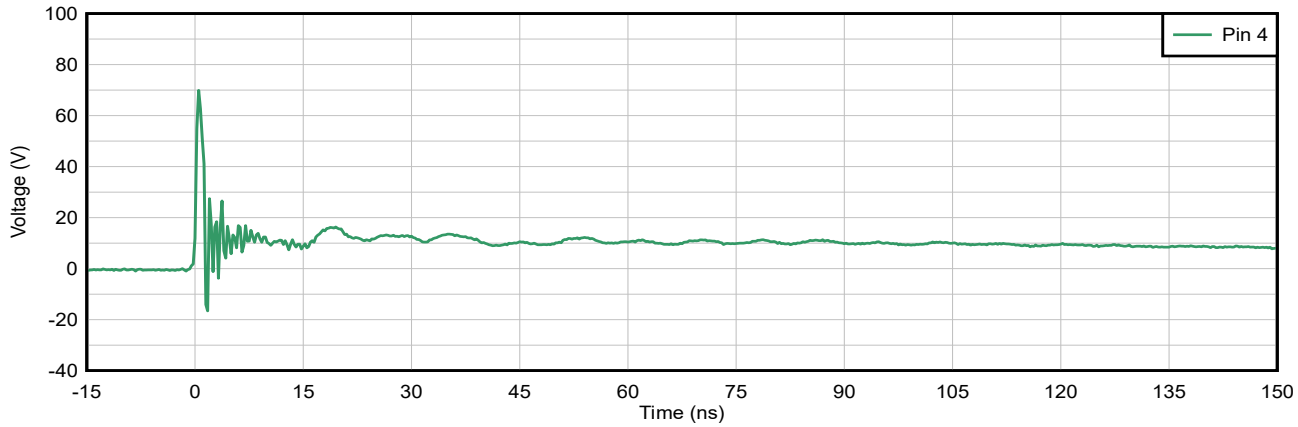


図 7-2. TPD4E001DRL IEC61000-4-2 Voltage Clamp Waveform 8kV Contact

Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Take care to make sure that the maximum voltage specifications for each pin are not violated.

8 Layout

8.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

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8.2 Layout Example

The following is a layout example for protecting two interface ports with the TPD4E001. One example is two USB 2.0 ports, as was discussed in the *セクション 7* section. For the USB 2.0 example, IO1 and IO2 is D+ and D–, respectively, of USB port 1. IO3 and IO4 is D– and D+, respectively, of USB port 2.

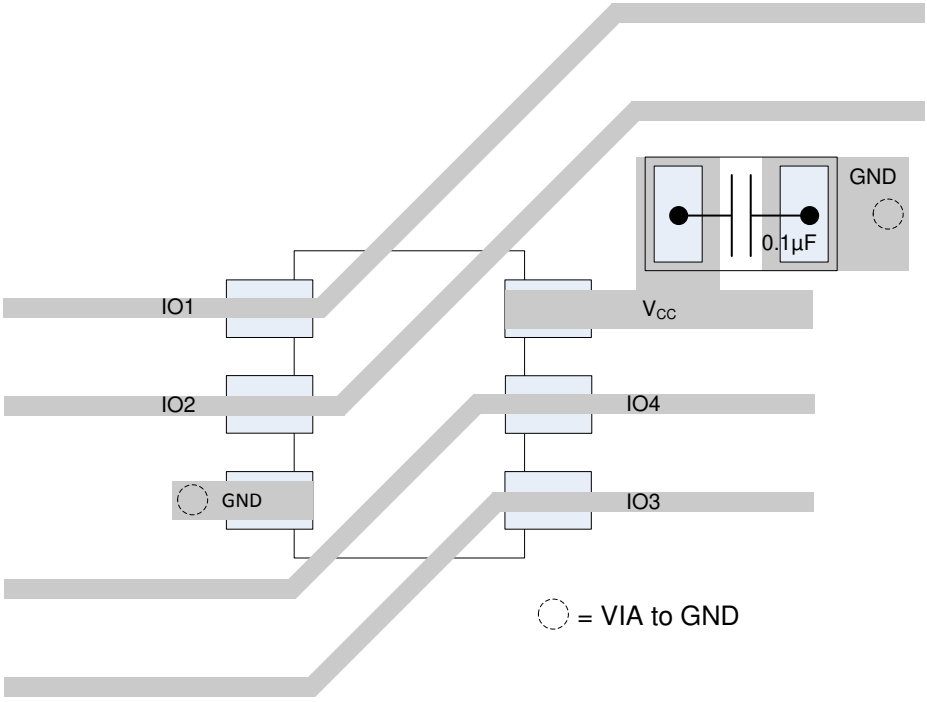


図 8-1. Routing With DRL Package

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9 Device and Documentation Support

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Datasheet*
- Texas Instruments, *ESD Layout Guide*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision O (July 2019) to Revision P (January 2025)	Page
• Removed DPK2 package from pin out drawings	3

Changes from Revision N (March 2018) to Revision O (July 2019)	Page
• Added TPD4E001R DBV Package image and updated Pin Funtions table	3

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Changes from Revision M (May 2017) to Revision N (March 2018) **Page**

- TPD4E001DBVR Device Marking changed from NFY to NFYF 13

Changes from Revision L (May 2016) to Revision M (May 2017) **Page**

- Updated Pin Functions table and DCK2 Package image..... 3
- Updated 'Surge Protection" to "IEC Specification" in *セクション 5.3* table..... 4

Changes from Revision K (January 2015) to Revision L (May 2016) **Page**

- Added frequency test condition to *Channel input capacitance* in the *Electrical Characteristics* table..... 5
- Added Community Resources 11

Changes from Revision J (December 2013) to Revision K (October 2014) **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1

Changes from Revision I (September 2012) to Revision J (November 2013) **Page**

- 「概要」を更新..... 1
- Removed Ordering Information table..... 3

Changes from Revision H (August 2012) to Revision I (September 2012) **Page**

- Added DCK2 package to pin out drawings..... 3
- Updated Electrical Characteristics table..... 5

Changes from Revision G (December 2011) to Revision H () **Page**

- Updated TOP-SIDE MARKING column in ORDERING INFORMATION table..... 3

Changes from Revision F (May 2011) to Revision G (December 2011) **Page**

- ドキュメントのフォーマットを更新..... 1
- Added DPK (PUSON) package and package information..... 3

Changes from Revision E (April 2011) to Revision F (May 2011) **Page**

- Added Peak Pulse Waveform Graph to Typical Operating Characteristics..... 6

Changes from Revision C (April 2007) to Revision D (December 2010) **Page**

- Added DBV (SOT-23) package and package information..... 3

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E001DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(NFY5, NFYF) (NFYP, NFYS)
TPD4E001DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(NFY5, NFYF) (NFYP, NFYS)
TPD4E001DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2CF, 2CR) (2CP, 2CP) 2CH
TPD4E001DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2CF, 2CR) (2CP, 2CP) 2CH
TPD4E001DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2CF 2CP
TPD4E001DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2CF 2CP
TPD4E001DPKR	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2C7
TPD4E001DPKR.B	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2C7
TPD4E001DPKRG4	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2C7
TPD4E001DPKRG4.B	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2C7
TPD4E001DPKT	Active	Production	USON (DPK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2C7
TPD4E001DPKT.B	Active	Production	USON (DPK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2C7
TPD4E001DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(2C7, 2CR) (2CG, 2CH)
TPD4E001DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2C7, 2CR) (2CG, 2CH)
TPD4E001DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2C7, 2CR) (2CG, 2CH)
TPD4E001DRSR	Active	Production	SON (DRS) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWM
TPD4E001DRSR.B	Active	Production	SON (DRS) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWM
TPD4E001DRSRG4	Active	Production	SON (DRS) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWM
TPD4E001DRSRG4.B	Active	Production	SON (DRS) | 6	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWM
TPD4E001RDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	NRYF
TPD4E001RDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NRYF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPD4E001 :

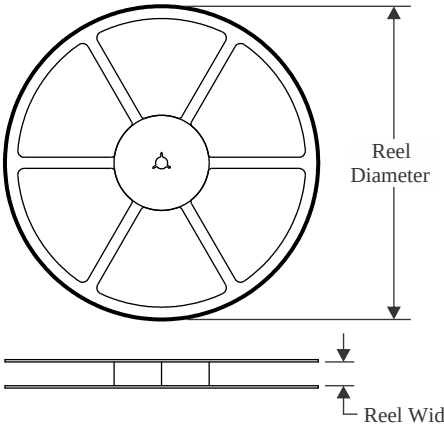
- Automotive : TPD4E001-Q1

NOTE: Qualified Version Definitions:

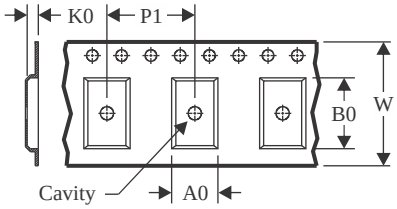
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

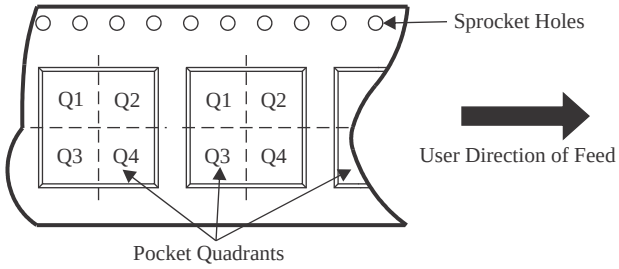


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

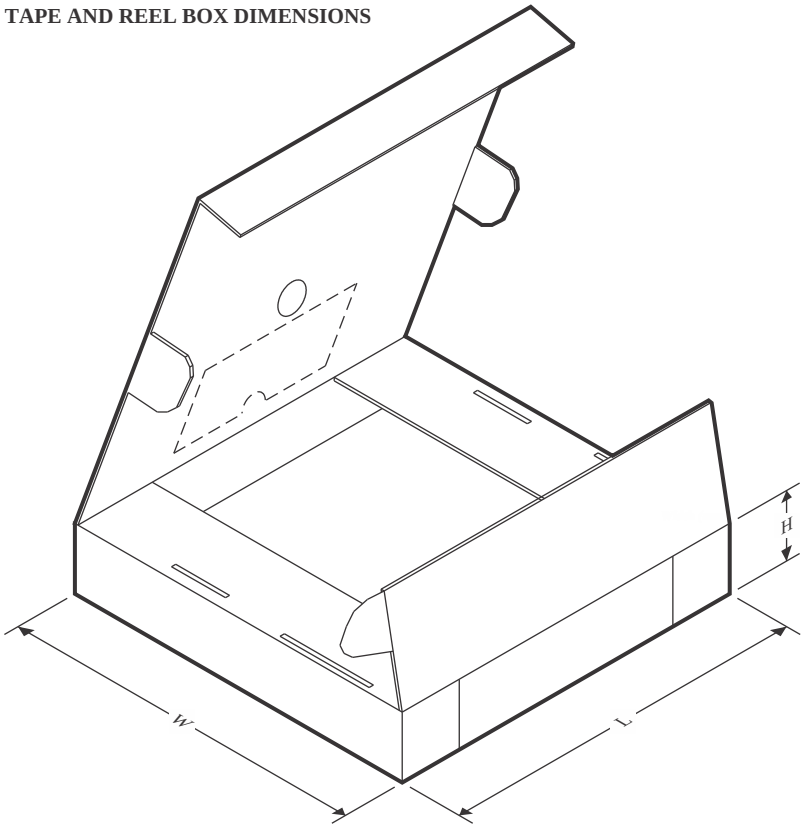
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E001DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPD4E001DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPD4E001DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPD4E001DPKR	USON	DPK	6	5000	180.0	9.5	1.75	1.75	0.7	4.0	8.0	Q2
TPD4E001DPKRG4	USON	DPK	6	5000	180.0	9.5	1.75	1.75	0.7	4.0	8.0	Q2
TPD4E001DPKT	USON	DPK	6	250	180.0	9.5	1.75	1.75	0.7	4.0	8.0	Q2
TPD4E001DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPD4E001DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TPD4E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD4E001DRSRG4	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD4E001RDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

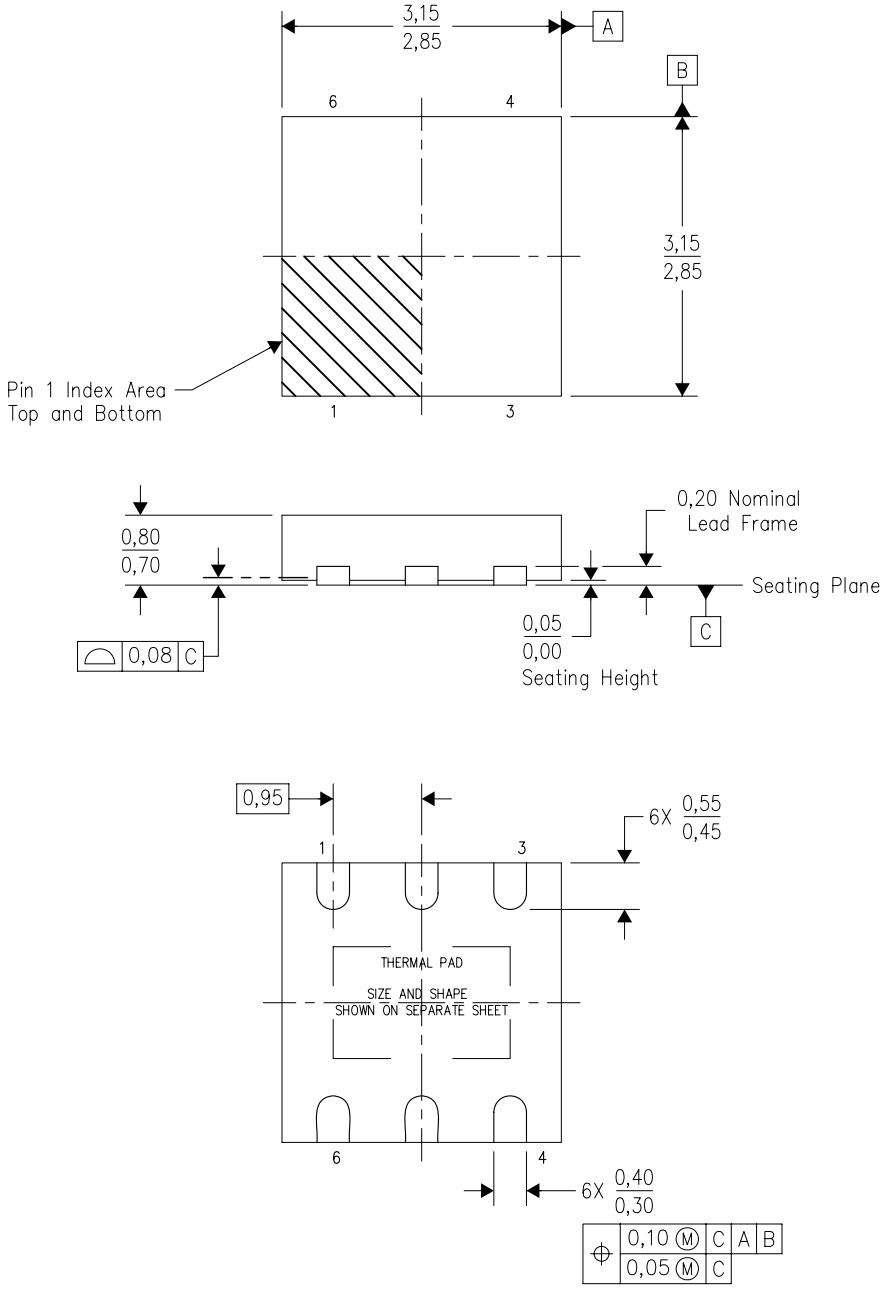
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E001DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
TPD4E001DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TPD4E001DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
TPD4E001DPKR	USON	DPK	6	5000	184.0	184.0	19.0
TPD4E001DPKRG4	USON	DPK	6	5000	184.0	184.0	19.0
TPD4E001DPKT	USON	DPK	6	250	184.0	184.0	19.0
TPD4E001DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPD4E001DRLR	SOT-5X3	DRL	6	4000	183.0	183.0	20.0
TPD4E001DRSR	SON	DRS	6	1000	353.0	353.0	32.0
TPD4E001DRSRG4	SON	DRS	6	1000	353.0	353.0	32.0
TPD4E001RDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206219/F 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

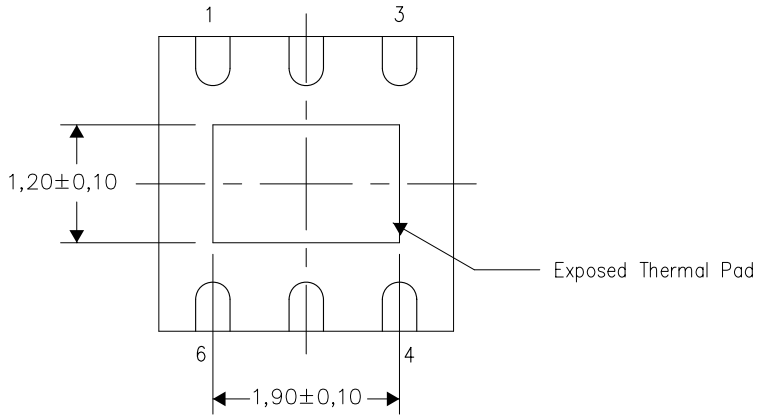
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



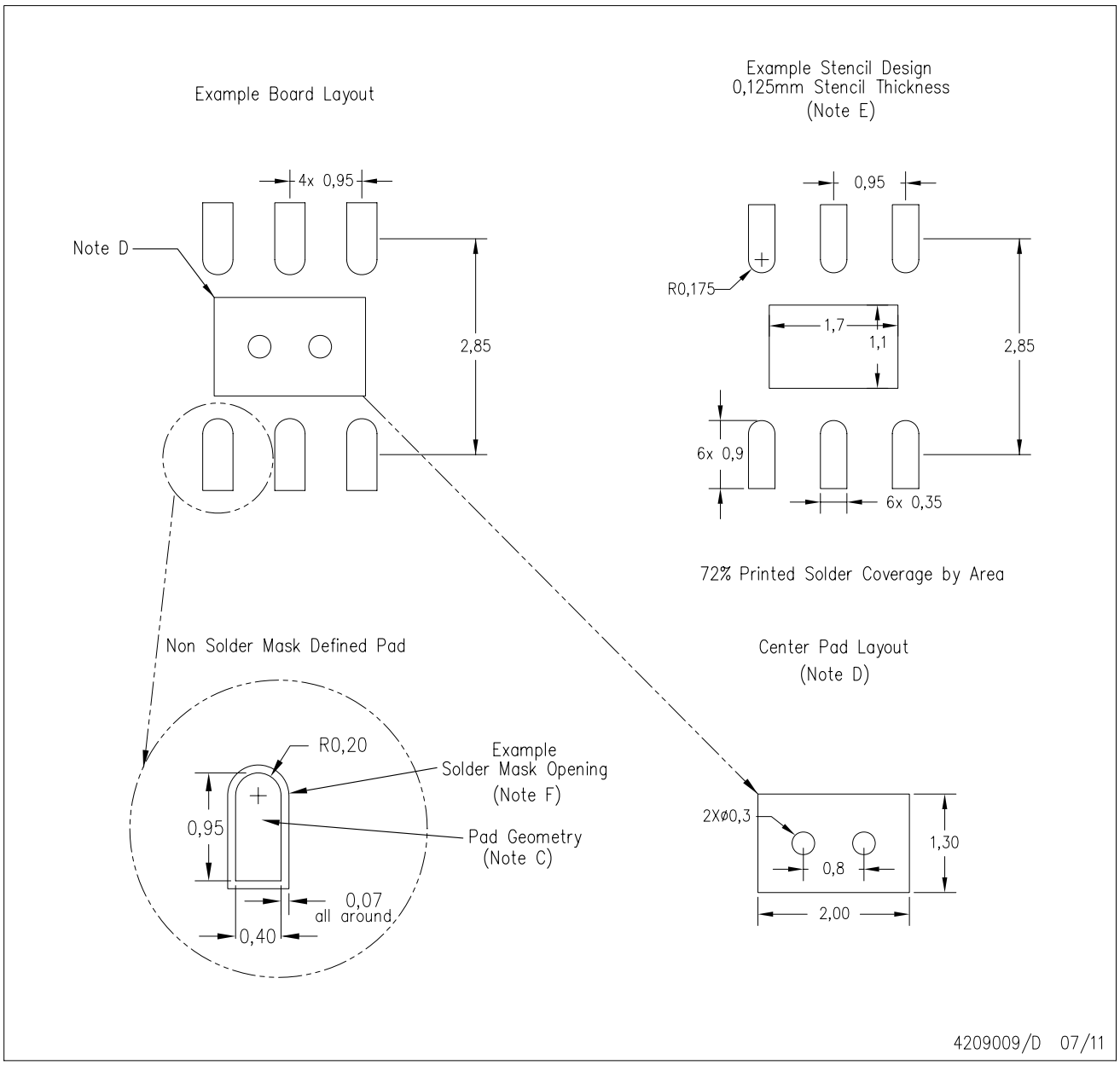
Bottom View

Exposed Thermal Pad Dimensions

4207663/E 07/11

NOTE: All linear dimensions are in millimeters

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

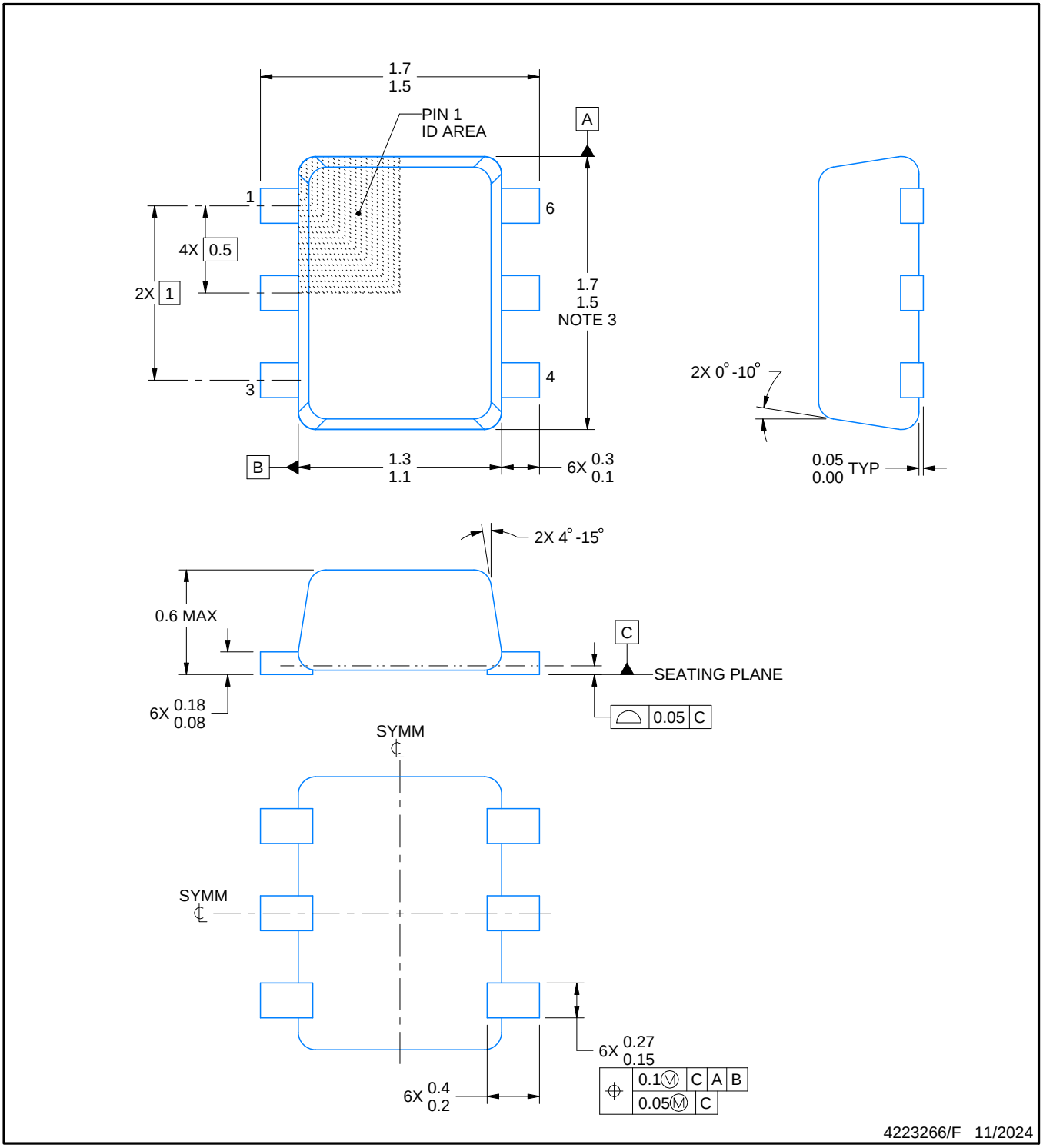


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

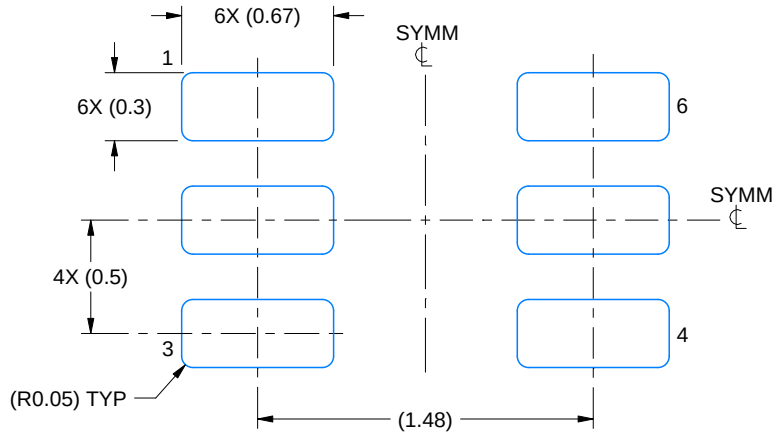
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

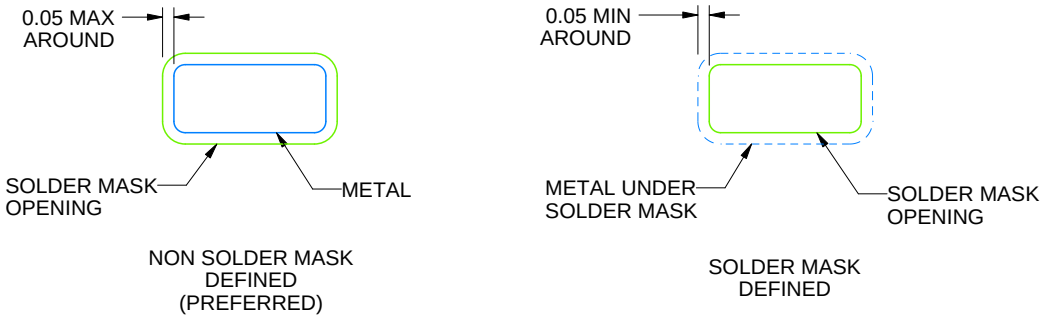
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

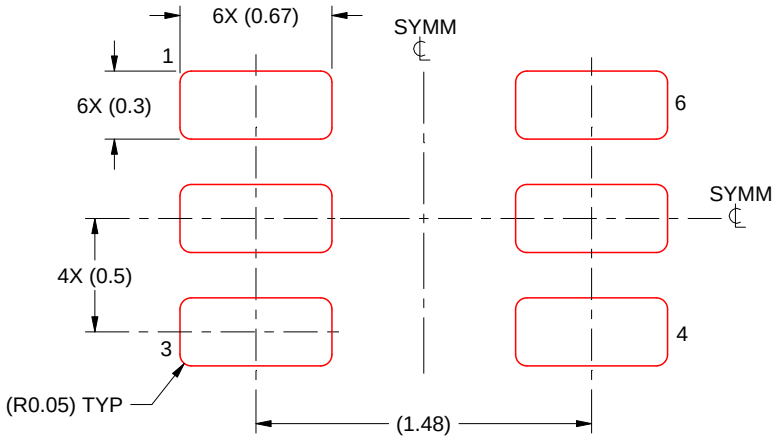
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

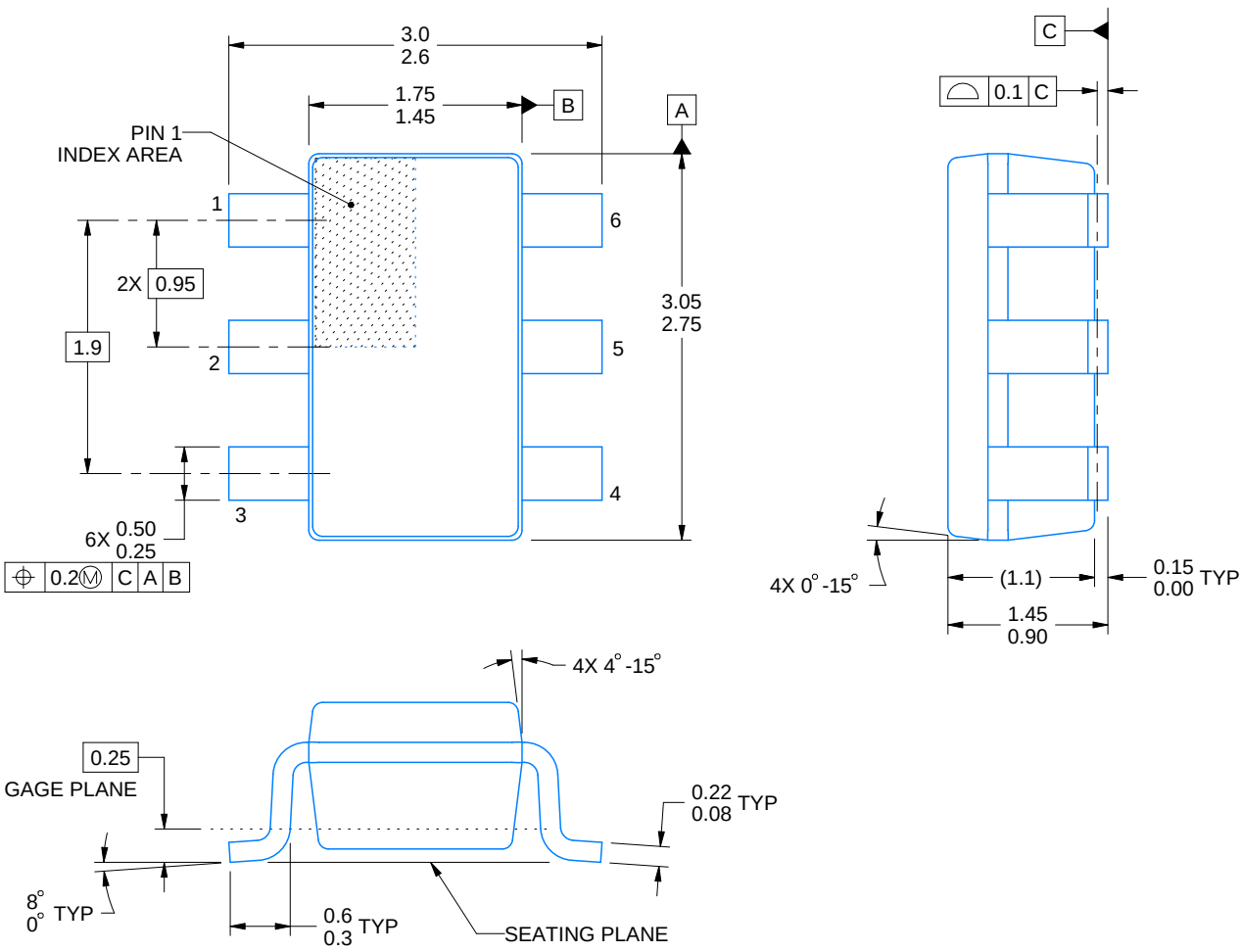
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

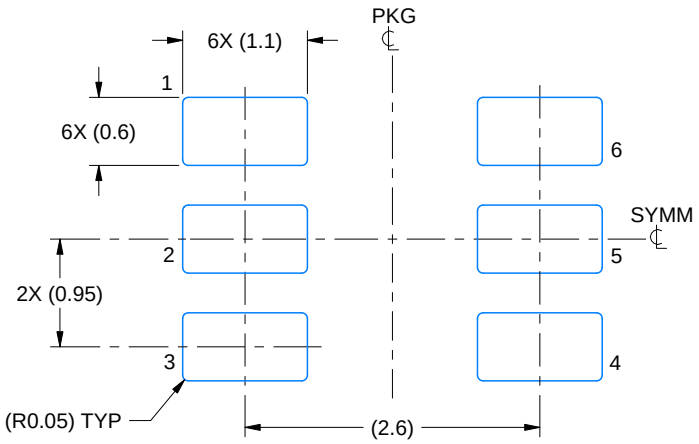
SMALL OUTLINE TRANSISTOR



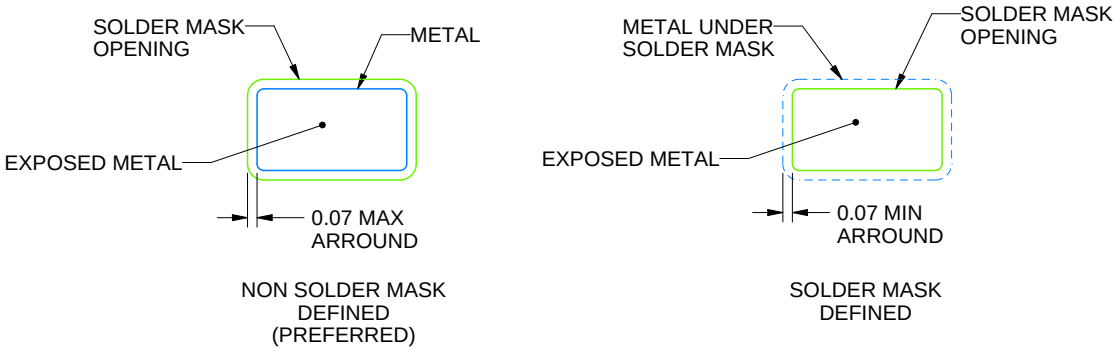
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

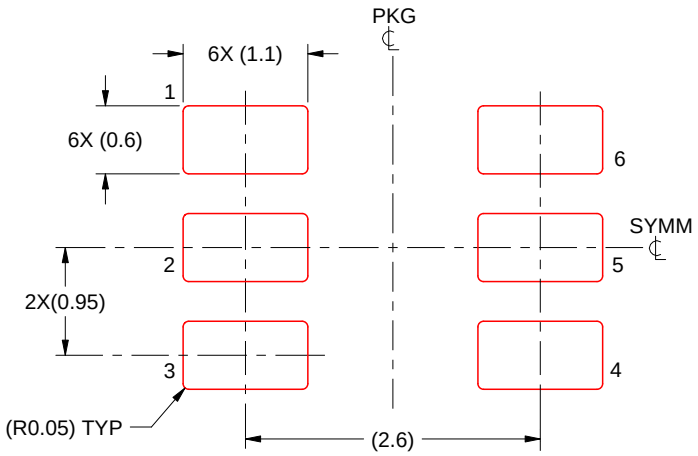


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



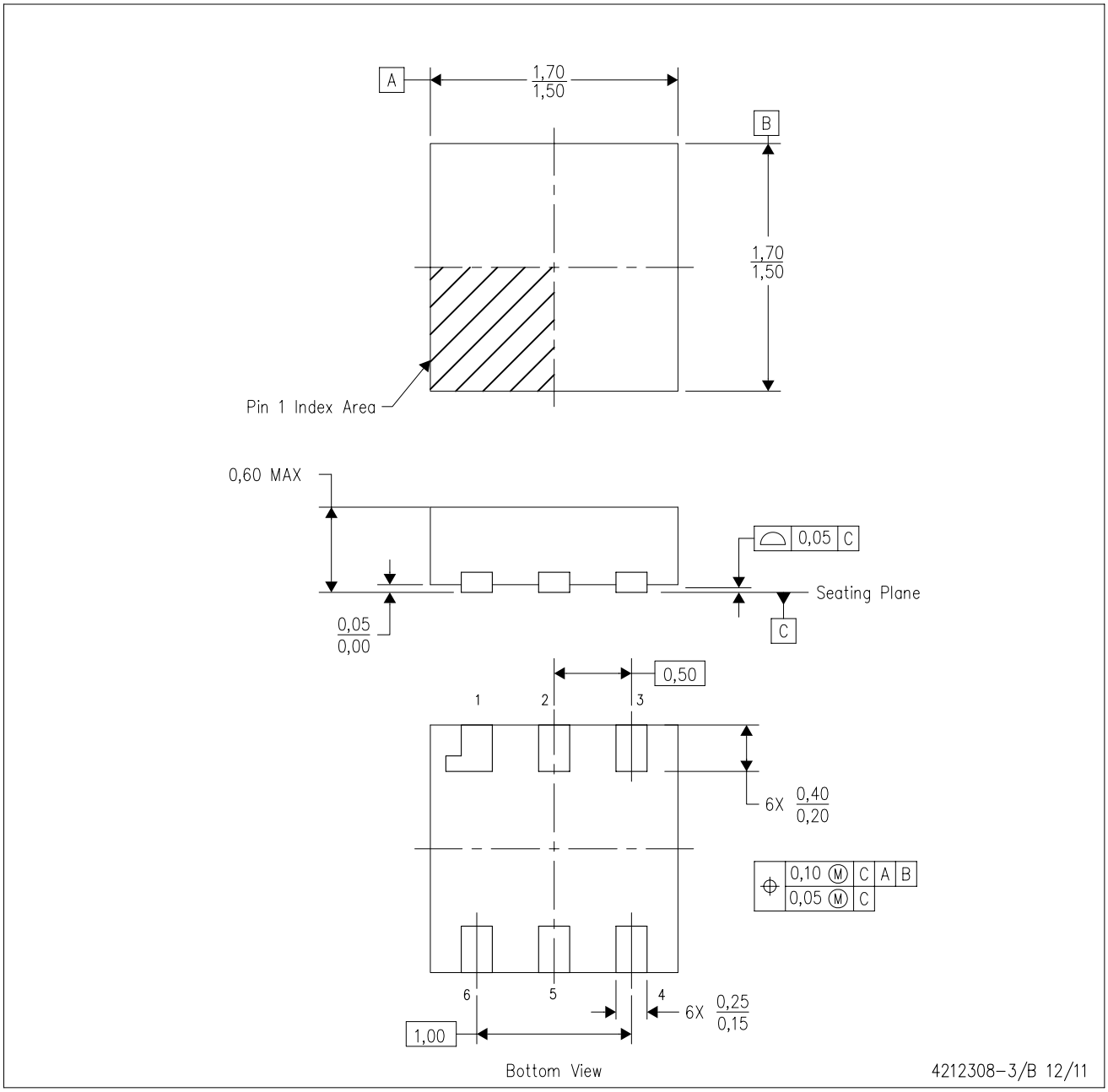
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

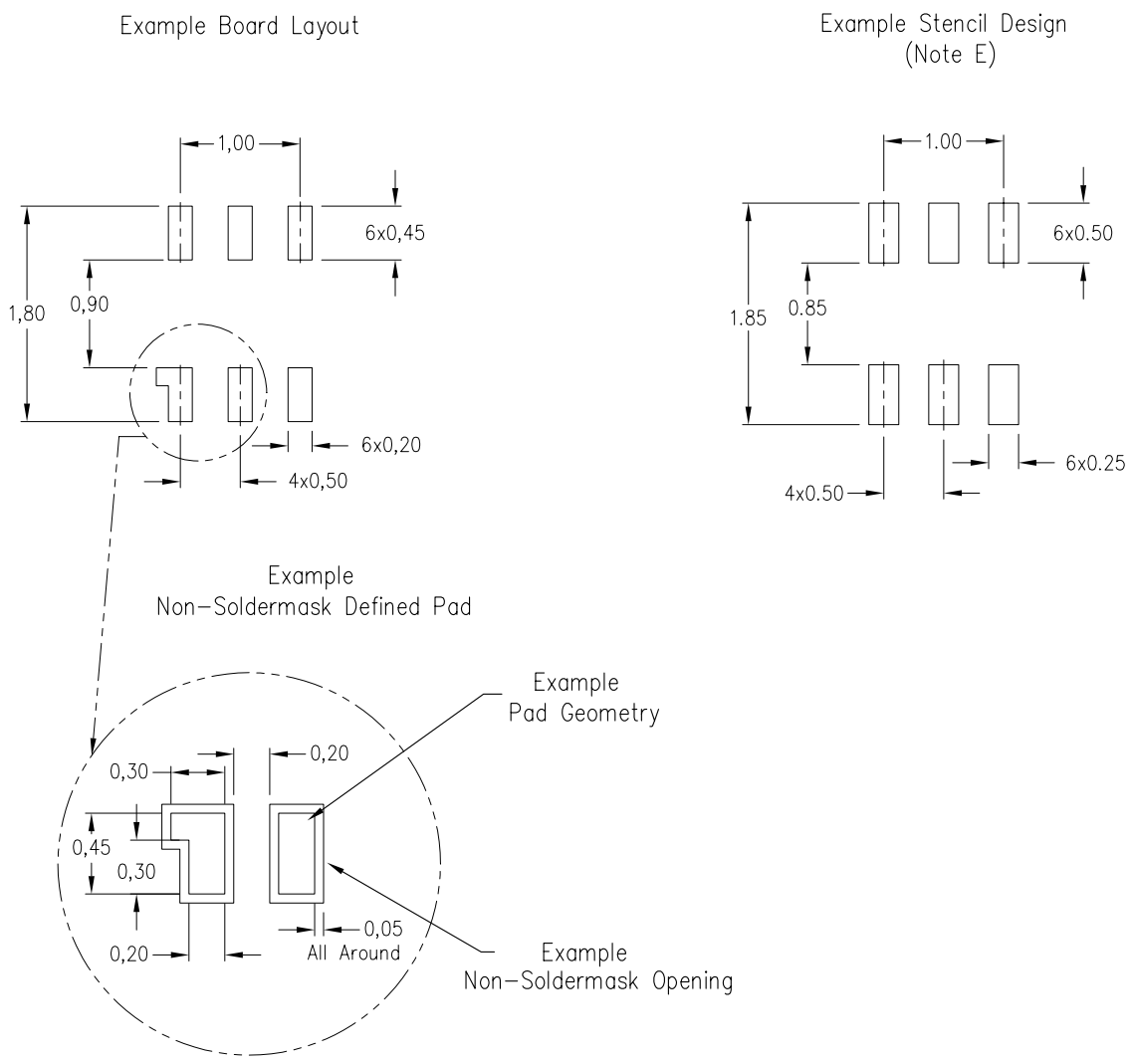
DPK (S–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

DPK (S–PUSON–N6)

PLASTIC SMALL OUTLINE NO–LEAD



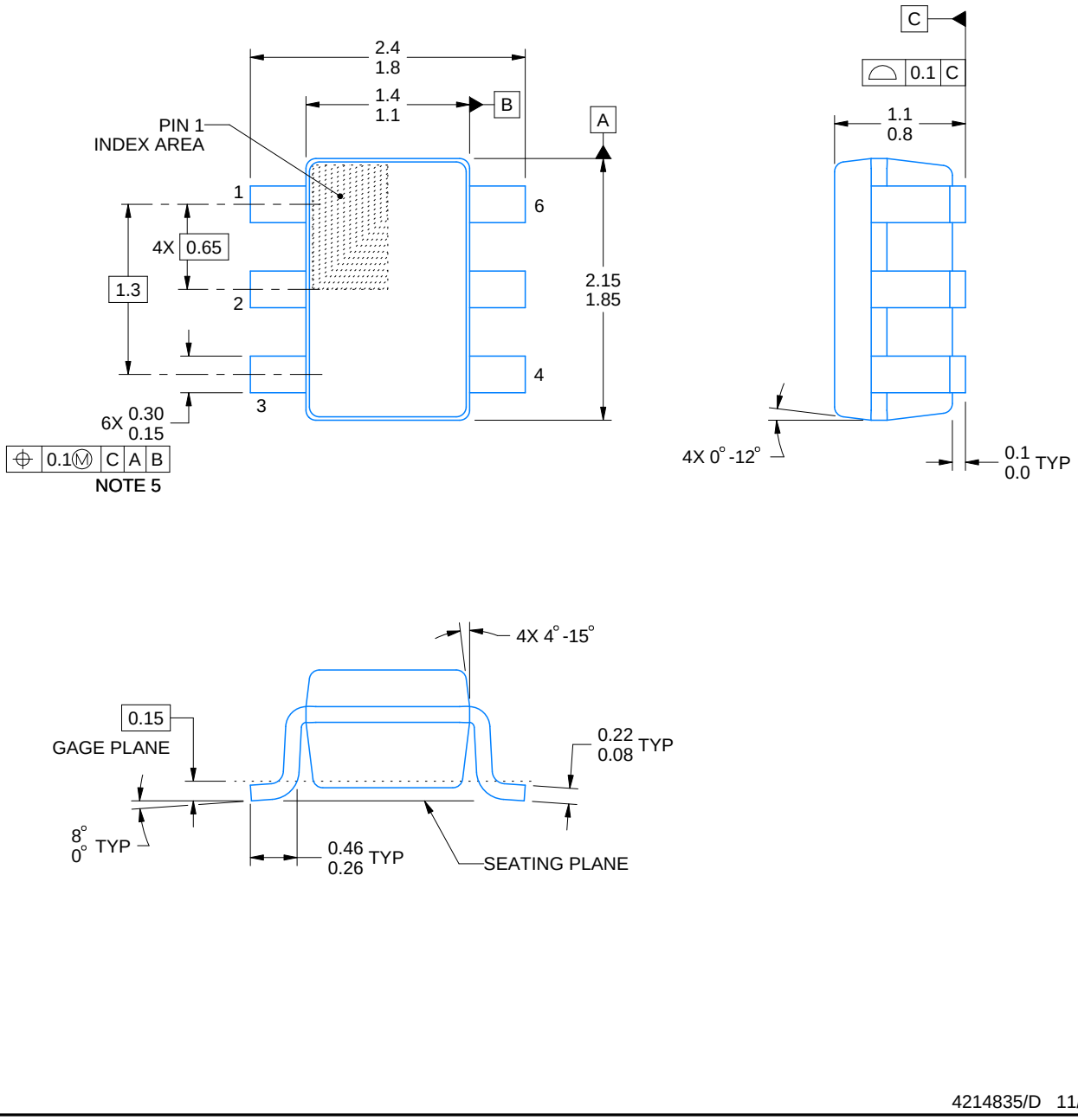
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

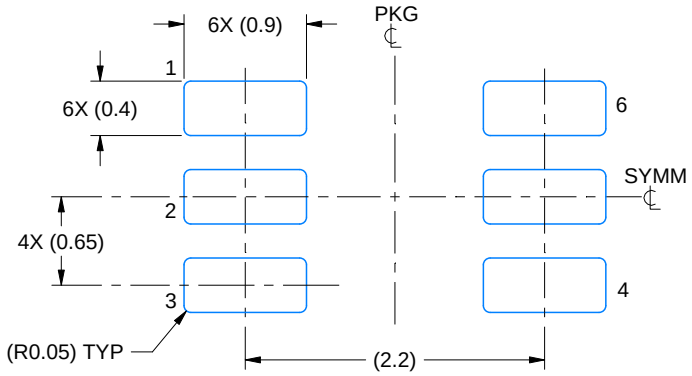
SMALL OUTLINE TRANSISTOR



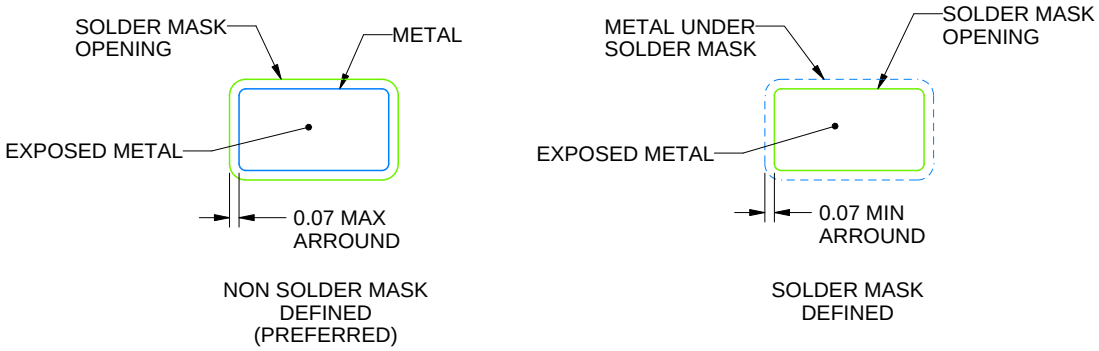
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

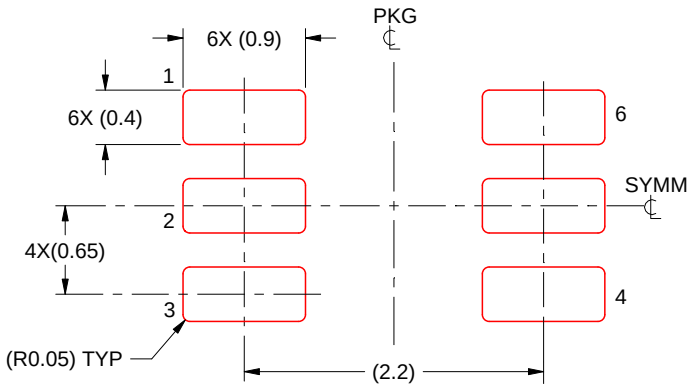


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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