TEXAS INSTRUMENTS

TPD4E004
JAJSQR8C – FEBRUARY 2008 – REVISED JULY 2023

TPD4E004 4 チャネル ESD 保護アレイ、高速データ・インターフェイス用

1 特長

- IEC 61000-4-2 ESD 保護：
  - ±8kV IEC 61000-4-2 接触放電
  - ±12kV IEC 61000-4-2 エアギャップ放電
- ANSI/ESDA/JEDEC JS-001：
  - ±15kV 人体モデル (HBM)
- 1.6pF の低入力静電容量
- 0.9V～5.5V の動作電源電圧範囲
- 4 チャネル・デバイス
- 省スペースの SON (DRY) パッケージ

2 アプリケーション

- USB
- イーサネット
- FireWire™
- ビデオ
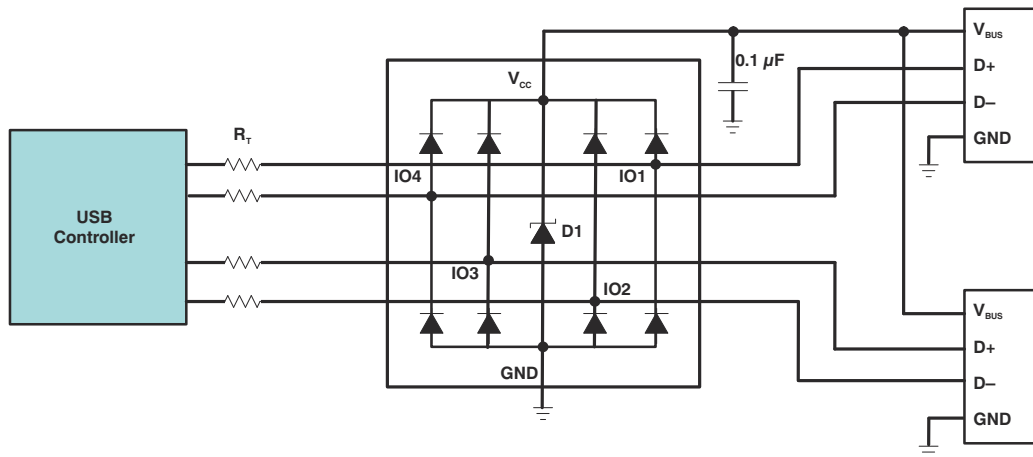- 携帯電話
- SVGA ビデオ接続
- 血糖値計

3 概要

TPD4E004 は低静電容量の過渡電圧抑制 (TVS) デバイスです。TPD4E004 は、通信ラインに接続された高感度電子機器を静電気放電 (ESD) から保護するように設計されています。4 つのチャネルはそれぞれ 1 対のダイオードで構成され、ESD 電流パルスを V_{CC} または GND に制御します。TPD4E004 は、最大 ±15kV の人体モデル (HBM) の ESD パルスから保護し、IEC 61000-4-2 で規定されている ±8kV の接触放電と ±12kV のエアギャップ放電から保護します。このデバイスにはチャネルごとに 1.6pF の容量があり、高速データ IO インターフェイスでの使用に理想的です。

TPD4E004 は、USB、イーサネット™、その他の高速アプリケーション用に設計されたクワッド ESD 構造です。

パッケージ情報

部品番号	パッケージ[1]	パッケージ・サイズ[2]
TPD4E004	DRY (SON、6)	1.45mm × 1mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

アプリケーション回路図

English Data Sheet: SLVS729

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (March 2016) to Revision C (July 2023)	Page
• パッケージ・サイズを含めるよう「パッケージ情報」表を更新	1
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Updated the *Overview* section to include IEC 61000-4-2 international standard Level 3	7

Changes from Revision A (February 2008) to Revision B (March 2016)	Page
• 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 注文情報を削除	1

Product Folder Links: *TPD4E004*

English Data Sheet: SLVS729

5 Pin Configuration and Functions
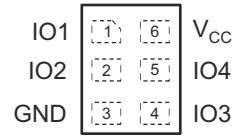
図 5-1. DRY Package, 6-Pin SON (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO1	1	IO	ESD-protected channel
IO2	2	IO	ESD-protected channel
GND	3	GND	Ground
IO3	4	IO	ESD-protected channel
IO4	5	IO	ESD-protected channel
V_{CC}	6	PWR	Power-supply input

(1)   I = input, O = outputs, GND = ground, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.3	5.5	V
V_{IO}	Input/output voltage		−0.3	V_{CC} + 0.3	V
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±15000	V
		IEC 61000-4-2	Contact Discharge	±8000	
			Air-Gap Discharge	±12000	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	−40	85	°C
V_{CC}	Operating voltage for pin V_{CC}	0.9	5.5	V
V_{IO}	Operating voltage for pins IO1, IO2, IO3, and IO4	0	Minimum of: (5.8, V_{CC})	V

6.4 Thermal Information

THERMAL METRIC[1]		TPD4E004 DRY (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	414.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	258.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	251.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	248.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 0.9 V to 5.5 V, T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{CC}	Supply voltage		0.9		5.5	V
I_{CC}	Supply current				500	nA
V_F	Diode forward voltage	I_F = 1 mA		0.8		V
I_I	Channel leakage current			±1		nA
V_{BR}	Break-down voltage	I_I = 10 μA	6		8	V
$C_{I/O}$	Channel input capacitance	V_{CC} = 5 V, Bias of V_{CC}/2, f = 10 MHz		1.6	2	pF

(1)   Typical values are at V_{CC} = 5 V and T_A = 25°C.

Product Folder Links: TPD4E004
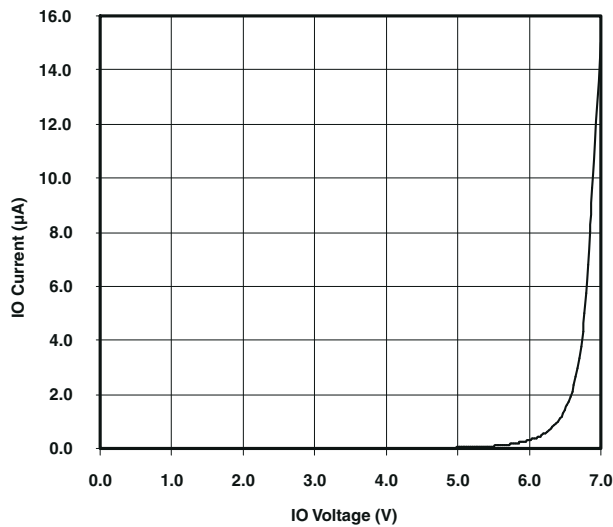
English Data Sheet: SLVS729

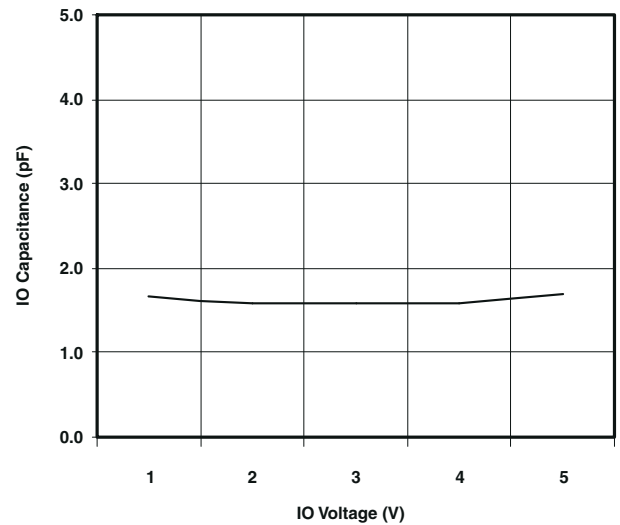## 6.6 Typical Characteristics
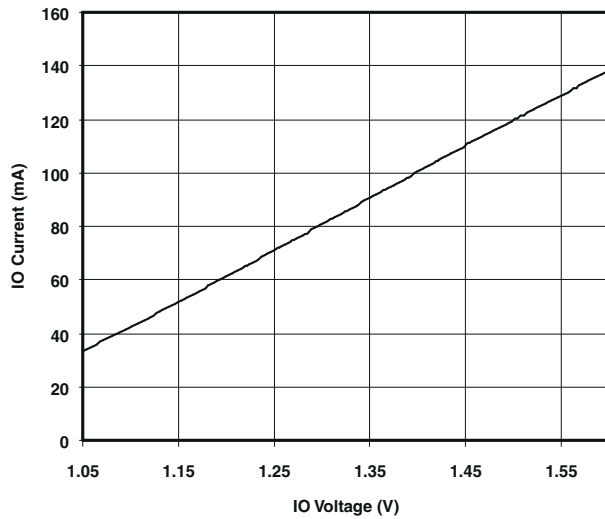
図 6-1. Forward Diode Voltage (Upper Clamp Diode) (V_{CC} = 0 V, DC Sweep Across the IO Pin)
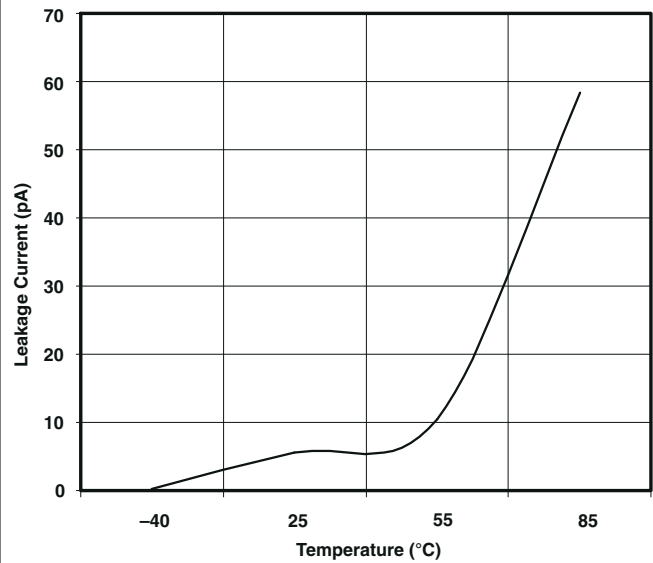
図 6-2. Leakage Current vs Temperature (V_{IO} = 2.5 V)

図 6-3. Reverse Diode Curve Current IO to GND (V_{CC} = Open)

図 6-4. IO Capacitance vs Input Voltage (V_{CC} = 5 V)

Product Folder Links: *TPD4E004*

English Data Sheet: SLVS729

7 Detailed Description

7.1 Overview

The TPD4E004 is a four-channel TVS protection diode array. The TPD4E004 is rated to dissipate contact ESD strikes of ±8-kV contact and ±12-kV air-gap, meeting Level 3 as specified in the IEC 61000-4-2 international standard. This device has a 1.6-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces.

7.2 Functional Block Diagram
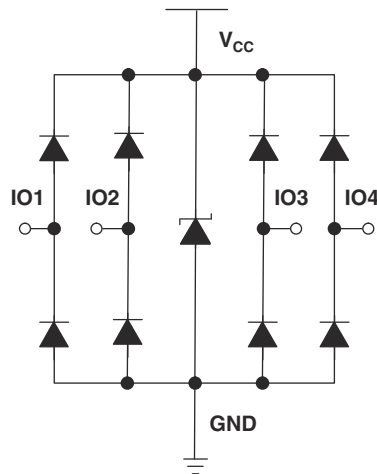
7.3 Feature Description

TPD4E004 is a TVS which provides ESD protection for up to four channels, withstanding up to ±8-kV contact and ±12-kV air-gap ESD per IEC 61000-4-2. The monolithic technology yields exceptionally small variations in capacitance between any IO pin of TPD4E004. The small footprint is ideal for applications where space-saving designs are important.

7.4 Device Functional Modes

The TPD4E004 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the diodes V_F of approximately –0.3 V. During ESD events, voltages as high as ±8-kV contact and ±12-kV air-gap ESD can be directed to ground through the internal diodes. Once the voltages on the protected line fall below the trigger levels of TPD4E004 (usually within 10's of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

TPD4E004 is a diode array type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level for the protected IC.

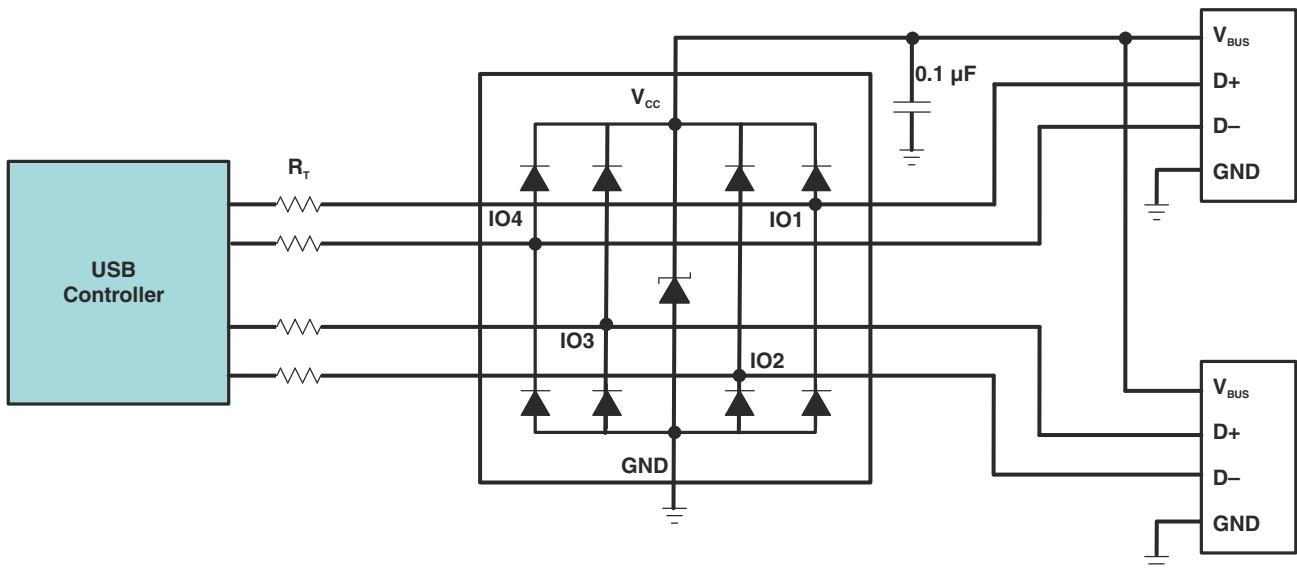## 8.2 Typical Application

図 8-1. Application Schematic

8.2.1 Design Requirements

For this design example, a single TPD4E004 is used to protect all the pins of two USB2.0 connectors. 表 8-1 lists the design parameters for the USB application.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, and IO4	0 V to 3.6 V
Signal voltage range on V_{CC}	0 V to 5.5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD4E004 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD4E004 is designed so that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, see the following layout and design guidelines should be followed:

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1. Place the TPD4E004 solution close to the connectors. This allows the TPD4E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E004 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15-A to 30-A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting two USB ports, none of the IO pins will be left unused.
5. The V_{CC} pin can be connected in two different ways:
    a. If the V_{CC} pin is connected to the system power supply, the TPD4E004 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD bypass.
    b. If the V_{CC} pin is not connected to the system power supply, the TPD4E004 can tolerate higher signal swing in the range up to 5.8 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curves

図 8-2 is a capture of the voltage clamping waveform of TPD4E004 during an +8-kV Contact IEC 61000-4-2 ESD strike.
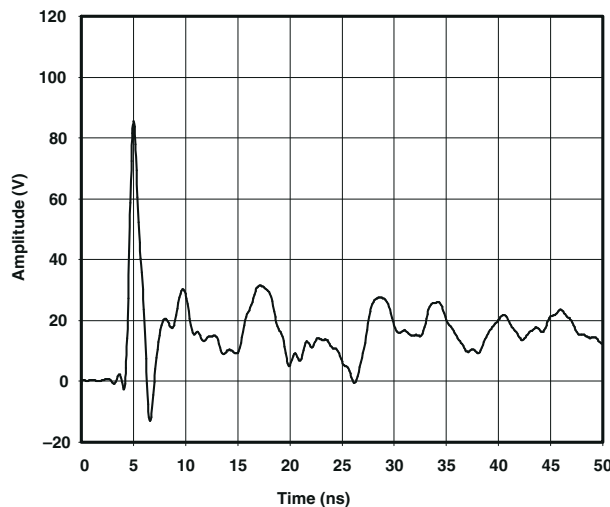
図 8-2. IEC ESD Clamping Waveforms +8-kV Contact
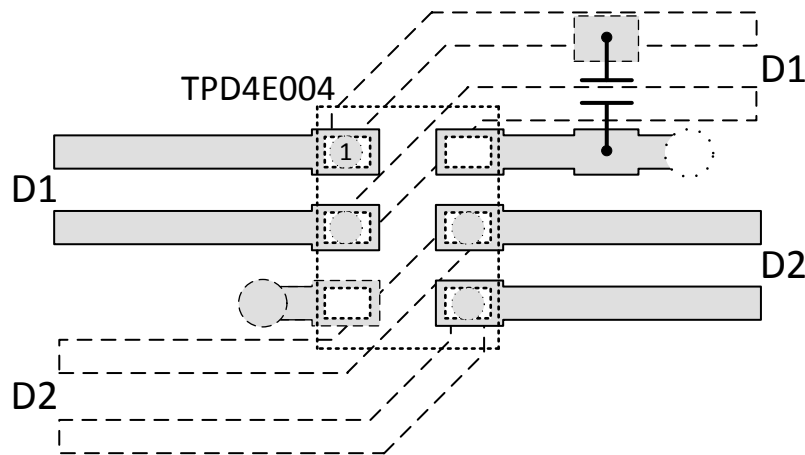
9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Make sure that the maximum voltage specifications for each pin are not violated.

Product Folder Links: *TPD4E004*

English Data Sheet: SLVS729

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

図 10-1. TPD4E004 Layout Example

Product Folder Links: *TPD4E004*

English Data Sheet: SLVS729

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*
- Texas Instruments, *ESD Protection Layout Guide*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E004DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P
TPD4E004DRYR.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P
TPD4E004DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P
TPD4E004DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E004DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E004DRYR	SON	DRY	6	5000	189.0	185.0	36.0

DRY 6

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

TEXAS
INSTRUMENTS

DRY0006A

PLASTIC SMALL OUTLINE - NO LEAD

B   1.05 / 0.95   A

PIN 1 INDEX AREA

1.5 / 1.4

0.6 MAX

C

0.05 / 0.00

SEATING PLANE

0.08 | C

3X 0.6

SYMM

(0.05) TYP

3   4

4X 0.5

2X 1

SYMM

1   6

0.4 / 0.3

6X 0.25 / 0.15

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ | C

PIN 1 ID (OPTIONAL)

5X 0.35 / 0.25

(0.127) TYP

4222894/A   01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM
℄

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM
℄

4X (0.5)

3

4

(R0.05) TYP

(0.6)

LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

0.05 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A   01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)

SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A   01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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