TPIC1021 LIN 物理インターフェイス

1 特長

- LIN 物理層仕様リビジョン 2.1 準拠は、LIN 用の SAEJ2602 推奨事例に準拠
- 最大 20kbps の LIN バス速度
- 12kV (人体モデル) までの ESD 保護 (LIN ピン)
- LIN ピンは、-40V～40V の電圧に対応
- 車載環境での過渡的なストレスに耐える (ISO 7637)
- 7V～27V DC の電源で動作
- 通常モードと低消費電力 (スリープ) モードの 2 つの動作モード
- 低消費電力モードにおける低消費電流
- LIN バス、ウェイクアップ入力 (外部スイッチ)、またはホスト MCU からウェークアップ可能
- 5V または 3.3V I/O ピンを使って MCU と接続
- TXD ピン上での支配的な状態タイムアウト保護
- RXD ピンでのウェイクアップ要求
- 外部電圧レギュレータの制御 (INH ピン)
- LIN レスポンダ・アプリケーション用プルアップ抵抗と直列ダイオードを内蔵
- 低 EME (電磁放射)、高 EMI (電磁耐性)
- バッテリへの短絡またはグランドへの短絡からバス端子を保護
- 過熱保護機能
- システム・レベルでのグランド切断のフェイルセーフ
- システム・レベルでのグランド・シフト動作
- 電力オフ・ノードはネットワークに不干渉

2 アプリケーション

- 産業用センシング
- 大型家電製品の分散制御

3 概要

TPIC1021 は LIN (Local Interconnect Network) 物理インターフェイスであり、このインターフェイスはウェイクアップおよび保護機能付きシリアル・トランシーバを内蔵しています。LIN バスとは、2.4kbps～20kbps の Baud レートを使った低速車内ネットワークで一般に使用されている単線式双方向バスです。

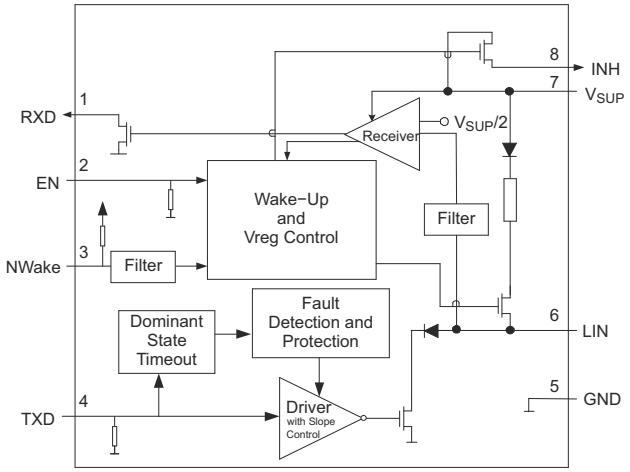
LIN バスには次の 2 つの論理値があります。支配的な状態 (グランドに近い電圧) は、ロジック 0 を表し、リセッシブ状態 (バッテリに近い電圧) は、ロジック 1 を表します。

リセッシブ状態では、LIN バスは TPIC1021 内部プルアップ抵抗 (30kΩ) と直列ダイオードによって High になるため、レスポンダ用途では外付けプルアップ部品は不要です。コマンダ用途では、外付けプルアップ抵抗 (1kΩ) と直列ダイオードが必要です。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPIC1021	SOIC (8)	4.90mm × 3.91mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

Changes from Revision D (June 2015) to Revision E (May 2022) **Page**

- 機能を以下のように変更:「...リビジョン 2.0 準拠」から「...リビジョン 2.1 準拠」へ ... 1
- 旧式の用語を使っている場合、すべてコマンダおよびレスポンダに変更 ... 1
- データシート全体にわたって次のように変更:「概要」(続き) で「LIN 物理層仕様のリビジョン 2.0」を「LIN 物理層仕様のリビジョン 2.1」に ... 3
- Added: (LIN 2.1 compatible) to Note 2 of the *Timing Requirements* ... 6
- Changed paragraph three in the Transmitter Characteristics section ... 8
- Changed three instances of "IHN" to "INH" in 図 8-1 ... 10

Changes from Revision C (July 2005) to Revision D (June 2015) **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

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5 概要 (続き)

LIN 物理層仕様のリビジョン 2.1 で規定されているように、TXD ピン上の LIN プロトコル出力データ・ストリームは、TPIC1021 によって制御機能付き電流制限波形整形ローサイド・ドライバを通して LIN バス信号に変換されます。本レシーバは LIN バスからのデータ・ストリームを変換し、RXD ピン経由でデータ・ストリームを出力します。

ウェイクアップ回路がアクティブ状態に維持されており、LIN バスによるリモート・ウェイクアップまたは、NWake または EN ピンによるローカル・ウェイクアップが可能だとしても、低消費電力モードでは、TPIC1021 は、非常に低い静止電流を要求します。

TPIC1021 は、過酷な車載用環境で動作するよう設計されています。本デバイスは、LIN バスの電圧スイングを 40V からグランドまで処理し、–40V まで耐えられます。また、グランド・シフトや電源電圧の切断が発生しても、LIN ピンを経由した電源入力への電流の逆流を防止します。低電圧、過熱、グランド喪失に対する保護機能も備えています。フォルト条件が発生した場合、出力は即座にオフになり、フォルト条件が解消するまでオフに維持されます。

6 Pin Configuration and Functions

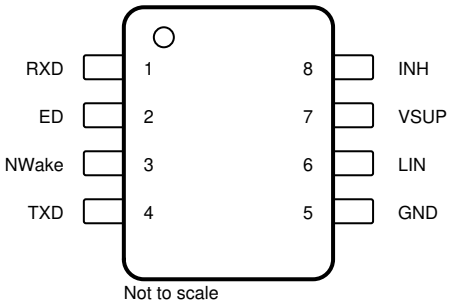


図 6-1. D Package, 8-Pin SOIC

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RXD	O	RXD output (open drain) pin interface reporting state of LIN bus voltage
2	ED	I	Enable input pin
3	NWake	I	High voltage input pin for device wake up
4	TXD	I	TXD input pin interface to control state of LIN output
5	GND	I	Ground connection
6	LIN	I/O	LIN bus pin single wire transmitter and receiver
7	V_{SUP}	Supply	Device supply pin (connected to battery in series with external reverse blocking diode)
8	INH	O	Inhibit pin controls external voltage regulator with inhibit input

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{SUP} (2)	Supply line supply voltage	Continuous	0	27	V
		Transient	0	40	V
	NWake DC and transient input voltage (through 33-kΩ serial resistor)		–1	40	V
	Logic pin input voltage (RXD, TXD, EN)		–0.3	5.5	V
	LIN DC input voltage		–40	40	V
T_A	Operational free-air temperature		–40	125	°C
T_J	Junction temperature		–40	150	°C
	Thermal shutdown			200	°C
	Thermal shutdown hysteresis			25	°C
T_{stg}	Storage temperature range		–40	165	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (2)	LIN pin	±12000	V
			NWake pin	±9000	
			All other pins	±3000	
		Machine model(3)	LIN and NWake pins	±400	
			All other pins	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) The machine model is a 200-pF capacitor through a 10-Ω resistor and a 0.75-μH coil.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_{SUP}	Supply voltage	7		27	V
T_{AMB}	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPIC1021 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

V_{SUP} = 7 V to 27 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SUPPLY						
	Operational supply voltage(2)		7	14	27	V
	Nominal supply line voltage(2)		7	14	18	V
	V_{SUP} undervoltage threshold(2)			4.5		V
I_{CC}	Supply Current	Normal Mode, EN = 1, Bus dominant (total bus load > 500 Ω)(3)		1.2	2.5	mA
		Standby Mode, EN = 0, Bus dominant (total bus load > 500 Ω)(3)		1	2.1	mA
		Normal Mode, EN = 1, Bus recessive		300	500	µA
		Standby Mode, EN = 0, Bus recessive		300	500	µA
		Low Power Mode, EN = 0, V_{SUP} < 14 V, NWake = V_{SUP} , LIN = V_{SUP}		20	50	µA
		Low Power Mode, EN = 0, 14 V < V_{SUP} < 27 V, NWake = V_{SUP}, LIN = V_{SUP}		50	100	µA
RXD OUTPUT PIN						
V_O	Output voltage		-0.3		5.5	V
I_{OL}	Low-level output current, open drain	LIN = 0 V, RXD = 0.4 V	3.5			mA
I_{IKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = 5 V	-5	0	5	µA
TXD INPUT PIN						
V_{IL}	Low-level input voltage(2)		-0.3		0.8	V
V_{IH}	High-level input voltage(2)		2		5.5	V
V_{IT}	Input threshold hysteresis voltage(2)		30		500	mV
	Pull-down resistor		125	350	800	kΩ
I_{IL}	Low-level input current	TXD = 0	-5	0	5	µA
LIN PIN (Referenced to V_{SUP})						
V_{OH}	High-level output voltage(2)	LIN recessive, TXD = High, I_O = 0 mA	V_{SUP}-1V			V
V_{OL}	Low-level output voltage(2)	LIN dominant, TXD = Low, I_O = 40 mA	0		0.2×V_{SUP}	V
	Pull-up resistor to V_{SUP}		20	30	60	kΩ
I_L	Limiting current	TXD = Low	50	150	250	mA
I_{IKG}	Leakage current	LIN = V_{SUP}	-5	0	5	µA
V_{IL}	Low-level input voltage(2)	LIN dominant	0×V_{SUP}		0.4×V_{SUP}	V
V_{IH}	High-level input voltage(2)	LIN recessive	0.6×V_{SUP}		V_{SUP}	V
V_{IT}	Input threshold voltage(2)		0.4×V_{SUP}	0.5×V_{SUP}	0.6×V_{SUP}	V
V_{hys}	Hysteresis voltage(2)		0.05×V_{SUP}		0.175×V_{SUP}	V
V_{IL}	Low-level input voltage for wake-up(2)		0		0.4×V_{SUP}	V
EN PIN						
V_{IL}	Low-level input voltage(2)		-0.3		0.8	V
V_{IH}	High-level input voltage(2)		2		5.5	V
V_{hys}	Hysteresis voltage(2)		30		500	mV
	Pull-down resistor		125	350	800	kΩ
I_{IL}	Low-level input current	EN = 0 V	-5	0	5	µA

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7.5 Electrical Characteristics (continued)

V_{SUP} = 7 V to 27 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
INH PIN						
V_o	DC output voltage	Transient voltage	-0.3		V_{SUP}+0.3	V
I_O	Output current		-50		2	mA
R_{on}	On state resistance	Between V_{SUP} and INH, INH = 2 mA drive, Normal or Standby Mode	25	40	100	Ω
I_{IKG}	Leakage current	Low Power mode, 0 < INH < V_{SUP}	-5	0	5	µA
NWake PIN						
V_{IL}	Low-level input voltage(2)		-0.3		V_{SUP}-3.3	V
V_{IH}	High-level input voltage(2)		V_{SUP}-1		V_{SUP}+0.3	V
	Pull-up current	NWake = 0 V	-40	-10	-4	µA
I_{IKG}	Leakage current	V_{SUP} = NWake	-5	0	5	µA
THERMAL SHUTDOWN						
	Shutdown junction thermal temperature			185		°C

(1) Typical values are given for V_{SUP} = 14 V at 25°C.
(2) All voltages are defined with respect to ground; positive currents flow into the TPIC1021 device.
(3) In the dominant state the supply current increases as the supply voltage increases due to the integrated LIN responder termination resistance. At higher voltages the majority of supply current is through the termination resistance. The minimum resistance of the LIN responder termination is 20 kΩ so the maximum supply current attributed to the termination is: $I_{SUP\ (dom)\ max\ termination} \approx (V_{SUP} – (V_{LIN_Dominant}+0.7\ V) / 20\ k\Omega$.

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
D1	Duty cycle 1(1) (2)	$TH_{REC(max)}$ = 0.744×V_{SUP}, $TH_{DOM(max)}$ = 0.581×V_{SUP}, V_{SUP} = 7.0 V to 18 V, t_{BIT} = 50 µs (20 kbps), See 図 7-1	0.396			
D2	Duty cycle 2(1) (2)	$TH_{REC(max)}$ = 0.284×V_{SUP}, $TH_{DOM(max)}$ = 0.422×V_{SUP}, V_{SUP} = 7.6 V to 18 V, t_{BIT} = 50 µs (20 kbps), See 図 7-1			0.581	
D3	Duty cycle 3(1) (2)	$TH_{REC(max)}$ = 0.778×V_{SUP}, $TH_{DOM(max)}$ = 0.616×V_{SUP}, V_{SUP} = 7.0 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), See 図 7-1	0.417			
D4	Duty cycle 4(1) (2)	$TH_{REC(max)}$ = 0.251×V_{SUP}, $TH_{DOM(max)}$ = 0.389×V_{SUP}, V_{SUP} = 7.6 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), See 図 7-1			0.590	
t_{rx_pdr}	Receiver rising propagation delay time	R_L = 2.4 kΩ, C_L = 20 pF, See 図 7-1			6	µs
t_{rx_pdf}	Receiver rising propagation delay time	R_L = 2.4 kΩ, C_L = 20 pF, See 図 7-1			6	µs
t_{rx_sym}	Symmetry of receiver propagation delay time (rising edge)	with respect to falling edge, See 図 7-1	–2		2	µs
t_{NWake}	NWake filter time for local wake-up	See 図 7-1	25	50	100	µs
t_{LINBUS}	LIN wake-up filter time (dominant time for wake-up via LIN bus)	See 図 7-1	25	50	100	µs
t_{DST}	Dominant state timeout(3)	See 図 7-1	6	9	14	ms

(1) Duty cycle = $t_{BUS_rec(min)}$/ (2×t_{BIT})
(2) Duty Cycles: LIN Driver bus load conditions (CLINBUS, RLINBUS): Load1 = 1 nF, 1 kΩ; Load2 = 6.8 nF, 660 Ω; Load3 = 10 nF, 500 Ω. Duty Cycles 3 and 4 are defined for 10.4 kbps operation. The TPIC1021 also meets these lower speed requirements, while it is capable of the higher speed 20.0 kbps operation as specified by Duty Cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions (LIN 2.1 compatible), for details please refer to the SAEJ2602 specification.
(3) Dominant state timeout will limit the minimum data rate to 2.4 kbps.

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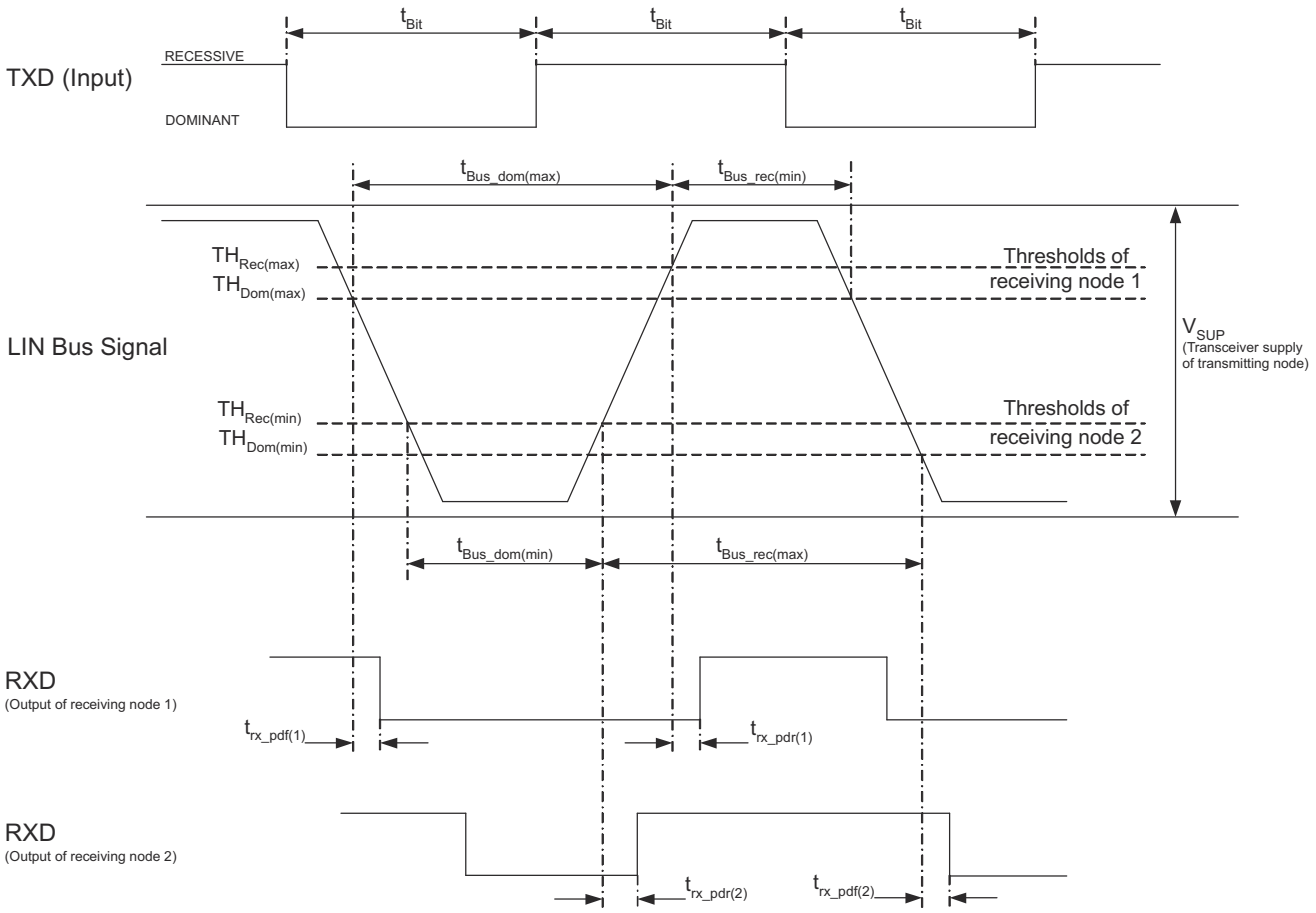


図 7-1. Definition of Bus Timing Parameters

7.7 Typical Characteristics

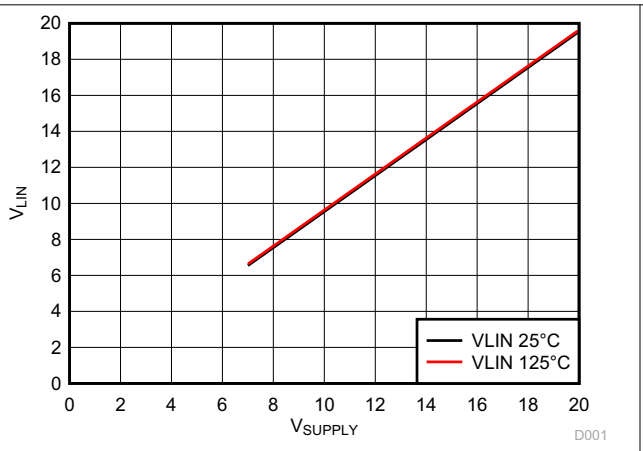


図 7-2. V_{OH} vs V_{SUPPLY} and Temperature

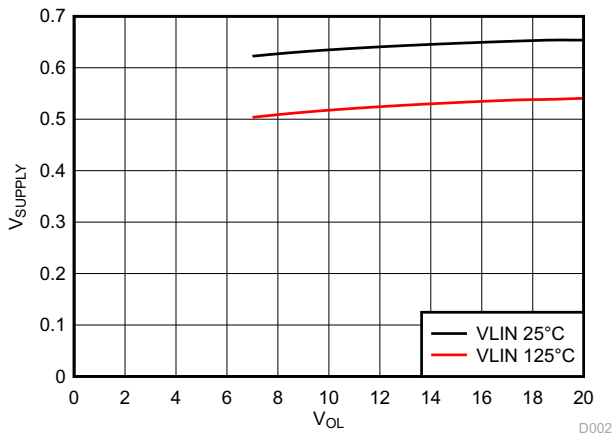


図 7-3. V_{OL} vs V_{SUPPLY} and Temperature

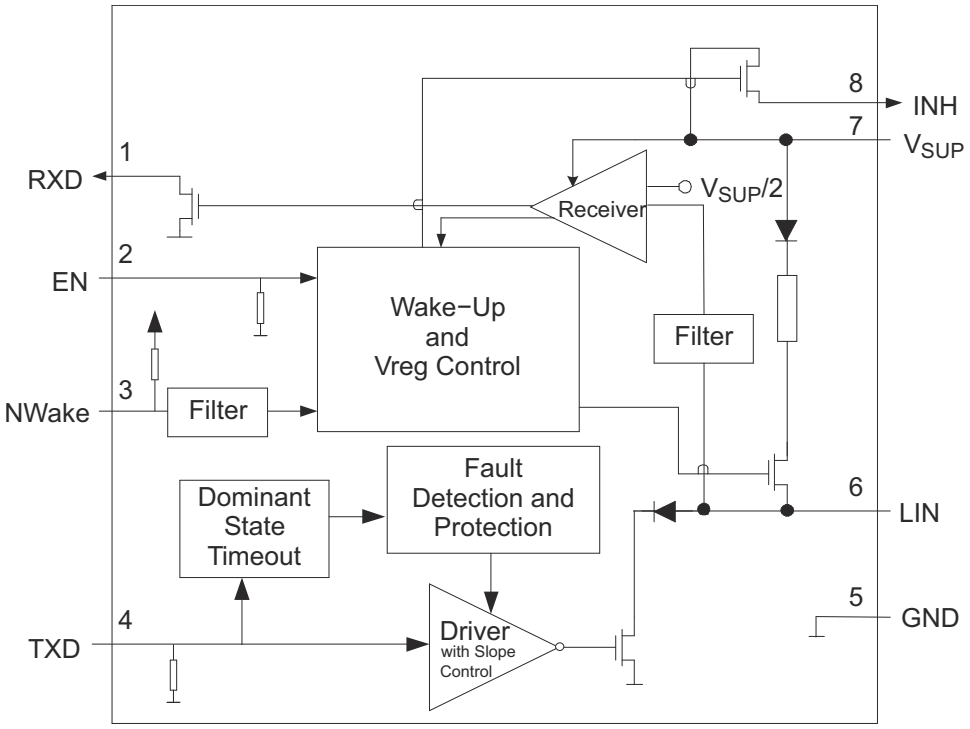
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8 Detailed Description

8.1 Overview

The TPIC1021 is a LIN (Local Interconnect Network) physical layer transceiver which integrates a serial transceiver with wake up and protection features. The LIN bus is a single wire, bi-directional bus that typically is used in low speed in vehicle networks with data rates that range from 2.4 kbps to 20 kbps.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 LIN Bus Pin

This I/O pin is the single-wire LIN bus transmitter and receiver.

8.3.1.1 Transmitter Characteristics

The driver is a low side transistor with internal current limitation and thermal shutdown. There is an internal 30-kΩ pull-up resistor with a serial diode structure to V_{sup} so no external pull-up components are required for LIN responder mode applications. An external pull-up resistor of 1 kΩ plus a series diode to V_{sup} must be added when the device is used for commander node applications.

Voltage on the LIN pin can go from -40 V to +40 V DC without any currents other than through the pull-up resistance. There are no reverse currents from the LIN bus to supply (V_{sup}), even in the event of a ground shift or loss of supply (V_{sup}).

The LIN thresholds and AC parameters are up-to-date with LIN Protocol Specification Revision 2.0, and compatible with Revision 2.1.

During a thermal shut down condition the driver is disabled.

8.3.1.2 Receiver Characteristics

The characteristic thresholds of the receiver are ratio-metric with the device supply pin. Typical thresholds are 50%, with a hysteresis between 5% and 17.5% of supply.

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8.3.2 Transmit Input Pin (TXD)

This pin is the interface to the MCU's LIN Protocol Controller or SCI/UART used to control the state of the LIN output. When TXD is low, LIN output is dominant (near ground). When TXD is high, LIN output is recessive (near battery). TXD input structure is compatible with microcontrollers with 3.3 V and 5.0 V I/O. This pin has an internal pull-down resistor.

8.3.2.1 TXD Dominant State Timeout

If the TXD pin is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by TPIC1021's Dominant State Timeout Timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on the TXD pin for longer than t_{DST}, the transmitter is disabled thus allowing the LIN bus to return to the recessive state and communication to resume on the bus. The timer is reset by a rising edge on TXD pin.

8.3.3 Receive Output Pin (RXD)

This pin is the interface to the LIN protocol controller or SCI/UART of the MCU, which reports the state of the LIN bus voltage. LIN recessive (near battery) is represented by a high level on RXD and LIN dominant (near ground) is represented by a low level on RXD. The RXD output structure is an open-drain output stage. This allows the TPIC1021 to be used with 3.3 V and 5 V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller I/O supply voltage is required.

8.3.3.1 RXD Wake-up Request

When the TPIC1021 has been in low power mode and encounters a wake-up event from the LIN bus or NWake pin the RXD pin will go LOW while the device enters and remains in Standby Mode (until EN is re-asserted high and the device enters Normal Mode).

8.3.4 Ground (GND)

This is the TPIC1021 device ground connection. The TPIC1021 operates with a ground shift as long as the ground shift does not reduce V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the TPIC1021 does not have a significant current consumption on the LIN pin while in the recessive state (<100 µA sourced via the LIN pin) and for the dominant state the pull-up resistor should be active.

8.3.5 Enable Input Pin (EN)

The enable input pin controls the operation mode of the TPIC1021 (Normal or Low Power Mode). When enable is high, the TPIC1021 is in normal mode allowing a transmission path from TXD to LIN and from LIN to RXD. When the enable input is low, the device is put into low power (sleep) mode and there are no transmission paths. The device can enter normal operating mode only after being woken up. The enable pin has an internal pull-down resistor to ensure the device remains in low power mode even if the enable pin floats.

8.3.6 NWake Input Pin (NWake)

The NWake input pin is a high-voltage input used to wake up the TPIC1021 from low power mode. NWake is usually connected to an external switch in the application. A falling edge on NWake with a low that is asserted longer than the filter time (t_{NWAKE}) results in a local wake-up. The NWake pin provides an internal pull-up current source to V_{SUP}.

8.3.7 Inhibit Output Pin (INH)

The inhibit output pin is used to control an external voltage regulator that has an inhibit input. When the TPIC1021 is in normal operating mode, the inhibit high-side switch is enabled and the external voltage regulator is activated. When TPIC1021 is in low power mode, the inhibit switch is turned off, which disables the voltage regulator. A wake-up event on for the TPIC1021 will return the INH pin to V_{SUP} level. The INH pin output current is limited to 2 mA. The INH pin can also drive an external transistor connected to an MCU interrupt input.

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8.4 Device Functional Modes

8.4.1 Operating States

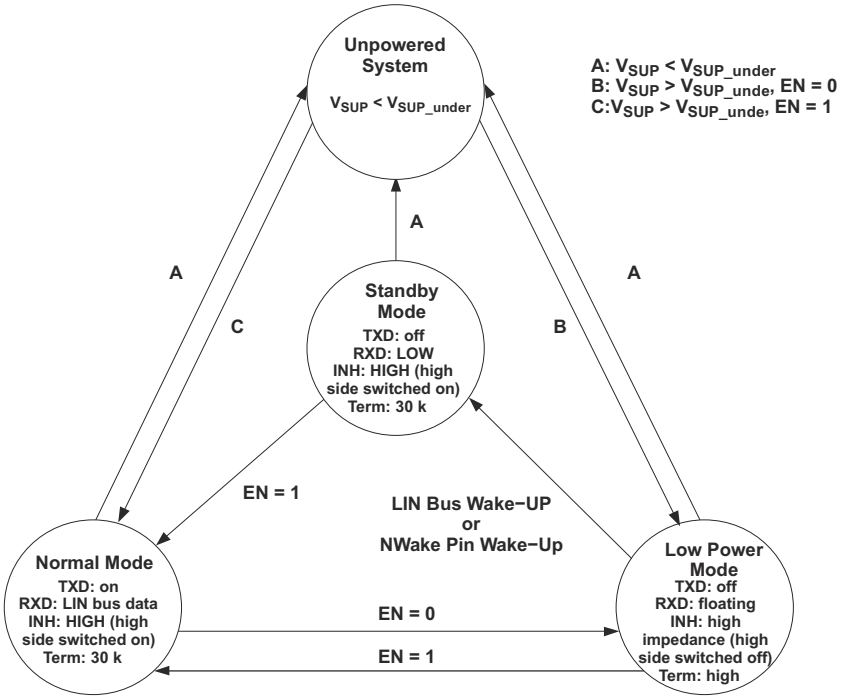


図 8-1. Operating States Diagram

表 8-1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	INH	TRANSMITTER	COMMENTS
Low Power	0	Floating	High impedance	High impedance	Off	
Standby	0	Low	30 kΩ (typical)	High	Off	Wake-up event detected, waiting on MCU to set EN
Normal	1	LIN bus data	30 kΩ (typical)	High	On	

8.4.1.1 Normal Mode

This is the normal operational mode where the receiver and driver are active. The receiver detects the data stream on the LIN bus and outputs it on the RXD pin for the LIN controller where recessive on the LIN bus is a digital high and dominate on the LIN bus is digital low. The driver transmits input data on the TXD pin to the LIN bus.

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8.4.1.2 Low Power Mode

The power saving mode for the TPIC1021 and the default state after power-up (assuming EN=0). Even with the extremely low current consumption in this mode, the TPIC1021 can still wake-up from LIN bus activity, a falling edge on the NWake pin or if EN is set high. The LIN bus and NWake pins are filtered to prevent false wake-up events. The wake-up events must be active for their respective time periods: t_{LINBUS}, t_{NWake}.

The low power mode is entered by setting the EN pin low.

While the device is in low power mode the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short-circuited to ground).
- The normal receiver is disabled.
- The INH pin is high impedance.
- EN input, NWake input and the LIN wake-up receiver are active.

8.4.1.3 Wake-Up Events

There are three ways to wake-up the TPIC1021 from Low Power Mode.

- Remote wake-up via recessive (high) to dominant (low) state transition on LIN Bus where dominant bus state of 50% threshold is detected. The dominant state must be held for t_{LINBUS} filter time (to eliminate false wake ups from disturbances on the LIN Bus).
- Local wake-up via falling edge on NWake pin which is held low for filter time t_{NWake} (to eliminate false wake ups from disturbances on NWake).
- Local wake-up via EN being set high

8.4.1.4 Standby Mode

This mode is entered whenever a wake-up event occurs via the LIN bus or NWake pin while the TPIC1021 is in low power mode. The LIN bus responder termination circuit and the INH pin are turned on when standby mode is entered. The application system powers up once the INH pin is driven high assuming it is using a voltage regulator connected via INH pin. Standby Mode is signaled via a low level on RXD pin.

When EN pin is set high while the TPIC1021 is in Standby Mode the device returns to Normal Mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are turned on.

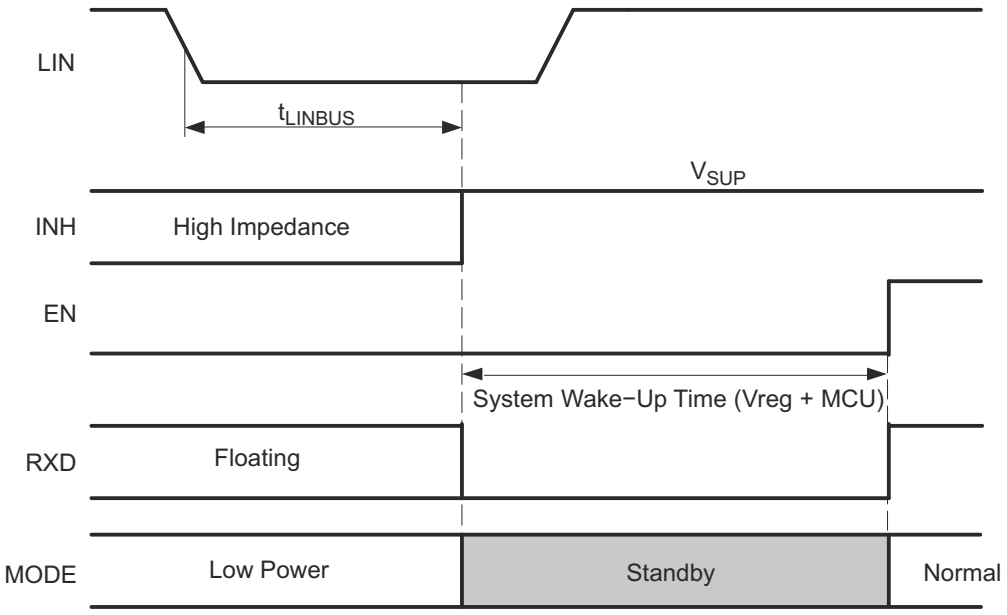


図 8-2. Wake-Up Via LIN Bus Timing Diagram

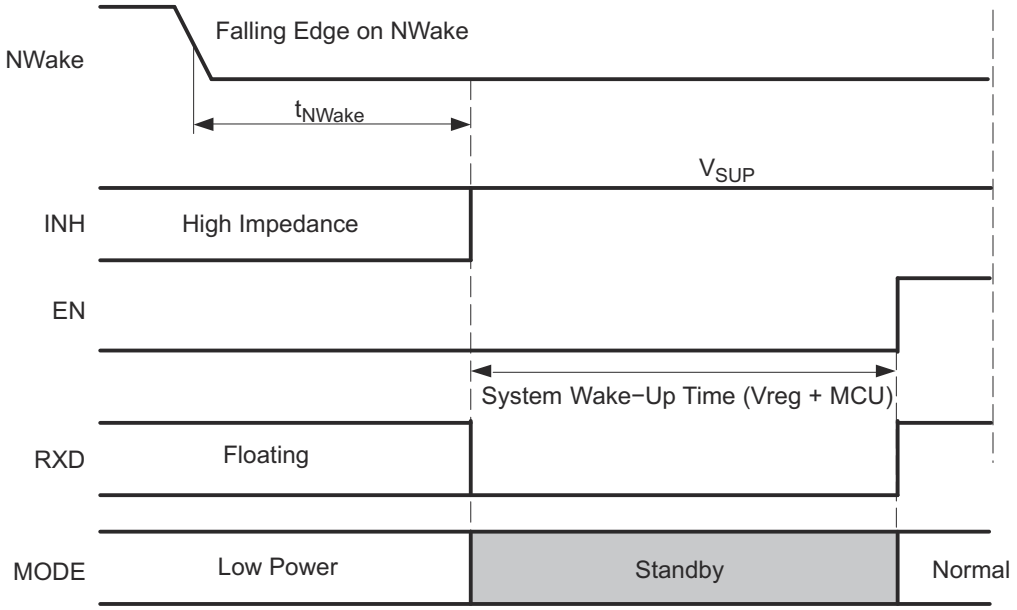


図 8-3. Wake-Up Via NWake Timing Diagram

8.4.2 Supply Voltage (V_{SUP})

This is the TPIC1021 device power supply pin. This pin is connected to the battery through an external reverse battery blocking diode. The continuous DC operating voltage range for the TPIC1021 is from 7 V to +27 V. The V_{SUP} is protected for harsh automotive conditions of up to + 40 V.

The device contains a reset circuit to avoid false bus messages during undervoltage conditions when V_{SUP} is less than V_{SUP_UNDER}.

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9 Application and Implementation

Note

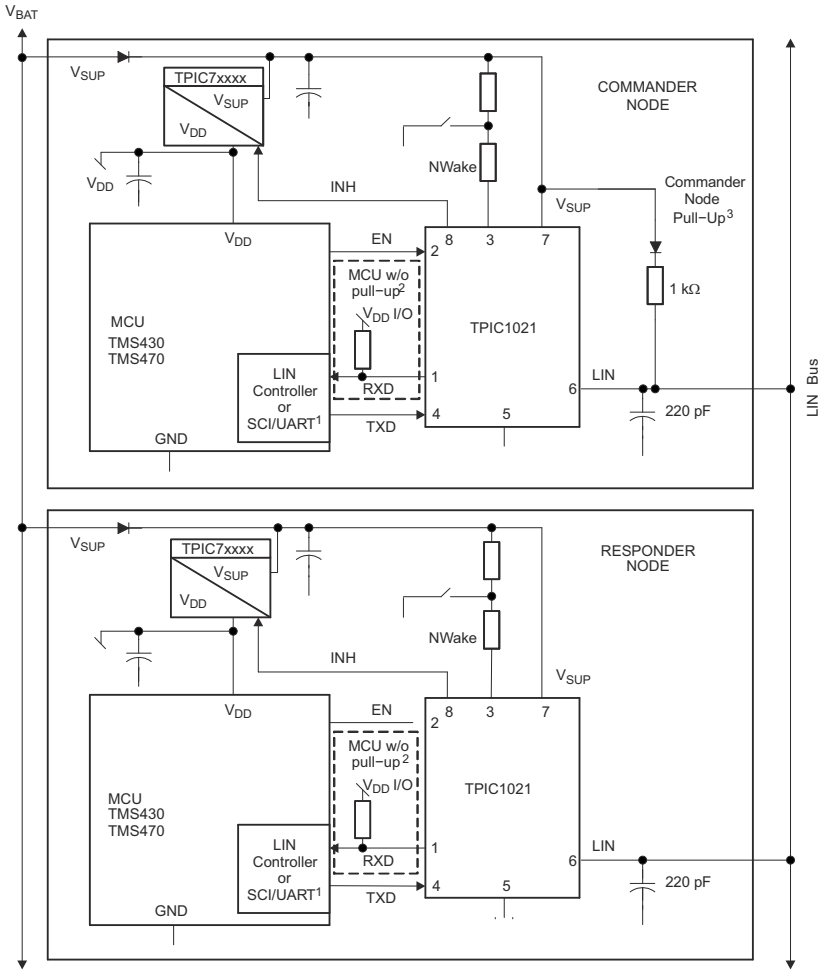
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPIC1021 can be used as both a responder device and a commander device in a LIN network. It comes with the ability to support both remote wake-up requests and local wake-up requests.

9.2 Typical Application

The device comes with an integrated 30-kΩ pullup resistor and series diode for responder applications, and for commander applications an external 1-kΩ pullup with series blocking diode can be used. 図 9-1 shows the device being used in both types of applications.



A. See 1 in the *セクション 9.2.1* section
B. See 2 in the *セクション 9.2.1* section
C. See 3 in the *セクション 9.2.1* section

図 9-1. Typical Application Schematic

9.2.1 Design Requirements

For this design, use these requirements:

1. RXD on MCU or LIN Responder has internal pullup, no external pullup resistor is needed.
2. RXD on MCU or LIN Responder without internal pull-up, requires external pullup resistor.
3. Commander Node applications require an external 1-kΩ pullup resistor and serial diode.

9.2.2 Detailed Design Procedure

The RXD output structure is an open-drain output stage. This allows the TPIC1021 to be used with 3.3-V and 5-V I/O microcontrollers. If the RXD pin of the microcontroller does not have an integrated pull-up, an external pullup resistor to the microcontroller I/O supply voltage is required.

The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible.

The NWAKE pin is a high voltage wake-up input to the device. If this pin is not being used it should be tied to V_{SUP}.

9.2.3 Application Curves

図 9-2 and 図 9-3 show the propagation delay from the TXD pin to the LIN pin for both the recessive to dominant and dominant to recessive states under lightly loaded conditions.

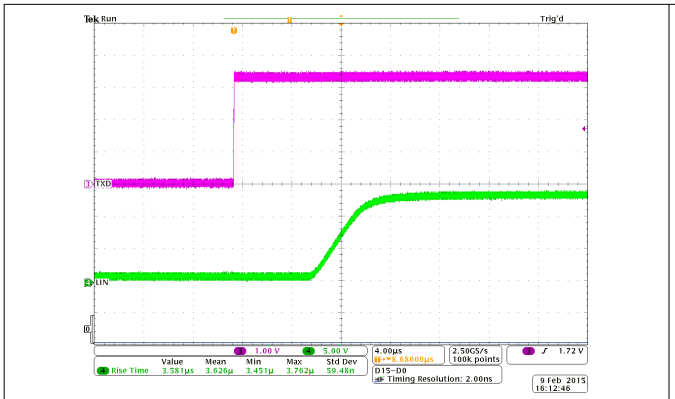


図 9-2. Dominant to Recessive Propagation Delay

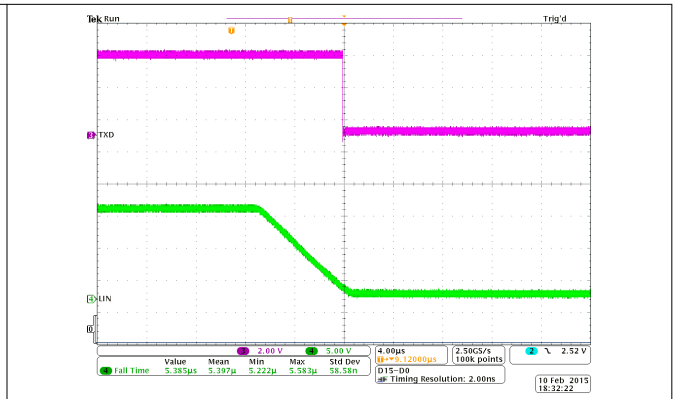


図 9-3. Recessive to Dominant Propagation Delay

9.3 Power Supply Recommendations

The TPIC1021 was designed to operate directly off car battery, or any other DC supply ranging from 7 V to 27 V. A 100-nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

9.4 Layout

9.4.1 Layout Guidelines

- Pin 1 is the RXD output of the TPIC1021. It is an open drain output and requires an external pull-up resistor in the range of 1 to 10 kΩ to function properly. If the micro-processor paired with the transceiver does not have an integrated pullup and external resistor should be placed between RXD and the regulated voltage supply for the micro-processor.
- Pin 2 is the EN input pin for the device that is used to place the device in low power sleep mode. If this feature is not used on the device, the pin should be pulled high to the regulated voltage supply of the micro-processor through a series 1-kΩ to 10-kΩ series resistor. Additionally, a series resistor may be placed on the pin to limit the current on the digital lines in the case of an overvoltage fault.
- Pin 3 is a high-voltage local wake up input pin. The device is typically externally controlled by a normally open switch tied between NWAKE and ground. When the momentary switch is pressed the NWAKE pin is pulled to ground signaling a local wake-up event. A series resistor between VBATT and the switch, and NWAKE and

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the switch should be placed to limit current. If the NWAKE local wake-up feature is not used, the pin can be tied to V_{SUP} through a 1-kΩ to 10-kΩ pullup resistor.

- Pin 4 is the transmit input signal to the device. A series resistor can be placed to limit the input current to the device in the case of an overvoltage on this pin. Also a capacitor to ground can be placed close to the input pin of the device to filter noise.
- Pin 5 is the ground connection of the device. This pin should be tied to a ground plane through a short trace with the use of two vias to limit total return inductance.
- Pin 6 is the LIN bus connection of the device. For responder applications a 220pF bus capacitor is implemented. For commander applications an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin.
- Pin 7 is the supply pin for the device. A 100-nF decoupling capacitor should be placed as close to the device as possible.
- Pin 8 is a high-voltage output pin that may be used to control the local power supplies. If this feature is not used the pin may be left floating.

Note

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

9.4.2 Layout Example

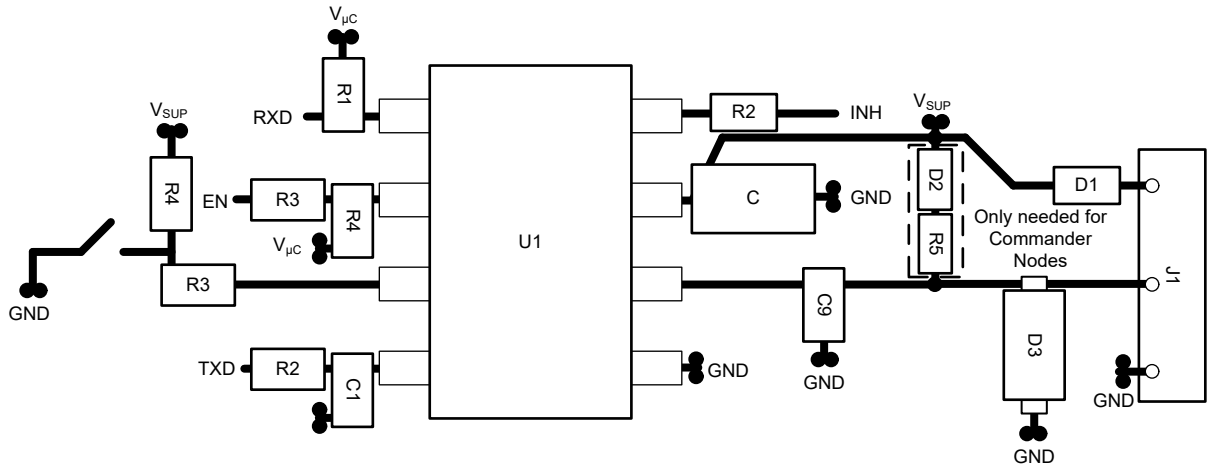


図 9-4. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPIC1021D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021
TPIC1021D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021
TPIC1021DG4	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	T1021
TPIC1021DG4.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021
TPIC1021DR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021
TPIC1021DR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021
TPIC1021DRG4	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	T1021
TPIC1021DRG4.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1021

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

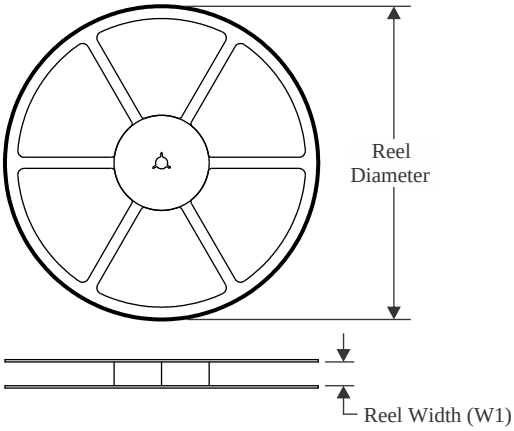
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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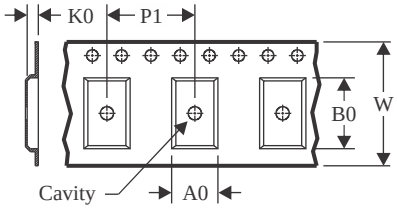
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

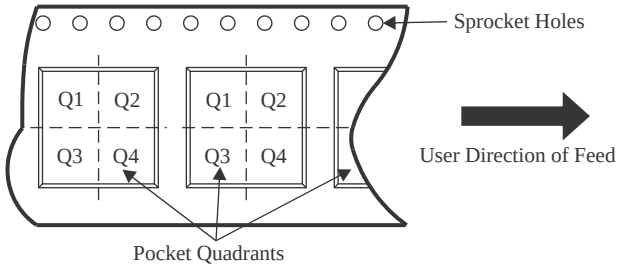


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

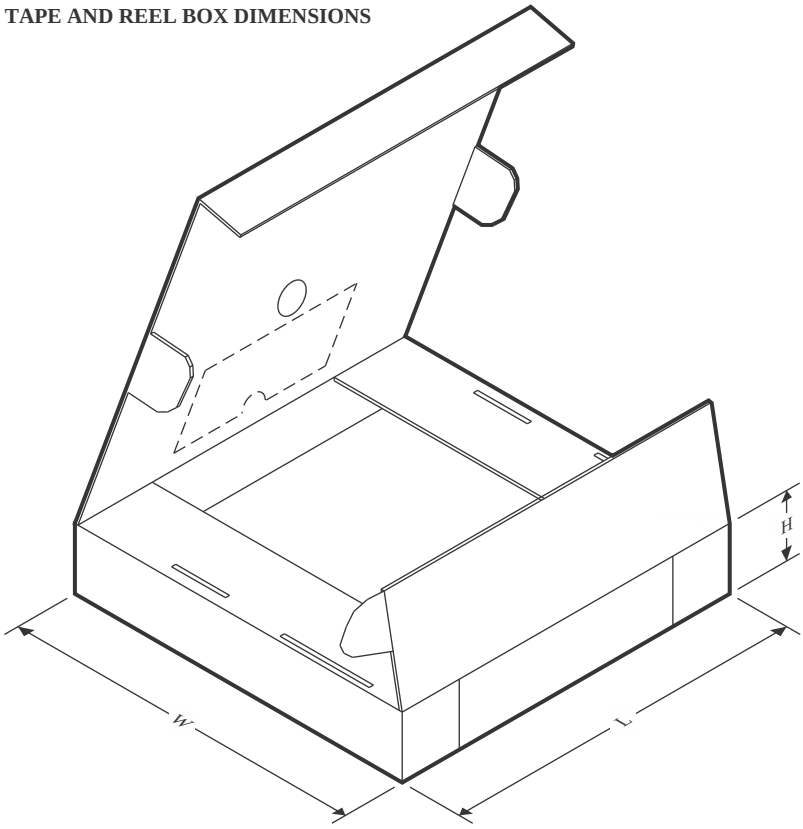
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC1021DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPIC1021DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

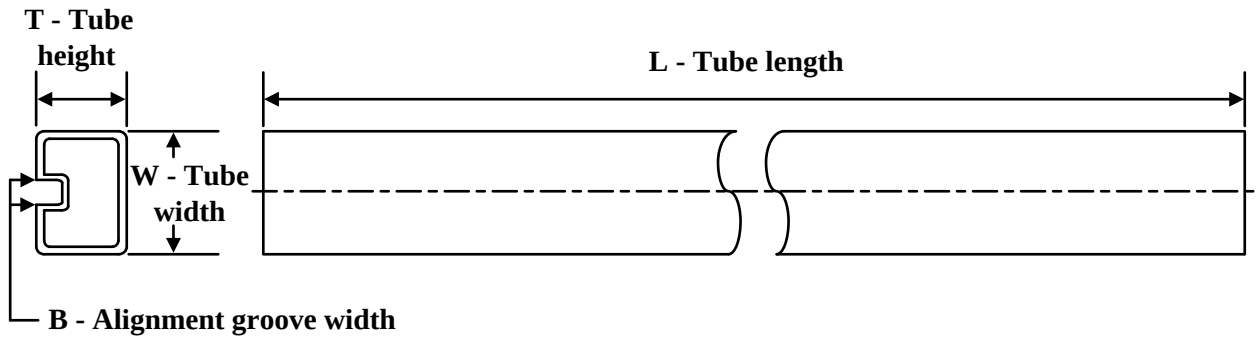
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

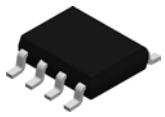
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC1021DR	SOIC	D	8	2500	353.0	353.0	32.0
TPIC1021DRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPIC1021D	D	SOIC	8	75	505.46	6.76	3810	4
TPIC1021D	D	SOIC	8	75	506.6	8	3940	4.32
TPIC1021D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPIC1021D.A	D	SOIC	8	75	506.6	8	3940	4.32
TPIC1021DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPIC1021DG4	D	SOIC	8	75	506.6	8	3940	4.32
TPIC1021DG4.A	D	SOIC	8	75	505.46	6.76	3810	4
TPIC1021DG4.A	D	SOIC	8	75	506.6	8	3940	4.32

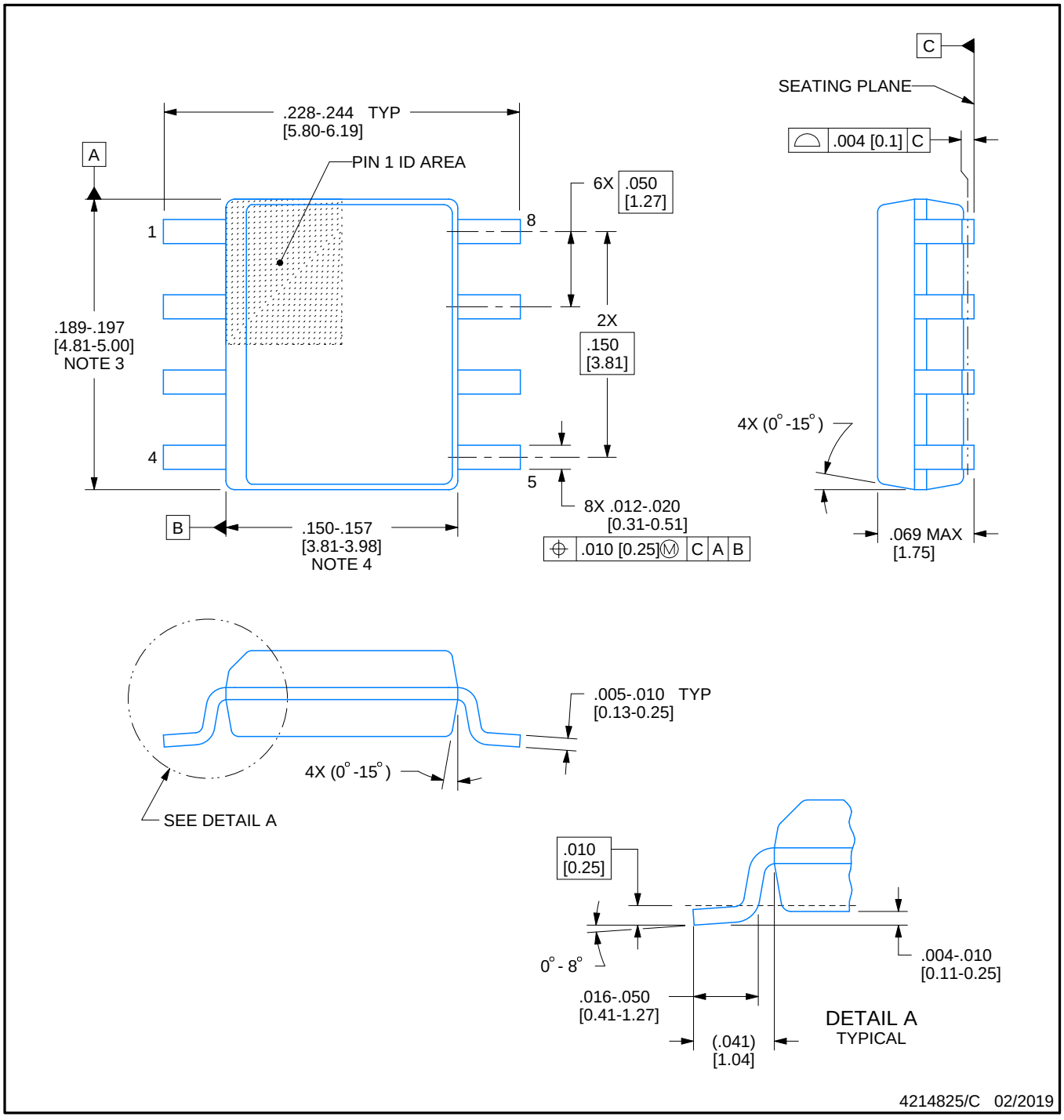


PACKAGE OUTLINE

D0008A

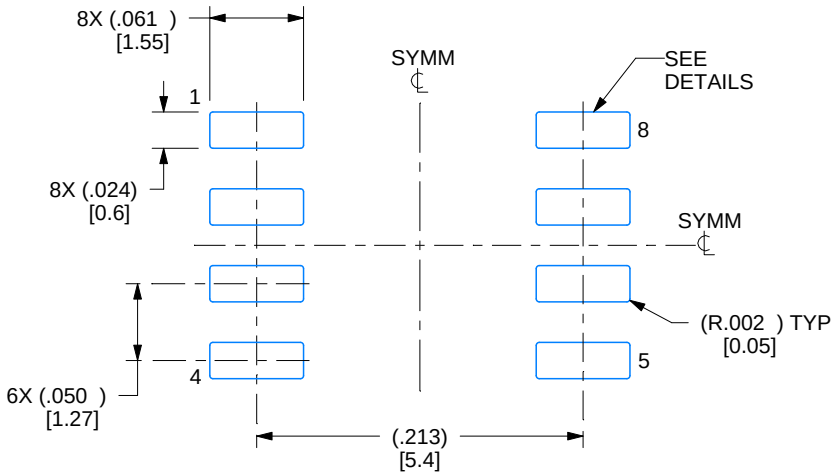
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

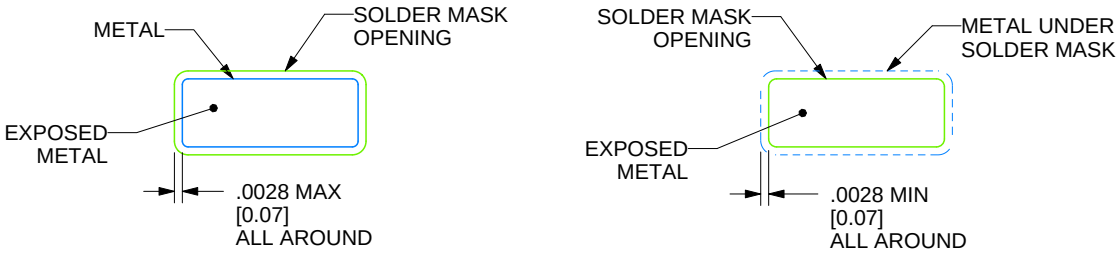


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

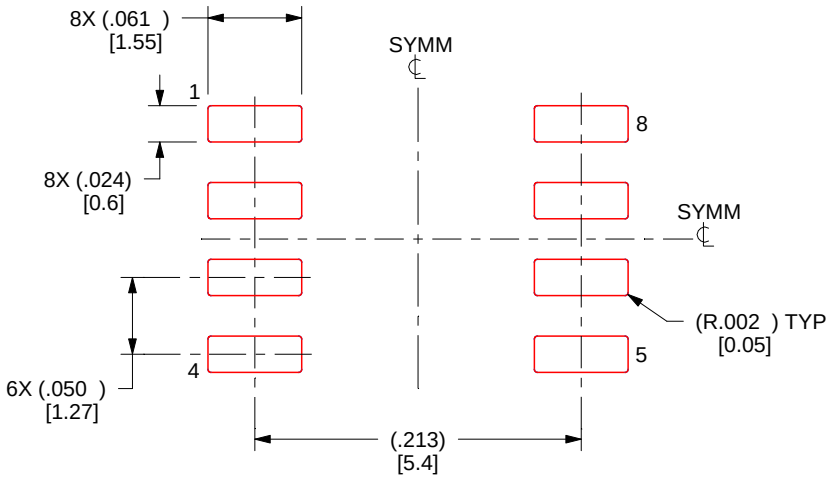
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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