TEXAS INSTRUMENTS
TPS22917
JAJSEO2B – SEPTEMBER 2017 – REVISED DECEMBER 2021

TPS22917x 1V～5.5V、2A、80mΩ、超低リーク負荷スイッチ

1 特長

- 動作入力電圧範囲 (V_{IN}):1V～5.5V
- 最大連続電流 (I_{MAX}):2A
- オン抵抗 (R_{ON})
  - $5V_{IN}$ = 80mΩ (標準値)
  - $1.8V_{IN}$ = 120mΩ (標準値)
  - $1V_{IN}$ = 220mΩ (標準値)
- 超低消費電力
  - オン状態 (I_Q):0.5µA (標準値)
  - オフ状態 (I_{SD}):10nA (標準値)
- ON ピンのスマート・プルダウン (R_{PD})
  - ON ≥ VIH (I_{ON}):10nA (最大値)
  - ON ≤ VIL (R_{PD}):750kΩ (標準値)
- 電源オンの調整により突入電流を制限可能 (t_{ON})
  - 72mV/µs (C_T = オープン) 時に 5V t_{ON} = 100µs
  - 2.3mV/µs (C_T = 1000pF) 時に 5V t_{ON} = 4000µs
- 出力放電および立ち下がり時間を変更可能
  - オプションの QOD 抵抗 ≥ 150Ω (内部)
- 常時オンの真の逆電流ブロック (RCB)
  - アクティブ化電流 (I_{RCB}):–500mA (標準値)
  - 逆リーク電流 ($I_{IN,RCB}$):–1µA 以下

2 アプリケーション

- 産業用システム
- セットトップ・ボックス
- 血糖値計
- POS システム

3 概要

TPS22917x デバイスは小型のシングル・チャネル負荷スイッチで、リーク電流の低い P チャネル MOSFET を使用し、電力損失を最小限に抑えています。高度なゲート制御設計により、最低 1V の電圧で動作し、オン抵抗と電力損失の増大は最小限です。

立ち上がりと立ち下がりの時間は、外付け部品により別々に変更でき、システム・レベルの最適化が可能です。タイミング・コンデンサ (C_T) および電源オン時間の変更により、不必要なシステム遅延を増やすことなしに、突入電流を管理できます。出力放電抵抗 (QOD) を使用して、出力の立ち下がり時間を調整できます。QOD ピンを出力に直接接続すると、立ち下がり時間が最短に、オープンにすると立ち下がり時間が最長になります。

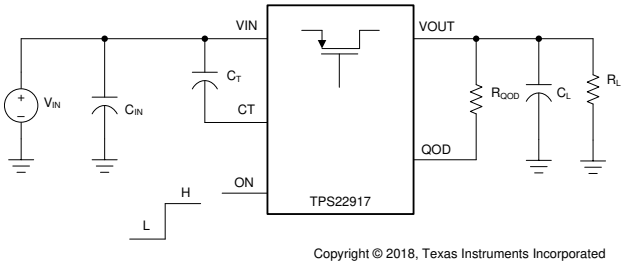
スイッチのオン状態はデジタル入力により制御され、この入力は低電圧の制御信号と直接接続できます。TPS22917 はアクティブ HIGH のイネーブル・ロジックを使っており、TPS22917L はアクティブ LOW のイネーブル・ロジックを使っています。電源が最初に印加されたときには、スマート・プルダウンを使用して、システムのシーケンシングが完了するまで、ON ピンがフローティング状態になることが防止されます。ON ピンが意図的に HIGH (≥ V_{IH}) に駆動された後、不必要な電力損失を避けるため、スマート・プルダウン (R_{PD}) は切断されます。

TPS22917x デバイスは、ハンダ接合部の目視検査が可能なリード付き SOT-23 パッケージ (DBV) で供給されます。このデバイスは、–40℃～125℃の温度範囲での動作が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS22917x	SOT-23 (6)	2.90mm × 1.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (February 2018) to Revision B (December 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• データシートに TPS22917L 注文可能製品を追加	1

Changes from Revision * (September 2017) to Revision A (February 2018)	Page
• 製品ステータスを事前情報から量産データに変更	1

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5 Device Comparison Table

Device	ON Pin Logic
TPS22917	Active High
TPS22917L	Active Low

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6 Pin Configuration and Functions

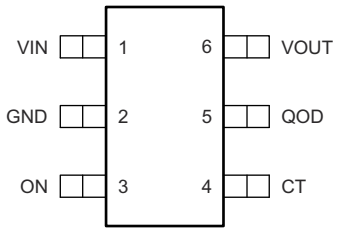


図 6-1. DBV Package 6-Pin SOT-23 Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input
2	GND	—	Device ground
3	ON	I	Active high switch control input. Do not leave floating.
4	CT	O	Switch slew rate control. Connect capacitor from this pin to VIN to increase output slew rate and turn-on time. Can be left floating for fastest timing.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for more information.
6	VOUT	O	Switch output

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	Enable voltage	–0.3	6	V
V_{QOD}	QOD pin voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		2.5	A
$T_{J,MAX}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead temperature (10-s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1	5.5	V
V_{OUT}	Output voltage	0	5.5	V
V_{IH}	High-level input voltage, ON	1	5.5	V
V_{IL}	Low-level input voltage, ON	0	0.35	V
V_{QOD}	QOD Pin Voltage	0	5.5	V
V_{CT}	Timing Capacitor Voltage Rating	7		V

7.4 Thermal Information

Thermal Parameters(1)		TPS22917 DBV (SOT-23) 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	183	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	152	°C/W
θ_{JB}	Junction-to-board thermal resistance	34	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies for all variants over the entire recommended power supply voltage range of 1 V to 5.5 V. Typical Values are at 25°C.

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
INPUT SUPPLY(VIN)								
$I_{Q,VIN}$	V_{IN} Quiescent current	Enabled, V_{OUT} = Open		–40°C to +85°C		0.5	1.0	µA
				–40°C to +125°C			1.2	µA
$I_{SD,VIN}$	V_{IN} Shutdown current	Disabled, V_{OUT} = GND (TPS22917)		–40°C to +85°C		10	100	nA
				–40°C to +105°C			250	nA
		Disabled, V_{OUT} = GND (TPS22917L)		–40°C to +85°C		175	300	nA
				–40°C to +105°C			400	nA
ON-RESISTANCE(R_{ON})								
R_{ON}	ON-Resistance	I_{OUT} = 200 mA	V_{IN} = 5 V	25°C		80	100	mΩ
				–40°C to +85°C			120	
				–40°C to +105°C			130	
				–40°C to +125°C			140	
			V_{IN} = 3.6 V	25°C		90	110	
				–40°C to +85°C			140	
				–40°C to +105°C			150	
				–40°C to +125°C			160	
			V_{IN} = 1.8 V	25°C		120	150	
				–40°C to +85°C			175	
				–40°C to +105°C			185	
				–40°C to +125°C			200	
			V_{IN} = 1.2 V	25°C		170	220	
				–40°C to +85°C			265	
				–40°C to +105°C			280	
				–40°C to +125°C			300	
			VIN = 1.0 V	25°C		220	300	
				–40°C to +85°C			350	
				–40°C to +105°C			370	
				–40°C to +125°C			390	
ENABLE PIN(ON)								
I_{ON}	ON Pin leakage	Enabled (TPS22917)		–40°C to +125°C	–10		10	nA
		Enabled (TPS22917L)		–40°C to +125°C	–20		20	nA
R_{PD}	Smart Pull Down Resistance	$V_{ON} \le V_{IL}$		–40°C to +105°C		750		kΩ
REVERSE CURRENT BLOCKING(RCB)								
I_{RCB}	RCB Activation Current	Enabled, $V_{OUT} > V_{IN}$		–40°C to +125°C		-0.5	-1	A
t_{RCB}	RCB Activation time	Enabled, $V_{OUT} > V_{IN}$ + 200mV		–40°C to +125°C		10		µs
V_{RCB}	RCB Release Voltage	Enabled, $V_{OUT} > V_{IN}$		–40°C to +125°C		25		mV
$I_{IN,RCB}$	VIN Reverse Leakage Current	0 V ≤ V_{IN} + V_{RCB} ≤ V_{OUT} ≤ 5.5 V		–40°C to +105°C	–1			µA
QUICK OUTPUT DISCHARGE(QOD)								
QOD	Output discharge resistance	Disabled		–40°C to +105°C		150		Ω

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7.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of C_L = 1 µF, R_L = 10 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	V_{IN} = 5.0 V	C_T = Open		100		µs
			C_T ≥ 100 pF		4		µs/pF
		V_{IN} = 3.6 V	C_T = Open		120		µs
			C_T ≥ 100 pF		3.8		µs/pF
		V_{IN} = 1.8 V	C_T = Open		200		µs
			C_T ≥ 100 pF		3.6		µs/pF
		V_{IN} = 1.2 V	C_T = Open		300		µs
			C_T ≥ 200 pF		3.4		µs/pF
		V_{IN} = 1.0 V	C_T = Open		400		µs
			C_T ≥ 400 pF		3		µs/pF
t_R	Output Rise Time	V_{IN} = 5.0 V	C_T = Open		55		µs
			C_T ≥ 100 pF		1.8		µs/pF
		V_{IN} = 3.6 V	C_T = Open		65		µs
			C_T ≥ 100 pF		1.6		µs/pF
		V_{IN} = 1.8 V	C_T = Open		100		µs
			C_T ≥ 100 pF		1.2		µs/pF
		V_{IN} = 1.2 V	C_T = Open		150		µs
			C_T ≥ 200 pF		0.95		µs/pF
		V_{IN} = 1.0 V	C_T = Open		200		µs
			C_T ≥ 400 pF		0.6		µs/pF
SR_{ON}	Turn ON Slew Rate(1)	V_{IN} = 5.0 V	C_T = Open		72		mV/µs
			C_T ≥ 100 pF		2300		(mV/µs)*pF
		V_{IN} = 3.6 V	C_T = Open		44		mV/µs
			C_T ≥ 100 pF		1900		(mV/µs)*pF
		V_{IN} = 1.8 V	C_T = Open		14		mV/µs
			C_T ≥ 100 pF		1100		(mV/µs)*pF
		V_{IN} = 1.2 V	C_T = Open		6.2		mV/µs
			C_T ≥ 200 pF		1000		(mV/µs)*pF
		V_{IN} = 1.0 V	C_T = Open		3.9		mV/µs
			C_T ≥ 400 pF		1100		(mV/µs)*pF
t_{OFF}	Turn OFF Time				10		µs
t_{FALL}	Output Fall Time(2)	R_L = 10 Ω	C_L = 1uF, R_{QOD} = Short		22		µs
		R_L = Open	C_L = 10uF, R_{QOD} = Short		3.8		ms
			C_L = 10uF, R_{QOD} = 100 Ω		5.9		ms
			C_L = 220uF, R_{QOD} = Short		72		ms

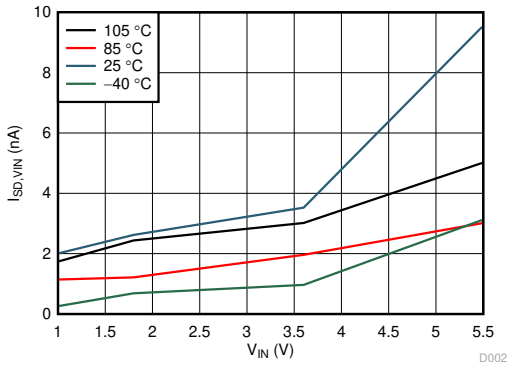
(1) SR_{ON} is the fastest Slew Rate during the turn on time (t_{ON})
(2) Output may not discharge completely if QOD is not connected to VOUT.

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7.7 Typical Characteristics

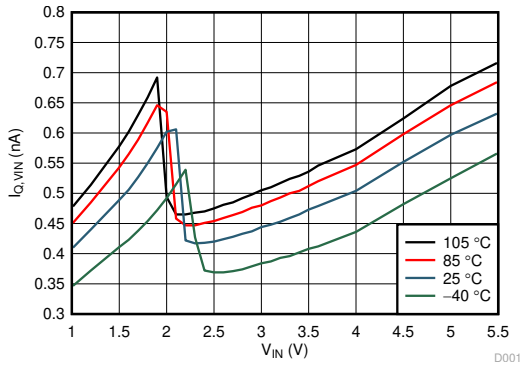
7.7.1 Typical Electrical Characteristics

The typical characteristics curves in this section apply at 25°C unless otherwise noted.



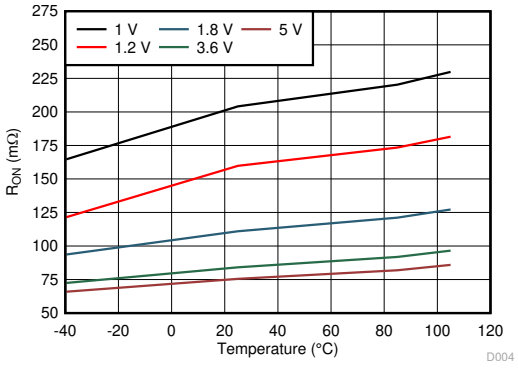
$V_{ON} \le V_{IL}$

図 7-1. Shutdown Current (I_{SD})



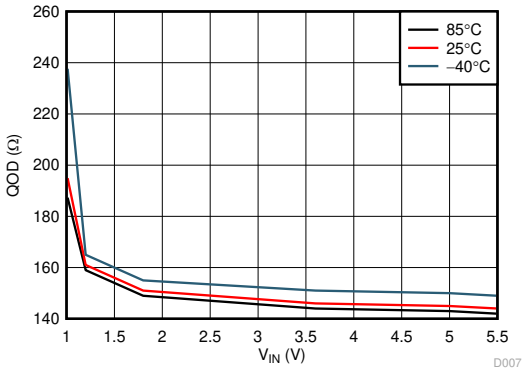
$V_{ON} \ge V_{IH}$

図 7-2. Quiescent Current (I_Q)



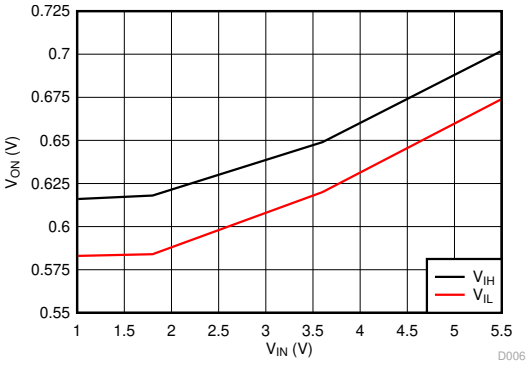
$V_{ON} \ge V_{IH}$

図 7-3. ON-Resistance (R_{ON})



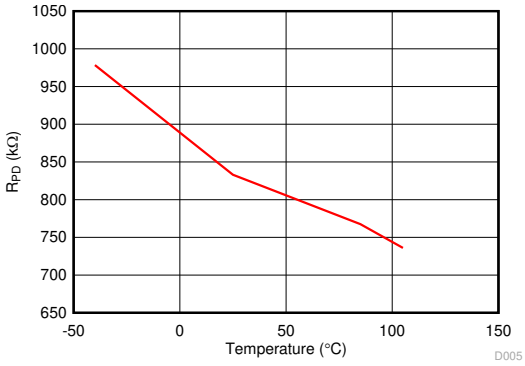
$V_{ON} \le V_{IL}$

図 7-4. Quick Output Discharge (QOD)



–40°C to +105°C

図 7-5. ON Pin Threshold



$V_{ON} \le V_{IL}$

図 7-6. ON Pin Smart Pulldown (R_{PD})

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7.7.2 Typical Switching Characteristics

The typical data in this section apply at 25°C with a load of C_L = 1 µF, R_L = 10 Ω, and QOD shorted to VOUT unless otherwise noted.

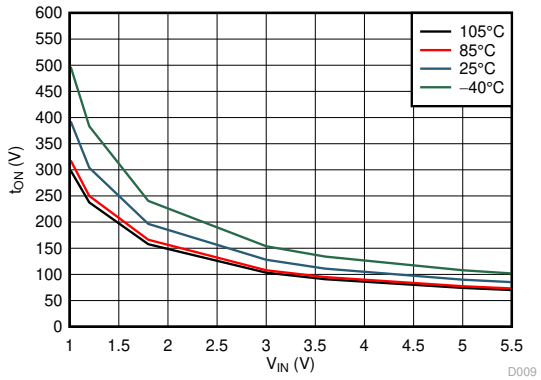


図 7-7. Turn-On Time (CT = Open)

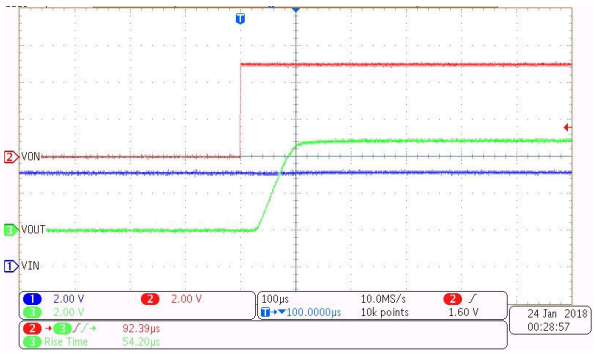


図 7-8. Turn-On at 5 V (CT = Open)

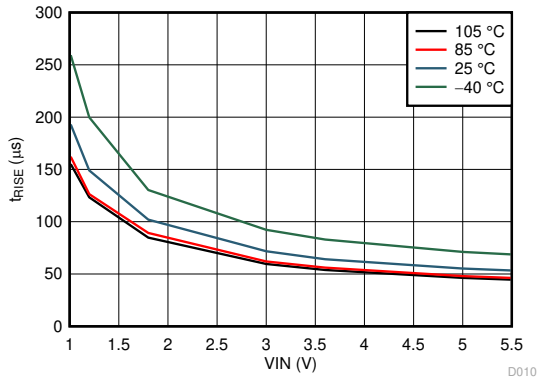


図 7-9. Rise Time (CT = Open)

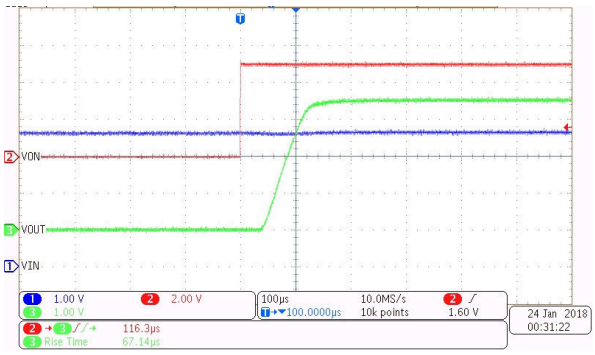


図 7-10. Turn-On at 3.6 V (CT = Open)

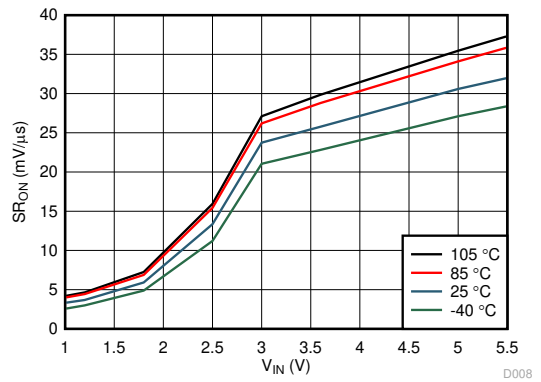


図 7-11. Slew Rate (CT = Open)

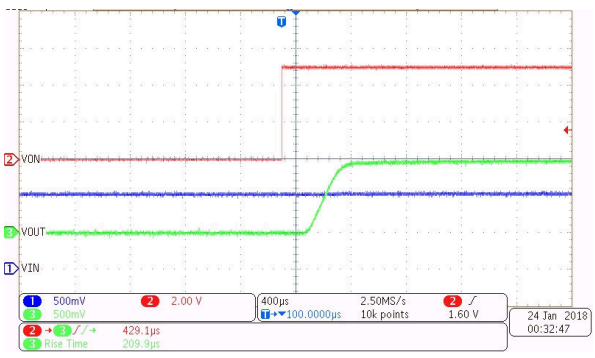


図 7-12. Turn On at 1 V (CT = Open)

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7.7.2 Typical Switching Characteristics (continued)

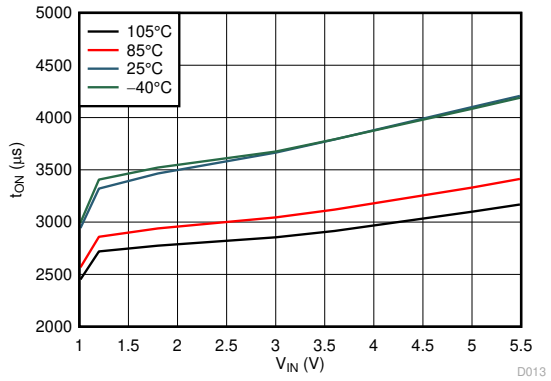


図 7-13. Turn On Time (CT = 1000 pF)

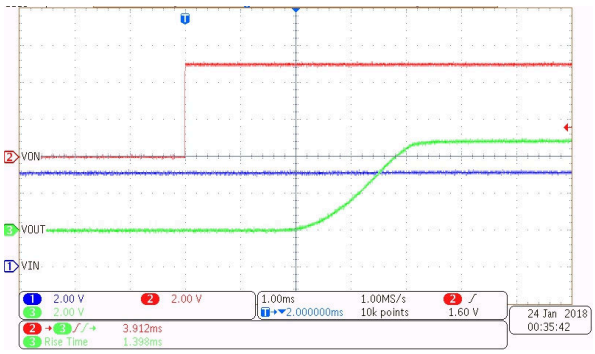


図 7-14. Turn-On at 5 V (CT = 1000 pF)

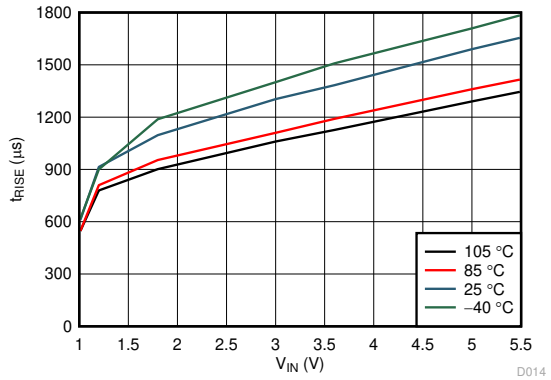


図 7-15. Rise Time (CT = 1000 pF)

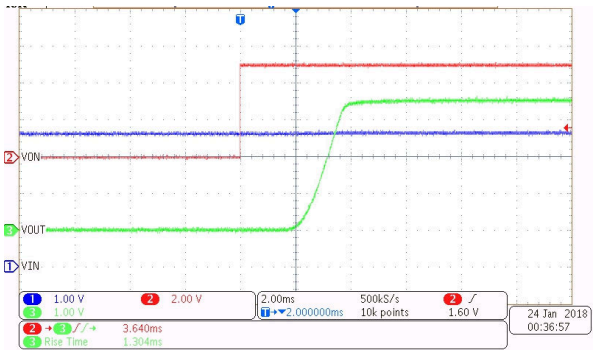


図 7-16. Turn-On at 3.6 V (CT = 1000 pF)

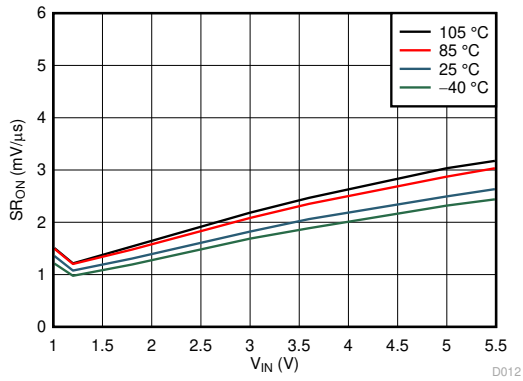


図 7-17. Slow Slew Rate (CT = 1000 pF)

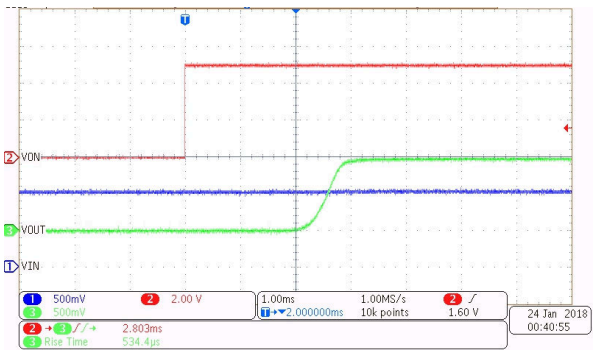
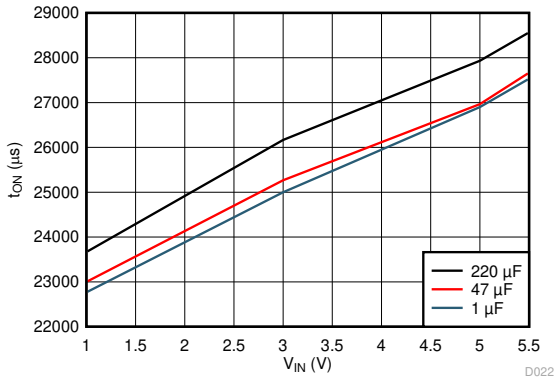


図 7-18. Turn-On at 1 V (CT = 1000 pF)

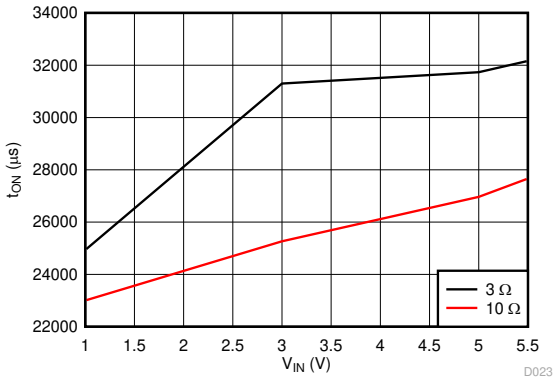
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7.7.2 Typical Switching Characteristics (continued)



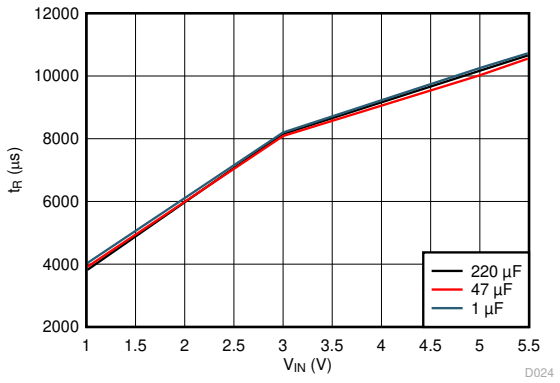
R_L = 10 Ω

図 7-19. Turn-On vs Load Capacitance (CT = 10000 pF)



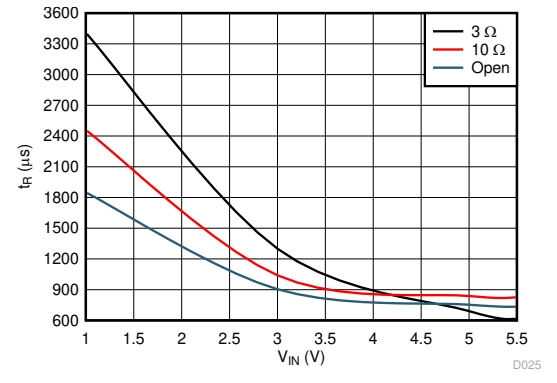
C_L = 47 µF

図 7-20. Turn-On vs Load Resistance (CT = 10000 pF)



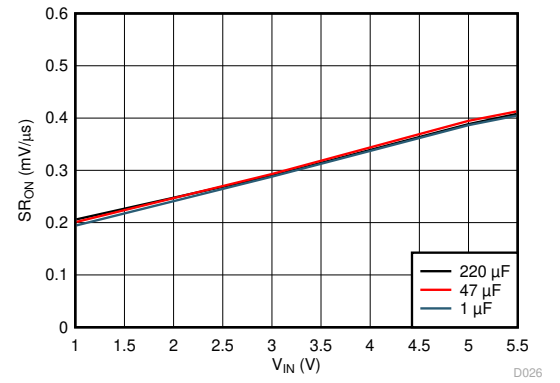
R_L = 10 Ω

図 7-21. Rise Time vs Load Capacitance (CT = 10000 pF)



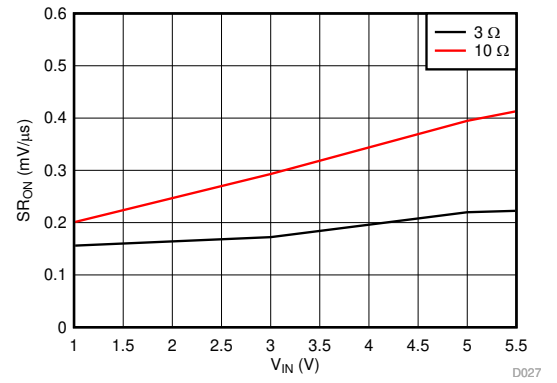
C_L = 47 µF

図 7-22. Rise Time vs Load Resistance (CT = 10000 pF)



R_L = 10 Ω

図 7-23. Slew Rate vs Load Capacitance (CT = 10000 pF)



C_L = 47 µF

図 7-24. Slew Rate vs Load Resistance (CT = 10000 pF)

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7.7.2 Typical Switching Characteristics (continued)

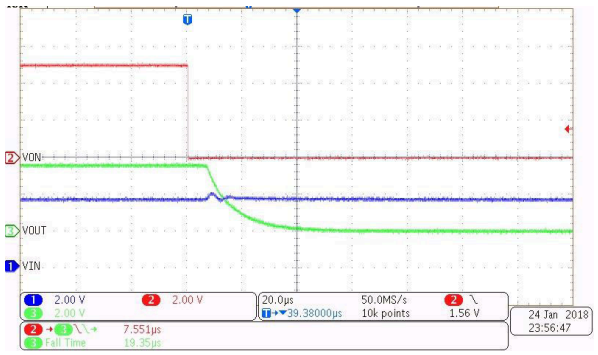
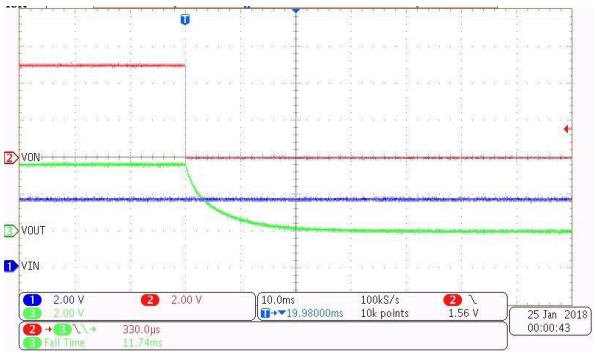
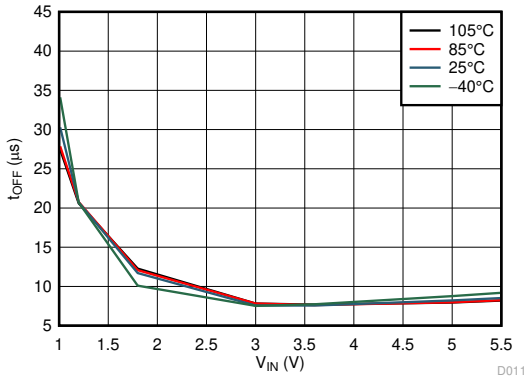


図 7-25. Turn-Off at 3.6 V



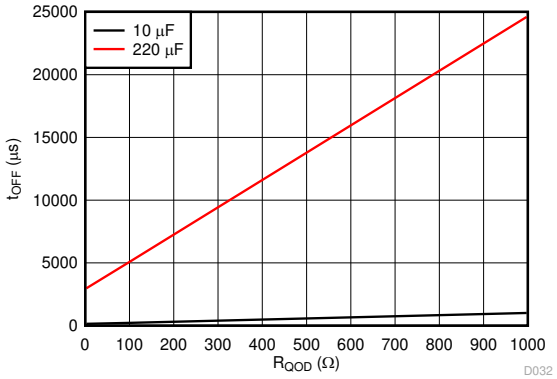
R_L = Open C_L = 47 µF

図 7-26. Turn-Off at 3.6 V (Open Load)



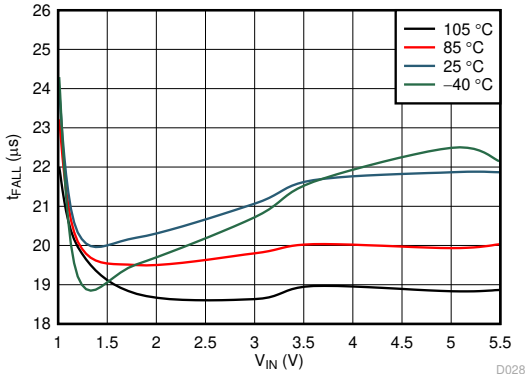
V_{IN} = 1 V to 5.5 V

図 7-27. Turn-Off Time



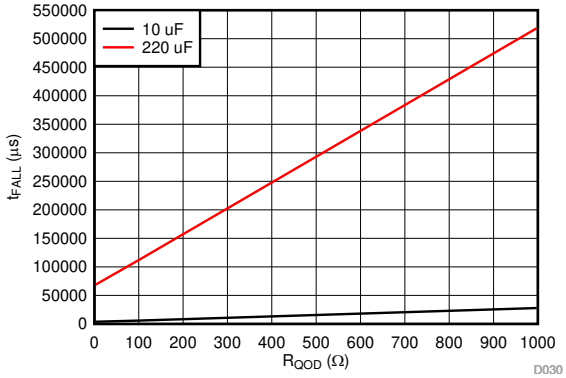
V_{IN} = 1 V to 5.5 V R_L = Open

図 7-28. Turn-Off Time (Open Load)



V_{IN} = 1 V to 5.5 V

図 7-29. Fall Time



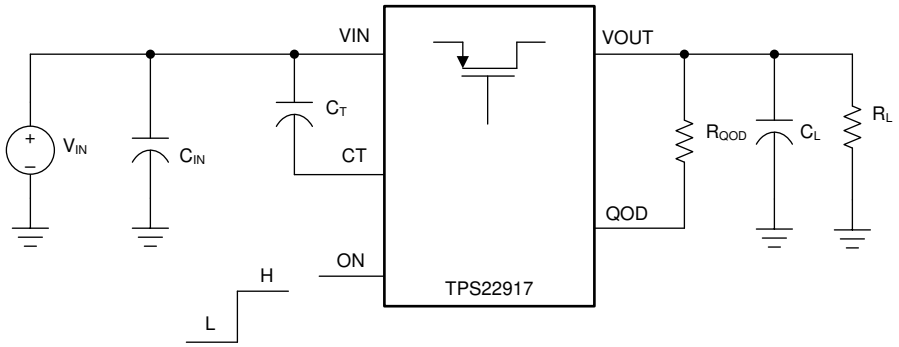
V_{IN} = 1 V to 5.5 V R_L = Open

図 7-30. Fall Time (Open Load)

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8 Parameter Measurement Information

8.1 Test Circuit and Timing Waveforms Diagrams



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A. Rise and fall times of the control signal are 100 ns.

B. Turn-off times and fall times are dependent on the time constant at the load. For TPS22917x, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is (R_{QOD} + QOD || R_L) × C_L.

図 8-1. Test Circuit

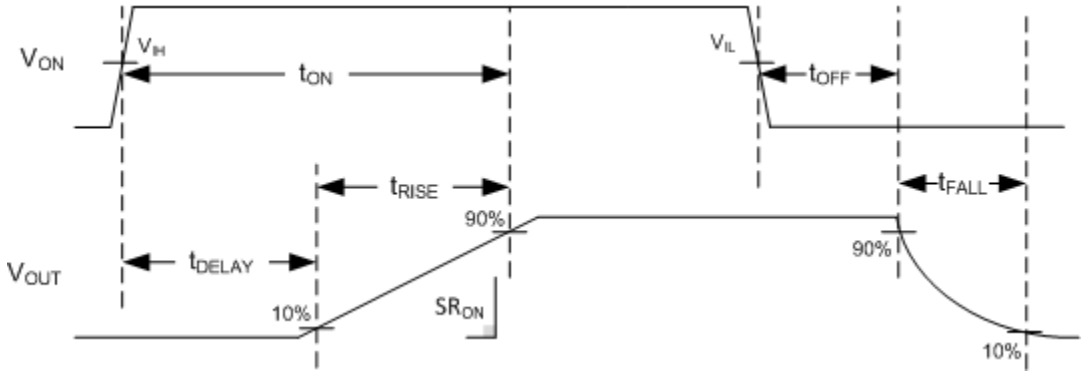


図 8-2. Timing Waveforms

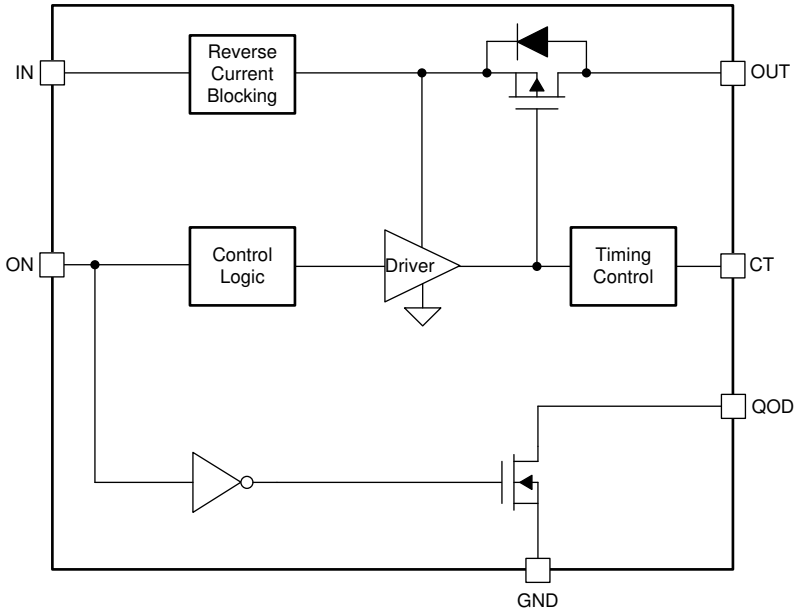
9 Detailed Description

9.1 Overview

The TPS22917x device is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance P-channel MOSFET which reduces the drop out voltage across the device.

The TPS22917x device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT after the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. The TPS22917 is enabled when the voltage applied to the ON pin is pulled above V_{IH}, while the TPS22917L is enabled when the voltage is below V_{IL}.

When power is first applied to VIN, a Smart Pulldown is used to keep the ON pin from floating until system sequencing is complete. After the ON pin is deliberately driven high ($\geq V_{IH}$), the Smart Pulldown is disconnected to prevent unnecessary power loss. 表 9-1 shown then the ON Pin Smart Pulldown is active.

表 9-1. Smart-ON Pulldown

VON	Pulldown
$\leq V_{IL}$	Connected
$\geq V_{IH}$	Disconnected

9.3.2 Turn-On Time (t_{ON}) and Adjustable Slew Rate (CT)

A capacitor to VIN on the CT pin sets the slew rate of V_{OUT}. The CT capacitor voltage ramps until shortly after the switch is turned on and V_{OUT} becomes stable.

Leaving the CT pin open results in the highest slew rate and fastest turn-on time. These values can be found in the Switching Characteristics Table. For slower slew rates the required CT capacitor can be found using 式 1:

$$CT = (\text{Slew Rate}) \div SR_{ON} \quad (1)$$

where

- Slew Rate = desired slew rate (mV/us)
- CT = the capacitance value on the CT pin (pF)
- SR_{ON} = slew rate constant from table [(mV/µs) × pF]

The total turn-on time has a direct correlation to the output slew rate. The fastest turn on times (t_{ON}), with CT pin open, can be found in the *Switching Characteristics*. For slower slew rates, the resulting turn-on time can be found with 式 2:

$$\text{Turn-On time} = CT \times t_{ON} \quad (2)$$

where

- Turn-On Time = total time from enable until V_{OUT} rises to 90% of V_{IN} (µs)
- CT =the capacitance value on the CT pin (pF)
- t_{ON} = Turn-On time constant (µs/pF)

9.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22917x device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD.
- QOD pin connected to VOUT pin using an external resistor R_{QOD}. After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, 式 3 can be used:

$$R_{DIS} = QOD + R_{QOD} \quad (3)$$

  - Where:
  - R_{DIS} = total output discharge resistance (Ω)
  - QOD = internal pulldown resistance (Ω)
  - R_{QOD} = external resistance placed between the VOUT and QOD pins (Ω)

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- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use 式 4.

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L \quad (4)$$

Where:

- t_{FALL} = output fall time from 90% to 10% (µs)
- R_{DIS} = total QOD + R_{QOD} resistance (Ω)
- R_L = output load resistance (Ω)
- C_L = output load capacitance (µF)

9.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN}. Past a certain V_{IN} level, the strength of the R_{PD} is reduced. If there is still remaining charge on the output capacitor, this results in longer fall times. For further information regarding this condition, see the *Setting Fall Time for Shutdown Power Sequencing* section.

9.4 Full-Time Reverse Current Blocking

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold (I_{RCB}) is exceeded, the switch is disabled within t_{RCB}. The Switch remains off and block reverse current as long as the reverse voltage condition exists. After V_{OUT} has dropped below the V_{RCB} release threshold the device turns back on with slew rate control.

9.5 Device Functional Modes

表 9-2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

表 9-2. VOUT Connection

ON	QOD CONFIGURATION	TPS22917 VOUT	TPS22917L VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND (via QOD + R_{QOD})	VIN
L	QOD pin tied to VOUT directly	GND (via QOD)	VIN
L	QOD pin left open	Floating	VIN
H	QOD pin connected to VOUT with R_{QOD}	VIN	GND (via QOD + R_{QOD})
H	QOD pin tied to VOUT directly	VIN	GND (via QOD)
H	QOD pin left open	VIN	Floating

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10 Application and Implementation

Note

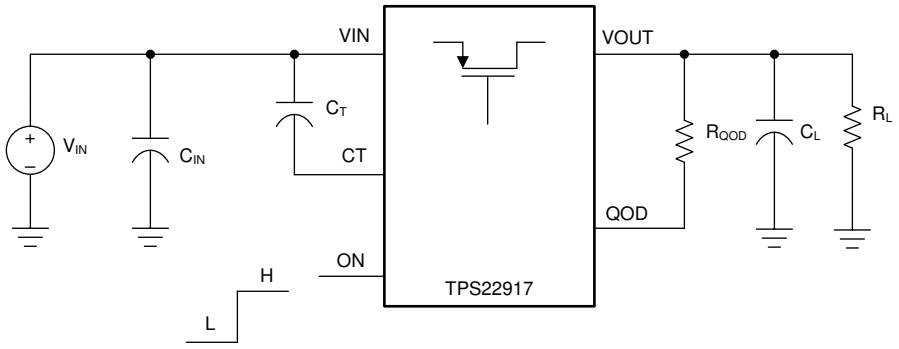
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10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

10.2 Typical Application

This typical application demonstrates how the TPS22917x device can be used to power downstream modules.



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図 10-1. Typical Application Schematic

10.2.1 Design Requirements

For this design example, use the values listed in 表 10-1 as the design parameters:

表 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	3.6 V
Load current / resistance (R_L)	1 kΩ
Load capacitance (C_L)	47 µF
Minimum fall time (t_F)	40 ms
Maximum inrush current (I_{RUSH})	150 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Limiting Inrush Current

Use 式 5 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{RUSH} \div C_L \quad (5)$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_L = capacitance on VOUT (µF)
- Slew Rate = Output Slew Rate during turn on (mV/µs)

After the required slew rate shown in 式 1 can be used to find the minimum CT capacitance

$$CT = SR_{ON} \div (\text{Slew Rate}) \quad (6)$$

$$CT = 1900 \div 3.2 = 594 \text{ pF} \quad (7)$$

To ensure an inrush current of less than 150 mA, choose a CT value greater than 594 pF. An appropriate value must be placed on such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.2.2 Application Curves

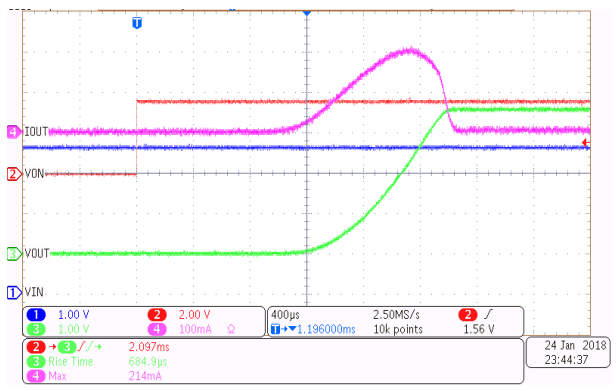


図 10-2. Inrush Current (CT = 470 pF)

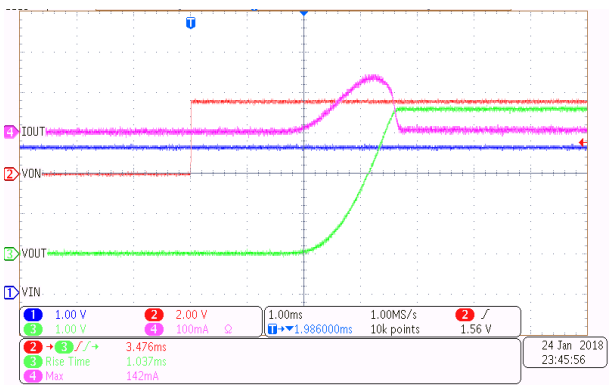


図 10-3. Inrush Current (CT = 1000 pF)

10.2.2.3 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22917x, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

After the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using 式 4:

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L \quad (8)$$

$$R_{DIS} = 630\ \Omega \quad (9)$$

式 3 can then be used to calculate the R_{QOD} resistance needed to acheive a particular discharge value:

$$R_{DIS} = QOD + R_{QOD} \quad (10)$$

$$R_{QOD} = 480\ \Omega \quad (11)$$

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To ensure a fall time greater than, choose an R_{QOD} value greater than 480 Ω.

10.2.2.4 Application Curves

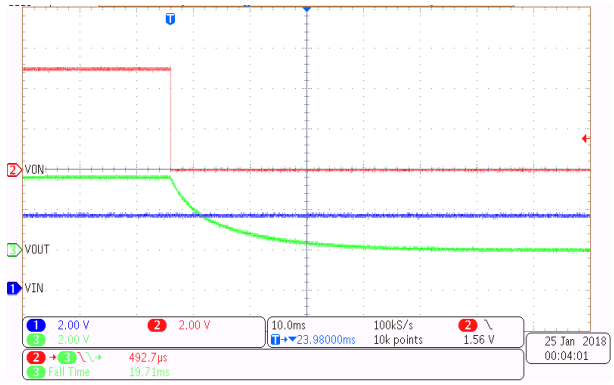


図 10-4. Fall Time (R_{QOD} = 100 Ω)

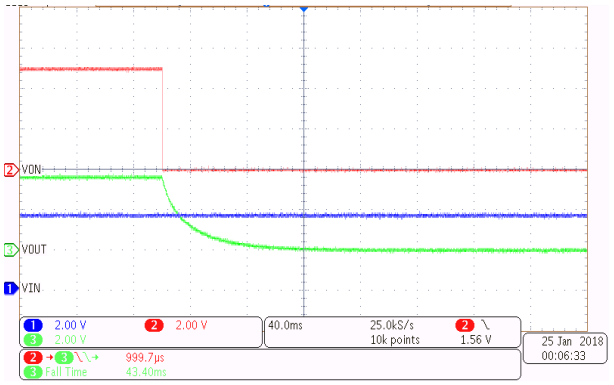


図 10-5. Fall Time (R_{QOD} = 1 kΩ)

11 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

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12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

12.2 Layout Example

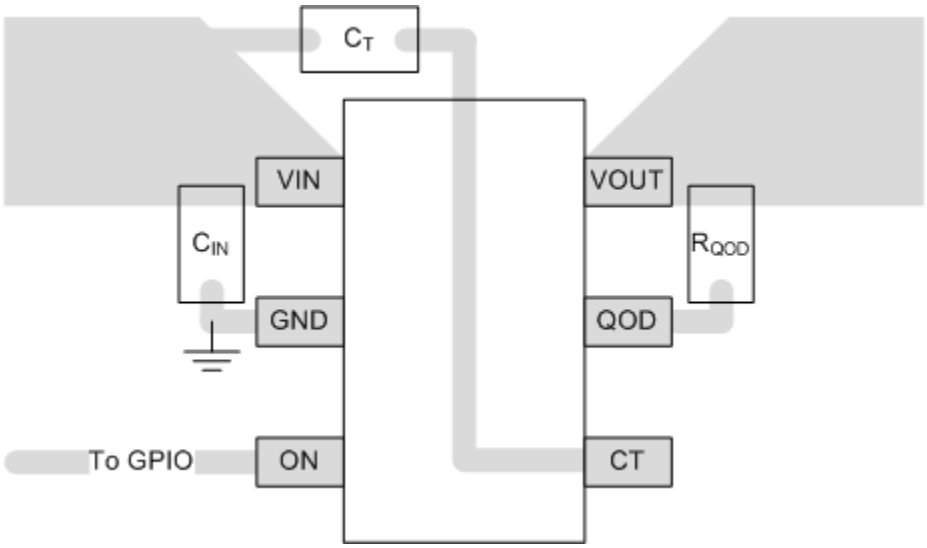


図 12-1. Recommended Board Layout

12.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 式 12:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (12)$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22917x)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the *Thermal Information* section. This parameter is highly dependent upon board layout.

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13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

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13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22917DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1IAF
TPS22917DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	1IAF
TPS22917DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	1IAF
TPS22917DBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	1IAF
TPS22917DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IAF
TPS22917DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	1IAF
TPS22917LDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-45 to 125	2K7F
TPS22917LDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	2K7F
TPS22917LDBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	2K7F
TPS22917LDBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-45 to 125	2K7F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

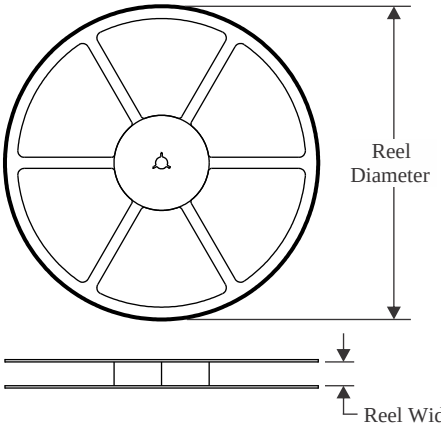
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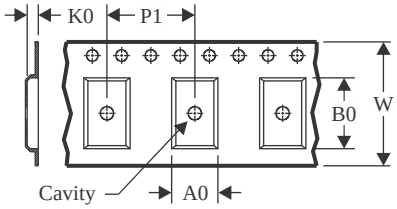
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

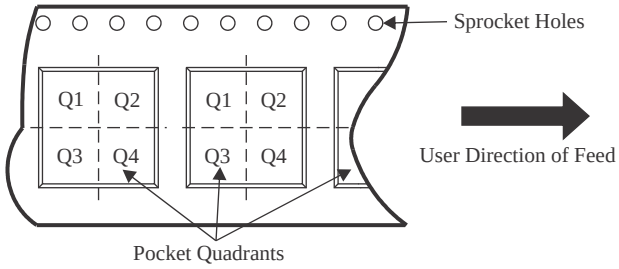


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

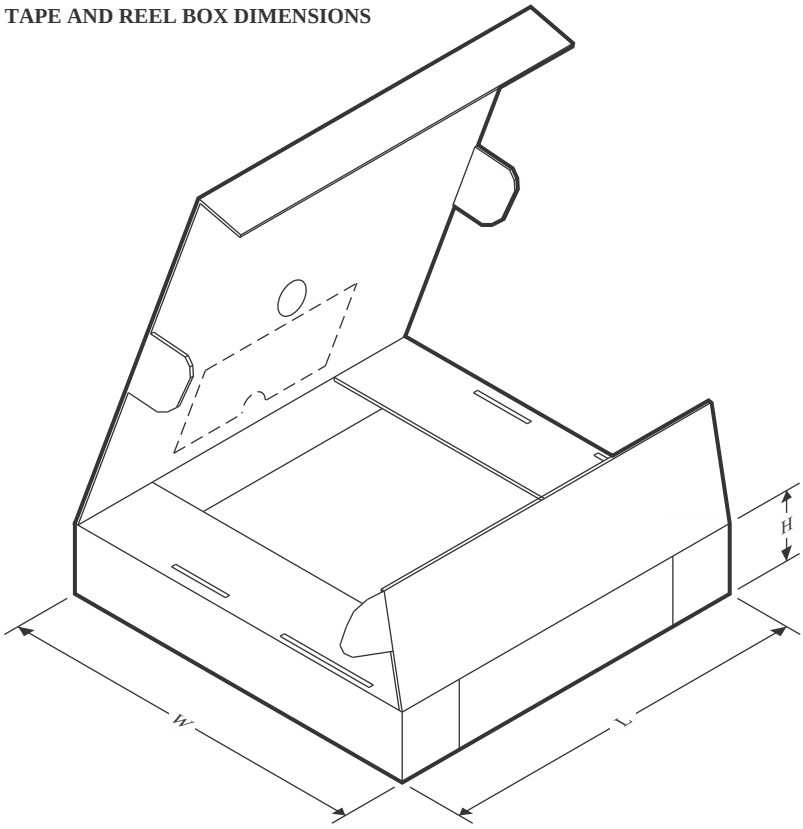
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22917DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22917DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22917DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22917LDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22917LDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22917LDBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

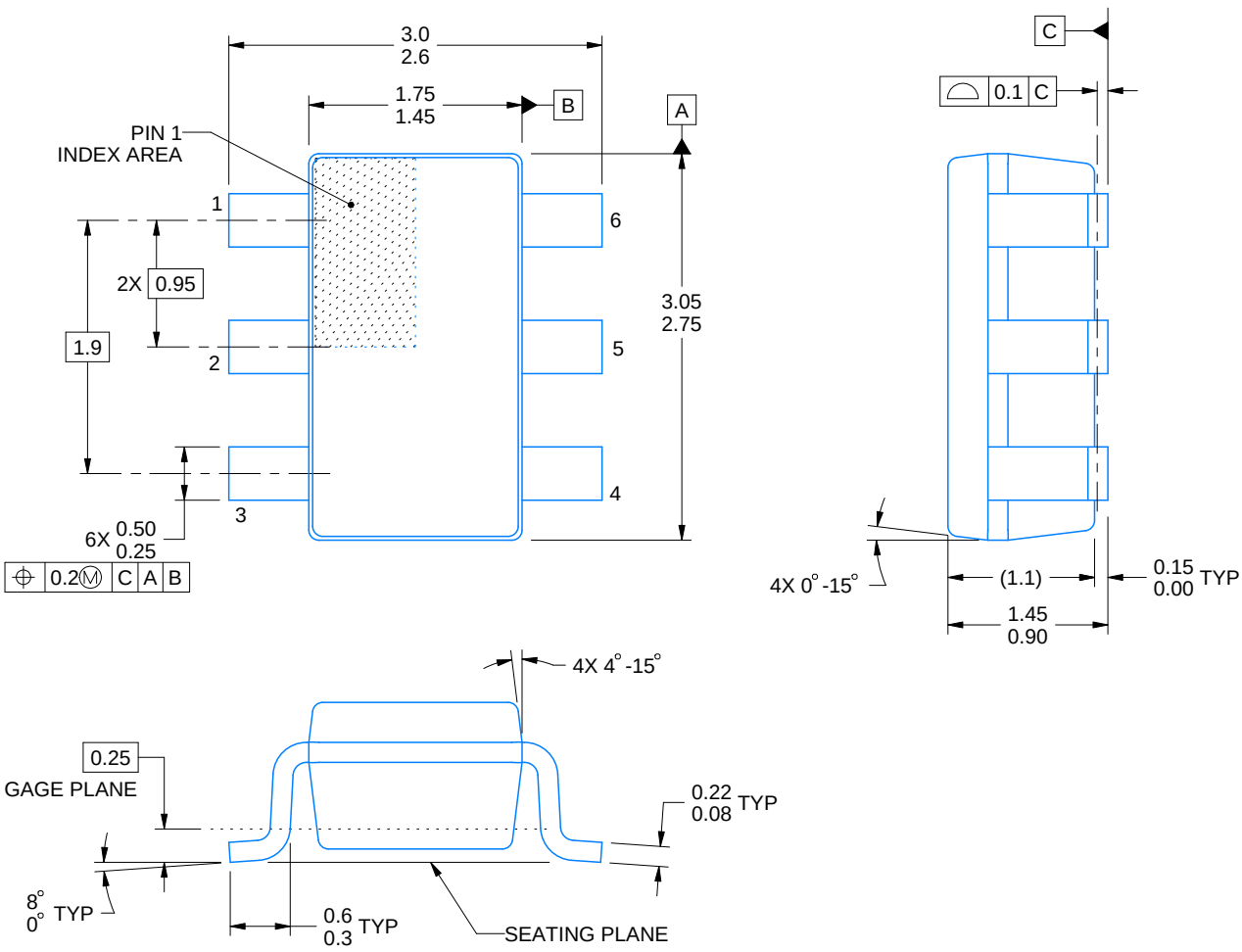
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22917DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
TPS22917DBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22917DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS22917LDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22917LDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22917LDBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

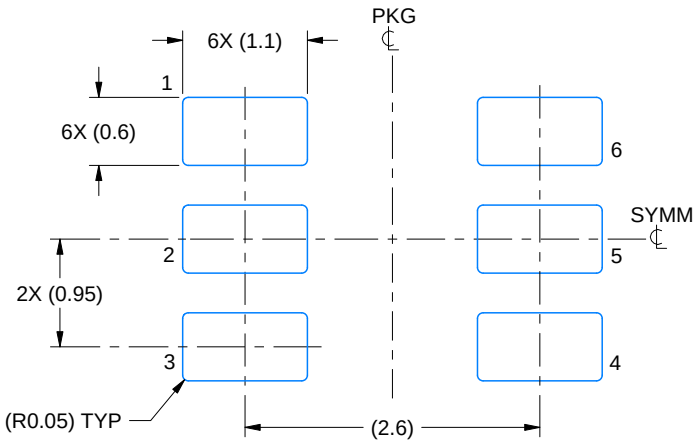
SMALL OUTLINE TRANSISTOR



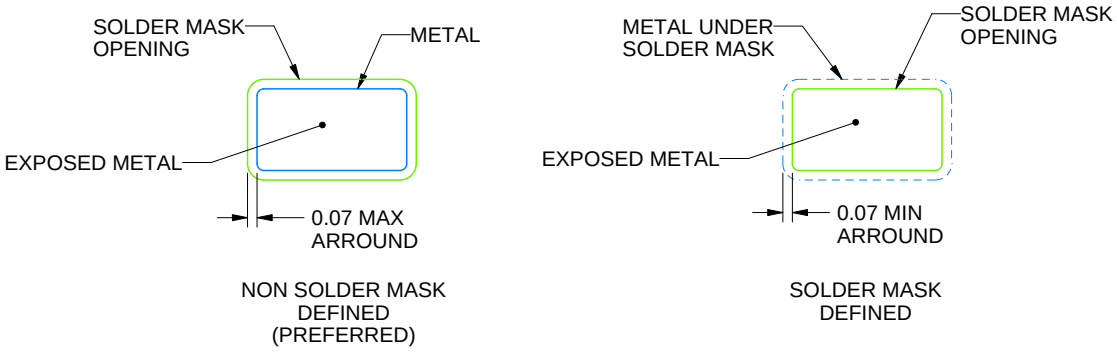
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

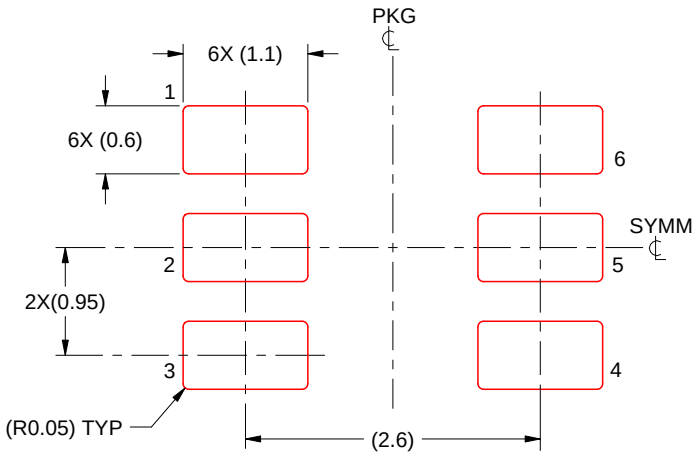


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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