TPS2559 高精度、可変電流制限、パワー・ディストリビューション・スイッチ

1 特長

- 動作範囲：2.5V～6.5V
- $I_{(LIMIT)}$ を 1.2A～4.7A に調整可能 (4.7A で ±4.4%)
- 短絡シャットオフ (標準値)：3.5µs
- ハイサイド MOSFET：13mΩ
- スタンバイ時の最大電源電流：2µA
- ソフト･スタート機能内蔵
- システムレベル ESD 対応：8kV/15kV
- UL 2367 認定 (申請中)

2 アプリケーション

- USB ポート / ハブ
- デジタル･ テレビ
- セット･ トップ･ ボックス
- VoIP 電話

3 概要

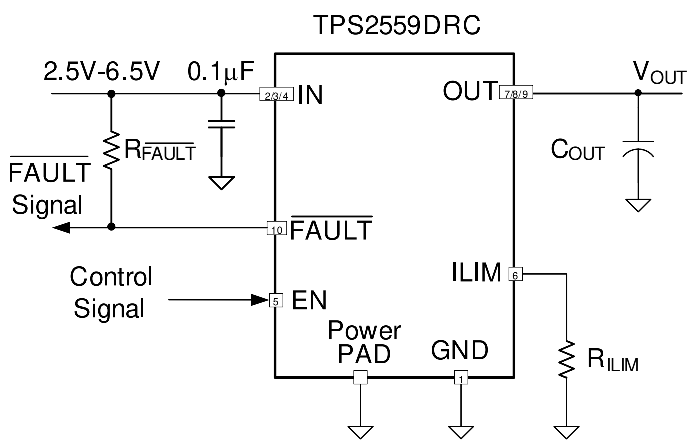
TPS2559 パワー･ ディストリビューション･ スイッチは、低抵抗、高精度の電流制限スイッチが必要なアプリケーション、または大きな容量性負荷の駆動が必要なアプリケーションを対象としています。TPS2559 は、最大 5.5A の連続負荷電流を供給します。グランドとの間に接続された 1 つの抵抗で設定される高精度の電流制限機能も備えています。出力負荷電流が電流制限スレッショルドを超えた場合、定電流モードに切り替えることで、出力電流を安全なレベルに維持します。過負荷状態中、出力電流は $R_{(ILIM)}$ で設定されたレベルに制限されます。継続的な過負荷が発生すると、デバイスはサーマル･ シャットオフに移行し、TPS2559 の損傷を防止します。

電源スイッチの立ち上がりおよび立ち下がり時間は、電源オン / オフ時の電流サージを最小限に抑えるように制御されます。過電流または過熱条件の間、$\overline{\text{FAULT}}$ ロジック出力は LOW をアサートします。

製品情報 (1) (1 ページ)

部品番号	パッケージ	本体サイズ (公称)
TPS2559	VSON (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2014) to Revision A (November 2020) — **Page**

- 文書全体にわたって表と図の採番方法を更新.......... 1
- Added OUT row to Voltage range parameter in *Absolute Maximum Ratings* table.......... 4
- Added T_{stg} row to *Absolute Maximum Ratings* table, moved from *ESD Ratings* table.......... 4
- Changled title of *ESD Ratings* table and updated to current standards.......... 4
- Added *Timing Diagrams* title to section, moved from *Parameter Measurement Information* section to match current standards.......... 7

5 Device Comparison Table

DEVICE	OPERATING RANGE (V)	OCP MODE	ICONT. ADJ. RANGE (A)	$R_{DS(on)}$ (mΩ)	I_{OS} TOLERANCE	PACKAGE: SON-8 (DRB) SOT-23 (DBV) SON-10 (DRC) SON-6 (DRV)
TPS2559	2.5 - 6.5	Auto retry	5.5	13	±4.4% at 4.7 A	DRC
TPS2552/3	2.5 - 6.5	Auto retry	1.2	85 (DBV) 100 (DRV)	±6% at 1.7 A	DBV, DRV
TPS2552/3-1	2.5 - 6.5	Latch off	1.2	85 (DBV) 100 (DRV)	±6% at 1.7 A	DBV, DRV
TPS2554/5 (dual Adjustable)	4.5 - 5.5	Auto retry	2.5	73	±9.7% at 2.8 A	DRC
TPS2556/7	2.5 - 6.5	Auto Retry	5	22	±6.5% at 4.5 A	DRB
TPS2560/61 (dual Channels)	2.5 - 6.5	Auto retry	2.5	44	±7.5% at 2.8 A	DRC
TPS2560A/61A (dual Channels)	2.5 - 6.5	Auto retry	2.5	44	2.1 A to 2.5 A including ±1% $R_{(ILIM)}$	DRC
TPS25200 (with OVP protection)	2.5 - 6.5 (withstand up to 20 V)	Auto retry	2.5	60	±6% at 2.9 A	DRV

6 Pin Configuration and Functions

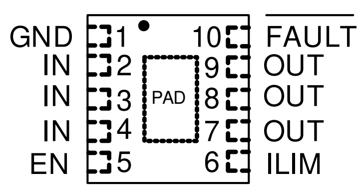


図 6-1. DRC Package, 10-Pin VSON, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1		Ground connection, connect externally to PowerPAD.
IN	2, 3, 4	I	Input voltage, connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the device as possible.
EN	5	I	Enable input, logic high turns on power switch.
ILIM	6	O	External resistor used to set current-limit threshold; recommended. 24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ.
OUT	7, 8, 9	O	Power-switch output.
$\overline{\text{FAULT}}$	10	O	Active-low open-drain output, asserted during over-current or overtemperature conditions.
PowerPAD™	PAD	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Voltage range	IN, EN, ILIM, $\overline{FAULT}$	–0.3	7	V
	OUT	–0.8	7	V
	IN to OUT	–7	7	V
Continuous output current, I_{OUT}	OUT	Internally limited		mA
Continuous $\overline{FAULT}$ sink current			20	mA
ILIM source current		Internally limited		mA
Maximum junction temperature, T_J		–40	OTSD2	°C
Storage temperature range, T_{stg}		–62	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	
		System level (contact/air) (3)	±8000	
			±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Surges per EN61000-4-2, 1999 applied between USB and output ground of the *TPS2559EVM-624 Evaluation Module* user guide (documentation available on the web.) These were the test levels, not the failure threshold.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage, IN	2.5	6.5	V
V_{EN}	Input voltage, EN	0	6.5	V
I_{OUT}	Continuous output current of OUT		5.5	A
	Continuous $\overline{FAULT}$ sink current		10	mA
$R_{(ILIM)}$	Recommended resistor limit range (1)	24.9	100	kΩ
T_J	Operating junction temperature	-40	125	°C

(1) $R_{(ILIM)}$ is the resistor from ILIM pin to GND and ILIM pin can be shorted to GND.

7.4 Thermal Information

THERMAL METRIC[1]		TPS2559 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

conditions are –40°C ≤ T_J ≤ 125°C, 2.5 V ≤ V_{IN} ≤ 6.5 V, $V_{(EN)}$ = V_{IN}, $R_{(ILIM)}$ = 49.9kΩ; positive current are into pins; typical value is at 25°C; all voltages are with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Input/output resistance[1]	T_J = 25°C		13	16	mΩ
		-40°C ≤ T_J ≤ 125°C			21	
ENABLE INPUT EN						
	EN turn-on/off threshold		0.66		1.1	V
	Hysteresis			55[2]		mV
$I_{(EN)}$	Input current	$V_{(EN)}$ = 0 V or $V_{(EN)}$ = 6.5 V	–1		1	µA
CURRENT LIMIT						
I_{OS}	OUT short-circuit current limit	$R_{(ILIM)}$ = 24.9 kΩ	4490	4731	4900	mA
		$R_{(ILIM)}$ = 44.2 kΩ	2505	2665	2775	
		$R_{(ILIM)}$ = 49.9 kΩ	2215	2360	2460	
		$R_{(ILIM)}$ = 61.9 kΩ	1780	1902	1990	
		$R_{(ILIM)}$ = 100 kΩ	1080	1176	1245	
		ILIM pin short to GND ($R_{(ILIM)}$ = 0)	5860	6650	7460	
SUPPLY CURRENT						
$I_{(IN\_OFF)}$	Disabled, IN supply current	$V_{(EN)}$ = 0 V, no load on OUT		0.1	2	µA
$I_{(IN\_ON)}$	Enabled, IN supply current	$R_{(ILIM)}$ = 100 kΩ, no load on OUT		97	125	µA
		$R_{(ILIM)}$ = 24.9 kΩ, no load on OUT		107	135	
$I_{(REV)}$	Reverse leakage current	V_{OUT} = 6.5 V, V_{IN} = 0 V, T_J = 25°C, measure I_{OUT}		0.01	1	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{UVLO}	IN rising UVLO threshold voltage			2.36	2.45	V
	Hysteresis			35[2]		mV
$\overline{FAULT}$						
V_{OL}	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			180	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 6.5 V			1	µA
THERMAL SHUTDOWN						
OTSD2	Thermal shutdown threshold		155			°C
OTSD1	Thermal shutdown threshold in current-limit		135			

7.5 Electrical Characteristics (continued)

conditions are –40°C ≤ T_J ≤ 125°C, 2.5 V ≤ V_{IN} ≤ 6.5 V, $V_{(EN)}$ = V_{IN}, $R_{(ILIM)}$ = 49.9kΩ; positive current are into pins; typical value is at 25°C; all voltages are with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Hysteresis			20 [(2)]		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.6 Timing Requirements

conditions are –40°C ≤ T_J = ≤ 125°C, 2.5 V ≤ V_{IN} ≤ 6.5 V, $V_{(EN)}$ = V_{IN}, $R_{(ILIM)}$ = 49.9kΩ; positive current are into pins; typical value is at 25°C; all voltages are with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
t_r	OUT voltage rise time	V_{IN} = 6.5 V	C_L = 1 µF, R_L = 100 Ω, see 図 7-2	2.6	3.65	5.2	ms
		V_{IN} = 2.5 V		1.3	2.6	3.9	
t_f	OUT voltage fall time	V_{IN} = 6.5 V		0.7	0.95	1.3	
		V_{IN} = 2.5 V		0.42	0.78	1.04	
ENABLE INPUT EN							
t_{on}	OUT voltage turn-on time	C_L = 1 µF, R_L = 100 Ω, see 図 7-3				15	ms
t_{off}	OUT voltage turn-off time					8	
CURRENT LIMIT							
t_{IOS}	Short-circuit response time[(1)]	V_{IN} = 5 V, R_{SHORT} = 50 mΩ, see 図 7-4			3.5[(1)]		µs
$\overline{\text{FAULT}}$							
	$\overline{\text{FAULT}}$ deglitch	$\overline{\text{FAULT}}$ assertion or de-assertion resulting from overcurrent condition		6	9.5	13	ms

(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Timing Diagrams

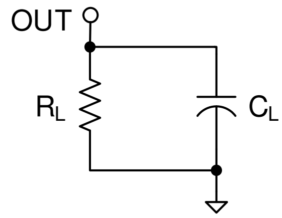


図 7-1. Output Rise/Fall Time Test Load

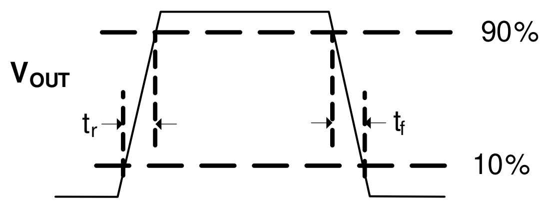


図 7-2. Power-On and Off Timing

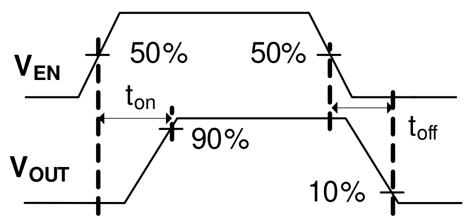


図 7-3. Enable Timing, Active High Enable

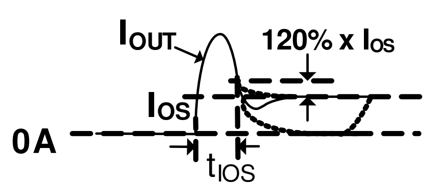


図 7-4. Output Short-Circuit Parameters

7.8 Typical Characteristics

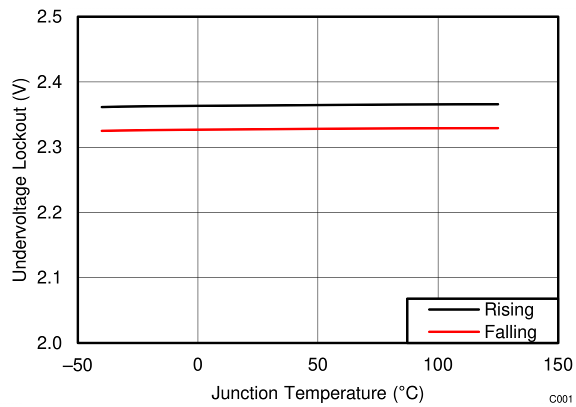
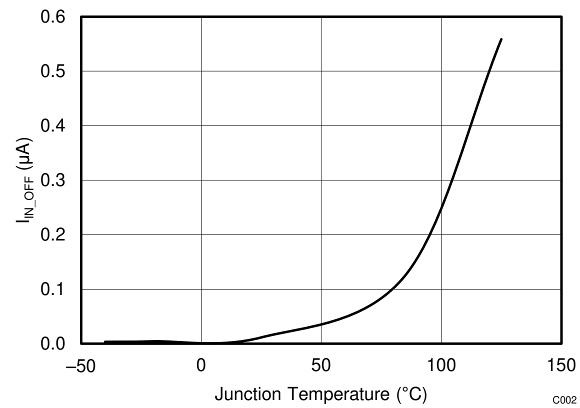
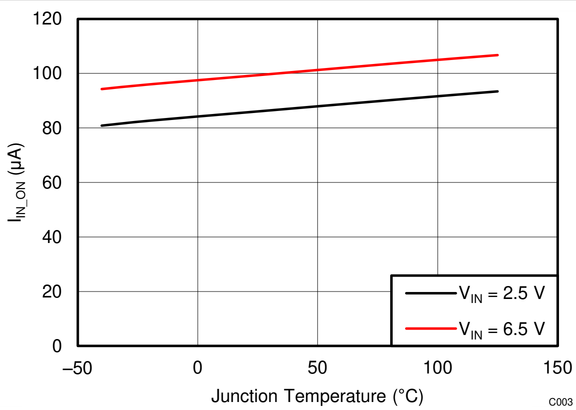


図 7-5. Undervoltage Lockout (UVLO) vs Temperature



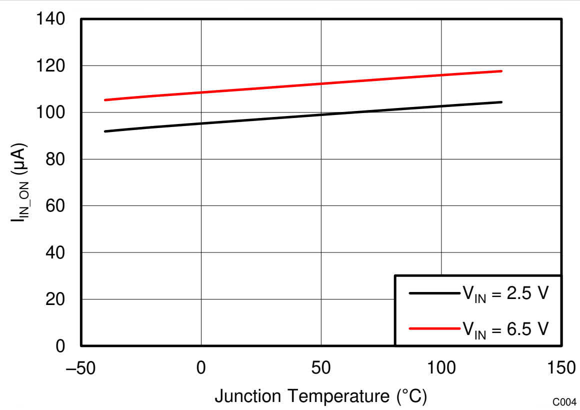
V_{IN} = 6.5 V

図 7-6. Supply Current, Output Disabled (I_{IN_OFF}) vs Temperature



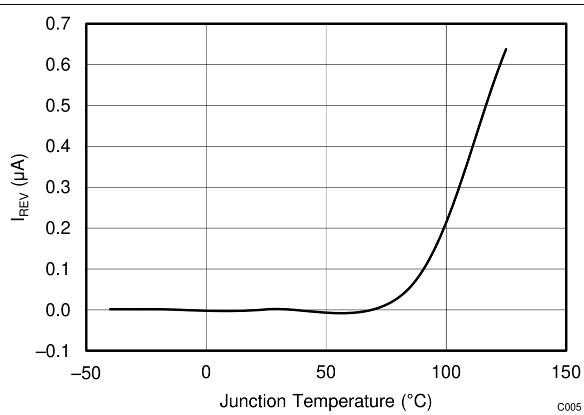
$R_{(ILIM)}$ = 100 kΩ

図 7-7. Supply Current, Output Enabled (I_{IN_ON}) vs Temperature



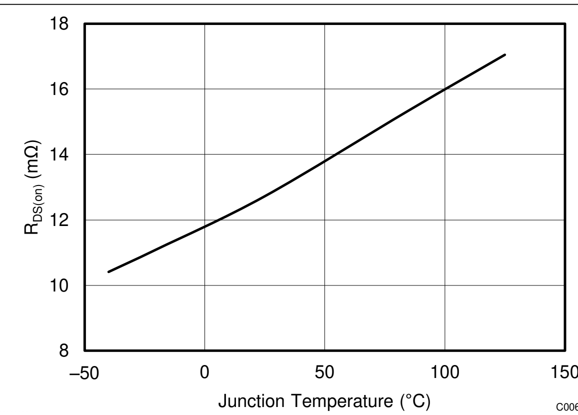
$R_{(ILIM)}$ = 24.9 kΩ

図 7-8. Supply Current, Output Enabled (I_{IN_ON}) vs Temperature



V_{OUT} = 6.5 V

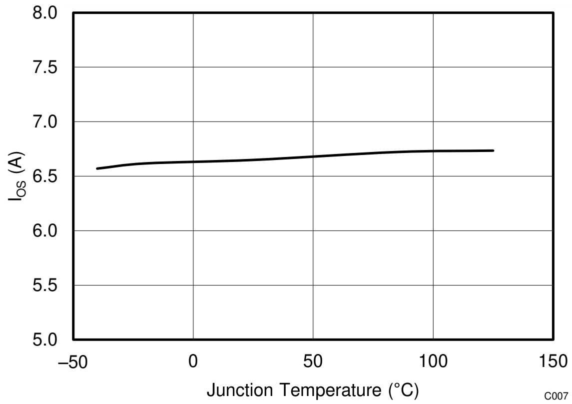
図 7-9. Reverse Leakage Current (I_{REV}) vs Temperature



V_{IN} = 5 V

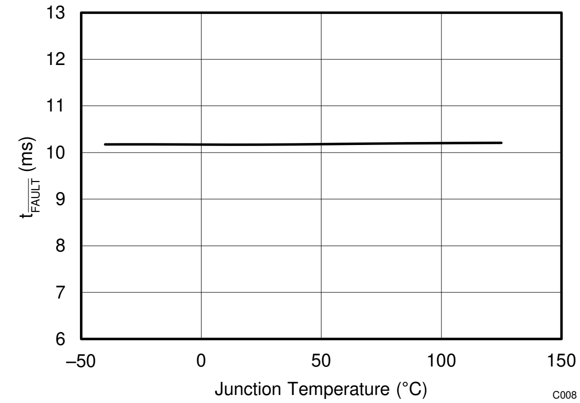
図 7-10. Input/Output Resistance ($R_{DS(on)}$) vs Temperature

7.8 Typical Characteristics (continued)



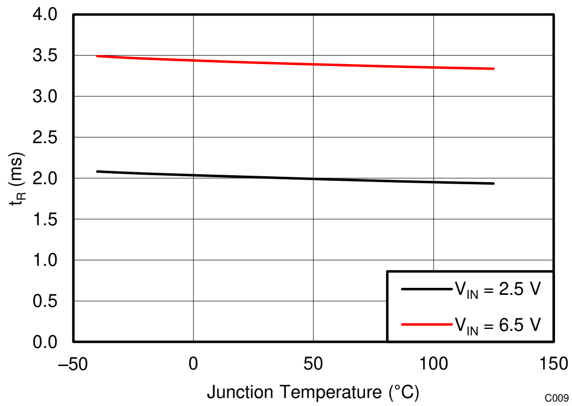
V_{IN} = 6.5 V, ILIM pin short to GND

図 7-11. Short-Circuit Current (I_{OS}) vs Temperature



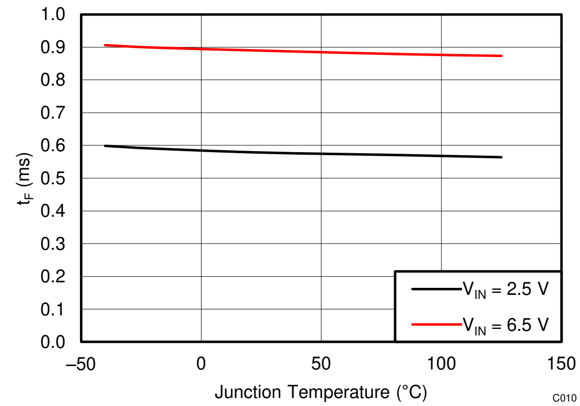
$V_{(\overline{FAULT})}$ = 2.5 V

図 7-12. Deglitch Time ($t_{\overline{FAULT}}$) vs Temperature



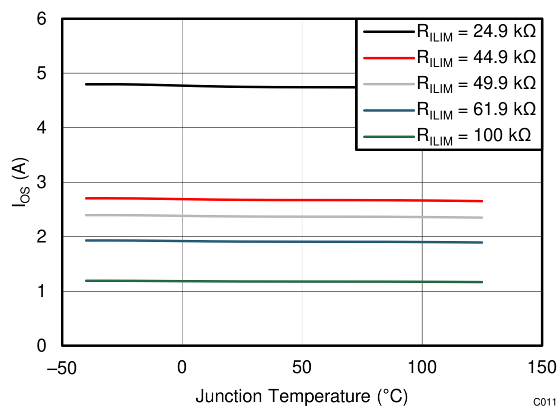
C_{OUT} = 1 µF, $R_{(LOAD)}$ = 100 Ω

図 7-13. Output Rise Time (t_R) vs Temperature



C_{OUT} = 1 µF, $R_{(LOAD)}$ = 100 Ω

図 7-14. Output Fall Time (t_F) vs Temperature



V_{IN} = 6.5 V

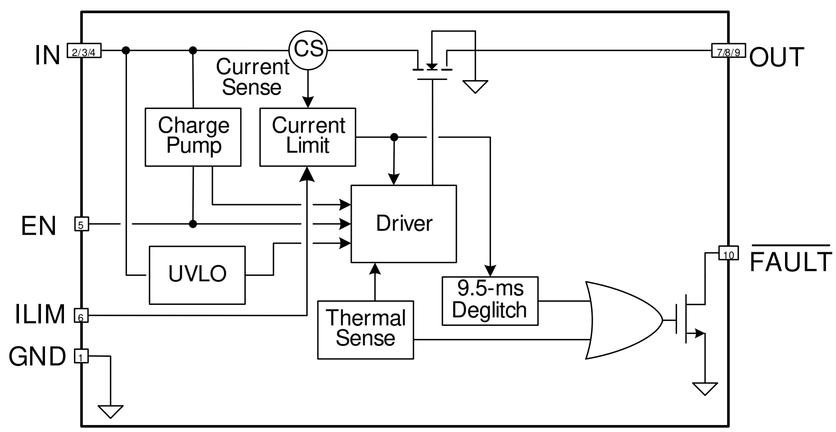
図 7-15. Short-Circuit Current (I_{OS}) vs Temperature

8 Detailed Description

8.1 Overview

The TPS2559 is a current-limited, power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered. This device allows the user to program the current-limit via an external resistor and the maximum continuous output current up to 5.5 A. This device incorporates an internal charge pump and the gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. The TPS2559 limits the output current to the programmed current-limit threshold IOS during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to IOS reduces the output voltage at OUT because N-channel MOSFET is no longer fully enhanced.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Thermal Sense

The TPS2559 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS2559 device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an over-current condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS2559 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 20°C. The TPS2559 continues to cycle off and on until the fault is removed.

8.3.2 Overcurrent Protection

The TPS2559 responds to overcurrent conditions by limiting their output current to IOS. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} × R_{LOAD}). Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2559 ramps the output current to I_{OS}. The TPS2559 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle (see 図 9-9).

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see 図 7-4). The response speed and shape will vary with the overload level, input circuit, and rate of application. The current-limit response will vary between simply settling to I_{OS}, or turnoff and controlled return to IOS. Similar to the previous case, the TPS2559 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS2559 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS2559 cycles on/off until the overload is removed (see 図 9-10).

8.3.3 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-current or over-temperature condition. The TPS2559 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS2559 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for over-current (9-ms typ.) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions. The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an over-temperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an over-temperature event.

8.4 Device Functional Modes

8.4.1 Operation with V_{IN} Undervoltage Lockout (UVLO) Control

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

8.4.2 Operation with EN Control

The logic enable controls the power switch and device supply current. The supply current is reduced to less than 2-µA when a logic low is present on EN. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2559 current limited power switch uses N-channel MOSFETs in applications requiring up to 5.5 A of continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

The TPS2559 power switch is used to protect the up-stream power supply when the output is overloaded.

9.2 Typical Application

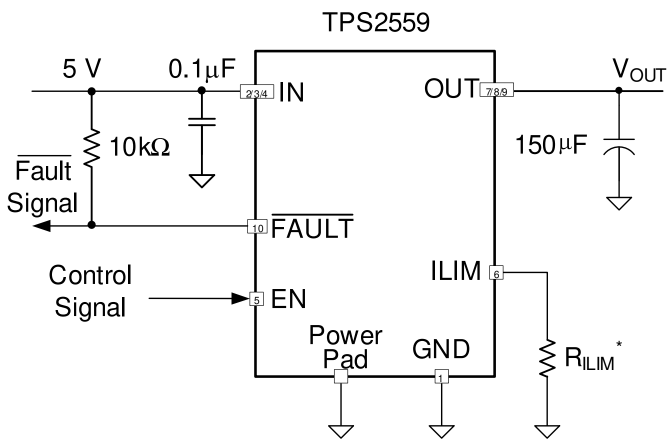


図 9-1. Typical TPS2559 Power Switch

Use the I_{OS} in the *Electrical Characteristics* table or I_{OS} in 式 1 to select the R_{ILIM}.

9.2.1 Design Requirements

表 9-1 lists the input parameters for this design example.

表 9-1. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input operation voltage	5 V
Rating current	3 A or 4.5 A
Minimum current limit	3 A
Maximum current limit	5 A

When choosing a power switch, there are several general steps:

1. Determine what is the power rail, 3.3 V or 5 V, and then choose the operation range of the power switch that can cover the power rail voltage range.
2. Determine what is the normal operation current. For example, the maximum allowable current drawn by portable equipment for a USB 2.0 port is 500 mA, so the normal operation current is 500 mA and the minimum current limit of power switch must exceed 500 mA to avoid false trigger during normal operation.
3. Determine what is the maximum allowable current provided by up-stream power, and then decide the maximum current limit of the power switch that must lower it to ensure the power switch can protect the up-stream power when an overload is encountered at the output of the power switch.

Note

Choosing power switch with tighter current limit tolerance can loosen the up-stream power-supply design.

9.2.2 Detailed Design Procedure

9.2.2.1 Step-by-Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

- Normal input operation voltage
- Rating current
- Minimum current limit
- Maximum current limit

9.2.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage undershoot from exceeding the UVLO of other load share one power rail with TPS2559 or overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output to reduce the undershoot, which caused by the inductance of the output power bus just after a short has occurred and the TPS2559 has abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges.

9.2.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS2559 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for $R_{(ILIM)}$ is 24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ to ensure stability of the internal regulation loop.

When ILIM pin short to GND (single point failure), maximum current limit is less than 8 A over temperature and process variation.

Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for $R_{(ILIM)}$. The equations and the graph below can be used to estimate the minimum and maximum variation of the current-limit threshold for a predefined resistor value within $R_{(ILIM)}$ is 24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ. This variation is an approximation only and does not take into account, for example, the resistor tolerance. For examples of more-precise variation of I_{OS} refer to the current-limit section of the *Electrical Characteristics* table.

$$I_{OS\,max}(mA) = \frac{121635\ V}{{R_{(ILIM)}}^{1.0013} k\Omega} + 36$$

$$I_{OSnom}(mA) = \frac{118079\ V}{{R_{(ILIM)}}^{1.0008} k\Omega}$$

$$I_{OS\,min}(mA) = \frac{113325\ V}{{R_{(ILIM)}}^{1.0010} k\Omega} - 47 \qquad (1)$$

$24.9\ k\Omega \le R_{(ILIM)} \le 100\ k\Omega$

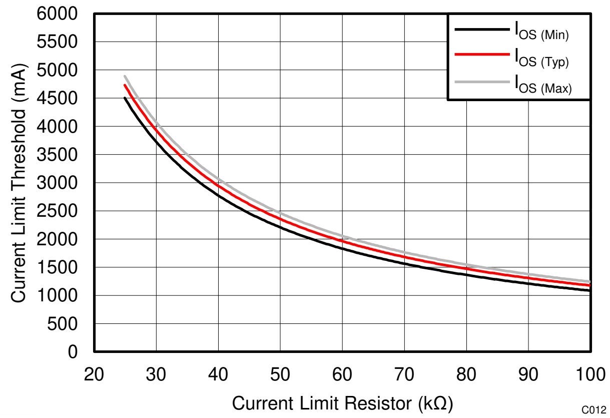


図 9-2. Current-Limit vs $R_{(ILIM)}$

9.2.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 3 A must be delivered to the load so that the minimum desired current-limit threshold is 3000 mA. Use the I_{OS} equations and 図 9-2 to select $R_{(ILIM)}$.

$$I_{OS\,min}(mA) = 3000\ mA$$

$$I_{OS\,min}(mA) = \frac{113325\ V}{R_{(ILIM)}{}^{1.0010}k\Omega} - 47$$

$$R_{(ILIM)}(k\Omega) = \left(\frac{113325}{I_{OS(min)} + 47}\right)^{\frac{1}{1.0010}} = \left(\frac{113325}{3000 + 47}\right)^{\frac{1}{1.0010}} = 37.06\ k\Omega \tag{2}$$

Select the closest 1% resistor less than the calculated value: $R_{(ILIM)}$ = 36.5 kΩ. This sets the minimum current-limit threshold at 3016 A.

$$I_{OS\,min}(mA) = \frac{113325\ V}{R_{(ILIM)}{}^{1.0010}k\Omega} - 47 = \frac{113325}{(36.5 \times 1.01)^{1.0010}} - 47 = 3016\ mA \tag{3}$$

Use the I_{OS} equations, Figure 9-2, and the previously calculated value for $R_{(ILIM)}$ to calculate the maximum resulting current-limit threshold.

$$I_{OS\,max}(mA) = \frac{121635}{R_{(ILIM)}{}^{1.0013}} + 36 = \frac{121635}{(36.5 \times 0.99)^{1.0013}} + 36 = 3387\ mA \tag{4}$$

The resulting maximum current-limit threshold minimum is 3016 mA and maximum is 3387 mA with a 36.5 kΩ ± 1%.

9.2.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 5A must be delivered to the load so that the minimum desired current-limit threshold is 5000 mA. Use the I_{OS} equations and 図 9-2 to select $R_{(ILIM)}$.

$$I_{OS\,max}(mA) = 5000\ mA$$

$$I_{OS\,max}(mA) = \frac{121635}{R_{(ILIM)}{}^{1.0013} k\Omega} + 36$$

$$R_{(ILIM)}(k\Omega) = \left(\frac{121635}{I_{OS(max)}}\right)^{\frac{1}{1.0013}} = \left(\frac{121635}{5000 - 36}\right)^{\frac{1}{1.0013}} = 24.4\ k\Omega \tag{5}$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 24.9 kΩ. This sets the maximum current-limit threshold at 4950 A.

$$I_{OS\,max}(mA) = \frac{121635}{R_{(ILIM)}{}^{1.0013} k\Omega} + 36 = \frac{121635}{(24.9 \times 0.99)^{1.0013}} + 36 = 4950\ mA \tag{6}$$

Use the I_{OS} equations, Figure 9-2, and the previously calculated value for $R_{(ILIM)}$ to calculate the minimum resulting current-limit threshold.

$$I_{OS\,min}(mA) = \frac{113325}{R_{(ILIM)}{}^{1.0010}} - 47 = \frac{113325}{(24.9 \times 1.01)^{1.0010}} - 47 = 4445\ mA \tag{7}$$

The resulting minimum current-limit threshold minimum is 4445 mA and maximum is 4950 mA with a 24.9 kΩ ± 1%.

9.2.2.6 Accounting for Resistor Tolerance

The previous sections described the selection of $R_{(ILIM)}$ given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2559 is bounded by an upper and lower tolerance centered on a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. 表 9-2 lists a process that accounts for worst-case resistor tolerance assuming 1% resistor values.

Step one follows the selection process outlined in the application examples above.

Step two determines the upper and lower resistance bounds of the selected resistor.

Step three uses the upper and lower resistor bounds in the IOS equations to calculate the threshold limits.

It is important to use tighter tolerance resistors, that is, 0.5% or 0.1%, when precision current limiting is desired.

表 9-2. Common $R_{(ILIM)}$ Resistor Selections

DESIRED NOMINAL CURRENT LIMIT (mA)	IDEAL RESISTOR (kΩ)	CLOSEST 1% RESISTOR (kΩ)	RESISTOR TOLERANCE		ACTUAL LIMITS		
			1% LOW (kΩ)	1% HIGH (kΩ)	I_{OS} MIN (mA)	I_{OS} NOM (mA)	I_{OS} MAX (mA)
1250	94.1	93.1	92.2	94	1153	1264	1348
1500	78.4	78.7	77.9	79.5	1372	1495	1588
1750	67.2	66.5	65.8	67.2	1633	1770	1874
2000	58.8	59	58.4	59.6	1847	1995	2107
2250	52.3	52.3	51.8	52.8	2090	2551	2373
2500	47.1	47.5	47	48	2306	2478	2610
2750	42.8	43.2	42.8	43.6	2541	2725	2866
3000	39.2	39.2	38.8	39.6	2805	3003	3155
3250	36.2	36.5	36.1	36.9	3016	3226	3386
3500	33.6	34	33.7	34.3	3241	3463	3633
3750	31.4	31.6	31.3	31.9	3491	3726	3907
4000	29.4	29.4	29.1	29.7	3757	4005	4197
4250	27.7	28	27.7	28.3	3947	4206	4405
4500	26.1	26.1	25.8	26.4	4238	4512	4724
4750	24.8	24.9	24.7	25.1	4445	4730	4950

9.2.2.7 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$P_D = r_{DS(on)} \times I_{OUT}{}^2$

Where:

P_D = Total power dissipation (W)
$r_{DS(on)}$ = Power switch on-resistance (Ω)
I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$T_J = P_D \times \theta_{JA} + T_A$

Where:

T_A = Ambient temperature (°C)
θ_{JA} = Thermal resistance (°C/W)
P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA} and thermal resistance is highly dependent on the individual package and board layout.

9.2.2.8 Auto-Retry

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{\text{FAULT}}$ pulls low EN. The part is disabled when EN is pulled below the turn-off threshold, and $\overline{\text{FAULT}}$ goes high impedance allowing $C_{(RETRY)}$ to begin charging. The part re-enables when the voltage on EN reaches the turn-on threshold. The part will continue to cycle in this manner until the fault condition is removed. The auto-retry cycling time is determined by the resistor/capacitor time constant, TPS2559 turn on time and $\overline{\text{FAULT}}$ deglitch time (see 図 9-13).

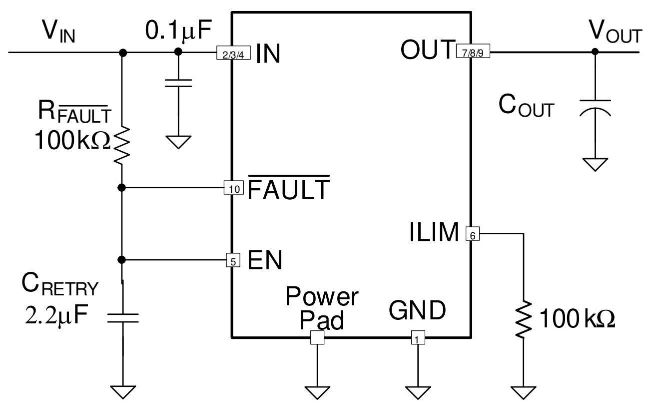


図 9-3. Auto-Retry Circuit

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. 図 9-4 shows how an external logic signal can drive EN through $R_{(\overline{FAULT})}$ and maintain auto-retry functionality. The resistor, capacitor time constant determines the auto-retry time-out period.

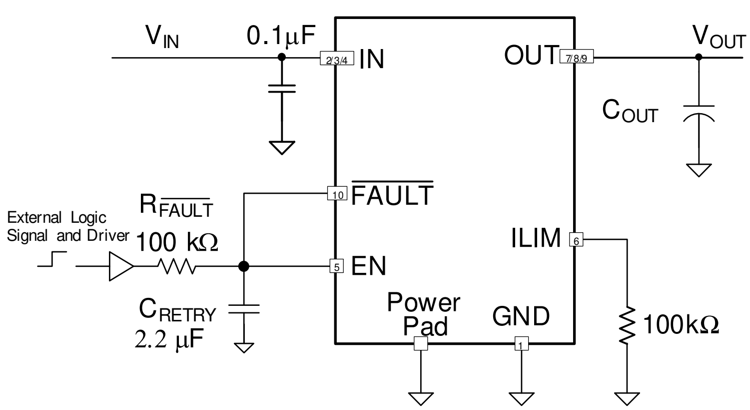


図 9-4. Auto-Retry Circuit with External EN Signal

See the *A Power-Distribution Switch With Latched OvercurrentProtection* application report for how to implement latch-off.

9.2.2.9 Two-Level Current-Limit

Some applications require different current-limit thresholds depending on external system conditions. 図 9-5 shows an implementation for an externally-controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see the *Programming the Current-Limit Threshold* section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND (see 図 9-14 and 図 9-15). Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

Note

ILIM must never be driven directly with an external signal.

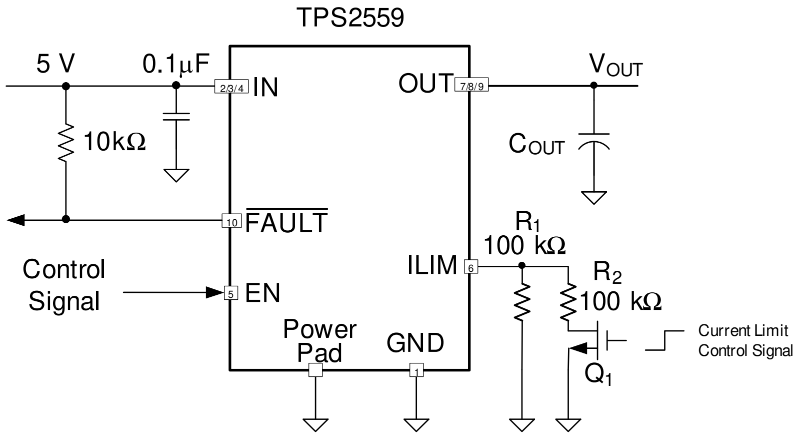


図 9-5. Two-Level Current-Limit Circuit

9.2.3 Application Curves

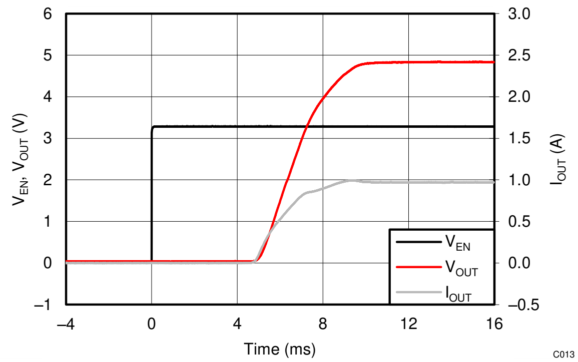


図 9-6. Output Rise With 150 µF // 5 Ω

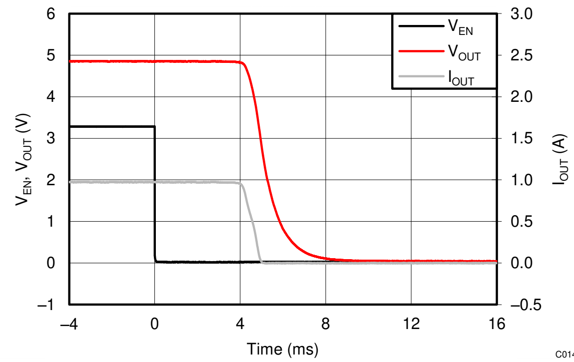


図 9-7. Output Fall With 150 µF // 5 Ω

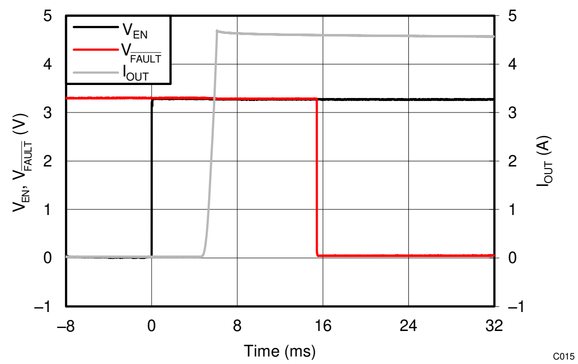


図 9-8. Enable Into Output Short

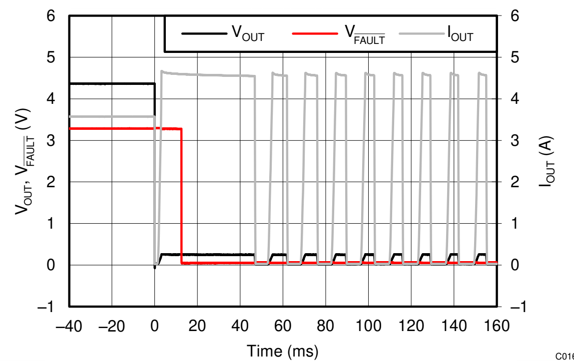


図 9-9. Full Load to Output Short Transient Response

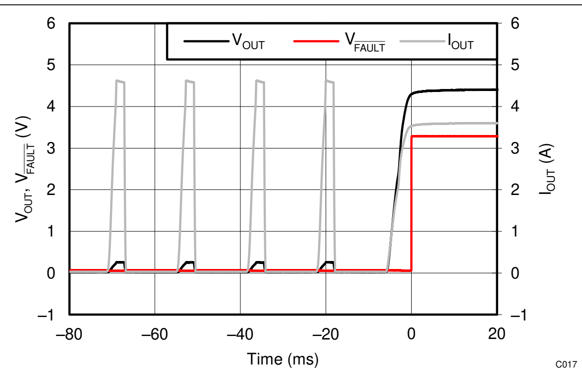


図 9-10. Output Short to Full Load Recovery Response

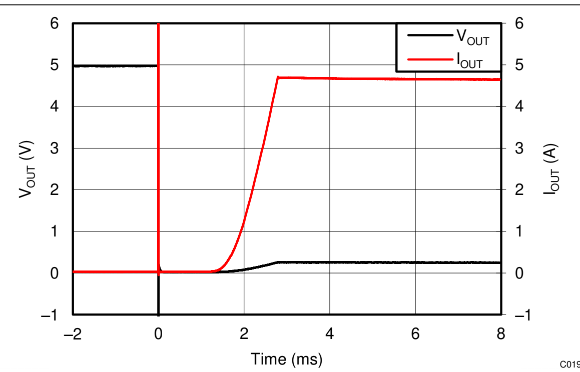


図 9-11. 50-mΩ Hot-Short

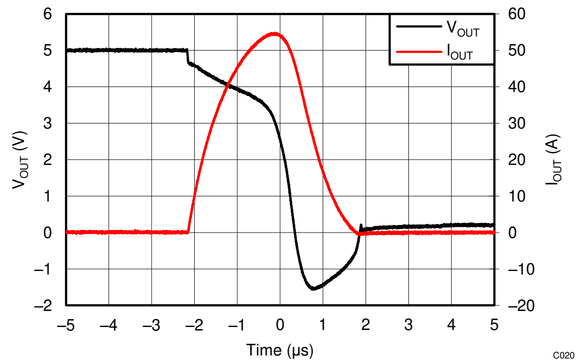


図 9-12. 50-mΩ Hot-Short Response Time

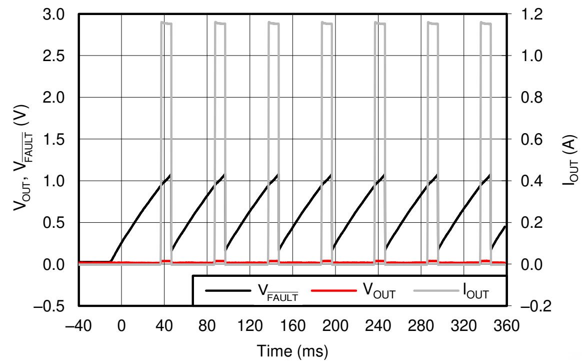


図 9-13. Auto-Retry Cycle

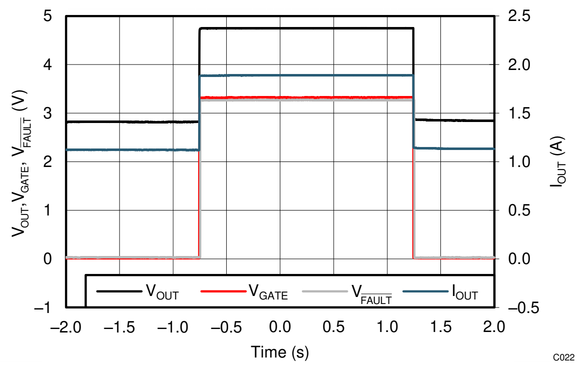


図 9-14. Two-Level Current Limit With R_{LOAD} = 2.5 Ω

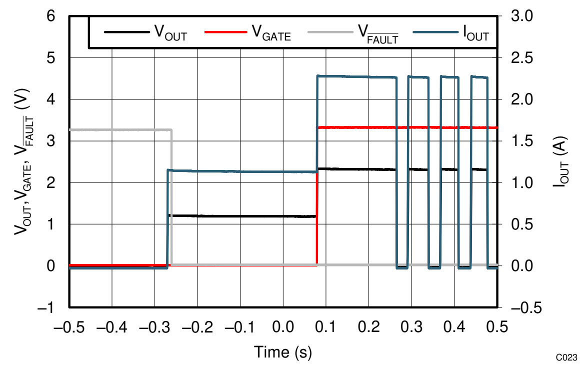


図 9-15. Two-Level Current Limit With R_{LOAD} = 1 Ω

10 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 2.5 V to 6.5 V. The current capability of the power supply should exceed the maximum current limit of the power switch.

11 Layout

11.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- Placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output.
- The traces routing the R_{ILIM} resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

11.2 Layout Example

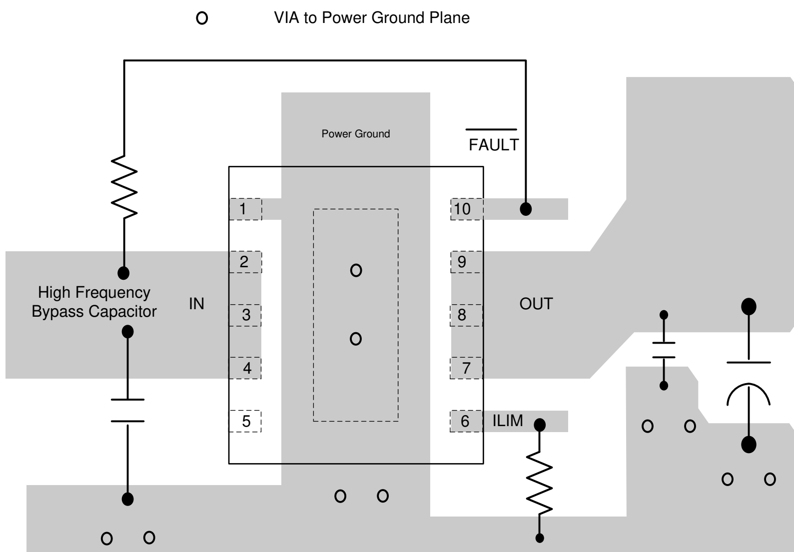


図 11-1. TPS2559 Board Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2559DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCR.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCRG4.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559
TPS2559DRCT.B	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2559

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2559 :

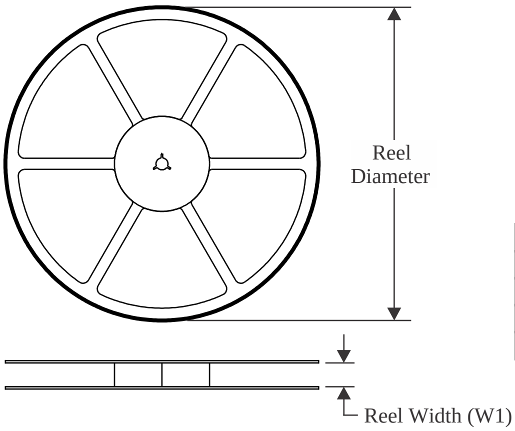
- Automotive : TPS2559-Q1

NOTE: Qualified Version Definitions:

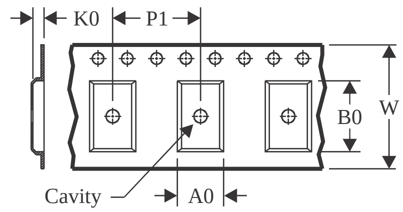
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

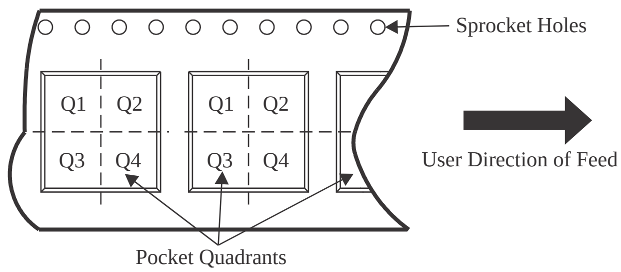


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

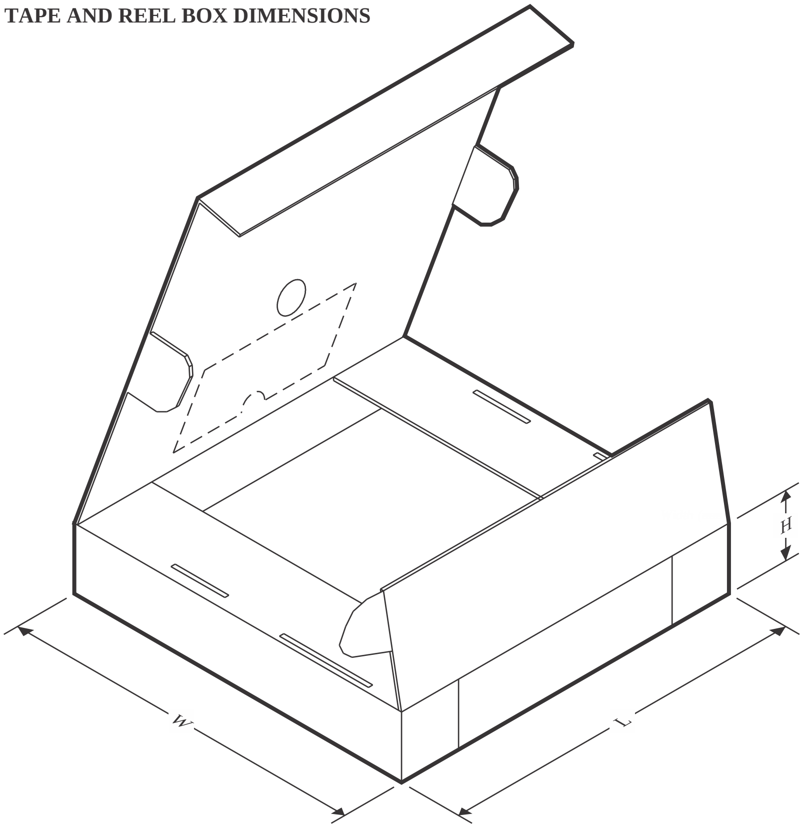
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2559DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2559DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2559DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2559DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2559DRCRG4	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2559DRCT	VSON	DRC	10	250	210.0	185.0	35.0

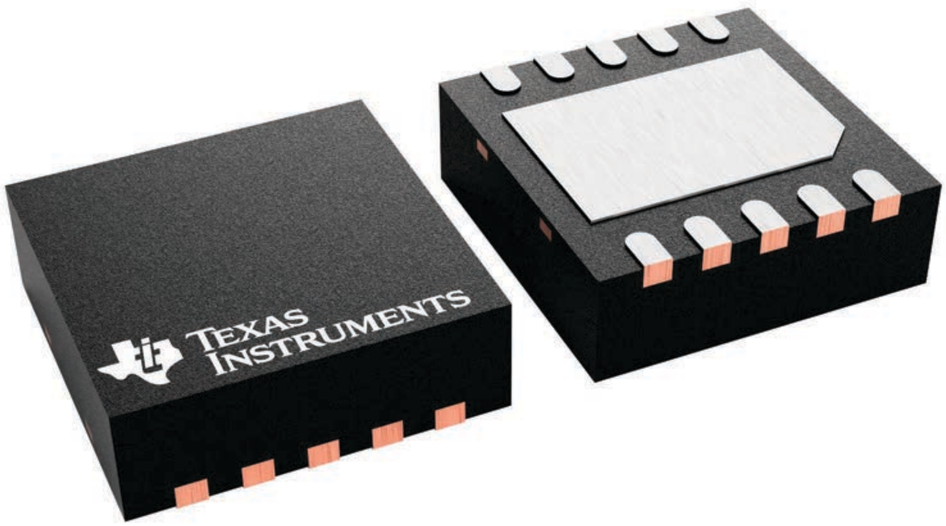
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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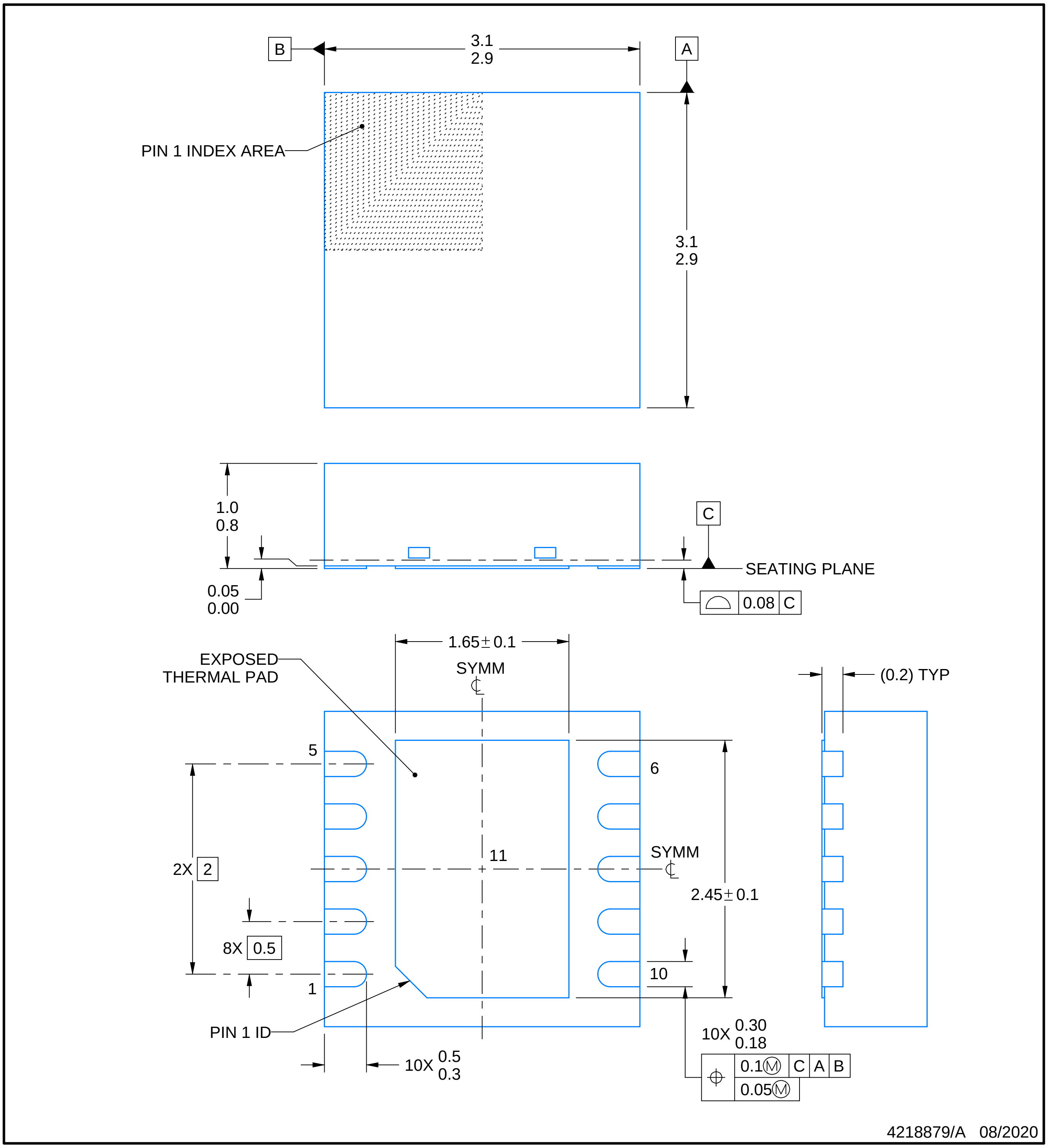
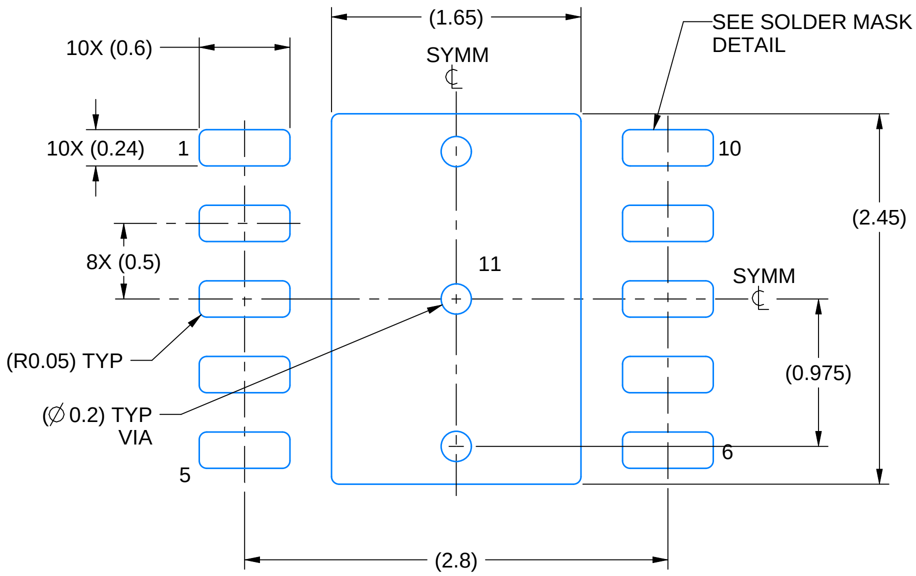
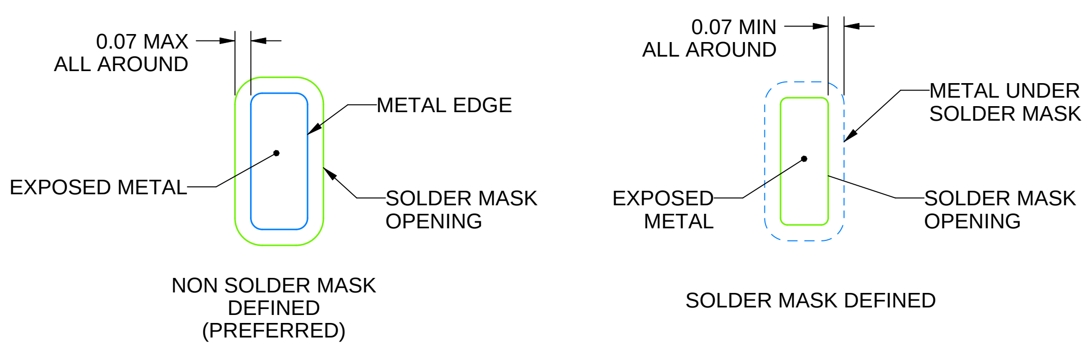


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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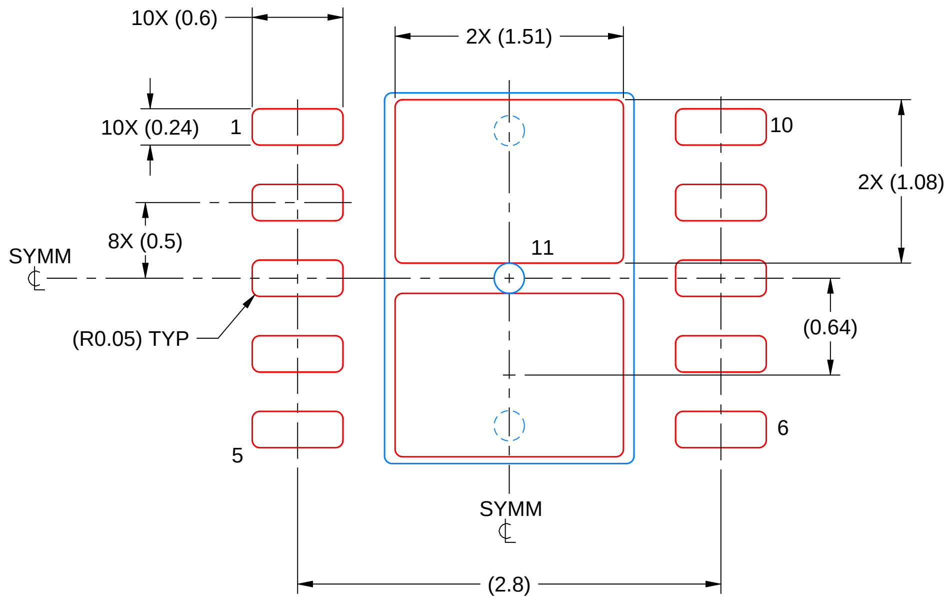
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月