TEXAS INSTRUMENTS
TPS25730
JAJSRT9 – OCTOBER 2023

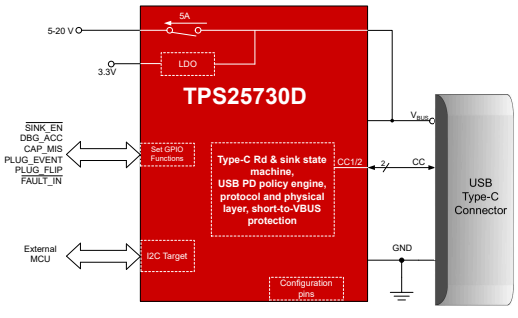
TPS25730 USB Type-C® および USB PD コントローラ、パワー・スイッチ内蔵、電源アプリケーションに最適化

1 特長

- シンク側のみのアプリケーション向け PD3.1 互換
  - PD3.1 は USB-IF による電力供給の最新仕様です
  - PD2 および PD3
- 完全に構成可能なシングル ポートの PD コントローラ
  - シンク側のみの USB Type-C および USB PD アプリケーション向けに最適化
  - USB Type-C への切り替えのためのバレル ジャック代替ソリューション
  - ピン ストラップにより完全に構成可能
  - 工業温度範囲をサポート
  - セレクション ガイドについてより詳しくは、『USB Type-C および PD ポートフォリオ』と『USB Type-C および PD コントローラの選択』を参照してください
- 完全に管理された内蔵のパワー パス
  - 過電圧保護および逆電流保護機能を内蔵
- USB Type-C PD コントローラ
  - 6 つの GPIO 設定機能
  - ケーブルの接続と方向の検出
  - デッド バッテリ Rd を内蔵
  - 物理層およびポリシー・エンジン
  - 消耗バッテリ向け VBUS 3.3V LDO を内蔵
  - 3.3V または VBUS 電源からの電力供給
  - 外付けマイクロコントローラ用の I2C アクセス

2 アプリケーション

- 電動工具、パワー・バンク、リテール・オートメーションおよびペイメント
- ワイヤレス・スピーカ、ヘッドホン
- その他のパーソナル・エレクトロニクスおよび産業用アプリケーション



3 概要

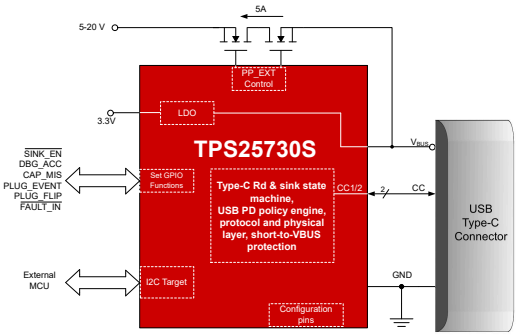
TPS25730 は、USB-C PD 電源に対応する、シンク側のみのアプリケーション向けに最適化された、高集積型スタンドアロン USB Type-C および PD (給電) コントローラです。TPS25730 は、完全に管理されたパワー パスと堅牢な保護機能を内蔵することにより、包括的な USB-C PD ソリューションを実現できます。また、TPS25730 は、内蔵ゲート ドライバを使用して外部パワー パスを制御する機能も備えています。TPS25730 は、従来ならバレル ジャックから給電されていた可能性がある、シンク側のみのアプリケーション向けに最適です。ユーザーは、抵抗ピン ストラップを使用することにより、TPS25730 を搭載したフル機能の USB Type-C PD ポートをプラットフォーム上に実装できます。外付け EEPROM や外付けマイクロコントローラ、いかなるファームウェア開発も必要ありません。

TPS25730 の目的は、シンク側のみの USB Type-C アプリケーションの設定を、シンプルかつ堅牢にすることです。ユーザーは、バレル ジャック ポートの利点をすべて活用すると同時に、USB Type-C と USB Type-C PD がシステムにもたらす利点も享受できます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)(2)
TPS25730D	QFN (REF)	4.00mm × 6.00mm
TPS25730S	QFN (RSM)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます



このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

DEVICE NUMBER	INTEGRATED HIGH VOLTAGE SINK LOAD SWITCH (PPHV)	HIGH VOLTAGE GATE DRIVER FOR EXTERNAL SINK PATH (PP_EXT)
TPS25730D	Yes	No
TPS25730S	No	Yes

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5 Pin Configuration and Functions

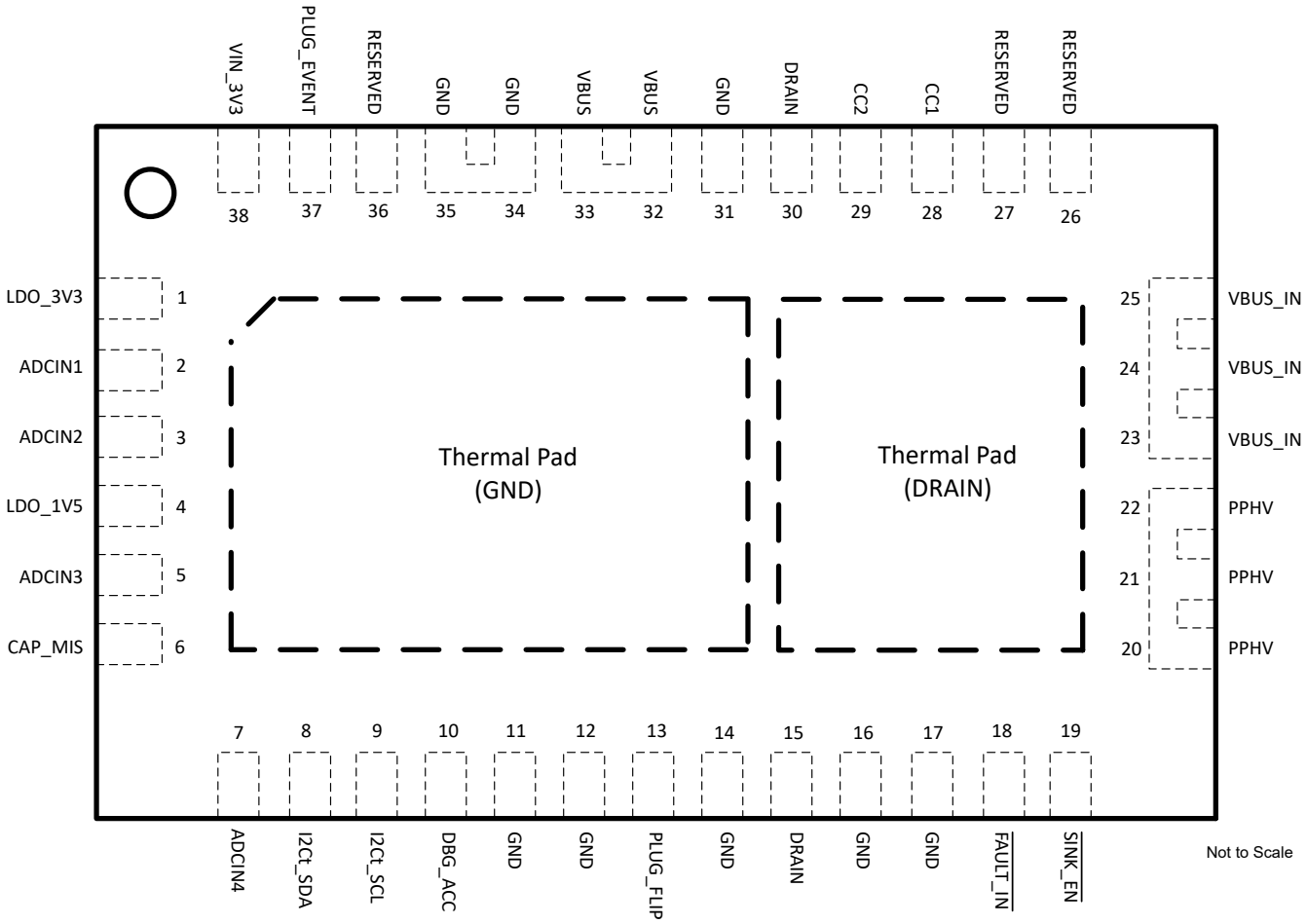


図 5-1. Top View of the TPS25730D 38-pin QFN Package

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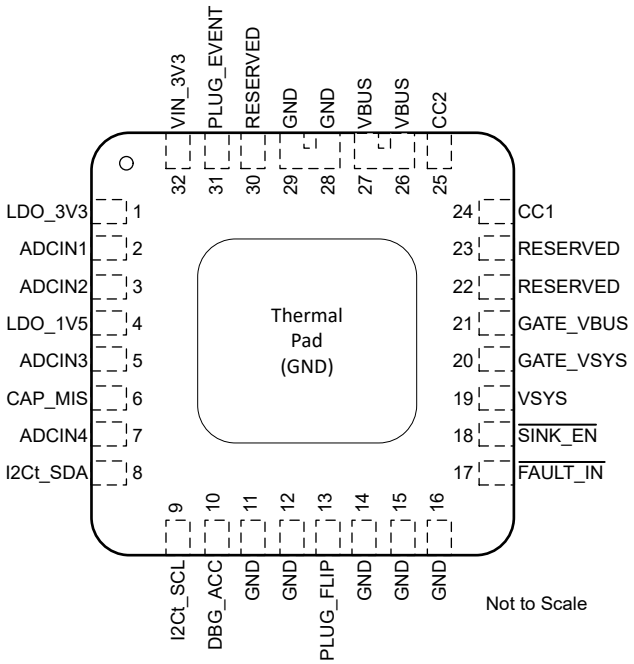


図 5-2. Top View of the TPS25730S 32-pin QFN Package

表 5-1. TPS25730D Pin Functions

PIN		TYPE(1)	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	28	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
CC2	29	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
GND	11, 12, 14, 16, 17, 31, 34, 35	—	—	Ground. Connect to ground plane.
ADCIN3	5	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CAP_MIS	6	O	Hi-Z	Open Drain Output, Capability Mismatch indicator. Toggled Output: Capability Mismatch in negotiated PD contract, No Toggled Output: No Capability Mismatch in negotiated PD contract.
ADCIN4	7	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
$\overline{\text{SINK_EN}}$	19	O	Hi-Z	Open Drain Output, Sink path enabled indicator, may be used to control an external load switch. 0: Sink Path Enabled, 1: Sink Path Disabled
RESERVED	26, 27, 36	I	Hi-Z	Tie to ground or LDO_3V3
PLUG_EVENT	37	O	Hi-Z	Open Drain Output, 1: Connection Present 0: No Connection Present
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
DBG_ACC	10	O	Hi-Z	Open Drain Output, Debug Accessory attached Rp/Rp or Rd/Rd. 1: Debug Accessory Present, 0: No Debug Accessory Present
PLUG_FLIP	13	O	Hi-Z	Open Drain Output, Cable plug orientation indicator. 1: CC2 connected (upside-down), 0: CC1 connected (upside-up)

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表 5-1. TPS25730D Pin Functions (続き)

PIN		TYPE(1)	RESET	DESCRIPTION
NAME	NO.			
$\overline{\text{FAULT_IN}}$	18	I	Hi-Z	Fault Input to disconnect from the port. When powered from VBUS this causes the PD controller to lose power when VBUS is removed. 0: Disconnect from port, 1: Maintain connection - no fault
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
DRAIN	15, 30	N/A	—	Connects to drain of internal FET.
PPHV	20, 21, 22	I/O		High-voltage sinking node in the system.
VBUS_IN	23, 24, 25	I/O		5-V to 20-V input.
VBUS	32, 33	O		VBUS input to LDO. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	38	I	—	Supply for core circuitry and I/O. Bypass with capacitance C_{VIN_3V3} to GND.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

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表 5-2. TPS25730S Pin Functions

PIN		TYPE(1)	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
CC2	25	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
GATE_VSYS	20	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VSYS
GATE_VBUS	21	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VBUS
GND	11, 12, 14, 15, 16, 28, 29	—	—	Ground. Connect to ground plane.
ADCIN3	5	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CAP_MIS	6	O	Hi-Z	Open Drain Output, Capability Mismatch indicator. Toggled Output: Capability Mismatch in negotiated PD contract, No Toggled Output: No Capability Mismatch in negotiated PD contract.
ADCIN4	7	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
$\overline{\text{SINK_EN}}$	18	O	Hi-Z	Open Drain Output, Sink path enabled indicator, may be used to control an external load switch. 0: Sink Path Enabled, 1: Sink Path Disabled
RESERVED	22, 23, 30	I	Hi-Z	Tie to ground or LDO_3V3
PLUG_EVENT	31	O	Hi-Z	Open Drain Output, 1: Connection Present 0: No Connection Present
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
DBG_ACC	10	O	Hi-Z	Open Drain Output, Debug Accessory attached Rp/Rp or Rd/Rd. 1: Debug Accessory Present, 0: No Debug Accessory Present
PLUG_FLIP	13	O	Hi-Z	Open Drain Output, Cable plug orientation indicator. 1: CC2 connected (upside-down), 0: CC1 connected (upside-up)
$\overline{\text{FAULT_IN}}$	17	I	Hi-Z	Fault Input to disconnect from the port. When powered from VBUS this causes the PD controller to lose power when VBUS is removed. 0: Disconnect from port, 1: Maintain connection - no fault
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
VSYS	19	I	—	High-voltage sinking node in the system. Used to implement reverse current protection (RCP) for the external sink path controlled by GATE_VSYS.
VBUS	26, 27	I/O		5-V to 20-V input. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

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6 Specifications

6.1 Absolute Maximum Ratings

6.1.1 TPS25730D and TPS25730S - Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range (2)	VIN_3V3	–0.3	4	V
	ADCINx	–0.3	4	
	VBUS_IN, VBUS(4)	–0.3	28	V
	CC1, CC2 (4)	–0.5	26	
	GPIOx	–0.3	6.0	
	I2Ct_SCL, I2Ct_SDA	–0.3	4	
Output voltage range (2)	LDO_1V5(3)	–0.3	2	V
	LDO_3V3(3)	–0.3	4	
Source current	Sink current VBUS		internally limited	A
	Positive sink current for I2Ct_SCL, I2Ct_SDA		internally limited	
	Positive source current for LDO_3V3, LDO_1V5		internally limited	
Source current	GPIOx		0.005	A
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent damage to the device. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

6.1.2 TPS25730D - Absolute Maximum Ratings

		MIN	MAX	UNIT
Input voltage range (1)	PPHV	–0.3	28	V
$V_{PPHV_VBUS_IN}$	Source-to-source voltage		28	V
Sink current	Continuous current to/from VBUS_IN to PPHV		7	A
	Pulsed current to/from VBUS_IN to PPHV(2)		10	
T_{J_PPHV} Operating junction temperature	PP_HV switch	–40	175	°C

(1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(2) Pulse duration ≤ 100 µs and duty-cycle ≤ 1%.

6.1.3 TPS25730S - Absolute Maximum Ratings

		MIN	MAX	UNIT
Output voltage range (1)	GATE_VBUS, GATE_VSYS(2)	–0.3	40	V
V_{GS}	V_{GATE_VBUS} - V_{VBUS}, V_{GATE_SYS} - V_{VSYS}	–0.5	12	V

(1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(2) Do not apply voltage to these pins.

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6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3.1 TPS25730D - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage range (1)	VIN_3V3	3.0	3.6	V
		ADCIN1, ADCIN2,VBUS_IN, VBUS(2)	4	22	
		PPHV	0	22	
V_{IO}	I/O voltage range (1)	I2Ct_SDA, I2Ct_SCL, ADCINx	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_{PP_HV}	Current from VBUS_IN to PPHV			7	A
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	Current from LDO_3V3		5	mA
T_A	Ambient operating temperature	$I_{PP_HV} \le 7$ A	–40	45	°C
		$I_{PP_HV} \le 6$ A	–40	65	
T_{J_PPHV}	Operating junction temperature	PP_HV switch	–40	150	°C
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(2) All VBUS and VBUS_IN pins be shorted together.

6.3.2 TPS25730S - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage range (1)	VIN_3V3	3.0	3.6	V
		VBUS	4	22	
		VSYS	0	22	
V_{IO}	I/O voltage range (1)	I2Ct_SDA, I2Ct_SCL, ADCINx	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	sum of current from LDO_3V3 and GPIOx		5	mA
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3 V	5	10		µF

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over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4 V	4.5		12	µF
C_{VBUS}	Capacitance on VBUS[3]	25 V	1	4.7	10	µF
C_{VSYS} (TPS25730S)	Capacitance on VSYS Sink from VBUS[4]	25 V		47	100	µF
C_{PPHV} (TPS25730D)	Capacitance on PPHV Sink from VBUS[4]	25 V		47	100	µF
C_{CCy}	Capacitance on CCy pins[2]	6.3 V	200	400	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value is 10 µF.
(2) Capacitance includes all external capacitance to the Type-C receptacle.
(3) The device can be configured to quickly disable the sinking power path upon certain events. When such a configuration is used, a capacitance on the higher side of the range is recommended.
(4) USB PD specification for cSnkBulkPd (100µF) is the maximum bulk capacitance allowed on a VBUS sink after a PD contract is in place. The capacitance is sufficient for all power conversion devices deriving power from the PD Controller sink path. For systems requiring greater than 100uF, VBUS surge current limiting is implemented as described in the USB3.2 specification.

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6.5 Thermal Information

6.5.1 TPS25730D - Thermal Information

THERMAL METRIC[1]		TPS25730D QFN 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (sinking through PP_HV)	57.4	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance (sinking through PP_HV)	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (sinking through PP_HV)	21.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (sinking through PP_HV)	18.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (sinking through PP_HV)	21.1	°C/W
$R_{\theta JC}$ (bot_GND)	Junction-to-case (bottom GND pad) thermal resistance	1.8	°C/W
$R_{\theta JC}$ (bot_DRAIN)	Junction-to-case (bottom DRAIN pad) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5.2 TPS25730S - Thermal Information

THERMAL METRIC[1]		TPS25730S QFN 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JC}$	Junction-to-board (bottom) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
V_{VBUS_UVLO}	VBUS UVLO threshold	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		
V_{VIN3V3_UVLO}	Voltage required on VIN_3V3 for power on	rising, V_{VBUS} = 0	2.56	2.66	2.76	V
		falling, V_{VBUS} = 0	2.44	2.54	2.64	
		hysteresis		0.12		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	Voltage on LDO_3V3	V_{VIN_3V3} = 0 V, 10 µA ≤ I_{LOAD} ≤ 18 mA, $_{VBUS}$ ≥ 3.9 V	3.0	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3} = 50 mA			1.4	Ω
V_{LDO_1V5}	Voltage on LDO_1V5	up to maximum internal loading condition	1.49	1.5	1.65	V

6.7 Power Consumption

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN_3V3,ActSnk}$	Current into VIN_3V3	Active Sink mode: 22 V ≥ V_{VBUS} ≥ 4.0 V, V_{VIN_3V3} = 3.3 V		3	6	mA
$I_{VIN_3V3,IdlSnk}$	Current into VIN_3V3	Idle Sink mode: 22 V ≥ V_{VBUS} ≥ 4.0 V, V_{VIN_3V3} = 3.3 V		1.0		mA
$I_{VIN_3V3,Sleep}$	Current into VIN_3V3	Sleep mode: V_{VBUS} = 0 V, V_{VIN_3V3} = 3.3 V		56		µA

6.8 PPHV Power Switch Characteristics - TPS25730D

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PPHV}	Resistance from VBUS_IN to PPHV power switch resistance	T_{J_PPHV} = 25°C, I_{PPHV} = 6.5 A		16	19	mΩ
		T_{J_PPHV} = 125°C, I_{PPHV} = 6.5A		24	29	
		T_{J_PPHV} = 150°C, I_{PPHV} = 6.5 A		27	32	mΩ
V_{RCP}	Comparator mode RCP threshold, V_{PPHV} - V_{VBUS}	4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	2	6	10	mV
SS	Soft start slew rate for GATE_VSYS	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	2.8	3.3	3.80	V/ms
t_{PPHV_OFF}	Time allowed to disable the internal PPHV switch in normal shutdown mode	V_{VBUS} = 20 V, V_{PPHV} = 20 V (initially), C_{PPHV}< 1 nF, I_{PPHV} = 0.1 A, switch is off when V_{VBUS_IN} – V_{PPHV} > 1V		400	1000	µs

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6.8 PPHV Power Switch Characteristics - TPS25730D (続き)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PPHV_OVP}	Time allowed to disable the internal PPHV switch in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator	OVP: $V_{OVP4RCP}$ = setting 57, V_{VBUS} = 20 V initially, then raised to 23 V in 50 ns, V_{PPHV} = V_{VBUS_IN} (initially), C_{PPHV}< 1 nF, I_{PPHV} = 0.1 A, switch is off when V_{VBUS_IN} – V_{PPHV} > 0.1 V		2	4	µs
t_{PPHV_RCP}	Time allowed to disable the internal PPHV switch in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator	RCP: V_{RCP}= setting 0, V_{VBUS} = 5 V, V_{VSYS} = 5 V initially, then raised to 6 V with dV/dt = 0.1 V/µs, $C_{VBUS=}$10 µF, measure time from V_{VSYS} > V_{BUS} + V_{RCP} to the time of peak voltage on VBUS		1	2	µs
t_{PPHV_FSD}	Time allowed to disable the internal PPHV switch in fast shutdown mode (OVP)	V_{PPHV} = 20 V (initially), V_{VBUS}=20 V then raised to 23 V in 50 ns, r_{OVP} = 1, C_{PPHV} < 1 nF, I_{PPHV} = 0.1 A, switch is off when V_{VBUS_IN} – V_{PPHV} > 0.5 V		0.25	20	µs
t_{PPHV_ON}	Time to enable the internal PPHV switch	V_{VBUS_IN} = 5 V, C_{PPHV} = 0, I_{PPHV} = 0, measure time from register write to enable PPHV until V_{VBUS_IN} - V_{PPHV} < 0.1 V, soft start setting 3	1500	1800	2100	µs

6.9 PP_EXT Power Switch Characteristics - TPS25730S

Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GATE_ON}	Gate driver sourcing current	0 ≤ V_{GATE_VSYS} - V_{VSYS} ≤ 6 V, V_{VSYS} ≤ 22 V, V_{VBUS} > 4 V, measure I_{GATE_VSYS}	8.5		11.5	µA
		0 ≤ V_{GATE_VBUS} - V_{VBUS} ≤ 6 V, 4 V ≤ V_{VBUS} ≤ 22 V, measure I_{GATE_VBUS}	8.5		11.5	µA
V_{GATE_ON}	Sourcing voltage (ON)	0 ≤ V_{VSYS} ≤ 22 V, I_{GATE_VSYS} < 4 µA, measure V_{GATE_VSYS} – V_{VSYS}, V_{VBUS} > 4 V	6		12	V
		4 V ≤ V_{VBUS} ≤ 22 V, I_{GATE_VBUS} < 4 µA, measure V_{GATE_VBUS} – V_{VBUS}	6		12	V
V_{RCP}	Comparator mode RCP threshold, V_{VSYS} - V_{VBUS}	4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	2	6	10	mV
I_{GATE_OFF}	Sinking strength	Normal turnoff: V_{VSYS} = 5 V, V_{GATE_VSYS} = 6 V, measure I_{GATE_VSYS}	13			µA
		Normal turnoff: V_{VBUS} = V_{VSYS} = 5 V, V_{GATE_VBUS} = 6 V, measure I_{GATE_VBUS}	13			µA

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6.9 PP_EXT Power Switch Characteristics - TPS25730S (続き)

Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{GATE_FSD}	Sinking strength	Fast turnoff: V_{VSYS} = 5 V, V_{GATE_VSYS} = 6 V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VSYS}			85	Ω
		Fast turnoff: V_{VBUS} = V_{VSYS} = 5 V, V_{GATE_VBUS} = 6 V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VBUS}			85	Ω
$R_{GATE_OFF_UVLO}$	Sinking strength in UVLO (safety)	V_{VIN_3V3} = 0 V, V_{VBUS} = 3.0 V, V_{GATE_VSYS} = 0.1 V, measure resistance from GATE_VSYS to GND			1.5	MΩ
SS	Soft start slew rate for GATE_VSYS	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	2.8	3.3	3.80	V/ms
$t_{GATE_VBUS_OFF}$	Time allowed to disable the external FET via GATE_VBUS in normal shutdown mode.(1)	V_{VBUS} = 20 V, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when V_{GATE_VBUS} – V_{VBUS} < 1 V		450	4000	µs
$t_{GATE_VBUS_OVP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator(1)	OVP: $V_{OVP4RCP}$ = setting 57, V_{VBUS} = 20 V initially, then raised to 23 V in 50 ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when V_{GATE_VBUS} – V_{VBUS} < 1 V		3	5	µs
$t_{GATE_VBUS_RCP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator(1)	RCP: V_{RCP} = setting 0, V_{VBUS} = 5 V, V_{VSYS} = 5 V initially, then raised to 5.5 V in 50 ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when V_{GATE_VBUS} – V_{VBUS} < 1 V		1	2	µs
$t_{GATE_VSYS_OFF}$	Time allowed to disable the external FET via GATE_VSYS in normal shutdown mode(1)	V_{VSYS}= 20 V, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when V_{GATE_VSYS} – V_{VSYS} < 1 V		450	4000	µs
$t_{GATE_VSYS_FSD}$	Time allowed to disable the external FET via GATE_VSYS in fast shutdown mode (OVP)(1)	V_{VBUS} = 20 V initially, then raised to 23 V in 50 ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when V_{GATE_VSYS} – V_{VSYS} < 1 V, r_{OVP} = 1		0.25	20	µs
$t_{GATE_VBUS_ON}$	Time to enable GATE_VBUS (1)	Measure time from when V_{GS} = 0 V until V_{GS} >3 V, where V_{GS} = V_{GATE_VBUS} – V_{VBUS}		0.25	2	ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values were measured when Px_GATE_VSYS and Px_GATE_VBUS were used to drive two CSD17571Q2 in common drain back-to-back configuration.

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6.10 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS overvoltage protection for RCP programmable range	OVP detected when V_{VBUS} > $V_{OVP4RCP}$	5.0		24	V
$V_{OVP4RCPH}$	Hysteresis		1.75	2	2.25	%
r_{OVP}	Ratio of OVP4RCP input used for OVP4VSYS comparator. r_{OVP} × $V_{OVP4VSYS}$ = $V_{OVP4RCP}$			1		V/V
$V_{OVP4VSYS}$	VBUS overvoltage protection range for VSYS protection	OVP detected when r_{OVP} × V_{VBUS} > $V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSYS}$	Hysteresis	VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP}	2	2.3	2.6	%
I_{DSCH}	VBUS discharge current	V_{VBUS} = 22 V, measure I_{VBUS}	4		15	mA

6.11 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Sink (Rd pull-down)						
V_{SNK1}	Open/Default detection threshold when Rd applied to Px_CCy	rising	0.2		0.24	V
	Open/Default detection threshold when Rd applied to Px_CCy	falling	0.16		0.20	V
	hysteresis			0.04		V
V_{SNK2}	Default/1.5A detection threshold	falling	0.62		0.68	V
	Default/1.5A detection threshold	rising	0.63	0.66	0.69	V
	hysteresis			0.01		V
V_{SNK3}	1.5A/3.0A detection threshold when Rd applied to Px_CCy	falling	1.17		1.25	V
	1.5A/3.0A detection threshold when Rd applied to Px_CCy	rising	1.22		1.3	V
	hysteresis			0.05		V
R_{SNK}	Rd pulldown resistance	0.25 V ≤ V_{Px_CCy} ≤ 2.1 V, measure resistance on Px_CCy	4.1		6.1	kΩ
V_{CLAMP}	Dead battery Rd clamp	V_{VIN_3V3}=0V, 64 µA < I_{Px_CCy}<96 µA	0.25		1.32	V
		V_{VIN_3V3}=0V, 166 µA < I_{Px_CCy}<194 µA	0.65		1.32	
		V_{VIN_3V3}=0V, 304 µA < I_{Px_CCy}< 356 µA	1.20		2.18	
R_{Open}	resistance from Px_CCy to GND when configured as open.	V_{Px_VBUS} = 0, V_{VIN_3V3}=3.3V, V_{Px_CCy}=5 V, measure resistance on Px_CCy	500			kΩ
		V_{Px_VBUS} = 5V, V_{VIN_3V3} = 0, V_{Px_CCy}=5 V, measure resistance on Px_CCy	500			kΩ
Common Sink						
t_{CC}	deglitch time for comparators on Px_CCy			3.2		ms

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6.12 CC PHY Parameters

Operating under these conditions unless otherwise noted: and (3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{VBUS} ≥ 3.9 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on CCy	Standard External load	–75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using CCy	measured at 750 kHz	33	54	75	Ω
t_{Rise}	Rise time. 10 % to 90 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520 pF	300			ns
t_{Fall}	Fall time. 90 % to 10 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520 pF	300			ns
V_{PHY_OVP}	OVP detection threshold for USB PD PHY	0 ≤ V_{VIN_3V3} ≤ 3.6 V, V_{VBUS} ≥ 4 V. Initially V_{CC1} ≤ 5.5 V and V_{CC2} ≤ 5.5 V, then V_{CCx} rises	5.5		8.5	V
Receiver						
Z_{BMCRX}	Receiver input impedance on CCy	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z	1			MΩ
C_{CC}	Receiver capacitance on CCy(1)	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX_SNK_R}$	Rising threshold on CCy for receiver comparator	Sink mode (rising)	499	525	551	mV
$V_{RX_SRC_R}$	Rising threshold on CCy for receiver comparator	Source mode (rising)	784	825	866	mV
$V_{RX_SNK_F}$	Falling threshold on CCy for receiver comparator	Sink mode (falling)	230	250	270	mV
$V_{RX_SRC_F}$	Falling threshold on CCy for receiver comparator	Source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{CCy} externally.

6.13 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		hysteresis		20		°C

6.14 ADC Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6-V max scaling, voltage divider of 3		14		mV
		25.2-V max scaling, voltage divider of 21		98		mV
		4.07-A max scaling		16.5		mA

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Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAIN_ERR	Gain error	0.05 V ≤ V_{ADCINx} ≤ 3.6 V, V_{ADCINx} ≤ V_{LDO_3V3}	–2.7		2.7	%
		0.05 V ≤ V_{GPIOx} ≤ 3.6 V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7 V ≤ V_{LDO_3V3} ≤ 3.6 V	–2.4		2.4	
		0.6 V ≤ V_{VBUS} ≤ 22 V	–2.1		2.1	
		1 A ≤ I_{VBUS} ≤ 3 A	–2.1		2.1	
VOS_ERR	Offset error(1)	0.05 V ≤ V_{ADCINx} ≤ 3.6 V, V_{ADCINx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
		0.05 V ≤ V_{GPIOx} ≤ 3.6 V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7 V ≤ V_{LDO_3V3} ≤ 3.6 V	–4.5		4.5	
		0.6 V ≤ V_{VBUS} ≤ 22 V	–4.1		4.1	
		1 A ≤ I_{VBUS} ≤ 3 A	–4.5		4.5	mA

(1) The offset error is specified after the voltage divider.

6.15 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45 V	–1		1	µA
GPIO_DG	GPIOx input deglitch			20		ns
GPIO0-9 (Outputs)						
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}= -2mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}=2mA			0.4	V
ADCINx						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} ≤ V_{LDO_3V3}	–1		1	µA
t_{BOOT}	time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

6.16 I2C Requirements and Characteristics

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Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL Common Characteristics Target)						
V_{IL}	Input low signal	V_{LDO_3V3}=3.3V,			0.54	V
V_{IH}	Input high signal	V_{LDO_3V3}=3.3V,	1.3			V
V_{HYS}	Input hysteresis	V_{LDO_3V3}=3.3V	0.165			V
V_{OL}	Output low voltage	I_{OL}=3 mA			0.36	V
I_{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	–3		3	µA
I_{OL}	Max output low current	V_{OL}=0.4 V	15			mA
I_{OL}	Max output low current	V_{OL}=0.6 V	20			mA
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 1.8V, 10 pF ≤ C_b ≤ 400 pF	12		80	ns

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Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 3.3V, 10 pF ≤ C_b ≤ 400 pF	12		150	ns
t_{SP}	I2C pulse width suppressed				50	ns
C_I	pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Target)						
f_{SCLS}	Clock frequency for target	V_{DD} = 1.8V or 3.3V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Target)						
f_{SCLS}	Clock frequency for target	V_{DD} = 1.8V or 3.3V	100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs
f_{SCLS}	Clock frequency for Fast Mode Plus	V_{DD} = 1.8V or 3.3V	400		800	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			0.55	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.55	µs

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6.17 Typical Characteristics

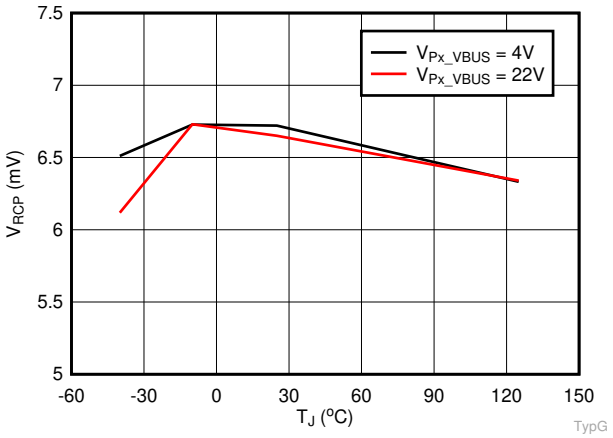


図 6-1. V_{RCP} vs. Temperature

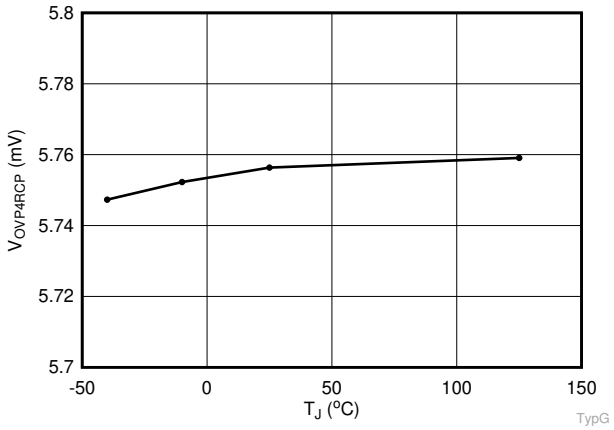


図 6-2. $V_{OVP4RCP}$ (Setting 2) vs. Temperature

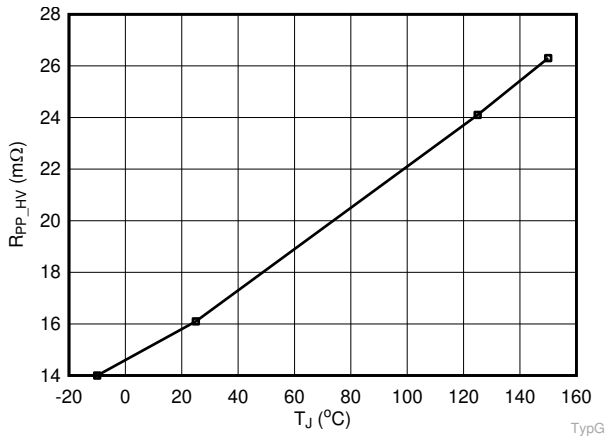


図 6-3. R_{PPHV} vs. Temperature for TPS25730D

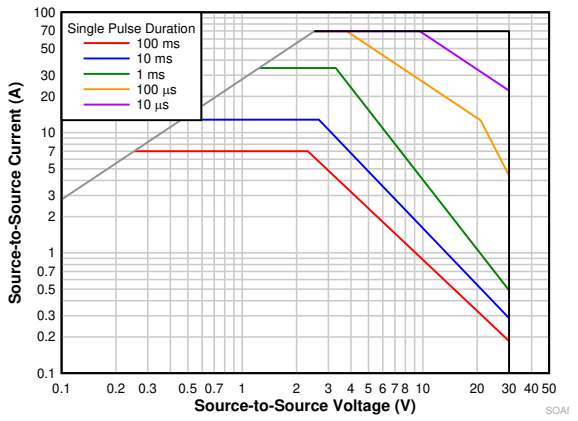


図 6-4. Safe-Operating-Area (SOA) of PPHV for TPS25730D

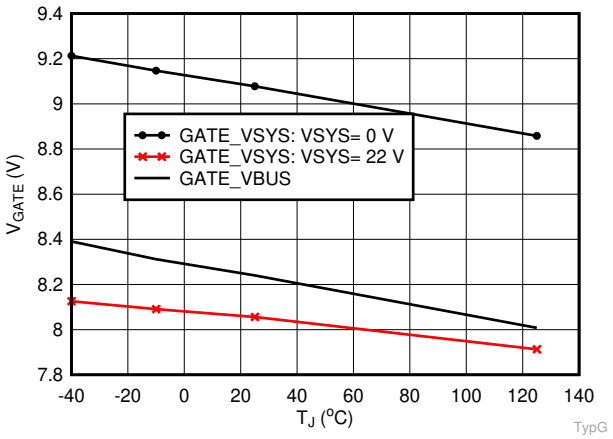


図 6-5. $V_{GATE_VBUS_ON}$ vs. Temperature for TPS25730S

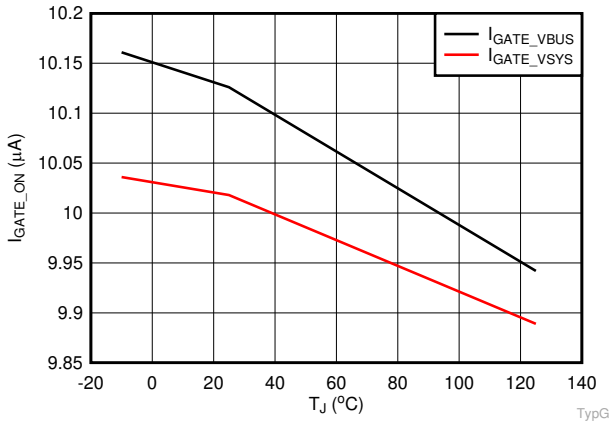


図 6-6. $V_{GATE_VSYS_ON}$ vs. Temperature for TPS25730S

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7 Parameter Measurement Information

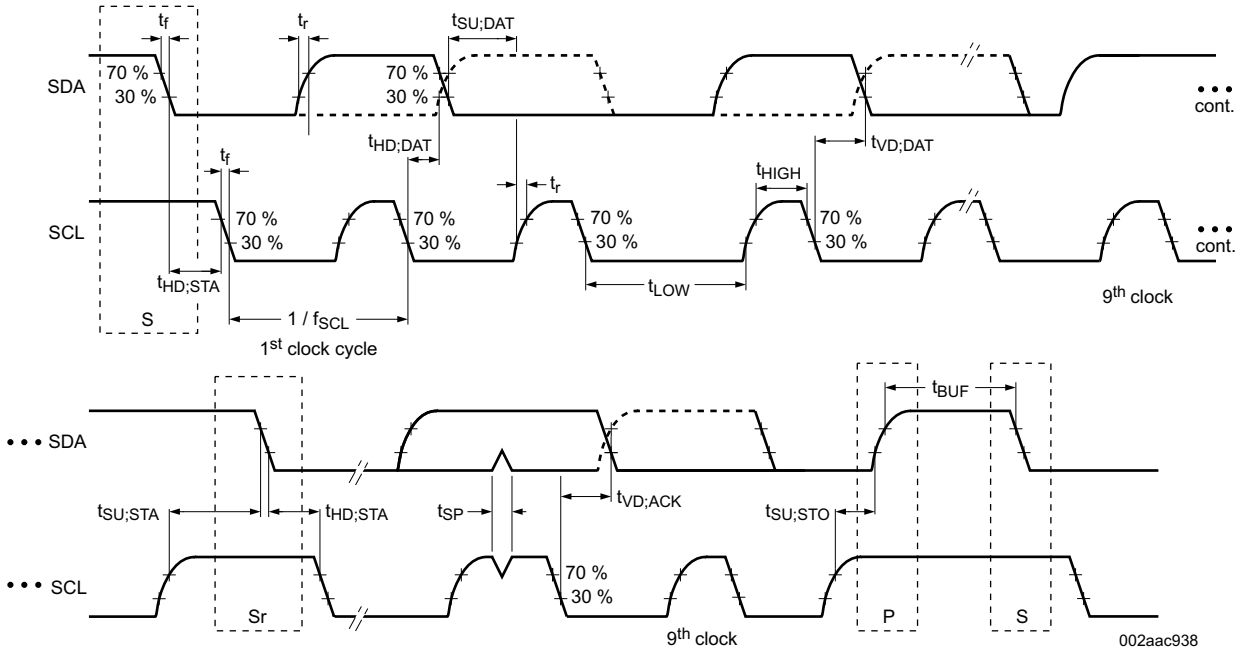


図 7-1. I²C Target Interface Timing

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8 Detailed Description

8.1 Overview

The TPS25730 is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacles. The TPS25730 communicates with the other USB Type-C and PD port partner at the opposite end of the cable. The device also enables integrates a high current port power switch for sinking.

The TPS25730 is divided into several main sections:

- USB-PD controller
- Cable plug and orientation detection circuitry
- Port power switch
- Power management circuitry
- Digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features, and more detailed circuitry, see *USB-PD Physical Layer*.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features, and more detailed circuitry, see *Cable Plug and Orientation Detection*.

For a high-level block diagram of the port power switch, a description of its features, and more detailed circuitry, see *Power Paths*.

The power management circuitry receives and provides power to the TPS25730 internal circuitry and LDO_3V3 output. See *Power Management* for more information.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS25730 functionality. For a high-level block diagram of the digital core, a description of its features, and more detailed circuitry, see *Digital Core*.

The TPS25730 also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

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8.2 Functional Block Diagram

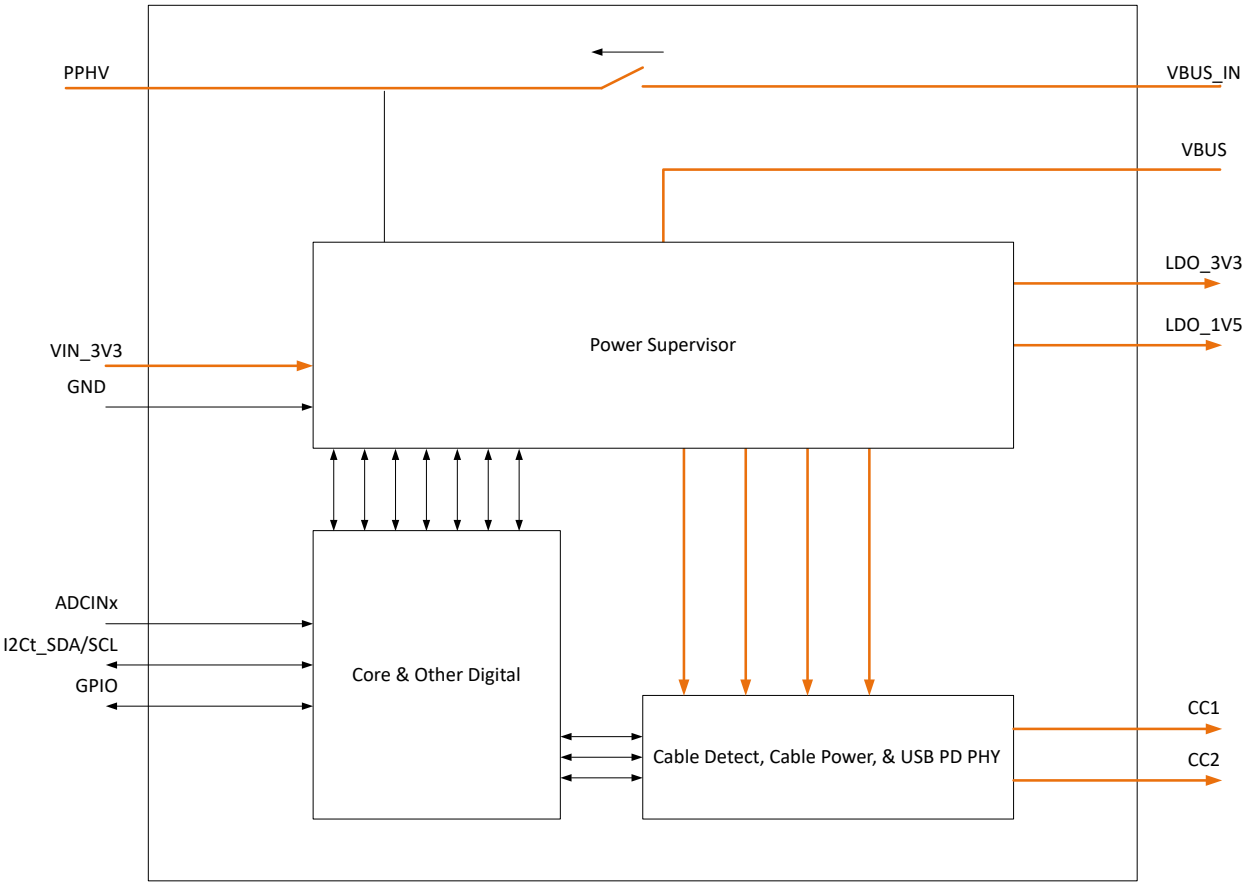


図 8-1. TPS25730D

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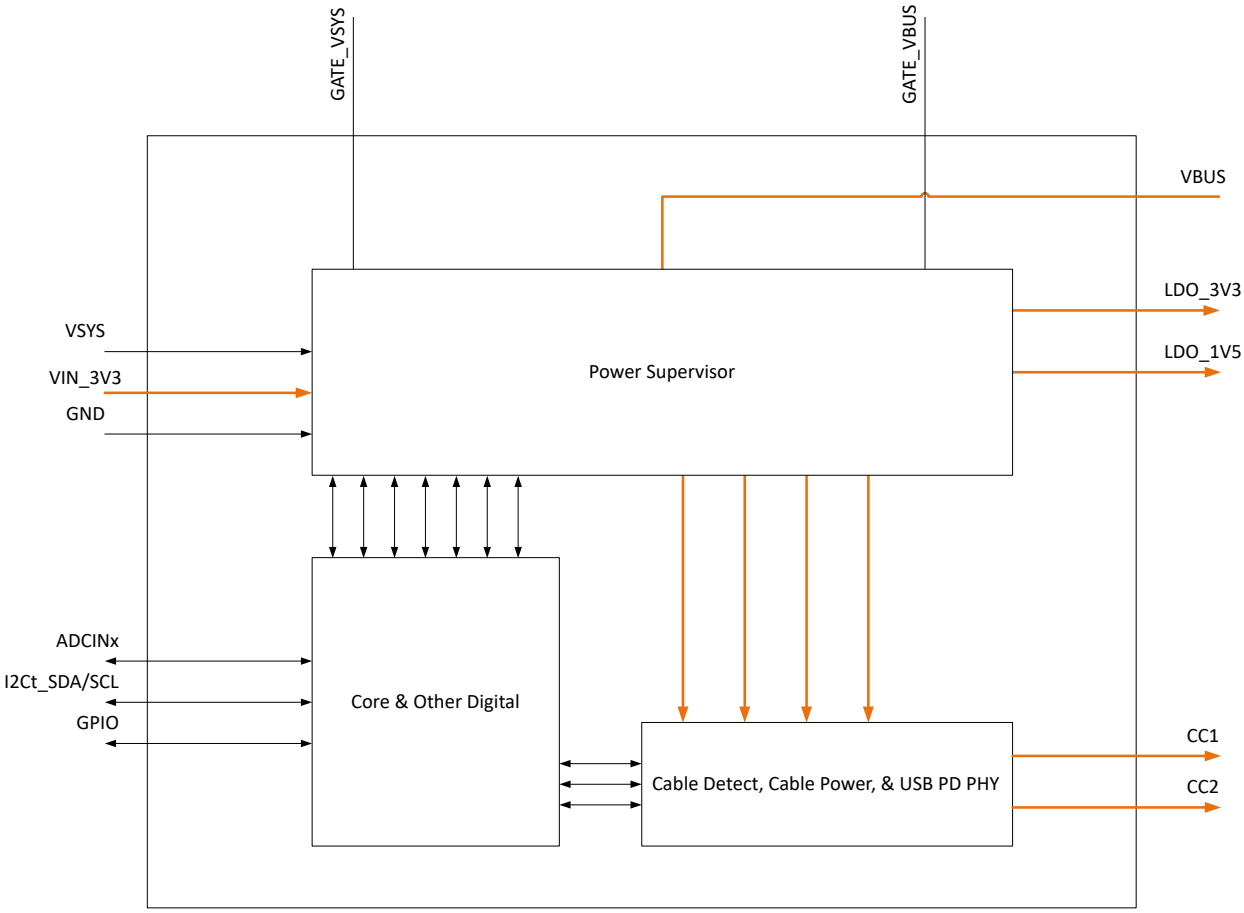


図 8-2. TPS25730S

8.3 Feature Description

8.3.1 USB-PD Physical Layer

図 8-3 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

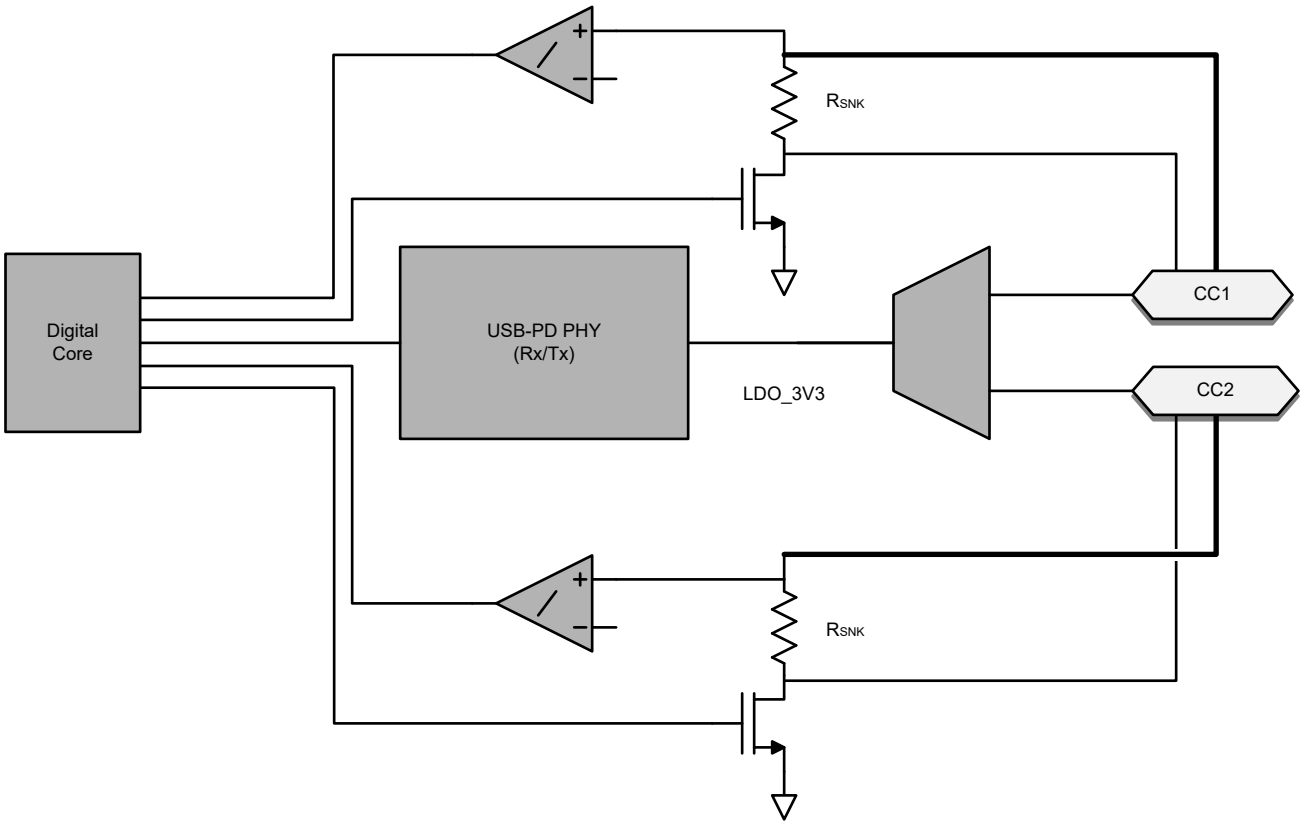


図 8-3. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

8.3.1.1 USB-PD Encoding and Signaling

図 8-4 illustrates the high-level block diagram of the baseband USB-PD transmitter. 図 8-5 illustrates the high-level block diagram of the baseband USB-PD receiver.

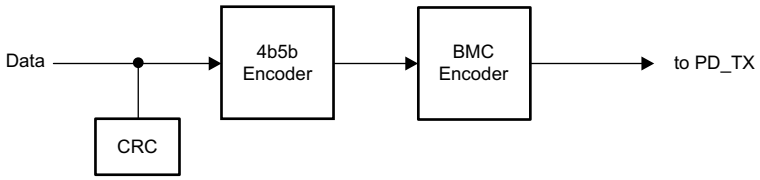


図 8-4. USB-PD Baseband Transmitter Block Diagram

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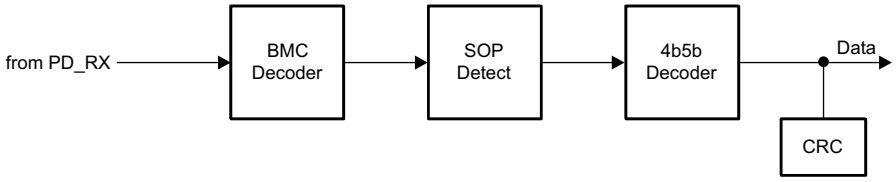


図 8-5. USB-PD Baseband Receiver Block Diagram

8.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS25730 is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). 図 8-6 illustrates Biphase Mark Coding.

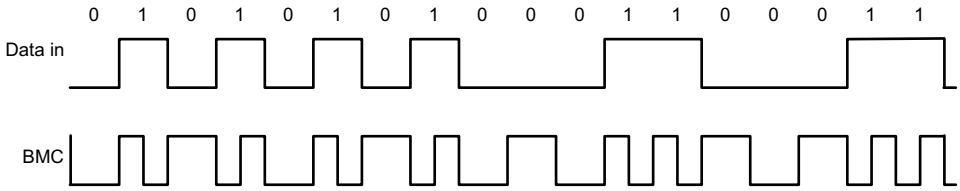


図 8-6. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD BMC Transmitter

The TPS25730 transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CCy pin when it is not transmitting. While either CC1 or CC2 can be used for transmitting and receiving, during a given connection only, the one that mates with the CC pin of the plug is used, so there is no dynamic switching between CC1 and CC2. 図 8-7 shows the USB-PD BMC TX and RX driver block diagram.

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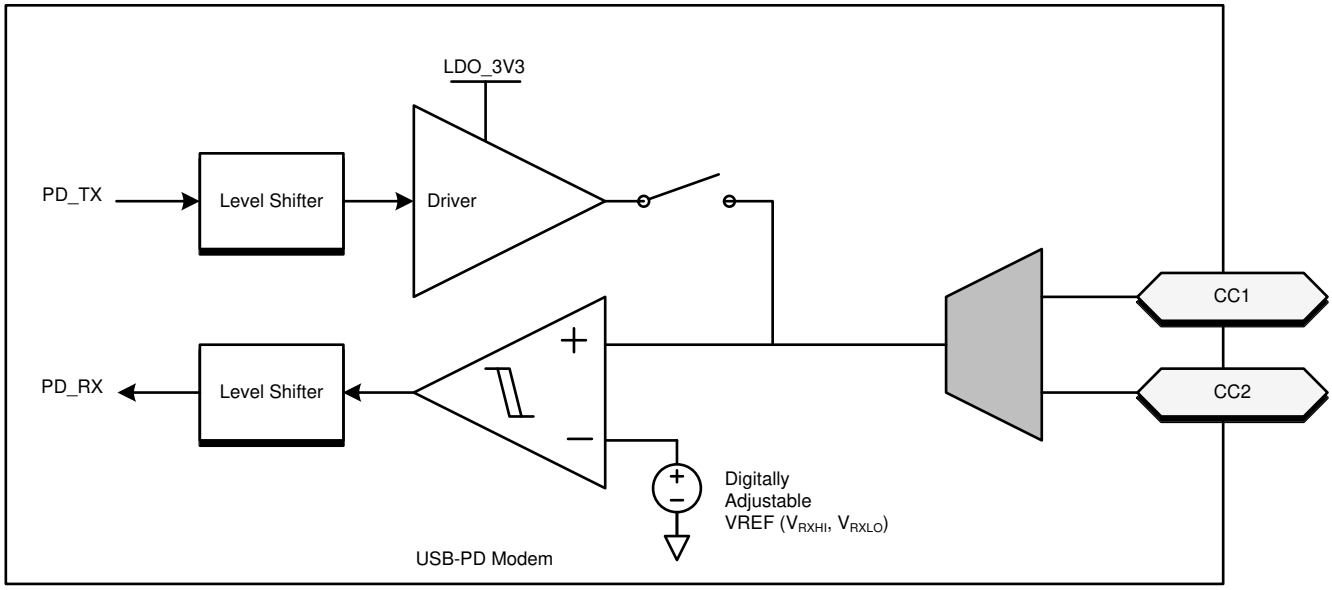


図 8-7. USB-PD BMC TX/Rx Block Diagram

図 8-8 shows the transmission of the BMC data on top of the DC bias. Note that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This note means that the DC bias can be above or below the VOH of the transmitter driver.

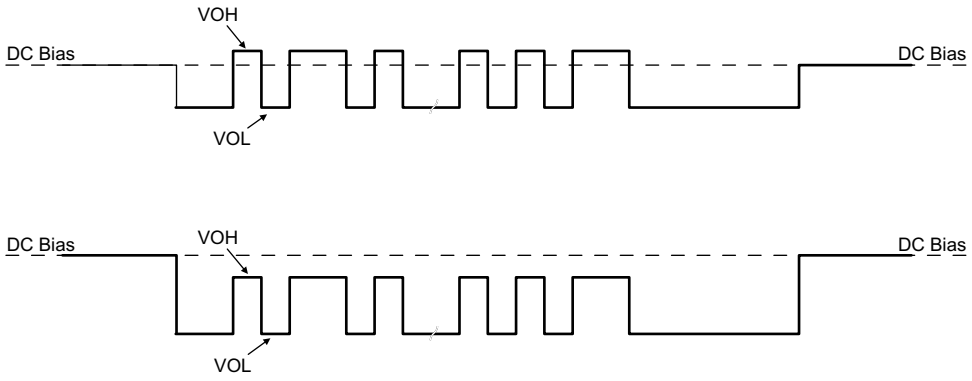


図 8-8. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

図 8-9 shows the simplified circuit determining Z_{DRIVER}. It is specified such that noise at the receiver is bounded.

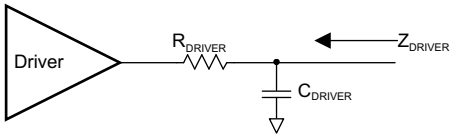


図 8-9. ZDRIVER Circuit

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8.3.1.4 USB-PD BMC Receiver

The receiver block of the TPS25730 receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

図 8-10 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

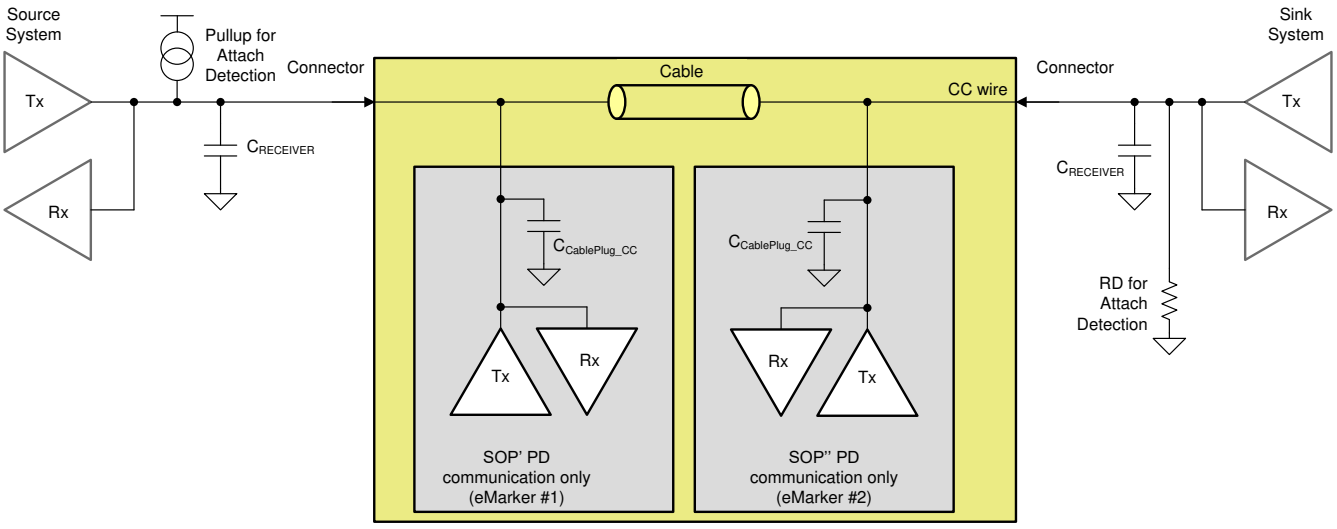


図 8-10. Example USB-PD Multi-Drop Configuration

8.3.1.5 Squelch Receiver

The TPS25730 has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

8.3.2 Power Management

The TPS25730 power management block receives power and generates voltages to provide power to the TPS25730 internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 can also be used as a low power output for external EEPROM memory. The power supply path is shown in 図 8-11.

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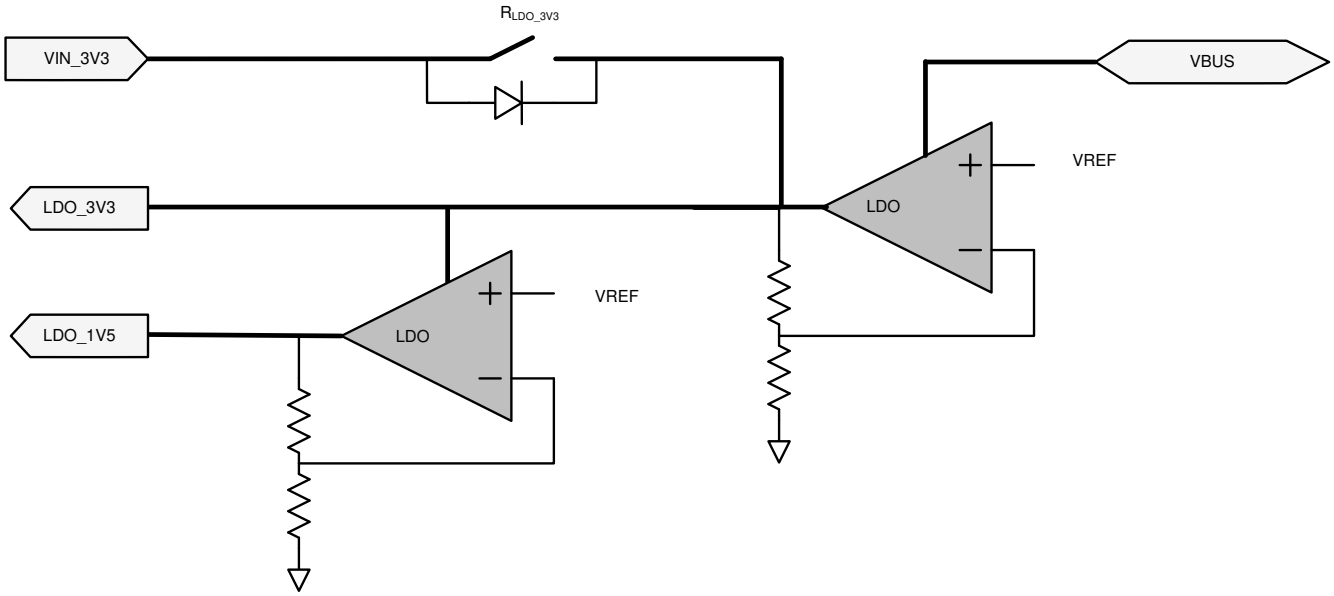


図 8-11. Power Supplies

The TPS25730 is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5-V core digital circuitry. When VIN_3V3 power is unavailable and power is available on VBUS, it is referred to as the dead-battery start-up condition. In a dead-battery start-up condition, the TPS25730 opens the VIN_3V3 switch until the host clears the dead-battery flag through I^2C. Therefore, the TPS25730 is powered from the VBUS input with the higher voltage during the dead-battery start-up condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO_3V3.

8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

8.3.2.2 VBUS LDO

The TPS25730 contains an internal high-voltage LDO which is capable of converting VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used when VIN_3V3 is low (the dead-battery condition). The VBUS LDO is powered from VBUS.

8.3.3 Power Paths

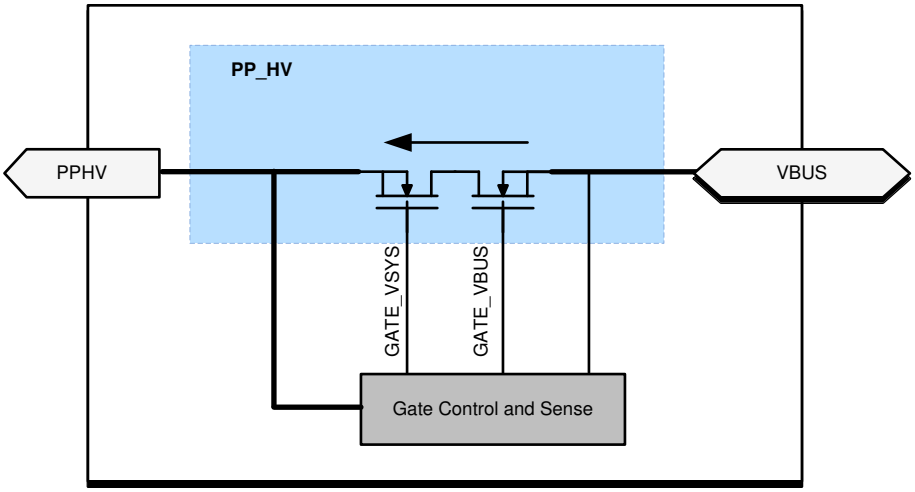
TPS25730D has a integrated high voltage load switch for sinking power path: PPHV. TPS25730S has a high voltage gate driver for sink path control: PP_EXT. Each power path is described in detail in this section.

8.3.3.1 TPS25730D Internal Sink Path

The TPS25730D has internal controls for internal FETs (GATE_VSYS and GATE_VBUS as shown in 図 8-12) that require that VBUS_IN be above V_{VBUS_UVLO} before being able to enable the sink path. 図 8-12 shows a diagram of the sink path. When a sink path is enabled, the circuitry includes a slew rate control loop to ensure that external switches do not turn on too quickly (SS). The TPS25730D senses the PPHV and VBUS voltages to control the gate voltages to enable or disable the FETs.

The sink-path control includes overvoltage protection (OVP) and reverse current protection (RCP).

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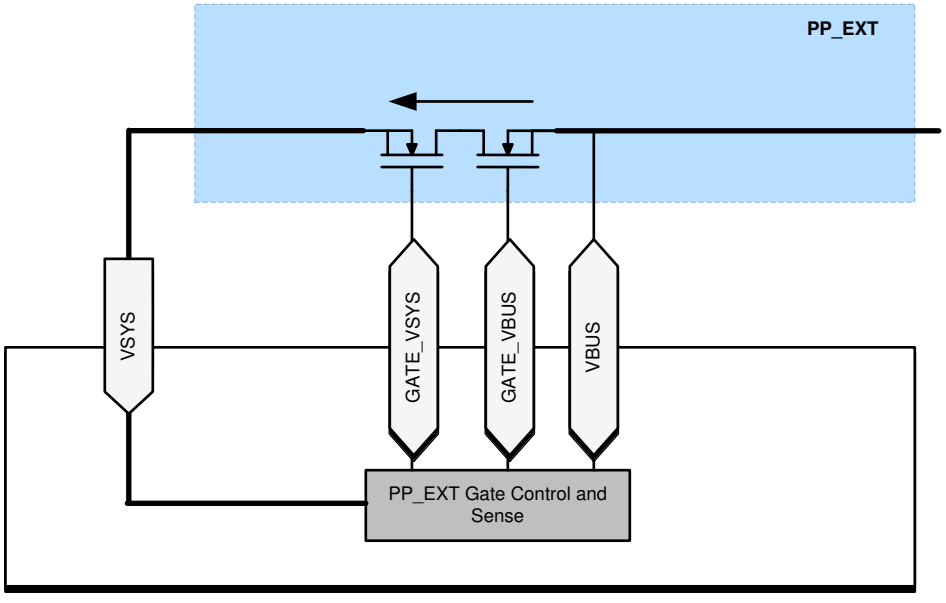
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図 8-12. Internal Sink Path

8.3.3.2 TPS25730S - External Sink Path Control PP_EXT

The TPS25730S has two N-ch gate drivers designed to control a sinking path from VBUS to VSYS. The charge pump for these gate drivers requires VBUS to be above VVBUS_UVLO. When a sink path is enabled, the circuitry includes a slew rate control loop to ensure that external switches do not turn on too quickly (SS). The TPS25730S senses the VSYS and VBUS voltages to control the gate voltages to enable or disable the external FETs.

The sink-path control includes overvoltage protection (OVP), and reverse current protection (RCP). Adding resistance in series with a GATE pin of the TPS25730S and the gate pin of the N-ch MOSFET slows down the turnoff time when OVP or RCP occurs. Any such resistance must be minimized, and not allowed to exceed 3 Ω.



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図 8-13. PP_EXT External Sink Path Control

図 8-14 shows the GATE_VSYS gate driver in more detail.

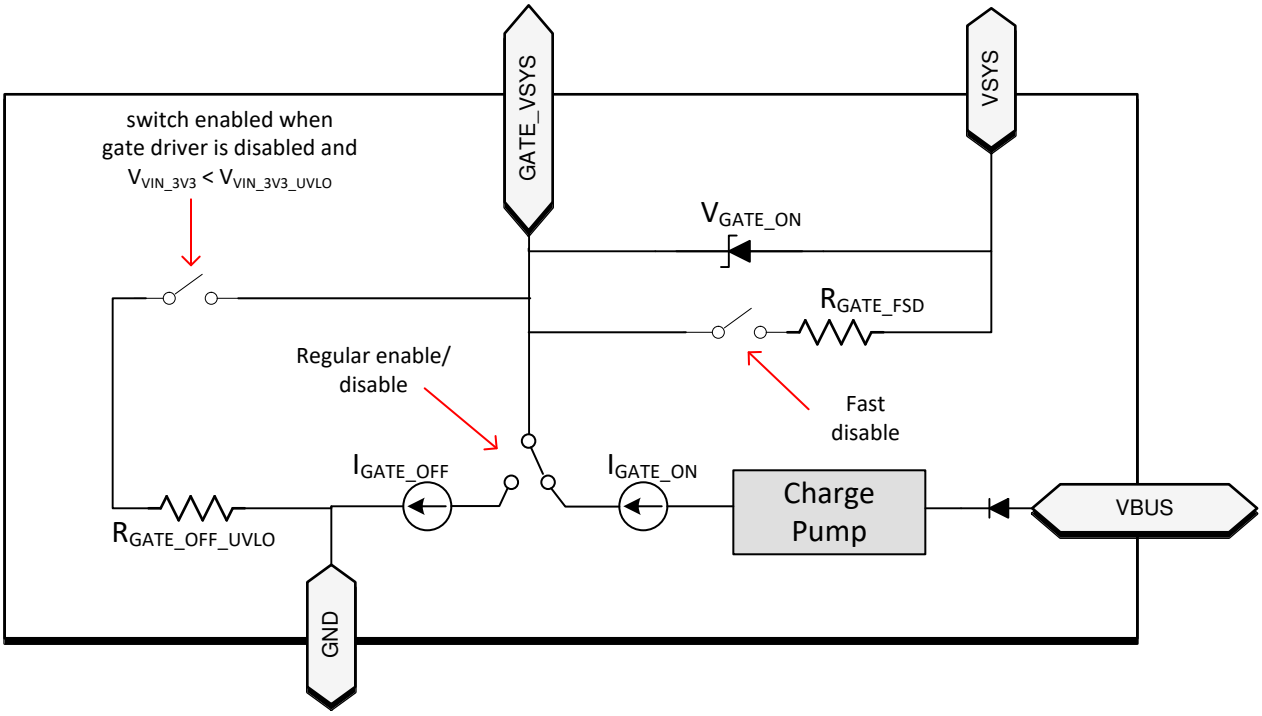


図 8-14. Details of the VSYS Gate Driver

8.3.4 Cable Plug and Orientation Detection

図 8-15 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

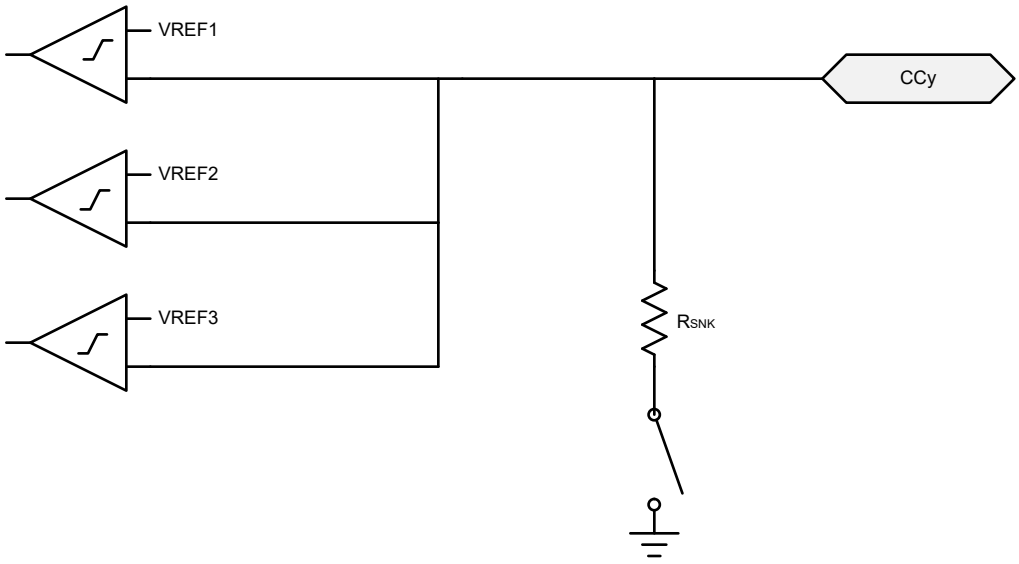


図 8-15. Plug and Orientation Detection Block

8.3.5 Overvoltage Protection (CC1, CC2)

The TPS25730 detects when the voltage on the CC1 or CC2 pin is too high and takes action to protect the system. The protective action is to disable the USB PD transmitter.

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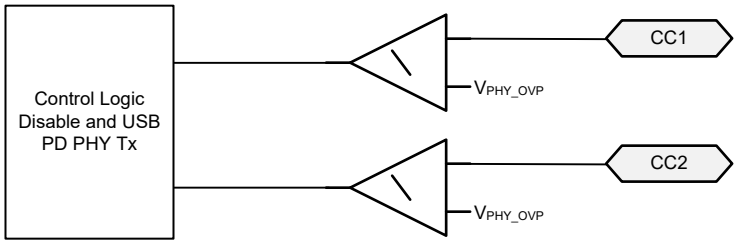


図 8-16. Overvoltage and Reverse Current Protection for CC1 and CC2

8.3.6 Default Behavior Configuration (ADCIN1, ADCIN2)

注

This functionality is firmware controlled and subject to change.

The ADCINx inputs to the internal ADC control the behavior of the TPS25730 in response to VBUS being supplied when VIN_3V3 is low (that is the dead-battery scenario). The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine start-up behavior. The available start-up configurations include options for I^2C target address of I2Ct_SCL/SDA, sink path control in dead-battery, and default configuration.

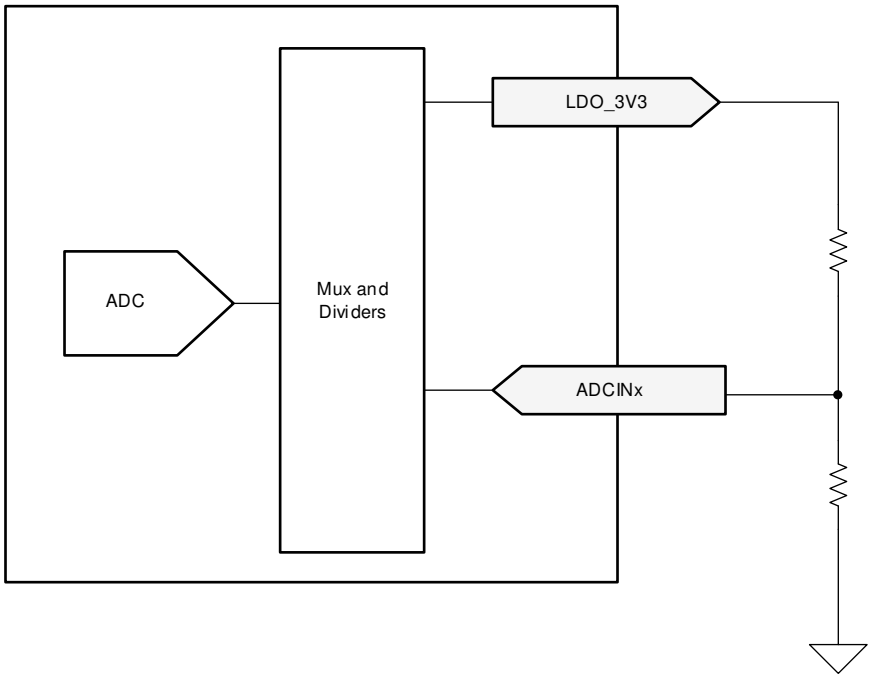


図 8-17. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCINx pins. The following table shows the decoded values for different resistor divider ratios. See *I^2C Address Setting* for details on how ADCINx decoded values affects default I^2C target address.

表 8-1. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without Using R_{UP} or R_{DOWN}	ADCINx Decoded Value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0

表 8-1. Decoding of ADCIN1 and ADCIN2 Pins (続き)

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without Using R_{UP} or R_{DOWN}	ADCINx Decoded Value
MIN	Target	MAX		
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) See *I²C Address Setting* to see the exact meaning of I²C Address Index.

8.3.7 ADC

The TPS25730 ADC is shown in 図 8-18. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

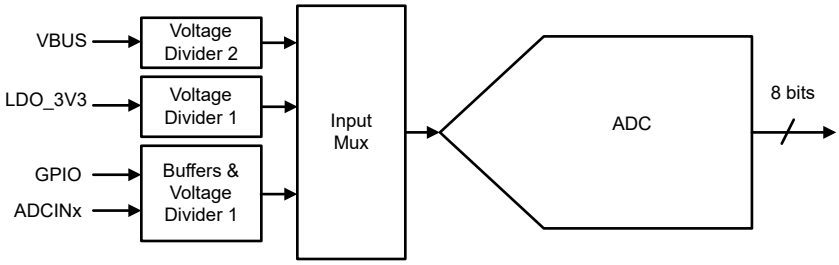


図 8-18. SAR ADC

8.3.8 Digital Interfaces

The TPS25730 contains several different digital interfaces which can be used for communicating with other devices. The available interfaces include an I2C target and preconfigured GPIO.

8.3.9 Digital Core

図 8-19 shows a simplified block diagram of the digital core.

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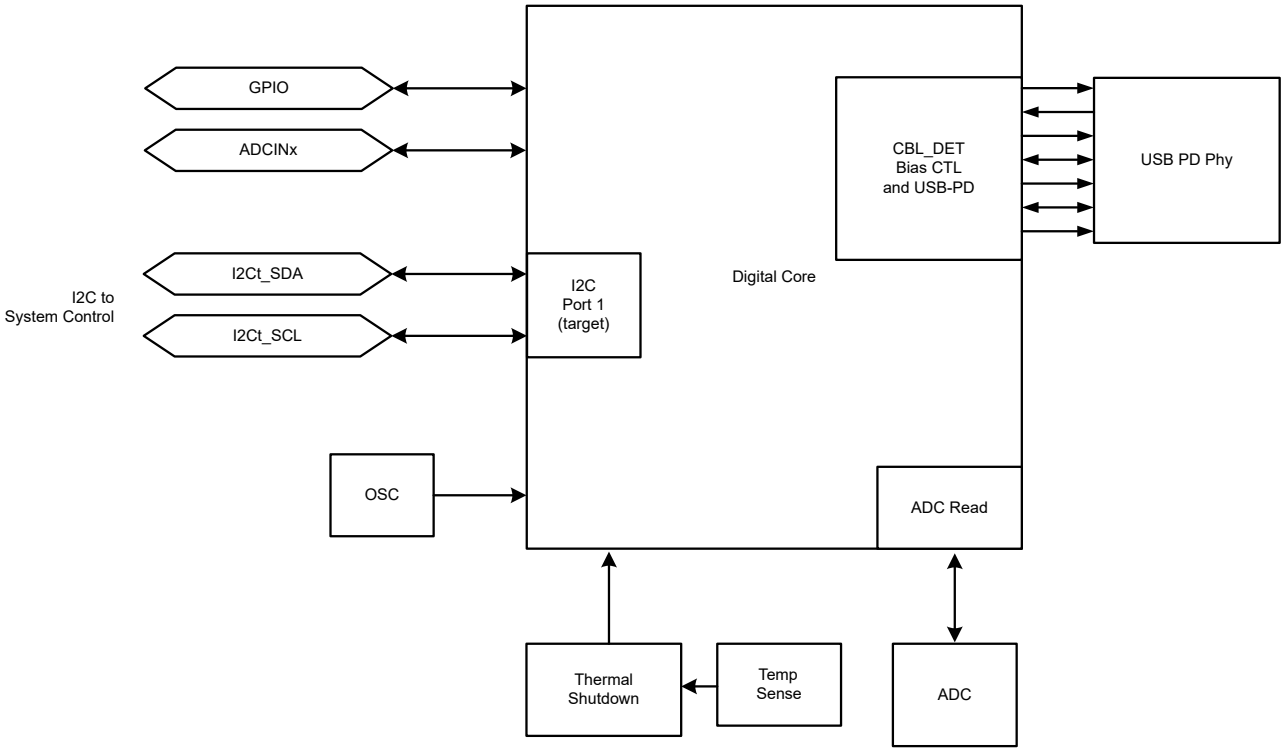


図 8-19. Digital Core Block Diagram

8.3.10 I²C Interface

The TPS25730 has one I2C target interface ports: I2Ct. I2C port I2Ct is comprised of the I2Ct_SDA and I2Ct_SCL pins. This interface provide general status information about the TPS25730, as well as the ability to control the TPS25730 behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS25730 is in 'APP ' mode TI recommends to use standard mode or Fast mode (that is a clock speed no higher than 400 kHz).

表 8-2. I²C Summary

I²C BUS	TYPE	TYPICAL USAGE
I2Ct	Target	Optionally can be connected to an external MCU. Also used to load the patch and application configuration.

8.3.10.1 I²C Interface Description

The TPS25730 supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer can be initiated only when the bus is not busy.

A controller sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

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Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

図 8-20 shows the start and stop conditions of the transfer. 図 8-21 shows the SDA and SCL signals for transferring a bit. 図 8-22 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

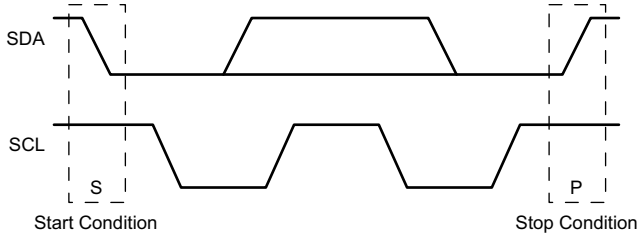


図 8-20. I²C Definition of Start and Stop Conditions

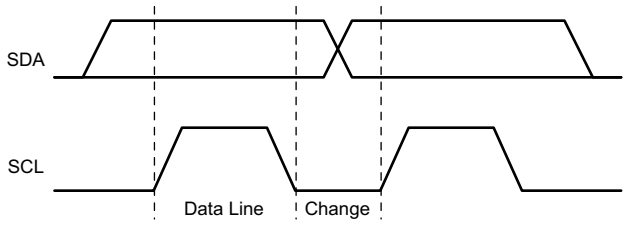


図 8-21. I²C Bit Transfer

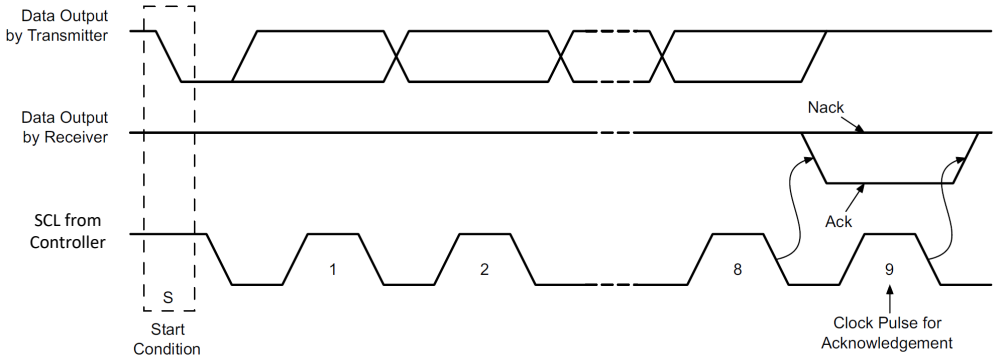


図 8-22. I²C Acknowledgment

8.3.10.1.1 I²C Clock Stretching

The TPS25730 features clock stretching for the I²C protocol. The TPS25730 target I²C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

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The controller must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse can be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.10.1.2 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C controller and a single TPS25730. The I²C target sub-address is used to receive or respond to Host Interface protocol commands. 図 8-23 and 図 8-24 show the write and read protocol for the I²C target interface, and a key is included in 図 8-25 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

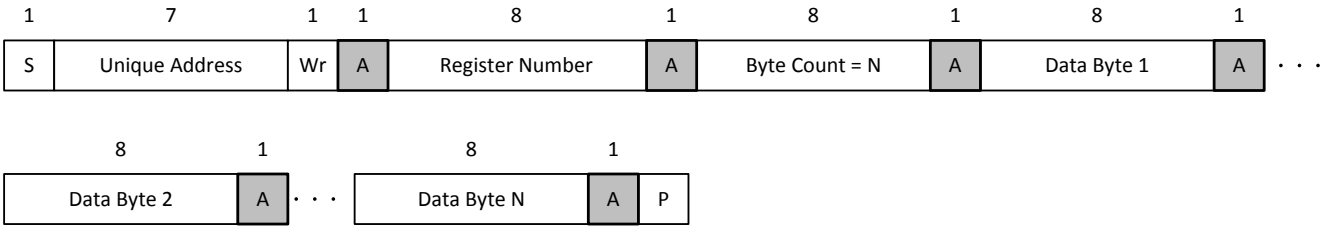


図 8-23. I²C Unique Address Write Register Protocol

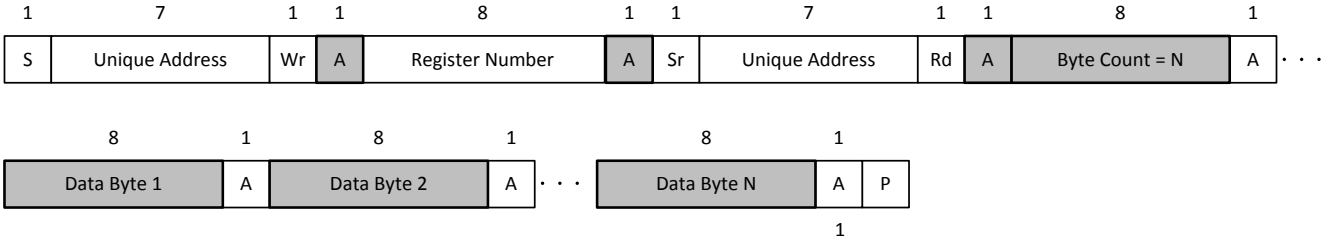
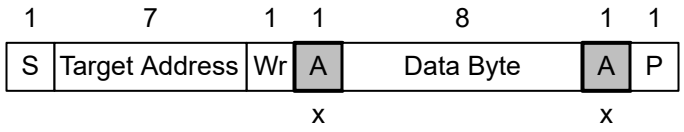


図 8-24. I²C Unique Address Read Register Protocol



S Start condition
SR Repeated start condition
Rd Read (bit value of 1)
Wr Write (bit value of 0
X Field is required to have the value x
A Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)
P Stop condition

Controller-to-target

Target-to-controller

Continuation of protocol

図 8-25. I²C Read/Write Protocol Key

8.3.10.1.3 Pin Strapping to Configure Default Behavior

During the boot procedure, the device reads the ADCINx pins and sets the I²C address and configuration based on the table below.

表 8-3. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 DECODED VALUE (MIN VOLTAGE) (1)	ADCIN2 DECODED VALUE (MAX VOLTAGE) (1)	I²C ADDRESS	DEAD BATTERY CONFIGURATION
0 (5V)	7 (20V)	0x20	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
1 (9V)	7 (20V)	0x21	
2 (12V)	7 (20V)	0x20	
3 (15V)	7 (20V)	0x21	
4 (20V)	7 (20V)	0x20	
0 (5V)	5 (15V)	0x20	
1 (9V)	5 (15V)	0x21	
2 (12V)	5 (15V)	0x20	
3 (15V)	5 (15V)	0x21	
0 (5V)	3 (12V)	0x20	
1 (9V)	3 (12V)	0x21	
2 (12V)	3 (12V)	0x20	
0 (5V)	1 (9V)	0x20	
1 (9V)	1 (9V)	0x21	

(1) See セクション 8.3.6 for how to configure a given ADCINx decoded value.

8.3.11 Minimum Voltage Configuration

The minimum voltage for the USB Power Delivery Sink Capabilities can be set according to the table below. When the received USB PD Source Capabilities do not meet the minimum and maximum voltage range the Capabilities Mismatch bit is set on the USB PD request. When the Minimum Voltage is set greater than 5 V the Higher Capability bit is set in the Sink Capabilities.

表 8-4. Minimum Voltage Configuration for Sink Capabilities - ADCIN1 Decoded

ADCIN1 Decoded Value	Minimum Voltage Configuration
0	5 V
1	9 V
2	12 V
3	15 V
4	20 V
5	Reserved
6	Reserved
7	Reserved

8.3.12 Maximum Voltage Configuration

The maximum voltage for the USB Power Delivery Sink Capabilities is set according to the table below. When the received USB PD Source Capabilities do not meet the minimum and maximum voltage range the Capabilities Mismatch bit is set on the USB PD request.

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表 8-5. Maximum Voltage Configuration for Sink Capabilities - ADCIN2 Decoded

ADCIN2 Decoded Value	Maximum Voltage Configuration
1	9 V
3	12 V
5	15 V
7	20 V

8.3.13 Sink Current Configuration

The sink current is configured according to the table below. The configuration sets Operating and Maximum Current in the USB PD request message. The Operating Current is defined as the the current required for the sink to be functional. The Maximum Current is defined as the maximum current the sink may use. The Operating and Maximum Current can be the same if the Operational Current is the maximum current required for the sink to be functional. The Capabilities Mismatch bit is set when the PD Source Capabilities do not meet the Operating Current. When the Operating Current is set to 0 A the Capability Mismatch bit is not set.

表 8-6. ADCIN3 & ADCIN4 Sink Current Configuration

ADCIN3	ADCIN4	Operating Current	Maximum Current
0	0	0	1.5 A
0	1	0	3 A
0	2	0	4 A
0	3	0	5 A
0	4	0.5 A	1.5 A
0	5	0.5 A	3 A
0	6	0.5 A	4 A
0	7	0.5 A	5 A
1	0	1 A	1.5 A
1	1	1 A	3 A
1	2	1 A	4 A
1	3	1 A	5 A
1	4	1.5 A	1.5 A
1	5	1.5 A	3 A
1	6	1.5 A	4 A
1	7	1.5 A	5 A
2	1	2 A	3 A
2	2	2 A	4 A
2	3	2 A	5 A
2	5	2.5 A	3 A
2	6	2.5 A	4 A
2	7	2.5 A	5 A
3	1	3 A	3 A
3	2	3 A	4 A
3	3	3 A	5 A

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表 8-6. ADCIN3 & ADCIN4 Sink Current Configuration (続き)

ADCIN3	ADCIN4	Operating Current	Maximum Current
3	6	3.5 A	4 A
3	7	3.5 A	5 A
4	2	4 A	4 A
4	3	4 A	5 A
4	7	4.5 A	5 A
5	3	5 A	5 A

8.3.14 Autonegotiate Sink Minimum Power

The minimum power required is determined by the Operating Current configuration multiplied by the Minimum Voltage configuration. When the received PD Source Capabilities power do not meet the Autonegotiate Sink Minimum Power the Capability Mismatch bit is set in the PD Request message.

表 8-7. Autonegotiate Sink Minimum Power Example

ADCIN1	ADCIN2	Minimum Voltage	Maximum Voltage	ADCIN3	ADCIN4	Operating Current	Maximum Current	Minimum Power
0	4	5 V	15 V	3	1	3 A	3 A	15 W
0	6	5 V	20 V	5	3	5 A	5 A	25 W

8.3.15 Extended Sink Capabilities Power Delivery Power

The Extend Sink Capabilities Power Delivery Power for Minimum, Operational, and Maximum PDP are determined by the configured Maximum/Minimum Voltage Configuration and the Current Configuration.

表 8-8. Extended Sink Capabilities Power Delivery Power Example

Power Delivery Power	ADCIN3/4 = 3/3	ADCIN1/2 = 0/6
Minimum PDP = 25W	Maximum Current = 5 A	Minimum Voltage = 5 V
Operational PDP = 100W	Maximum Current = 5 A	Maximum Voltage = 20 V
Maximum PDP = 100W	Maximum Current = 5 A	Maximum Voltage = 20 V

8.4 Device Functional Modes

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8.4.1 Power States

The TPS25730 can operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in 表 8-9. The device automatically transitions between the three power states based on the circuits that are active and required. See 図 8-26. In the Sleep state, the TPS25730 detects a Type-C connection. Transitioning between the Active mode to Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I^2C transactions
- Voltage alert
- Fault alert

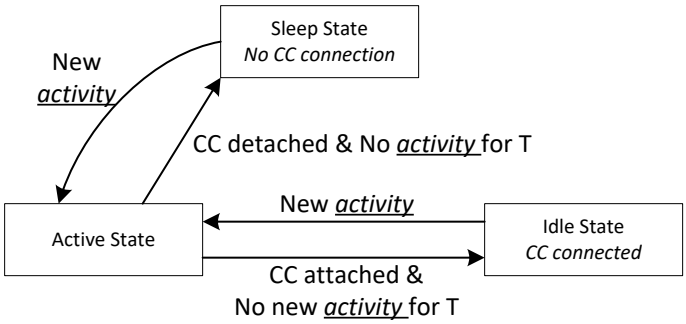


図 8-26. Flow Diagram for Power States

表 8-9. Power Consumption States

	ACTIVE SINK MODE(3)	IDLE SINK MODE	MODERN STANDBY SINK MODE(2)	SLEEP MODE(1)
PP_HV (TPS25730D)	enabled	enabled	disabled	disabled
PP_EXT (TPS25730S)	enabled	enabled	disabled	disabled
external CC1 termination	Rp 3.0A	Rp 3.0A	open	open
external CC2 termination	open	open	open	open

(1) This mode is used for: $I_{VIN_3V3,Sleep}$
(2) This mode is used for: $P_{MstbySnk}$
(3) This mode is used for: $I_{VIN_3V3,ActSnk}$

8.5 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25730 during sudden disconnects due to inductive effects in a cable, TI recommends that a Schottky diode be placed from VBUS to ground.

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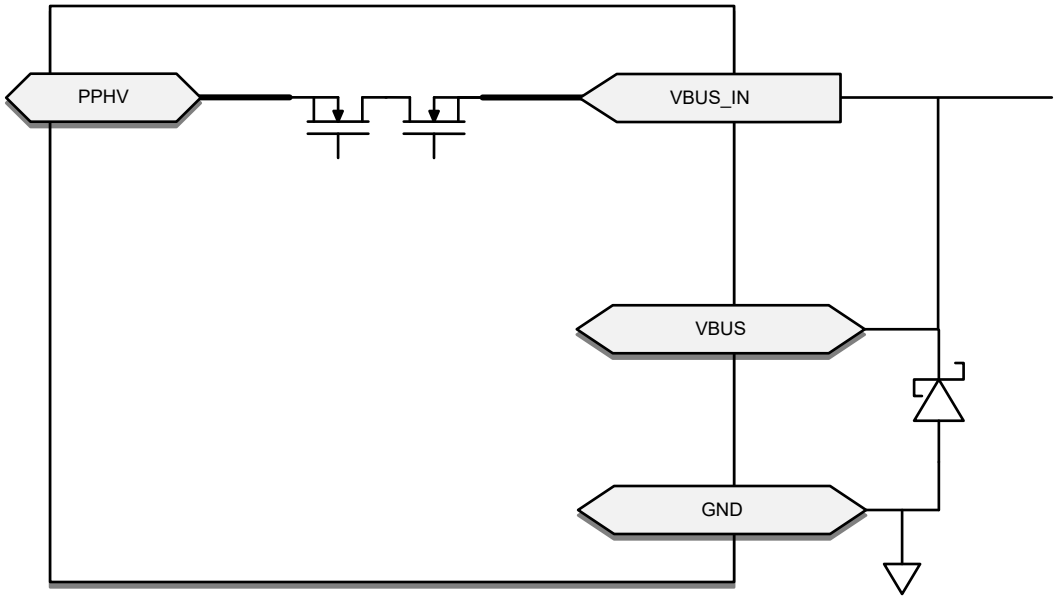


図 8-27. TPS25730D Schottky for Current Surge Protection

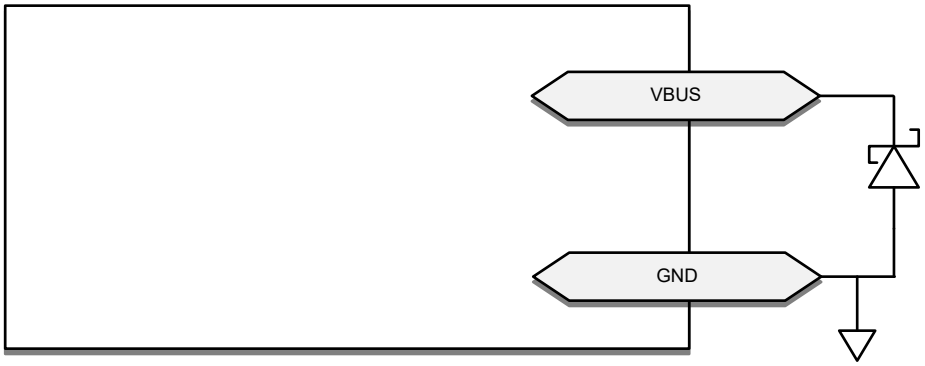


図 8-28. TPS25730S Schottky for Current Surge Protection

8.6 Thermal Shutdown

The TPS25730 features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

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9 Application and Implementation

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9.1 Application Information

The TPS25730 is a stand-alone Type-C PD controller for sink power only USB-PD applications. The PD controller is configured from with resistor pin strapping to set the appropriate voltage and current requirements. There is no need for an external EEPROM, external microcontroller, or firmware development for a rapid barrel jack to Type-C replacement

9.1.1 Supported Sink Power Configurations

The ADCINx pin configurations on the TPS25730 lets the user select the supported voltage and current range. The following shows two sink configurations for the TPS25730.

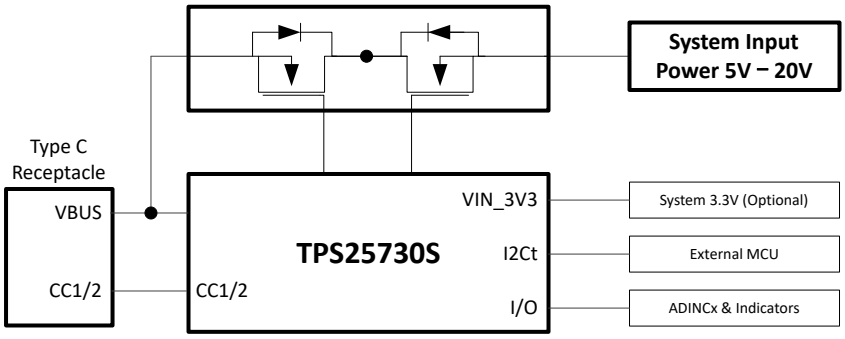


図 9-1. TPS25730S Sink Configuration

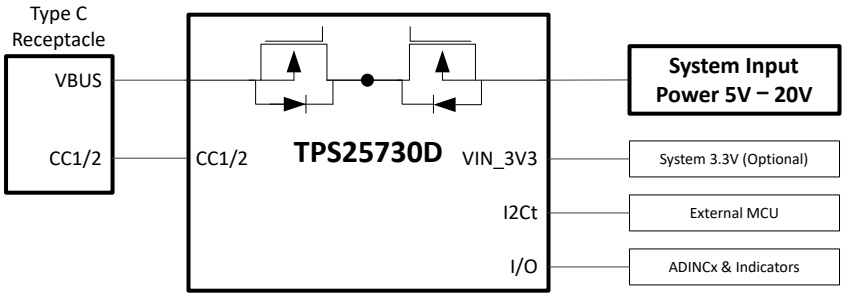


図 9-2. TPS25730D Sink Configuration

9.2 Typical Application

9.2.1 Design Requirements

For barrel jack replacements applications, the TPS25730 is configured to negotiate a PD contract according to the voltage required by the system. The TPS25730 supports 5V, 9V, 12V, 15V, and 20V up to 5A to replace a barrel jack. Power is provided to the system through the power path on the PD controller.

9.2.2 Detailed Design Procedure

The ADCINx pin configurations on the TPS25730 lets the user select the supported voltage and current range. The following shows an example schematic for the TPS25730 configured for 20 V at 3 A.

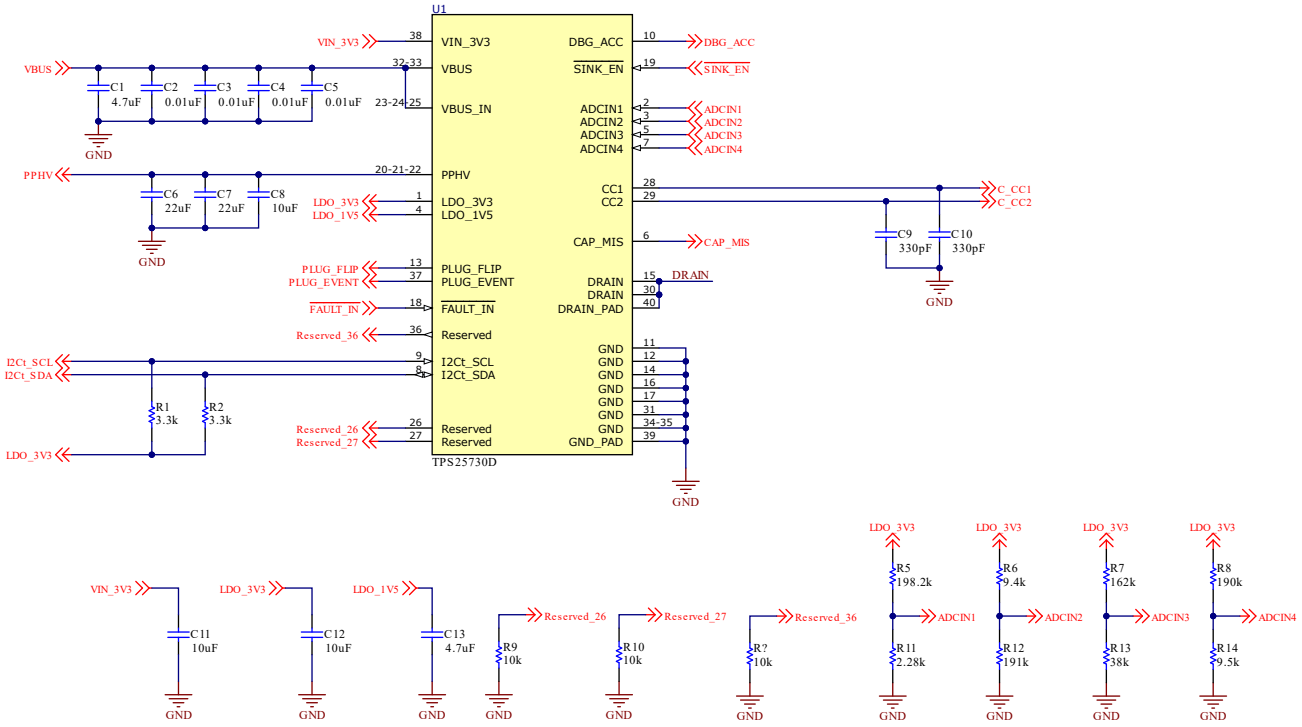


図 9-3. TPS25730D Sink Example Schematic

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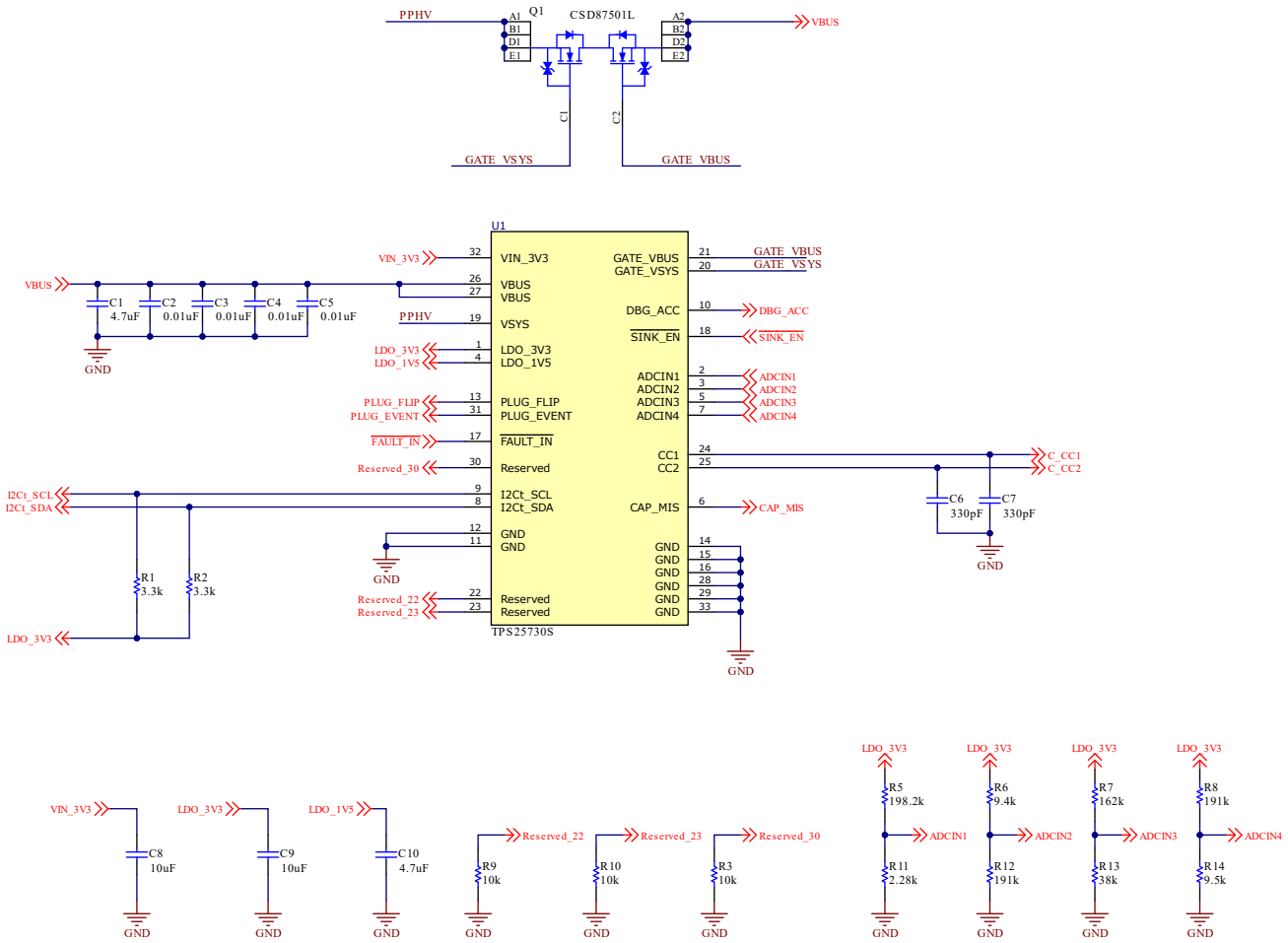


図 9-4. TPS25730S Sink Example Schematic

9.2.3 Application Curves

The following figures show the GPIO, VBUS, CC1, CC2 and PPHV behavior for various conditions.

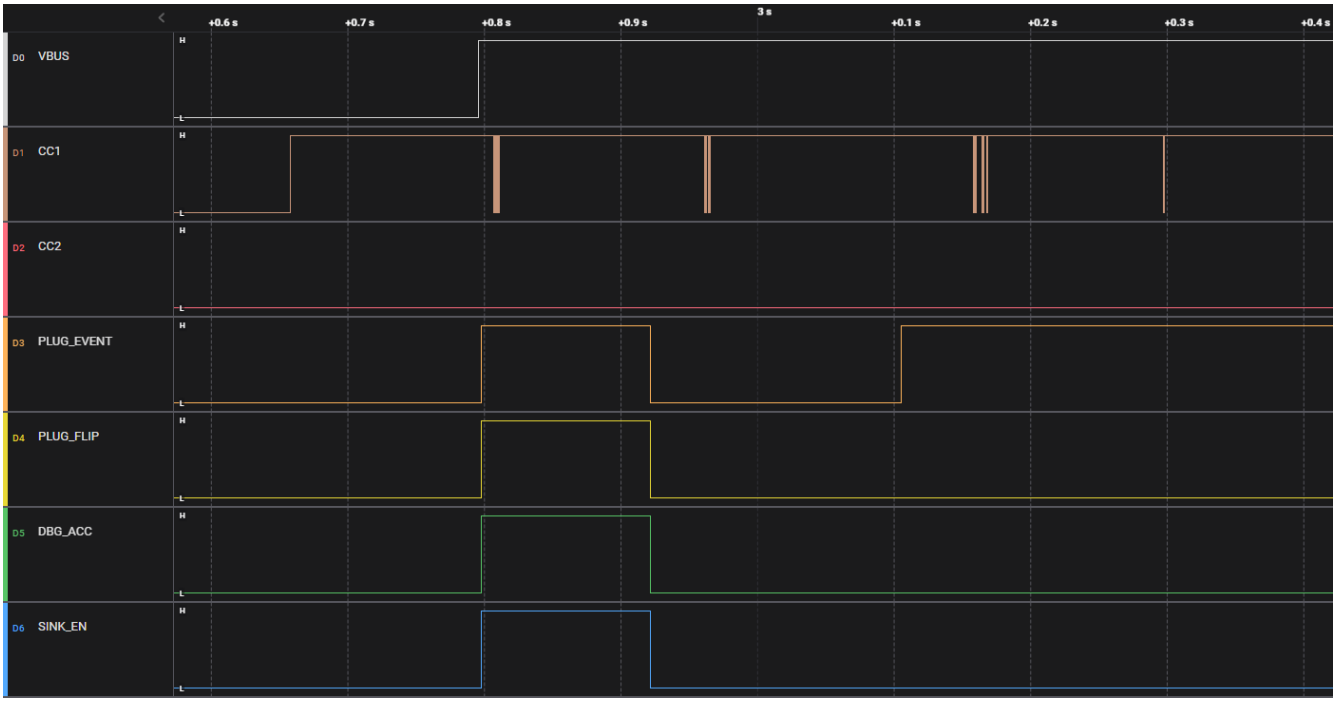


図 9-5. PLUG_EVENT, PLUG_FLIP, DBG_ACC, and $\overline{\text{SINK_EN}}$ - CC1 Normal Orientation

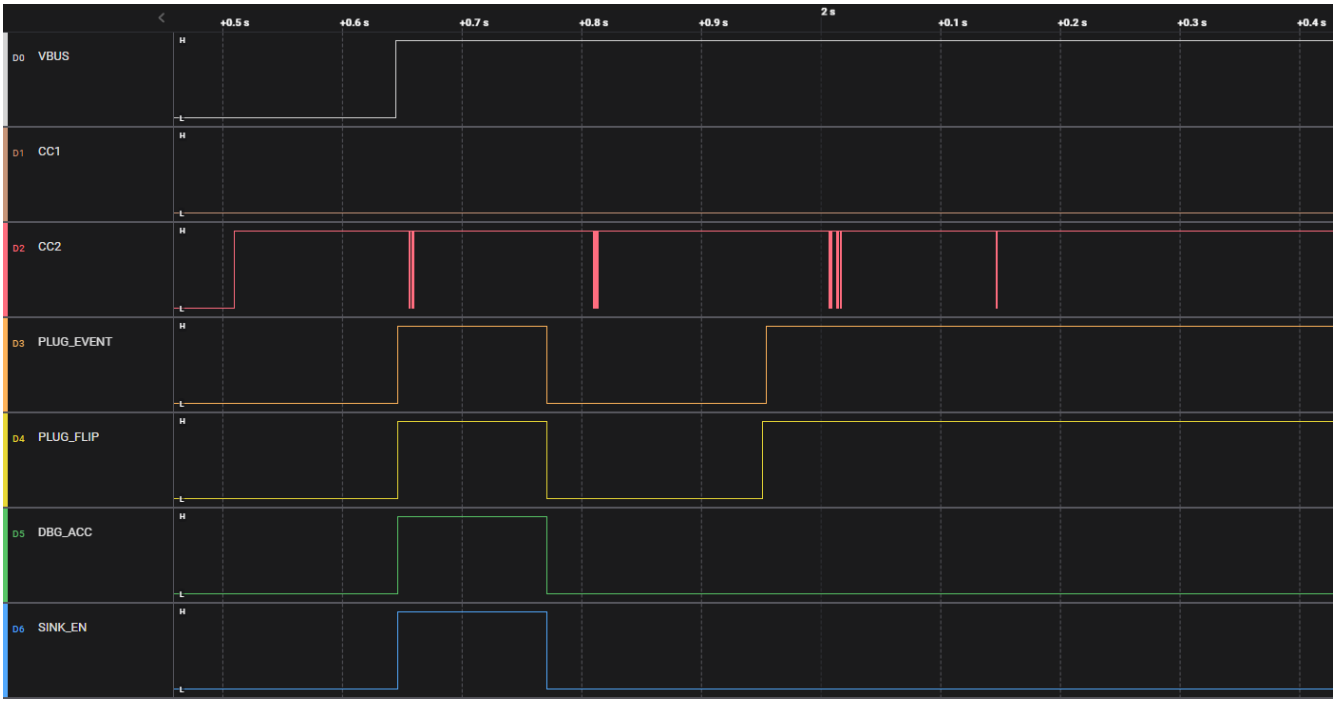


図 9-6. PLUG_EVENT, PLUG_FLIP, DBG_ACC, and $\overline{\text{SINK_EN}}$ - CC2 Flipped Orientation

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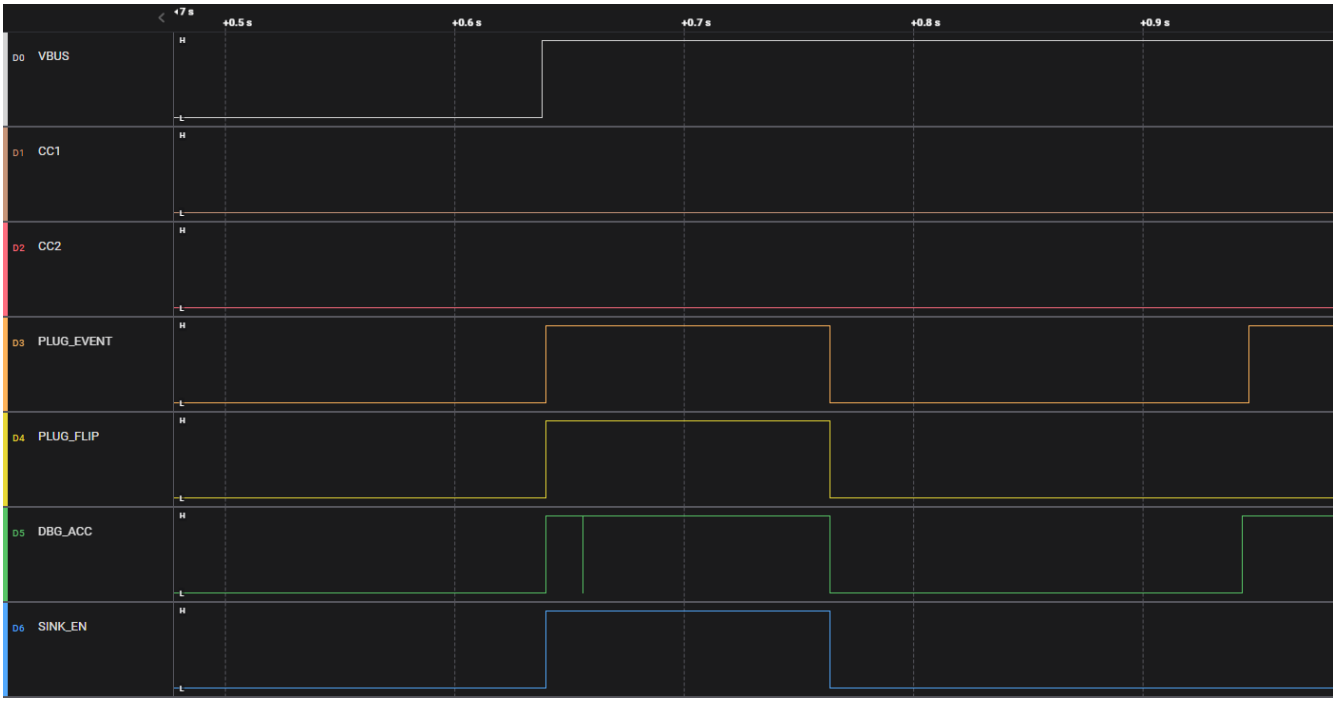


図 9-7. PLUG_EVENT, PLUG_FLIP, DBG_ACC, and $\overline{\text{SINK_EN}}$ - Debug Accessory Detection

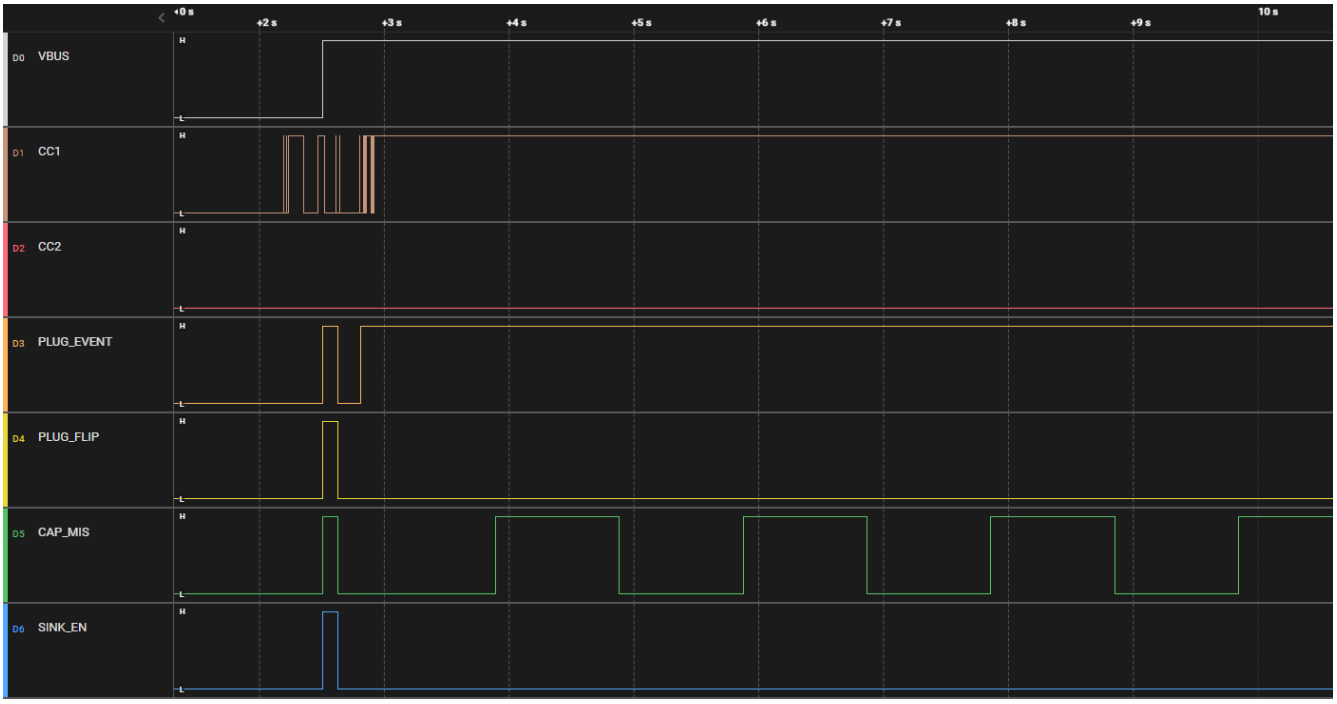


図 9-8. PLUG_EVENT, PLUG_FLIP, CAP_MIS, and $\overline{\text{SINK_EN}}$ - PD Contract w/ Capabilities Mismatch

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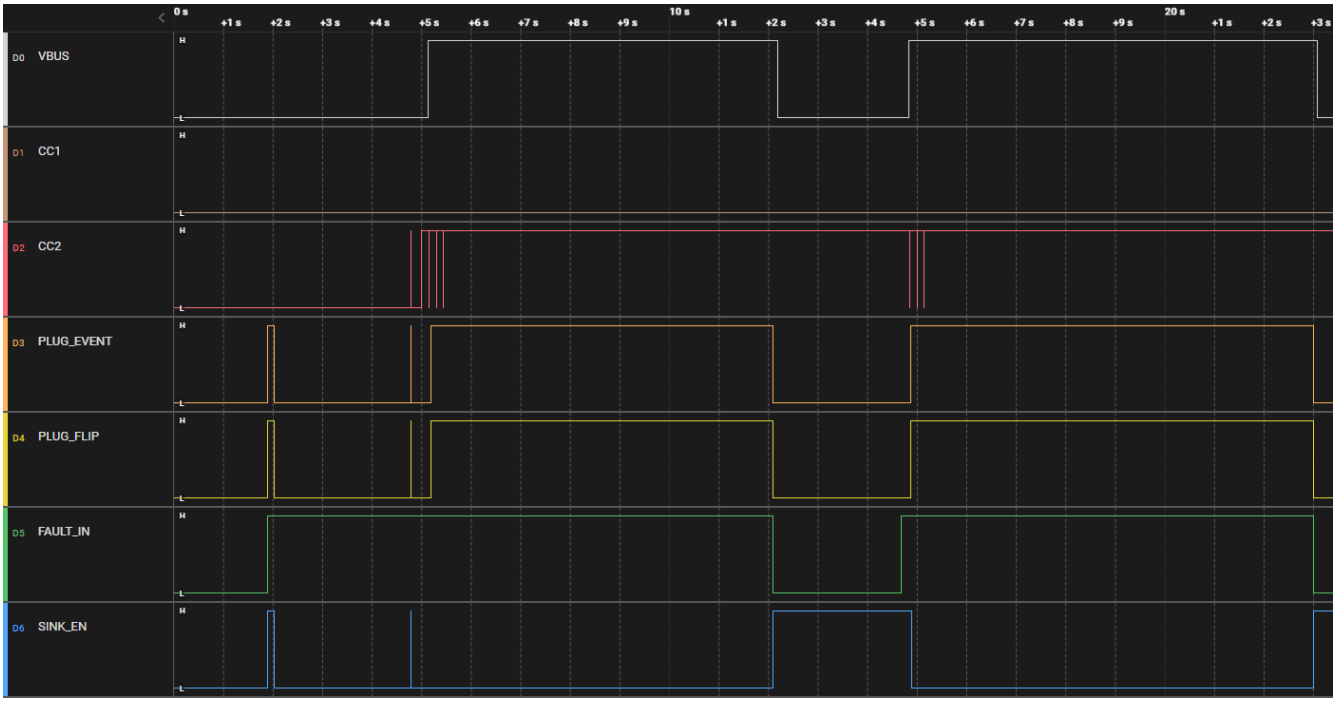


図 9-9. PLUG_EVENT, PLUG_FLIP, $\overline{\text{FAULT_IN}}$, and $\overline{\text{SINK_EN}}$ - $\overline{\text{FAULT_IN}}$ Input

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図 9-10. 20V PD Contract VBUS & PPHV (1-VBUS, 2-CC1, 3-CC2, 4-PPHV)

9.3 Power Supply Recommendations

9.3.1 3.3-V Power

9.3.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS25730 device. The VIN_3V3 switch (see *Power Management*) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3-V supply is available and the dead-battery flag is cleared. The recommended capacitance C_{VIN_3V3} (see *Recommended Capacitance*) must be connected from the VIN_3V3 pin to the GND pin).

9.3.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see *Recommended Capacitance*) from the LDO_1V5 pin to the GND pin.

9.3.3 Recommended Supply Load Capacitance

Recommended Capacitance lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible.

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The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

9.4 Layout

9.4.1 TPS25730D - Layout

9.4.1.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

9.4.1.1.1 Top Placement and Bottom Component Placement and Layout

When the TPS25730 is placed on top and its components on bottom, the solution size is at its smallest.

9.4.1.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25730.

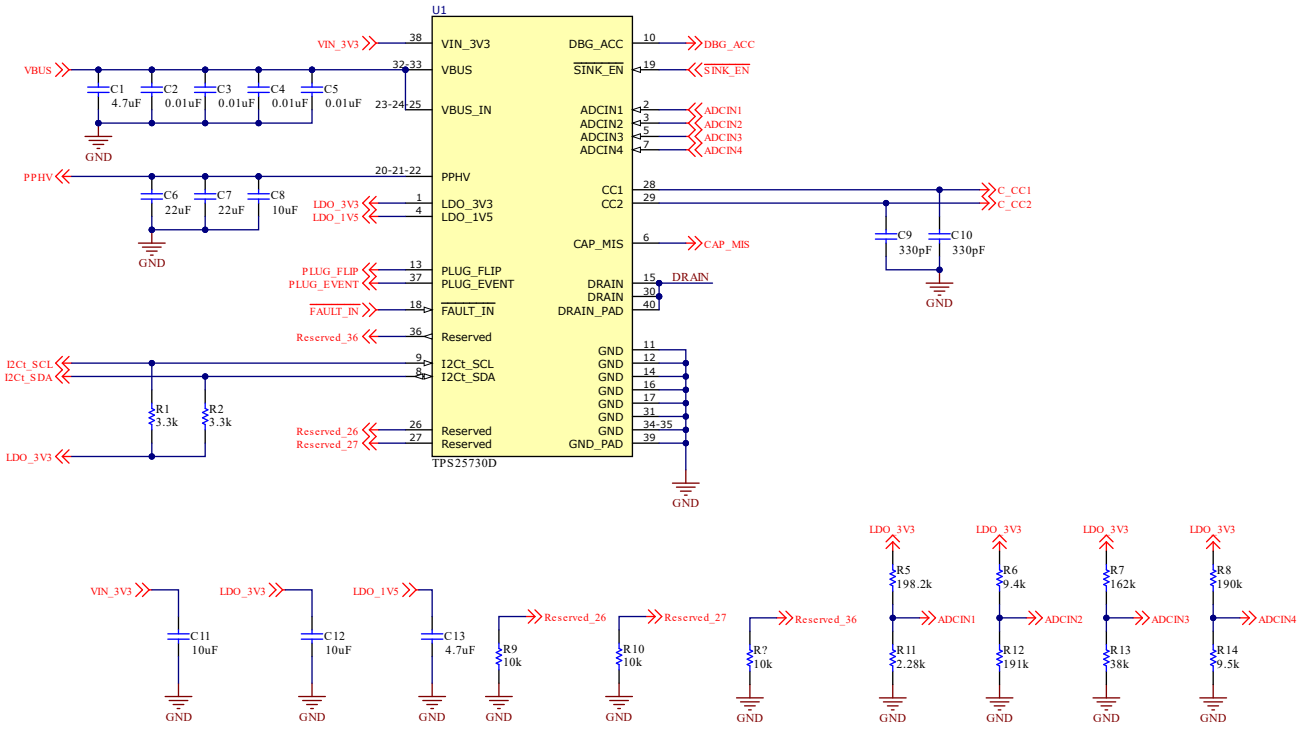


図 9-11. Example Schematic

9.4.1.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25730D is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, TI recommends that they are placed directly under the TPS25730D. When placing the VBUS and PPHV capacitors, it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS25730D or to the side because the drain connection pads on the bottom layer must not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS25730D must be placed where the GND terminal is underneath the GND pad.

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The CC capacitors must be placed on the same side as the TPS25730D close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

図 9-12 through 図 9-13 show the placement in 2-D and 3-D.

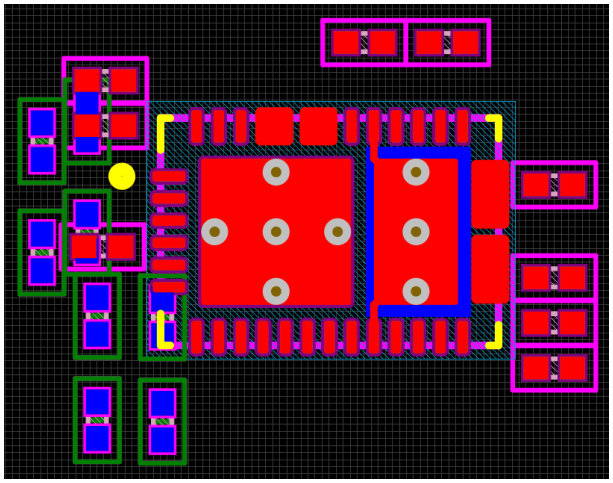


図 9-12. Top View Layout

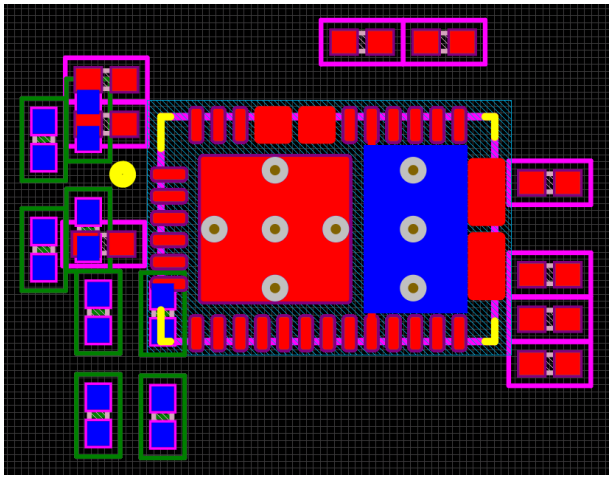


図 9-13. Bottom View Layout

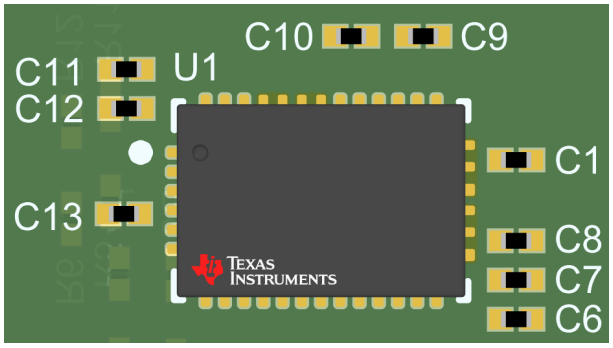


図 9-14. Top View 3-D

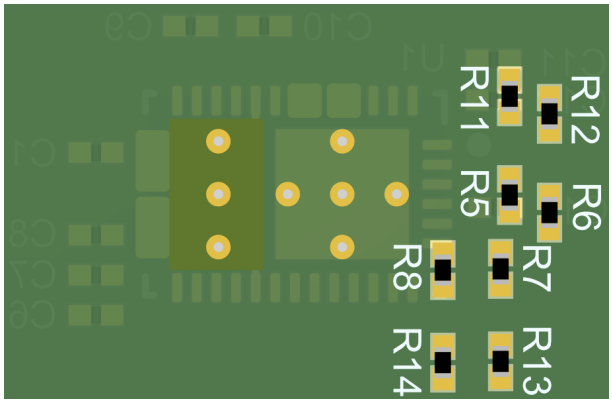


図 9-15. Bottom View 3-D

9.4.1.4 Routing VBUS, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for VBUS, VBUS_IN, and PPHV. Connect VBUS from the top layer to the bottom layer using at least 6 8-mil hole and 16-mil diameter vias. See 図 9-16 for the recommended via sizing. For VBUS_IN and PPHV, connect from the top to bottom layer using 15 8-mil hole and 16-mil diameter vias. The via placement and copper pours are highlighted in 図 9-17.

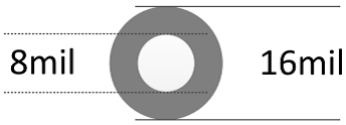


図 9-16. Recommended Minimum Via Sizing

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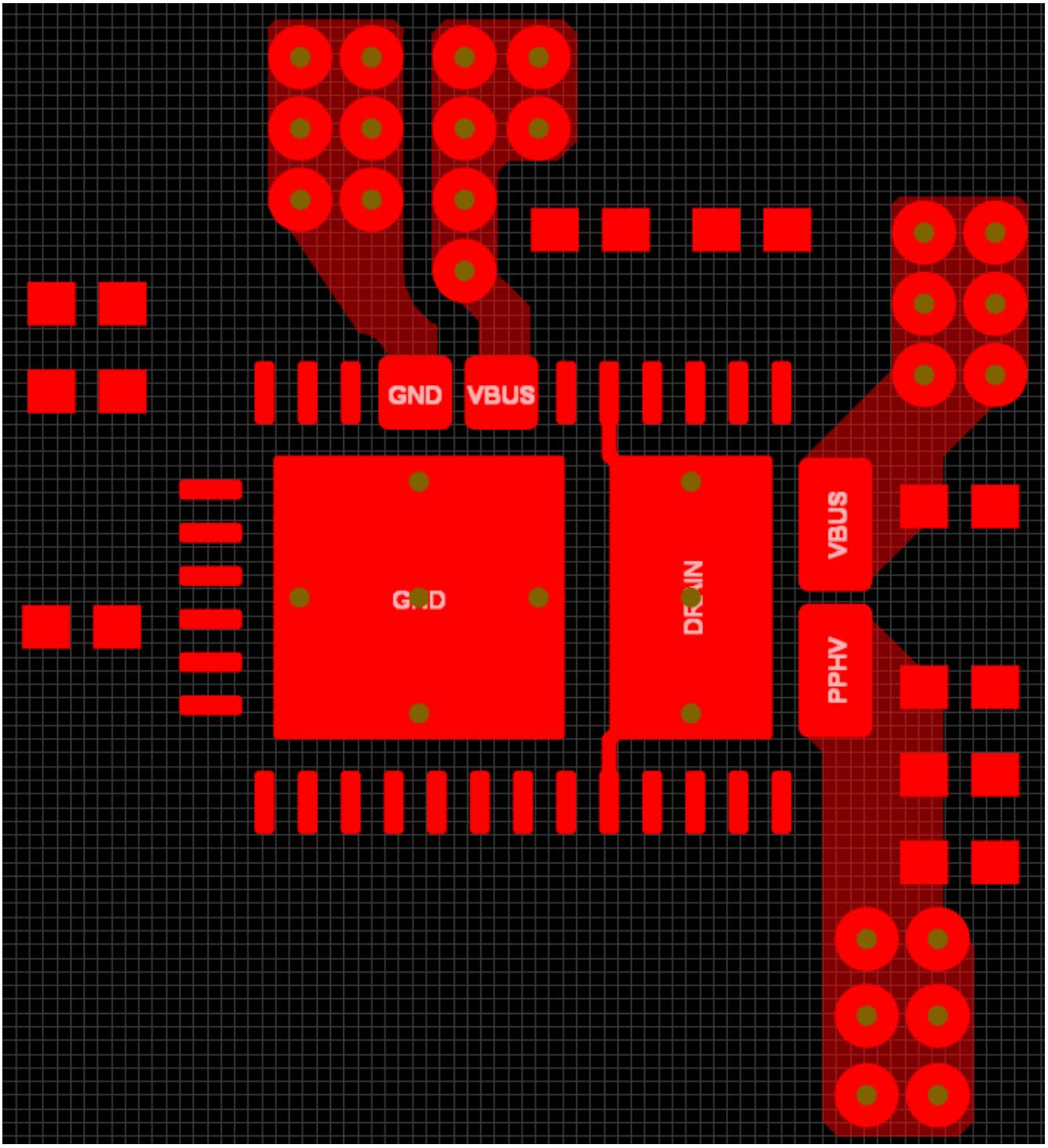


図 9-17. VBUS, VBUS_IN, and PPHV Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 route to their respective decoupling capacitors. Additionally, a copper pour on the bottom side is added to connect PPHV to their decoupling capacitors located on the bottom of the PCB. This action is highlighted in 図 9-18.

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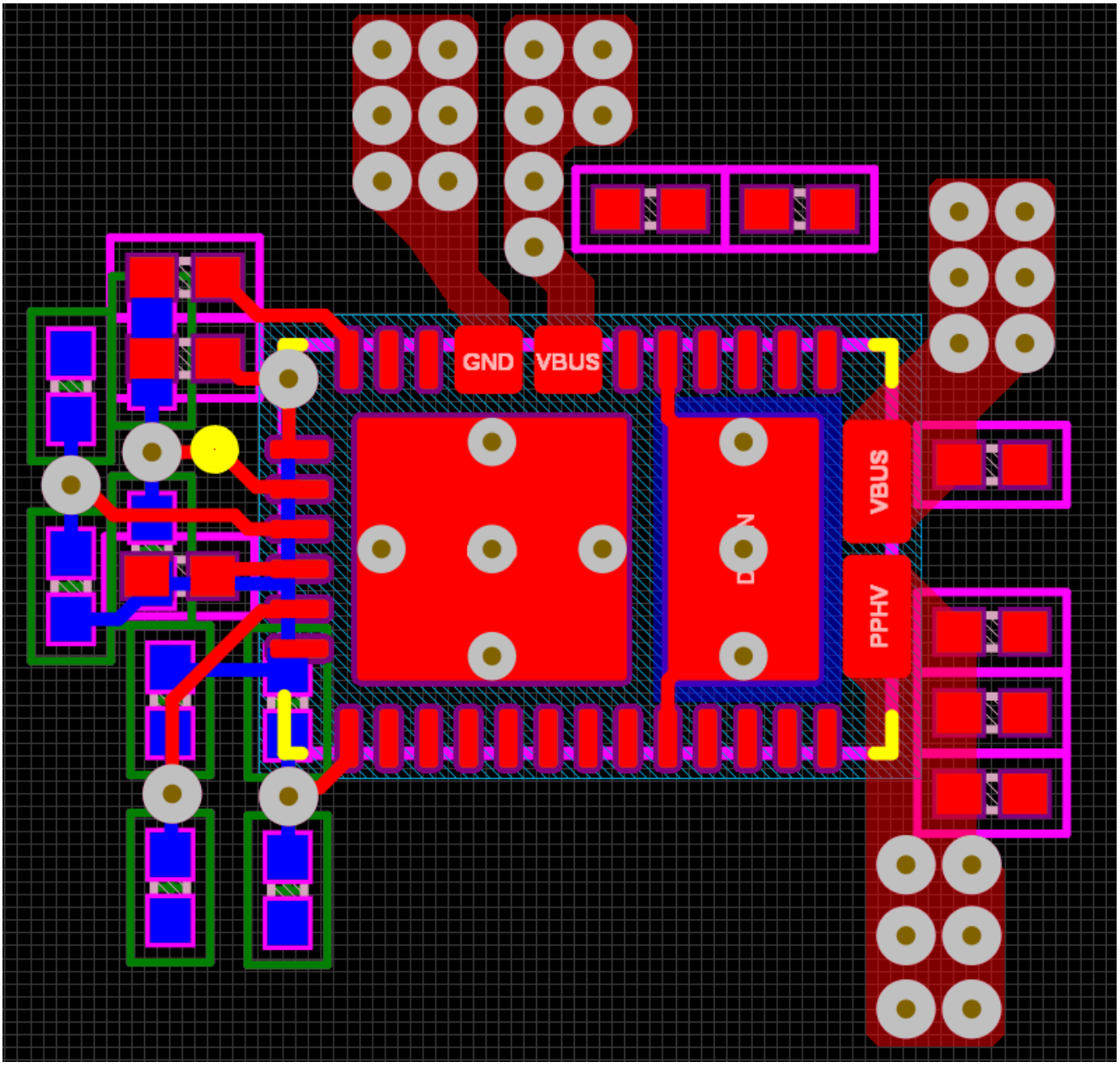


図 9-18. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

9.4.1.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace ensures the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil or 10-mil trace. The following images highlights how the CC lines and GPIOs are routed out.

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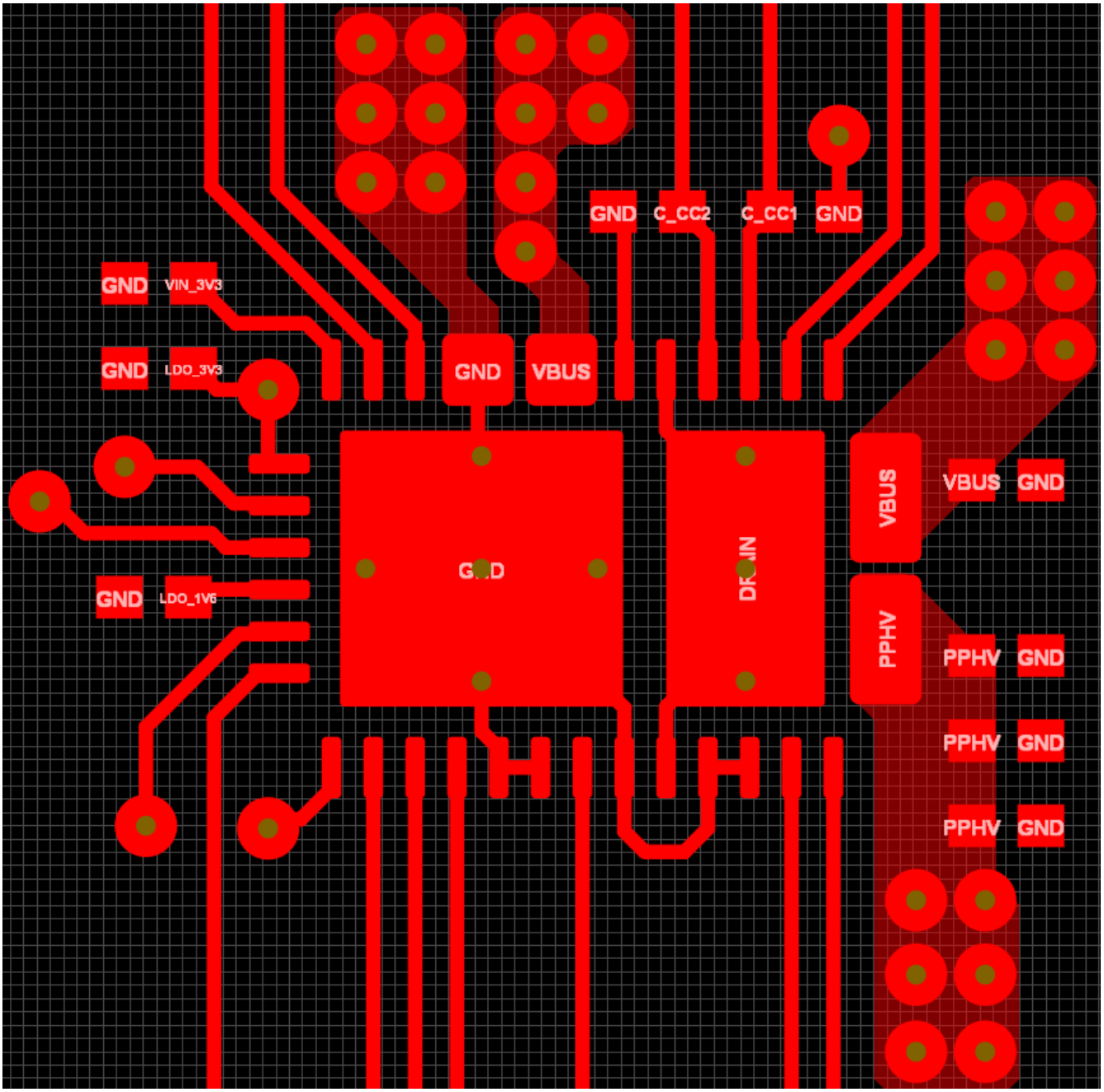


図 9-19. Top Layer GPIO Routing

表 9-1. Routing Widths

ROUTE	WIDTH (MIL MINIMUM)
CC1, CC2	8
VIN_3V3, LDO_3V3, LDO_1V8	8
Component GND	10
GPIO	8

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9.4.2 TPS25730S - Layout

9.4.2.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

9.4.2.1.1 Top Placement and Bottom Component Placement and Layout

When the TPS25730 is placed on top and its components on bottom, the solution size is at its smallest.

9.4.2.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25730S.

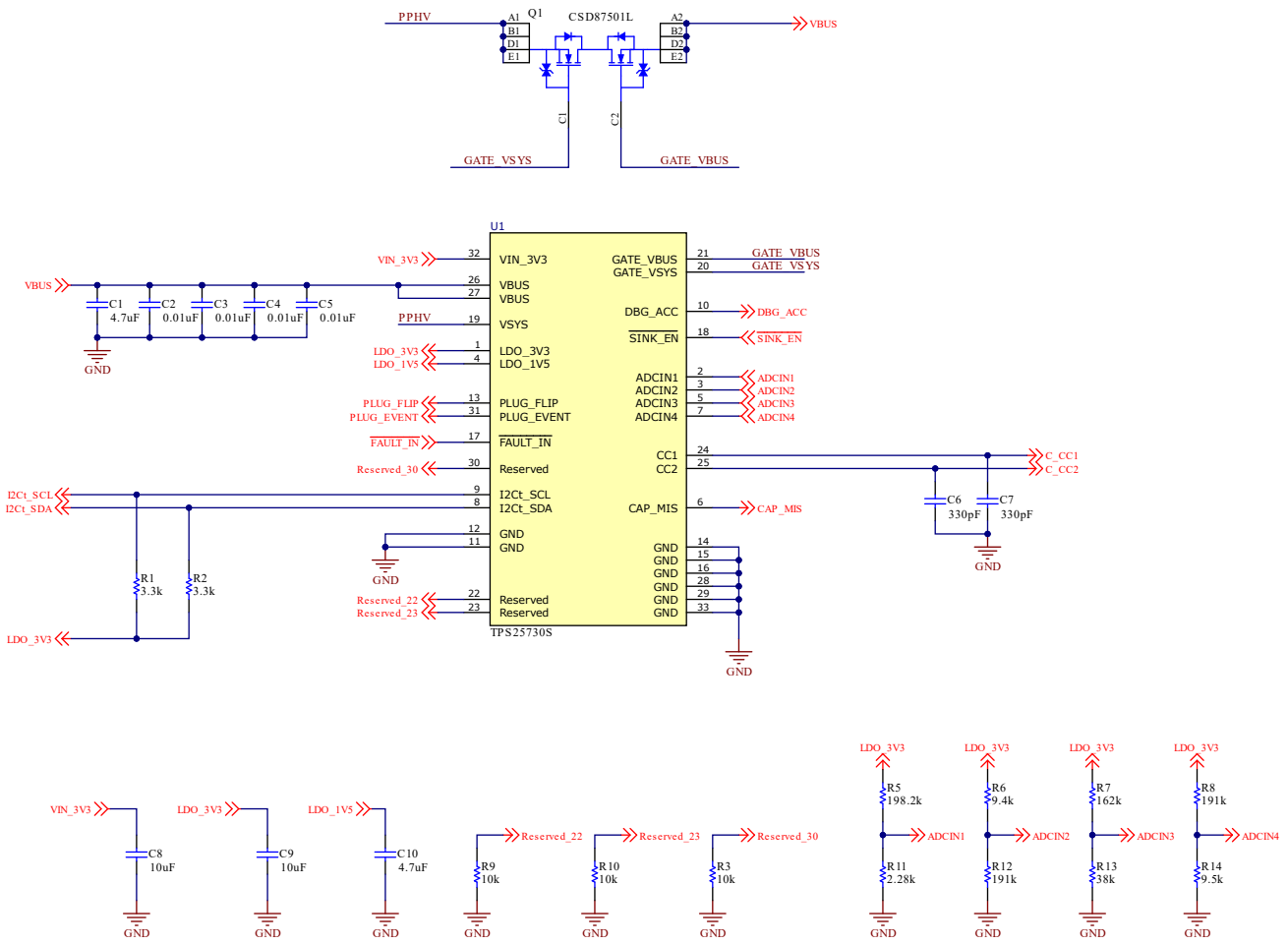


図 9-20. Example Schematic

9.4.2.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25730S is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, TI recommends that they are placed directly under the TPS25730S. All other components that are for pins on the GND pad side of the TPS25730S must be placed where the GND terminal is underneath the GND pad.

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The CC capacitors must be placed on the same side as the TPS25730S close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

図 9-21 through 図 9-22 show the placement in 2-D and 3-D.

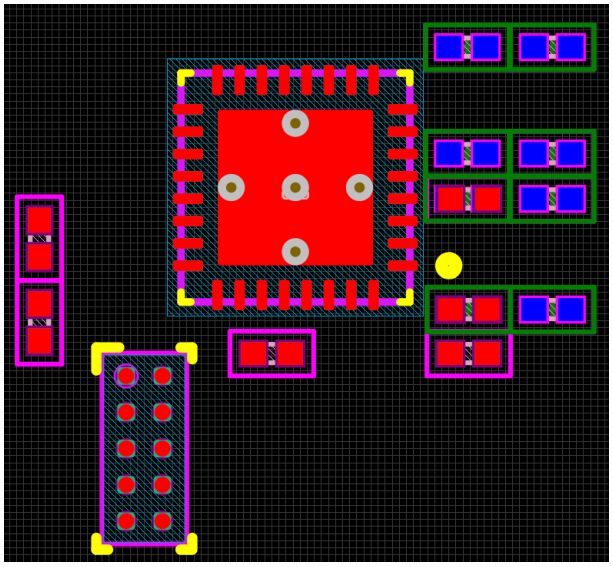


図 9-21. Top View Layout

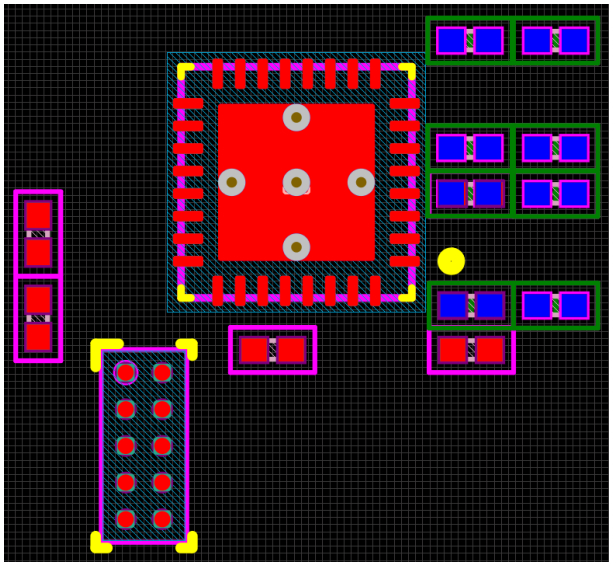


図 9-22. Bottom View Layout

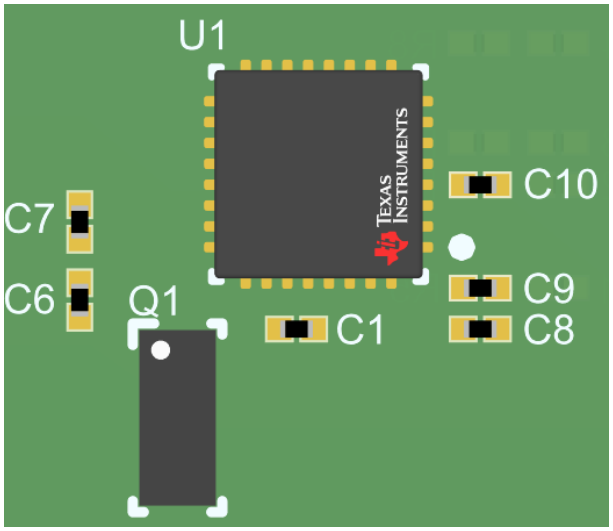


図 9-23. Top View 3-D

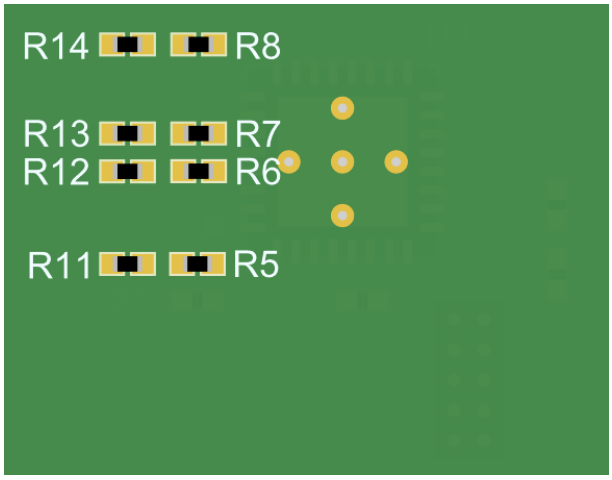


図 9-24. Bottom View 3-D

9.4.2.4 Routing VBUS, PPHV, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for VBUS, and PPHV. Connect PPHV from the top layer to the bottom layer using at least 12, 8-mil hole and 16-mil diameter vias. See 図 9-25 for the recommended via sizing. The via placement and copper pours are highlighted in 図 9-26.

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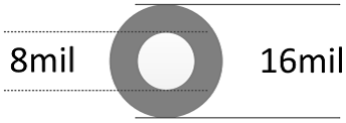


図 9-25. Recommended Minimum Via Sizing

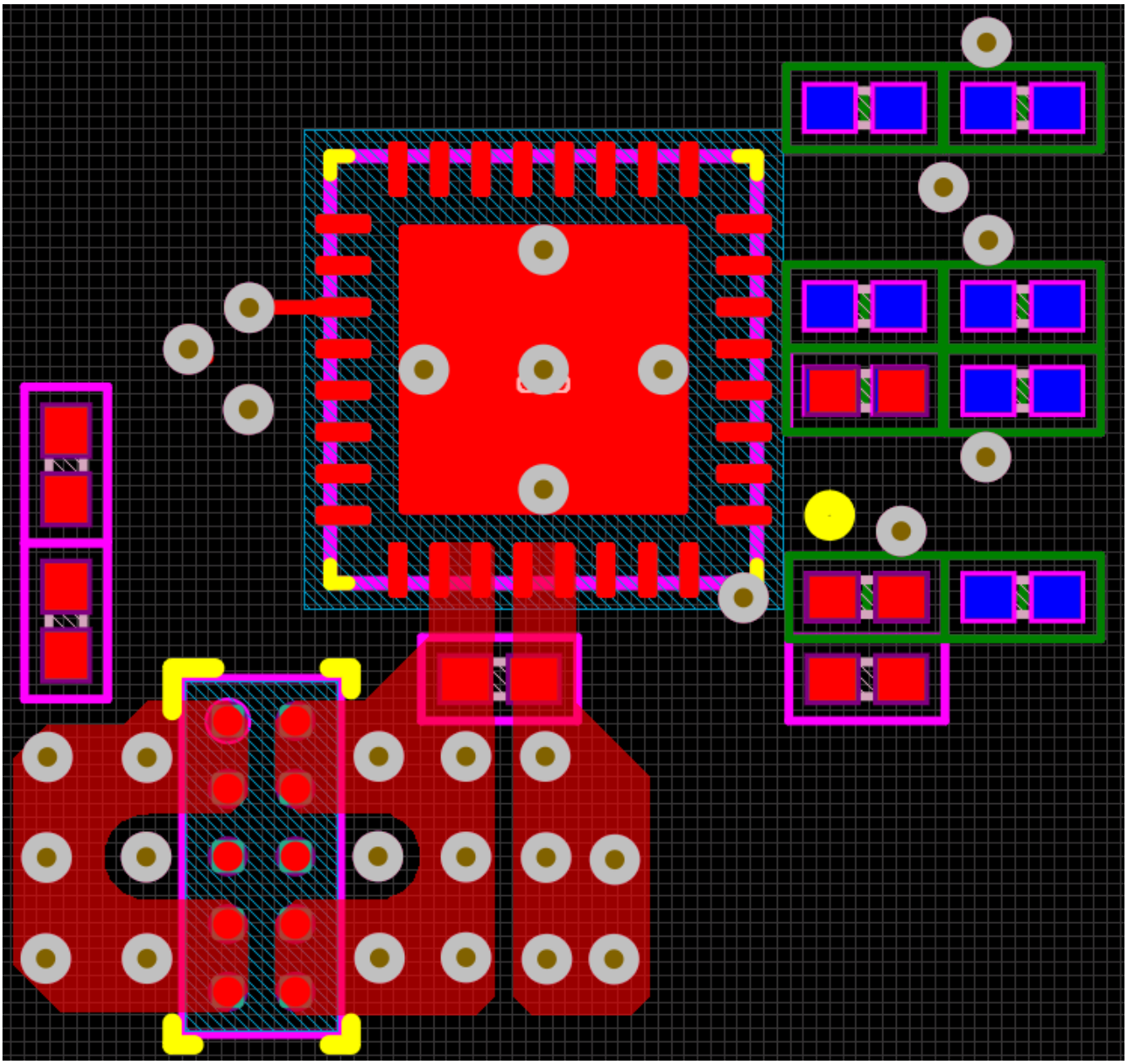


図 9-26. VBUS Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 are routed to their respective decoupling capacitors. This action is highlighted in 図 9-27.

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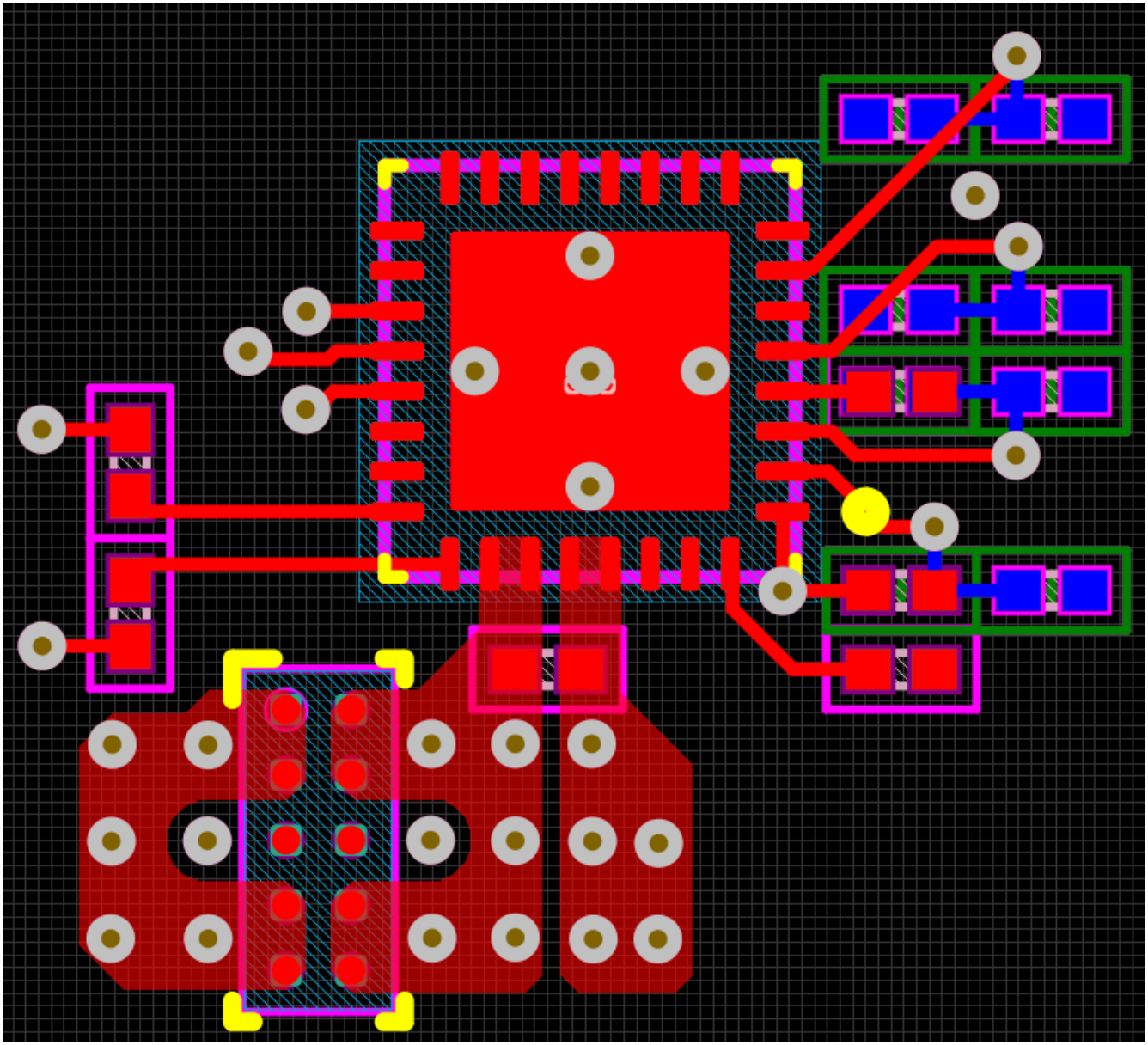


図 9-27. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

図 9-28 and 図 9-29 show how to properly connect VSYS and the SYS_Gate control signals for the external N-FETs. The control signals can be routed on an internal layer using a 12-mil trace, and the trace going to VSYS must be as short as possible to minimize impedance, so placing a via directly on the high-voltage power path is ideal.

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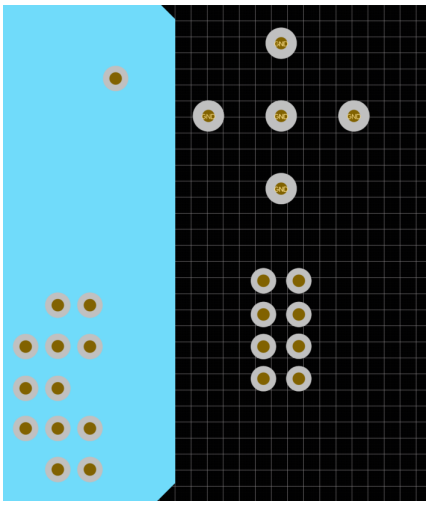


図 9-28. Top Polygon Pours

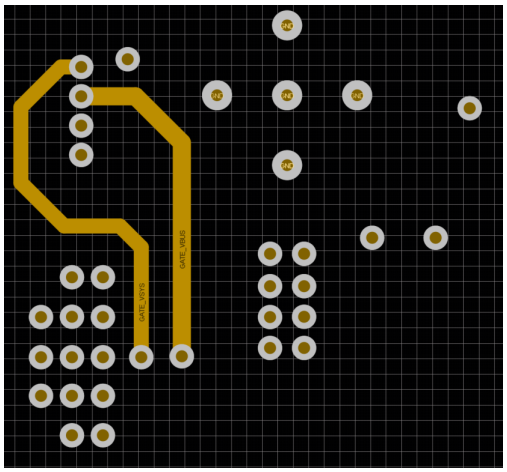


図 9-29. Bottom Polygon Pours

9.4.2.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace ensures the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil trace or a 10-mil trace. The following images highlight how the CC lines and GPIOs are routed out.

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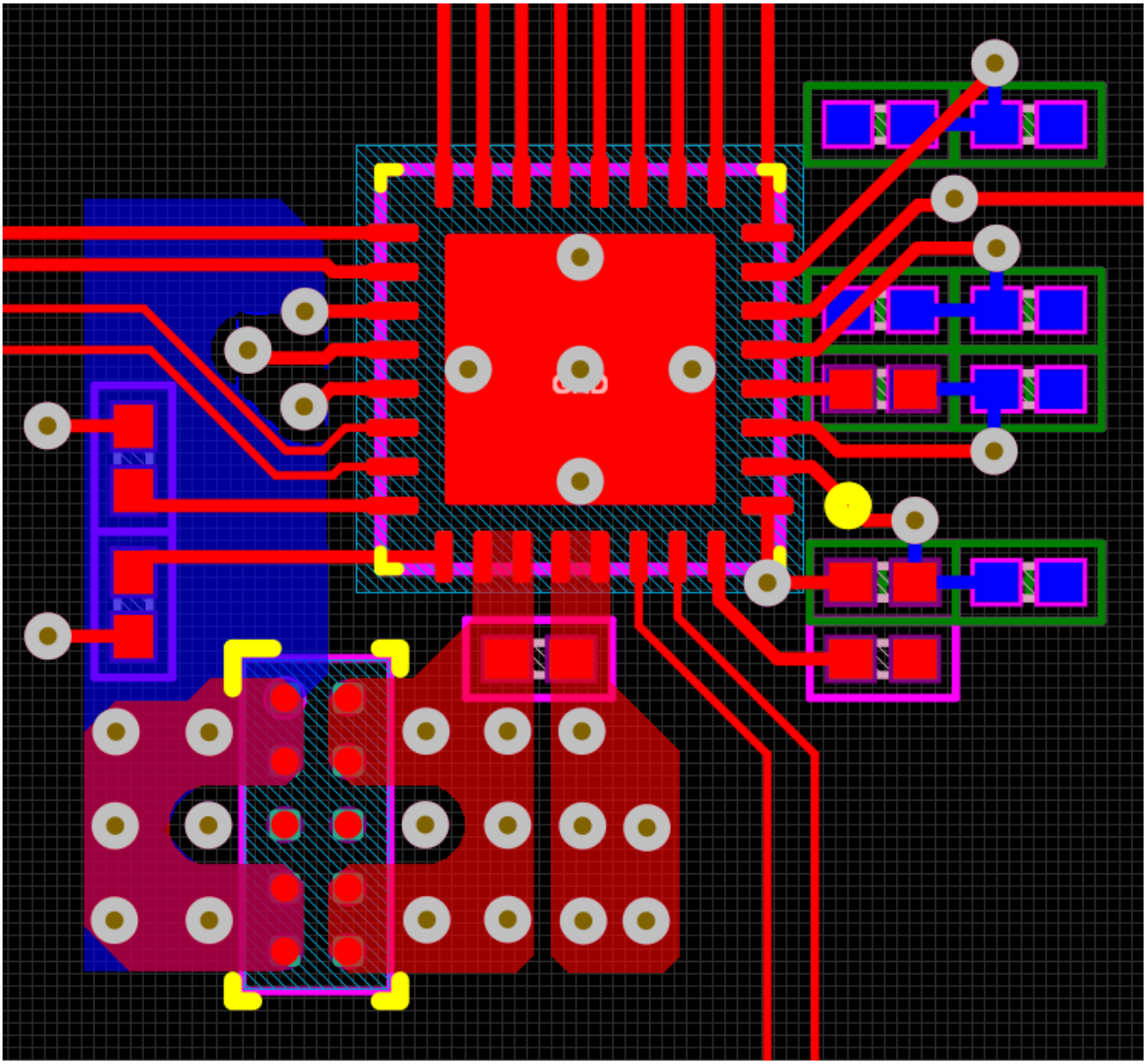


図 9-30. Top Layer GPIO Routing

表 9-2. Routing Widths

ROUTE	WIDTH (MIL MINIMUM)
PA_CC1, PA_CC2, PB_CC1, PB_CC2	8
VIN_3V3, LDO_3V3, LDO_1V8	6
Component GND	10
GPIO	4

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10 Device and Documentation Support

10.1 Device Support

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10.2 Documentation Support

10.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2023	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25730DREFR	Active	Production	WQFN (REF) | 38	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25730D BH
TPS25730DREFR.A	Active	Production	WQFN (REF) | 38	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25730D BH
TPS25730SRSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25730S BH
TPS25730SRSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25730S BH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

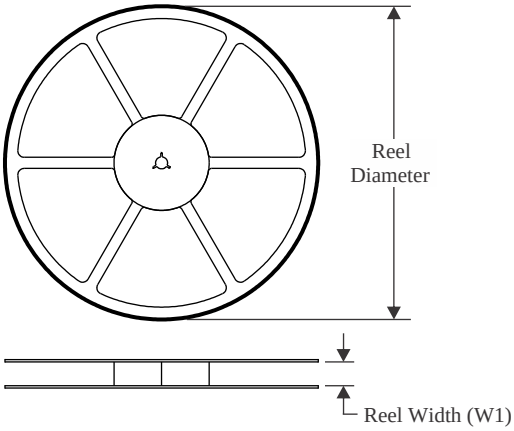
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

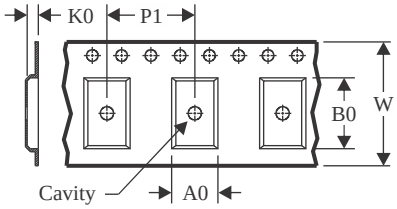
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

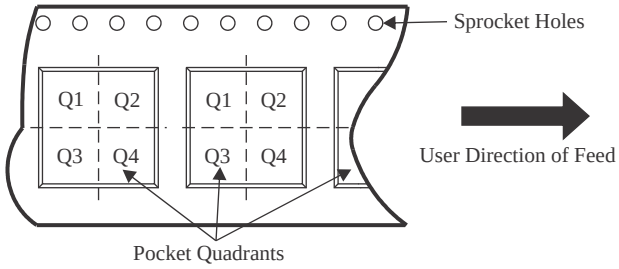


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

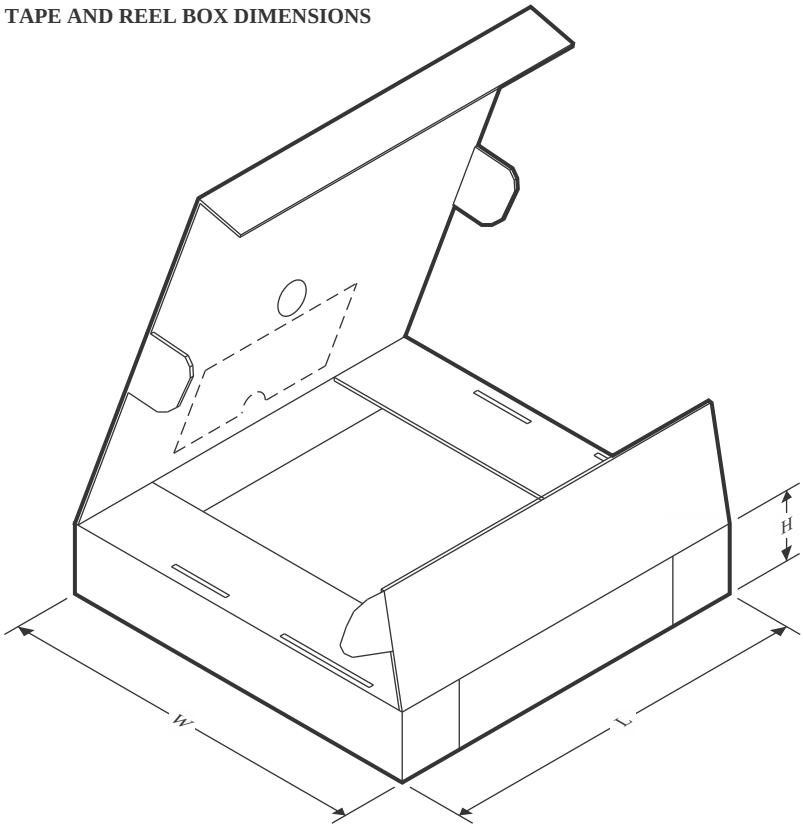
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25730DREFR	WQFN	REF	38	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TPS25730SRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

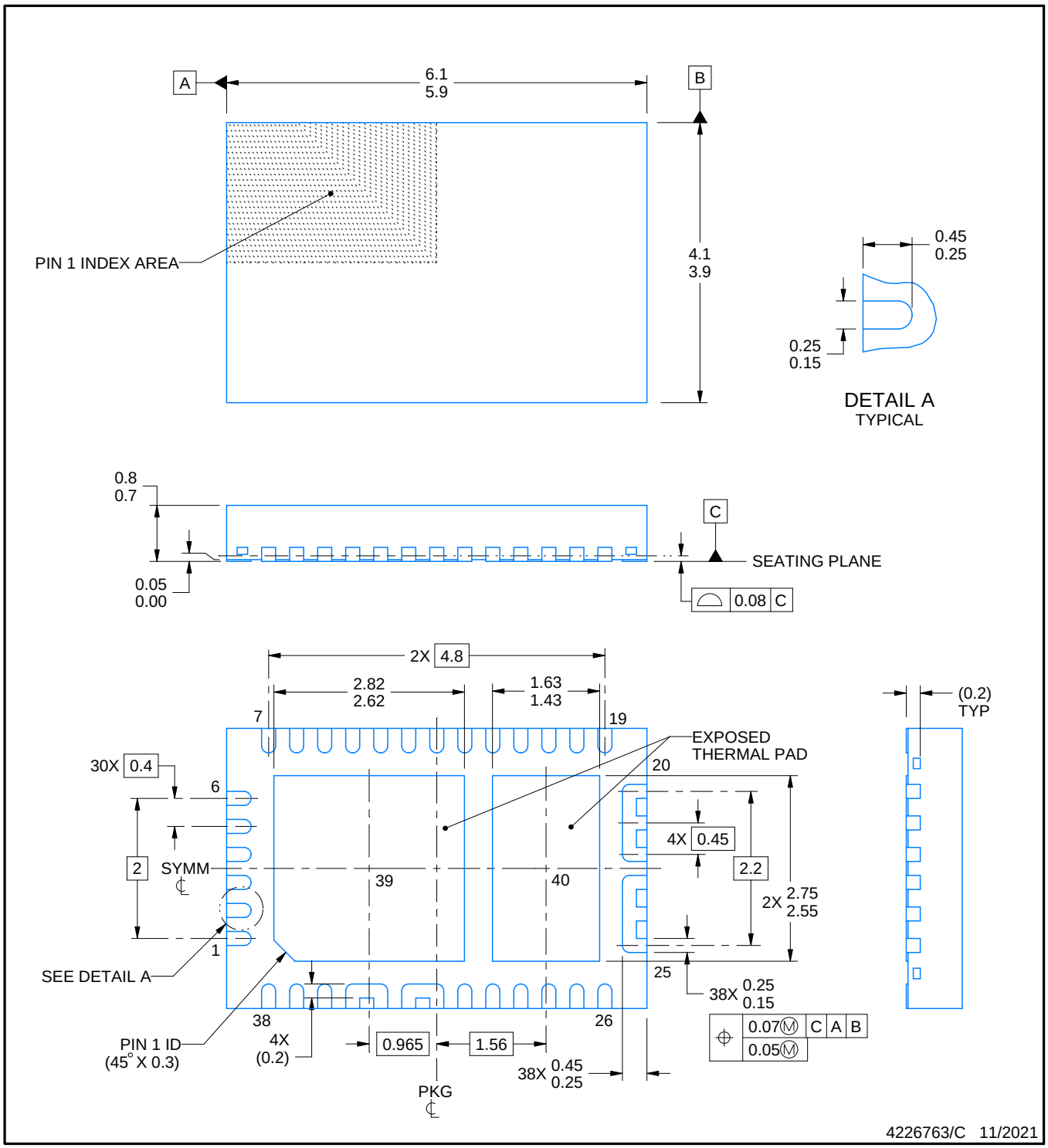
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25730DREFR	WQFN	REF	38	3000	360.0	360.0	36.0
TPS25730SRSMR	VQFN	RSM	32	3000	360.0	360.0	36.0

REF0038A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

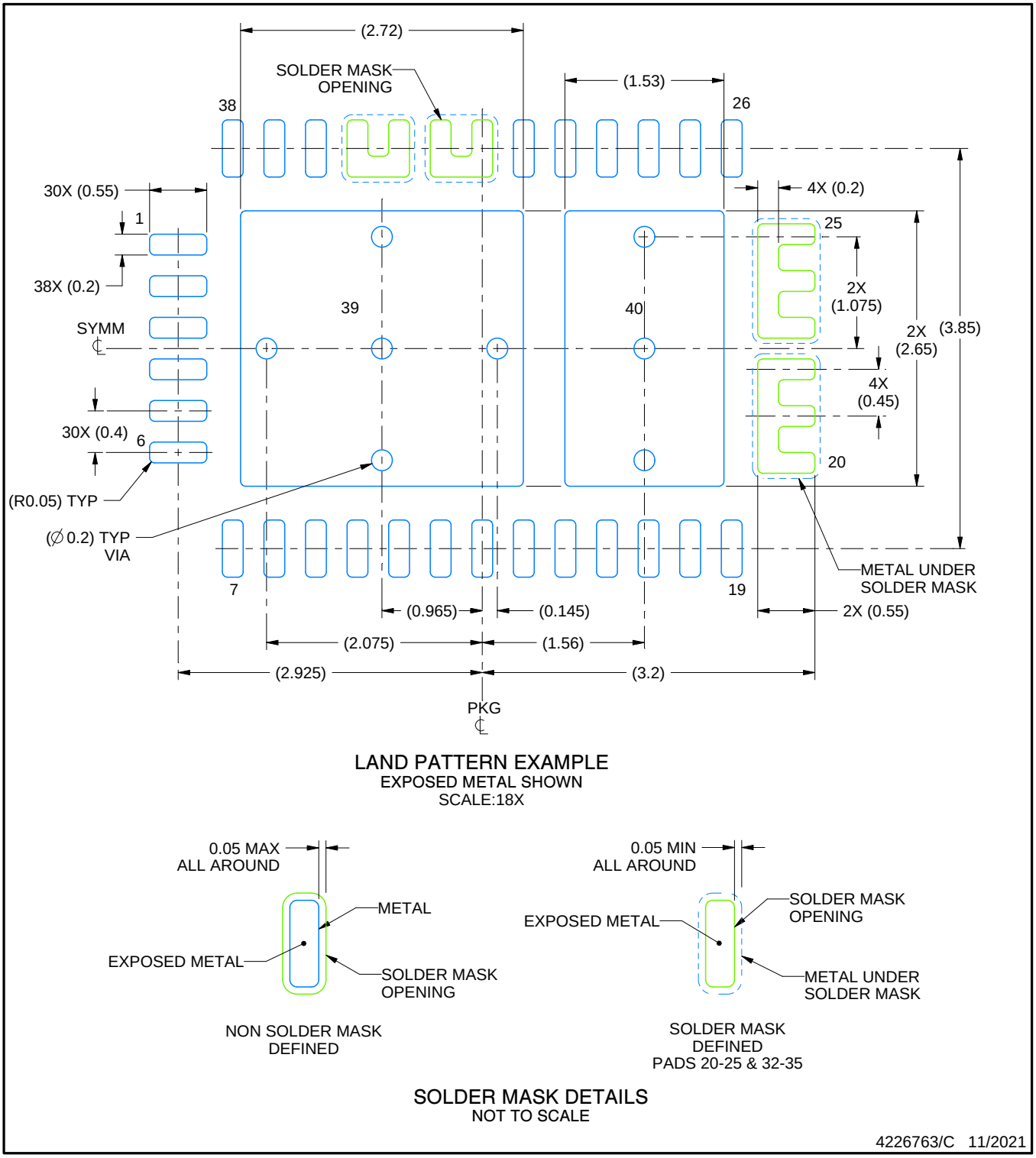
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REF0038A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

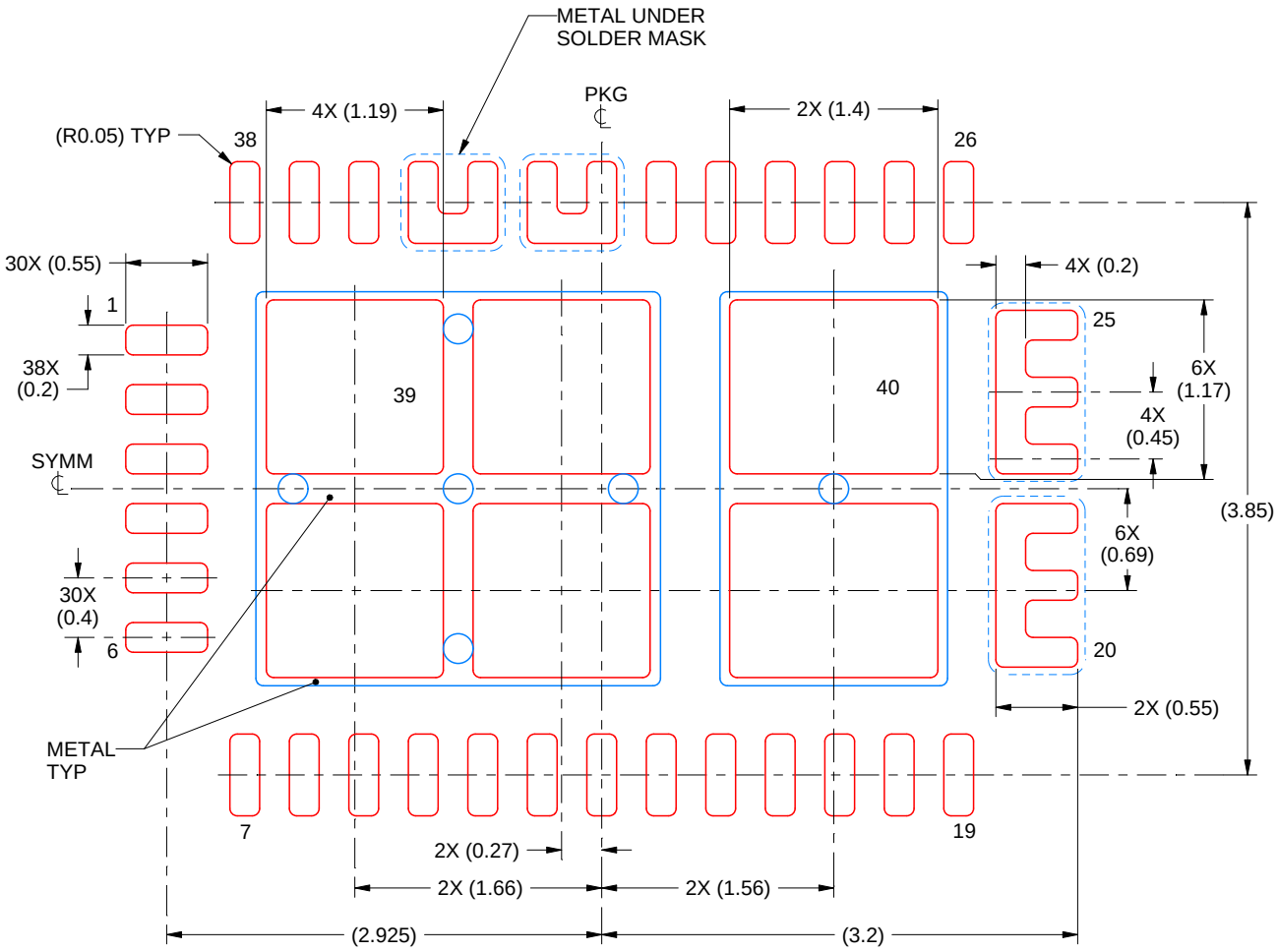
4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REF0038A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 39
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PADS 40
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

SCALE:20X

4226763/C 11/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

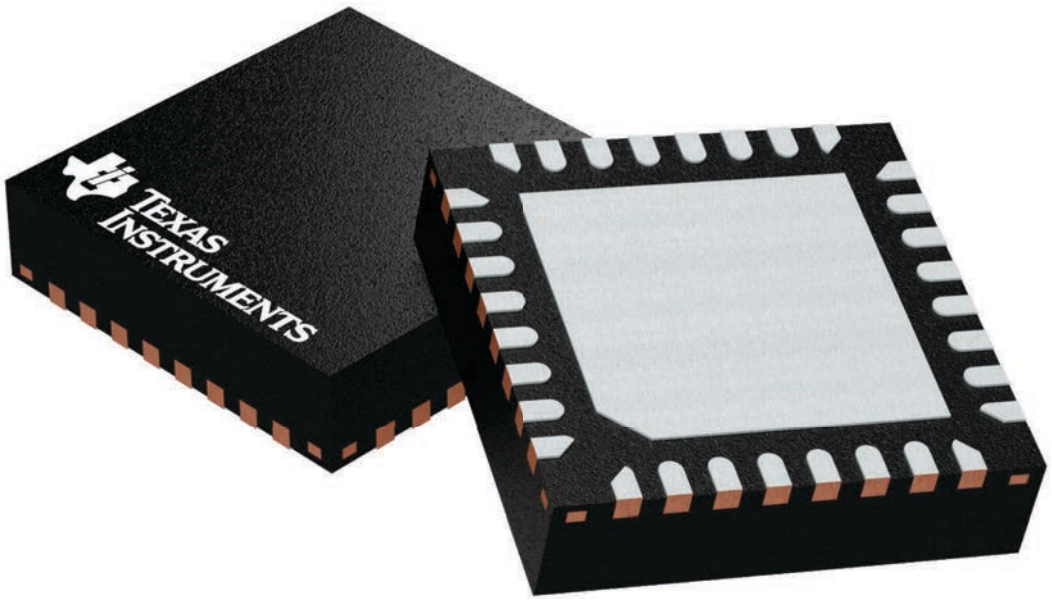
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



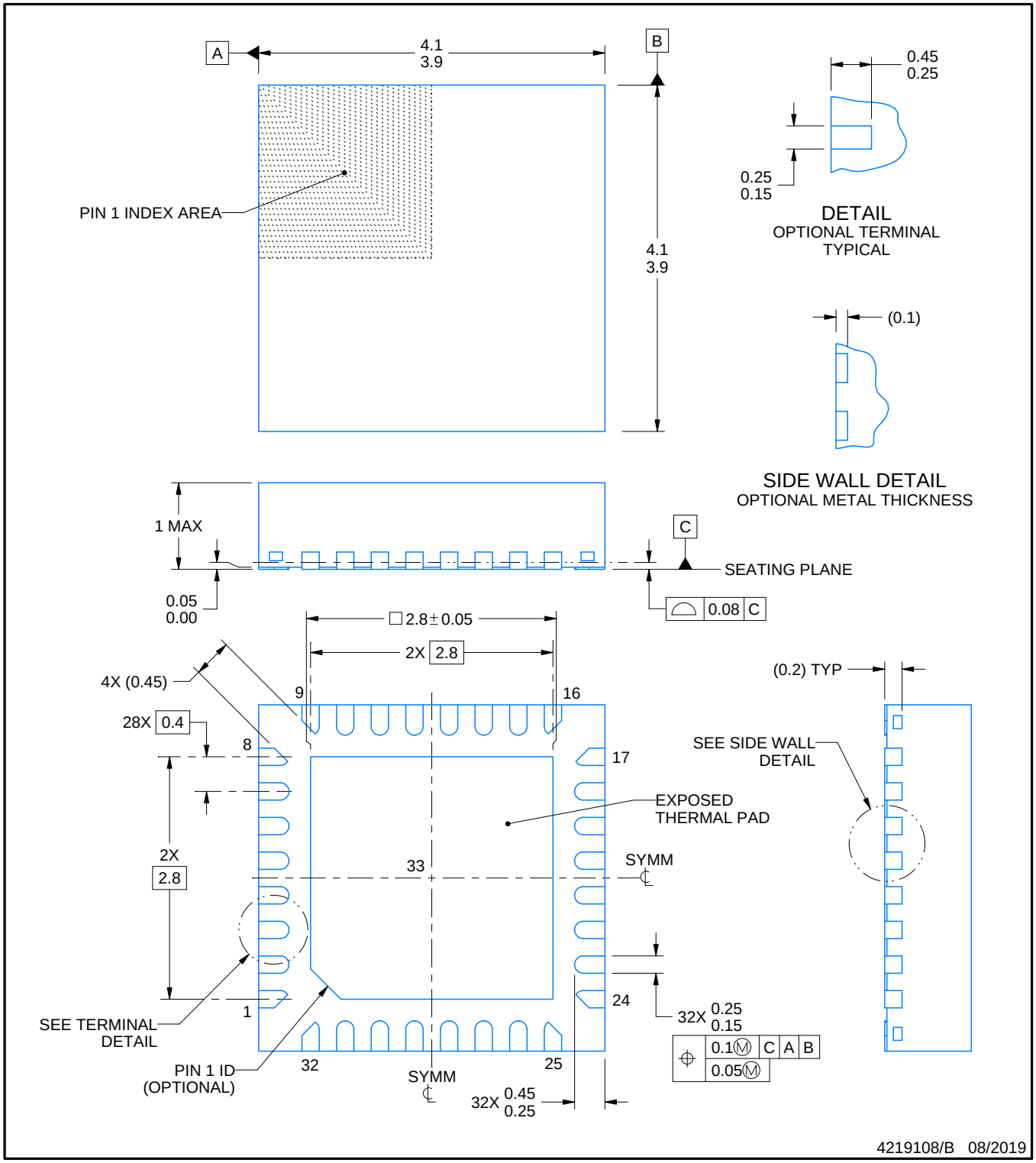
4224982/A

PACKAGE OUTLINE

RSM0032B

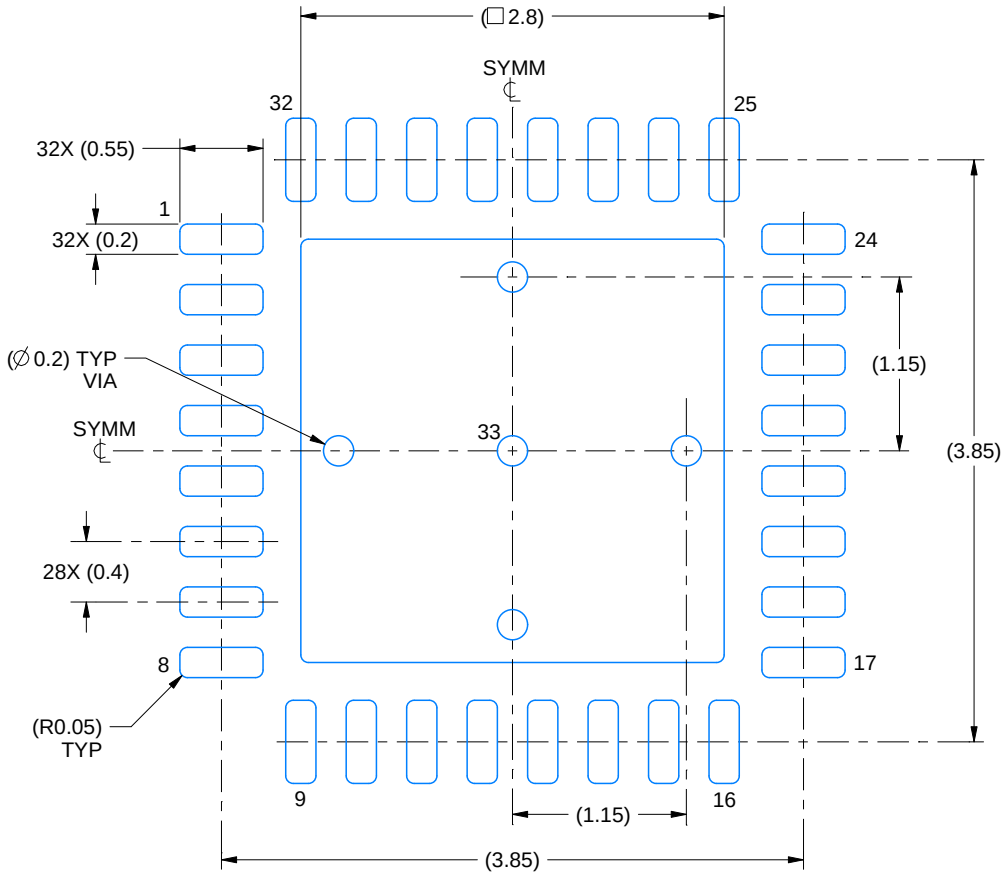
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

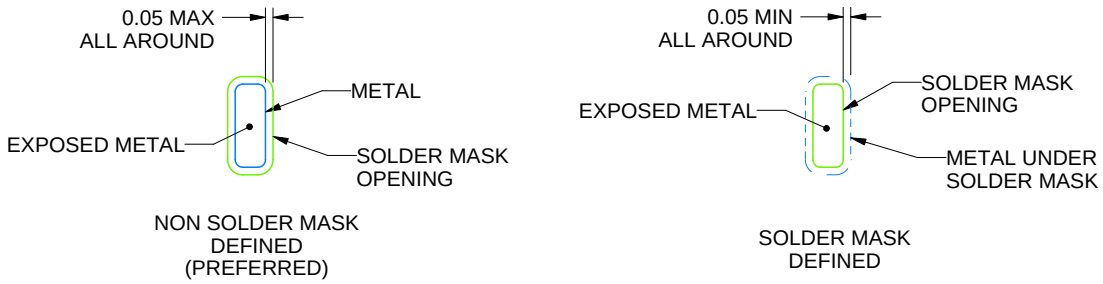


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

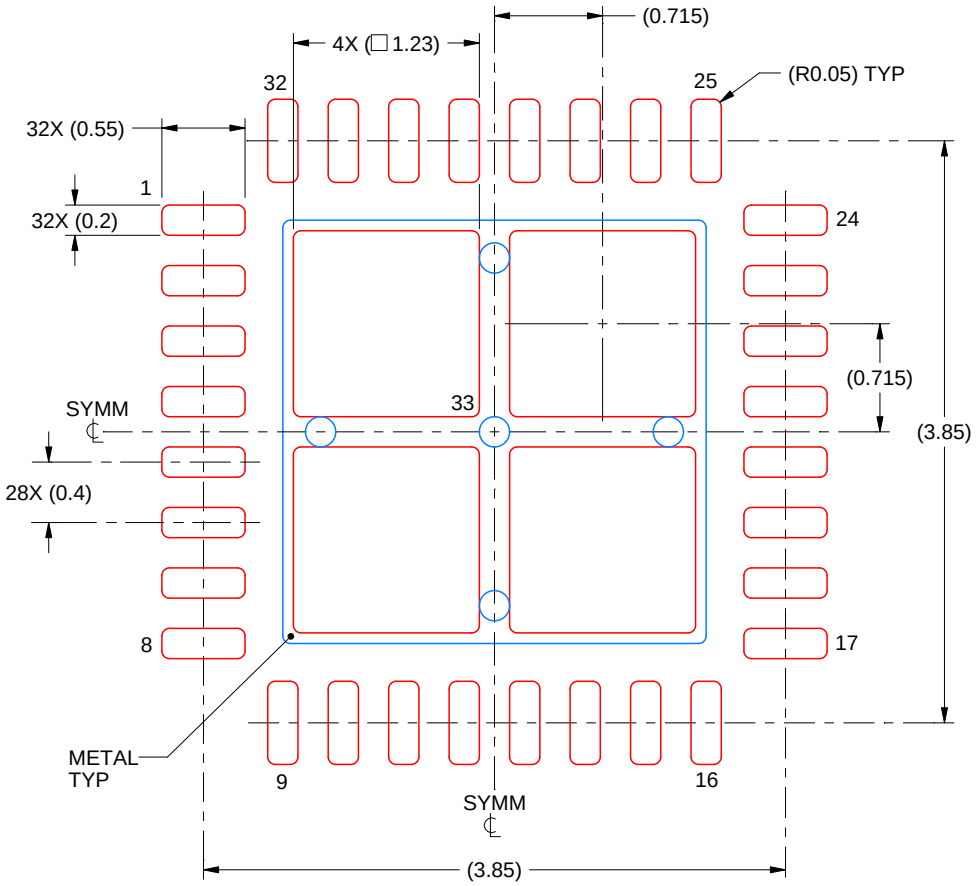


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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