TPS2595xx 2.7V～18V、4A、高速過電圧保護搭載の34mΩ eFuse

1 特長

- 広い入力電圧範囲: 2.7V～18V
  - 絶対最大定格20V
  - TPS2595x5バージョンでは3V～18V
- 低いオン抵抗: R_{ON} = 34mΩ (標準値)
- 高速過電圧保護クランプ(3.8V、5.7V、13.7Vオプション)、応答時間5µs (標準値)
- TPS2595x0、TPS2595x1、TPS2595x5: アクティブHIGHのイネーブル入力、低電圧誤動作防止(UVLO)を設定可能
- TPS2595x3: アクティブLOWのイネーブル入力、過電圧誤動作防止(OVLO)を設定可能
- 可変の電流制限と負荷電流監視出力(ILM)
  - 電流範囲: 0.5A～4A
  - 電流制限精度: ±7.5%
- 可変の出力スルー・レート(dVdt)制御
- 過熱保護(OTP)
- フォルト表示ピン($\overline{FLT}$)
- UL 2367認定済み - ファイル番号E169910
  - R_{ILM} >= 487Ω (最大4.42A)
- IEC 62368-1認定済み
- 単一点障害テストの安全性(IEC 62368-1)
  - ILMピンのオープン/短絡検出

2 アプリケーション

- ホットスワップ、ホットプラグ
- アダプタから給電を受けるシステム
- 多機能プリンタ
- SSDおよびHDD
- 産業用システム
- 白物家電
- セットトップ・ボックス
- デジタルTV

3 概要

TPS2595xxファミリのeFuses (統合FETホットスワップ・デバイス)は、小さなパッケージに組み込まれた、高度に統合された回路保護および電力管理ソリューションです。このデバイスは、非常に少ない数の外付け部品で複数の保護モードを提供し、過負荷、短絡、電圧サージ、および過剰な突入電流に対して堅牢な保護を行います。

出力電流制限レベルは、単一の外付け抵抗により設定できます。また、電流制限抵抗の両端で電圧降下を測定することにより、出力負荷電流を正確に検出可能です。特定の突入電流要件を持つアプリケーションでは、単一の外付けコンデンサにより出力スルー・レートを設定できます。過電圧イベントは内部のクランピング回路により、固定された安全な最大電圧へと迅速に制限されるため、外付け部品が必要ありません。TPS259573バリアントには、ユーザー定義の過電圧カットオフ・スレッショルドを設定するオプションがあります。

TPS2595x5バリアントには、OUTピンをQODピンに接続することで、迅速な出力放電機能を実装できます。

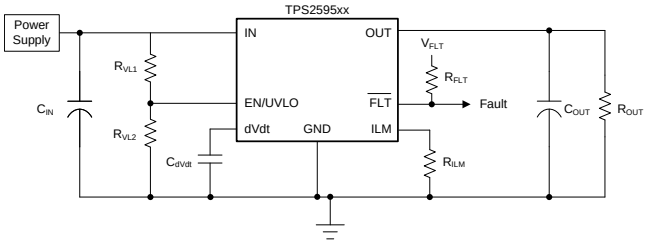
このデバイスは、-40℃～+125℃の温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS2595xxDSG	WSON (8)	2.00mm×2.00mm

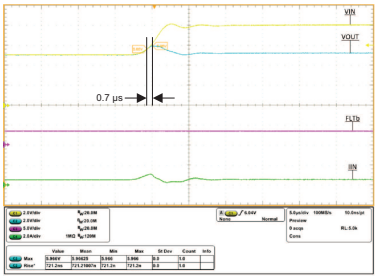
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



Copyright © 2017, Texas Instruments Incorporated

TPS25953x過電圧クランプの応答時間



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 4
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 6
7.5 Electrical Characteristics ... 7
7.6 Switching Characteristics ... 8
7.7 Typical Characteristics ... 10
8 Detailed Description ... 18
8.1 Overview ... 18
8.2 Functional Block Diagram ... 18
8.3 Feature Description ... 18
8.4 Device Functional Modes ... 25
9 Application and Implementation ... 27
9.1 Application Information ... 27
9.2 Typical Application ... 27
10 Power Supply Recommendations ... 33
10.1 Transient Protection ... 33
10.2 Output Short-Circuit Measurements ... 34
11 Layout ... 34
11.1 Layout Guidelines ... 34
11.2 Layout Example ... 35
12 デバイスおよびドキュメントのサポート ... 36
12.1 ドキュメントのサポート ... 36
12.2 ドキュメントの更新通知を受け取る方法 ... 36
12.3 コミュニティ・リソース ... 36
12.4 商標 ... 36
12.5 静電気放電に関する注意事項 ... 36
12.6 Glossary ... 37
13 メカニカル、パッケージ、および注文情報 ... 37

4 改訂履歴

Revision B (March 2018) から Revision C に変更 **Page**

- 「特長」セクションの単一点障害テストの安全性に(IEC 62368-1)を 追加 ... 1
- Changed UL 60950 to IEC 62368-1 in the Specifications *Electrical Characteristics* table ... 5

Revision A (December 2017) から Revision B に変更 **Page**

- 変更 multiplication symbol to an equal symbol before 229.2 mW in 式 15 ... 29

2017年6月発行のものから更新 **Page**

- ステータスを「事前情報」から「量産データ」に変更 ... 1

Copyright © 2017–2018, Texas Instruments Incorporated

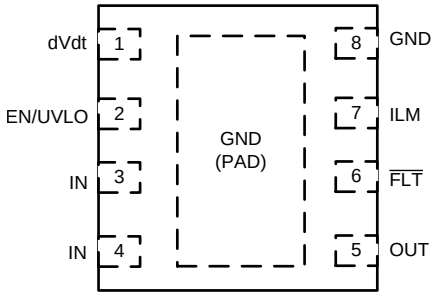
5 Device Comparison Table

DEVICE NUMBER	OUTPUT VOLTAGE CLAMP	RESPONSE TO THERMAL SHUTDOWN (TSD)	ENABLE	QUICK OUTPUT DISCHARGE
TPS259520DSG	3.8 V (typ)	Latch-off	Active high	No
TPS259521DSG	3.8 V (typ)	Auto-retry	Active high	No
TPS259530DSG	5.7 V (typ)	Latch-off	Active high	No
TPS259531DSG	5.7 V (typ)	Auto-retry	Active high	No
TPS259533DSG	5.7 V (typ)	Auto-retry	***Active low***	No
TPS259540DSG	13.7 V (typ)	Latch-off	Active high	No
TPS259541DSG	13.7 V (typ)	Auto-retry	Active high	No
TPS259570DSG	No OV clamp	Latch-off	Active high	No
TPS259571DSG	No OV clamp	Auto-retry	Active high	No
TPS259573DSG	Programmable Overvoltage Lockout	Auto-retry	***Active low***	No
TPS259525DSG	3.8 V (typ)	Auto-retry	Active high	***Yes***
TPS259535DSG	5.7 V (typ)	Auto-retry	Active high	***Yes***

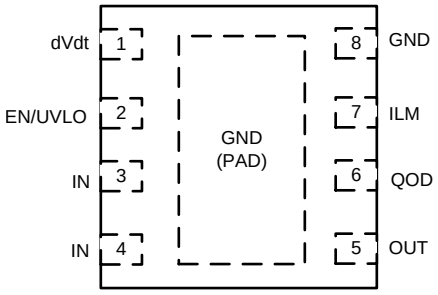
Copyright © 2017–2018, Texas Instruments Incorporated

6 Pin Configuration and Functions

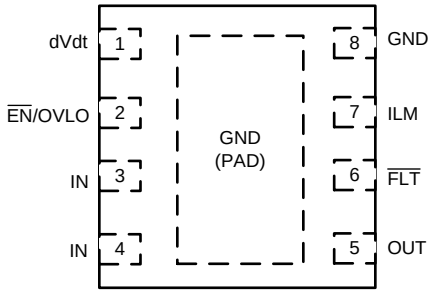
TPS2595x0/1 DSG Package
8-Pin WSON
Top View



TPS2595x5 DSG Package
8-Pin WSON
Top View



TPS2595x3 DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	dVdt	Analog I/O	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. (See *Switching Characteristics*).
2	EN/UVLO	Analog input	Active high enable for the **TPS2595x0, TPS2595x1, TPS2595x5** variants. A resistor divider can be used to adjust the undervoltage lockout threshold. Do not leave floating.
	$\overline{\text{EN}}$/OVLO		Active low enable for the **TPS2595x3** variants. A resistor divider can be used to adjust the overvoltage lockout threshold. Do not leave floating.
3,4	IN	Power	Power input
5	OUT	Power	Power output
6	$\overline{\text{FLT}}$	Digital output	**TPS2595x0, TPS2595x1, TPS2595x3**: Fault event indicator which is pulled low when a fault is detected. It is an open drain output that requires an external pull up resistance.
	QOD		**TPS2595x5**: Quick Output Discharge Pin, when tied to OUT directly or through external resistor.
7	ILM	Analog I/O	This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit. The pin voltage can also be used to monitor the output load current. Do not leave floating.
8	GND	Ground	Ground
PAD	GND	Thermal/Ground	The exposed pad is used primarily for heat dissipation and must be connected to GND.

Copyright © 2017–2018, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{IN}	Maximum input voltage	IN	–0.3	20	V
V_{OUT}	Maximum output voltage	OUT	–0.3	V_{IN} + 0.3	V
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–1.2		V
V_{EN}	Maximum enable pin voltage	EN/UVLO or $\overline{EN}$/OVLO	–0.3	7	V
V_{FLTB}	Maximum fault pin voltage (TPS2595x0/1/3)	$\overline{FLT}$	–0.3	7	V
V_{QOD}	Maximum QOD pin voltage (TPS2595x5)	QOD	–0.3	7	V
V_{dVdt}	Maximum dVdt pin voltage	dVdt		2.5	V
I_{FLTB}	Maximum fault pin sink current	$\overline{FLT}$		10	mA
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		
$T_{J,MAX}$	Maximum junction temperature		Internally limited		
T_{LEAD}	Maximum lead temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range (TPS2595x0/1/3)	IN	2.7	18 (1)	V
V_{IN}	Input voltage range (TPS2595x5)	IN	3.0	18(1)	V
V_{OUT}	Output voltage	OUT	0	V_{IN} + 0.3	V
V_{EN}	Enable pin voltage	EN/UVLO or $\overline{EN}$/OVLO	0	6(2)	V
V_{FLTB}	Fault pin voltage (TPS2595x0/1/3)	$\overline{FLT}$	0	6	V
V_{QOD}	Fault pin voltage (TPS2595x5)	QOD	0	6	V
I_{MAX}	Continuous output current (T_J = –40 to 125°C)	IN to OUT		4	A
	Continuous output current (T_J = –40 to 105°C)	IN to OUT		5(3)	A
R_{ILM}	ILM pin resistance (Active Current Limiting Operation)	ILM	487	5000	Ω
C_{dVdt}	dVdt capacitor value	dVdt	3300		pF
V_{dVdt}	dVdt pin capacitor voltage rating	dVdt	4		V
T_J	Operating junction temperature		–40	125	°C

(1) The nominal input voltage should be limited to the output clamp voltage for the selected device option as listed in the Electrical Characteristics section
(2) For supply voltages below 6V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 6V, it is recommended to use an appropriate resistor divider between IN, EN and GND to ensure the voltage at the EN pin is within the specified limits.
(3) Guaranteed by design. Not tested at production.

Copyright © 2017–2018, Texas Instruments Incorporated

7.4 Thermal Information

THERMAL METRIC (1)		TPS2595x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2017–2018, Texas Instruments Incorporated

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V for TPS25954x/7x, V_{IN} = 5 V for TPS25953x, V_{IN} = 3.3 V for TPS25952x, V_{EN} = 5 V (= 0 V for TPS2595x3 only) , R_{ILM} = 487 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT SUPPLY (IN)								
I_Q	IN quiescent current	TPS2595x0/1/5	$V_{EN} \geq V_{UVLO}$			175	250	µA
		TPS2595x3	$V_{EN} \leq V_{OVLO}$					
I_{SD}	IN shutdown current	TPS2595x0/1/5	V_{EN} < 0.5V	$V_{IN} \leq 5$ V		0.04		µA
				5 V < VIN ≤ 18 V		0.45	2	µA
		TPS2595x3	V_{EN} > 2 V			45	65	µA
V_{UVP}	IN Undervoltage Protection Threshold	TPS2595x5	V_{IN} Rising		2.7	2.8	2.9	V
		TPS2595x5	V_{IN} Falling		2.58	2.68	2.78	V
		TPS2595x0/1/3	V_{IN} Rising		2.44	2.54	2.64	V
		TPS2595x0/1/3	V_{IN} Falling		2.33	2.43	2.53	V
OUTPUT VOLTAGE CLAMP (OUT)								
V_{OVC}	Overvoltage clamp threshold(1)	TPS25952x	V_{IN} Rising, R_{OUT} = 10 kΩ		3.65	3.87	4.1	V
		TPS25953x			5.5	5.7	5.9	V
		TPS25954x			13.3	13.7	14.3	V
V_{CLAMP}	Output voltage while clamping(1)	TPS25952x	$V_{IN} \geq V_{OVC}$, I_{OUT} = 10 mA		3.4	3.6	3.8	V
		TPS25953x			5.2	5.45	5.7	V
		TPS25954x			13	13.55	14.1	V
t_{OVC}	Output clamp response time(1)	TPS25952x/3x/4x	I_{OUT} = 4 A			5		µs
			I_{OUT} = 100 mA			10		µs
OUTPUT CURRENT LIMIT AND MONITOR (ILM)								
G_{IMON}	Current monitor gain as measured on ILM pin (I_{ILM} / I_{OUT})	I_{OUT} = 4 A			254	276	299	µA/A
		I_{OUT} = 1 A			249	276	304	µA/A
I_{LIMIT}	I_{OUT} Current limit(2)	R_{ILM} = 487 Ω			3.87	4.17	4.42	A
		R_{ILM} = 1780 Ω			1.09	1.17	1.24	A
		R_{ILM} = 4420 Ω(3)			0.46	0.49	0.52	A
		R_{ILM} = Open (Single Point Failure Test IEC 62368-1)				0		A
I_{CB}	I_{OUT} Circuit Breaker Threshold during R_{ILM} Short condition	R_{ILM} = Short to GND (Single Point Failure Test IEC 62368-1)				3		A
t_{LIM}	Current limit response time(2)	I_{OUT} > I_{LIMIT} + 20% to I_{OUT} ≤ I_{LIMIT}				250		µs
t_{SC}	Short circuit response time(4)	I_{OUT} > I_{SC} to I_{OUT} ≤ I_{LIMIT}				5		µs
ON-RESISTANCE (IN - OUT)								
R_{ON}	ON state resistance	V_{IN} = 4 V to 18 V	T_J = 25°C			34	37	mΩ
			T_J = –40°C to 85°C				47	mΩ
			T_J = –40°C to 125°C				53	mΩ
		V_{IN} = 2.7 V to 4 V	T_J = 25°C			36	40	mΩ
			T_J = –40°C to 85°C				51	mΩ
			T_J = –40°C to 125°C				58	mΩ

(1) Refer to Fig 49
(2) Refer to Fig 50
(3) Guaranteed by design and characterization. Not tested at production.
(4) Refer to Fig 52

Copyright © 2017–2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V for TPS25954x/7x, V_{IN} = 5 V for TPS25953x, V_{IN} = 3.3 V for TPS25952x, V_{EN} = 5 V (= 0 V for TPS2595x3 only) , R_{ILM} = 487 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO) - TPS2595x0/1/5							
I_{EN}	EN/UVLO pin leakage current			–0.1		0.1	µA
$V_{UVLO(R)}$	Undervoltage lockout threshold	V_{EN} rising		1.13	1.2	1.27	V
$V_{UVLO(F)}$		V_{EN} falling		1.03	1.1	1.17	V
$\overline{\text{ENABLE}}$ / OVERVOLTAGE LOCKOUT ($\overline{\text{EN}}$/OVLO) - TPS2595x3							
I_{EN}	$\overline{\text{EN}}$/OVLO pin leakage current			–0.1		0.1	µA
$V_{OVLO(R)}$	Overvoltage lockout threshold	V_{EN} rising		1.13	1.2	1.27	V
$V_{OVLO(F)}$		V_{EN} falling		1.03	1.1	1.17	V
t_{OVLO}	Overvoltage lockout response time	V_{EN} > V_{OVLO} to $\overline{\text{FLT}}$ ↓			3		µs
FAULT INDICATION ($\overline{\text{FLT}}$) - TPS2595x0/1/3							
R_{FLTB}	$\overline{\text{FLT}}$ pin resistance	$\overline{\text{FLT}}$ ↓			12		Ω
I_{FLTB}	$\overline{\text{FLT}}$ pin leakage current	V_{EN} = 2 V, V_{FLTB} = 0 V to 6 V		–0.1		0.1	µA
QUICK OUTPUT DISCHARGE (QOD) - TPS2595x5							
R_{QOD}	QOD effective resistance	IN connected to EN, OUT connected to QOD, EN↓ to 1V			19		Ω
OVERTEMPERATURE PROTECTION (TSD)							
TSD	Thermal shutdown		T_J Rising		157		°C
TSD_{HYS}	Thermal shutdown hysteresis		T_J Falling		5		°C
$t_{TSD,RST}$	Thermal Shutdown Auto-Retry Interval	TPS2595x1/3/5	Device Enabled and T_J < TSD - TSD_{HYS}		93		ms

7.6 Switching Characteristics

Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_{OUT} = 100 Ω, C_{OUT} = 1 µF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 3300pF	UNIT
SR_{ON}	Output Rising slew rate	3.3 V	16.3	10.0	V/ms
		5 V	21.9	11.6	
		12 V	38.2	12.4	
$t_{D,ON}$	Turn on delay	3.3 V	147	254	µs
		5 V	149	289	
		12 V	153	335	
t_R	Rise time	3.3 V	157	259	µs
		5 V	179	349	
		12 V	248	763	
$t_{D,OFF}$	Turn off delay	3.3 V	11.6	11.6	µs
		5 V	11.3	11.5	
		12 V	11.0	11.4	

Copyright © 2017–2018, Texas Instruments Incorporated

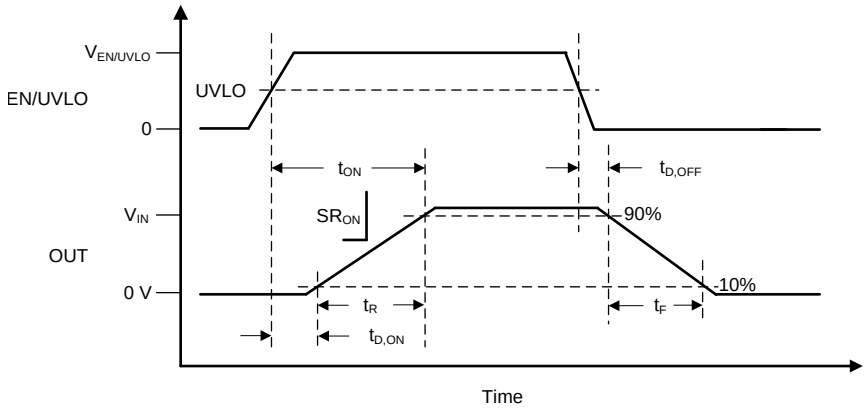


図 1. TPS2595x0, TPS2595x1, TPS2595x5 Switching Times

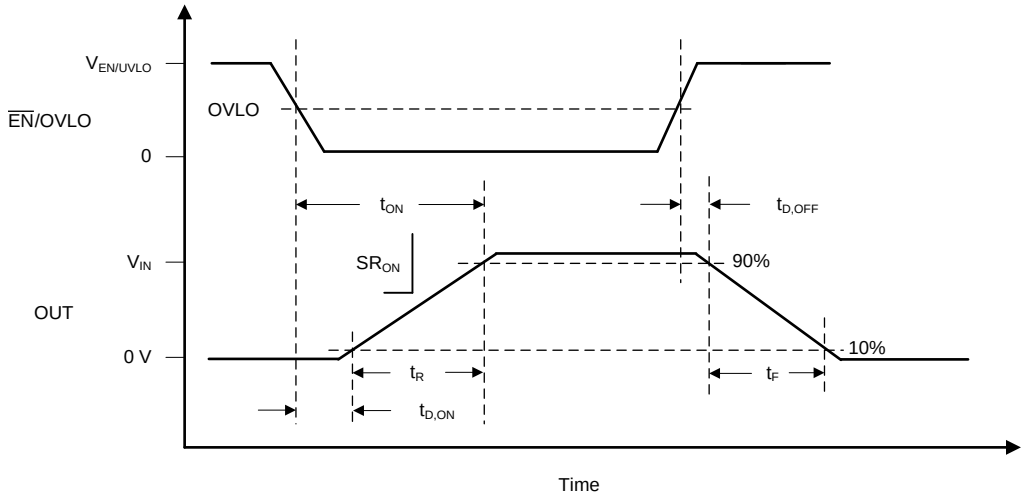
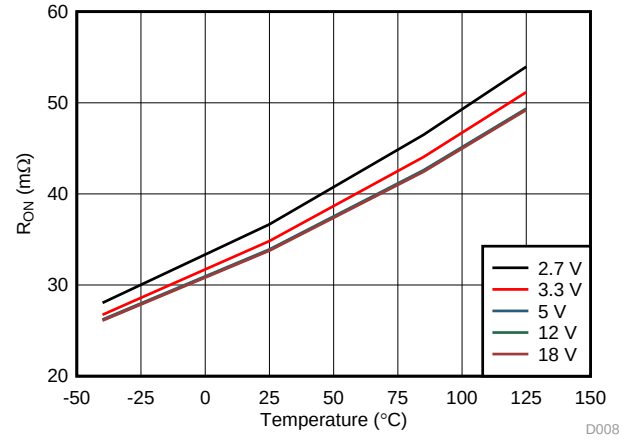


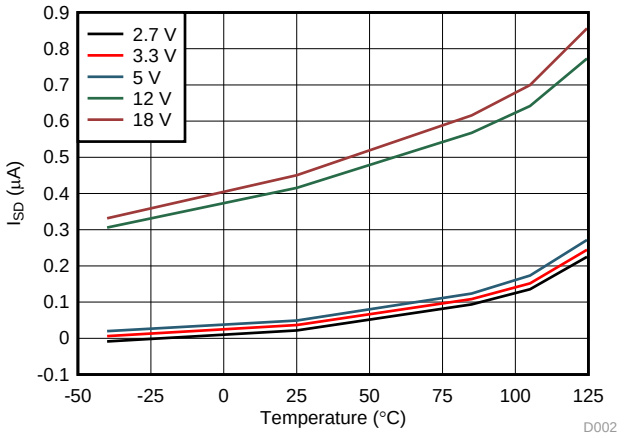
図 2. TPS2595x3 Switching Times

7.7 Typical Characteristics



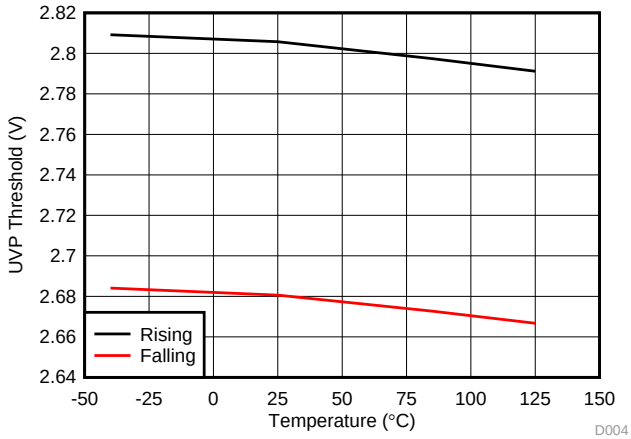
I_{OUT} = 0.5A , Different Input Voltages

図 3. On-resistance vs Temperature



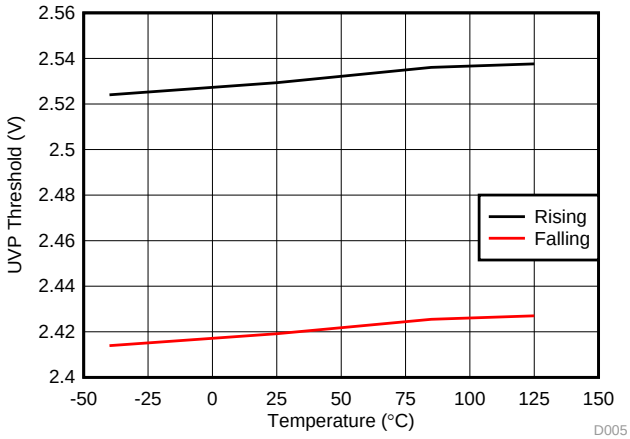
TPS2595x0/1/5, EN=GND, OUT=Open, Different Input Voltages

図 4. Shutdown Current vs Temperature



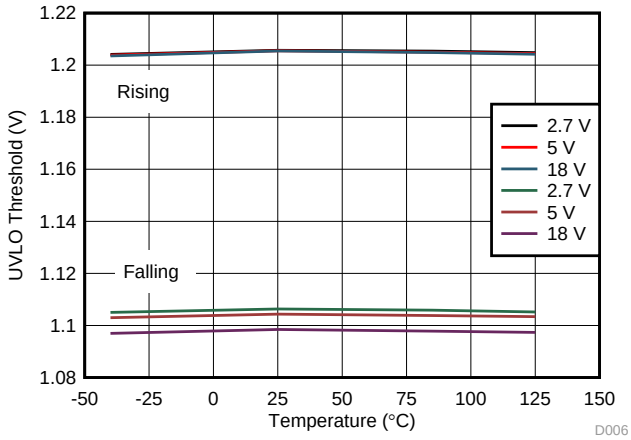
TPS2595x5

図 5. UVP Threshold vs Temperature



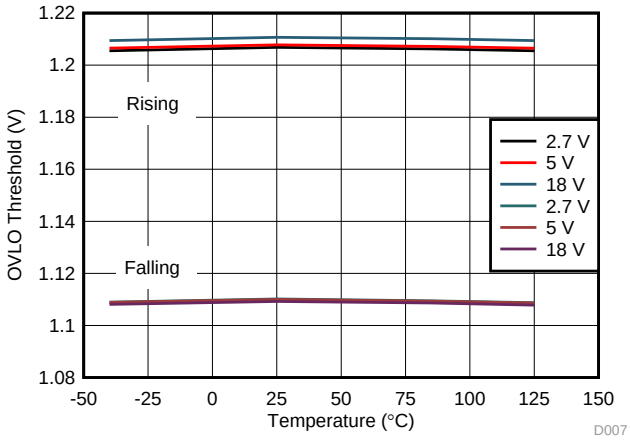
TPS2595x0/1/3

図 6. UVP Threshold vs Temperature



TPS2595x0/1/5, Different Input Voltages

図 7. UVLO Threshold vs Temperature



TPS259573, Different Input Voltages

図 8. OVLO Threshold vs Temperature

Copyright © 2017–2018, Texas Instruments Incorporated

Typical Characteristics (continued)

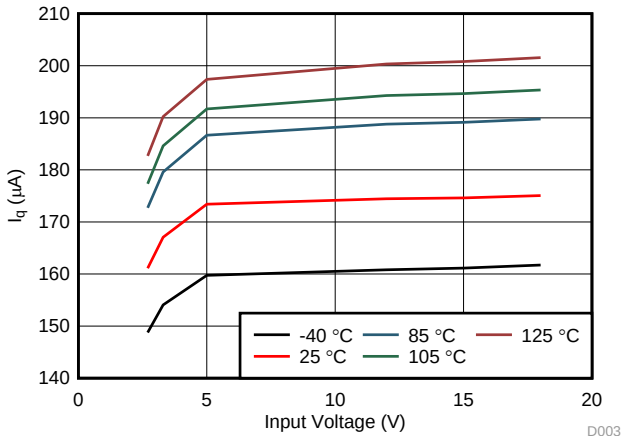
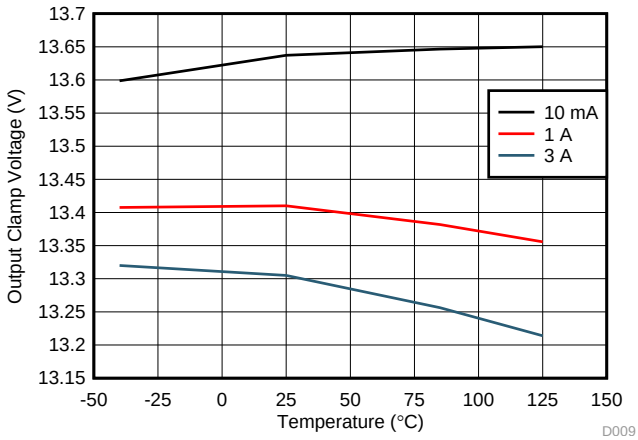
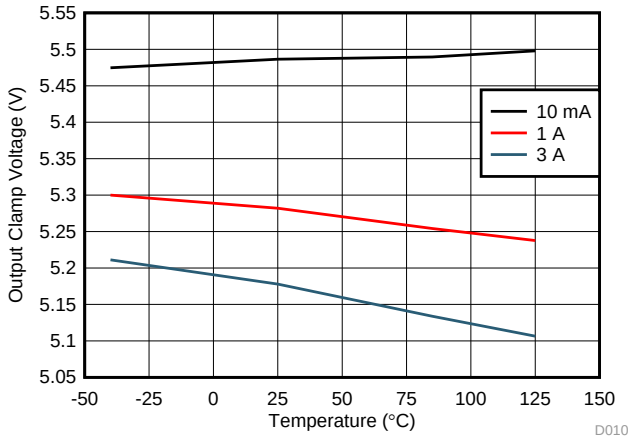


図 9. Quiescent Current vs Input Voltage



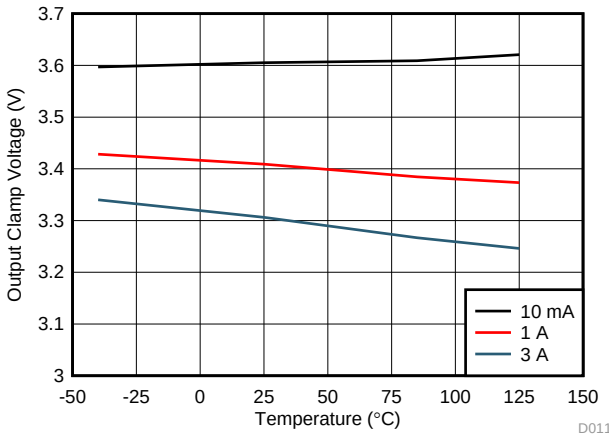
TPS25954x, Different Output Load Currents

図 10. OVC Threshold vs Temperature



TPS25953x, Different Output Load Currents

図 11. OVC Threshold vs Temperature



TPS25952x, Different Output Load Currents

図 12. OVC Threshold vs Temperature

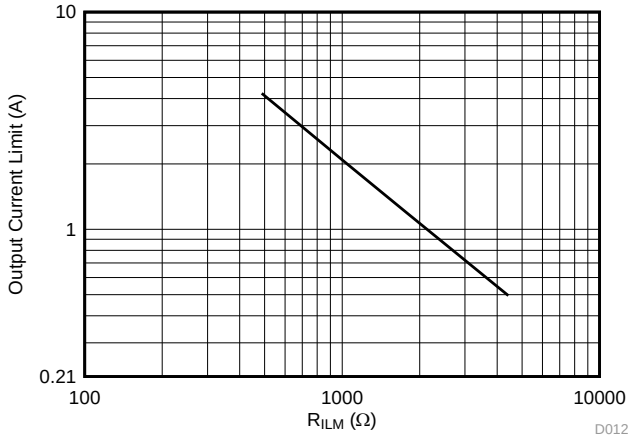
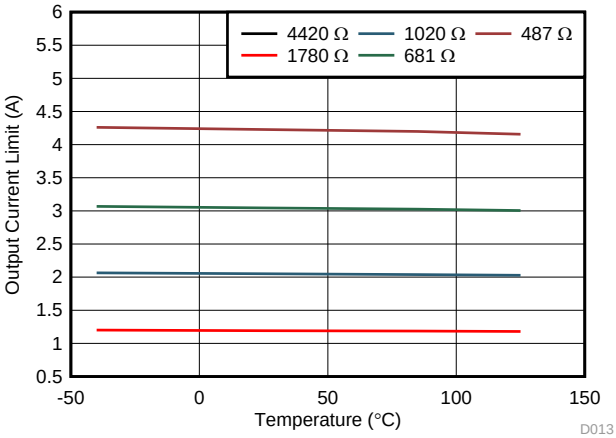


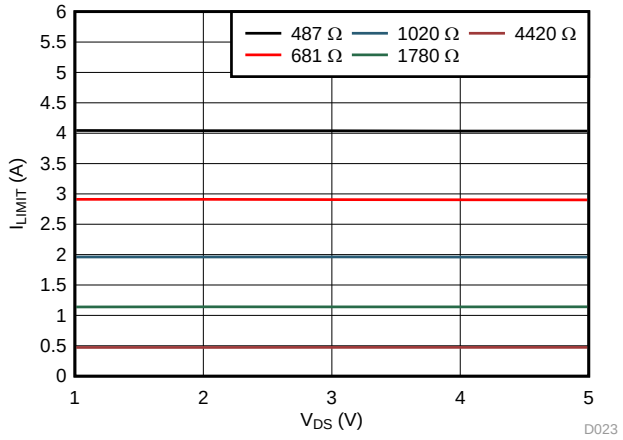
図 13. Output Current Limit (I_{LIMIT}) vs R_{ILM}



V_{IN} = 12V, Different R_{ILM} values

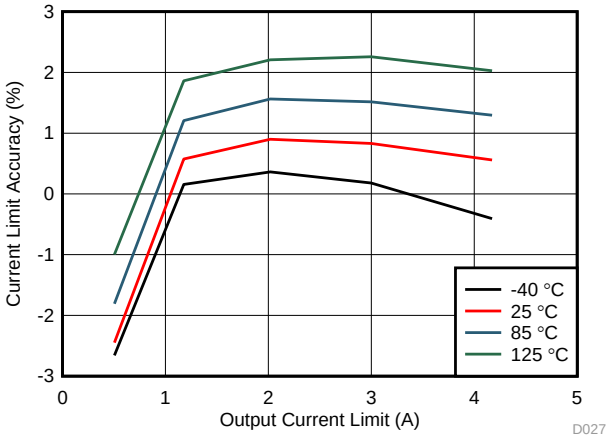
図 14. Output Current Limit (I_{LIMIT}) vs Temperature

Typical Characteristics (continued)



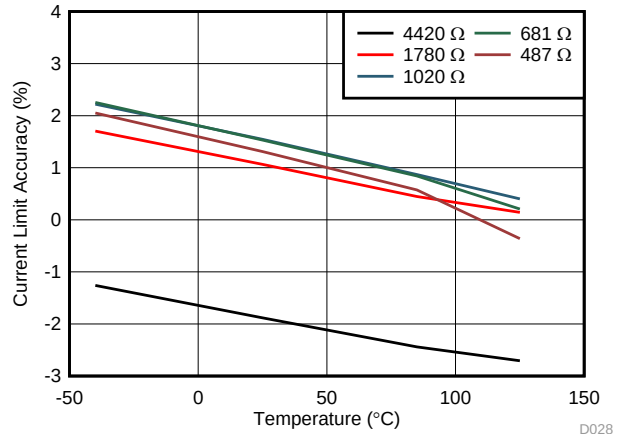
Different R_{ILM} values

図 15. Output Current Limit vs V_{DS}



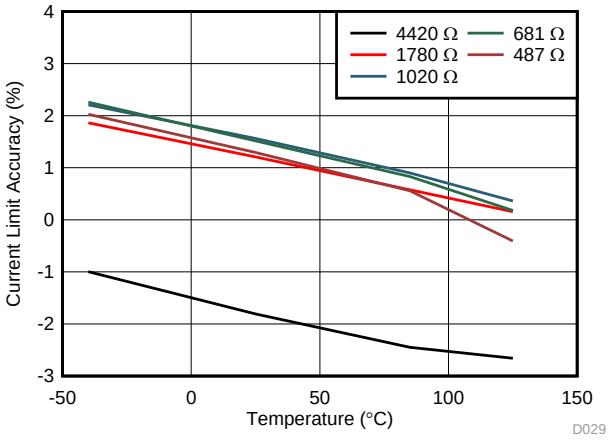
V_{IN} = 5 V

図 16. Output Current Limit Accuracy vs Output Current Limit



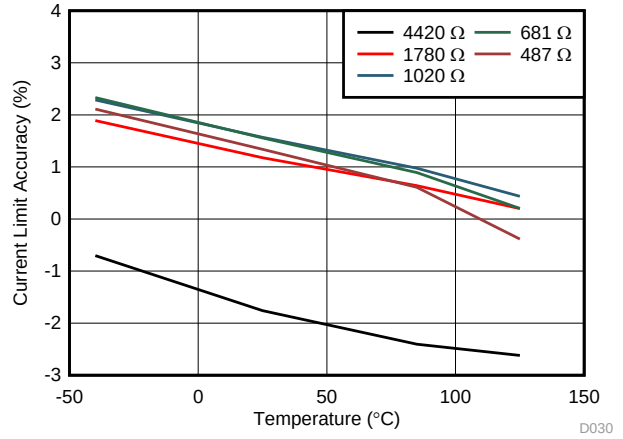
V_{IN} = 3.3 V, Different R_{ILM} values

図 17. Output Current Limit Accuracy vs Temperature



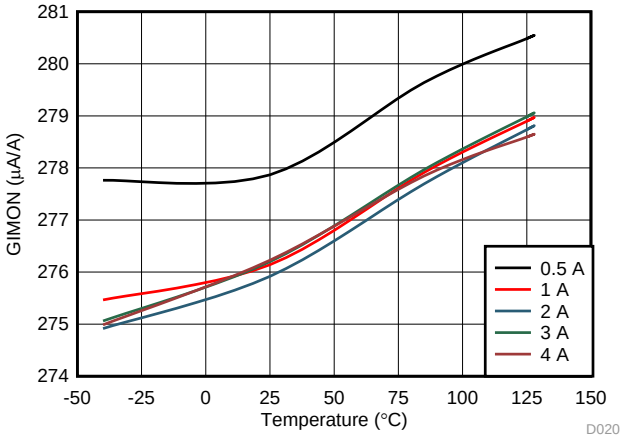
V_{IN} = 5 V, Different R_{ILM} values

図 18. Output Current Limit Accuracy vs Temperature



V_{IN} = 12 V, Different R_{ILM} values

図 19. Output Current Limit Accuracy vs Temperature

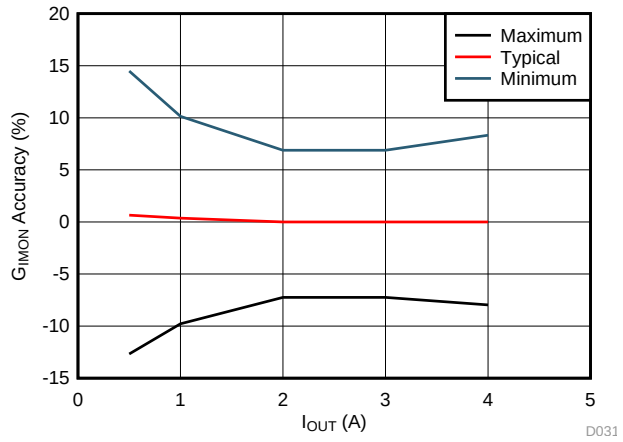


Different Output Load Currents

図 20. Load Current Monitor Gain vs Temperature

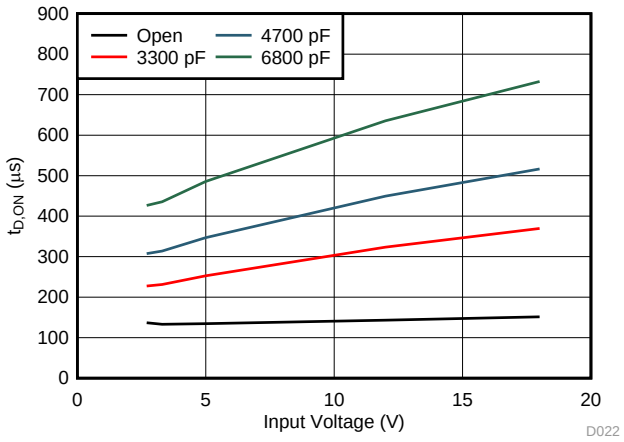
Copyright © 2017–2018, Texas Instruments Incorporated

Typical Characteristics (continued)



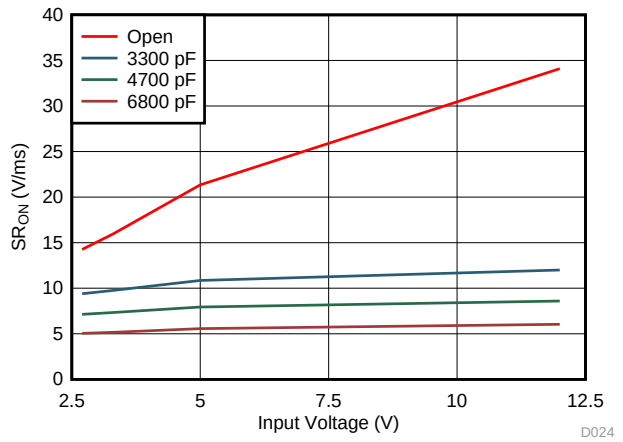
Normalized to reference value of G_{IMON} = 276uA/A

図 21. Load Current Monitor Gain Accuracy vs Load Current



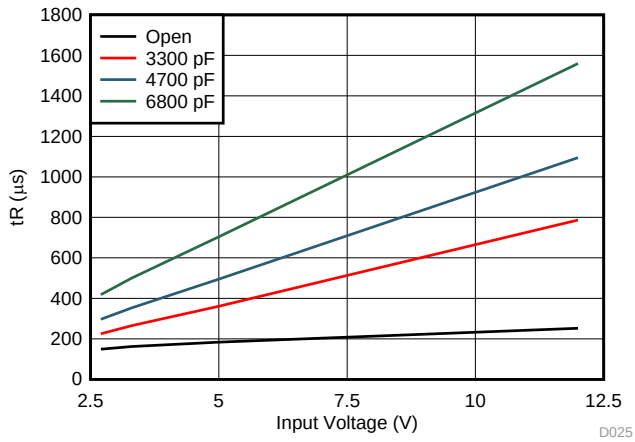
Different C_{dVdt} values

図 22. Turn on Delay vs Input Voltage



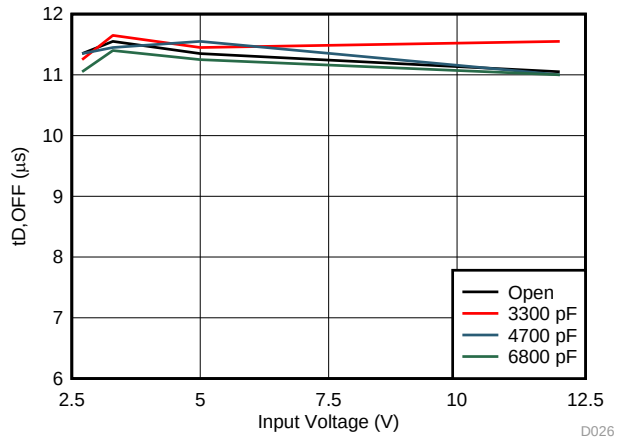
Different C_{dVdt} values

図 23. ON Slew Rate vs Input Voltage



Different C_{dVdt} values

図 24. Rise Time vs Input Voltage



Different C_{dVdt} values

図 25. Turn OFF Delay vs Input Voltage

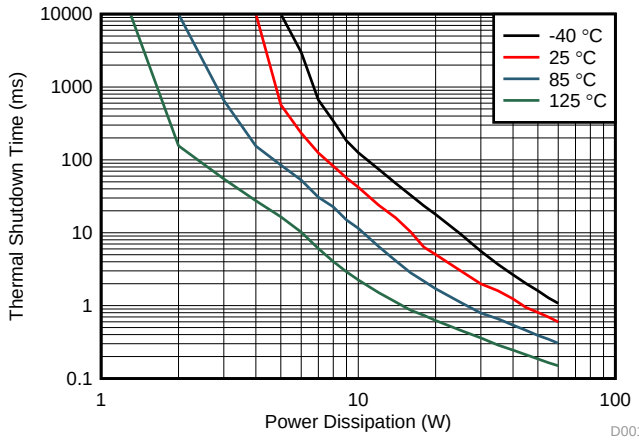
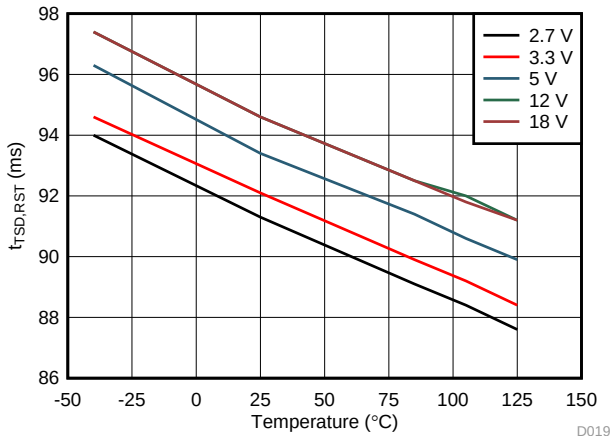


図 26. Thermal Shutdown Time vs Power Dissipation

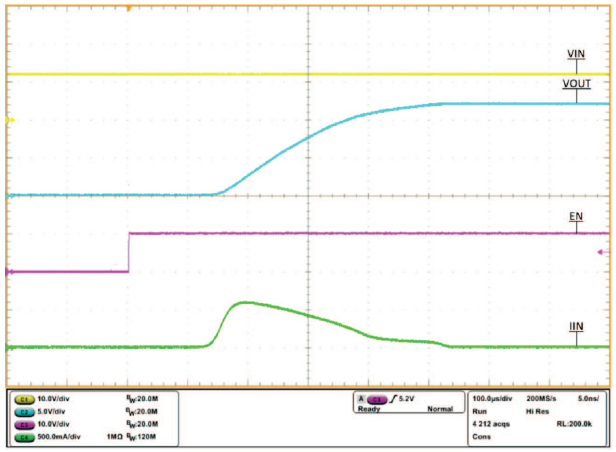
Copyright © 2017–2018, Texas Instruments Incorporated

Typical Characteristics (continued)



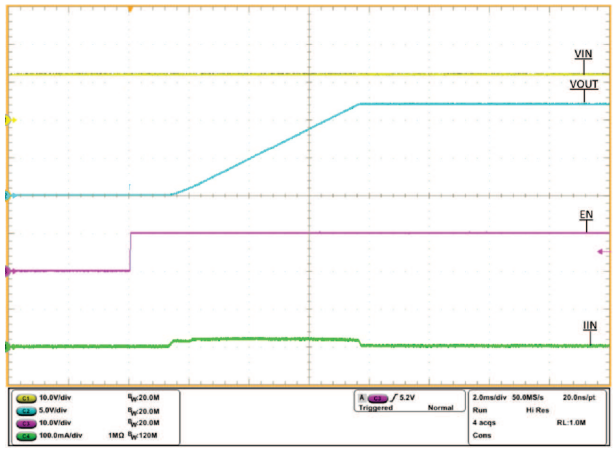
TPS2595x1/3/5, Different Input Voltages

図 27. Thermal Shutdown Auto-Retry Interval vs Temperature



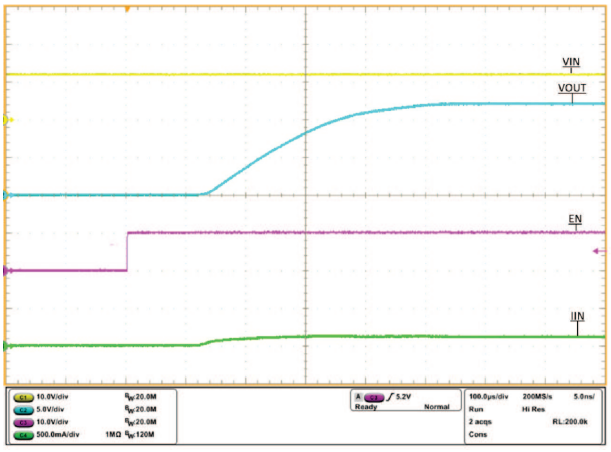
V_{IN} = 12 V, C_{OUT} = 10 µF, R_{ILM} = 487 Ω, V_{EN} = 5 V

図 28. Output Voltage Ramp and Inrush Current at Start Up, C_{dVdT} = Open



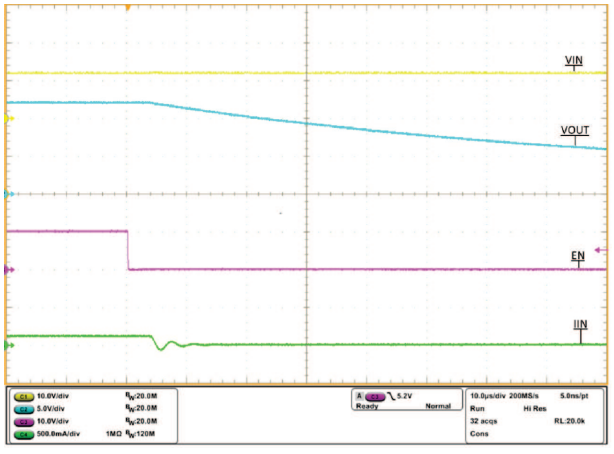
V_{IN} = 12 V, C_{OUT} = 10 µF, R_{ILM} = 487 Ω, V_{EN} = 5 V

図 29. Output Voltage Ramp and Inrush Current at Start Up, C_{dVdT} = 22 nF



V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} = 100 Ω

図 30. Turn ON Delay

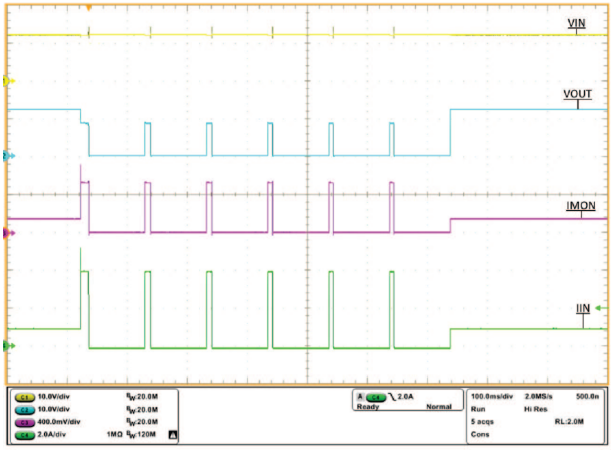


V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} = 100 Ω

図 31. Turn OFF Delay

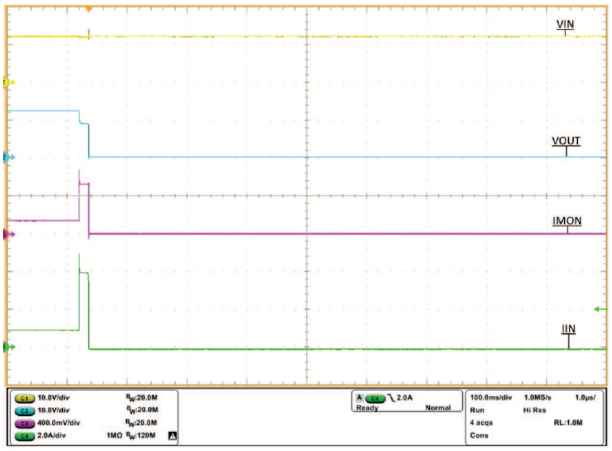
Copyright © 2017–2018, Texas Instruments Incorporated

Typical Characteristics (continued)



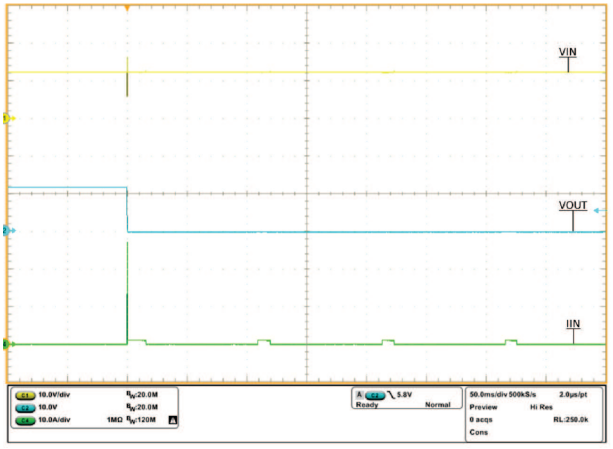
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} varied from 12 Ω to 2 Ω to 12 Ω

図 32. TPS2595x1, TPS2595x3, TPS2595x5 OverCurrent Response



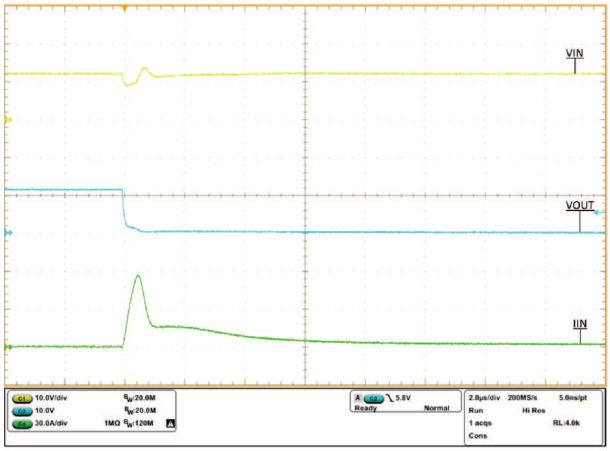
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} varied from 12 Ω to 2 Ω to 12 Ω

図 33. TPS2595x0 Overcurrent Response



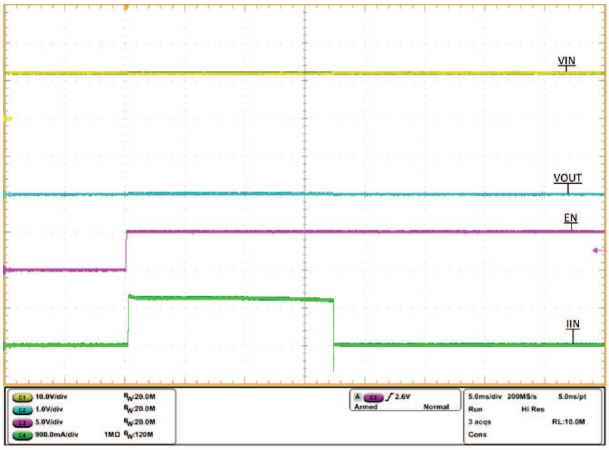
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

図 34. Output Hot Short to GND Response



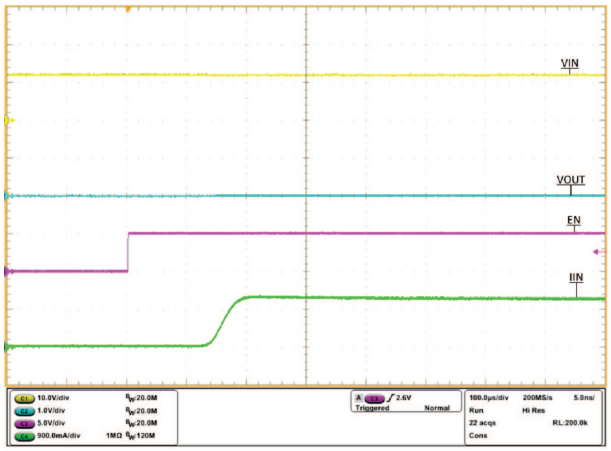
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

図 35. Output Hot Short to GND Response (Zoomed In)



V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

図 36. Wake Up With Output Short to GND

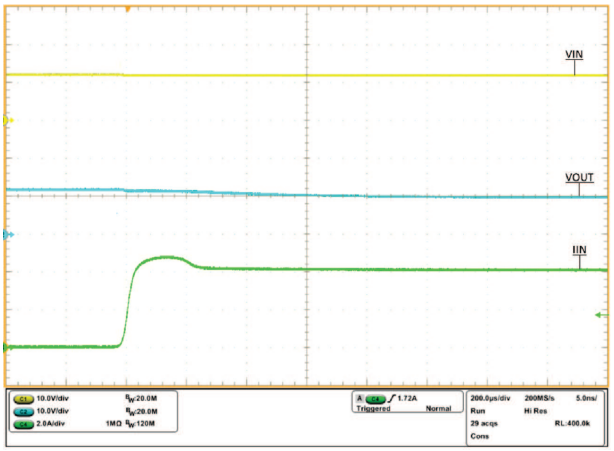


V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

図 37. Wake Up With Output Short to GND (Zoomed In)

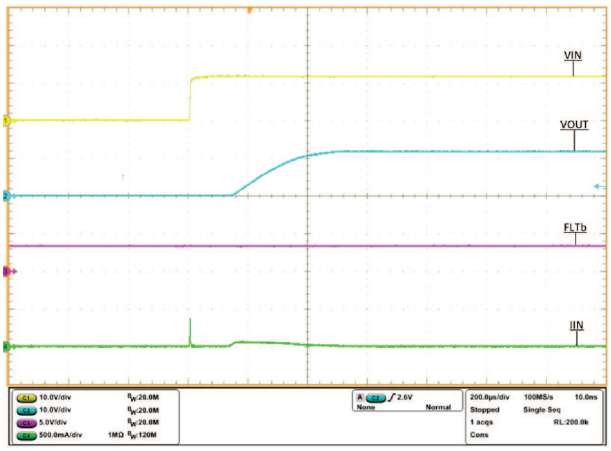
Copyright © 2017–2018, Texas Instruments Incorporated

Typical Characteristics (continued)



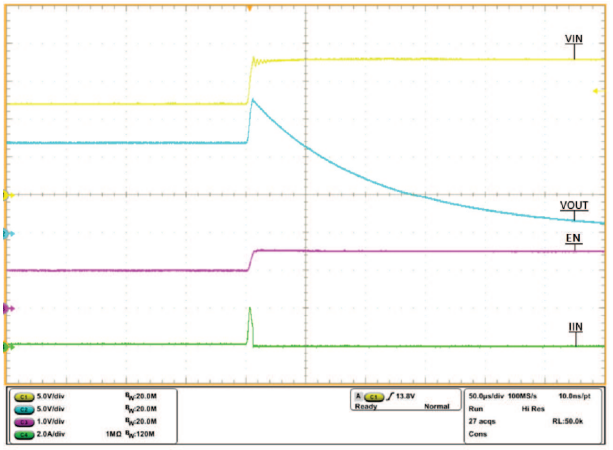
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, I_{OUT} stepped from 4 A to 4.8 A

図 38. Output Load Transient Response



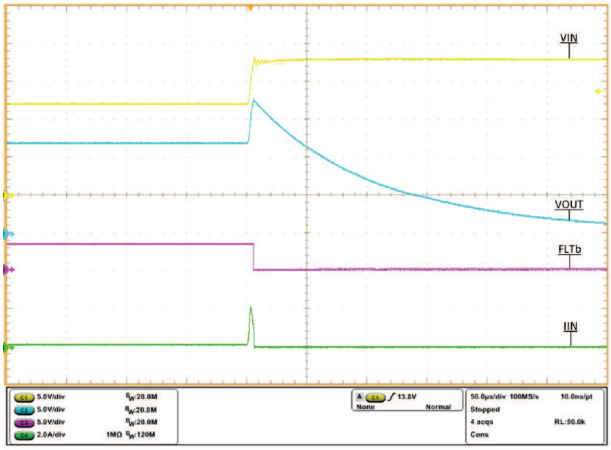
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ

図 39. Hot Plug Response



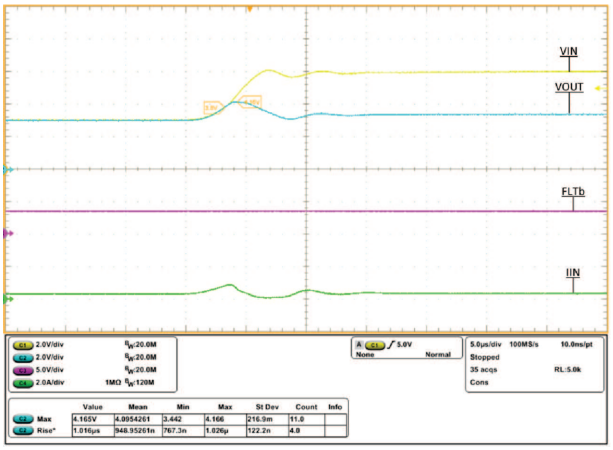
V_{IN} stepped from 12 V to 18 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 100 Ω

図 40. TPS259573 Overvoltage Lockout Response



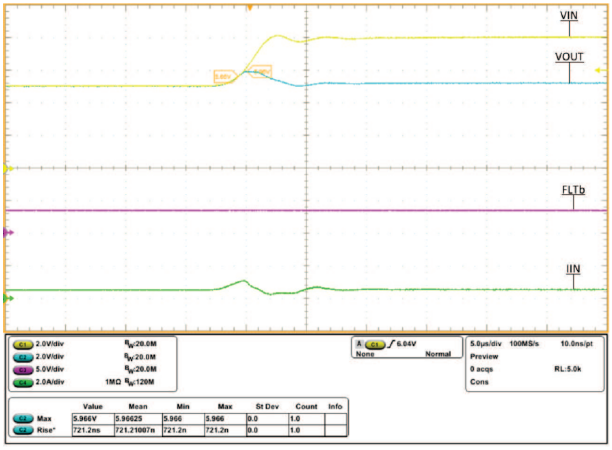
V_{IN} stepped from 12 V to 18 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 100 Ω

図 41. TPS259573 Overvoltage Lockout $\overline{FLT}$ Response



V_{IN} stepped from 3 V to 6 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$= 3.3 V through 10 kΩ, R_{OUT} = 10 Ω

図 42. TPS25952x Overvoltage Clamp Response

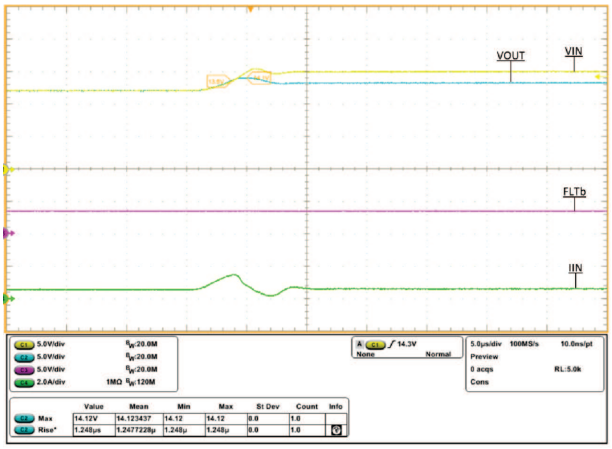


V_{IN} stepped from 5 V to 8 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 10 Ω

図 43. TPS25953x Overvoltage Clamp Response

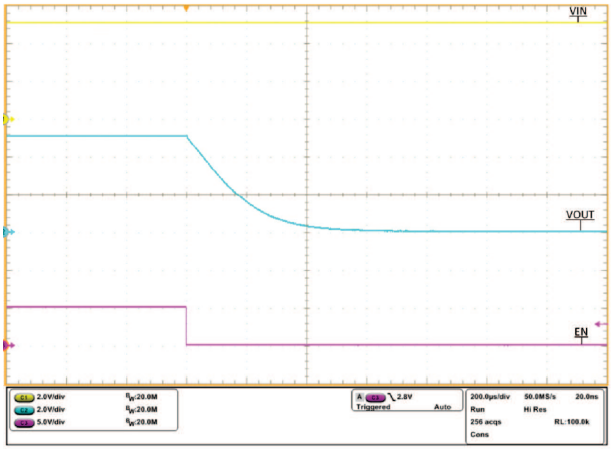
Copyright © 2017–2018, Texas Instruments Incorporated

Typical Characteristics (continued)



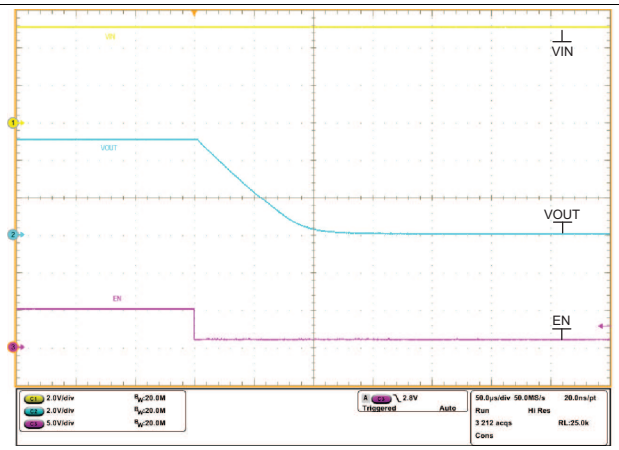
V_{IN} Stepped from 12 V to 15 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 20 Ω

図 44. TPS25954x Overvoltage Clamp Response



V_{IN} = 5 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

図 45. TPS2595x5 Quick Output Discharge, EN stepped from 5 V to 0 V



V_{IN} = 5 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

図 46. TPS2595x5 Quick Output Discharge, EN stepped from 5 V to 1 V

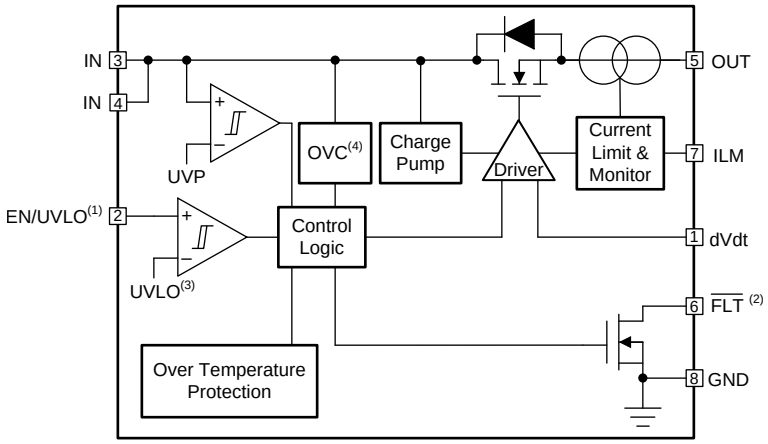
Copyright © 2017–2018, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The TPS2595xx devices are integrated eFuse that are used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

8.2 Functional Block Diagram



(1) For TPS2595x3, this pin is $\overline{\text{EN}}$/OVLO

(2) For TPS2595x5, this pin is QOD

(3) For TPS2595x3, this voltage is OVLO

(4) This block is not available in the TPS25957x

8.3 Feature Description

8.3.1 Undervoltage Protection (UVP) and Undervoltage Lockout (UVLO)

All the TPS2595xx devices constantly monitor the input supply to ensure that the load is powered up only when the voltage is at a sufficient level. During the start-up condition, the device waits for the input supply to rise above a fixed threshold V_{UVP} before it proceeds to turn ON the FET. Similarly, during the ON condition, if the input supply falls below the UVP threshold, the FET is turned OFF. The UVP rising and falling thresholds are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The TPS2595x0, TPS2595x1, TPS2595x5 devices provide an user programmable UVLO mechanism to ensure that the load is powered up only when the voltage is at a sufficient level. This can be achieved by dividing the input supply and feeding it to the EN/UVLO pin. Whenever the voltage at the EN/UVLO pin falls below a threshold V_{UVLO}, the device turns OFF the FET. The FET is turned ON again when the voltage rises above the threshold. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The user must choose the resistor divider values appropriately to map the desired input undervoltage level to the UVLO threshold of the part. See 図 47.

Copyright © 2017–2018, Texas Instruments Incorporated

Feature Description (continued)

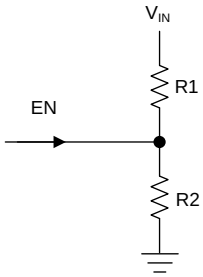


図 47. Undervoltage Lockout

$$V_{SUPPLY} = \frac{V_{UVLO} \times (R1 + R2)}{R2} \quad (1)$$

8.3.2 Overvoltage Protection

The TPS2595xx devices provide 2 ways to handle an input overvoltage condition.

8.3.2.1 Overvoltage Lockout (OVLO)

The TPS259573 device provides an user programmable OVLO mechanism to ensure that the supply to the load is cut off if the input supply voltage exceeds a certain level. This can be achieved by dividing the input supply and feeding it to the $\overline{EN}$/OVLO pin. Whenever the voltage at the $\overline{EN}$/OVLO pin rises above a threshold V_{OVLO}, the device turns OFF the FET. When the voltage at the $\overline{EN}$/OVLO pin falls below the threshold, the FET is turned ON again.

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

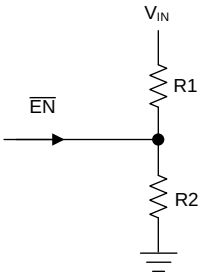


図 48. Overvoltage Lockout

8.3.2.2 Overvoltage Clamp (OVC)

The TPS25952x, TPS25953x, TPS25954x devices provide a mechanism to clamp the output voltage to a predefined level quickly if the input voltage crosses a certain threshold. This ensures the load is not exposed to high voltages on any overvoltage at the input supply, and lowers the dependency on external protection devices (such as TVS/Zener diodes) in this condition. Once the input supply voltage rises above the OVC threshold voltage V_{OVC}, the device responds by clamping the voltage to V_{CLAMP} within a very short response time t_{OVC}. As long as an overvoltage condition is present on the input, the output voltage will be clamped to V_{CLAMP}. When the input drops below the output clamp threshold V_{OVC}, the clamp releases the output voltage. See 図 49.

During the overvoltage clamp condition, there could be significant heat dissipation in the internal FET depending on the V_{IN} - V_{OUT} voltage drop and the current through the FET leading to a thermal shutdown if the condition persists for an extended period of time. In this case, the device would either stay latched-off or start a auto retry cycle as explained in the *Overtemperature Protection (OTP)* section.

Copyright © 2017–2018, Texas Instruments Incorporated

Feature Description (continued)

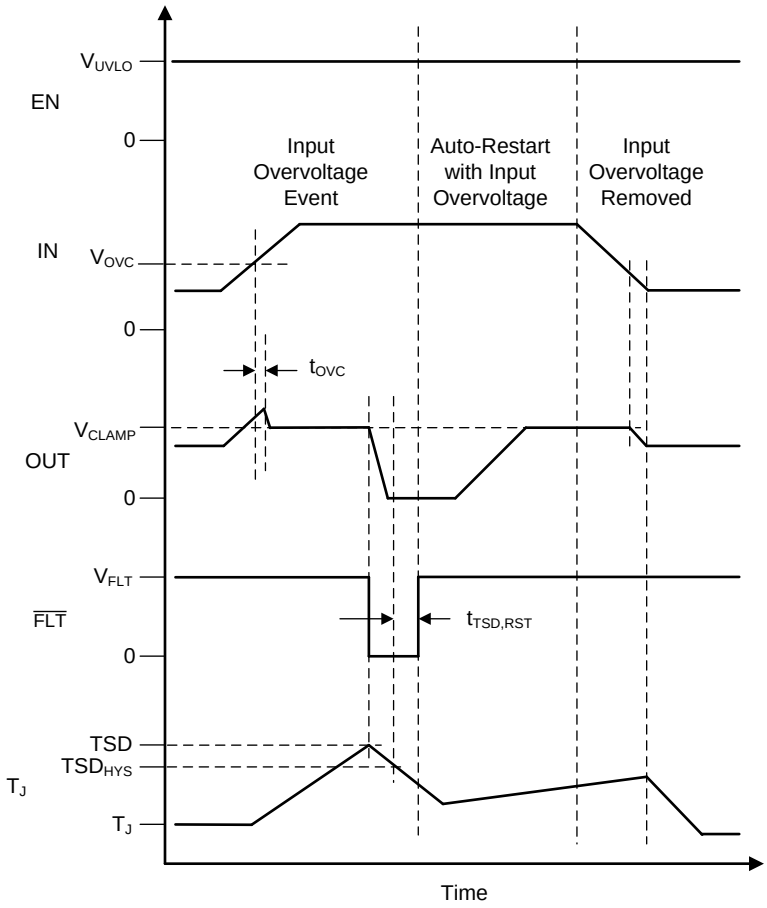


図 49. TPS2595xx Overvoltage Clamp Response (Auto-Retry)

Multiple device options are offered with different clamping voltage thresholds. See the *Device Comparison Table* for list of available voltage clamp options.

8.3.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS2595xx devices incorporates three levels of protection against overcurrent:

- Adjustable slew rate for inrush current control (dVdt).
- Active current limiting (I_{LIMIT}) for overcurrent protection.
- A fast short circuit limit (I_{SC}) to protect against hard short circuits.

8.3.3.1 Slew Rate and Inrush Current Control (dVdt)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. 式 2 can be used to find the slew rate SR_{ON} required to limit the inrush current I_{INRUSH} for a given load capacitance C_{OUT}.

$$SR_{ON}\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{2}$$

For loads requiring a slower rising slew rate, a capacitance can be added to the dVdt pin to adjust the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using 式 3.

Copyright © 2017–2018, Texas Instruments Incorporated

Feature Description (continued)

$$C_{dVdt}\,(pF) = \frac{42000}{SR_{ON}\left(\frac{V}{ms}\right)} \quad (3)$$

8.3.3.2 Active Current Limiting

The load current is monitored during start-up and normal operation. When the load current exceeds the current limit trip point I_{LIMIT} programmed by R_{ILM} resistor, the device regulates the current to the set limit I_{LIMIT} within t_{LIM}. The device exits current limiting when the load current falls below limit. 式 4 can be used to find the R_{ILM} value for a desired current limit.

$$R_{ILM} = \frac{2000}{\left(I_{LIMIT} - 0.04\right)} \quad (4)$$

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to a thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto retry cycle as explained in the *Overtemperature Protection (OTP)* section.

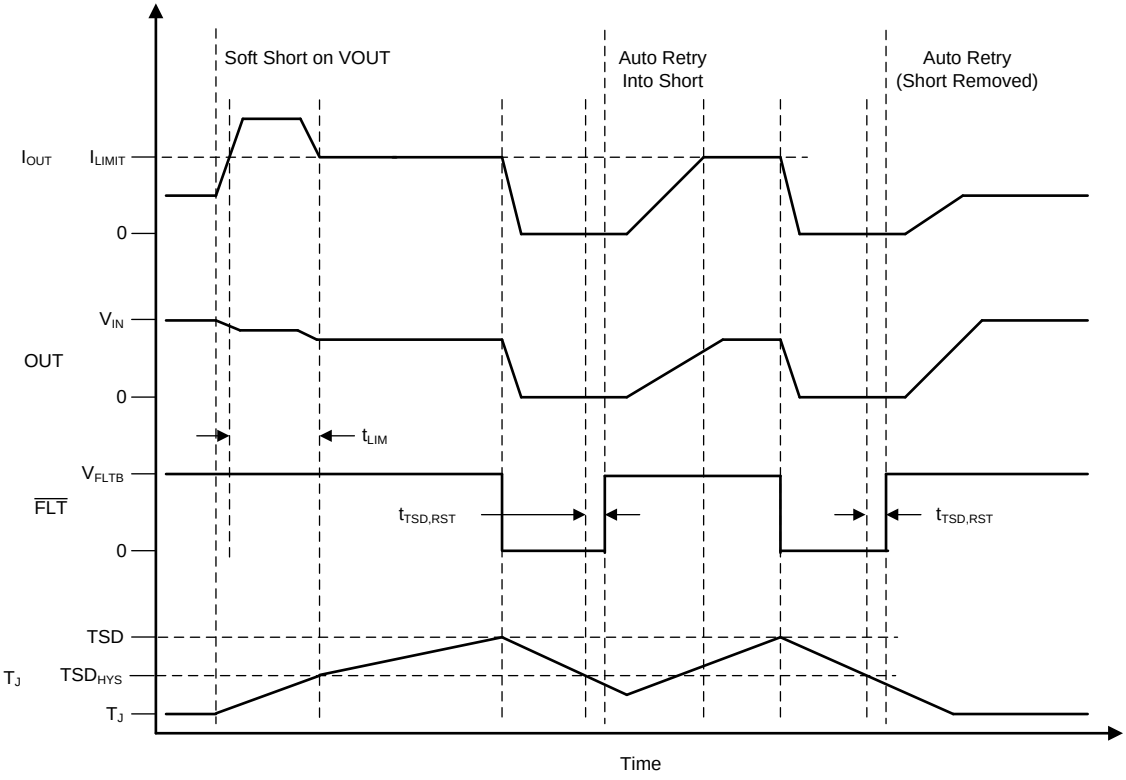


図 50. TPS2595x1, TPS2595x3, TPS2595x5 Overcurrent Response (Auto-Retry)

Feature Description (continued)

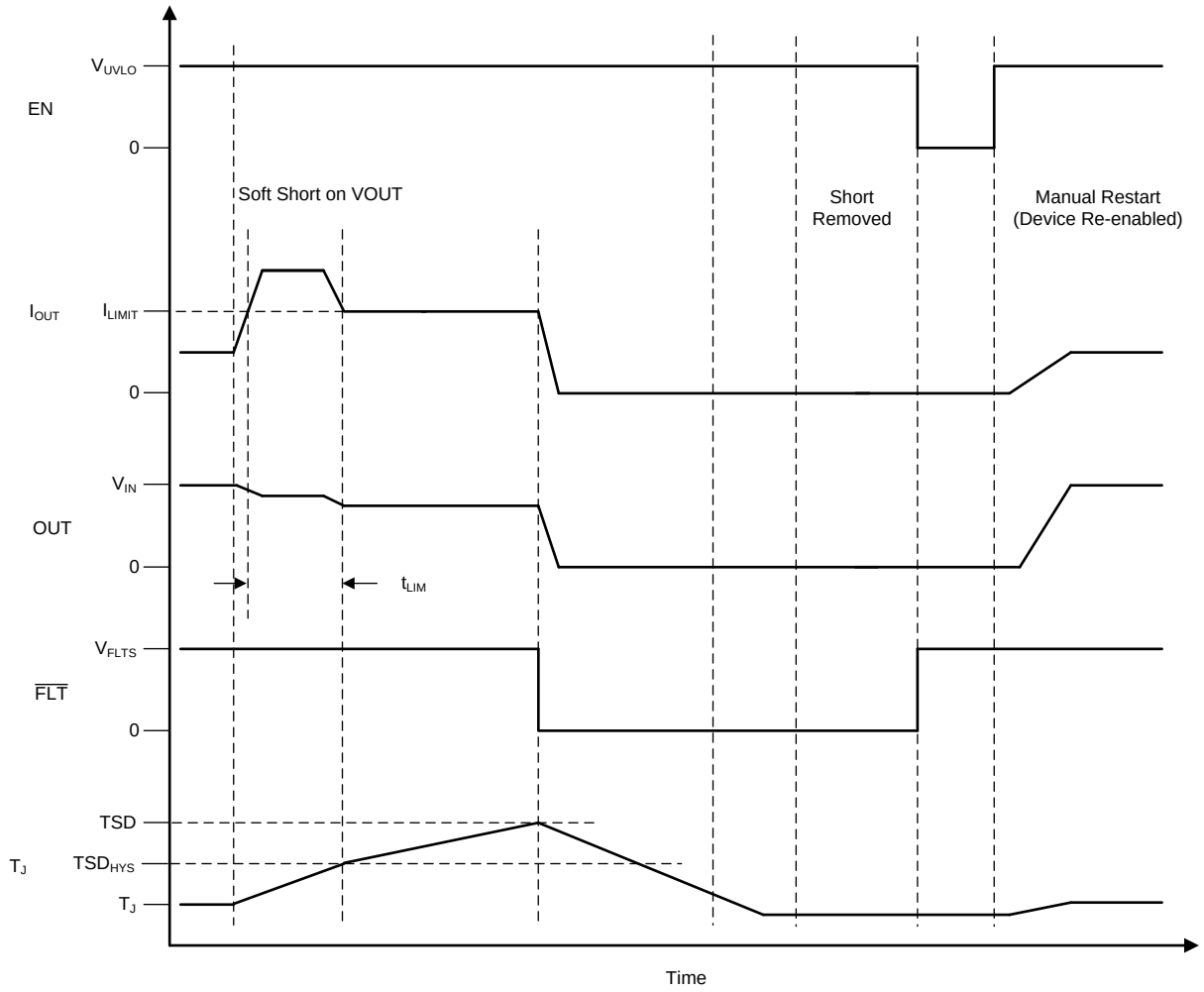


図 51. TPS2595x0 Overcurrent Response (Latch-Off)

8.3.3.3 Short Circuit Protection

The current through the device increases very rapidly during a transient short circuit event. The short circuit threshold I_{SC} is adjusted based on the selected current limit. When a short circuit is detected, the device quickly limits the current to I_{LIMIT}. The device stops limiting the current once the load current falls below the programmed I_{LIMIT} threshold. See 図 52.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and leads to a thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto retry cycle as explained in the *Overtemperature Protection (OTP)* section.

Copyright © 2017–2018, Texas Instruments Incorporated

Feature Description (continued)

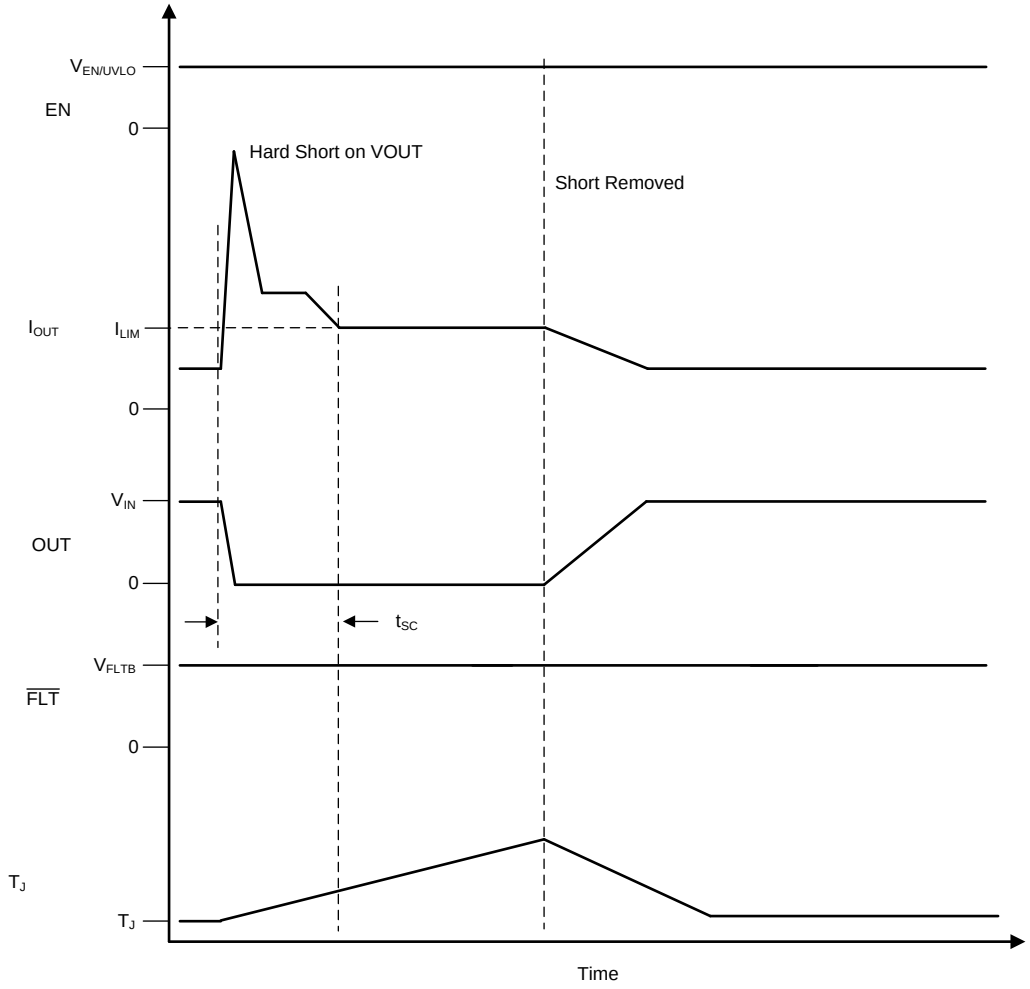


図 52. TPS2595xx Short Circuit Response

8.3.4 Overtemperature Protection (OTP)

Thermal shutdown occurs when the junction temperature T_J exceeds TSD. When the TPS2595x0 detects a thermal overload, it shuts down and remains latched off until the device is re-enabled or power cycled. When the TPS2595x1, TPS2595x3, TPS2595x5 devices detects a thermal overload, it remains off until the T_J decreases by TSD_{HYS} and then waits for an additional delay of $t_{TSD,RST}$ after which it automatically retries to turn on if it is still enabled. See 表 1.

表 1. TPS2595xx Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS2595x0 (Latch-off)	$T_J \geq$ TSD	$T_J <$ TSD and Device Power Cycled or re-enabled using EN/UVLO pin
TPS2595x1, TPS2595x3, TPS2595x5 (Auto-retry)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} and $t_{TSD,RST}$ Timer Expired

Copyright © 2017–2018, Texas Instruments Incorporated

8.3.5 Fault Indication ($\overline{FLT}$)

表 2 summarizes the protection response to various fault conditions.

表 2. TPS2595x0, TPS2595x1, TPS2595x3 Fault Summary

EVENT / FAULT	PROTECTION RESPONSE	$\overline{FLT}$ INDICATION
Overtemperature	Shutdown	Yes
Overvoltage	Output Voltage Clamp (OVC) (TPS25952x,TPS25953x,TPS25954x only)	No
Overvoltage	Shutdown (OVLO) (TPS259573 only)	Yes
Undervoltage	Shutdown (UVP or UVLO)	No
Overcurrent	Current Limiting	No
Short circuit	Current Limiting	No
ILM pin open	Shutdown	No
ILM pin short	Shutdown If $I_{OUT} > I_{CB}$	Yes If $I_{OUT} > I_{CB}$

When the TPS2595x0, TPS2595x1, TPS2595x3 devices are turned off as a result of a fault as described in the table above, the $\overline{FLT}$ pin is pulled low.

All faults will be cleared if the device loses power or if it is re-enabled using the EN/UVLO (or $\overline{EN}$/OVLO) pin.

8.3.6 Quick Output Discharge (QOD)

Some applications require the output capacitor to be discharged quickly when the eFuse is turned off. This prevents any unpredictable behavior from the downstream devices as the capacitor discharges slowly. The TPS2595x5 device provides a Quick Output Discharge feature that can be enabled by connecting OUT pin to QOD pin. An internal FET provides a fast discharge path for the output capacitor resulting in the OUT voltage falling to 0 V in a short time. The FET initially operates in saturation region and provides a constant current discharge. After the FET enters linear region, it offers a discharge path similar to a resistor.

It is possible to model this as a simple equivalent resistance, which would discharge a given capacitor charged to a given voltage in the same time as the overall discharge circuit. This parameter is specified as the effective QOD resistance R_{QOD} for the device. It takes a time equivalent to 5 time constants ($\tau = R \times C$) to discharge a capacitor by 99.3%. For example, with an effective QOD resistance of 19 Ω, the time taken to discharge a 100-µF capacitor from 5 V to 35 mV can be calculated as in 式 5.

$$t_{Discharge} = 5 \times 19\ \Omega \times 100\ \mu F = 9.5\ ms \quad (5)$$

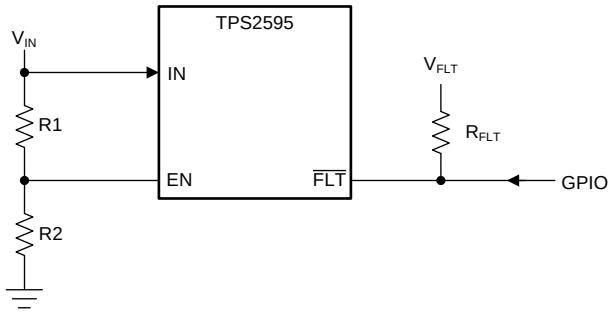
Copyright © 2017–2018, Texas Instruments Incorporated

8.4 Device Functional Modes

The features of the device depend on the operating mode.

8.4.1 Enable and Fault Pin Functional Mode 1: Single Device, Self-Controlled

In this mode of operation, the device is enabled by the V_{IN} voltage without the need of an external processor to drive the ENABLE pin. The $\overline{FLT}$ pin is optionally monitored by an external host. See 図 53.

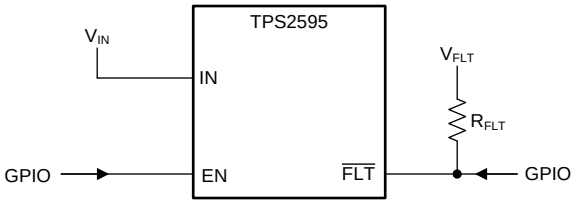


Copyright © 2017, Texas Instruments Incorporated

図 53. Single Device, Self-Controlled

8.4.2 Enable and Fault Pin Functional Mode 2: Single Device, Host-Controlled

In this mode of operation, the device enable pin is driven by an external host. The pin can be driven directly from a GPIO without the need for any glue logic. The $\overline{FLT}$ pin is optionally monitored by the host. See 図 54.



Copyright © 2017, Texas Instruments Incorporated

図 54. Single Device, Host-Controlled

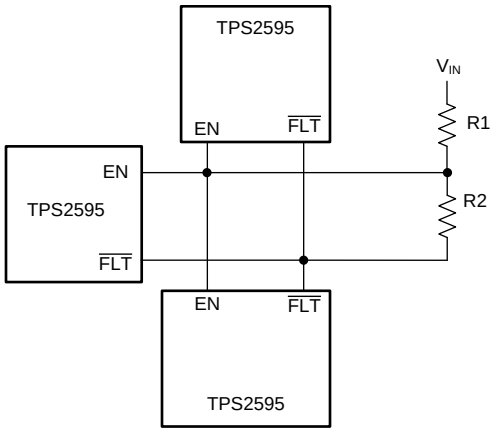
8.4.3 Enable and Fault Pin Functional Mode 2: Multiple Devices, Self-Controlled

In this mode of operation, the devices are self-controlled (no host present). The EN and $\overline{FLT}$ pins are shorted together, and connected with up to three total devices as shown in 図 55. In this configuration, when any one of the TPS2595xx devices detects a fault, it automatically disables the other TPS2595xx devices in the system.

注

This configuration is only applicable to the Active High Enable variants TPS2595x0, TPS2595x1, TPS2595x5.

Device Functional Modes (continued)



Copyright © 2017, Texas Instruments Incorporated

図 55. Multiple Devices, Self-Controlled

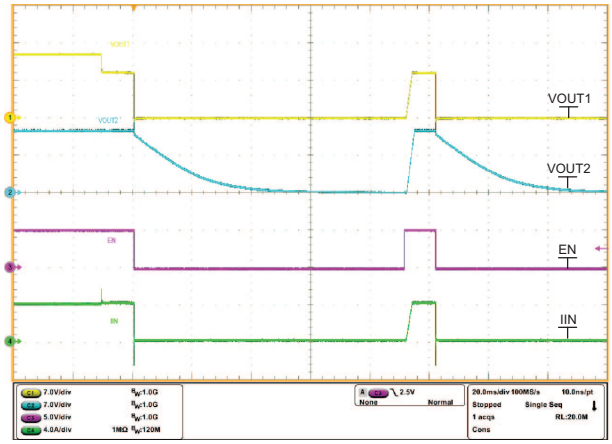


図 56. TPS259541 Self-controlled Mode Response with Overload Fault on OUT1 Followed by Auto-retry with Persistent Fault

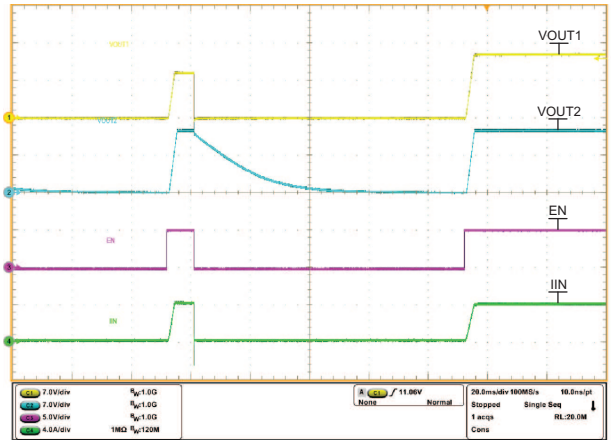


図 57. TPS259541 Self-controlled Mode Response with Overload on OUT1 Followed by Recovery with Fault Removed

Copyright © 2017–2018, Texas Instruments Incorporated

9 Application and Implementation

注

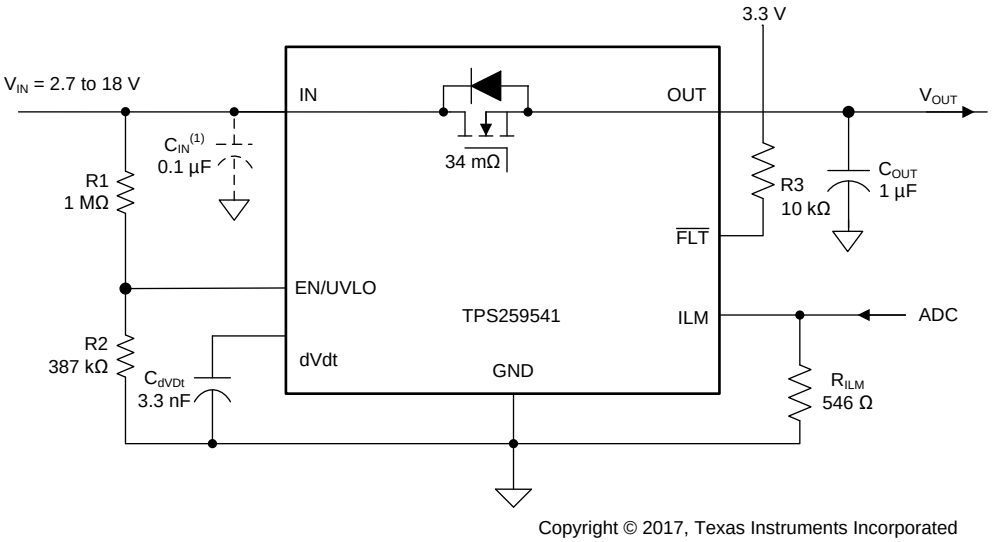
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2595xx device is an integrated eFuse that is typically used for hot-swap and power rail protection applications. The device operates from 2.7 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as set-top box, DTVs, gaming consoles, SSDs, HDDs, and smart meters. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool *TPS2595xx Design Calculation Tool* is available.

9.2 Typical Application



Copyright © 2017, Texas Instruments Incorporated

(1) C_{IN} is optional and 0.1 µF is recommended to suppress transients due to the inductance of PCB routing or from input wiring.

図 58. Typical Application Schematic: Simple e-Fuse for Set-Top Boxes

9.2.1 Design Requirements

表 3 lists the TPS25954x design requirements.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage , V_{IN}	12 V
Undervoltage lockout set point, V_{UV}	4.3 V
Overvoltage protection set point , V_{OV}	Default: V_{OVC} = 13.7 V
Load at start-up, $R_{L(SU)}$	4 Ω
Current limit, I_{LIMIT}	3.7 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperatures, T_A	85°C

9.2.2 Detailed Design Procedure

The designer must know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

9.2.2.1 Programming the Current-Limit Threshold: R_{ILM} Selection

The R_{ILM} resistor at the ILM pin sets the over load current limit, this can be set using 式 6.

$$R_{ILM} = \frac{2000}{I_{LIMIT} - 0.04} \tag{6}$$

For I_{LIMIT} = 3.7 A, from 式 6, R_{ILM} is 546 Ω, choose closest standard value resistor with 1% tolerance.

9.2.2.2 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving 式 7.

$$V_{UV} = \frac{R1 + R2}{R2} \times V_{UVLO(R)} \tag{7}$$

Where $V_{UVLO(R)}$ is UVLO rising threshold (1.2 V). Because R1 and R2 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}.

The current drawn by R1 and R2 from the power supply is $I_{R12} = V_{IN} / (R1 + R2)$.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R12} must be chosen to be 20 times greater than the leakage current expected.

To set the UVLO at V_{UVR} = 4.3 V, select R2 = 387 kΩ, and R1 = 1 MΩ.

9.2.2.3 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The required ramp-up capacitor C_{dVdT} is calculated considering the two possible cases (see Case 1: Start-Up Without Load. Only Output Capacitance C_{OUT} Draws Current and Case 2: Start-Up With Load. Output Capacitance C_{OUT} and Load Draw Current).

9.2.2.3.1 Case 1: Start-Up Without Load. Only Output Capacitance C_{OUT} Draws Current

During start-up, as the output capacitor charges, the voltage drop as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using 式 9.

For TPS2592xx device, the inrush current is determined as shown in 式 8.

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{dVdT}} \tag{8}$$

Power dissipation during start-up is shown in 式 9.

Copyright © 2017–2018, Texas Instruments Incorporated

$$P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (9)$$

式 9 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.2.3.2 Case 2: Start-Up With Load. Output Capacitance C_{OUT} and Load Draw Current

When the load draws current during the turnon sequence, there is additional power dissipated. Considering a resistive load during start-up $R_{L(SU)}$, load current ramps up proportionally with increase in output voltage during T_{dVdT} time. 式 10 to 式 13 show the average power dissipation in the internal FET during charging time due to resistive load.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V_{IN}^2}{R_{L(SU)}} \quad (10)$$

Total power dissipated in the device during start-up is 式 11.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (11)$$

Total current during start-up is given by 式 12.

$$I_{STARTUP} = I_{INRUSH} + I_L(t) \quad (12)$$

If $I_{STARTUP} > I_{LIMIT}$, the device limits the current to I_{LIMIT} and the current-limited charging time is determined by 式 13.

$$T_{dvdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{LIMIT}}{I_{INRUSH}} - 1 + LN\left(\frac{I_{INRUSH}}{I_{LIMIT} - \frac{V_{IN}}{R_{L(SU)}}} \right) \right] \quad (13)$$

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in 図 59.

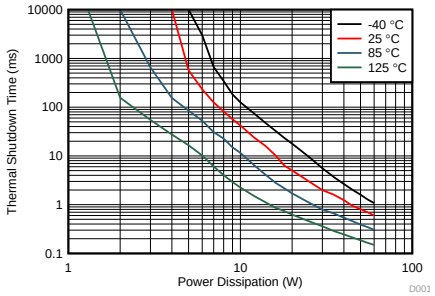


図 59. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdt} = OPEN. The default slew rate for C_{dVdt} = OPEN is 38.2 mV/µs. With slew rate of 38.2 mV/µs, the ramp-up time T_{dVdt} for 12 V input is 248 µs.

The inrush current drawn by the load capacitance C_{OUT} during ramp-up using 式 14.

$$I_{INRUSH} = \frac{1\,\mu F \times 38.2\,mV}{\mu s} = 38.2\,mA \quad (14)$$

The inrush power dissipation is calculated using 式 15.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 38.2\,m = 229.2\,mW \quad (15)$$

For 229.2 mW of power loss, the thermal shutdown time of the device must not be less than the ramp-up time T_{dVdt} to avoid the false trip at the maximum operating temperature. 図 59 shows the thermal shutdown limit at T_A = 85°C, for 229.2 mW of power, the shutdown time is infinite. Therefore, it is safe to use 248 µs as the start-up time without any load on the output.

Copyright © 2017–2018, Texas Instruments Incorporated

The additional power dissipation when a 4 Ω load is present during start-up is calculated using 式 10.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6 \text{ W} \quad (16)$$

The total device power dissipation during start-up is given in 式 17.

$$P_{D(STARTUP)} = 6 + 229.2 \text{ m} = 6.229 \text{ W} \quad (17)$$

The 図 59 shows T_A = 85°C and the thermal shutdown time for 6.229 W is more than 10 ms, which is well within the acceptable limits to not use an external capacitor C_{dVdt} with a start-up load of 4 Ω.

When C_{OUT} is large, there is a need to decrease the power dissipation during start-up. This can be done by increasing the value of the C_{dVdt} capacitor.

9.2.3 Support Component Selection: C_{IN}

C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range from 0.001 µF to 0.1 µF is recommended for C_{IN}.

9.2.4 Application Curves

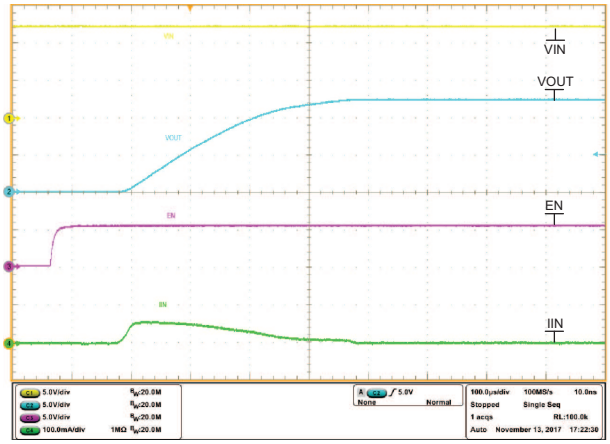


図 60. Output Ramp without Any Load

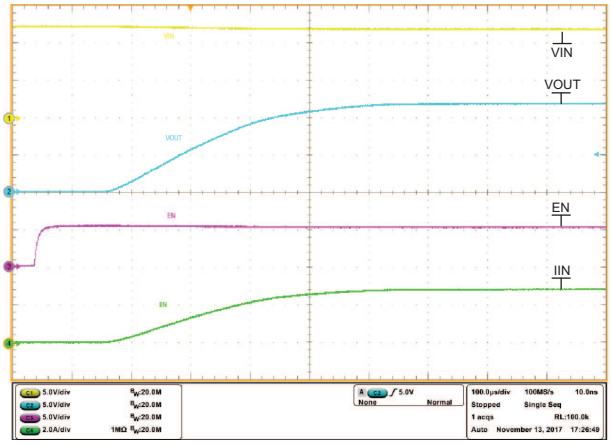
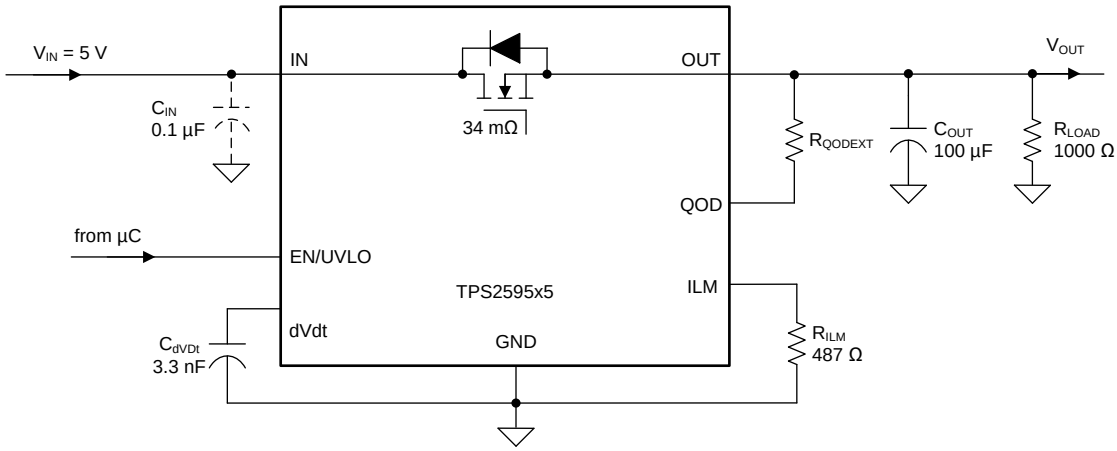


図 61. Output Ramp with 4 Ω Load at Start-up

9.2.5 Controlled Power Down (Quick Output Discharge) using TPS2595x5

When the TPS2595x5 device is disabled, the output voltage is left floating and the power-down profile is entirely dictated by the load. In some applications, this can lead to undesired activity because the load is not powered down to a defined state. Controlled output discharge can ensure the load is completely turned off and is not in an undefined operational state. The QOD pin in the TPS2595x5 device can be connected to the OUT pin to facilitate the Quick Output Discharge function, as shown in 図 62. When the TPS2595x5 device is disabled, the QOD pin is pulled low and provides a quick discharge path for the output capacitor. The output voltage discharge rate is dictated by the output capacitor C_{OUT}, the total discharge path resistance (internal plus external), and the load.

Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2017, Texas Instruments Incorporated

図 62. Circuit Implementation with Quick Output Discharge Function using TPS2595x5

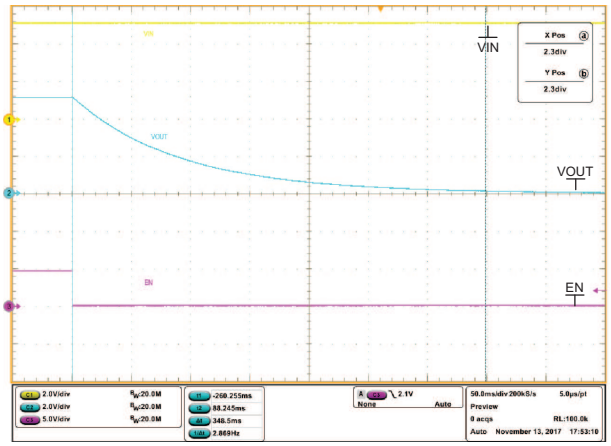


図 63. Output Voltage Discharge using TPS259535 without QOD [V_{IN} = 5 V, EN = H → L, C_{OUT} = 100 µF, R_{LOAD} = 1000 Ω, R_{QODEXT} = OPEN]

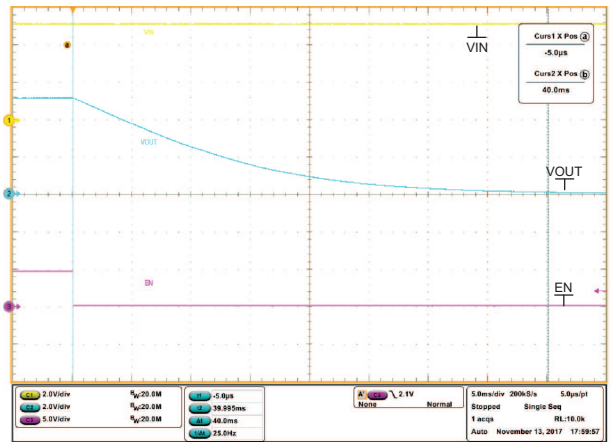
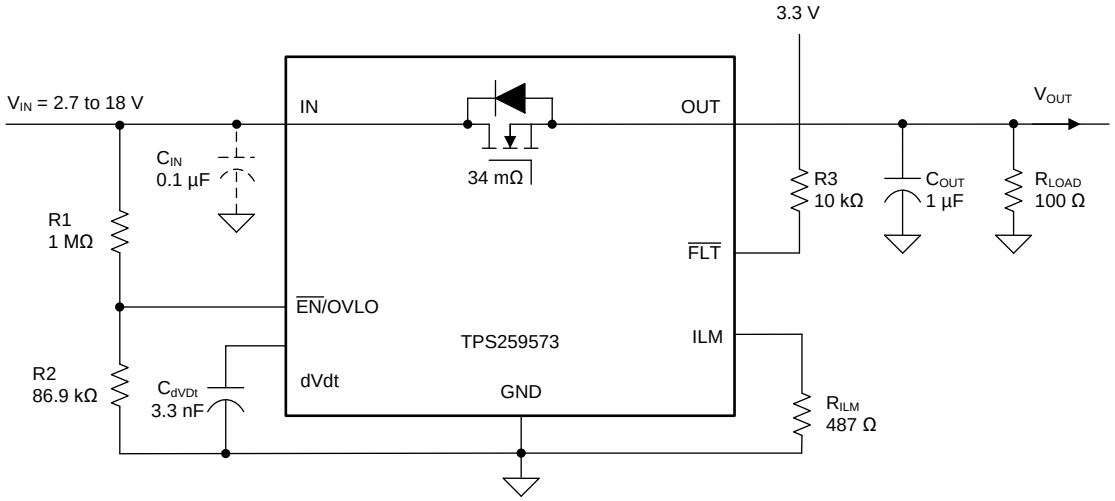


図 64. Output Voltage Discharge using TPS259535 with QOD [V_{IN} = 5 V, EN = H → L, C_{OUT} = 100 µF, R_{LOAD} = 1000 Ω, R_{QODEXT} = Short]

9.2.6 Overvoltage Lockout using TPS259573

The TPS259573 device incorporates a circuit to protect the system during overvoltage conditions. A resistor divider connected from the supply to the EN/OVLO pin to GND (as shown in 図 65) programs the overvoltage threshold. A voltage more than V_{OVLO} on the EN/OVLO pin turns off the internal FET and protects the downstream load. 図 66 shows overvoltage cut-off at the input voltage of 15 V.



Copyright © 2017, Texas Instruments Incorporated

図 65. Circuit Implementation for Overvoltage Lockout using TPS259573

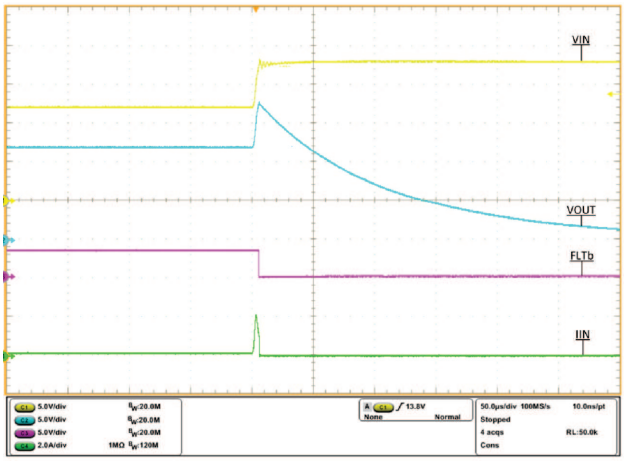


図 66. Overvoltage Lockout Response using TPS259573

Copyright © 2017–2018, Texas Instruments Incorporated

10 Power Supply Recommendations

The TPS2595xx devices are designed for a supply voltage range of 2.7 V ≤ VIN ≤ 18 V. An input ceramic bypass capacitor higher than 0.1 μF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Use a low-value ceramic capacitor C_{IN} = 0.001 μF to 0.1 μF to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with 式 18:

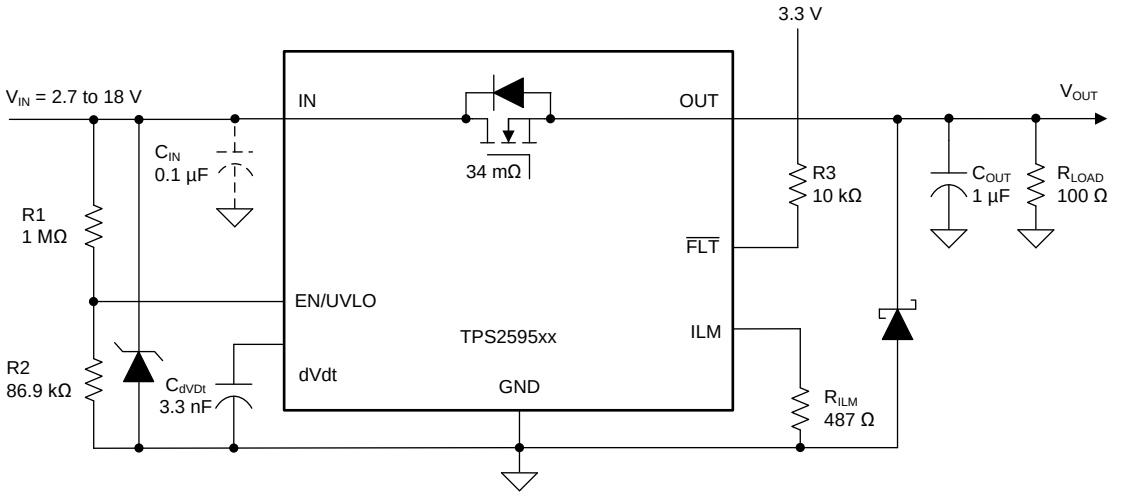
$$V_{SPIKE\,(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (18)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in 図 67.



Copyright © 2017, Texas Instruments Incorporated

図 67. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

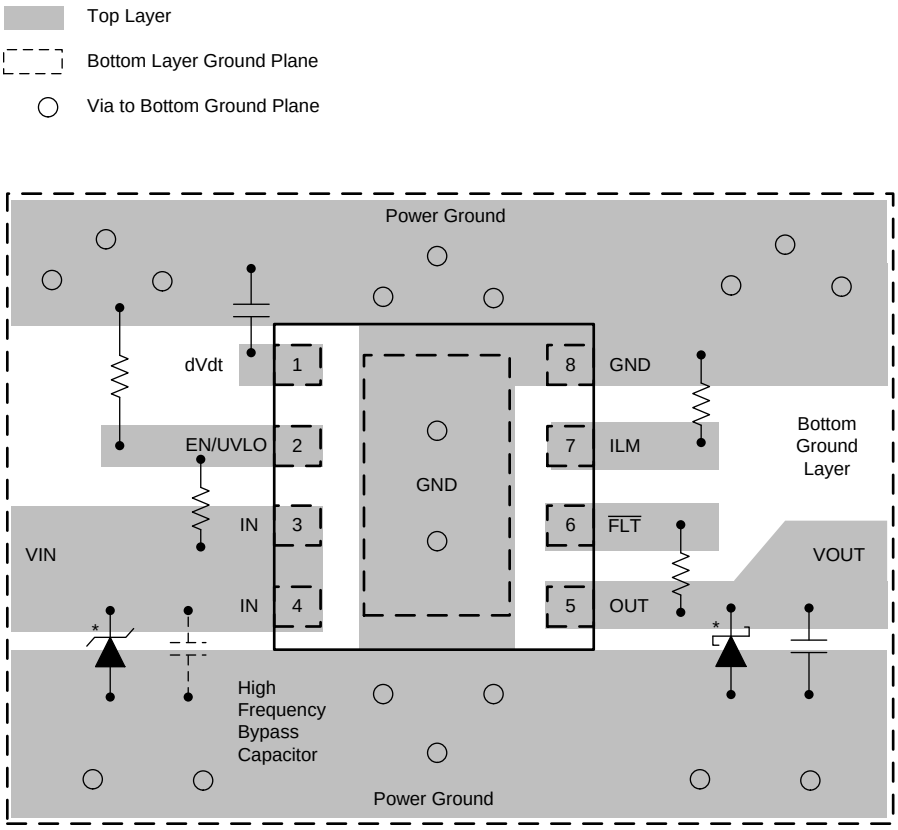
11.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.01 µF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See 図 68 for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - Resistors for the EN/UVLO (or $\overline{EN}$/OVLO) pin

  Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM} and C_{dVdT} components to the device must be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; *Layout Example* has been shown to produce good results and is intended as a guideline.

Copyright © 2017–2018, Texas Instruments Incorporated

11.2 Layout Example



(1) Optional: Needed only to suppress the transients caused by inductive load switching

図 68. TPS2595xx Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『TPS2595EVM eFuse評価ボード』
『TPS2595xx 設計計算ツール』

12.1.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS259520	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259521	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259530	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259531	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259533	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259540	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259541	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259570	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259571	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259573	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259525	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS259535	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

Copyright © 2017–2018, Texas Instruments Incorporated

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2017–2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259520DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES20
TPS259520DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES20
TPS259520DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES20
TPS259520DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES20
TPS259520DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES20
TPS259520DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES20
TPS259521DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES21
TPS259521DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES21
TPS259521DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES21
TPS259521DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES21
TPS259521DSGTG4	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES21
TPS259521DSGTG4.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES21
TPS259525DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES25
TPS259525DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES25
TPS259525DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES25
TPS259525DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES25
TPS259530DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES30
TPS259530DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES30
TPS259530DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES30
TPS259530DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES30
TPS259531DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES31
TPS259531DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES31
TPS259531DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES31
TPS259531DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES31
TPS259531DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES31
TPS259531DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES31
TPS259533DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES33
TPS259533DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES33
TPS259533DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES33

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259533DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES33
TPS259533DSGTG4	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES33
TPS259533DSGTG4.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES33
TPS259535DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES35
TPS259535DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES35
TPS259535DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES35
TPS259535DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES35
TPS259540DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES40
TPS259540DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES40
TPS259540DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES40
TPS259540DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES40
TPS259540DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES40
TPS259540DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES40
TPS259541DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES41
TPS259541DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES41
TPS259541DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES41
TPS259541DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES41
TPS259541DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES41
TPS259541DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES41
TPS259570DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES70
TPS259570DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES70
TPS259570DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES70
TPS259570DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES70
TPS259570DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES70
TPS259570DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES70
TPS259571DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES71
TPS259571DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES71
TPS259571DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES71
TPS259571DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES71
TPS259571DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES71
TPS259571DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES71

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259573DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES73
TPS259573DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES73
TPS259573DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES73
TPS259573DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES73
TPS259573DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES73
TPS259573DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ES73

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

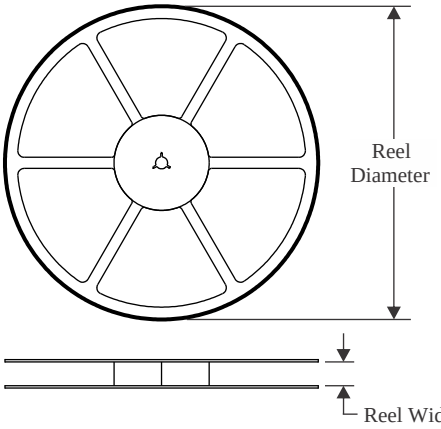
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

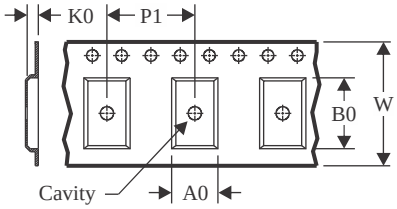
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

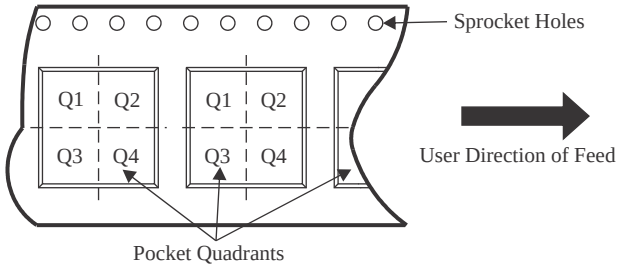


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

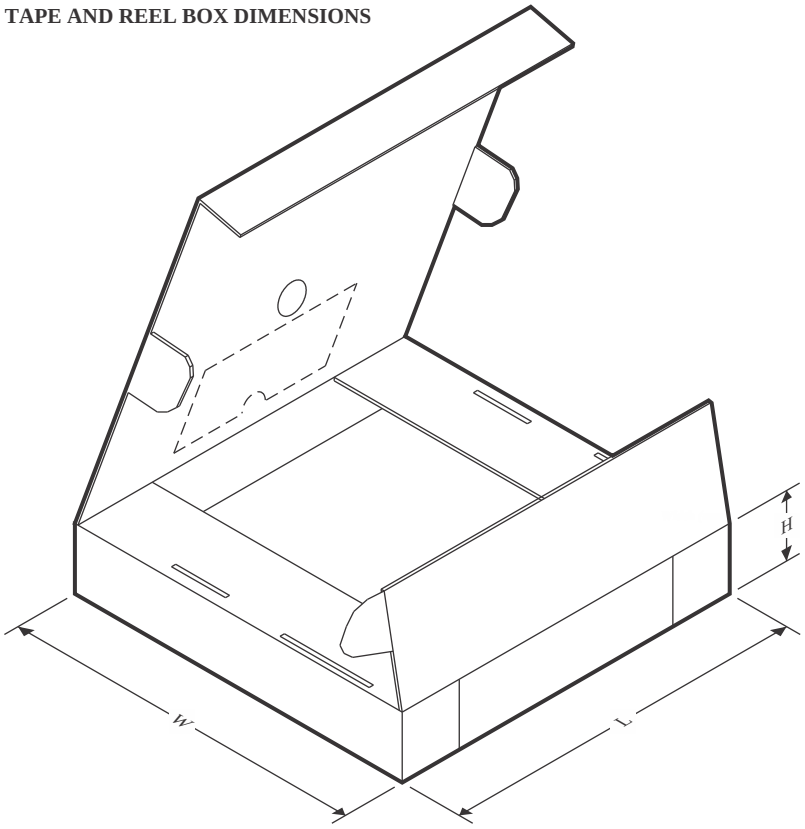


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259520DSGR	WSON	DSG	8	3000	178.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259520DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259520DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259521DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259521DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259521DSGTG4	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259525DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259525DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259530DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259530DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259531DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259531DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259531DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259533DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259533DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259533DSGTG4	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259535DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259535DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259540DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259540DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259540DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259541DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259541DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259541DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259570DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259570DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259570DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259571DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259571DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259571DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259573DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259573DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259573DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259520DSGR	WSON	DSG	8	3000	208.0	191.0	35.0
TPS259520DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259520DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259521DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259521DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259521DSGTG4	WSON	DSG	8	250	210.0	185.0	35.0
TPS259525DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259525DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259530DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259530DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259531DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259531DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259531DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259533DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259533DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259533DSGTG4	WSON	DSG	8	250	210.0	185.0	35.0
TPS259535DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259535DSGT	WSON	DSG	8	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259540DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259540DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259540DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259541DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259541DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259541DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259570DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259570DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259570DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259571DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259571DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259571DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259573DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259573DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259573DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

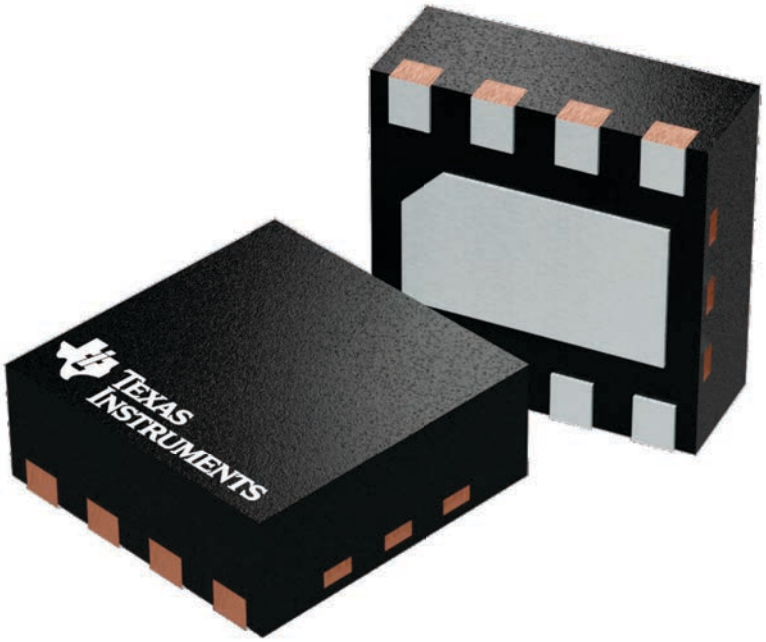
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



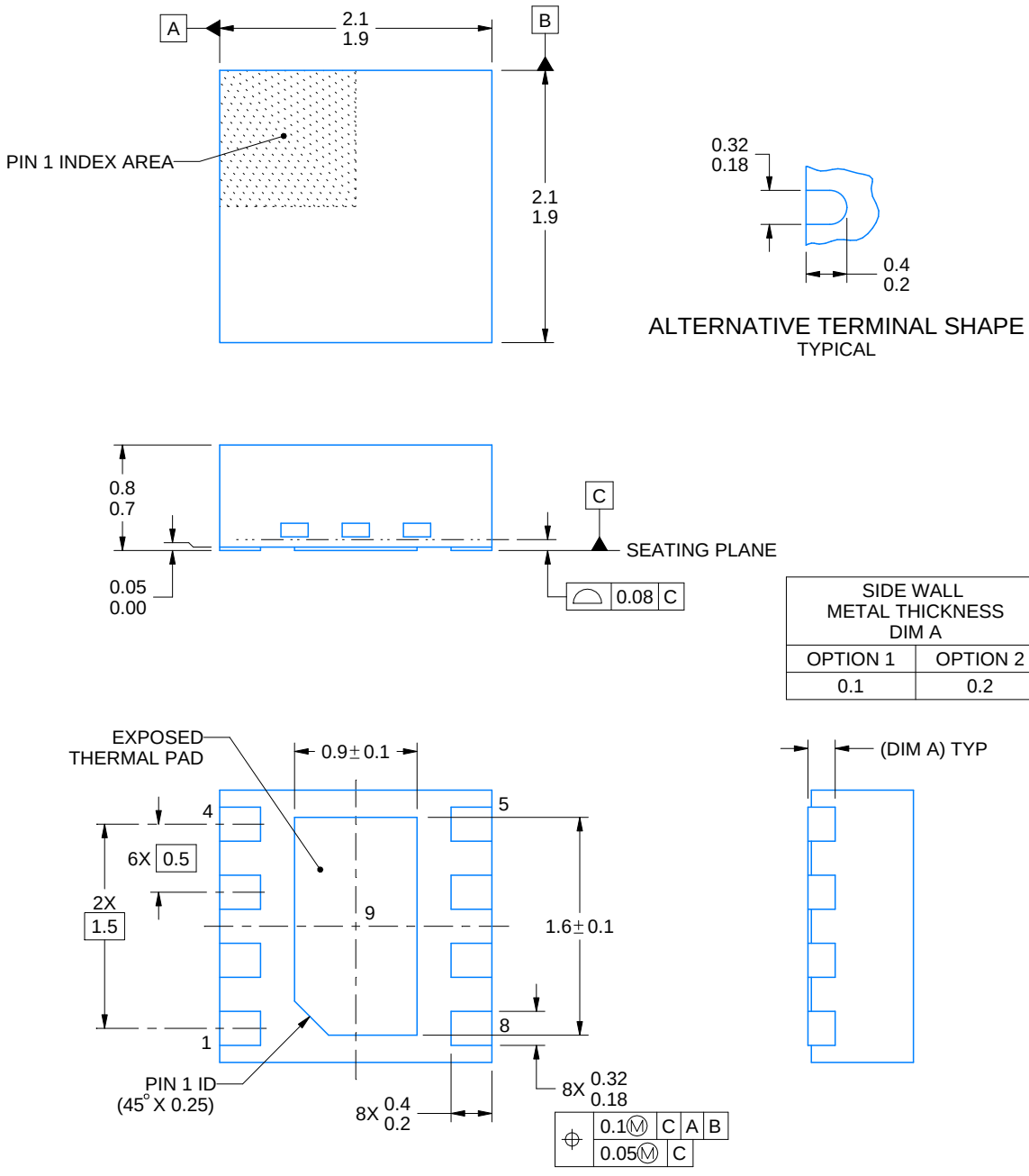
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

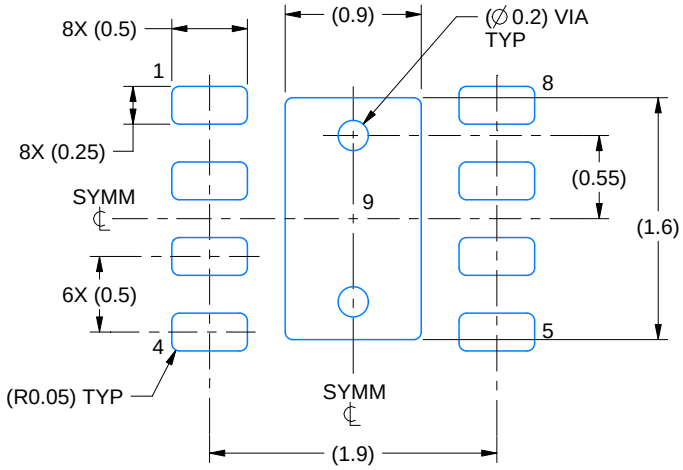
PLASTIC SMALL OUTLINE - NO LEAD



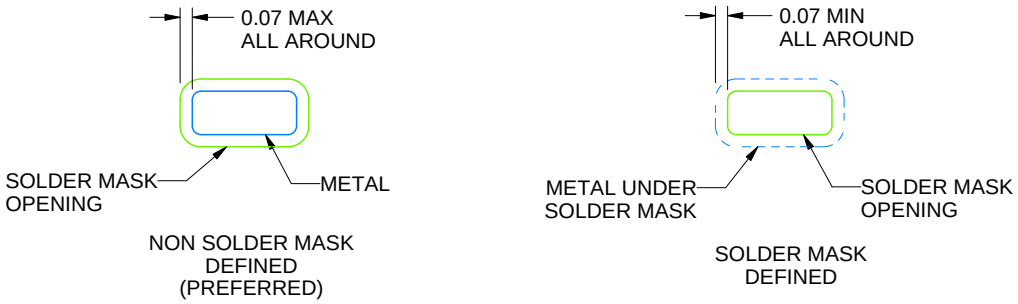
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

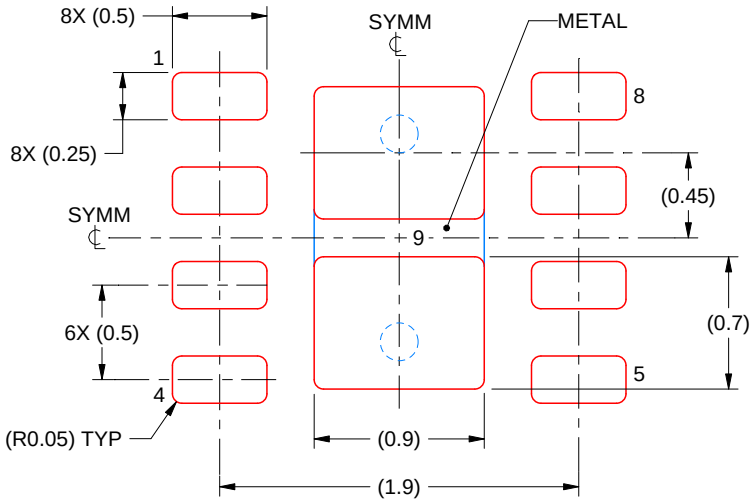


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月