TEXAS INSTRUMENTS
TPS25961
JAJSOA2 – DECEMBER 2022

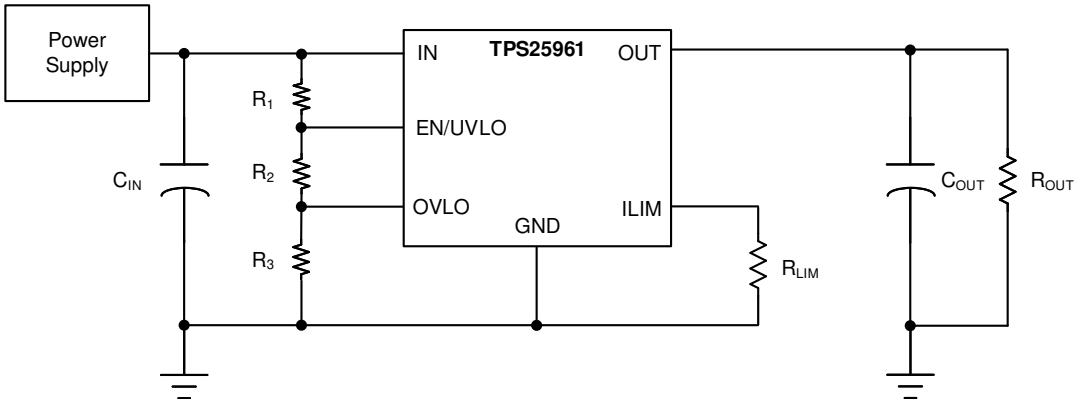
TPS25961 調整可能な電流制限機能と短絡保護機能搭載の 2.7V～19V、106mΩ、eFuse

1 特長

- 広い入力電圧範囲:2.7 V～19 V
  - 絶対最大定格 21V
- 低い オン抵抗:Ron = 106 mΩ (標準値)
- アクティブ High のイネーブル入力、調整可能な低電圧ロックアウト (UVLO) 付き
- 応答時間 1.3µs (標準値) の過電圧保護機能
  - 固定の内部スレッショルド:5.98V (標準値)
  - 外付けの分圧抵抗により調整可能なスレッショルド
- 過電流保護:
  - 調整可能な電流制限スレッショルド:0.1A～2A
  - 電流制限精度:
    - 電流範囲全体で±20% (標準値)
    - 1.45A の電流制限で ±18% (最大値、T_A = 25℃)
- 応答時間 5µs (標準値) の短絡保護機能
- 出力スルーレート制御機能 (dVdt):5.17V/ms (標準値)
- 過熱保護 (OTP)
- フォルト後の自動リトライ
- 低い静止電流:130µA (標準値)
- UL 2367 認定 (申請中)
- IEC 62368 CB 認証 (申請中)
- 小型サイズ:2mm × 2mm SON パッケージ

2 アプリケーション

- アダプタの入力保護
- 電力量計
- スマート・スピーカ
- ワイヤレス・イヤフォン充電器
- セット・トップ・ボックス
- IP ネットワーク・カメラ



概略回路図

3 概要

TPS25961 eFuse (FET 内蔵型ホットスワップ・デバイス) は、回路保護および電力管理のソリューションを、小さなパッケージ内で高度に統合しています。このデバイスは、非常に少ない数の外付け部品で複数の保護モードを提供し、過負荷、短絡、電圧サージ、および過剰な突入電流に対して堅牢な保護を行います。出力電流制限レベルは、1 つの外付け抵抗により設定できます。突入電流は、内蔵の出力スルーレート制御機能により管理されます。入力過電圧状態からの保護のため、本デバイスでは固定の内部スレッショルドを使用する他に、ユーザー定義の過電圧カットオフ・スレッショルドを外部で設定するオプションもあります。

これらのデバイスは、-40℃～+125℃の接合部温度範囲で動作が規定されています。

製品情報

部品番号 (1)	パッケージ	本体サイズ (公称)
TPS25961DRV	SON (6)	2.00mm × 2.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2022	*	Initial Release

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5 Pin Configuration and Functions

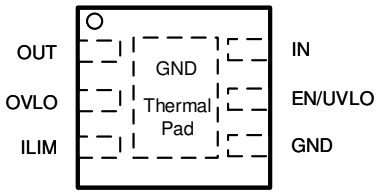


図 5-1. DRV Package, 6-Pin SON (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	Power	Power output.
OVLO	2	Analog Input	An external resistor divider from supply rail can be used to adjust the overvoltage lockout threshold. Connect to GND directly to use internal fixed overvoltage lockout threshold. **Do not leave floating.**
ILIM	3	Analog Output	An external resistor from this pin to GND sets the output current limit threshold. Leave it open to set the current limit threshold to minimum value.
GND	4	Ground	Connect to system electrical ground.
EN/UVLO	5	Analog Input	Active High Enable for the device. A resistor divider from supply rail can be used to adjust the undervoltage lockout threshold. **Do not leave floating.**
IN	6	Power	Power input.
GND	PAD	Thermal/ Ground	The exposed pad is used primarily for heat dissipation and must be connected to GND plane on the PCB.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40℃ ≤ T_J ≤ 125℃	IN	–0.3	21	V
V_{OUT}	Maximum output voltage range, –40℃ ≤ T_J ≤ 125℃	OUT	–0.3	V_{IN} + 0.3	
$V_{EN/UVLO}$	Maximum EN/UVLO pin voltage range	EN/UVLO	–0.3	20	V
V_{OV}	Maximum OVLO pin voltage range	OVLO	–0.3	6.5	V
V_{ILIM}	Maximum ILIM pin voltage range	ILIM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	19	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5(1)	V
V_{OV}	OVLO pin voltage range	OVLO	0.5	1.5	V
R_{ILIM}	ILIM pin resistance to GND	ILIM	25		kΩ
I_{MAX}	Continuous switch current, T_J ≤ 125℃	IN to OUT		2	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

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6.4 Thermal Information

THERMAL METRIC (1) (2)		TPS25961 DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	80.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	16.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p)

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6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 1 V, ILIM = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		130	165	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		144	230	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		0.6	1.5	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.46	2.54	2.61	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.31	2.42	2.54	V
$V_{OVP(R)}$	VIN fixed overvoltage rising threshold, OVLO = GND, T_J = 25°C	5.55	5.98	6.5	V
V_{OVPHys}	VIN fixed overvoltage hysteresis, OVLO = GND	85	111	135	mV
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, ILIM = Open, T_J = 25°C		0.116		A
	Overcurrent threshold, R_{ILIM} = 250 kΩ, T_J = 25°C		0.212		A
	Overcurrent threshold, R_{ILIM} = 100 kΩ, T_J = 25°C		0.516		A
	Overcurrent threshold, R_{ILIM} = 62.5 kΩ, T_J = 25°C		0.856		A
	Overcurrent threshold, R_{ILIM} = 34.48 kΩ, T_J = 25°C	1.189	1.45	1.711	A
	Overcurrent threshold, R_{ILIM} = 25 kΩ, T_J = 25°C		2.36		A
I_{SC}	Fast-trip threshold		8.25		A
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 1 A, R_{ILIM} = 34.48 kΩ		132	240	mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 1 A, R_{ILIM} = 34.48 kΩ		106	177	mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.1 A, R_{ILIM} = 100 kΩ, T_J = 25°C		243		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.1 A, R_{ILIM} = 100 kΩ, T_J = 25°C		195		mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.1 A, R_{ILIM} = 250 kΩ, T_J = 25°C		455		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.1 A, R_{ILIM} = 250 kΩ, T_J = 25°C		367		mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.05 A, ILIM = Open, T_J = 25°C		833		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.05 A, ILIM = Open, T_J = 25°C		702		mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.2	1.24	1.27	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.1	1.132	1.16	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.6			V
I_{ENLKG}	EN/UVLO pin leakage current	-0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO)					
$V_{OVLO(R)}$	OVLO rising threshold	1.2	1.24	1.27	V
$V_{OVLO(F)}$	OVLO falling threshold	1.1	1.13	1.161	V
I_{OVLKG}	OVLO pin leakage current	-0.1		0.1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J ↑		170		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J ↓		30		°C

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6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT} ↓		1.3		µs
t_{LIM}	Current limit response time	I_{OUT} > 1.5 × I_{LIM} to I_{OUT} within 5% of I_{LIM}		30		µs
t_{SC}	Short-circuit response time	I_{OUT} > I_{SC} to output current cut off		5		µs
$t_{TSD,RST}$	Thermal Shutdown auto-retry Interval	Device enabled and T_J < TSD – TSD_{HYS}		110		ms

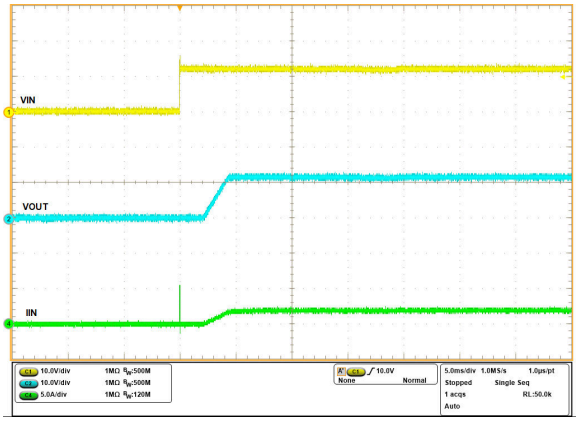
6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

PARAMETER		V_{IN}	Typ	UNITS
SR_{ON}	Output rising slew rate	3.3 V	4.43	V/ms
		12 V	5.17	
		18 V	5.19	
$t_{D,ON}$	Turn on delay	3.3 V	2.14	ms
		12 V	2.37	
		18 V	2.50	
t_R	Rise time	3.3 V	0.58	ms
		12 V	1.83	
		18 V	2.67	
t_{ON}	Turn on time	3.3 V	2.71	ms
		12 V	4.2	
		18 V	5.17	
$t_{D,OFF}$	Turn off delay	3.3 V	15.00	µs
		12 V	14.22	
		18 V	12.44	

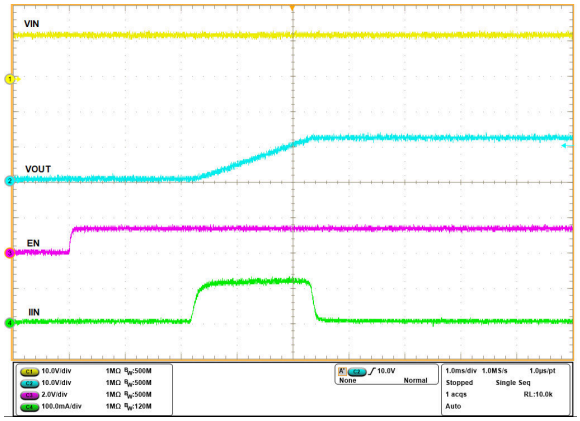
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6.8 代表的特性



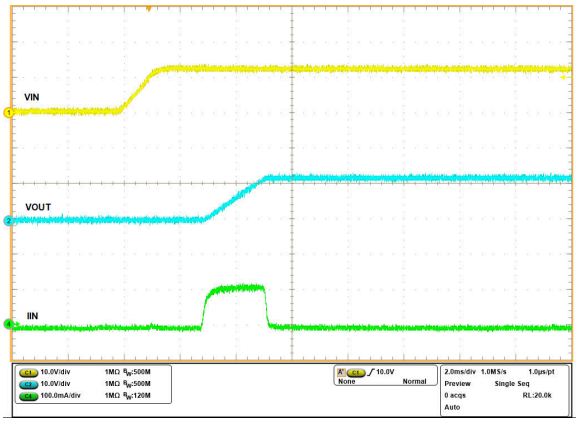
C_{OUT} = 22µF、R_{OUT} = 6Ω、12V への入力ホットプラグ

図 6-1. 入力ホットプラグ応答



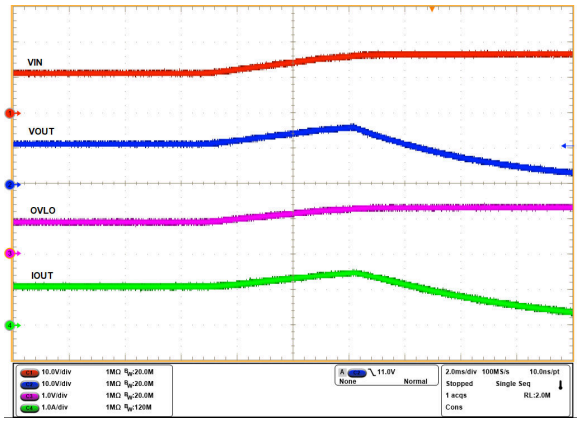
V_{IN} = 12V、C_{OUT} = 22µF、EN ピン電位を 0V から 1.5V に切り替え

図 6-2. イネーブルピンを使用した電源立ち上げ



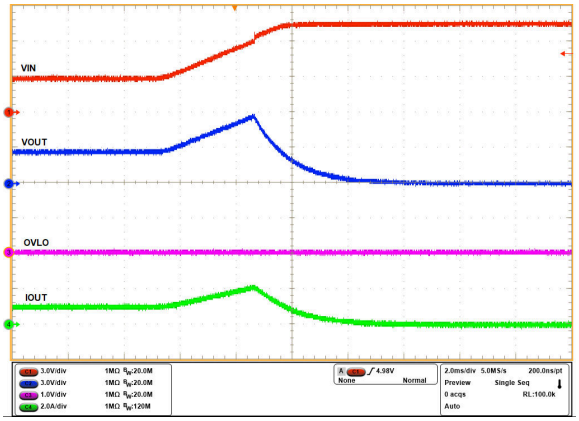
C_{OUT} = 22µF、EN ピンは High に保持、V_{IN} を 12V まで上昇

図 6-3. 入力電源を使用した電源立ち上げ



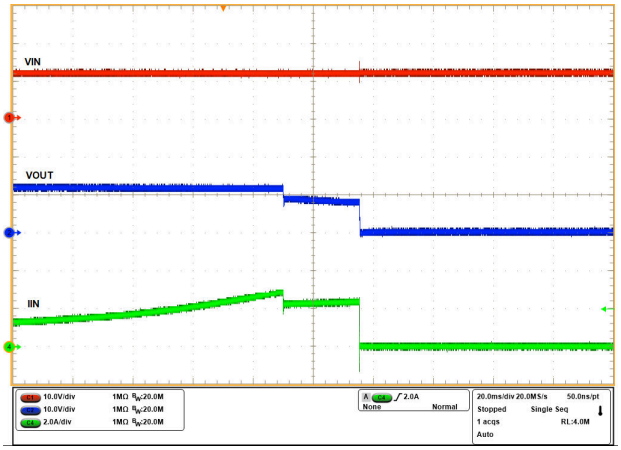
Vin から GND にラダー抵抗を接続し OVLO スレッショルドを 16V に設定、C_{OUT} = 470µF、R_{OUT} = 12Ω、V_{IN} を 10V から 17V まで上昇

図 6-4. 過電圧ロックアウト応答-可変スレッショルド



OVLO ピンを GND に短絡、C_{OUT} = 470µF、R_{OUT} = 3.3Ω、V_{IN} を 2.7V から 7.5V まで上昇

図 6-5. 過電圧ロックアウト応答-内部固定スレッショルド

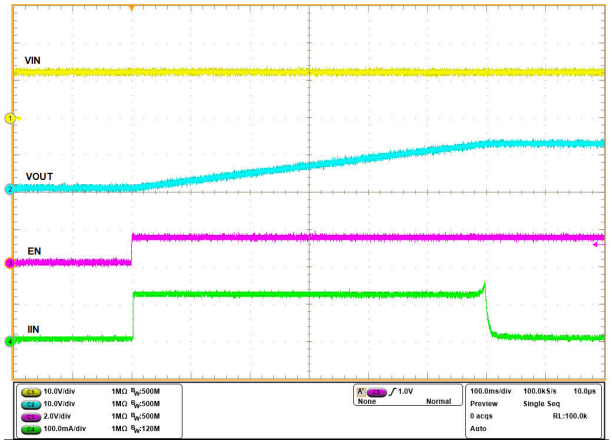


V_{IN} = 12V、R_{ILIM} = 25kΩ、負荷は 2.5A を超えて徐々に上昇中

図 6-6. 電流制限に続くサーマル・シャットダウン

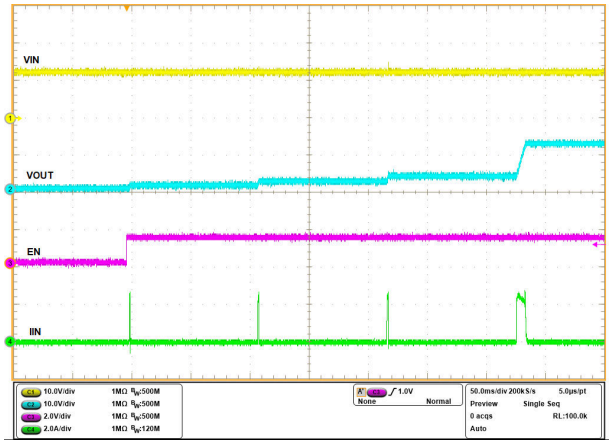
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6.8 代表的特性 (continued)



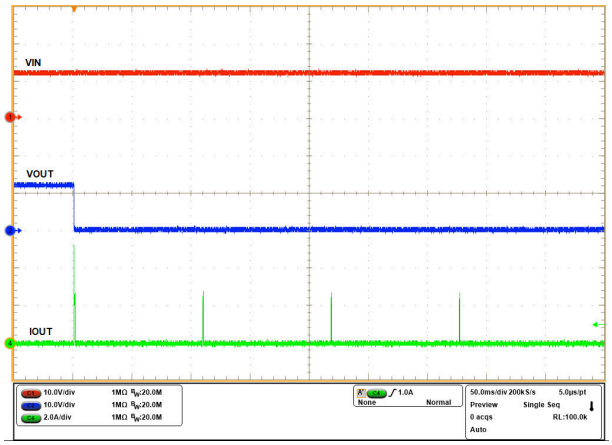
V_{IN} = 12V、C_{OUT} = 6400µF、R_{OUT} = 開放、R_{ILIM} = 開放、EN ピンを Low から High に切り替え

図 6-7. 低電流制限設定を使用した大容量コンデンサの充電



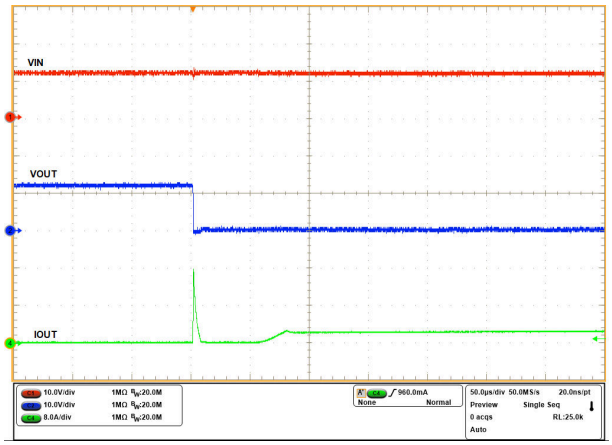
V_{IN} = 12V、C_{OUT} = 2200µF、R_{OUT} = 開放、R_{ILIM} = 25kΩ、EN ピンを Low から High に切り替え

図 6-8. 高電流制限設定を使用した大容量コンデンサの充電-ヒカップ・モード



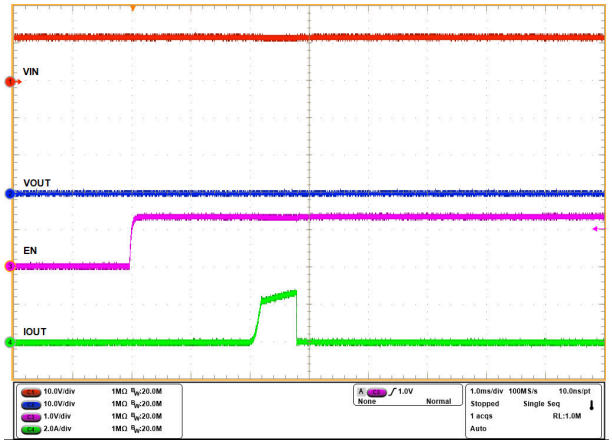
V_{IN} = 12V、R_{ILM} = 25kΩ、OUT ピンを GND に短絡

図 6-9. オン時の出力短絡



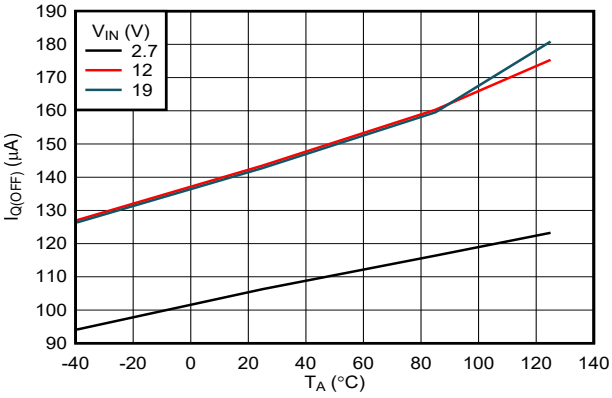
V_{IN} = 12V、R_{ILM} = 25kΩ、OUT ピンを GND に短絡

図 6-10. オン時の短絡 （拡大図）



V_{IN} = 12V、R_{ILM} = 25kΩ、OUT ピンを GND に短絡した状態で EN ピンを Low から High に切り替え

図 6-11. 短絡時の電源立ち上げ

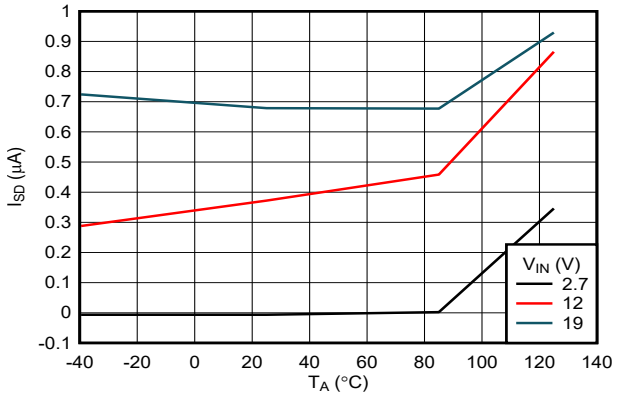


EN/UVLO ピン電圧 > $V_{UVLO(R)}$

図 6-12. 定常状態での静止電流と温度との関係

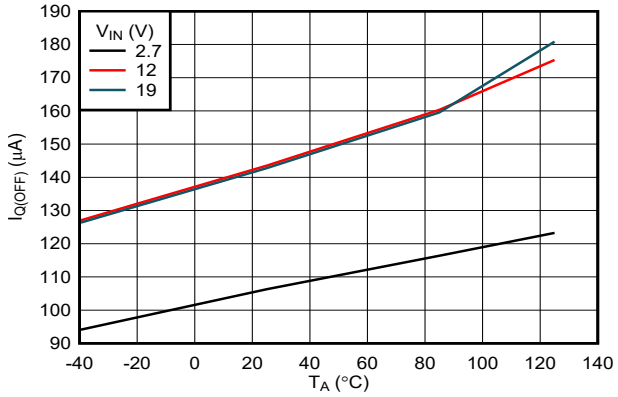
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6.8 代表的特性 (continued)



EN/UVLO ピン電圧 < $V_{SD(F)}$

図 6-13. シャットダウン電流と温度との関係



$V_{SD(F)}$ < EN/UVLO ピン電圧 < $V_{UVLO(F)}$

図 6-14. オフ状態電流と温度との関係

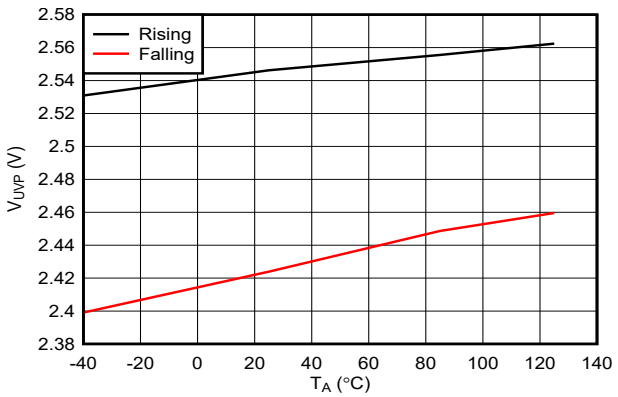


図 6-15. 電源入力の低電圧スレッショルドと温度との関係

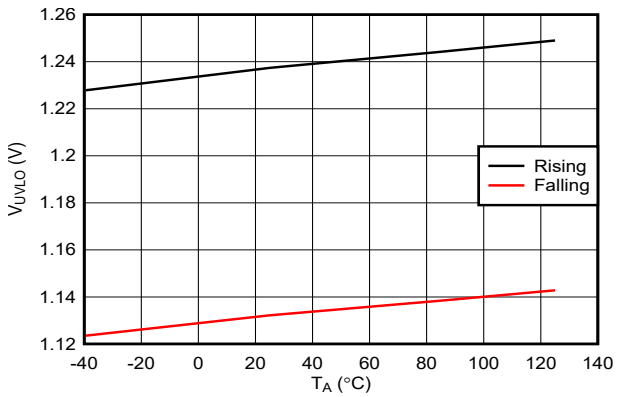


図 6-16. FET オン/オフ制御の EN/UVLO ピン・スレッショルドと温度との関係

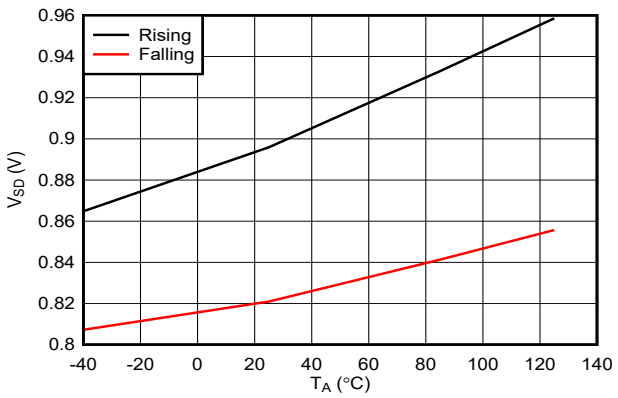


図 6-17. 最小シャットダウン電流のための EN/UVLO ピンのスレッショルドと温度との関係

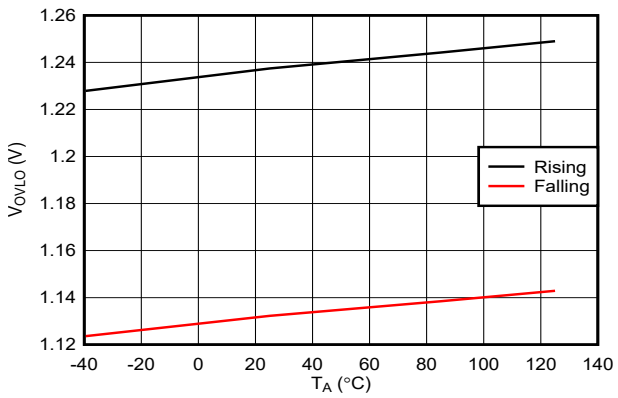


図 6-18. OVLO ピン・スレッショルドと温度との関係

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6.8 代表的特性 (continued)

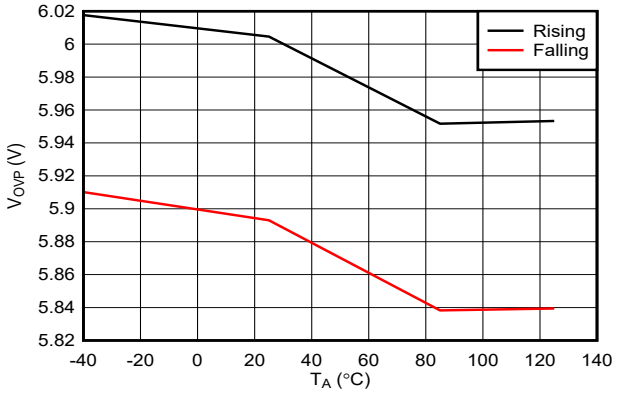
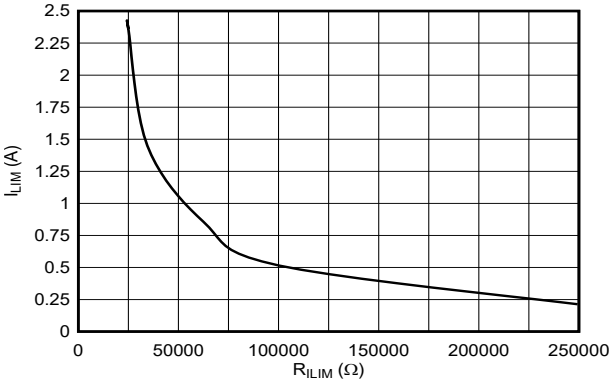
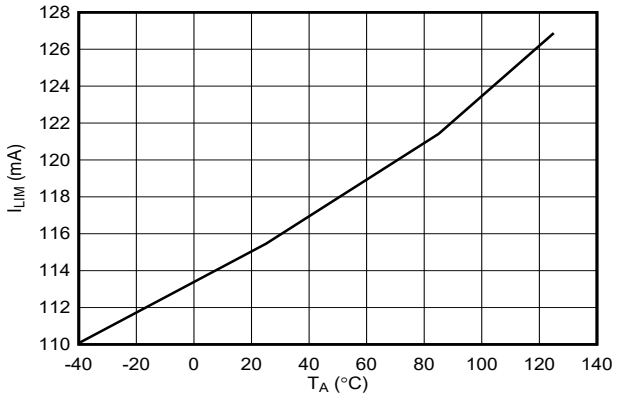


図 6-19. 内部固定の過電圧スレッショルドと温度との関係



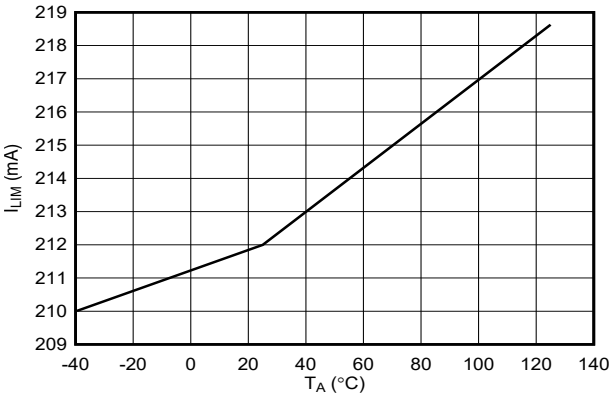
I_{LIM} > 0.2A の場合に適用が可能 、その他の考慮事項については、このセクションを参照してください。

図 6-20. 電流制限スレッショルドと ILIM 抵抗との関係



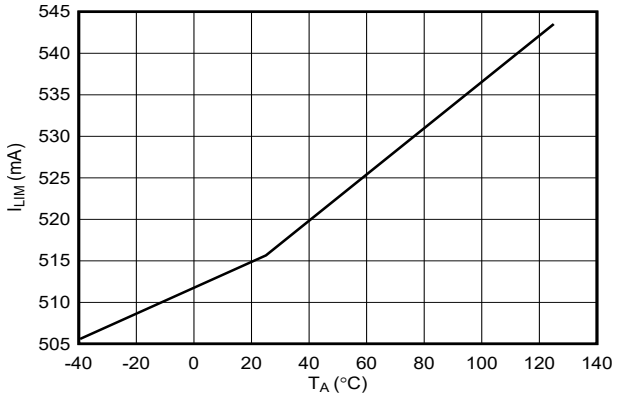
ILIM ピンは開放

図 6-21. 電流制限スレッショルドと温度との関係



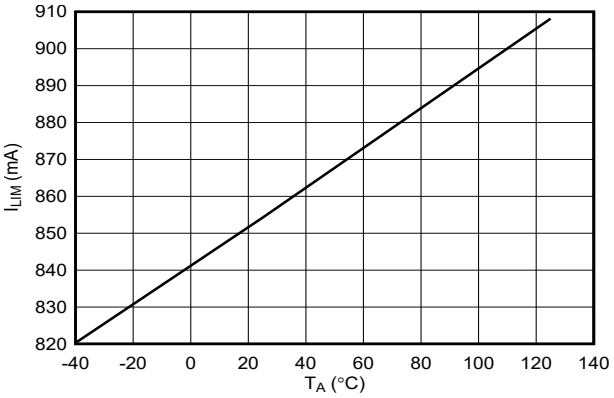
R_{ILIM} = 250kΩ

図 6-22. 電流制限スレッショルドと温度との関係



R_{ILIM} = 100kΩ

図 6-23. 電流制限スレッショルドと温度との関係

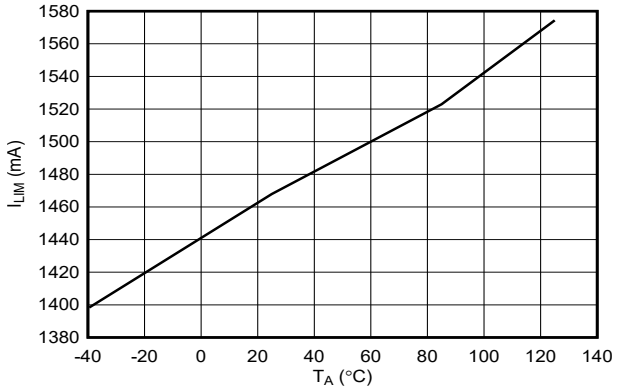


R_{ILIM} = 62.5kΩ

図 6-24. 電流制限スレッショルドと温度との関係

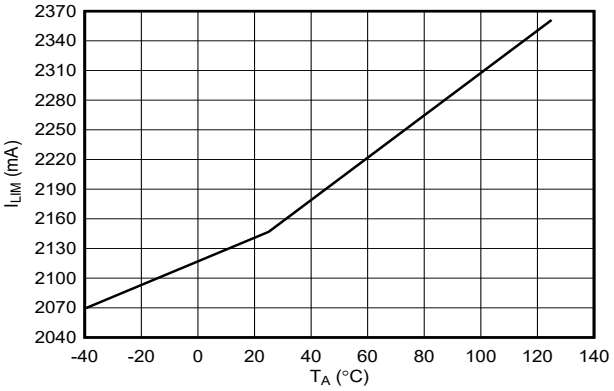
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6.8 代表的特性 (continued)



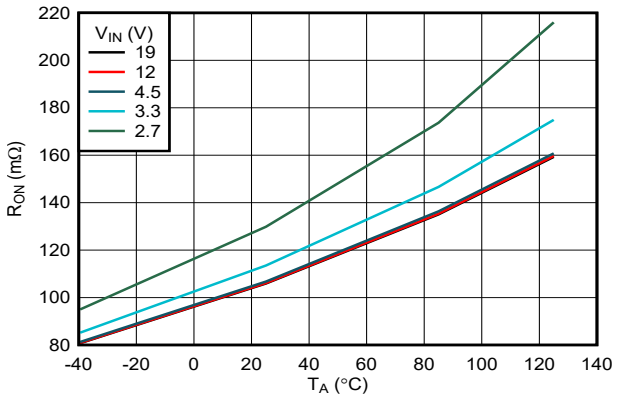
R_{ILIM} = 34.48kΩ

図 6-25. 電流制限スレッショルドと温度との関係



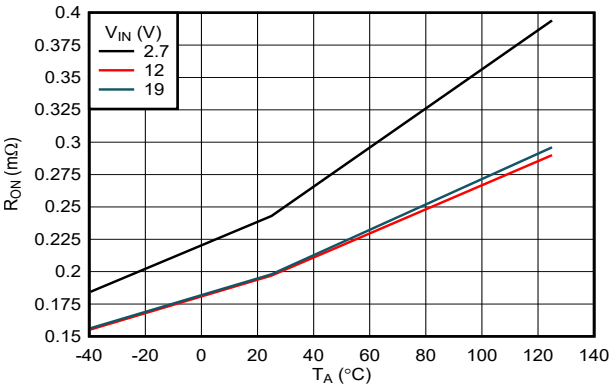
R_{ILIM} = 25kΩ

図 6-26. 電流制限スレッショルドと温度との関係



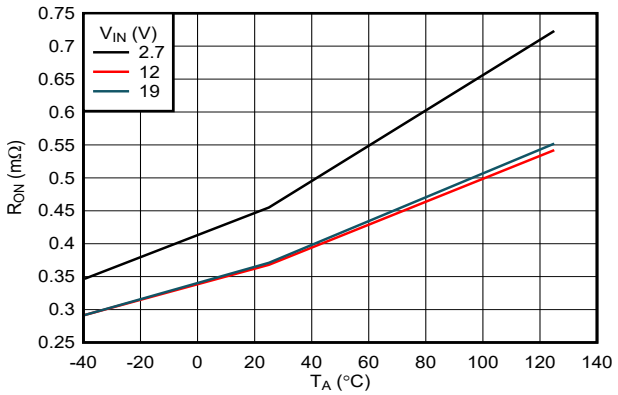
R_{ILIM} < 58.8kΩ

図 6-27. オン抵抗と温度との関係



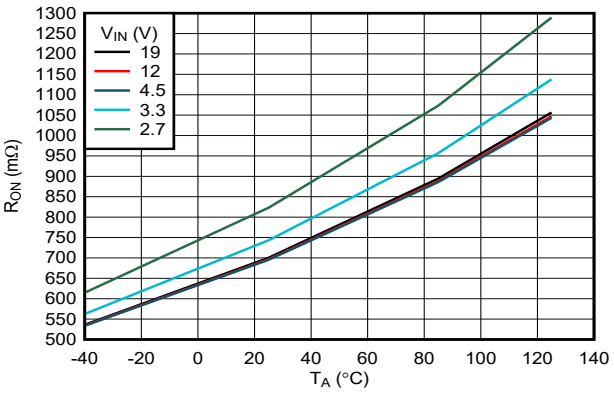
66.7kΩ < R_{ILIM} < 111kΩ

図 6-28. オン抵抗と温度との関係



142kΩ < R_{ILIM} < 250kΩ

図 6-29. オン抵抗と温度との関係



R_{ILIM} > 500kΩ

図 6-30. オン抵抗と温度との関係

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6.8 代表的特性 (continued)

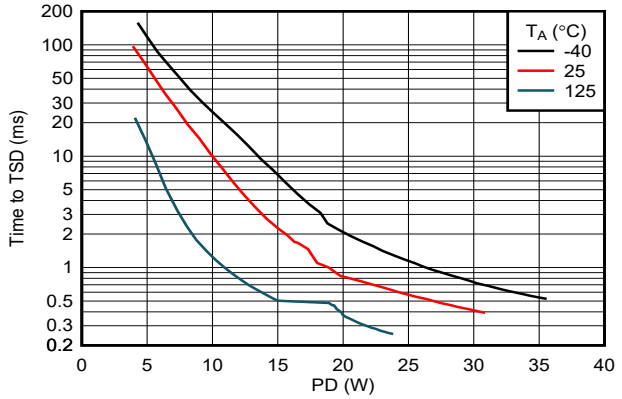


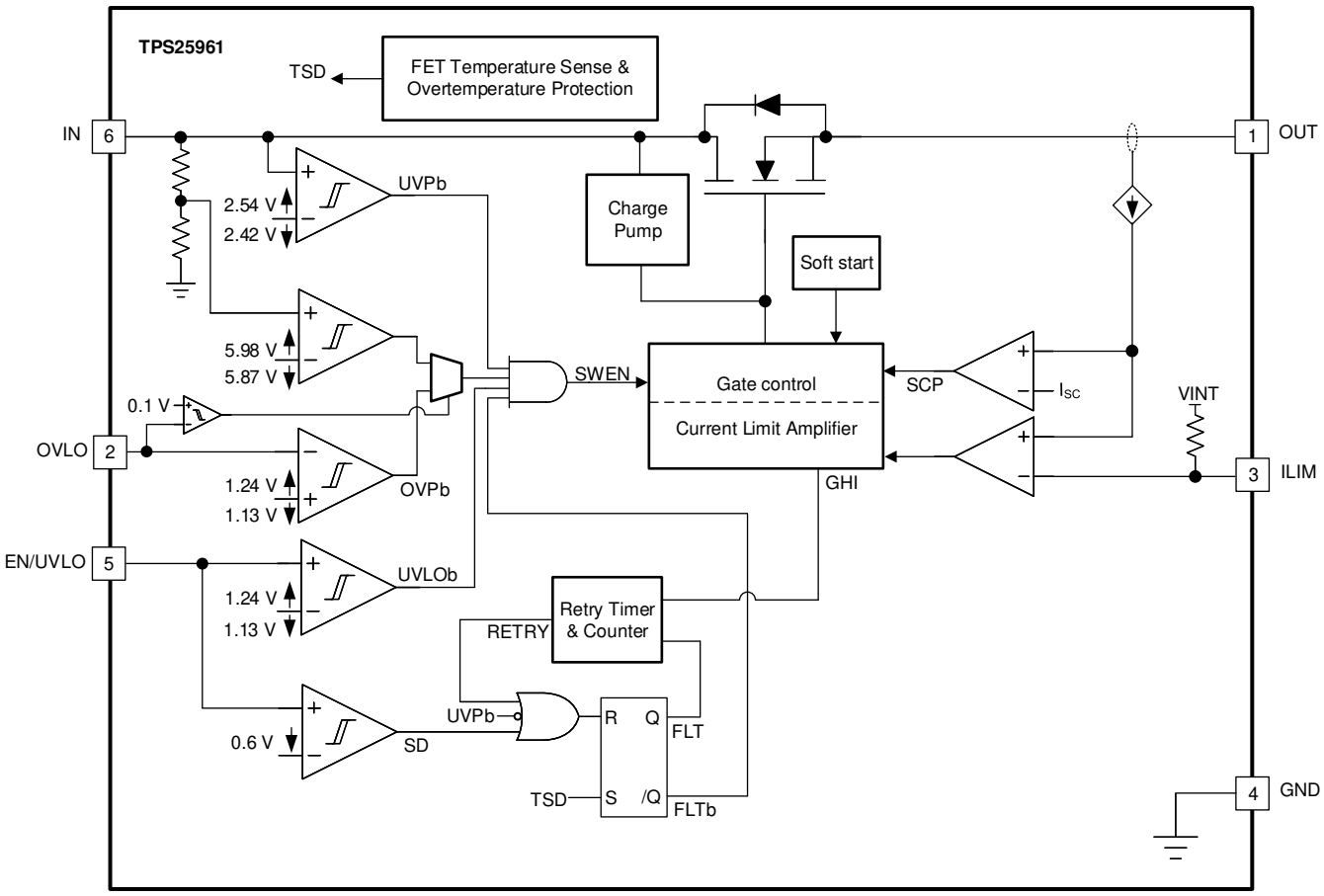
図 6-31. サーマル・シャットダウンまでの時間と消費電力との関係

7 Detailed Description

7.1 Overview

The TPS25961 is an integrated eFuse device that is used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 過電圧保護 (UVP) および低電圧ロックアウト (UVLO)

TPS25961 は入力電源を継続的に監視し、電圧が十分なレベルにある場合にのみ、負荷に対し電源を供給します。スタートアップ状態では、デバイスは入力電源が内部の固定スレッショルド $V_{UVP(R)}$ を上回るまで待機してから、FET をオンにします。同様に、オン状態で入力電源が UVP スレッショルド $V_{UVP(F)}$ を下回った場合は、FET がオフされます。UVP の立ち上がりスレッショルドと立ち下がりスレッショルドはわずかに異なるため、ある程度のヒステリシスが発生し、スレッショルド電圧付近で安定した動作が保証されます。

また、TPS25961 にはユーザー調整可能な UVLO メカニズムも搭載されており、特定のシステム要件に従って、電圧が十分なレベルにあるときのみ負荷に電源を供給できます。これは、入力電源電圧を分圧し EN/UVLO ピンに供給することで実現できます。EN/UVLO ピンの電圧がスレッショルド $V_{UVLO(F)}$ を下回ると、デバイスは FET をオフにします。この電圧がスレッショルド $V_{UVLO(R)}$ を上回ると、FET は再度オンになります。このピンの、立ち上がりスレッショルドと立ち下がりスレッショルドはわずかに異なっているため、ある程度のヒステリシスが得られ、スレッショルド電圧付近で安定した動作が保証されます。

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ユーザーは、目的の入力低電圧レベルをこの UVLO スレッショルドにマッピングするために、分圧抵抗の値を適切に選択する必要があります。

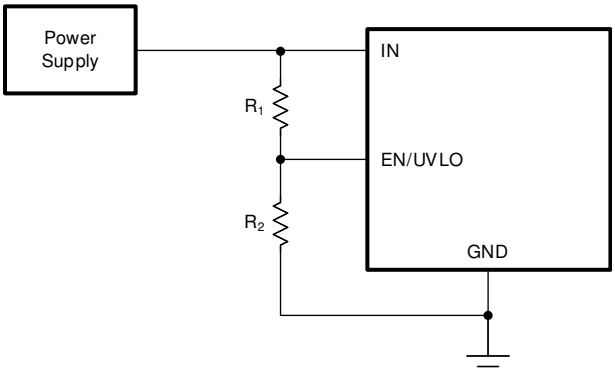


図 7-1. 可変の低電圧ロックアウト

以下の式で、与えられた電源電圧に対して UVLO 設定ポイントを設定するための分圧抵抗値の計算を示します。

$$VIN\ (UV)\ = VUVLO\ (F) \times \frac{R1 + R2}{R2} \quad (1)$$

7.3.2 Overvoltage Protection

The TPS25961 implements Overvoltage Protection on V_{IN} in case the applied voltage becomes too high for the system or device to properly operate. The Overvoltage Protection has a default lockout threshold of V_{OVP} , which is achieved by connecting the OVLO pin to GND.

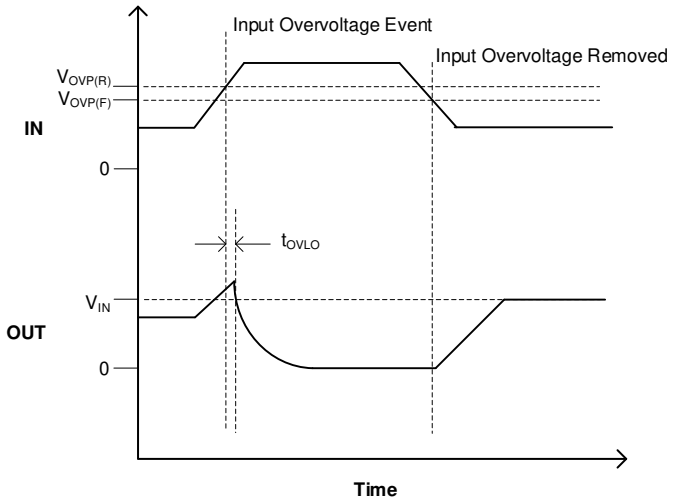


図 7-2. TPS25961 Fixed Overvoltage Lockout Response

It’s possible to override the default OVLO threshold and adjust it to an user defined value as per the system requirements. This can be achieved by dividing the input supply and feeding it to the OVLO pin. Whenever the voltage at the OVLO pin rises above a threshold $V_{OVLO(R)}$, the device turns OFF the FET. When the voltage at the OVLO pin falls below the threshold $V_{OVLO(F)}$, the FET is turned ON again. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

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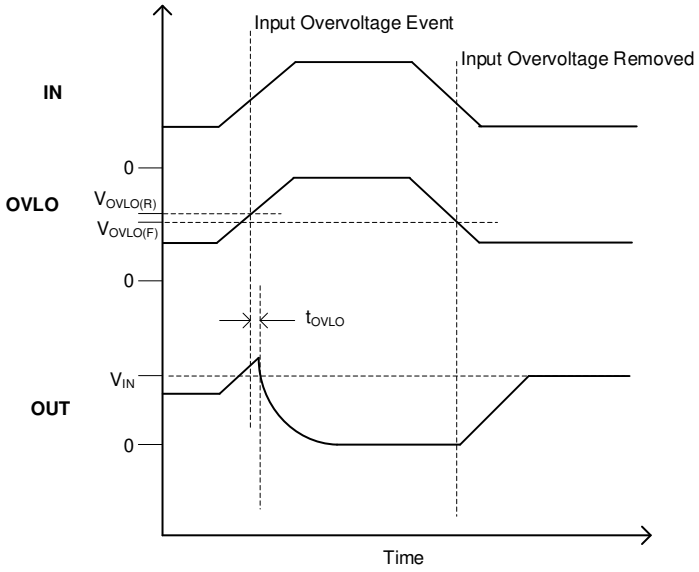


図 7-3. TPS25961 Adjustable Overvoltage Lockout Response

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

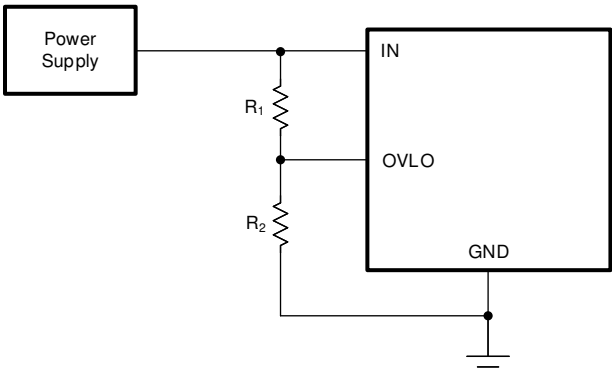


図 7-4. TPS25961 Adjustable Overvoltage Lockout

The equation below shows the calculations for the resistor divider values to be used to set the OVLO set-point for a given voltage supply.

$$\mathrm{VIN(OV)} = \mathrm{VOVLO(F)} \times \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}} \quad (2)$$

7.3.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS25961 incorporates three levels of protection against overcurrent:

- Fixed slew rate for inrush current control (dVdt)
- Active current limiting with adjustable limit (I_{LIM}) for overcurrent protection
- Fast short-circuit response to protect against hard short-circuits

7.3.3.1 Slew Rate and Inrush Current Control (dVdt)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate.

$$\mathrm{IINRUSH} = \mathrm{COUT} \times \mathrm{SRON} \quad (3)$$

TPS25961 provides a controlled turn on at a fixed slew rate (SR_{ON}) which helps to minimize the inrush current.

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7.3.3.2 Active Current Limiting

The device responds to output overcurrent conditions by actively limiting the current.

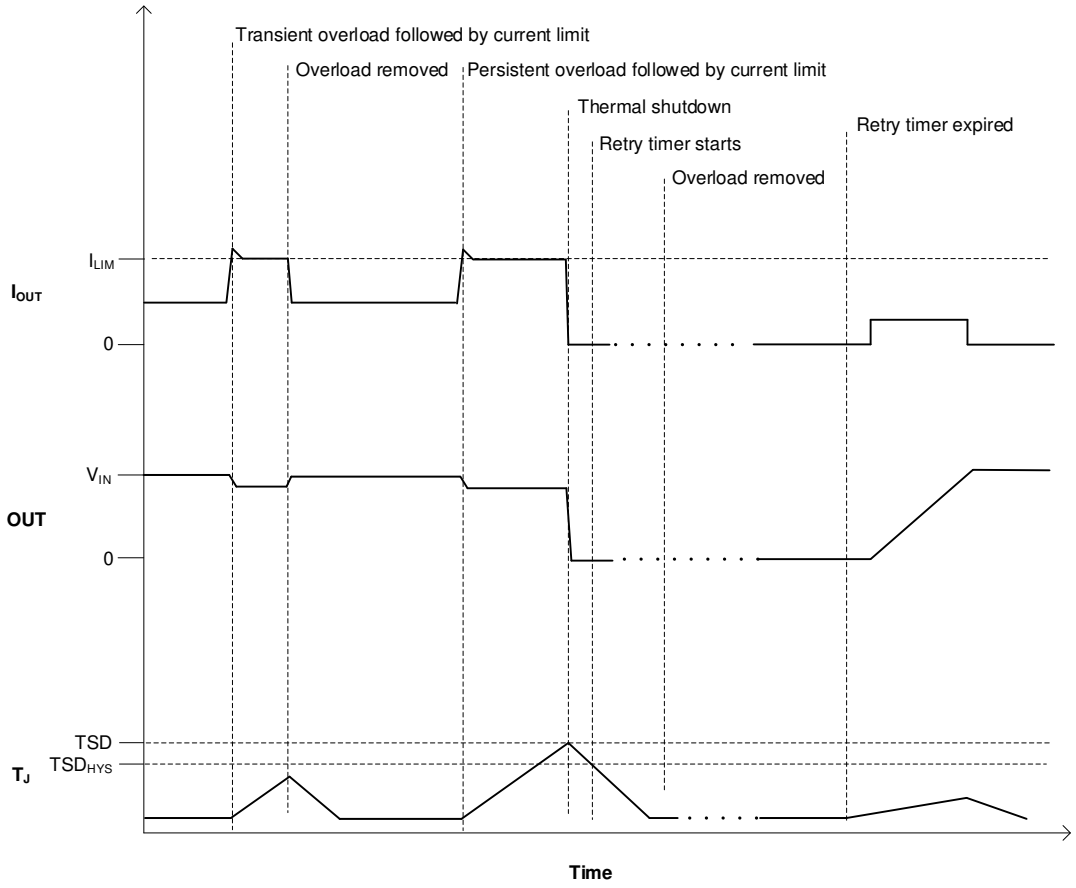


図 7-5. TPS25961 Overcurrent Response

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to thermal shutdown if the condition persists for an extended period of time. In this case, the device performs 3 auto-retry attempts to allow the system to recover and then latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

The current limit threshold can be adjusted by pinstrapping the ILIM pin.

Use equation below to calculate the R_{ILIM} value for overcurrent thresholds < 200 mA.

$$\mathrm{RILIM} = \frac{50000}{\mathrm{ILIM} - 0.000002} \tag{4}$$

Use equation below to calculate the R_{ILIM} value for overcurrent thresholds ≥ 200 mA.

$$\mathrm{RILIM} = \frac{50000}{\mathrm{ILIM}} \tag{5}$$

注

1. Leaving the ILIM pin open sets the current limit to its minimum value.
2. The device scales the FET ON resistance in discrete steps according to the R_{ILIM} setting to provide optimum performance for the desired current level. At higher I_{LIM} settings, the ON resistance is lower and at lower I_{LIM} settings, the ON resistance is higher. However, for certain R_{ILIM} resistor values, the device may select an incorrect ON resistance scaling which is too high for the target load current leading to excessive voltage drop and power dissipation. To avoid this situation, it's recommended to avoid certain R_{ILIM} values as per 表 7-1.

表 7-1. R_{ILIM} Values to Avoid

ILIM Resistor Value	Device ON Resistance
250 kΩ < R_{ILIM} < 500 kΩ	Undefined
111 kΩ < R_{ILIM} < 142 kΩ	Undefined
58.8 kΩ < R_{ILIM} < 66.7 kΩ	Undefined

7.3.3.3 Short-Circuit Protection

The current through the device increases very rapidly during an output short-circuit event. In this event, the device engages a fast current clamping circuit to regulate down the current faster (t_{SCP}) as compared to the nominal overcurrent response time (t_{LIM}). Instead of completely turning off the power FET, the device tries to actively limit the current to ensure uninterrupted power in the event of transient overcurrents or supply transients. The device stops limiting the current once the load current falls below the programmed I_{LIM} threshold.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and might lead to thermal shutdown if the condition persists for an extended period of time. In this case, the device performs 3 auto-retry attempts to allow the system to recover and then latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

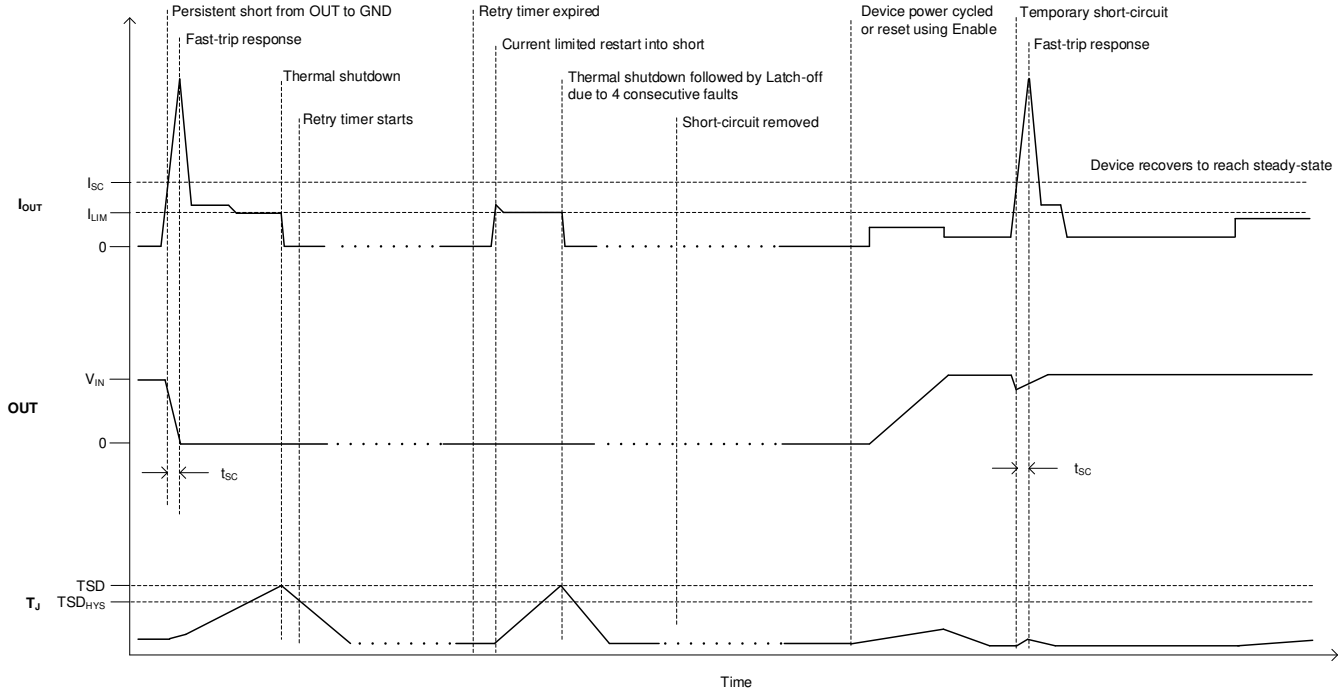


図 7-6. TPS25961 Short Circuit Response

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7.3.4 Overtemperature Protection (OTP)

Thermal Shutdown occurs when the junction temperature (T_J) exceeds the thermal shutdown threshold (TSD). When the TPS25961 detects thermal overload, it shut downs and remains off until it has cooled down sufficiently. Once the TPS25961 junction has cooled down below TSD - TSD_{HYS}, it remains off for an additional delay of $t_{TSD,RST}$ after which it automatically retries to turn on. The device performs 3 auto-retry attempts to allow the system to recover before it latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

表 7-2. TPS25961 Thermal Shutdown

Enter TSD	Exit TSD
$T_J \geq$ TSD	$T_J <$ TSD - TSD_{HYS} and $t_{TSD,RST}$ timer expired

7.3.5 Fault Response

表 7-3 summarizes the protection response to various fault conditions.

表 7-3. Fault Response

Event / Fault	Protection Response	Fault Latched Internally
Steady-state	N/A	N/A
Overtemperature	Shutdown	Yes
Undervoltage	Cut-off	No
Overvoltage	Cut-off	No
Overcurrent	Current Limit	No
Short-circuit	Current Limit	No

Once the device turns off due to a latched fault, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault. Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition.

At the end of the $t_{TSD,RST}$ timer after a latched fault, the device will attempt to automatically restart 3 times. If the fault was caused by a transient condition which goes away and the device is able to recover and reach steady state, it clears the fault counter.

If the fault is persistent, the device will eventually shut down completely after 3 attempts and then remain latched-off till it's power cycled.

7.4 Device Functional Modes

The features of the device depend on the operating mode.

表 7-4. Overvoltage protection modes

OVLO pin	OVLO threshold
< 0.1 V or connected to GND	Fixed 5.98 V
Resistor ladder from IN	Adjustable

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25961 device is an integrated eFuse that is typically used for input hot-swap and power rail protection applications for systems such as energy meters, set-top boxes, building automation and adapter input protection. The device operates from 2.7-V to 19-V with adjustable current limit, overvoltage and undervoltage protection. The device aids in controlling the inrush current and provides current limiting during overload conditions.

The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, TPS25961 Design Calculator, is available in the web product folder.

8.2 代表的なアプリケーション

8.2.1 Adapter input protection for set-top boxes

TPS25961 can be used for input power protection in set-top boxes. Operating voltage is generally around 12-V and can vary from 10-V to 14-V. During event like input voltage overshoot, TPS25961 overvoltage protection acts to cut off the path and protect downstream load from overvoltage. Also inrush current control and configurable current limit feature helps in preventing power supply from collapsing during events like hotplug and overload.

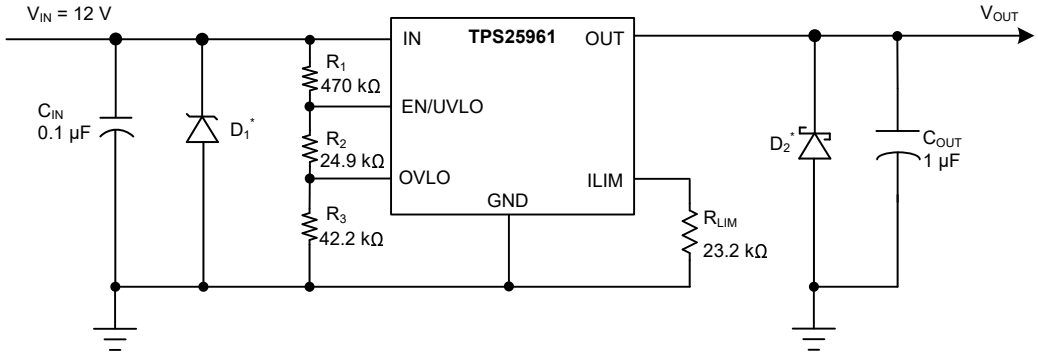


図 8-1. Typical Application Schematic

* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to Transient Protection section for details.

8.2.2 Design Requirements

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage , V_{IN}	12 V
Undervoltage lockout set point, V_{UV}	9 V
Overvoltage protection set point , V_{OV}	15.5 V
Current limit, I_{LIM}	2 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperature, T_A	85°C

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8.2.3 Detailed Design Procedure

8.2.3.1 Programming the Current-Limit Threshold: R_{ILM} Selection

The R_{ILM} resistor at the ILM pin sets the over load current limit. Since required current limit of 2 A is greater than 200 mA, below 式 6 for current limit can be used for calculating R_{ILIM}.

$$\text{RILIM} = \frac{50000}{\text{ILIM}} \tag{6}$$

Closest standard value resistor is 25.5 kΩ with 1% tolerance. It is recommended that final R_{ILM} selected does not lie in the ranges mentioned in 表 7-1. Final value of 25.5 kΩ does not lie in those non-recommended ranges and is fine to use in design.

8.2.3.2 低電圧および過電圧ロックアウトの設定点

電源の低電圧および過電圧スレッショルドは、抵抗 R1、R2、R3 を使用して設定します。これらの値は、式 10 および式 11 を使用して計算できます。

$$\text{VIN (UV)} = \frac{\text{VUVLO(R)} \times (\text{R1} + \text{R2} + \text{R3})}{\text{R2} + \text{R3}} \tag{7}$$

$$\text{VIN (OV)} = \frac{\text{VOVLO (R) X (R1} + \text{R2} + \text{R3)}}{\text{R3}} \tag{8}$$

ここで、$V_{UVLO(R)}$ は EN/UVLO ピンの立ち上がりスレッショルド、$V_{OVLO(R)}$ は OVLO ピンの立ち上がりスレッショルドです。R1、R2、R3 は入力電源 VIN から電流をリークするため、VIN におけるリーク電流の許容範囲を考慮して、これらの抵抗を選択する必要があります。電源から R1、R2、R3 によって引き出される電流は、IR123 = VIN/ (R1 + R2 + R3) です。ただし、この抵抗列に外部のアクティブ部品が接続されたことによるリーク電流は、これらの計算に誤差を生じさせる可能性があります。したがって、抵抗列電流 = IR123 は、EN/UVLO および OVLO ピンで予測されるリーク電流の 20 倍になるよう選択する必要があります。デバイスの電気的仕様から、EN/UVLO と OVLO の両方のリーク電流は 0.1µA (最大値)、$V_{OVLO(R)}$ = 1.24V、$V_{UVLO(R)}$ = 1.24V です。設計要件から、VIN (OV)= 15.5V、VIN (UV)= 9V となります。最初に R1 = 470kΩ の値を選択すると、上記の式を使用して R2 = 31.5kΩ および R3 = 43.6kΩ が算出されます。標準の 1% 抵抗で最も近い値を使用すると、R1 = 470kΩ、R2 = 31.6kΩ、R3 = 44.2kΩ となります。

8.2.3.3 Output Voltage Rise Time (tR)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to to determine that power dissipation is below a certain limit to avoid thermal shutdown during start-up.

Slew rate is 5 V/ms typically for TPS25961. The inrush current can be calculated as:

$$\text{IINRUSH (mA)} = \text{SR (V/ms) x COUT (µF)} = 5 \text{ x } 1 = 5 \text{ mA} \tag{9}$$

The average power dissipation inside the part during inrush can be calculated as:

$$\text{PDINRUSH (W)} = \frac{\text{IINRUSH (A) x VIN (V)}}{2} = \frac{0.005 \text{ x } 12}{2} = 0.03 \text{ W} \tag{10}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 図 8-2 shows the thermal shutdown limit, for 0.03 W of power, the shutdown time is very large as compared to t_R = 2.4 ms. Therefore this application will have successful startup.

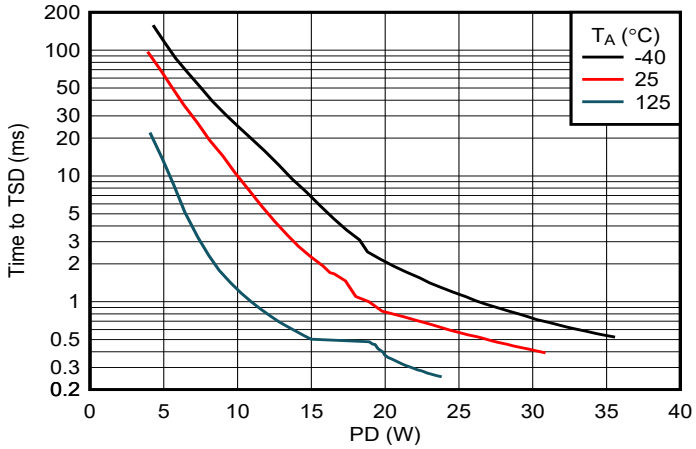


図 8-2. Time to Thermal Shutdown vs Power Dissipation

8.2.4 Application Curves

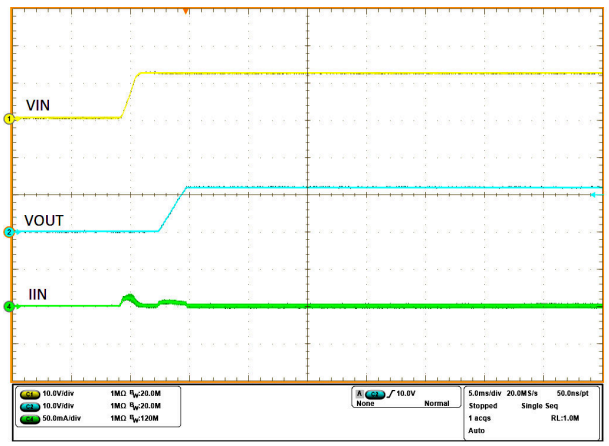


図 8-3. Output Ramp

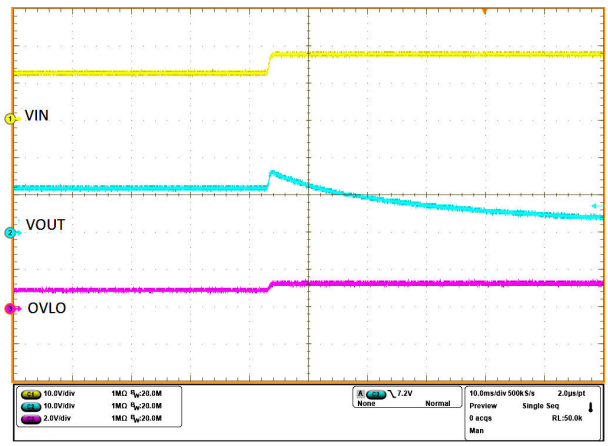


図 8-4. Overvoltage Protection (OVLO)

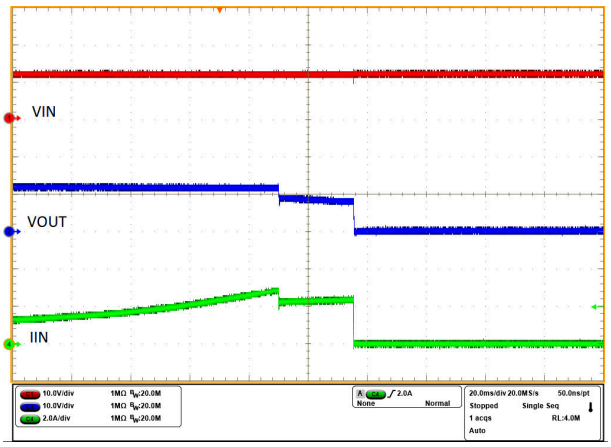


図 8-5. Overcurrent Protection

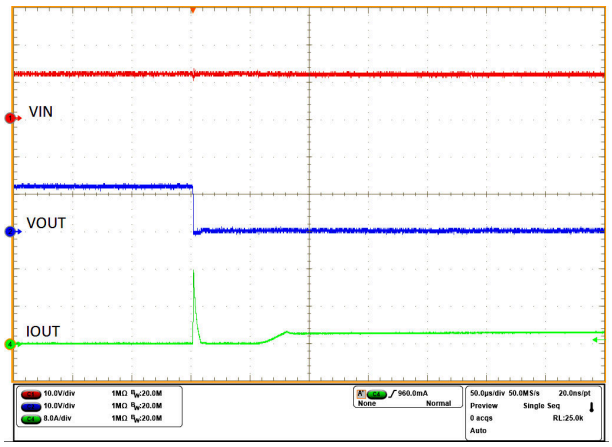


図 8-6. Short at Output Protection

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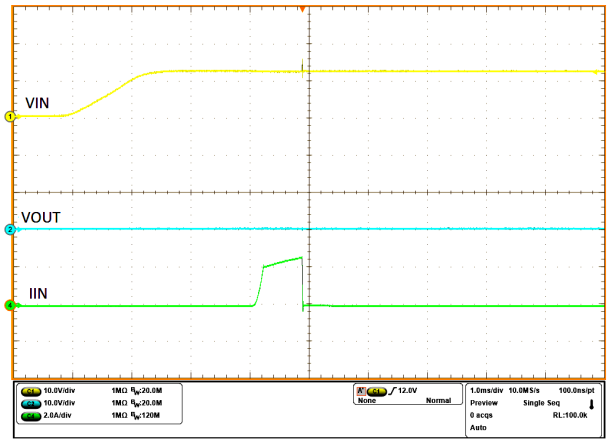


図 8-7. Wakeup in Short Protection

8.3 Application Example

TPS25961 can also be used as a low cost current limiter device replacing discrete PTC for memory card port protection in end equipments like IP camera, Laptop etc. Typical SD cards operate at 3.3-V and draw current less than 100 mA. TPS25961 can be configured for protection in this application without the need for many external components. Keeping OVLO pin grounded and ILIM pin open would set fixed overvoltage protection thresold of 5.98 V and current limit of 115 mA. EN pin can be tied to VIN pin through a pullup resistor. 図 8-9 shows example layout for TPS25961 for above mentioned configuration, achieved on a single layer board with minimum components.

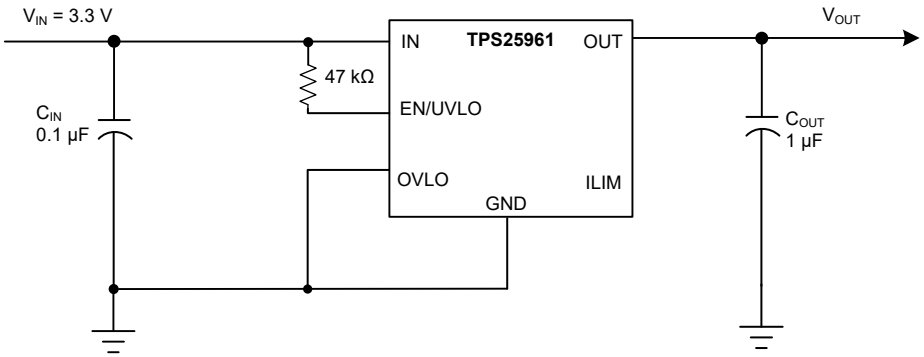


図 8-8. SD card port protection using TPS25961

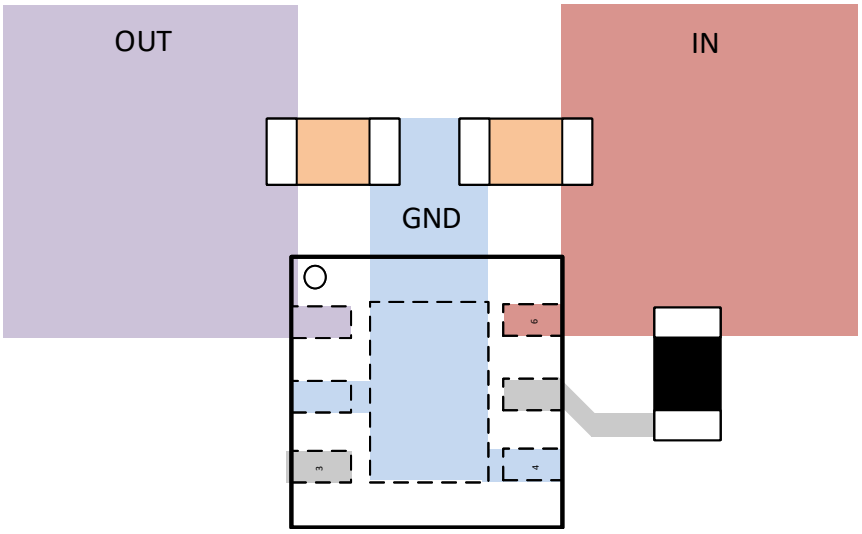


図 8-9. TPS25961 layout example for SD card port protection application

8.3.1 Application Curves

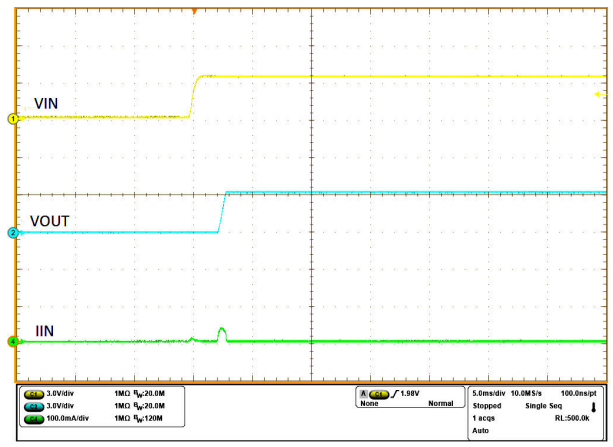


図 8-10. Output Ramp

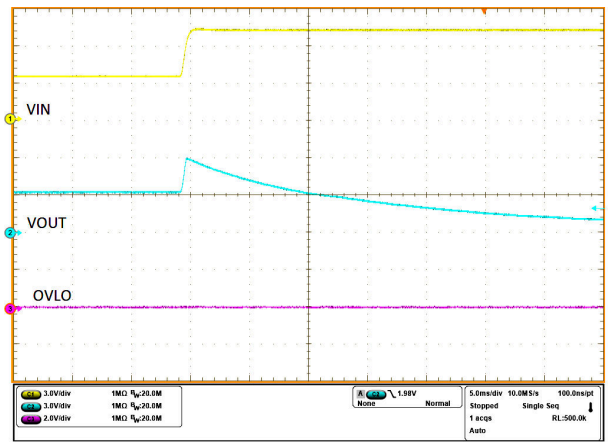


図 8-11. Overvoltage protection

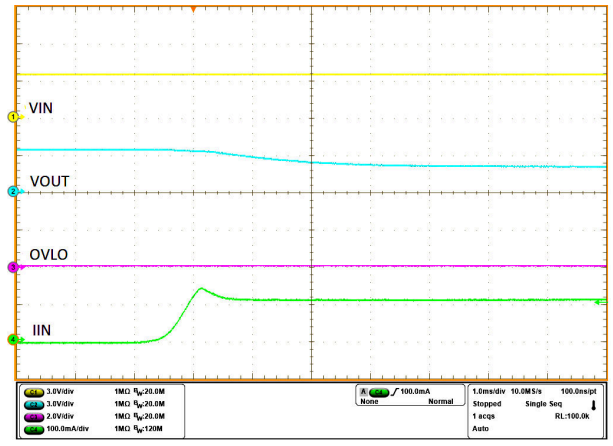


図 8-12. Overcurrent Protection

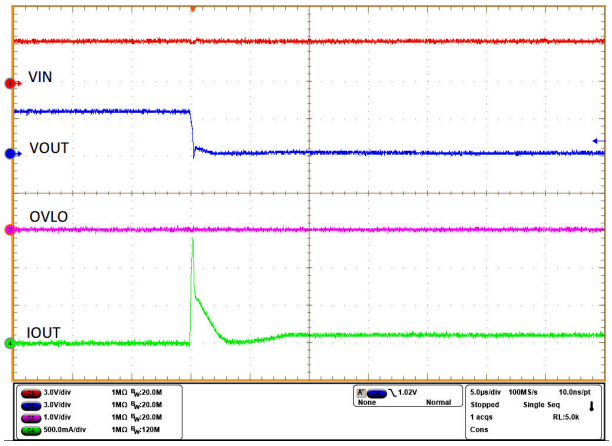


図 8-13. Short at Output Protection

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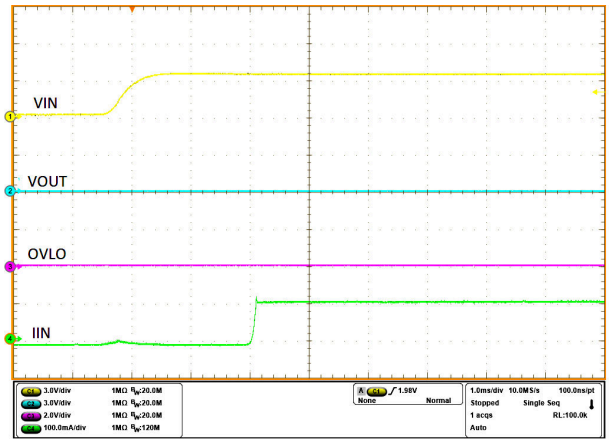


図 8-14. Wake up into Short Protection

8.4 Power Supply Recommendations

The TPS25961 devices are designed for a supply voltage range of 2.7-V ≤ V_{IN} ≤ 19-V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.4.1 過渡保護

デバイスが電流フローに割り込むタイミングで、短絡および過負荷電流による制限が発生した場合、入力インダクタンスによって入力に正の電圧スパイクが生成され、出力インダクタンスによって出力に負の電圧スパイクが生成されます。電圧スパイク (過渡現象) のピーク振幅は、デバイスの入力または出力に存在する直列インダクタンスの値に依存します。この問題に何等かの策を講じない場合は、上記の過渡現象によって、デバイスの絶対最大定格を超える可能性があります。過渡現象に対処する一般的な方法は、以下のとおりです。

- デバイスの入出力において、リード長を短くしインダクタンスを最小限に抑えます。
- PCB には、大きい GND プレーンを使用します。
- 出力の両極間にショットキー・ダイオードを配置して、負のスパイクを吸収します。
- 低値のセラミック・コンデンサ (C_{IN} = 0.1µF) を使用して、エネルギーを吸収し、過渡現象を減衰させます。入力容量の近似値は、次の式を使用して推定できます。

$$\text{VSPIKE (絶対値)} = \text{VIN} + \text{ILOAD} \times \sqrt{\frac{\text{LIN}}{\text{CIN}}} \quad (11)$$

ここで

- V_{IN} は公称電源電圧
- I_{LOAD} は負荷電流
- L_{IN} はソースから見た実効インダクタンスに等しい値
- C_{IN} は入力に存在する容量

注

注：電気的高速過渡状態 (EFT) への耐性に関する IEC 61000-4-4 試験に合格する必要があるシステムでは、EFT バースト中に TPS25961 がオフになることを防止するため、最小の C_{IN} (2.2µF) を使用する必要があります。

一部のアプリケーションでは、過渡状態においてデバイスの絶対最大定格を超えないように、過渡電圧サプレッサ (TVS) を追加する必要があります。オプションの保護部品 (セラミック・コンデンサ、TVS、ショットキー・ダイオード) を使用した回路実装例を、「図 8-15」に示します。

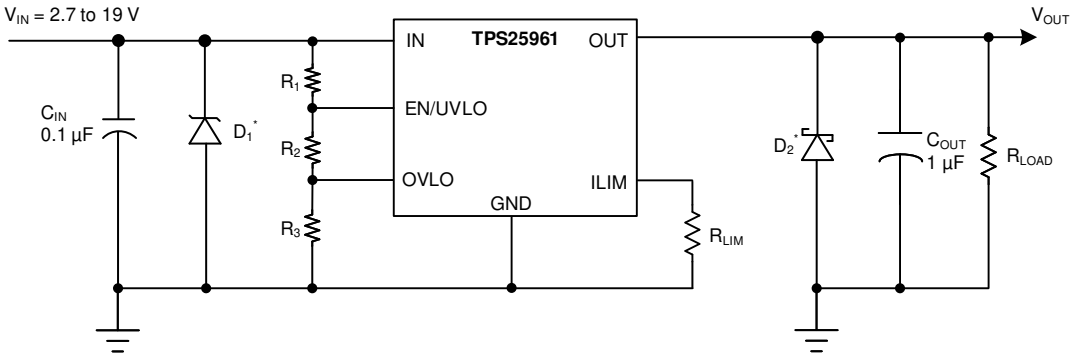


図 8-15. オプションの保護部品を使用した回路実装

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8.4.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.5 Layout

8.5.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate the following support components close to their connection pins:
  - R_{ILIM}
  - Resistor network for the EN/UVLO pin
  - Resistor network for the OVLO pin

  Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing from the components to the device pins must be as short as possible to reduce parasitic effects on the current limit and overvoltage response. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible. The example shown in セクション 8.5.2 has been shown to produce good results and is intended as a guideline.

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8.5.2 Layout Example

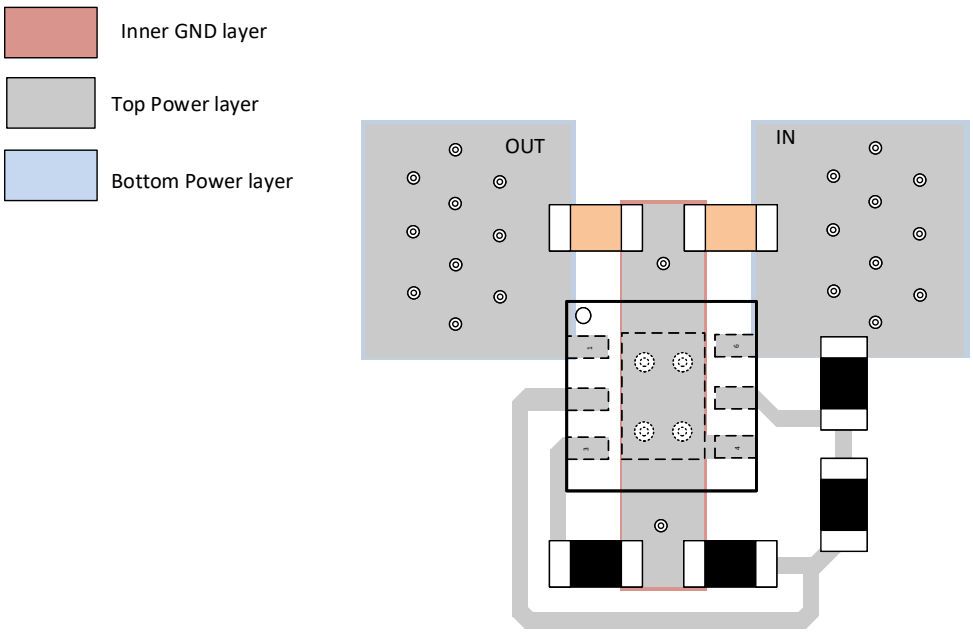


図 8-16. TPS25961 Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- TPS25961 Design Calculator
- TPS25961EVM eFuse Evaluation Board
- *Basics of eFuses*

9.2 ドキュメントの更新通知を受け取る方法

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25961DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T961
TPS25961DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T961

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

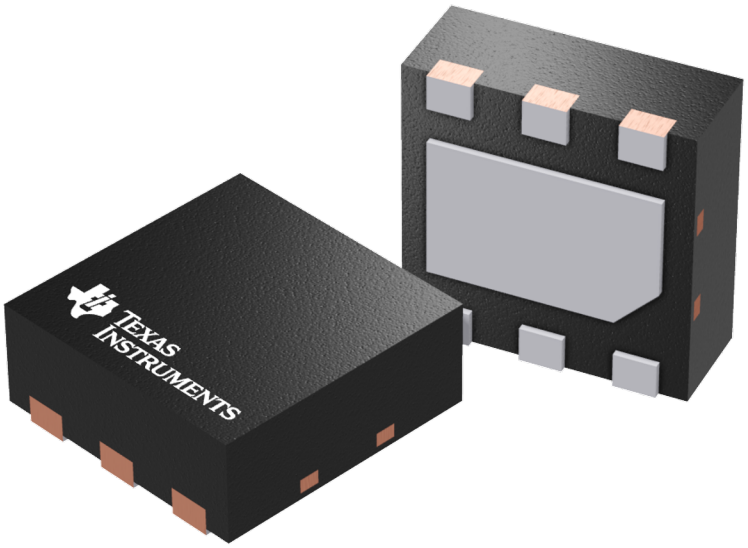
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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