TPS274C65CP 72mΩ、クワッド チャネル、スマート ハイサイド スイッチ、診断機能付き

1 特長

- クワッド チャネル、72mΩ の R_{ON} のスマート ハイサイド スイッチ
  - 低い R_{ON} により、最大 2A の DC 負荷で低消費電力を保証
- 可変電流制限によるシステム レベルの信頼性の向上
  - TPS274C65CP：250mA～1.9A の電流制限設定ポイント
  - TPS274C65CPH：290mA～2.26A の電流制限設定ポイント
- 誘導性、容量性、抵抗性負荷を駆動
  - コンデンサ充電の電流制限を調整可能
  - 誘導性負荷の逆起電圧の発生を防止する出力クランプを内蔵
- 強力な出力保護
  - サーマル シャットダウン機能を内蔵
  - グランドへの短絡イベントに対する保護
  - フォルト処理を設定可能
- 診断機能によりモジュールのインテリジェンスの向上が可能
  - ワイヤ破損検出
  - 電源への短絡を検出
- 6mm x 6mm の小型リードレス パッケージ

2 アプリケーション

- 産業用 PLC システム
  - デジタル出力モジュール
  - IO-Link マスタ・ポート
  - センサ電源

3 概要

TPS274C65CP デバイスは、産業用制御システムの要件を満たすように設計された、クワッド チャネル スマート ハイサイド スイッチです。72mΩ の低い R_{DSON} により、大きな出力負荷電流が供給される場合でもデバイスの消費電力が最小限に抑えられます。このデバイスは、保護および診断機能を内蔵しており、短絡や負荷障害などの有害な事象が発生した場合でもシステムを確実に保護します。このデバイスは、出力負荷電流に関係なく保護を提供するために、300mA～2.26A の調整可能な信頼性の高い電流制限を備えて故障を防止します。

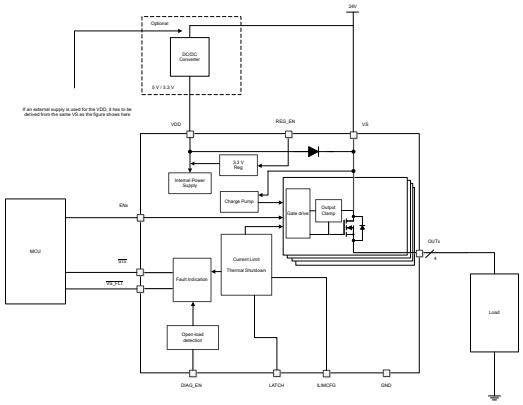
TPS274C65CP は、内部レールの電圧を生成するために内部レギュレータを備えています。また、消費電力を低減するために、VS から供給する必要がある外部 VDD 電源の使用を可能にする VDD ピンが提供されています。包括的なフォルト レポートには、VS の低電圧を示す専用の VS_FLT ピンと、各チャネルで発生したフォルトを示す個別のフォルト ピン $\overline{STx}$ が含まれます。

TPS274C65CP は、0.5mm のピン ピッチの小型 6mm × 6mm VQFN パッケージで供給され、設計の PCB の占有面積を最小限に抑えます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS274C65CP	RHA (VQFN、40)	6.00mm × 6.00mm
TPS274C65CPH		

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

表 4-1. Functionality Comparison

PART NUMBER	INTERFACE	CURRENT SENSE	CURRENT LIMIT SETTINGS ALLOW FOR 2A OPERATION	WETTABLE FLANK VERSION AVAILABLE
TPS274C65**CP**	GPIO	No current sense	No	Yes
TPS274C65**CPH**	GPIO	No current sense	Yes	Yes

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5 Pin Configuration and Functions

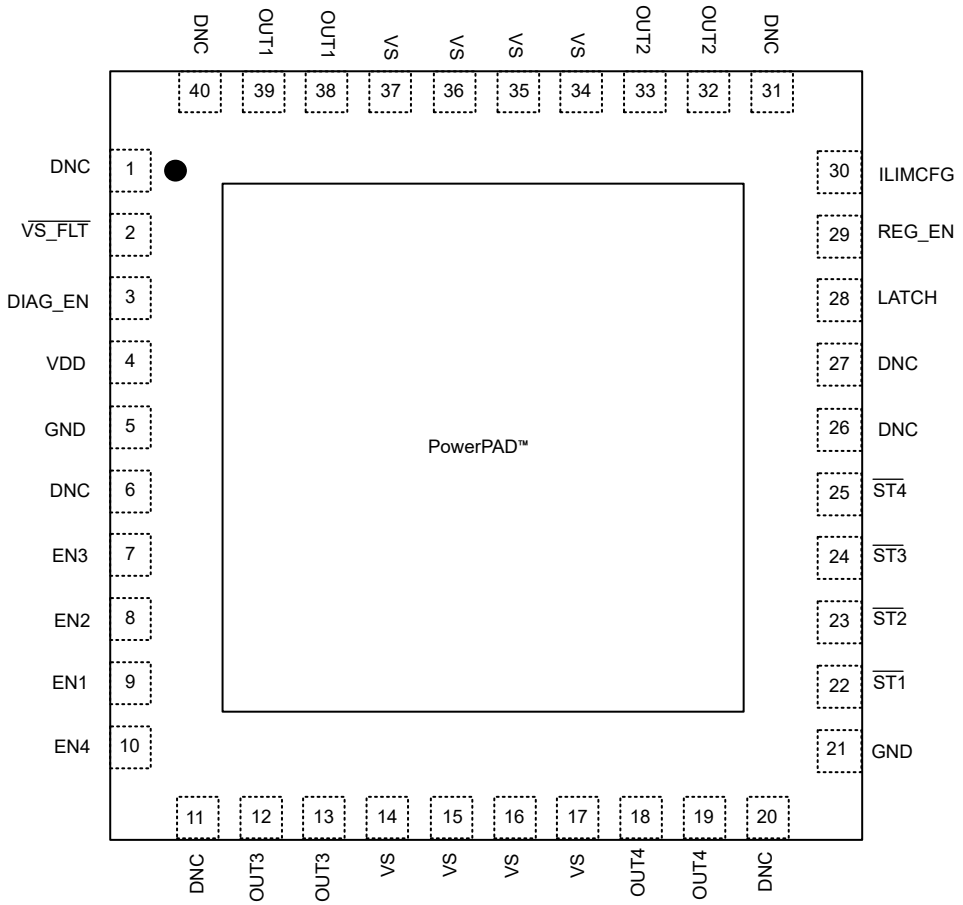


図 5-1. RHA Package, 40-Pin VQFN (Top View)

表 5-1. Pinout - Version CP, CPH

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	DNC	—	Do not connect.
2	$\overline{\text{VS_FLT}}$	O	Supply fault output – open drain, pull up with a 4.7K resistor to VDD pin.
3	DIAG_EN	I	Enable diagnostics.
4	VDD	P	Logic supply input[2].
7	EN3	I	Enable Ch3 output.
8	EN2	I	Enable Ch2 output.
9	EN1	I	Enable Ch1 output.
10	EN4	I	Enable Ch4 output.
30	ILIMCFG	I	Current limit configuration pin – set the 3-bit setting of the current limit with a resistor to the GND pin of the IC.
29	REG_EN	I	Internal regulator enable pin, float to enable. Tie to the GND pin of the IC to disable and use an external supply input to VDD.
28	LATCH	I	Configure the device in latch (on fault) mode when the pin is pulled HI. Set the pin LO for auto-retry on fault.
22	$\overline{\text{ST1}}$	O	CH1 fault status, open drain, pull up with a 4.7K resistor to VDD pin.

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表 5-1. Pinout - Version CP, CPH (続き)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
23	$\overline{ST2}$	O	CH2 fault status, open drain, pull up with a 4.7K resistor to VDD pin.
24	$\overline{ST3}$	O	CH3 fault status, open drain, pull up with a 4.7K resistor to VDD pin.
25	$\overline{ST4}$	O	CH4 fault status, open drain, pull up with a 4.7K resistor to VDD pin.
6,26,27,20	DNC	—	Do not connect.
14-17	VS	P	24V switch supply input to the IC.
38,39	OUT1	O	OUT1
32,33	OUT2	O	OUT2
12,13	OUT3	O	OUT3
18,19	OUT4	O	OUT4
34-37	VS	P	24V switch supply input to the IC.
21,5	GND	—	Device ground.
40,31,11,20	DNC	—	Do not connect.
Exposed Pad	GND	I	Connect to the GND pin of the IC.

(1) I = input, O = output, P = power
(2) When the device is configured to support an external regulator connected to VDD, the supply input for the external regulator must be derived from the same VS supply of TPS274C65CP, as shown in the Typical Application Schematic.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Continuous supply voltage, V_{VS} to IC_GND		–0.3	40	V
Maximum transient (< 1 ms) voltage at the supply pin (with respect to IC GND), V_{VS}, during ON state		–0.3	60	V
VOUT voltage to IC_GND		–30	V_{VS} + 0.3	V
V_{DS} voltage	V_{DS} voltage	–0.7	39	V
Low voltage supply pin voltage, V_{DD}	Low voltage supply pin voltage, V_{DD}	–0.3	7.0	V
Digital Input pin voltages, V_{DIG}		–0.3	7.0	V
Analog pin voltage REG_EN		–0.3	7.0	V
$\overline{FLT}$ pin voltage, $V_{\overline{FLT}}$	$\overline{FLT}$ pin voltage, $V_{\overline{FLT}}$	–0.3	7.0	V
$\overline{ST}$ pin voltage, $V_{\overline{ST}}$	$\overline{ST}$ pin voltage, $V_{\overline{ST}}$	–0.3	7.0	V
Reverse ground current, I_{GND}	V_S < 0 V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD1}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except VS and VOUTx	±2000	V
V_{ESD2}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	VS and VOUTx with respect to GND	±4000	V
V_{ESD3}	Electrostatic discharge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	All pins	±500	V
V_{surge}	Electrostatic discharge	Surge protection with 42 Ω, per IEC 61000-4-5; 1.2/50 µs	VS, OUTx	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{S_OPMAX}	Nominal supply voltage	12	36	V
V_{DD}	Low voltage supply voltages	3.0	5.5	V
V_{DIG}	All digital input pin voltage	–0.3	5.5	V
V_{ST}	$\overline{ST}$ pin voltage	–0.3	5.5	V
V_{ANA}	REG_EN pin voltage	–0.3	5.0	V
T_A	Operating free-air temperature	–40	125	°C

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6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS274C65X RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{VS} = 11 V to 36 V, V_{VDD} = 3.0 V to 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{DS_Clamp} CHx	V_{DS} clamp voltage	FET current = 10 mA, V_S = 24 V		40	44	50	V
V_{DS_Clamp} CHx	V_{DS} clamp voltage	FET current = 10 mA, V_S = 19 V		40	44	50	V
V_{DS_Clamp} CHx	V_{DS} clamp voltage	FET current = 10 mA, V_S = 10 V		33	37	41	V
V_{S_UVPF}	V_S undervoltage protection falling	Measured with respect to the GND pin of the device, All channels ON	Output FETs turned off at VS less than this threshold.	8.6	9	9.3	V
V_{S_UVPR}	V_S undervoltage protection recovery rising	Measured with respect to the GND pin of the device, All channels ON	Output FETs turned ON at VS more than this threshold.	9.5	10	10.3	V
V_{S_UVPRH}	V_S undervoltage protection deglitch time	Time from triggering the UVP fault to FET turn-off		15	20	25	µs
V_{S_UVWF}	V_S undervoltage warning falling	Measured with respect to the GND pin of the device,		12	12.5	13.5	V
V_{S_UVWR}	V_S undervoltage warning recovery rising	Measured with respect to the GND pin of the device,		11.2	13.5	15.8	V
V_{S_UVLOF}	V_S undervoltage lockout falling	Measured with respect to the GND pin of the device			3.0		V
$V_{S,UVLOR}$	V_S undervoltage lockout rising	Measured with respect to the GND pin of the device		2.7	3	3.3	V
$V_{DD,UVLOF}$	V_{DD} undervoltage lockout falling	Measured with respect to the GND pin of the device		2.7	2.8	2.9	V
$V_{DD,UVLOR}$	V_{DD} undervoltage lockout rising	Measured with respect to the GND pin of the device		2.8	2.88	2.98	V
IL_{NOM}	Continuous load current, per channel	All channels enabled, T_{AMB} = 85°C			1.6		A
		Two channels enabled, T_{AMB} = 85°C			2.5		A
$I_{OUT,LEAKX}$	Leakage current from OUT to GND in OFF state	Vs = VOUT < 36 V, Switch and all diagnostics disabled, measured into the OUTx pin				40	µA

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6.5 Electrical Characteristics (続き)

V_{VS} = 11 V to 36 V, V_{VDD} = 3.0 V to 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OUT(OFF)}$	Output leakage current (per channel)	VS <= 36 V, V_{OUT} = 0 Channel disabled, diagnostics disabled Tj <= 125°C		0	0.8	10	µA
VDD I_Q	V_{DD} quiescent current, all diagnostics disabled, external VDD	V_S ≤ 36 V, V_{DD} = 5.5 V All channels enabled, I_{OUTx} = 0 A			1.85	2.1	mA
VS I_Q	V_S quiescent current, internal VDD	V_S ≤ 36 V, All channels enabled, I_{OUTx} = 0 A			4.9	5.6	mA
VS I_Q	V_S quiescent current, external VDD	V_S ≤ 36 V, V_{DD} = 3.0 V All channels enabled, I_{OUTx} = 0 A			2.0	2.45	mA
I_{leak_LG}	Leakage current out of the output pins with the GND of IC disconnected, Load ground connected to supply ground	V_S≤ 30 V, V_{DD} = 5.5 V, RL = 24 Ω All channels enabled			0.8	0.9	mA
RON CHARACTERISTICS							
R_{ON}	On-resistance (Includes MOSFET and package)	10 V ≤ V_S ≤ 36 V, I_{OUT1} = I_{OUT2} = 200 mA	T_J = 25°C		72		mΩ
			T_J = 125°C			110	mΩ
	On-resistance when 2 channels are paralleled (Includes MOSFET and package)	10 V ≤ V_S ≤ 36 V, I_{OUT1} = I_{OUT2} > 200 mA. V_{OUT1} tied to V_{OUT2}	T_J = 25°C		33		mΩ
			T_J = 125°C			55	mΩ
VDD_REG CHARACTERISTICS							
V_{VDD}	VDD Output voltage (Internal regulator enabled)	6 V ≤ V_S ≤ 36 V, I_{VDD} < 20 mA	Includes load and line regulation across the range.	3.1	3.3	3.6	V
LR_{VDD}	Load regulation of internal VDD regulator when enabled	6 V ≤ V_S ≤ 36 V, I_{VDD} < 20 mA				0.95	V/A
LR_{tran_VDD}	Load transient regulation of internal VDD regulator when enabled	6 V ≤ V_S ≤ 36 V, I_{VDD} <step from 5 mA to 15 mA in 10 µs	1 uF			10	mV
I_{CL_VDD}	Current Limit of internal regulator	6 V ≤ V_S ≤ 36 V		25		50	mA
CURRENT LIMIT CHARACTERISTICS							
I_{CLx}	CHx I_{CL} current limitation level, H version	Regulated current at short circuit RL < 200 mohms when Enabled. VDD = 3.3 V.	Setting = 2.26 A	2.01	2.26	2.88	A
			Setting = 1.9 A	1.6	1.9	2.3	A
			Setting = 1.52 A	1.28	1.52	1.76	A
			Setting = 1.15 A	0.92	1.15	1.38	A
			Settting = 0.86 A	0.74	0.86	0.98	A
			Setting = 0.67 A	0.57	0.67	0.77	A
			Setting = 0.48 A	0.38	0.48	0.57	A
			Setting = 0.29 A	0.22	0.29	0.39	A

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6.5 Electrical Characteristics (続き)

V_{VS} = 11 V to 36 V, V_{VDD} = 3.0 V to 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CLx}	CHx I_{CL} current limitation level	Regulated current at short circuit RL < 200 mohms when Enabled. VDD = 3.3 V.	Setting = 1.9 A	1.6	1.9	2.3	A
			Setting = 1.6 A	1.35	1.6	1.85	A
			Setting = 1.25 A	1	1.25	1.5	A
			Setting = 1 A	0.85	1	1.15	A
			Setting = 0.72 A	0.62	0.72	0.82	A
			Setting = 0.56 A	0.47	0.56	0.63	A
			Setting = 0.4 A	0.32	0.4	0.47	A
			Setting = 0.25 A	0.19	0.25	0.33	A
I_{CL_PK1}	CHx Peak current enabling into permanent short	T_J = -40°C to 125°C, VS = 24V	Settting = 1.0A			2.80	A
I_{CL_PK2}	CHx Peak current threshold when short is applied while switch enabled	T_J = -40°C to 125°C VS = 24V, Minimum inductance = 2.2 uH	Settting = 1.0A			8	A
FAULT CHARACTERISTICS							
I_{WB_OFF}	Off State Wirebreak or Open-load (OL) detection internal pullup current	Switch disabled, DIAG_EN = HIGH		38	51	64	µA
$V_{WB_OFF_TH}$	Off state WireBreak (WB) or Open-load (OL) detection voltage	Channel Disabled, off-state wire-break diagnostics enabled		5.6	6	6.5	V
T_{ABS}	Thermal shutdown			160	185	210	°C
T_{HYS}	Thermal shutdown hysteresis			20	27	35	°C
V_{ol_FLT}	Fault low-output voltage	I_{FLT} = 2 mA, sink current into the pin				0.4	V
t_{RETRY}	Retry time	Time from thermal shutdown until switch re-enable.			0.6		ms
DIGITAL INPUT PIN CHARACTERISTIC							
$V_{IH, DIG}$	DIG pin Input voltage high-level	3.0 V ≤ VDD ≤ 5.5 V		0.7 × V_{VDD}			V
$V_{IL, DIG}$	DIG pin Input voltage low-level	3.0 V ≤ VDD ≤ 5.5 V				0.3 × V_{VDD}	V
R_{REG_EN}	Internal pullup resistance for REG_EN pin				1		MΩ
R_{DIGx}	Internal pulldown resistor			0.7	1	2.0	MΩ
$I_{IH, DIG}$	Input current high-level	V_{DIG} = 5 V			5		µA
DIGITAL OUTPUT PIN CHARACTERISTICS							
V_{OL_ST}	Output Logic Low Voltage	ST Pin current = –4 mA				0.4	V

6.6 Switching Characteristics

V_S = 6 V to 36 V, T_J = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	CHx Turnon delay time	V_S = 24 V, R_L = 48 Ω 50% of EN to 10% of VOUT	5	18	25	µs
t_{DF}	CHx Turnoff delay time	V_S = 24 V, R_L = 48 Ω 50% of EN to 90% of VOUT	16	24	33	µs

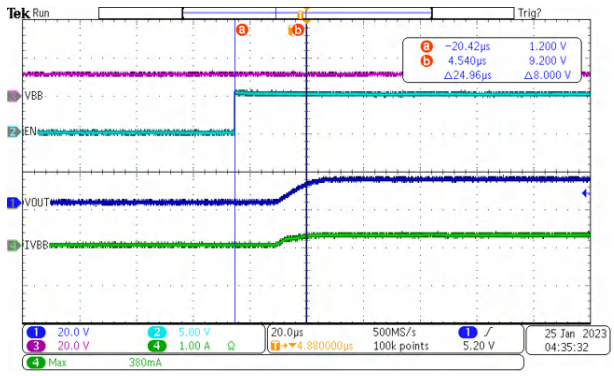
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6.6 Switching Characteristics (続き)

V_S = 6 V to 36 V, T_J = –40°C to +125°C (unless otherwise noted)

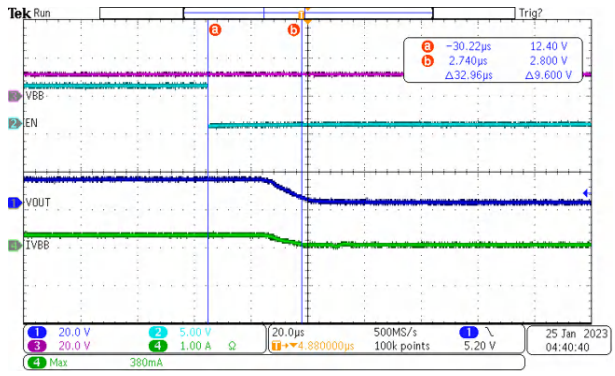
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$SR2_R$	VOUTx rising slew rate	V_S = 24 V, 25% to 75% of V_{OUT}, R_L = 48 Ω,	1	1.6	2.2	V/µs
$SR2_F$	VOUTx falling slew rate	V_S = 24 V, 75% to 25% of V_{OUT}, R_L = 48 Ω,	1	1.4	1.8	V/µs
f_{max}	Maximum PWM frequency				1	kHz
t_{ON}	CHx Turnon time	V_S = 24 V, R_L = 48 Ω 50% of EN to 90% of VOUT		33	42	µs
t_{OFF}	CHx Turnoff time	V_S = 24 V, R_L = 48 Ω 50% of EN to 10% of VOUT		46	57	µs
t_{ON} - t_{OFF}	CHx Turnon and off matching	1ms ON time switch enable pulse V_{BB} = 24 V, R_L = 48 Ω	–41	–7	23	µs
t_{ON} - t_{OFF}	CHx Turnon and off matching	100-µs OFF time switch enable pulse, V_S = 24 V, R_L = 48 Ω, F = f_{max}	–41	–7	23	µs
t_{ON} - t_{OFF}	CHxTurnon and off matching	100-µs ON time switch enable pulse, V_S = 24 V, R_L = 48 Ω, F = f_{max}	–41	–7	23	µs
Δ_{PWM}	CHx PWM accuracy - average load current	200-µs enable pulse, V_S = 24 V, R_L = 48 Ω F = f_{max}	–20		20	%

6.7 Typical Characteristics



V_{EN} = 0 to 5 V VS = 12 V T_{AMB} = 25 °C

図 6-1. Turn-on Time (tON)



V_{EN} = 5 to 0 V VS = 12 V T_{AMB} = 25 °C

図 6-2. Turn-off Time (tOFF)

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7 Parameter Measurement Information

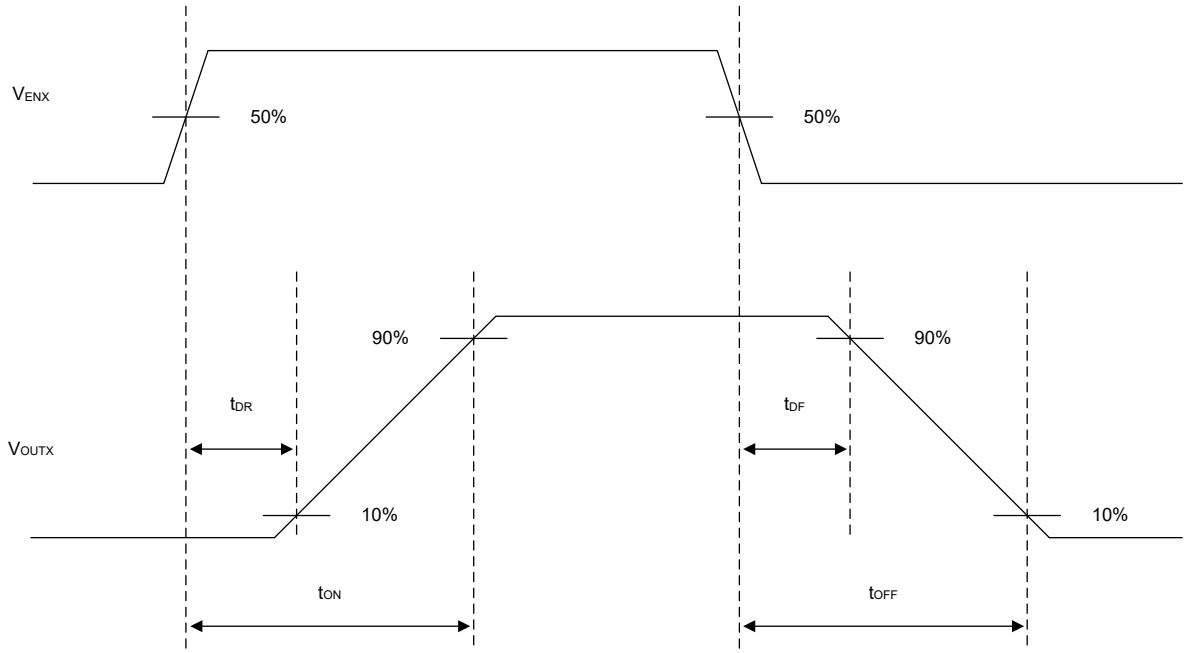


図 7-1. Switching Characteristics Definitions

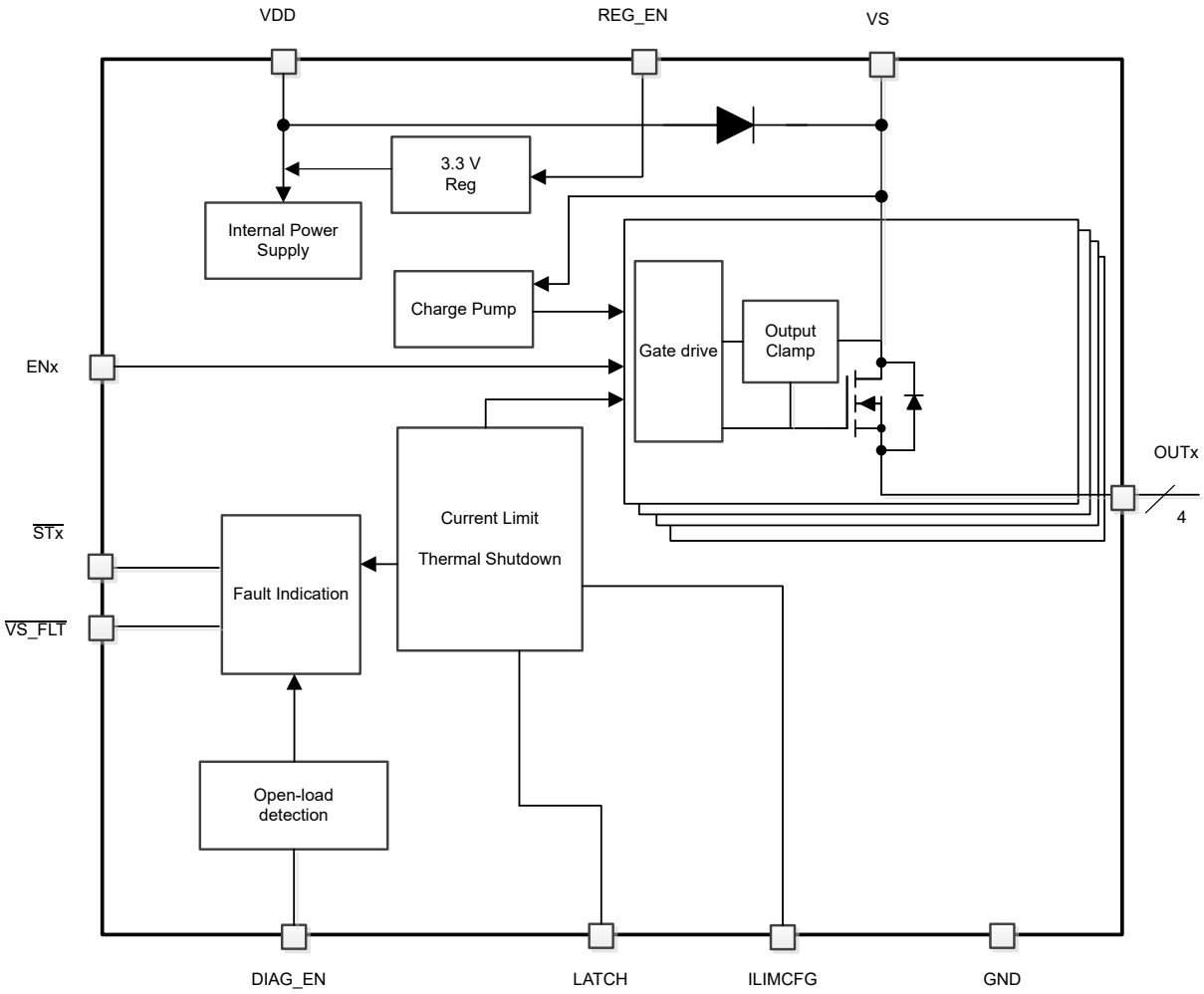
8 Detailed Description

8.1 Overview

The TPS274C65CP device is a quad channel 72-mΩ smart high-side switch intended for use for output ports with protection for 24-V industrial systems. The device is designed to drive a variety of resistive, inductive and capacitive loads. The device integrates various protection features including overload protection through current limiting, thermal protection, short-circuit protection, and reverse current protection. For more details on the protection features, refer to the *Feature Description* and *Application Information* sections of the document.

In addition, the device diagnostics features include VS UVLO reporting, individual channel fault reporting, adjustable current limit and thermal shutdown. The device also integrates open load detection in the OFF state to enable protection against wire breaks, the function can be enabled through the DIAG_EN pin. The device includes open drain $\overline{STx}$ pin output for each channel that indicates device fault states such as short to GND, short-to-supply, overtemperature, and the other fault states discussed.

8.2 Functional Block Diagram

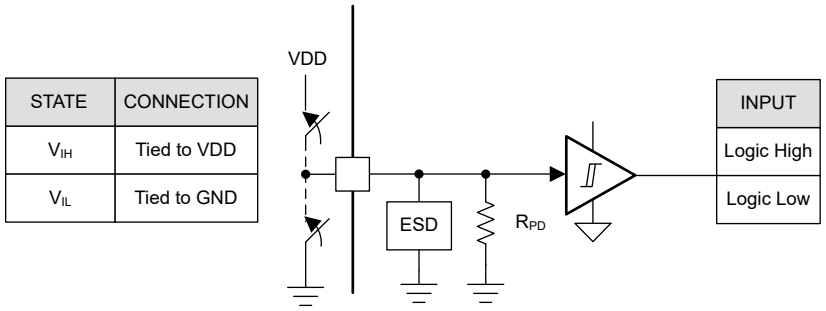


8.3 Feature Description

8.3.1 Pin Diagrams

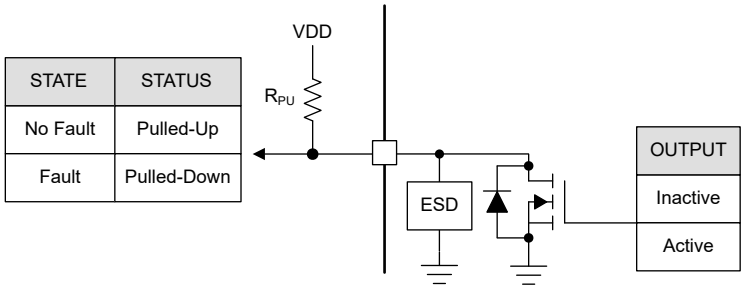
This section presents the I/O structure of all digital input and output pins.

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Logic level input pin

図 8-1. Logic Level Input PIn



Shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function properly.

図 8-2. Open Drain Output Pin ($\overline{ST}$)

8.3.2 Programmable Current Limit

The TPS274C65CP integrates an adjustable current limit feature. With external resistor at ILIMCFG pin, the current limit of the device can be adjusted. When the overload or short-circuit situation happens, the device clamps the current at preset current limit level.

A lower current limit lowers fault energy and current during a load failure event such as a short-circuit or a partial load failure. By lowering fault energy and current, the overall system improves through:

- Reduced size and cost in current carrying components such as PCB traces and module connectors
- Less disturbance at the power supply (V_S pin) during a short circuit event
- Less additional budget for the power supply to account for overload currents in one channel or more
- Improved protection of the downstream load

表 8-1. ILIMCFG Table for TPS274C65CP

Resistor Value (kΩ)(1)	Typical ILIM Threshold (A)
13.3	0.25
17.8	0.4
23.7	0.56
31.6	0.72
44.2	1
59	1.25
78.7	1.6
110	1.9

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表 8-2. ILIMCFG Table for TPS274C65CPH

Resistor Value (kΩ)(1)	Typical ILIM Threshold (A)
13.3	0.29
17.8	0.48
23.7	0.67
31.6	0.86
44.2	1.15
59	1.52
78.7	1.9
110	2.26

(1) The tolerance of the resistance is 1%.

8.3.3 Protection Mechanisms

The TPS274C65CP protects the system against load fault events like short circuits, inductive load kickback, overload events and over-temperature events. This section describes the details for protecting against each of these fault cases.

Thermal shutdown will cause the switch to automatically disable. Another scenario is when switch hits current limit, the switch will get overheated and hit thermal shutdown eventually.

The fault indication is reset and the switch turns back on when all of the below conditions are met:

- t_{RETRY} has expired
- All faults are cleared (thermal shutdown and current limit)
- LATCH pin is low

8.3.3.1 Over-current Protection

When I_{OUT} reaches the current limit threshold, I_{CL}, the device registers an overcurrent fault and begins regulating the current at the set limit. When either switch is in the FAULT state, it is indicated on the corresponding $\overline{STx}$ pin. This protects the system against overload cases where the load attempts to draw more than the maximum rated current, so the TPS274C65 can recognize and limit current or shut off these cases. In the case of a slow overload with the device channel enabled for a while, the current limit levels are as shown in 図 8-3.

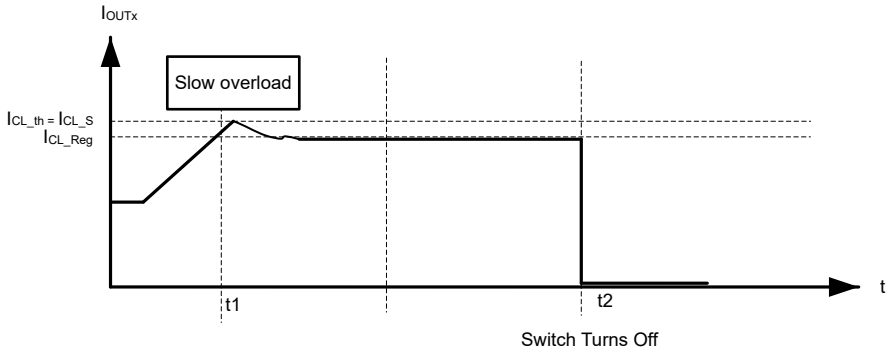


図 8-3. Overload Response

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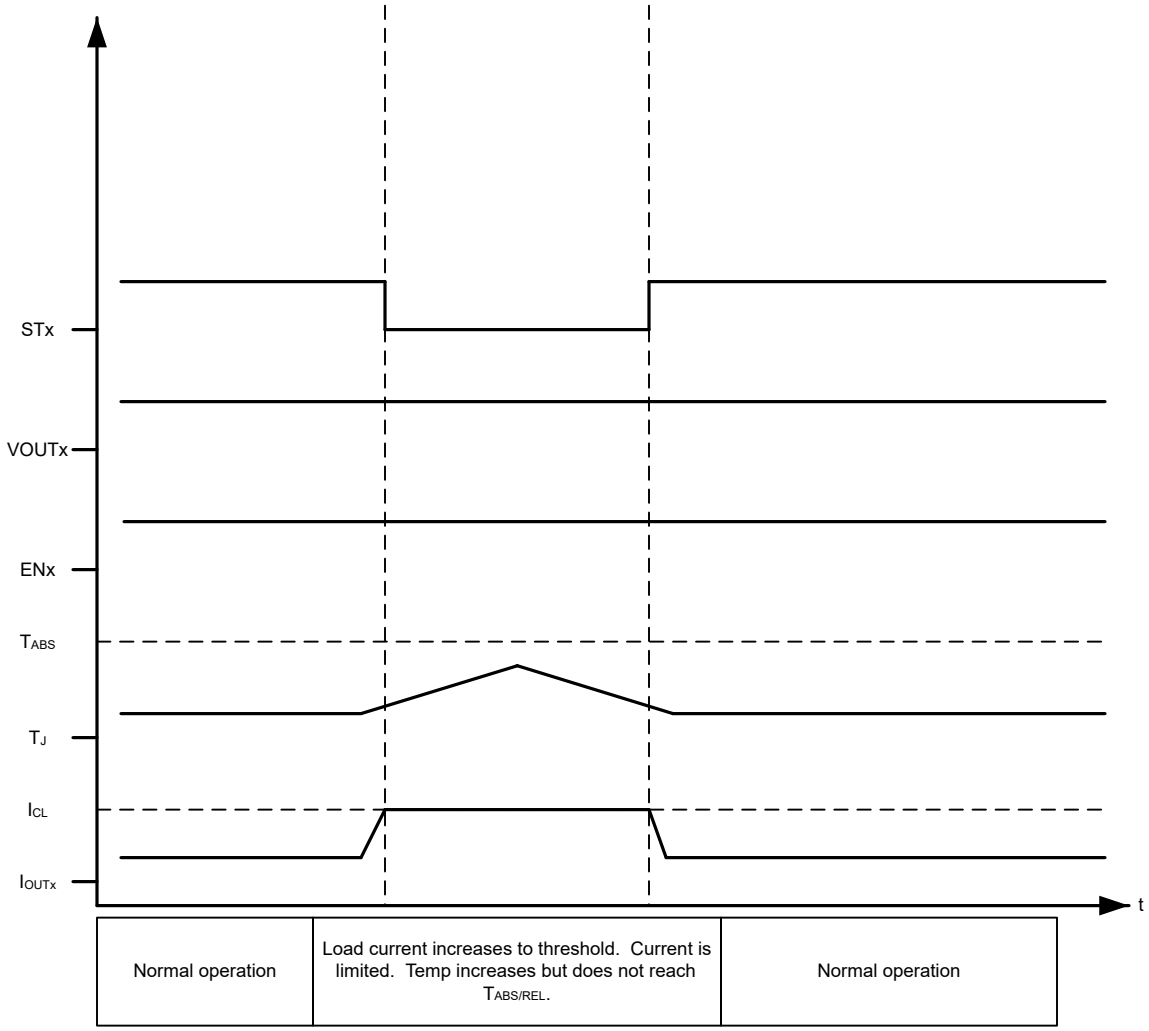


図 8-4. Overcurrent Behavior

For more details on the current limiting functionality, please see *Programmable Current Limit*.

8.3.3.2 Short-Circuit Protection

The TPS274C65CP provides output short-circuit protection to ensure that the device prevents current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The TPS274C65CP is guaranteed to protect against short-circuit events regardless of the state of the ILIM pins.

図 8-5 shows the behavior of the TPS274C65CP when the device is enabled into a short circuit.

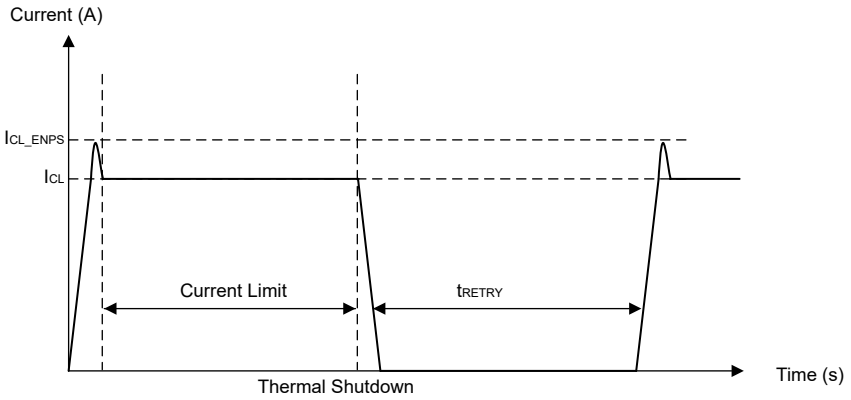


図 8-5. Enable into Short-Circuit Behavior

Due to the low impedance path, the output current rapidly increases until it hits the current limit threshold. Due to series inductance and deglitch, the measured maximum current can temporarily exceed the I_{CL} value defined as I_{CL_ENPS}, however, it settles to the current limit.

In this state, high power is dissipated in the FET, so eventually the internal thermal protection temperature for the FET is reached and the device safely shuts down. If the device is not configured in latch mode, the device waits t_{RETRY} amount of time and turns the channel back on.

図 8-6 shows the behavior of the TPS274C65CP when a short-circuit occurs when the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to ensure overshoot is limit, the device implements a fast trip level at a level I_{OVCR}. When this fast trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to I_{CL_Reg} level after a brief transient overshoot to the I_{CL_ENPS} level. The device then keeps the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device safely shuts off.

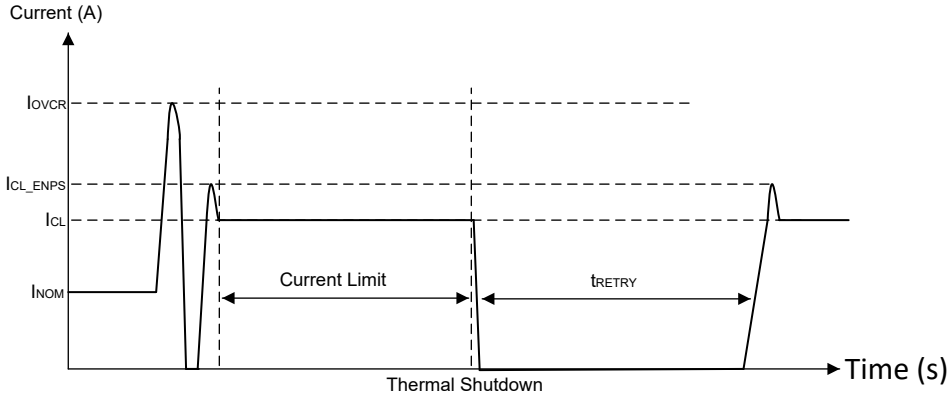


図 8-6. On-State Short-Circuit Behavior

Soft Short- Circuit Behavior shows the behavior of the TPS274C65CP when there is a small change in impedance that sends the load current above the I_{CL} threshold. The current rises to I_{CL_LINPK} since the FET is still in the linear mode. Then the current limit kicks in and the current drops to the I_{CL} value.

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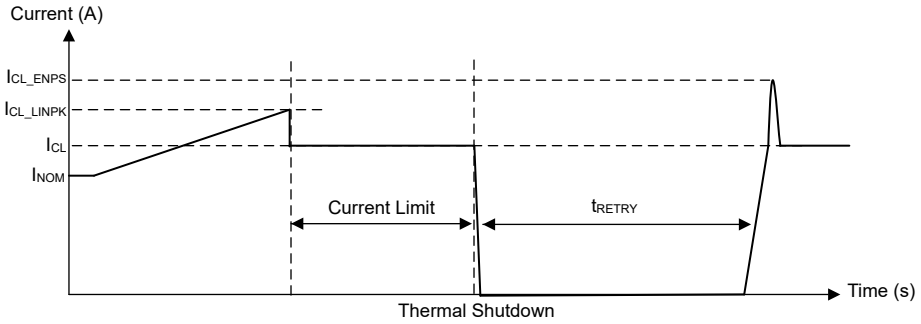


図 8-7. Soft Short-Circuit Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

8.3.3.2.1 V_S During Short-to-Ground

When V_{OUT} is shorted to ground, the module power supply (V_S) can see a transient decrease. This decrease is caused by the sudden increase in current flowing through the cable inductance. For ideal system behavior, TI recommends that the module supply capacitance be increased by adding bulk capacitance on the power supply node.

8.3.3.3 Thermal Shutdown Behavior

図 8-8 shows the thermal shutdown behavior when LATCH pin is high. As shown, the switch clamps the current until it hits thermal shutdown, and then the device will remain latched off until the EN or LATCH pin toggles. Although the device is configured in latched condition, there is an internal t_{RETRY} period. ST pin will remain low and output will remain OFF even when EN or LATCH toggled within the t_{RETRY} period.

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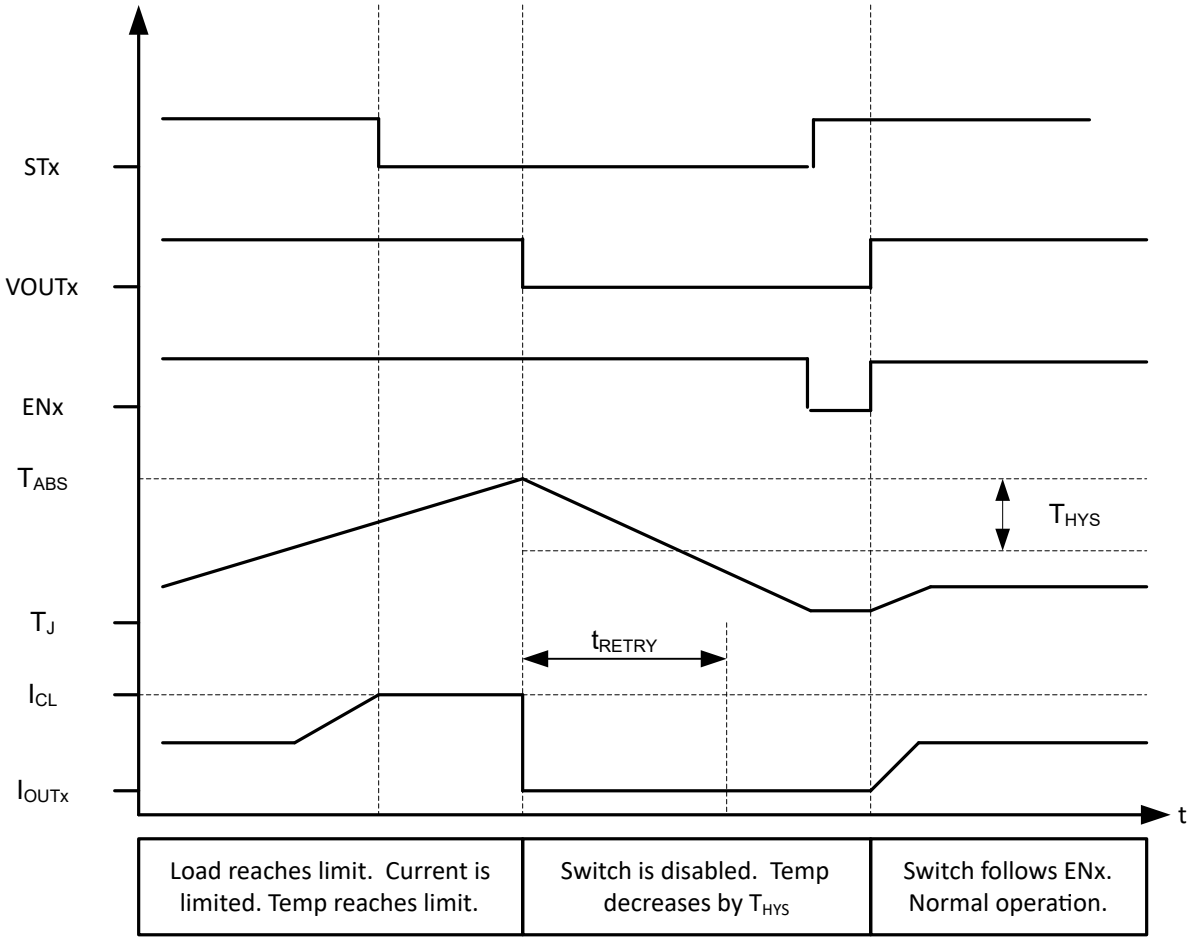


図 8-8. Thermal Shutdown – Latched Behavior

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図 8-9 shows the behavior with LATCH pin low (auto-retry mode). hence, the switch will retry after the fault is cleared and t_{RETRY} has expired.

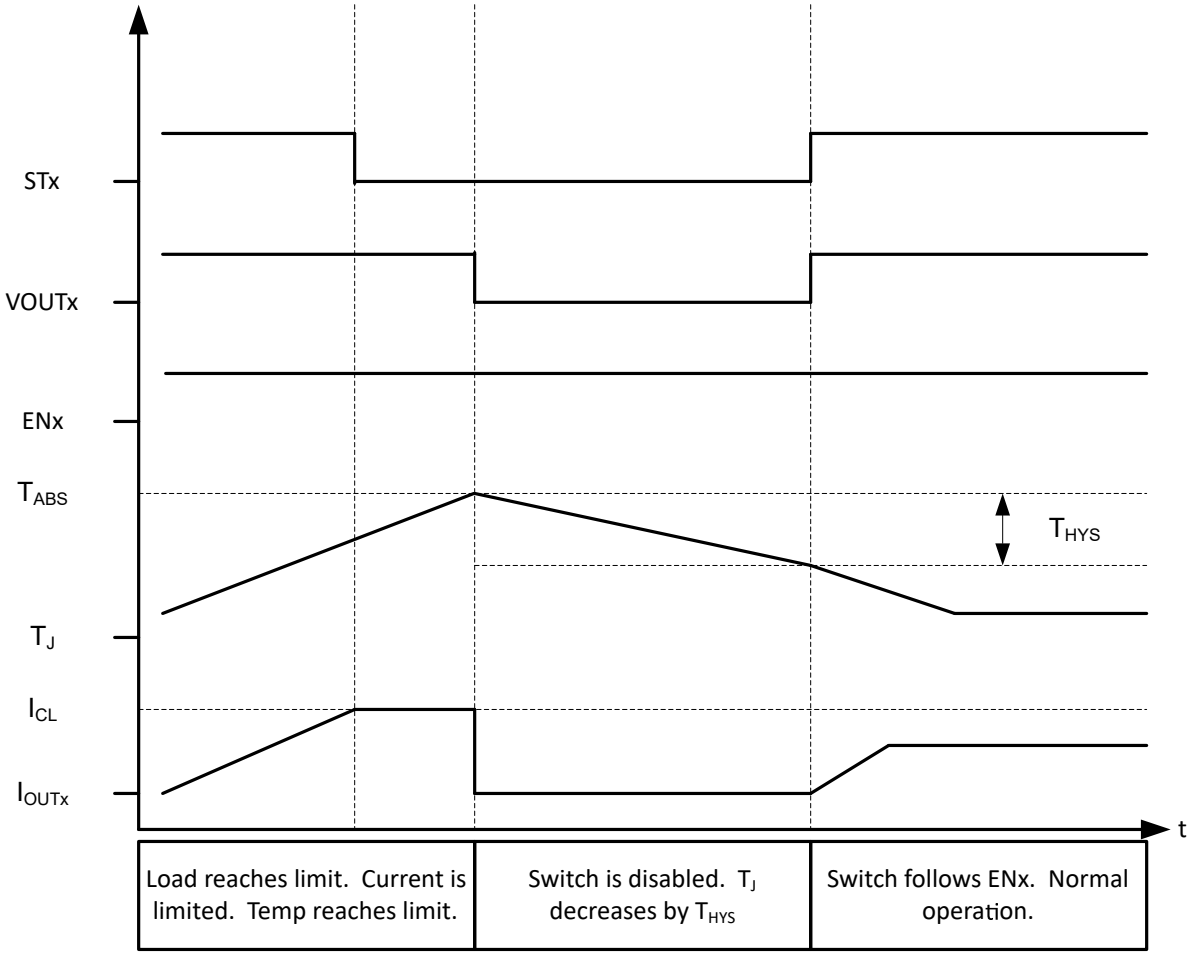


図 8-9. Thermal Shutdown - Auto-retry Behavior

8.3.3.4 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,clamp}$, the clamp diode between the drain and gate.

$$V_{DS,Clamp} = V_S - V_{OUT} \quad (1)$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply (E_S) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_S + E_{LOAD} = E_S + E_L - E_R \quad (2)$$

From the high-side power switch's view, E_{HSD} equals the integration value during the current-decay period.

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$$E_{HSD} = \int_{0}^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \tag{3}$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \tag{4}$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{5}$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \tag{6}$$

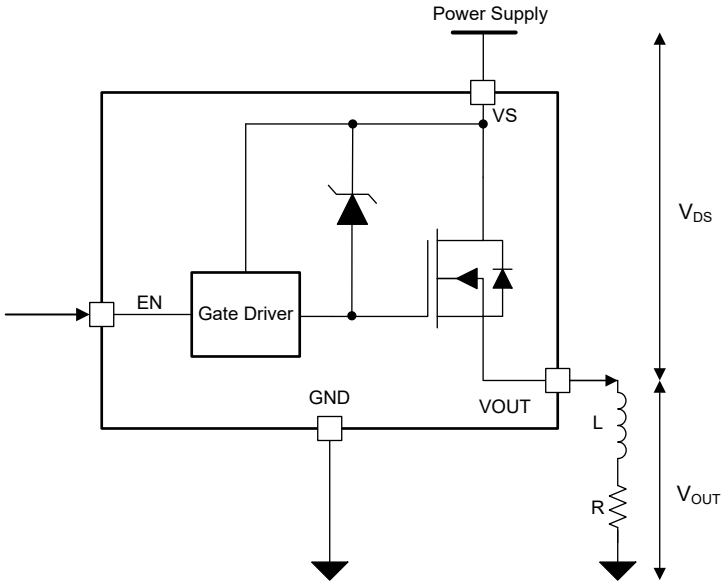


図 8-10. Driving Inductive Load

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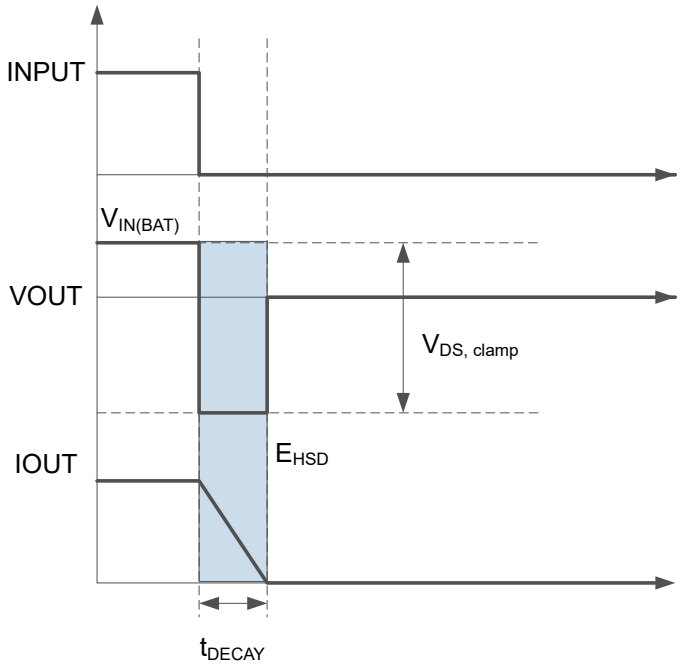


図 8-11. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, supply energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

8.3.3.5 Inductive Load Demagnetization

When switching off an inductive load, the inductor can impose a negative voltage on the output of the switch. The TPS274C65 includes voltage clamps between VS and VOUT to limit the voltage across the FETs and demagnetize load inductance if there is any. The negative voltage applied at the OUT pin drives the discharge of inductor current. 図 8-12 shows the device discharging a load of 100 mH paralleled with 48 Ω, resulting 500mA at the turn-off.

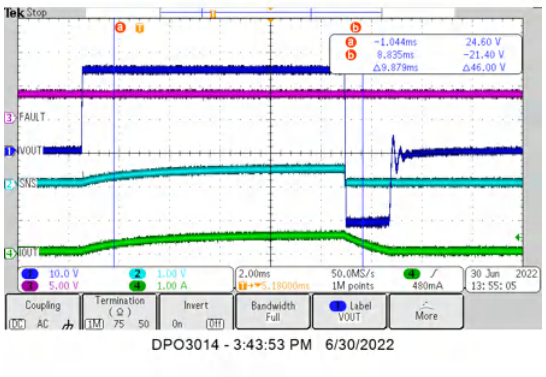


図 8-12. TPS274C65 Inductive Discharge (100 mH + 48 Ω)

The maximum acceptable load inductance is a function of the energy dissipated in the device and therefore the load current and the inductive load. The maximum energy and the load inductance the device can withstand for one pulse inductive dissipation at 125°C is shown in 図 8-13. The device can withstand 40% of this energy for

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one million inductive repetitive pulses with a 2-Hz repetitive pulse. If the application parameters exceed this device limit, use a protection device like a freewheeling diode to dissipate the energy stored in the inductor.

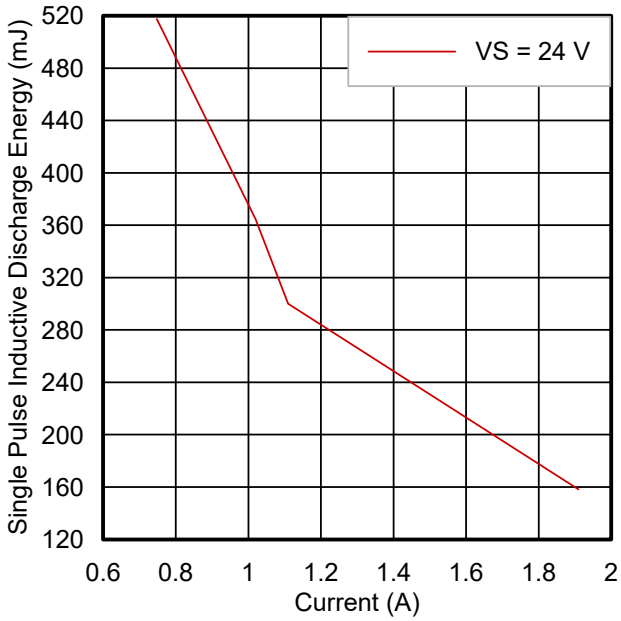


図 8-13. Maximum Energy Dissipation (E_{AS}) Allowed $T_{J,\,START}$ = 125°C - Single Pulse, One Channel

8.3.3.6 Thermal Shutdown

The TPS274C65CP includes a temperature sensor on the power FET and also within the controller portion of the device. There are two cases that the device registers a thermal shutdown fault:

- $T_{J,FET} > T_{ABS}$
- $(T_{J,FET} – T_{J,controller}) > T_{REL}$

The first condition enables the device to register a long-term overtemperature event (caused by ambient temperature or too high DC current flow), while the second condition allows the device to quickly register transient heating that is causes in events like short-circuits.

After the fault is detected, the switch turns off. If $T_{J,FET}$ passes T_{ABS}, the fault is cleared when the switch temperature decreases by the hysteresis value, T_{HYS}. If instead the T_{REL} threshold is exceeded, the fault is cleared after T_{RETRY} passes.

Each channel shuts down independently in case of a thermal event, as each has its own temperature sensor and fault reporting.

8.3.3.7 Undervoltage Protection on VS (UVP)

The device monitors the supply voltage V_S to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{S_UVPF}, the switches shut off. If the voltage is still above the $V_{S,UVLOR}$, the $\overline{VS_FLT}$ pin is pulled low to signal the supply fault if the supply. When the supply rises up to V_{S_UVPR}, the device turns back on and $\overline{VS_FLT}$ is cleared.

Fault is not indicated on the $\overline{STx}$ pin during an UVLO event. During an initial ramp of V_{VS} from 0 V at a ramp rate slower than 1 V/ms, V_{ENx} pins must be held low until V_S is above the UVP threshold. For best operation, ensure that V_S has risen above UVP before setting the V_{ENx} pins to high.

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8.3.3.8 Undervoltage Lockout on Low Voltage Supply (VDD_UVLO)

The device monitors the input supply voltage V_{VDD} (in versions A/C) to prevent unpredictable behavior in the event that the supply voltage is too low. When the supply voltage falls down to V_{VDD_UVLOF}, the device channel outputs are disabled. The device resumes normal operation when VDD rises above the VDD_{UVLOR} threshold.

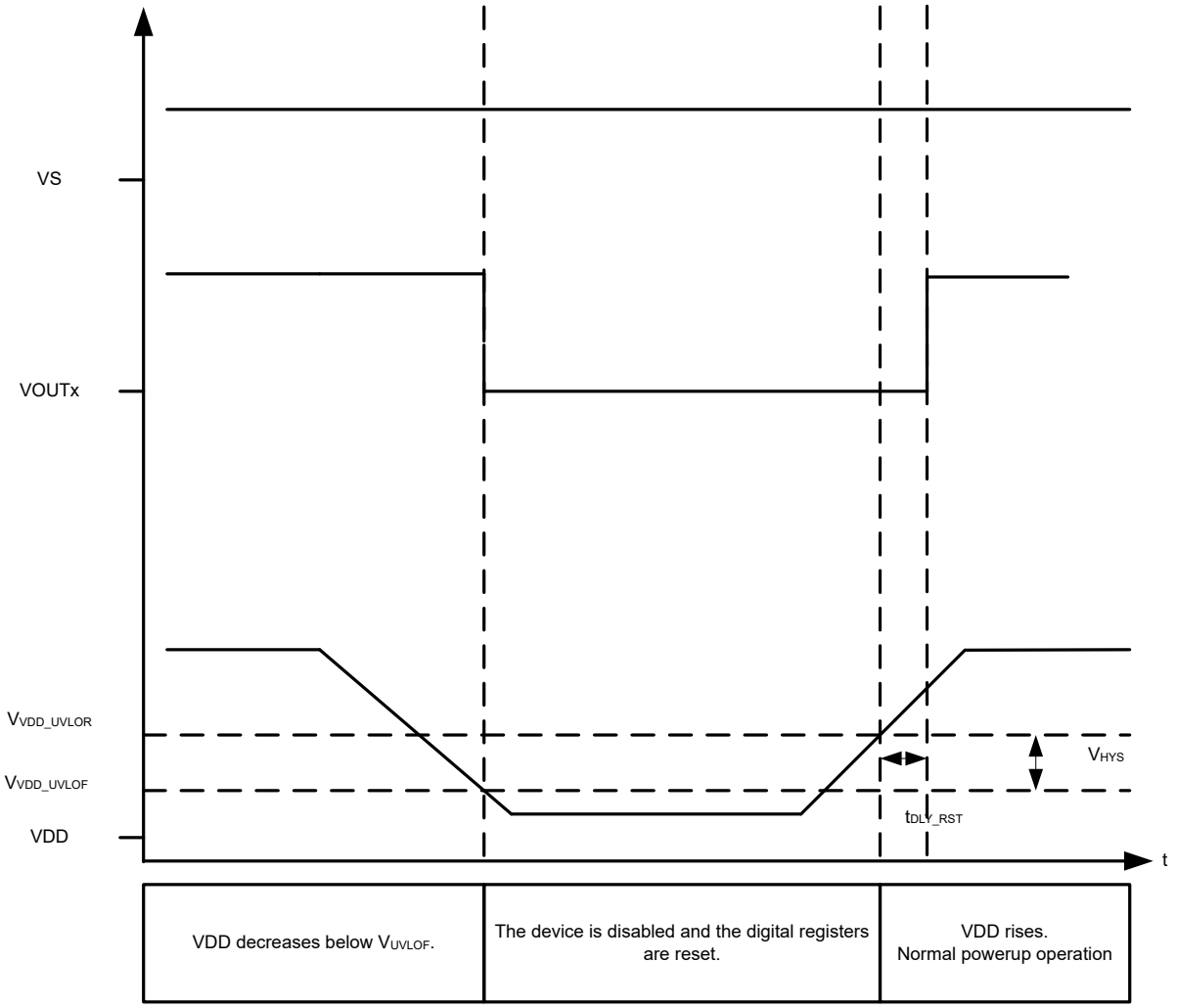


図 8-14. VDD UVLO

8.3.3.9 Power-Up and Power-Down Behavior

Device is in OFF or POR state when the device is not powered. $\overline{STx}$ and VOUTx are in the high-Z state.

After the $V_S > V_{S_UVPR}$ and $V_{DD} > V_{DD,UVLOR}$, the device is ready for full operation.

In case the VDD power supply is enabled first and the VDD voltage exceed $V_{DD,UVLOR}$ before the VS supply is up and VS voltage exceeds V_{S_UVPR}, the outputs remain disabled.

8.3.4 Diagnostic Mechanisms

As systems demand more intelligence, having robust diagnostics measuring the conditions of output power is increasingly important. The TPS274C65 integrates many diagnostic features that enable modules to provide predictive maintenance and intelligence power monitoring to the system.

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8.3.4.1 Fault Indication

The following faults are a register a fault that show on the $\overline{ST}$ pin:

- FET thermal shutdown
- Active current regulation
- Open load detection in OFF state
- V_{OUT} short to battery during OFF state

Condition	VS	VDD	ENx	OUTx	DIAG_EN	LATCH	$\overline{VS_FAULT}$	$\overline{STx}$	FAULT Recovery
VS Undervoltage	< V_{S_UVP}	> $V_{DD,UVLO}$	X	X	X	X	L	H	-
Normal	> V_{S_UVP}	> $V_{DD,UVLO}$	L	L	X	X	H	H	-
	> V_{S_UVP}	> $V_{DD,UVLO}$	H	H	X	X	H	H	-
OFF-state Short to Supply, OFF-state open load	> V_{S_UVP}	> $V_{DD,UVLO}$	L	H	H	X	H	L	-
Short to GND, Overload, TSD	> V_{S_UVP}	> $V_{DD,UVLO}$	H	L	X	L	H	L	Auto-retry
	> V_{S_UVP}	> $V_{DD,UVLO}$	H	L	X	H	H	L	Latch-off. Fault recovers when ENx toggles.

8.3.4.2 Short-to-Battery and Open-Load Detection

The TPS274C65CP is capable of detecting short-to-battery and open-load events when the switch is in the OFF state if the DIAG_EN is high. The fault will be report to $\overline{STx}$ pin. The feature can be turned off by pulling the DIAG_EN pin low. The detection threshold will be when V_{OUT} > $V_{WB_OFF_TH}$.

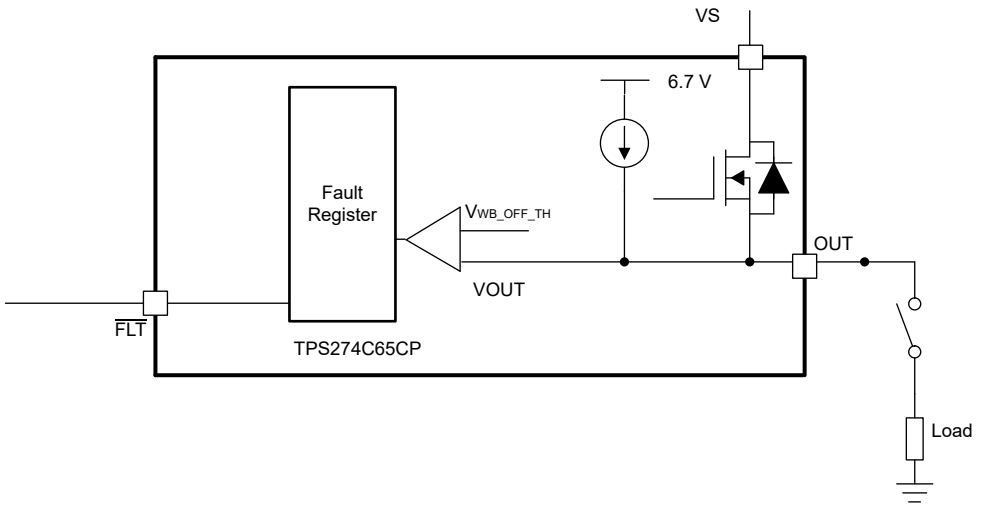


図 8-15. Open-Load Detection Circuit

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8.4 Device Functional Modes

During typical operation, the TPS274C65CP can operate in a number of states that are described below.

8.4.1 Off

OFF state occurs when the device is not powered.

8.4.2 Active

In ACTIVE state, the switch is enabled with ENx high. The diagnostic functions can be either on or off during ACTIVE state.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections give examples of typical implementation and design examples.

9.2 Typical Application

図 9-1 shows the schematic of a typical application of the TPS274C65. the schematic includes all standard external components. This section of the data sheet discusses the considerations in implementing commonly required application functionality.

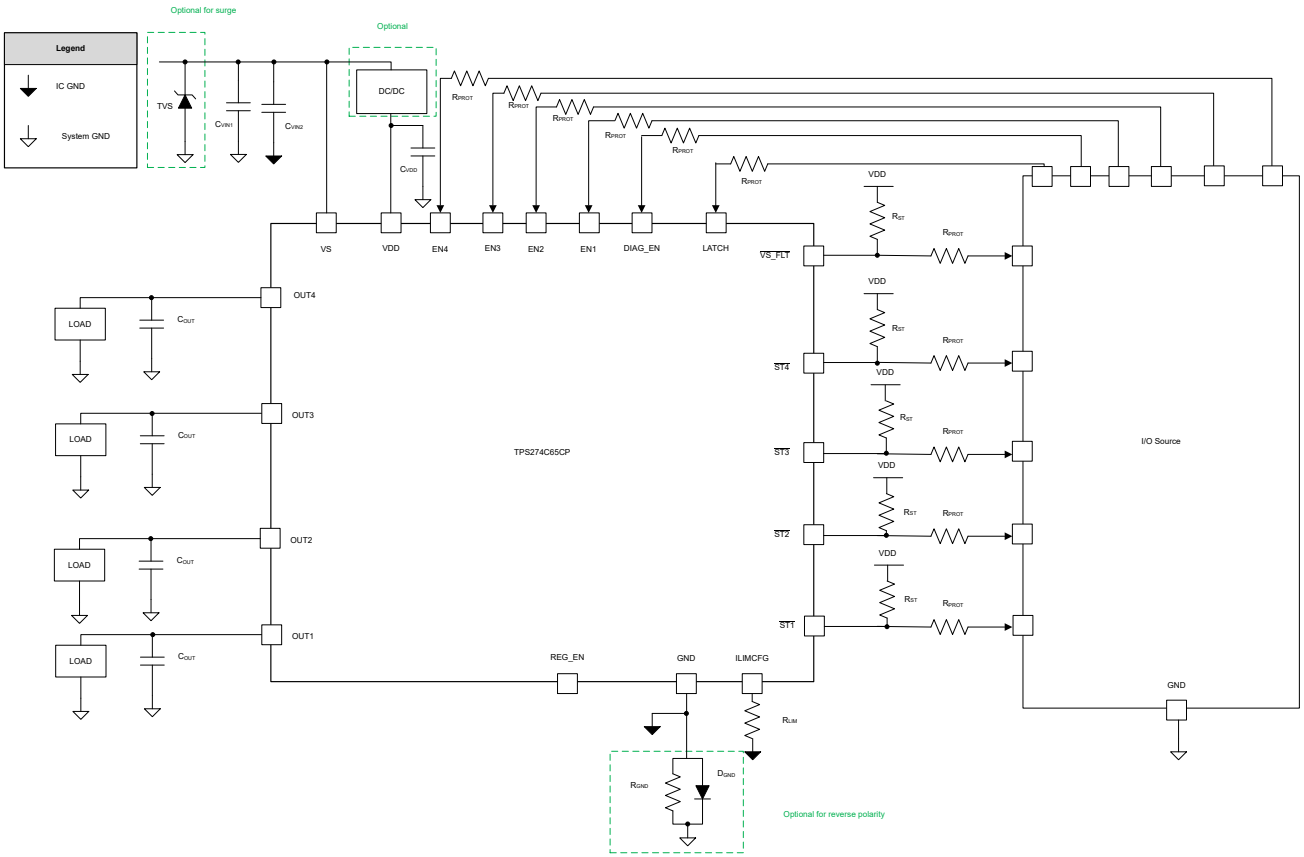


図 9-1. Typical Application Circuit

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9.2.1 Design Requirements

表 9-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{PROT}	5-10 kΩ	Protect microcontroller and device I/O pins
R_{ST}	4.7 kΩ	Open-drain pull-up resistor
R_{ILIMx}	13.3 kΩ to 110 kΩ	Discrete value outlined in 表 8-1
C_{Vin1}	100 nF to System GND	Stabilize the input supply and filter out low frequency noise
C_{Vin2}	4.7 nF to IC GND	Filtering of voltage transients (for example, ESD, IEC 61000-4-5) and improved emissions
C_{VDD}	2.2 uF to Module GND	Stabilize the input supply and limit supply excursions.
C_{OUT}	22 nF	Filtering of voltage transients (for example, ESD, RF transients)
Z_{TVS}	36-V TVS	Clamp surge voltages at the supply input
D_{GND}	Diode with < 0.7-V forward voltage drop	Optional for reverse polarity protection - if needed
R_{GND}	4.7 kΩ	Stabilize IC GND in the event of negative output swings when GND network is used

9.2.2 Detailed Design Procedure

In an example application with maximum load current of 500 mA, the current limit must be set to an acceptable level. With the current limit variation and tolerance allowed for this specific application, the current limit setting of 1 A is chosen. Referring back to the 表 8-1, 44.2-kΩ resistor with 1% tolerance needs to be placed at the ILIMCFG pin.

Depending on the tolerance on the maximum current for the application, the current limit resistor can be chosen to leave the overhead needed before the current limit engages.

9.2.2.1 IEC 61000-4-5 Surge

The TPS274C65 is designed to survive against IEC 61000-4-5 surge using external TVS clamps. The device is rated to 48 V ensuring that external TVS diodes can clamp below the rated maximum voltage of the TPS274C65. Above 48 V, the device includes V_{DS} clamps to help shunt current and ensure that the device survives the transient pulses. Depending on the class of the output,TI recommends that the system has a SMBJ36A or SMCJ36A between VS and module GND.

9.2.2.2 Loss of GND

The ground connection can be lost either on the device level or on the module level. If the ground connection is lost, both the channel outputs are disabled irrespective of the EN input level. If the switch was already disabled when the ground connection was lost, the outputs remain disabled even when the channels are enabled. The steady state current from the output to the load that remains connected to the system ground is below the level specified in the *Specifications* section of this document. When the ground is reconnected, normal operation resumes.

9.2.2.3 Paralleling Channels

If an application requires lower power dissipation than is possible with a 65-mΩ switch. Since the retry timer for each channel is not synchronized in TPS274C65CP, TI recommends to have the current limit for a single channel set higher than the total current for the paralleled channel. For example, if two of the channel are paralleled to drive 2A total current through the two channels, then the individual channel current limit needs to be set higher than 2A.

If the current limit cannot be set higher, a manual toggle of ENx (enable signals for the channels being paralleled) is needed after a thermal fault event happened.

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9.2.3 Application Curves

図 9-2 shows a test example of switching the load with 250 kHz PWM signal. Test conditions: VS =12 V, Duty Cycle = 5%, T_{AMB} = 25 °C. Channel 1 is V_{OUT} voltage. Channel 2 is EN pin voltage. Channel 3 is VS voltage. Channel 4 is VS current.

図 9-3 shows a test example of enabling a switch while there is a short at the output. Test conditions: VS = 24 V, T_{AMB} = 25 °C. Channel 1 is V_{OUT} voltage. Channel 2 is $\overline{FAULT}$ pin voltage. Channel 3 is VS voltage. Channel 4 is VS current.

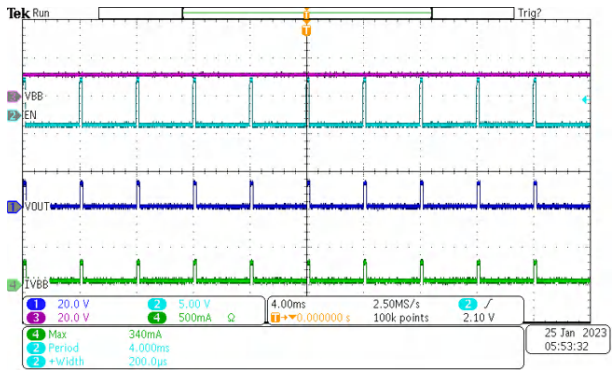


図 9-2. 250 kHz PWM Switching

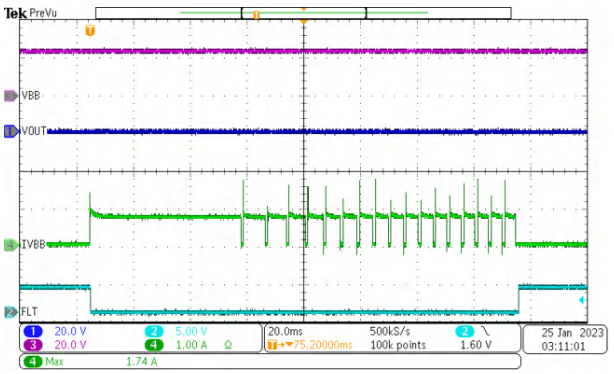


図 9-3. Enable into Short Circuit

9.3 Power Supply Recommendations

表 9-2. Operating Voltage Range

V_S Voltage Range	Note
12 V to 36 V	Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected up to 125°C.
36 V to 39 V	Functional operation per data sheet (switch can turn off), but can not meet parametric specifications.

9.4 Layout

9.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than T_{ABS}. If the output current is very high, the power dissipation can be large. The VQFN package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

1. Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
2. Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board
3. Plate shut or plug and cap all thermal vias on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

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9.4.2 Layout Example

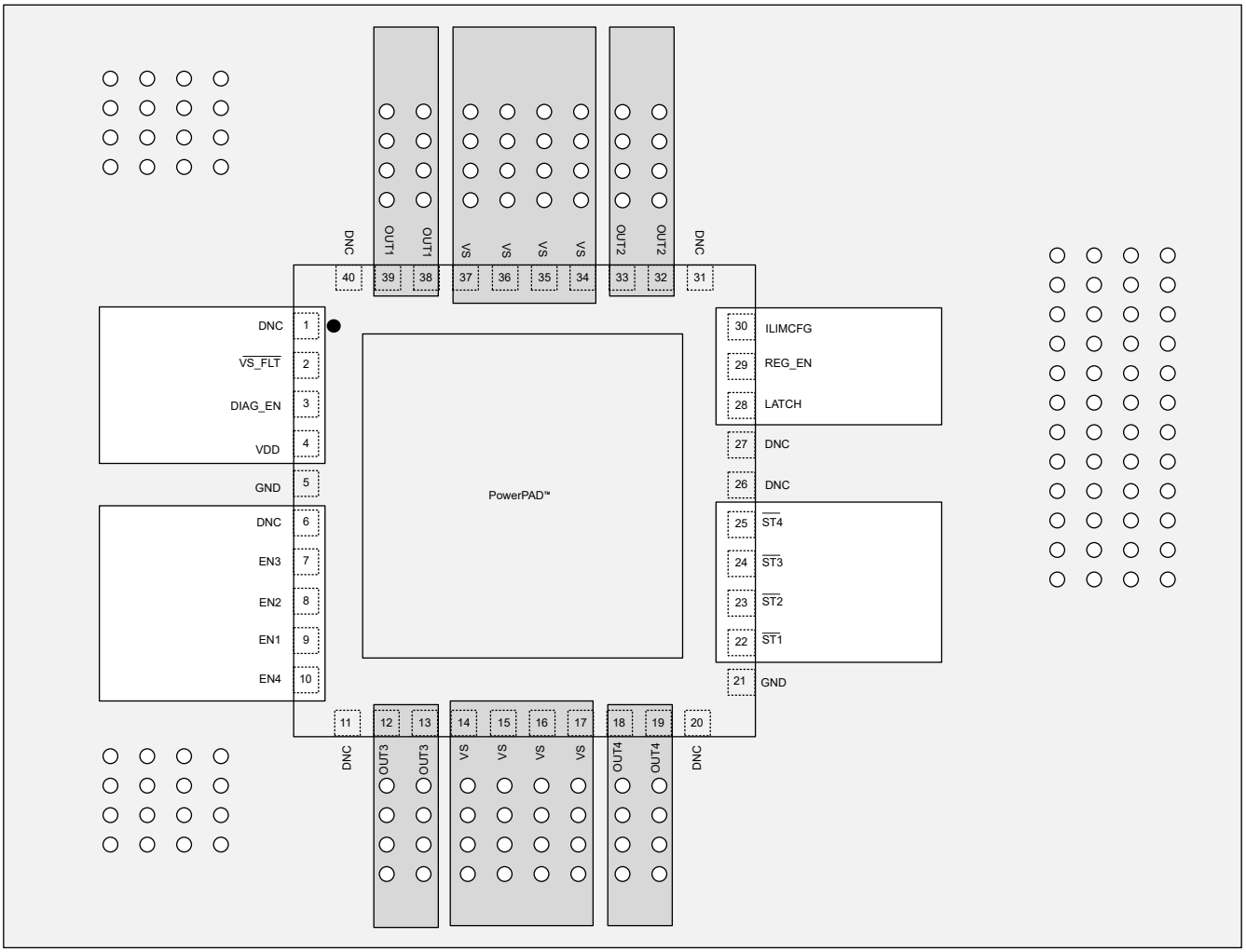


図 9-4. TPS274C65CP Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Texas Instruments, *Adjustable Current Limit of Smart Power Switches* application report

Texas Instruments, *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads* application report

Texas Instruments, *Improved Automotive Short Circuit Reliability Through Adjustable Current Limiting* application note

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (February 2024)	Page
• Updated *Device Comparison Table* to include the H version	3
• Updated *Electrical Characteristics* table to include the current limit for H version devices	6
• Added plots for thermal shutdown latched and auto-retry behavior in *Thermal Shutdown Behavior* section	17

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS274C65CPHRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C6 5CPHRHA
TPS274C65CPHRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C6 5CPHRHA
TPS274C65CPHWRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C6 5CPHWRHA
TPS274C65CPHWRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C6 5CPHWRHA
TPS274C65CPRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C 65CPRHA
TPS274C65CPRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C 65CPRHA
TPS274C65CPWRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C 65CPWRHA
TPS274C65CPWRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS274C 65CPWRHA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

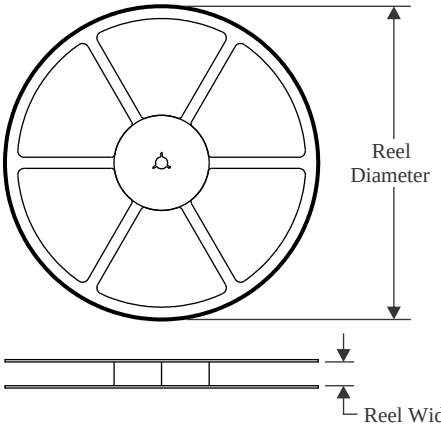
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

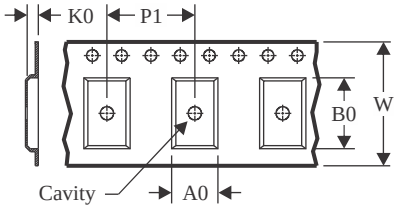
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

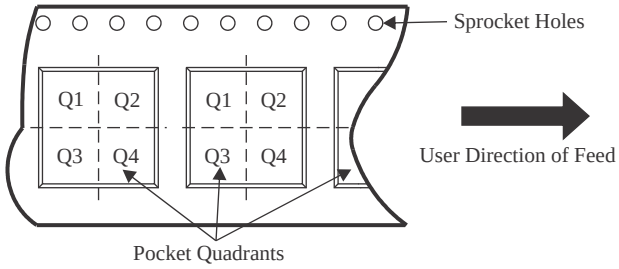


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

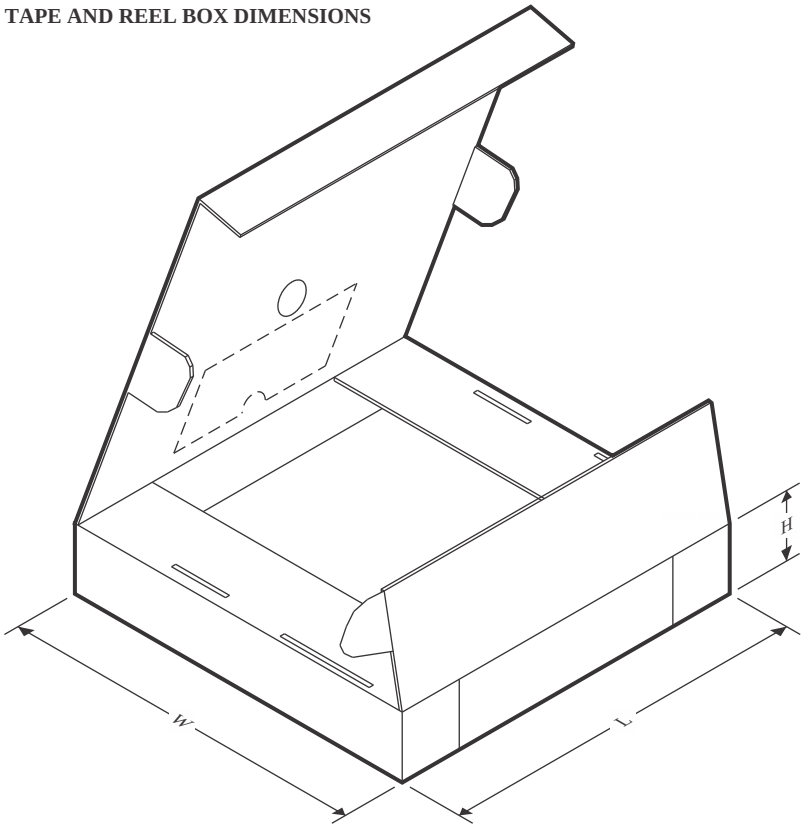
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS274C65CPHRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS274C65CPHWRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS274C65CPRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS274C65CPWRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS274C65CPHRHAR	VQFN	RHA	40	2500	360.0	360.0	36.0
TPS274C65CPHWRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
TPS274C65CPRHAR	VQFN	RHA	40	2500	360.0	360.0	36.0
TPS274C65CPWRHAR	VQFN	RHA	40	2500	360.0	360.0	36.0

GENERIC PACKAGE VIEW

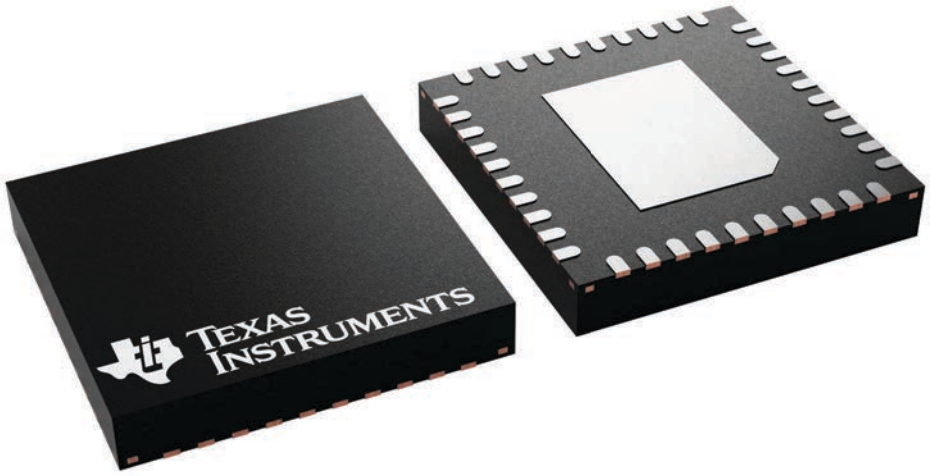
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



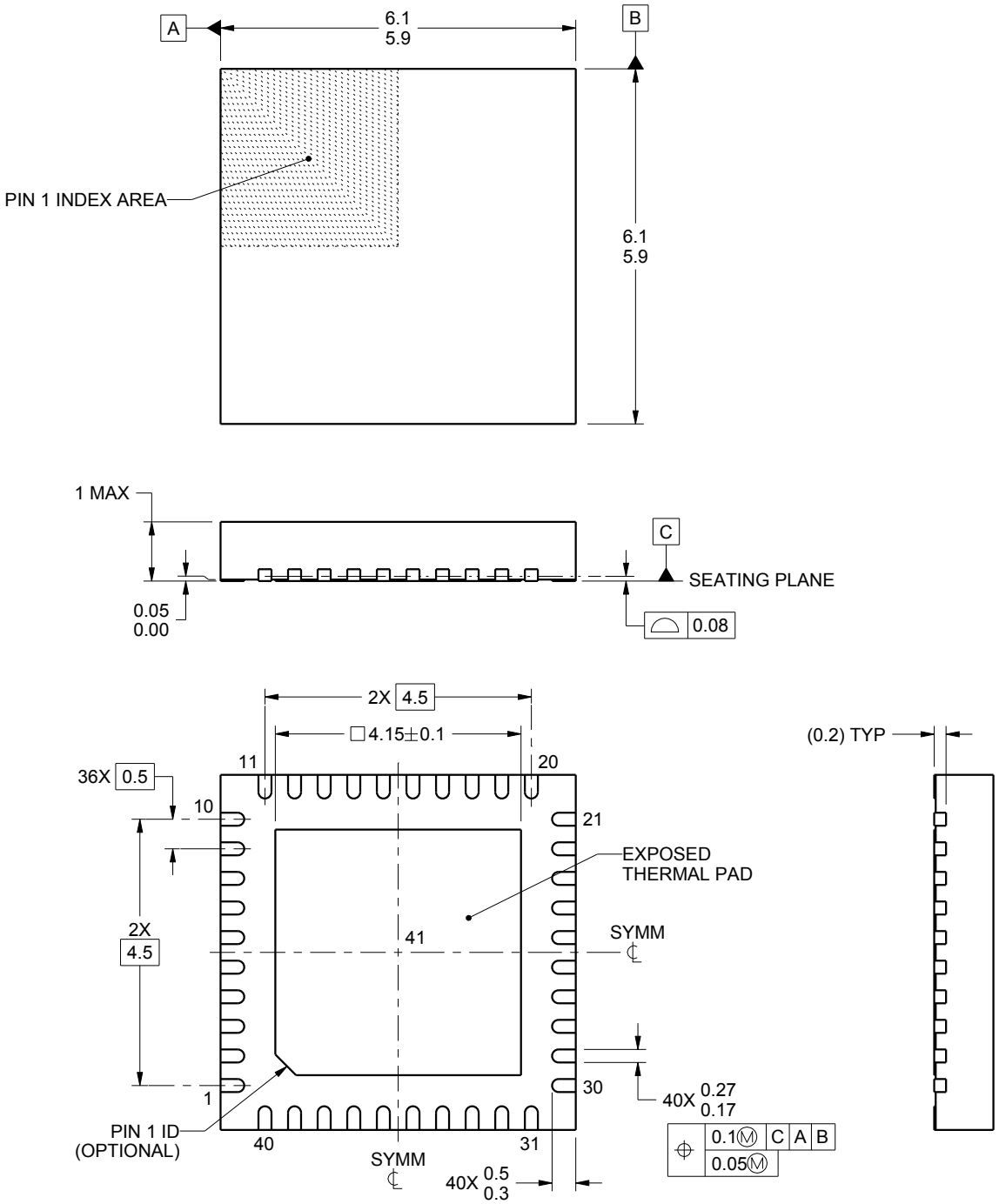
4225870/A

PACKAGE OUTLINE

RHA0040B

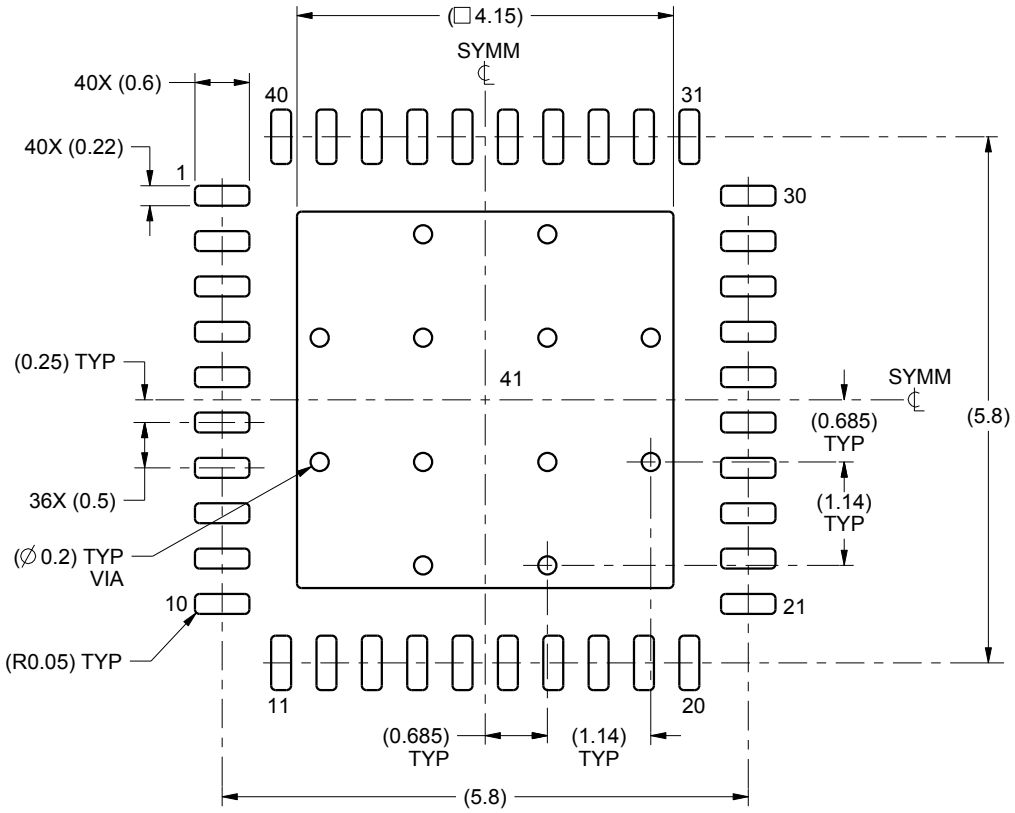
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

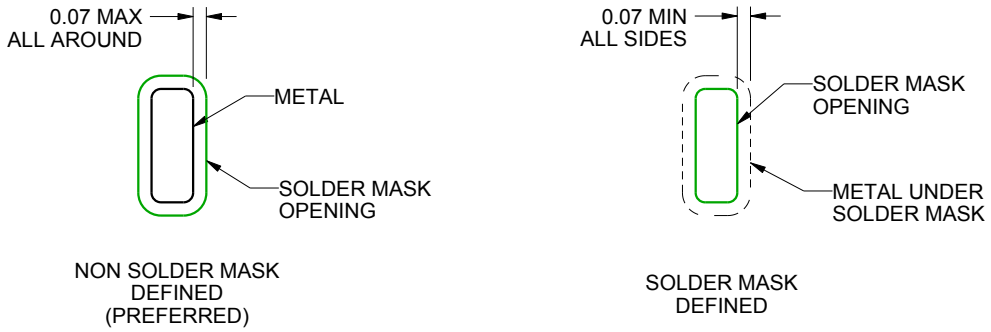


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

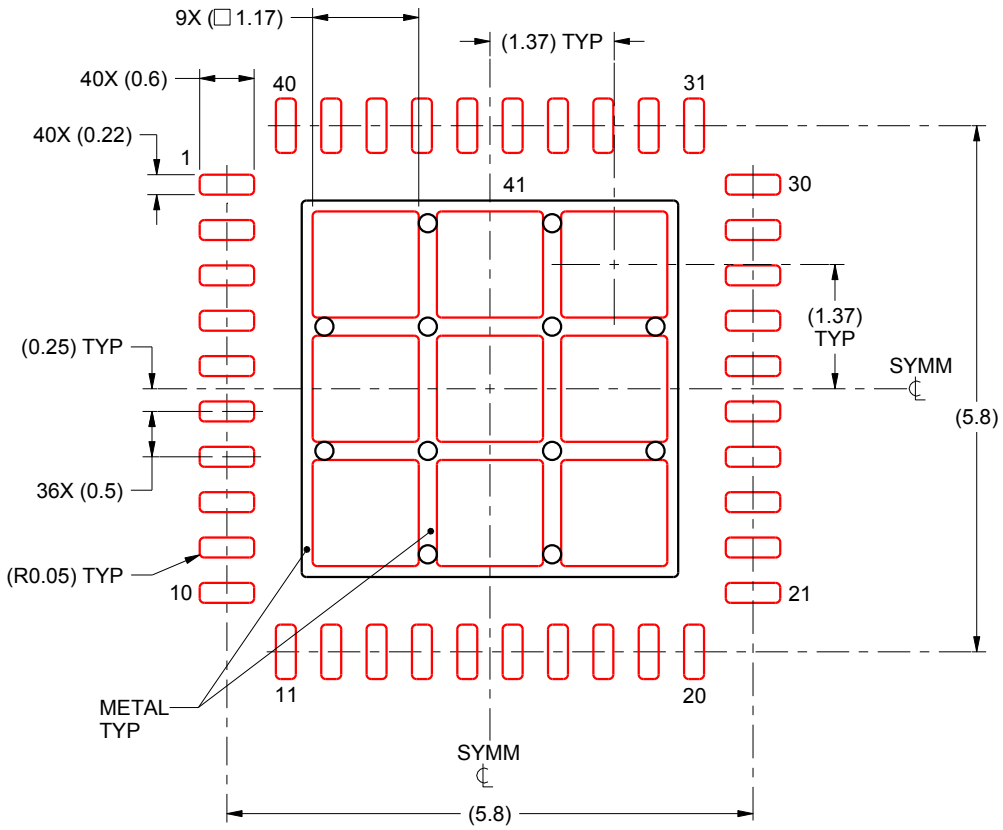


SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

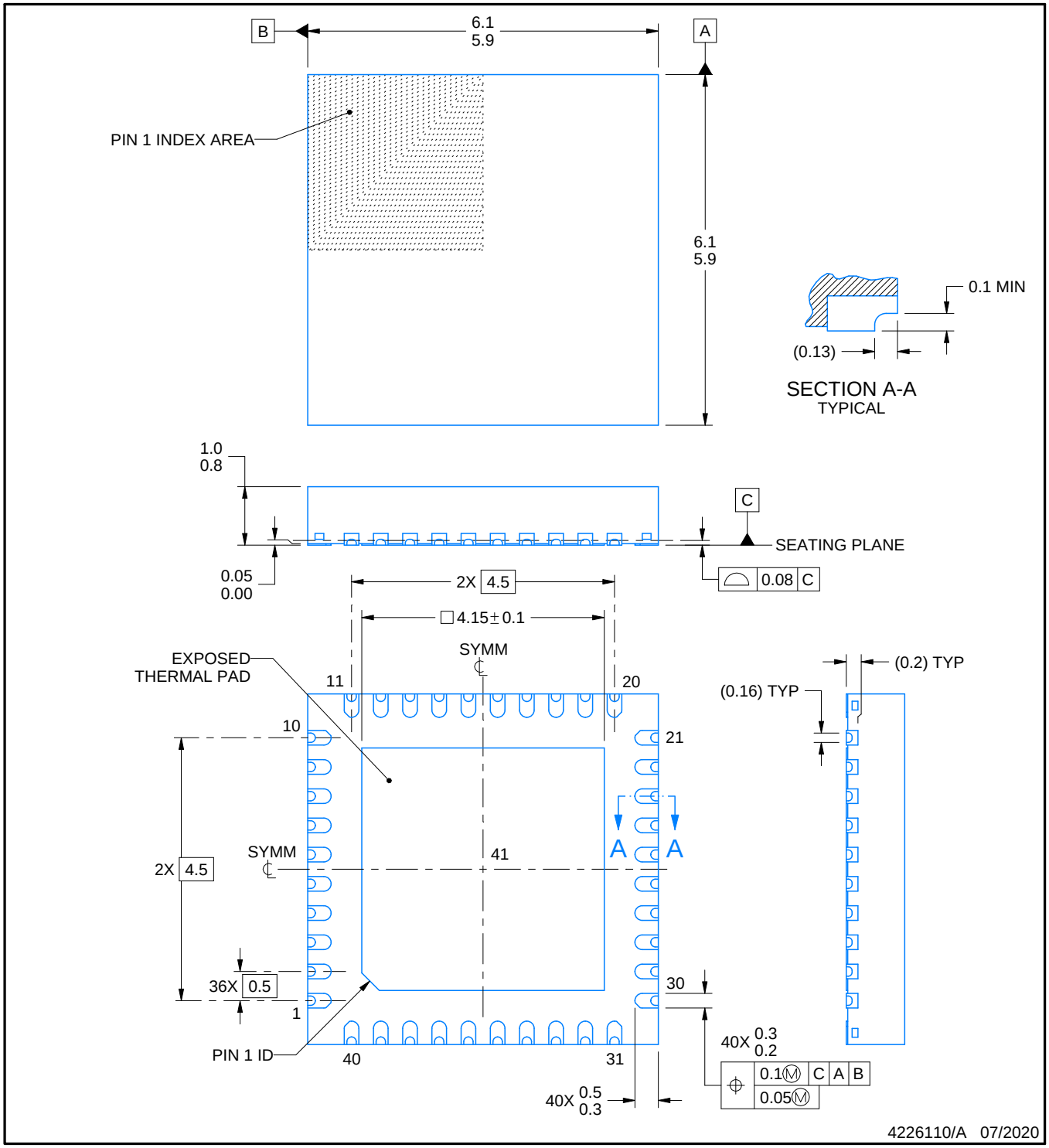
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHA0040M

PACKAGE OUTLINE

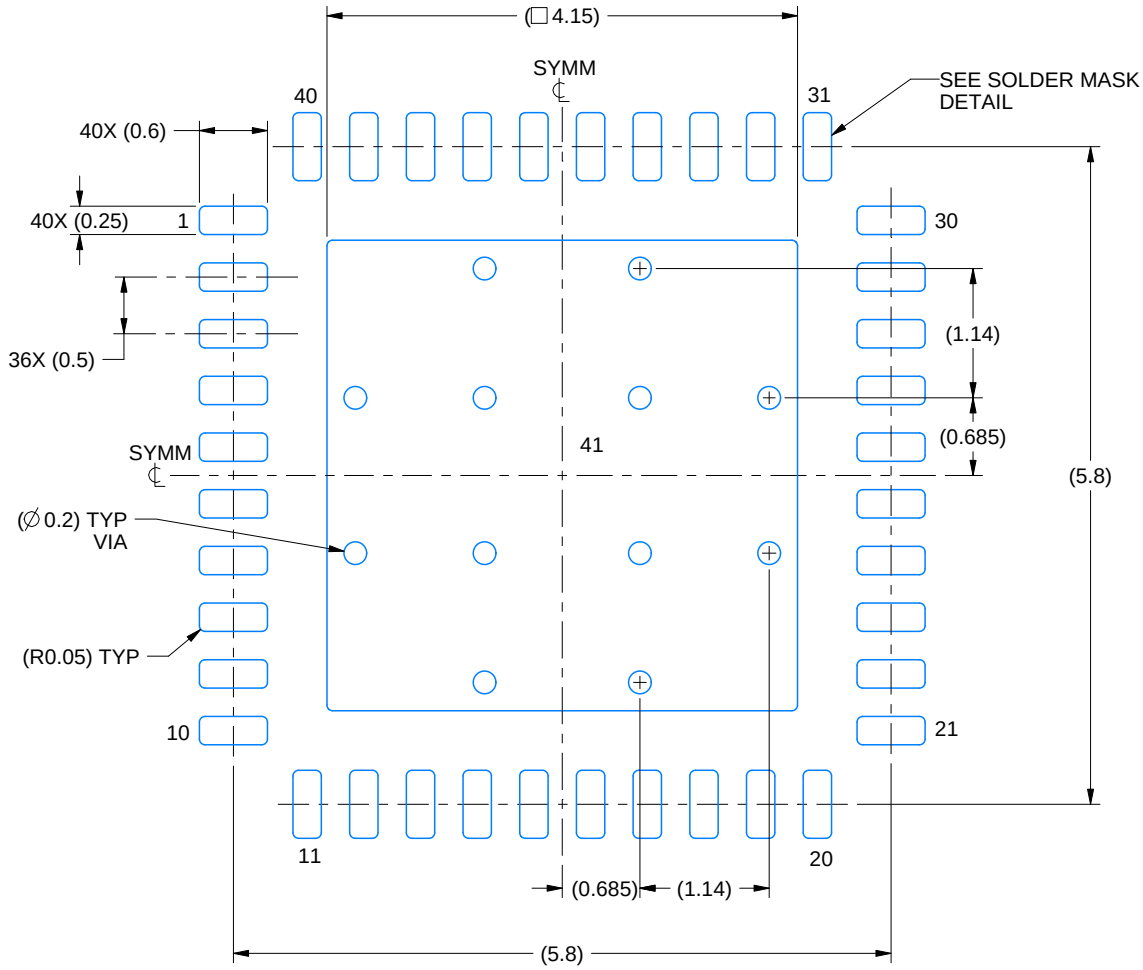
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

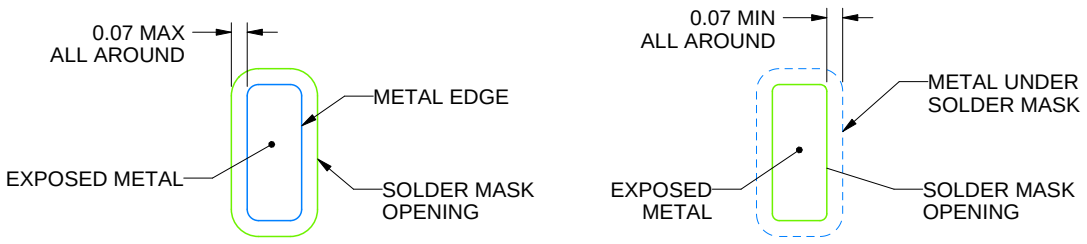


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

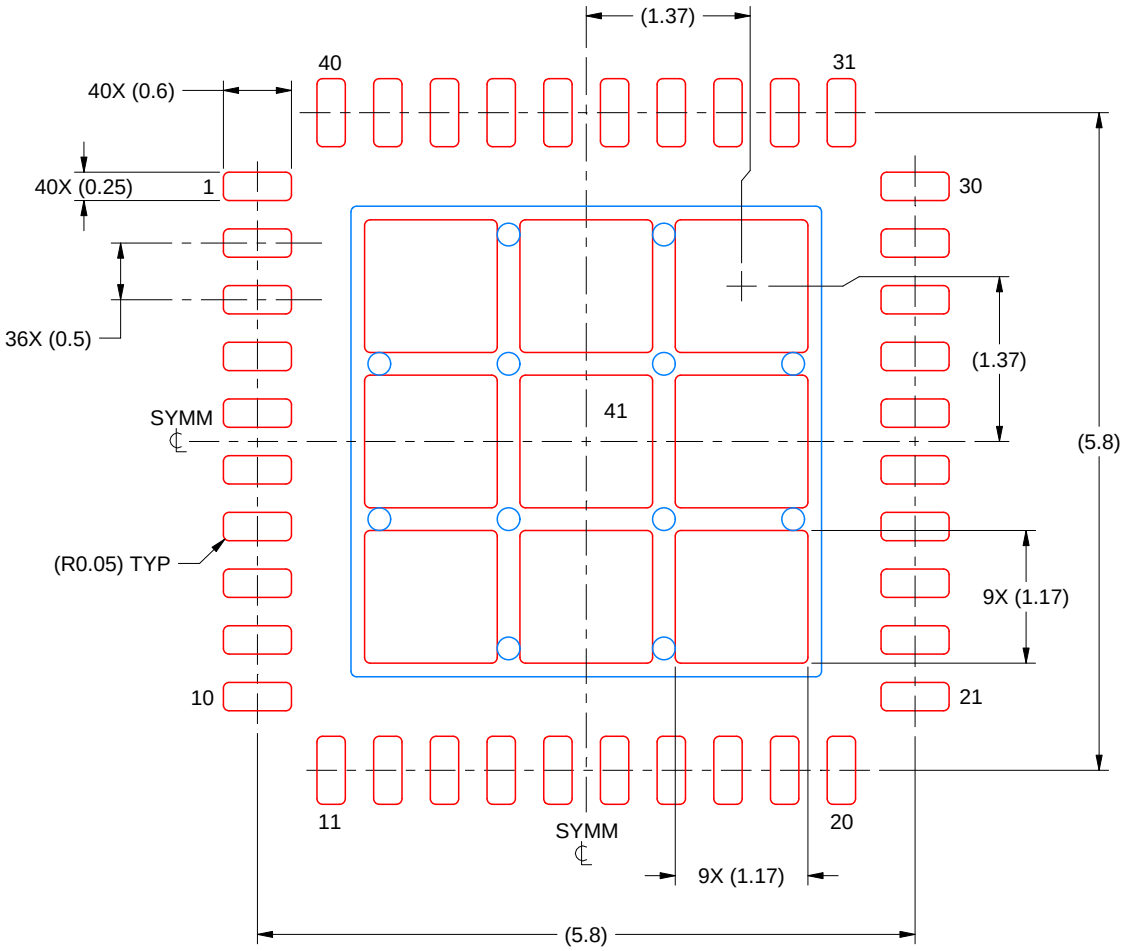
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226110/A 07/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226110/A 07/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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