TPS3123 Ultra-Low Voltage Processor Supervisory Circuits

1 Features

- Minimum supply voltage of 0.75 V
- Supply voltage supervision range:
  - 1.2 V, 1.5 V, 1.8 V (TPS312x)
  - 3 V (TPS3125 devices only)
  - Other versions on request
- Power-on reset generator with fixed delay time of 180 ms
- Manual reset input (TPS3123/5/6/8)
- Watchdog timer retriggers the $\overline{\text{RESET}}$ output at $V_{DD} \geq V_{IT}$
- Supply current of 14 µA (Typ)
- Small SOT23-5 package
- Temperature range of –40°C to +85°C
- Reset output available in Push-Pull (Active Low and High) and Open-Drain (Active-Low)

2 Applications

- Portable / battery-powered equipment
- Wireless communication systems
- Factory automation
- Servers
- Building automation

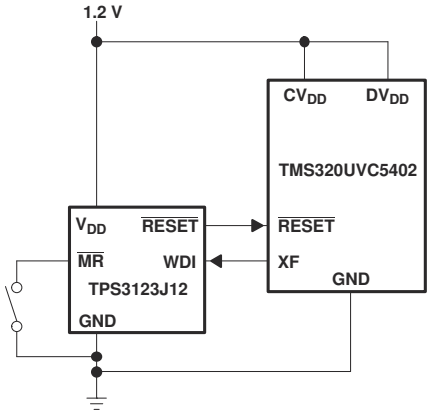
3 Description

The TPS312x family of voltage supervisory circuits provides voltage monitoring down to 1.2V rails and timing supervision, primarily for DSP and processor-based systems. All devices in the family monitor the power rail and assert $\overline{\text{RESET}}$ output when the power rail is under the threshold voltage target (V_{IT-}). The threshold voltage is programmed into the device to minimize external components. Built-in hysteresis prevents false triggering. The $\overline{\text{RESET}}$ output is not valid for supply voltage (V_{DD}) under 0.75 V. The TPS312x family includes devices with active high output for use as disable during malfunction and active low outputs for most systems where high output indicates properly functioning system.

The TPS3123/3124/3128 also include the watchdog timer functionality to monitor timely digital pulses from the processor and issue an alert if the expected pulse does not arrive on time due to potential software freeze or hang. Such integration of supply rail monitoring and the watch dog timer feature is very helpful in always on systems, such as Factory Automation and Communications Infrastructure.

In addition the TPS3123/5/6/8 devices incorporate a manual reset input, MR, to force RESET triggered by an event unrelated to the voltage rail monitoring of the pulses monitored by the watch dog timer. A low level at MR causes RESET to become active. The TPS3124 devices do not have the input MR, but include a high-level output RESET same as the TPS3125 and TPS3126 devices.

All devices in the family are available in a 5-pin SOT23-5 package and are characterized for operation over a temperature range of –40°C to +85°C.



Typical Low-Voltage DSP Application

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2011) to Revision F (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the description to highlight benefits of the key features	1
• Moved table of the details on package, threshold and top mark to the device and documentation support section in the back, leaving only the nomenclature and the topology summary here in this device comparison table section	3
• Moved pin out figures from first page to this new pin configuration section and added pin function table	4
• Added this missing section on ESD ratings	5
• Moved Timing Diagrams to section of their own and added legend for the letters on the diagrams	8
• Moved and updated device overview, block diagram and function mode table to this newly created section and added subsections for detailed feature descriptions for MR, output topology (active high/low, push-pull/ open-drain and watchdog timer)	12

Changes from Revision D (December 2006) to Revision E (August 2011)	Page
• Removed *TPS3128E12DBVR* from list of orderable devices in Section 5	3

5 Device Comparison

Figure 5-1 shows the device naming nomenclature to compare the different device variants. See Section 9 for ordering information on various variants of TPS3123/3124/3125/3126/ and TPS3128.

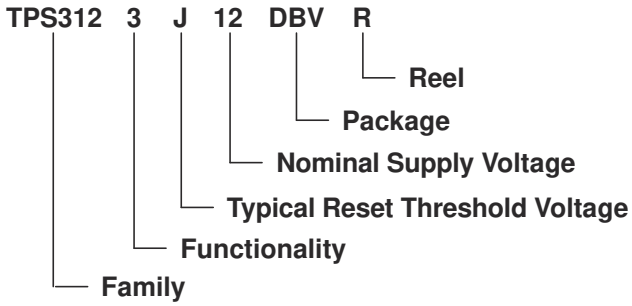


Figure 5-1. Device Naming Nomenclature

Table 5-1. Reset Output Topologies

DEVICES	OPEN DRAIN	PUSH-PULL
TPS3123		X
TPS3124		X
TPS3125		X
TPS3126	X	
TPS3128	X	

6 Pin Configuration and Functions

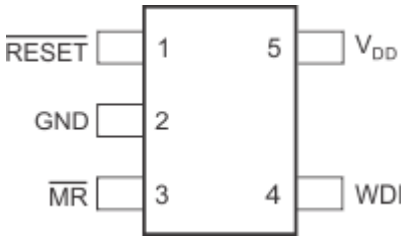


Figure 6-1. TPS3123 / TPS3128: DBV PACKAGE 5-Pin SOT-23 Top View

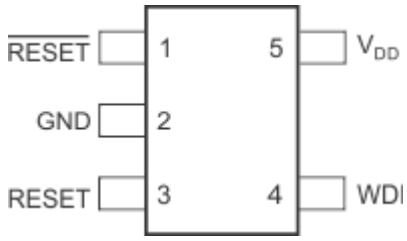


Figure 6-2. TPS3124: DBV PACKAGE 5-Pin SOT-23 Top View

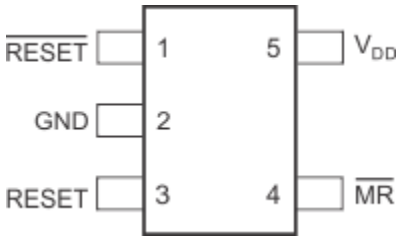


Figure 6-3. TPS3125 / TPS3126: DBV PACKAGE 5-Pin SOT-23 Top View

Table 6-1. Pin Functions

PIN				I/O	DESCRIPTION
PIN NUMBER	TPS3123 TPS3128	TPS3124	TPS3125 TPS3126		
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	O	**Active-Low Output Reset Signal:** This pin is driven to a logic low when VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.
2	GND	GND	GND	-	**GROUND**
3	$\overline{\text{MR}}$	-	-	I	**Manual Reset:** Pull this pin to a logic low to assert a reset signal in the $\overline{\text{RESET}}$ output pin. After $\overline{\text{MR}}$ pin is left floating or pulls to logic high, the $\overline{\text{RESET}}$ output deasserts to the nominal state after the reset delay time (t_D) expires.
3	-	RESET	RESET	O	**Active-High Output Reset Signal:** This pin is driven to a logic high when VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.
4	WDI	WDI	$\overline{\text{MR}}$	I	**Watchdog timer input:** If WDI remains high or low longer than the timeout period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge. If unused, the WDI connection must be high impedance to prevent it from causing a reset event.
5	VDD	VDD	VDD	I	**Input Supply Voltage:** Supply voltage pin. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
	Manual reset, $\overline{MR}$	–0.3 V to V_{DD} + 0.6 V
	$\overline{RESET}$	–0.3 V to V_{DD} + 0.6 V
V_{DD}	Supply voltage	3.6 V
WDI	Watchdog input	–0.3 V to V_{DD} + 0.6 V
I_{OL}	Maximum low output current	5 mA
I_{OH}	Maximum high output current	–5 mA
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{DD})	±10 mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{DD})	±10 mA
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range,	–40°C to +85°C
T_{stg}	Storage temperature range,	–65°C to +150°C
	Soldering temperature	+260°C
	Open drain RESET outputs	–0.3 V to V_{DD} + 0.3 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings for TPS3123

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

at specified temperature range.

			MIN	MAX	UNIT
V_{DD}	Supply voltage	T_A = 0°C to +85°C	0.75	3.3	V
		T_A = –40°C to +85°C	0.85	3.3	
V_{DD}	Manual reset voltage		0.0	V_{DD} +0.3	V
V_{WD1}	Watchdog input voltage		0	V_{DD} +0.3	V
V_{IH}	High-level input voltage		0.7×V_{DD}		V
V_{IL}	Low-level input voltage			0.3×V_{DD}	V
Δ t/ΔV	Input transition rise and fall rate at WDI			1	µs/V
T_A	Operating free-air temperature range		40	+85	°C

7.4 Dissipation Rating Table

PACKAGE	T_A ≤ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\overline{MR}}$	$\overline{MR}$ pullup resistor (internal)					27		kΩ
I_{IH}	High-level input current	WDI	WDI = V_{DD} = 3.3 V		1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD},	V_{DD} = 3.3 V	20		55	
I_{IL}	Low-level input current	WDI	WDI = 0 V,	V_{DD} = 3.3 V	1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0 V,	V_{DD} = 3.3 V	80		170	
I_{OH}	High-level output current (leakage into $\overline{RESET}$ pin)	TPS3126-xx, TPS3128-xx	V_{DD} = V_{OH} = 3.3 V				200	nA
V_{OH}	High-level output voltage (TPS3123/4/5 only)	$\overline{RESET}$	V_{DD} = 1.5 V,	I_{OH} = –1 mA	0.8×V_{DD}			V
			V_{DD} = 3.3 V,	I_{OH} = –4.5 mA				
		RESET	V_{DD} = 0.75 V,	I_{OH} = –8 µA				
			V_{DD} = 1.5 V,	I_{OH} = –1 mA				
V_{OL}	Low-level output voltage	$\overline{RESET}$	V_{DD} = 0.75 V,	I_{OL} = 15 µA			0.2 × V_{DD}	V
			V_{DD} = 1.5 V,	I_{OL} = 1.4 mA				
		RESET	V_{DD} = 1.5 V,	I_{OL} = 1.4 mA				
			V_{DD} = 3.3 V,	I_{OL} = 3 mA			0.4	
$V_{IT–}$	Negative-going input threshold voltage (1)	TPS312xJ12	T_A = –40°C to +85°C		1.04	1.08	1.12	V
		TPS312xG15			1.35	1.40	1.45	
		TPS312xJ18			1.56	1.62	1.68	
		TPS312xL30			2.57	2.64	2.71	
		TPS312xE12			1.10	1.14	1.18	
		TPS312xE15			1.38	1.43	1.48	
		TPS312xE18			1.65	1.71	1.77	
V_{HYS}	Hysteresis at V_{DD} input		1 V < $V_{IT–}$ < 1.4 V			15		mV
			1.4 V < $V_{IT–}$ < 2 V			20		
			2 V < $V_{IT–}$ < 3 V			30		
I_{DD}	Supply current	TPS3123-xx TPS3124-xx TPS3128-xx	WDI = V_{DD}, $\overline{MR}$ unconnected	V_{DD} = 0.75 V		14		µA
				V_{DD} = 3.3 V		22	30	
		TPS3125-xx TPS3126-xx (2)	$\overline{MR}$ unconnected	V_{DD} = 0.75 V		14		
				V_{DD} = 3.3 V		18	25	
C_i	Input capacitance at $\overline{MR}$, WDI		V_I = 0 V to 3.3 V			5		pF

(1) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
(2) The supply current during delay time t_d is typical 5 µA higher.

7.6 Timing Requirements

at R_L = 1 MΩ, C_L = 50 pF, T_A = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w Pulse width	At V_{DD}	$V_{IH} = V_{IT-} + 0.2$ V, $V_{IL} = V_{IT-} - 0.2$ V	6			µs
	At $\overline{MR}$	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1			
	At WDI		0.1			

7.7 Switching Characteristics

at R_L = 1 MΩ, C_L = 50 pF, T_A = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{tout}	Watchdog time out		$V_{DD} \geq V_{IT-} + 0.2$ V, See timing diagram	0.8	1.4	2.1	s
t_d	Delay time		$V_{DD} > V_{IT-} + 0.2$ V, See timing diagram	100	180	260	ms
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3123/5/6/8)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.8 \times V_{DD}$			0.1	µs
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3125/6)				0.1	
t_{PHL}	Propagation delay time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			10	µs
t_{PLH}	Propagation delay time, low-to-high-level output	V_{DD} to RESET delay (TPS3124/5/6)				10	

7.8 Timing Diagrams

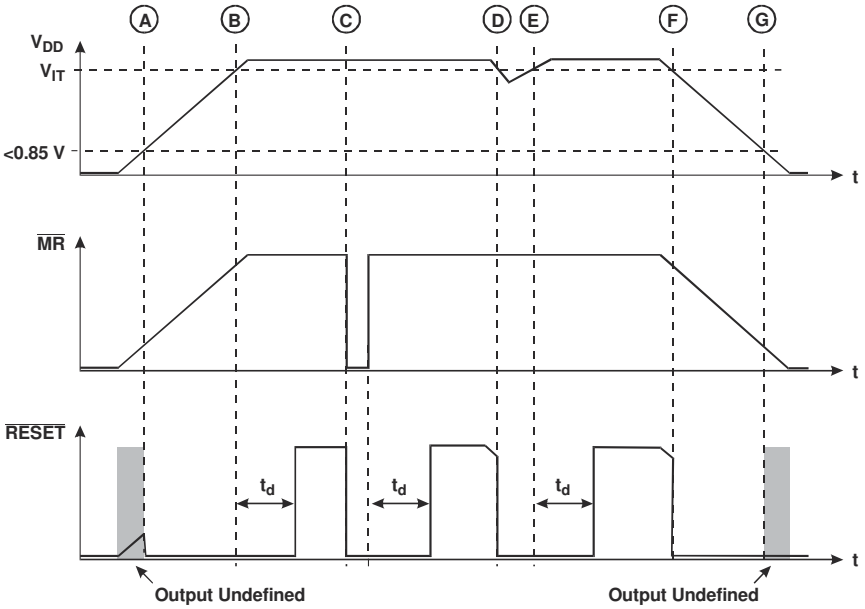


Figure 7-1. Timing Diagram TPS3123/5/6/8

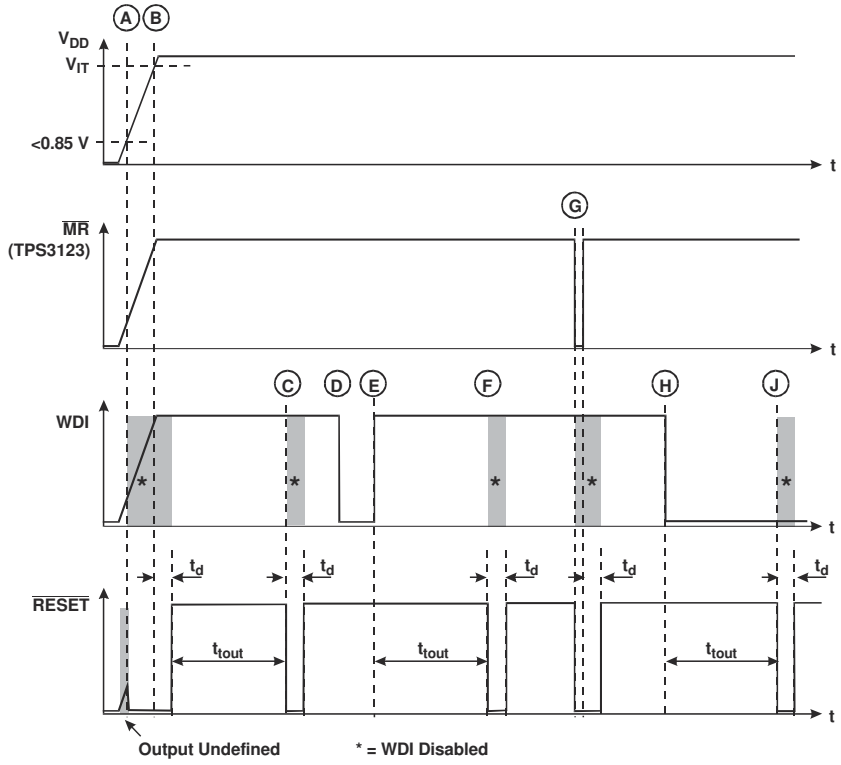


Figure 7-2. Timing Diagram TPS3123/4/8

Note

A=Min VDD, B=VDD threshold, C,F,J=Watch Dog timeout, D,E,H=Watch Dog retriggered, G=Manual Reset

7.9 Typical Characteristics

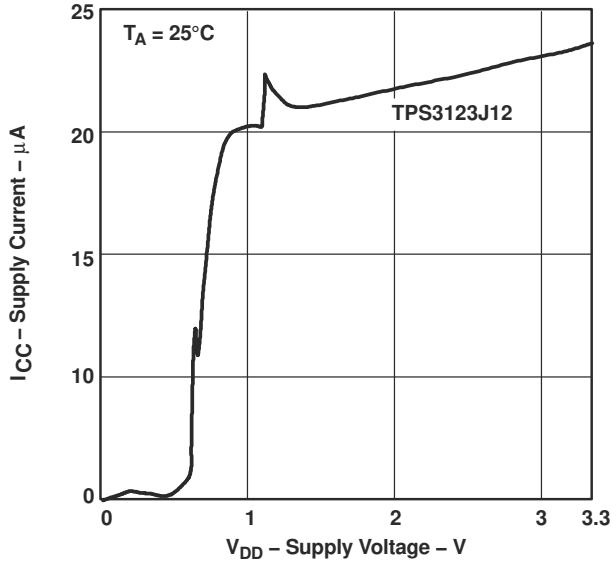


Figure 7-3. SUPPLY CURRENT vs SUPPLY VOLTAGE

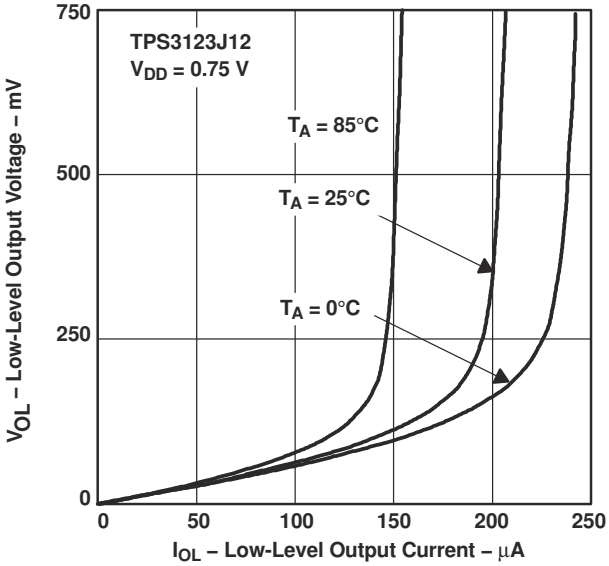


Figure 7-4. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

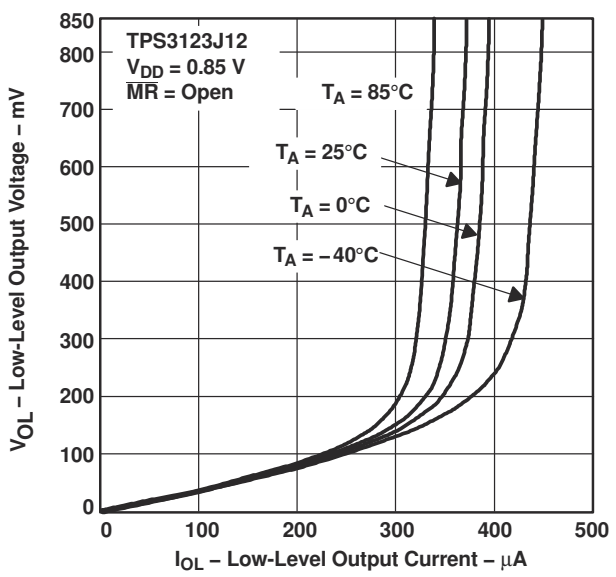


Figure 7-5. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

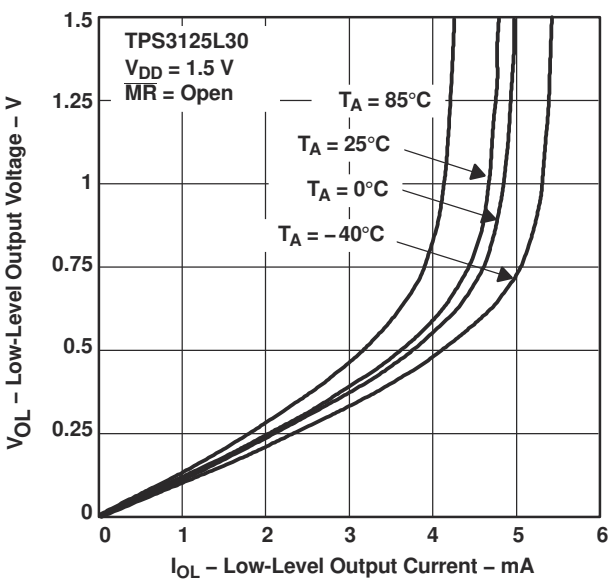


Figure 7-6. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

7.9 Typical Characteristics (continued)

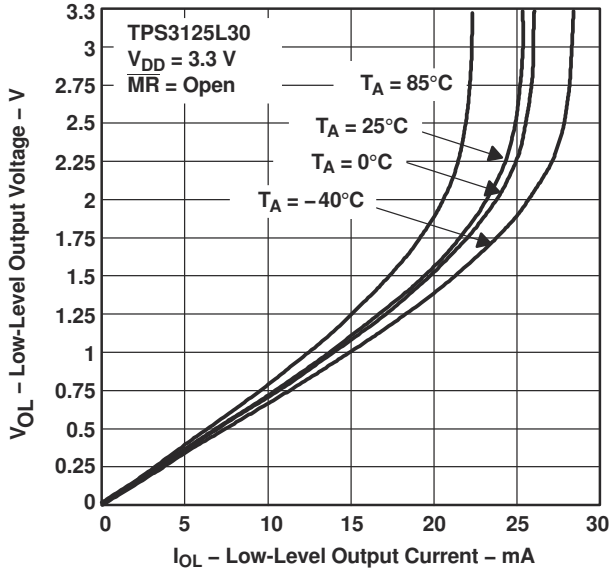


Figure 7-7. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

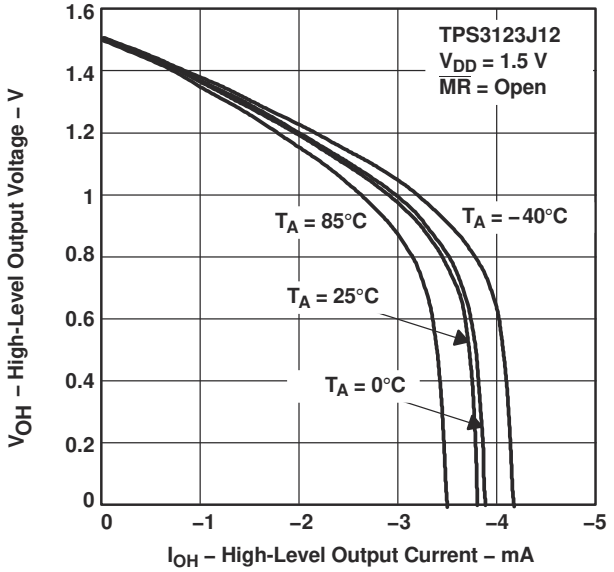


Figure 7-8. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

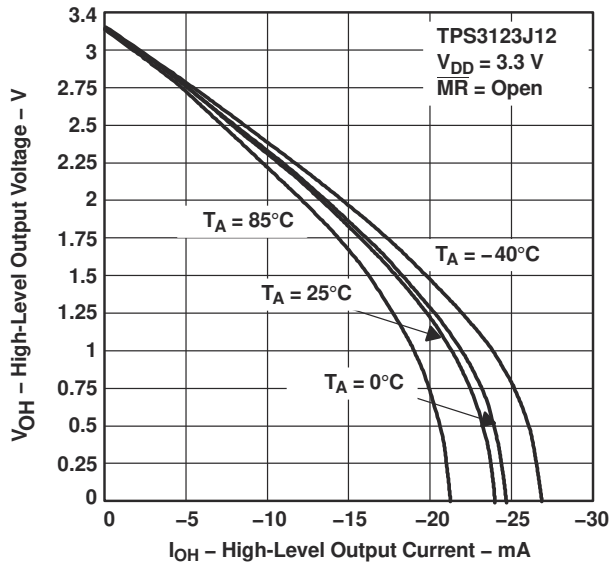


Figure 7-9. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

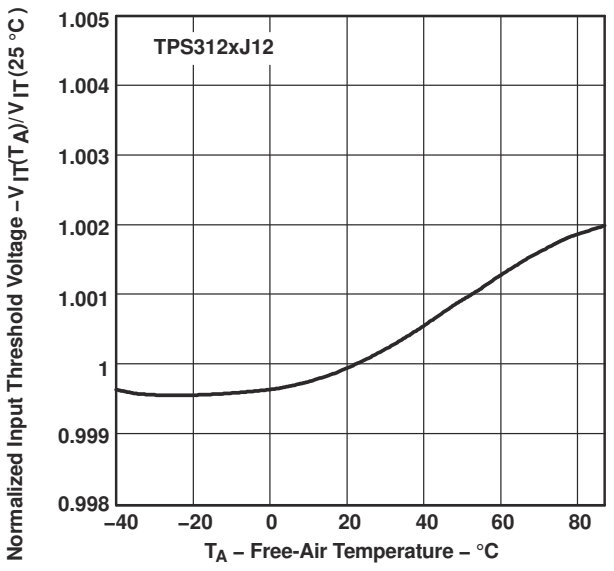


Figure 7-10. NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

7.9 Typical Characteristics (continued)

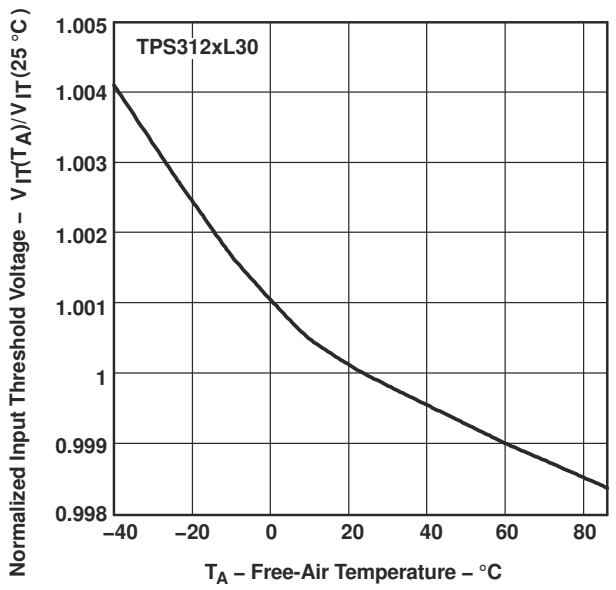


Figure 7-11. NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

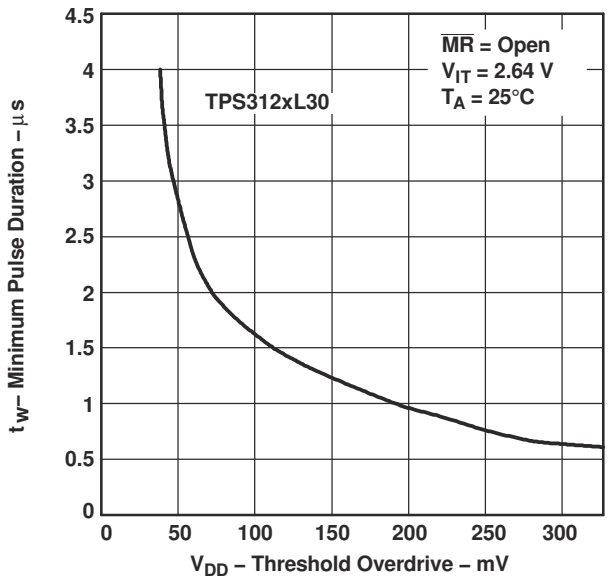


Figure 7-12. MINIMUM PULSE DURATION vs THRESHOLD OVERDRIVE

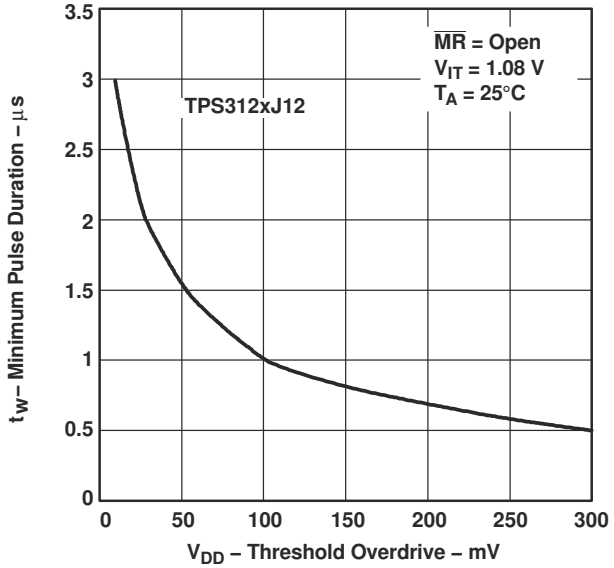


Figure 7-13. MINIMUM PULSE DURATION vs THRESHOLD OVERDRIVE

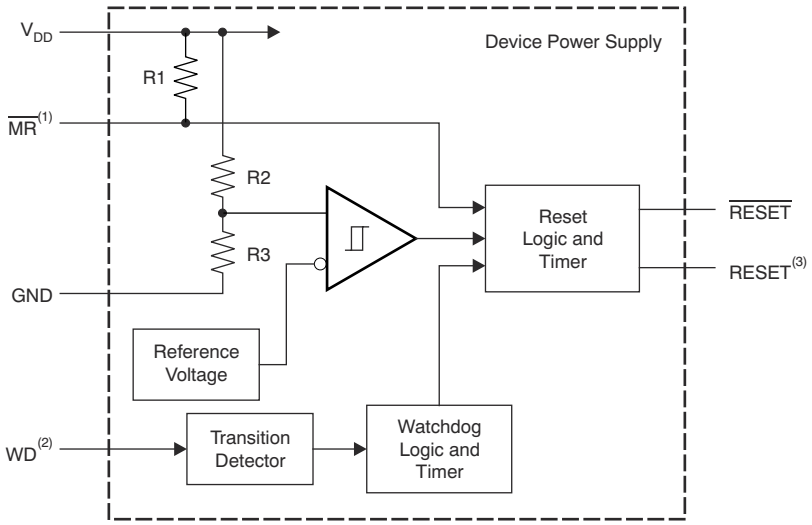
8 Detailed Description

8.1 Overview

The TPS312x family of supervisors provide circuit initialization and timing supervision. Optional configurations include devices with active-high and active-low output signals (TPS3124/3125/3126), devices with a watchdog timer (TPS3123/3124/3128), and devices with manual reset ($\overline{MR}$) pins (TPS3123/3125/3126/3128). $\overline{RESET}$ output is valid when the supply voltage, V_{DD}, is above 0.75 V. For devices with active-low output logic, the device monitors V_{DD} and keeps $\overline{RESET}$ low as long as V_{DD} remains below the negative threshold voltage, V_{IT-}. For devices with active-high output logic, RESET remains high as long as V_{DD} remains below V_{IT-}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d, starts after V_{DD} rises above the positive threshold voltage ($V_{IT-} + V_{HYS}$). When the supply voltage drops below V_{IT-}, the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage, V_{IT-}, set by an internal voltage divider, so no external components are required.

The TPS312x family is designed to monitor voltages listed on Table 9-2. For devices with the manual reset functionality, a low level at $\overline{MR}$ causes $\overline{RESET}$ to become active. For devices with the watch dog timer functionality, when the supervising system fails to retrigger the watchdog circuit within the time-out interval t_{tout} = 0.8 s, $\overline{RESET}$ output becomes active for the time period (t_d). This event also reinitializes the watchdog timer. The devices are available in a 5-pin SOT-23 package and are characterized for operation over a temperature range of −40°C to 85°C.

8.2 Functional Block Diagram



NOTES:
(1) TPS3123/5/6/8
(2) TPS3123/4/8
(3) TPS3124/5/6

Figure 8-1. FUNCTIONAL BLOCK DIAGRAM

8.3 Feature Description

8.3.1 Manual Reset ($\overline{MR}$)

The $\overline{MR}$ input allows an external logic signal from processors, logic circuits, and/or discrete sensors to force a reset signal regardless of V_{DD} with respect to V_{IT-} or the state of the watchdog timer. A low level at $\overline{MR}$ causes the reset signals to become active.

8.3.2 Active-High or Active-Low Output

All TPS312x devices have an active-low logic output ($\overline{\text{RESET}}$), while the TPS3124/3125/3126 devices also include an active-high logic output (RESET).

8.3.3 Push-Pull or Open-Drain Output

All TPS312x devices, except for TPS3126/3128, have push-pull outputs. TPS3126/3128 devices have an open-drain output.

8.3.4 Watchdog Timer (WDI)

The TPS3123, TPS3124, and TPS3128 devices have a watchdog timer that must be periodically triggered by either a positive or negative transition at WDI to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{\text{RESET}}$ becomes active for the time period t_d. This event also reinitializes the watchdog timer.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the TPS312x devices.

Table 8-1. Device Functional Modes Table

TPS3123/8			TPS3124			TPS3125/6			
$\overline{\text{MR}}$	VDD > V_{IT}	$\overline{\text{RESET}}$	VDD > V_{IT}	$\overline{\text{RESET}}$	RESET	$\overline{\text{MR}}$	VDD > V_{IT}	$\overline{\text{RESET}}$	RESET
L	0	L	0	L	H	L	0	L	H
L	1	L	1	H	L	L	1	L	H
H	0	L				H	0	L	H
H	1	H				H	1	H	L

9 Device and Documentation Support

Table 9-1. Ordering Information Application Specific Versions (1)

DEVICE NAME	NOMINAL SUPPLY VOLTAGE, V_{NOM}	DEVICE NAME	TYPICAL RESET THRESHOLD VOLTAGE–V_{IT-}
TPS312xx12DBV	1.2 V	TPS312xAxxDBV	V_{NOM} –1%
TPS312xx15DBV	1.5 V	TPS312xBxxDBV	V_{NOM} –2%
TPS312xx18DBV	1.8 V	TPS312xCxxDBV	V_{NOM} –3%
TPS312xx30DBV	3.0 V	TPS312xDxxDBV	V_{NOM} –4%
		TPS312xExxDBV	V_{NOM} –5%
		TPS312xFxxDBV	V_{NOM} –6%
		TPS312xGxxDBV	V_{NOM} –7%
		TPS312xHxxDBV	V_{NOM} –8%
		TPS312xIxxDBV	V_{NOM} –9%
		TPS312xJxxDBV	V_{NOM} –10%
		TPS312xKxxDBV	V_{NOM} –11%
		TPS312xLxxDBV	V_{NOM} –12%
		TPS312xMxxDBV	V_{NOM} –13%
		TPS312xNxxDBV	V_{NOM} –14%
		TPS312xOxxDBV	V_{NOM} –15%

1. For the application-specific versions contact Texas Instruments for availability, lead time, and minimum order quantities.

Table 9-2. Package Information, Standard Versions(1) (2)

T_A	DEVICE NAME		THRESHOLD VOLTAGE	MARKING
-40°C to +85°C	TPS3123J12DBVR(3)	TPS3123J12DBVT(4)	1.08 V	PBNI
	TPS3123G15DBVR(3)	TPS3123G15DBVT(4)	1.40 V	PBOI
	TPS3123J18DBVR(3)	TPS3123J18DBVT(4)	1.62 V	PBPI
	TPS3124J12DBVR(3)	TPS3124J12DBVT(4)	1.08 V	PBQI
	TPS3124G15DBVR(3)	TPS3124G15DBVT(4)	1.40 V	PBRI
	TPS3124J18DBVR(3)	TPS3124J18DBVT(4)	1.62 V	PBSI
	TPS3125J12DBVR(3)	TPS3125J12DBVT(4)	1.08 V	PBTI
	TPS3125G15DBVR(3)	TPS3125G15DBVT(4)	1.40 V	PBUI
	TPS3125J18DBVR(3)	TPS3125J18DBVT(4)	1.62 V	PBVI
	TPS3125L30DBVR(3)	TPS3125L30DBVT(4)	2.64 V	PBXI
	TPS3126E12DBVR(3)	TPS3126E12DBVT(4)	1.14 V	PFOI
	TPS3126E15DBVR(3)	TPS3126E15DBVT(4)	1.43 V	PFPI
	TPS3126E18DBVR(3)	TPS3126E18DBVT(4)	1.71 V	PFQI
	TPS3128E15DBVR(3)	TPS3128E15DBVT(4)	1.43 V	PFSI
	TPS3128E18DBVR(3)	TPS3128E18DBVT(4)	1.71 V	PFTI

1. Other versions available. Contact Texas Instruments for details; minimum order quantities apply.
2. For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
3. The DBVR passive indicates tape and reel of 3000 parts.
4. The DBVT passive indicates tape and reel of 250 parts.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3123J12DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBNI	Samples
TPS3123J18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBPI	Samples
TPS3124G15DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBRI	Samples
TPS3124J12DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBQI	Samples
TPS3124J18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBSI	Samples
TPS3125G15DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBUI	Samples
TPS3125J12DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBTI	Samples
TPS3125J18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBVI	Samples
TPS3125L30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBXI	Samples
TPS3126E12DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFOI	Samples
TPS3126E15DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFPI	Samples
TPS3126E18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFQI	Samples
TPS3128E12DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFRI	Samples
TPS3128E15DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFSI	Samples
TPS3128E18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFTI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

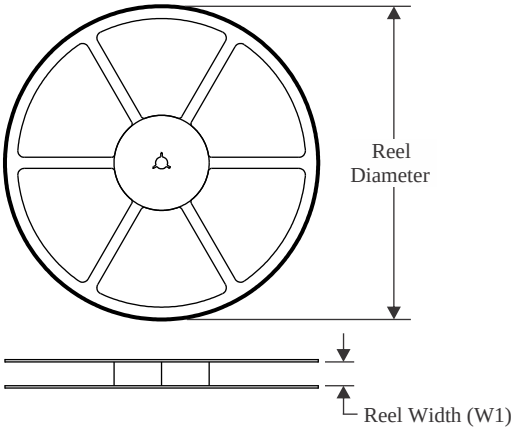
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

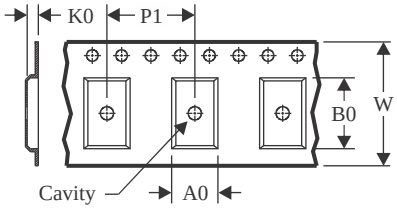
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

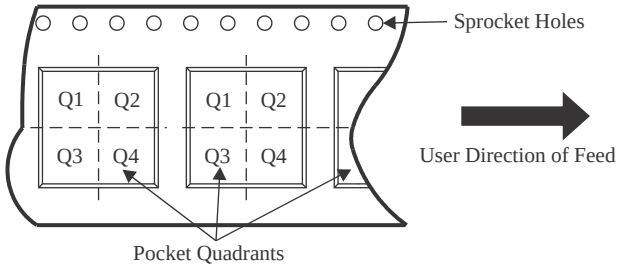


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

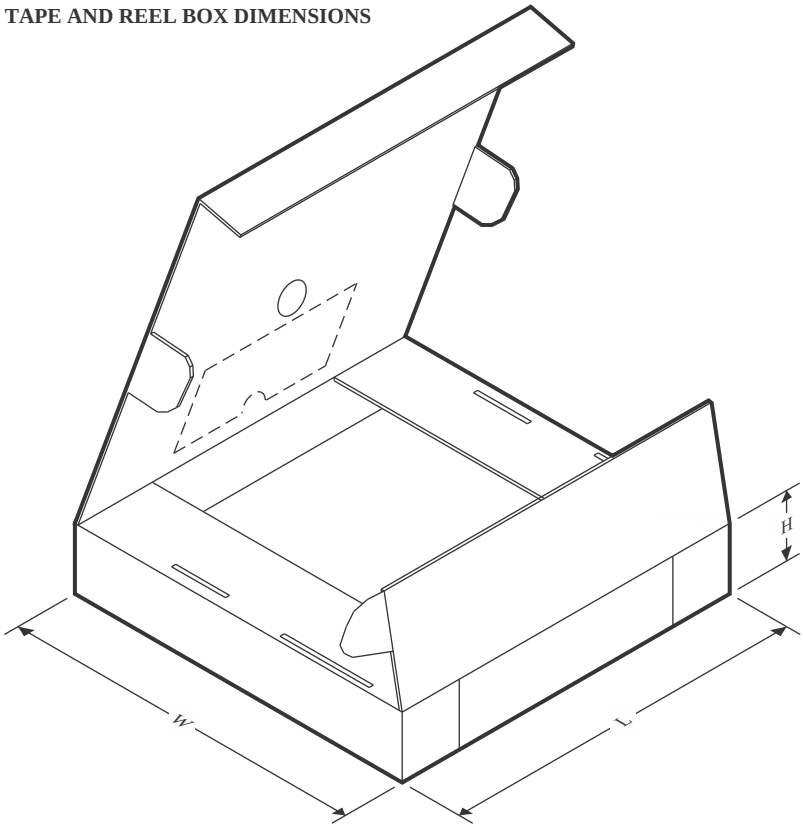
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3123J12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3123J18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3124G15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3124J12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3124J18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125G15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125J12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125J18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125L30DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3126E12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3126E15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3126E18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3128E12DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3128E15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3128E18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

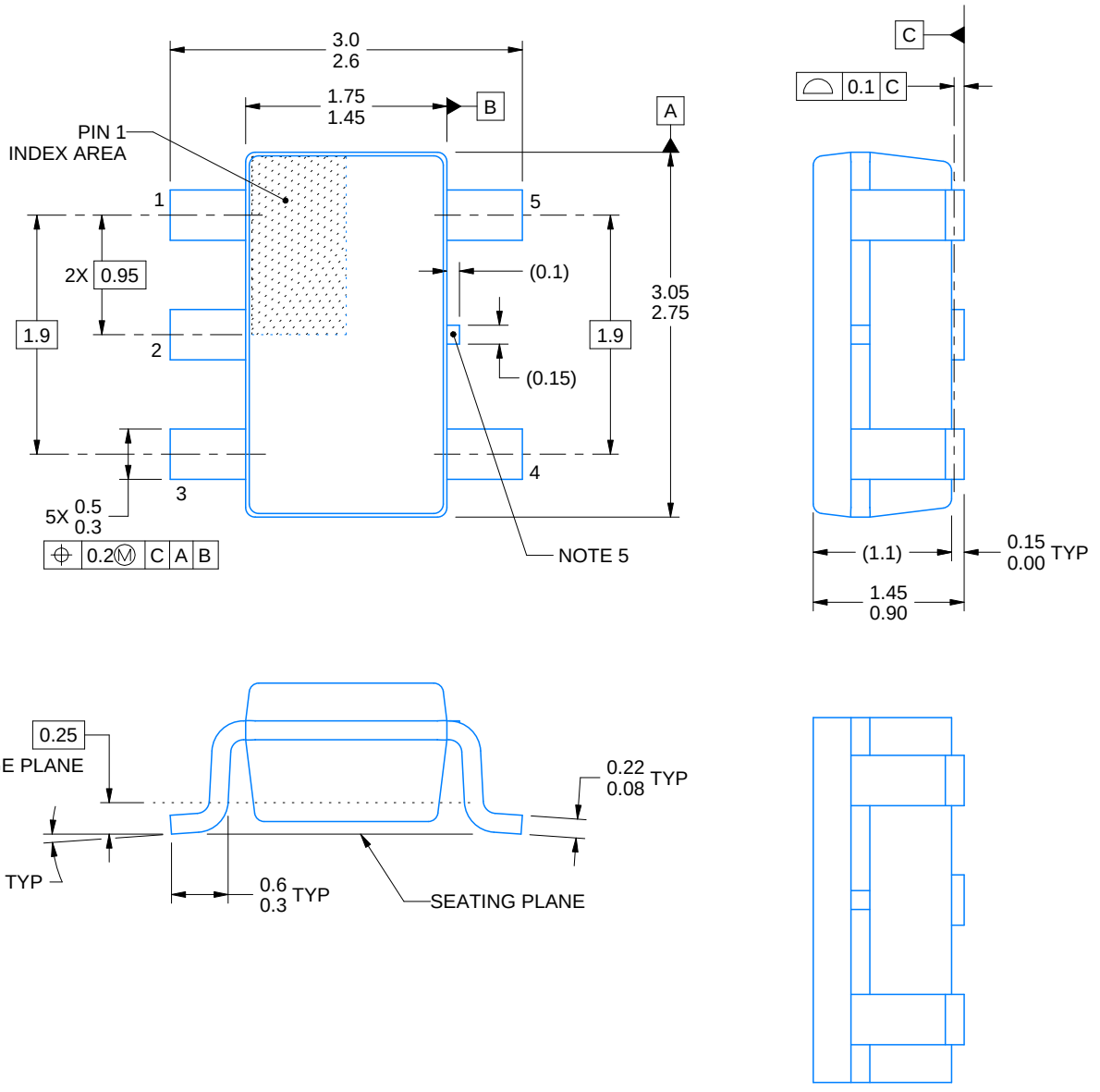
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3123J12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3123J18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3124G15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3124J12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3124J18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125G15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125J12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125J18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125L30DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3126E12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3126E15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3126E18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3128E12DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TPS3128E15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3128E18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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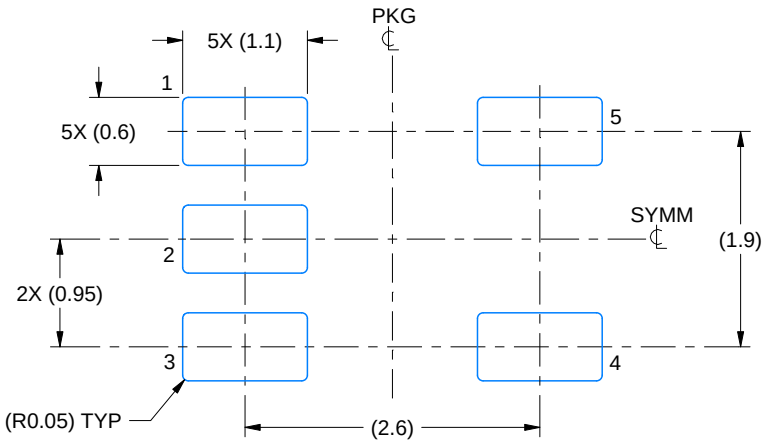
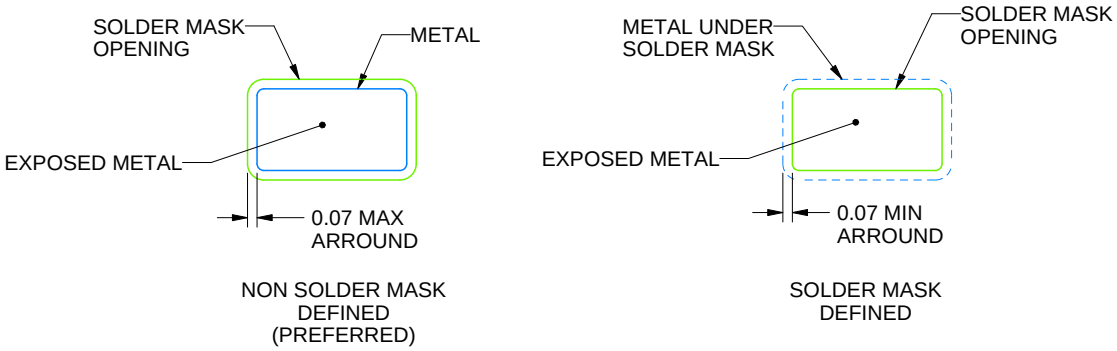
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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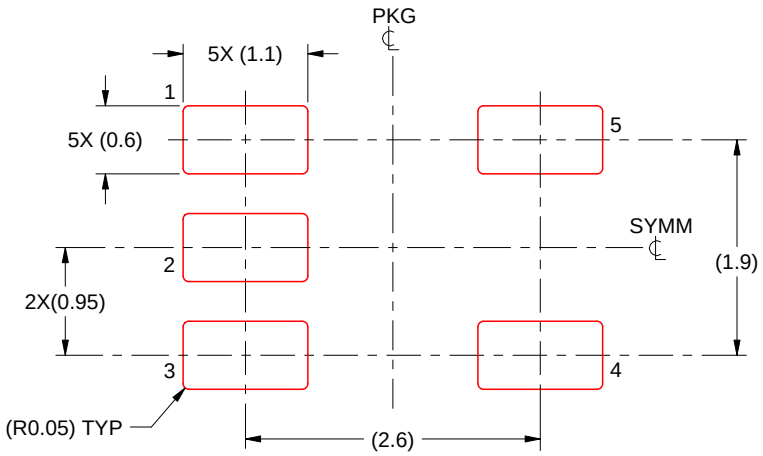
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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