# TPS36-Q1 車載用 Nano IQ 高精度電圧監視回路、高精度ウィンドウ・ウォッチドッグ・タイマ付き

## 1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～125℃
- 工場出荷時にプログラム済みまたはユーザーがプログラム可能なウォッチドッグ・タイムアウト
  - ±10% 精度のタイマ (最大値)
  - 工場出荷時にプログラム済みのクローズ・ウィンドウ:1msec～100sec
- 工場出荷時にプログラム済みまたはユーザーがプログラム可能なリセット遅延
  - ±10% 精度のタイマ (最大値)
  - 工場出荷時にプログラム済みのオプション:2msec～10sec
- 入力電圧範囲:$V_{DD}$ = 1.04V～6.0V
- 固定スレッショルド電圧 ($V_{IT-}$):1.05V～5.4V
  - スレッショルド電圧は 50mV 刻みで利用可能
  - 1.2% の電圧スレッショルド精度 (最大値)
  - ヒステリシス内蔵 ($V_{HYS}$):5% (標準値)
- 超低電源電流:$I_{DD}$ = 250nA (標準値)
- オープン・ドレイン、プッシュプル、アクティブ Low 出力
- 各種のプログラマビリティ・オプション:
  - ウォッチドッグ・イネーブル / ディセーブル
  - ウォッチドッグ・スタートアップ遅延:遅延なし～10秒
  - オープン・ウィンドウとクローズ・ウィンドウの比率オプション:1 倍～511 倍
  - ラッチ付き出力オプション
- $\overline{MR}$ 機能のサポート

## 2 アプリケーション

- オンボード・チャージャ (OBC) およびワイヤレス・チャージャ
- ドライバー監視
- バッテリ管理システム (BMS)
- フロント・カメラ
- サラウンド・ビュー・システムの ECU

## 3 概要

TPS36-Q1 は、超低消費電力 (標準値 250nA) のデバイスであり、高精度電圧監視回路を備え、プログラム可能なウィンドウ・ウォッチドッグ・タイマを搭載しています。TPS36-Q1 は、低電圧監視のための広いスレッショルド・レベルをサポートしており、規定された温度範囲全体にわたって 1.2% の精度を達成しています。

TPS36-Q1 は、さまざまなアプリケーションに対応する多くの機能を備えた高精度ウィンドウ・ウォッチドッグ・タイマを提供します。クローズ・ウィンドウ・タイマは、工場出荷時にプログラムするか、または、外付けコンデンサを使用してユーザーがプログラムするか、いずれかが可能です。オープン・ウィンドウとクローズ・ウィンドウの比率は、ロジック・ピンの組み合わせを使用して動作中でも変更できます。また、このウォッチドッグは、イネーブル / ディセーブル、スタートアップ遅延、独立 WDO ピン・オプションなどの独自の機能も備えています。

$\overline{RESET}$ または $\overline{WDO}$ 遅延は、工場出荷時にプログラムされるデフォルトの遅延設定で設定するか、または外付けコンデンサでプログラムできます。また、このデバイスはラッチ付き出力動作も備えており、監視回路またはウォッチドッグのフォルトがクリアされるまで出力がラッチされます。

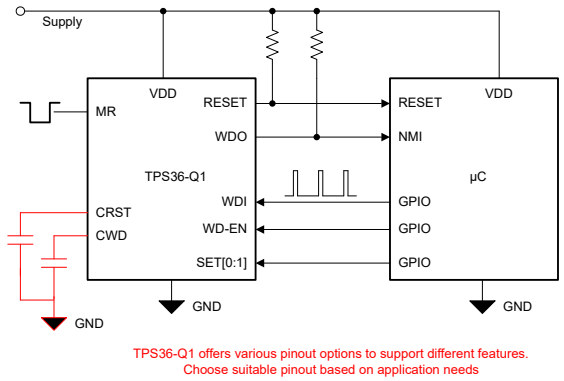
TPS36-Q1 は、TPS3852-Q1 デバイス・ファミリに代わる性能アップグレード製品です。TPS36-Q1 は、小型の 8 ピン SOT-23 パッケージで供給されます。

**製品情報**

| 部品番号 | パッケージ (1) | 本体サイズ (公称) |
|---|---|---|
| TPS36-Q1 | DDF (8) | 2.90mm × 1.60mm |

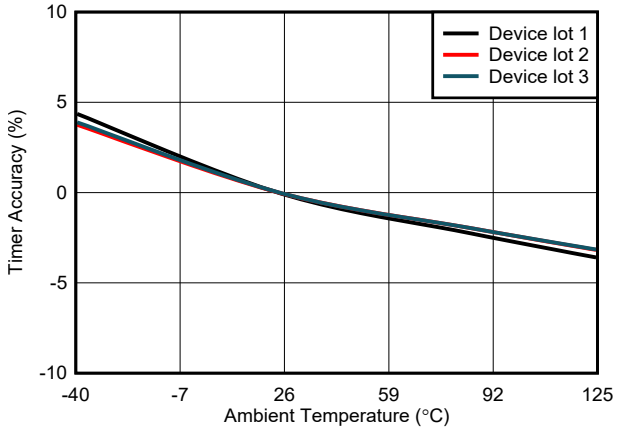
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。




TPS36-Q1 offers various pinout options to support different features.
Choose suitable pinout based on application needs

**代表的なアプリケーション回路**





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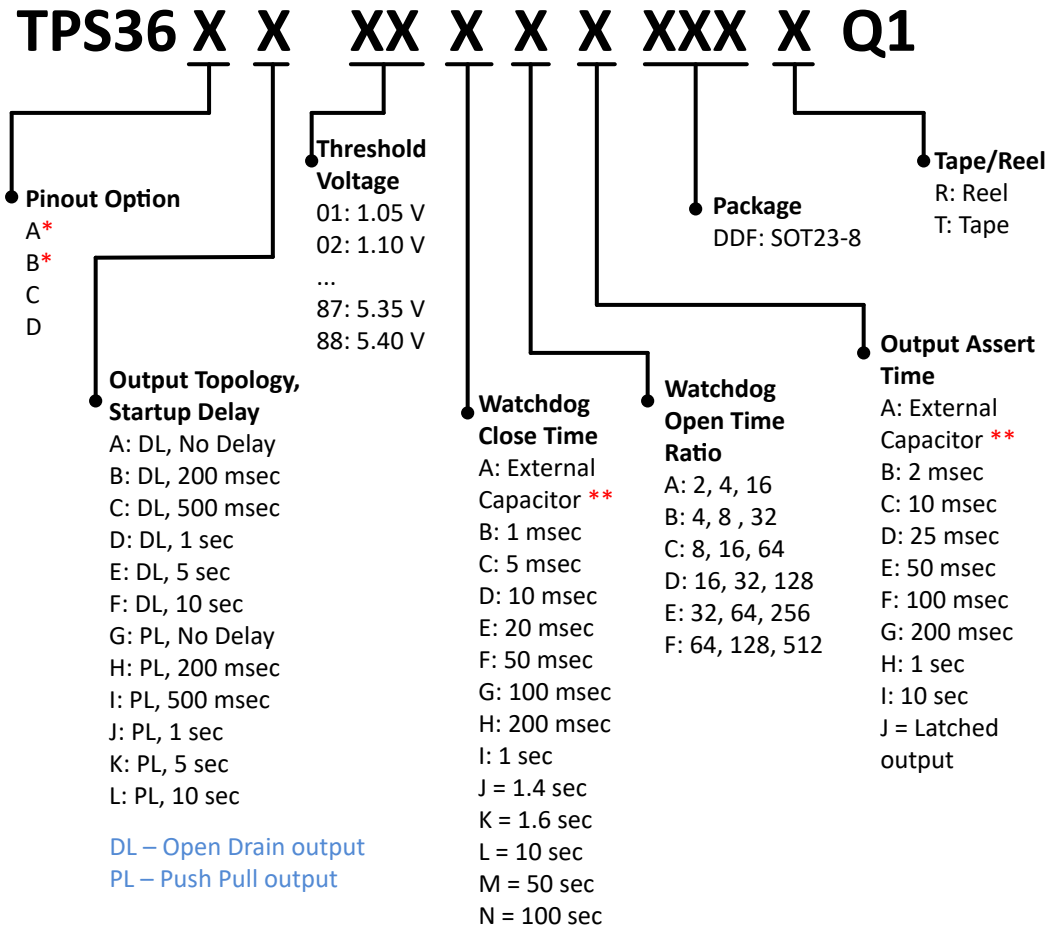
## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (November 2022) to Revision A (December 2022) | Page |
|---|---|
| • 事前情報から量産データのリリースに変更 | 1 |

## 5 デバイスの比較

図 5-1 に、TPS36-Q1 のデバイス命名規則 を示します。可能なすべての出力タイプ、スレッショルド電圧オプション、ウォッチドッグ時間オプション、および出力アサート遅延オプションの詳細については、セクション 8 を参照してください。他のオプションの詳細と提供状況については、TI の販売代理店または TI の E2E フォーラム にお問い合わせください。




* Pinout option supports Start up Delay settings of “No Delay” and “10 sec” only.
** Capacitor programmable time feature available with pinout options A & B. For fixed time and latched output features use pinout options C & D.
Refer ‘Mechanical, Packaging and Orderable Information’ section for list of released orderable.
For any other orderable, contact local TI support.

**図 5-1. デバイスの命名規則**

TPS36-Q1 表 5-1 に示すように、さまざまな機能セットを提供するピン互換デバイス・ファミリに属します。

**表 5-1. ピン互換デバイス・ファミリ**

| デバイス | 電圧監視 | ウォッチドッグのタイプ |
|---|---|---|
| TPS35-Q1 | あり | タイムアウト |
| TPS36-Q1 | あり | ウィンドウ |
| TPS3435-Q1 | なし | タイムアウト |
| TPS3436-Q1 | なし | ウィンドウ |


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# 6 Pin Configuration and Functions

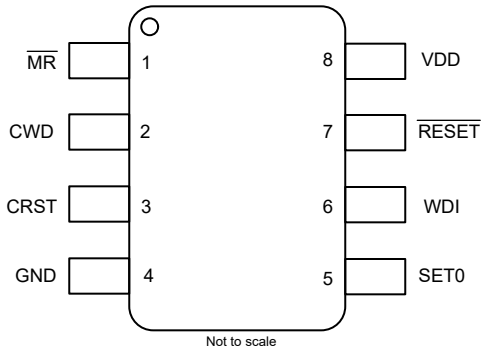



**図 6-1. Pin Configuration Option A DDF Package, 8-Pin SOT-23, TPS36-Q1 Top View**

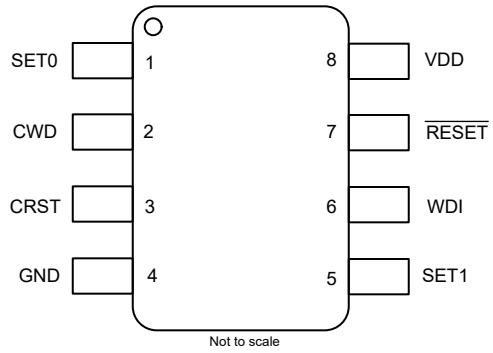



**図 6-2. Pin Configuration Option B DDF Package, 8-Pin SOT-23, TPS36-Q1 Top View**

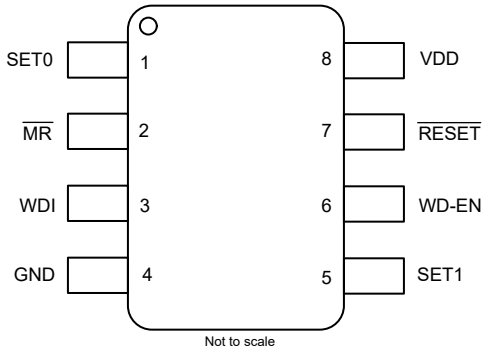



**図 6-3. Pin Configuration Option C DDF Package, 8-Pin SOT-23, TPS36-Q1 Top View**

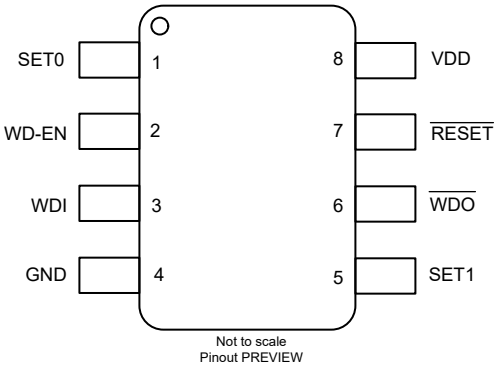



**図 6-4. Pin Configuration Option D DDF Package, 8-Pin SOT-23, TPS36-Q1 Top View**

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**表 6-1. Pin Functions**

| PIN NAME | PIN NUMBER | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| | PINOUT A | PINOUT B | PINOUT C | PINOUT D | | |
| CRST | 3 | 3 | — | — | I | Programmable reset timeout pin. Connect a capacitor between this pin and GND to program the reset timeout period. See *セクション 8.3.4* for more details. |
| CWD | 2 | 2 | — | — | I | Programmable watchdog timeout input. Watchdog close time is set by connecting a capacitor between this pin and ground. See セクション 8.3.2.1 for more details. |
| GND | 4 | 4 | 4 | 4 | — | Ground pin |
| $\overline{MR}$ | 1 | — | 2 | — | I | Manual reset pin. A logic low on this pin asserts the $\overline{RESET}$. See *セクション 8.3.3* for more details. |
| $\overline{RESET}$ | 7 | 7 | 7 | 7 | O | Reset output. Connect $\overline{RESET}$ to VDD using a pull up resistance when using open drain output. $\overline{RESET}$ is asserted when the voltage at the VDD pin goes below the undervoltage threshold ($V_{IT-}$) or $\overline{MR}$ pin is driven LOW. For pinout options which do not support independent $\overline{WDO}$ pin, $\overline{RESET}$ is also asserted for watchdog error. See *セクション 8.3.4* for more details. |
| SET0 | 5 | 1 | 1 | 1 | I | Logic input. SET0, SET1, and WD-EN pins select the watchdog window ratios and enable-disable the watchdog; see セクション 8.3.2.5 for more details. |
| SET1 | — | 5 | 5 | 5 | I | Logic input. SET0, SET1, and WD-EN pins select the watchdog window ratios and enable-disable the watchdog; see セクション 8.3.2.5 for more details. |
| VDD | 8 | 8 | 8 | 8 | I | Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended. |
| WD-EN | — | — | 6 | 2 | I | Logic input. Logic high input enables the watchdog monitoring feature. See *セクション 8.3.2.3* for more details. |
| WDI | 6 | 6 | 3 | 3 | I | Watchdog input. A falling transition (edge) must occur at this pin during the open window in order for $\overline{RESET}$ / $\overline{WDO}$ to not assert. See セクション 8.3.2 for more details. |
| $\overline{WDO}$ | — | — | — | 6 | O | Watchdog output. Connect $\overline{WDO}$ to VDD using pull up resistance when using open drain output. $\overline{WDO}$ asserts when a watchdog error occurs. $\overline{WDO}$ only asserts when $\overline{RESET}$ is high. When a watchdog error occurs, $\overline{WDO}$ asserts for the set $\overline{RESET}$ timeout delay ($t_D$). When $\overline{RESET}$ is asserted, $\overline{WDO}$ is deasserted and watchdog functionality is disabled. See *セクション 8.3.4* for more details. |


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VDD | –0.3 | 6.5 | V |
| Voltage | $C_{WD}$, $C_{RST}$, WD–EN, SETx, WDI, $\overline{MR}$ (2), $\overline{RESET}$ (Push Pull), $\overline{WDO}$ (Push Pull) | –0.3 | $V_{DD}$+0.3 (3) | V |
| | $\overline{RESET}$ (Open Drain), $\overline{WDO}$ (Open Drain) | –0.3 | 6.5 | |
| Current | $\overline{RESET}$, $\overline{WDO}$ pin | –20 | 20 | mA |
| Temperature (4) | Operating ambient temperature, $T_A$ | –40 | 125 | ℃ |
| Temperature | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If the logic signal driving $\overline{MR}$ is less than $V_{DD}$, then additional current flows into $V_{DD}$ and out of $\overline{MR}$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller
(4) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | VDD (Active Low output) | 0.9 | | 6 | V |
| | $C_{WD}$, $C_{RST}$, WD–EN, SETx, WDI, $\overline{MR}$ (1) | 0 | | VDD | |
| | $\overline{RESET}$ (Open Drain) , $\overline{WDO}$ (Open Drain) | 0 | | 6 | |
| | $\overline{RESET}$ (Open Drain) , $\overline{WDO}$ (Push Pull) | 0 | | VDD | |
| Current | $\overline{RESET}$, $\overline{WDO}$ pin current | –5 | | 5 | mA |
| $C_{RST}$ | $C_{RST}$ pin capacitor range | 1.5 | | 1800 | nF |
| $C_{WD}$ | $C_{WD}$ pin capacitor range | 1.5 | | 1000 | nF |
| $T_A$ | Operating ambient temperature | –40 | | 125 | ℃ |

(1) If the logic signal driving $\overline{MR}$ is less than $V_{DD}$, then additional current flows into $V_{DD}$ and out of $\overline{MR}$. $V_{MR}$ should not be higher than $V_{DD}$.

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## 7.4 Thermal Information

| THERMAL METRIC(1) | | TPS36-Q1 DDF (SOT23-8) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 175.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 94.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 92.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 91.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 7.5 Electrical Characteristics

At 1.04 V ≤ $V_{DD}$ ≤ 6 V, $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output load ($C_{LOAD}$) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **COMMON PARAMETERS** | | | | | | | |
| $V_{DD}$ | Input supply voltage | Active LOW output | | 1.04 | | 6 | V |
| $V_{IT–}$ | Negative-going input threshold accuracy (1) | $V_{IT–}$ = 1.05 V to 1.95 V | | –1.4 | ±0.5 | 1.4 | % |
| | | $V_{IT–}$ = 2.0 V to 5.4 V | | –1.2 | ±0.5 | 1.2 | |
| $V_{HYS}$ | Hysteresis $V_{IT–}$ pin | $V_{IT–}$ = 1.05 V to 5.4 V | | 3 | 5 | 7 | % |
| $I_{DD}$ | Supply current into VDD pin (2) | $V_{DD}$ = 2 V<br>$V_{IT–}$ = 1.05 V to 1.95 V | $T_A$ = –40°C to 85°C | | 0.25 | 0.8 | µA |
| | | | | | 0.25 | 3 | |
| | | $V_{DD}$ = 6 V<br>$V_{IT–}$ = 1.05 V to 5.4 V | $T_A$ = –40°C to 85°C | | 0.25 | 0.8 | |
| | | | | | 0.25 | 3 | |
| $V_{IL}$ | Low level input voltage WD–EN, WDI, SETx, $\overline{MR}$ (3) | | | | | 0.3$V_{DD}$ | V |
| $V_{IH}$ | High level input voltage WD–EN, WDI, SETx, $\overline{MR}$ (3) | | | 0.7$V_{DD}$ | | | V |
| $R_{\overline{MR}}$ | Manual reset internal pull-up resistance | | | | 100 | | kΩ |
| **$\overline{RESET}$ / $\overline{WDO}$ (Open-drain active-low)** | | | | | | | |
| $V_{OL}$ | Low level output voltage | $V_{DD}$ =1.5 V, 1.55 V ≤ $V_{IT–}$ ≤ 3.35 V<br>$I_{OUT(Sink)}$ = 500 µA | | | | 300 | mV |
| | | $V_{DD}$ = 3.3 V, 3.4 V ≤ $V_{IT–}$ ≤ 5.4 V<br>$I_{OUT(Sink)}$ = 2 mA | | | | 300 | |
| $I_{lkg(OD)}$ | Open-Drain output leakage current | $V_{DD}$ = $V_{PULLUP}$ = 6V<br>$T_A$ = –40°C to 85°C | | | 10 | 30 | nA |
| | | $V_{DD}$ = $V_{PULLUP}$ = 6V | | | 10 | 120 | nA |
| **$\overline{RESET}$ / $\overline{WDO}$ (Push-pull active-low)** | | | | | | | |
| $V_{POR}$ | Power on $\overline{RESET}$ voltage (5) | $V_{OL(max)}$ = 300 mV<br>$I_{OUT(Sink)}$ = 15 µA | | | | 900 | mV |
| $V_{OL}$ | Low level output voltage | $V_{DD}$ = 0.9 V, 1.05 V ≤ $V_{IT–}$ ≤ 1.5 V<br>$I_{OUT(Sink)}$ = 15 µA | | | | 300 | mV |
| | | $V_{DD}$ = 1.5 V, 1.55 V ≤ $V_{IT–}$ ≤ 3.35 V<br>$I_{OUT(Sink)}$ = 500 µA | | | | 300 | |
| | | $V_{DD}$ = 3.3 V, 3.4 V ≤ $V_{IT–}$ ≤ 5.4 V<br>$I_{OUT(Sink)}$ = 2 mA | | | | 300 | |
| $V_{OH}$ | High level output voltage | $V_{DD}$ = 1.8 V, 1.05 V ≤ $V_{IT–}$ ≤ 1.4 V<br>$I_{OUT(Source)}$ = 500 µA | | 0.8$V_{DD}$ | | | V |
| | | $V_{DD}$ = 3.3 V, 1.45 V ≤ $V_{IT–}$ ≤ 3.0 V<br>$I_{OUT(Source)}$ = 500 µA | | 0.8$V_{DD}$ | | | |
| | | $V_{DD}$ = 6 V, 3.05 V ≤ $V_{IT–}$ ≤ 5.4 V<br>$I_{OUT(Source)}$ = 2 mA | | 0.8$V_{DD}$ | | | |

(1) $V_{IT–}$ threshold voltage range from 1.05 V to 5.4 V in 50 mV steps.
(2) If the logic signal driving $\overline{MR}$ is less than $V_{DD}$, then additional current flows into $V_{DD}$ and out of $\overline{MR}$.
(3) $V_{POR}$ is the minimum $V_{DD}$ voltage level for a controlled output state

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## 7.6 Timing Requirements

At 1.04 V ≤ $V_{DD}$ ≤ 6 V, $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output RESET / WDO load ($C_{LOAD}$) = 10 pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at $T_A$ = 25℃

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{GI_VIT-}$ | Glitch immunity $V_{IT-}$ | 5% $V_{IT-}$ overdrive(1) | | 15 | | µs |
| $t_{\overline{MR}_PW}$ | $\overline{MR}$ pin pulse duration to assert reset | | | 100 | | ns |
| $t_{P-WD}$ | WDI pulse duration to start next frame (2) | $V_{DD}$ > $V_{IT-}$ | 500 | | | ns |
| $t_{HD-WDEN}$ | WD-EN hold time to enable or disable WD operation (2) | $V_{DD}$ > $V_{IT-}$ | 200 | | | µs |
| $t_{HD-SETx}$ | SETx hold time to change WD timer setting (2) | $V_{DD}$ > $V_{IT-}$ | 150 | | | µs |
| $t_{WC}$ | Watchdog close window time period | Orderable Option TPS36xxxxB | 0.8 | 1 | 1.2 | ms |
| | | Orderable Option TPS36xxxxC | 4 | 5 | 6 | |
| | | Orderable Option TPS36xxxxD | 9 | 10 | 11 | |
| | | Orderable Option TPS36xxxxE | 18 | 20 | 22 | |
| | | Orderable Option TPS36xxxxF | 45 | 50 | 55 | |
| | | Orderable Option TPS36xxxxG | 90 | 100 | 110 | |
| | | Orderable Option TPS36xxxxH | 180 | 200 | 220 | |
| | | Orderable Option TPS36xxxxI | 0.9 | 1 | 1.1 | s |
| | | Orderable Option TPS36xxxxJ | 1.26 | 1.4 | 1.54 | |
| | | Orderable Option TPS36xxxxK | 1.44 | 1.6 | 1.76 | |
| | | Orderable Option TPS36xxxxL | 9 | 10 | 11 | |
| | | Orderable Option TPS36xxxxM | 45 | 50 | 55 | |
| | | Orderable Option TPS36xxxxN | 90 | 100 | 110 | |
| $t_{WO}$ | Watchdog open window time period | SETx pin decide multipler *n* | | *(n-1)* X $t_{WC}$ | | ms |

(1) Overdrive % = [($V_{DD}$/ $V_{IT-}$) – 1] × 100%
(2) Not production tested


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## 7.7 Switching Characteristics

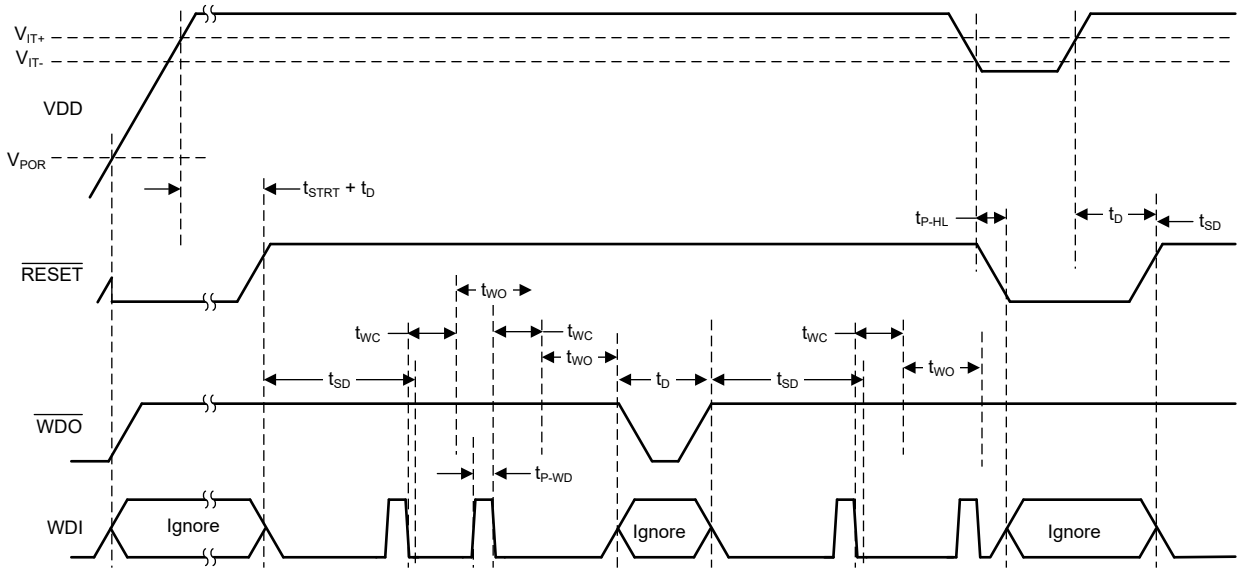
At 1.04 V ≤ $V_{DD}$ ≤ 6 V, $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output RESET / WDO load ($C_{LOAD}$) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STRT}$ | Startup delay(4) | | | | 500 | µs |
| $t_{P_HL}$ | RESET detect delay for VDD falling below $V_{IT-}$ | $V_{DD}$ : ($V_{IT+}$ + 10%) to ($V_{IT-}$ – 10%) (1) | | 30 | 50 | µs |
| $t_{SD}$ | Watchdog startup delay | Orderable part number TPS36xA, TPS36xG | | 0 | | ms |
| | | Orderable part number TPS36xB, TPS36xH | 180 | 200 | 220 | |
| | | Orderable part number TPS36xC, TPS36xI | 450 | 500 | 550 | |
| | | Orderable part number TPS36xD, TPS36xJ | 0.9 | 1 | 1.1 | s |
| | | Orderable part number TPS36xE, TPS36xK | 4.5 | 5 | 5.5 | |
| | | Orderable part number TPS36xF, TPS36xL | 9 | 10 | 11 | |
| $t_D$ | Reset time delay (3) | Orderable part number TPS36xxxxxxB | 1.6 | 2 | 2.4 | ms |
| | | Orderable part number TPS36xxxxxxC | 9 | 10 | 11 | ms |
| | | Orderable part number TPS36xxxxxxD | 22.5 | 25 | 27.5 | ms |
| | | Orderable part number TPS36xxxxxxE | 45 | 50 | 55 | ms |
| | | Orderable part number TPS36xxxxxxF | 90 | 100 | 110 | ms |
| | | Orderable part number TPS36xxxxxxG | 180 | 200 | 220 | ms |
| | | Orderable part number TPS36xxxxxxH | 0.9 | 1 | 1.1 | s |
| | | Orderable part number TPS36xxxxxxI | 9 | 10 | 11 | s |
| $t_{WDO}$ | Watchdog timeout delay | | | $t_D$ | | s |
| $t_{\overline{MR}_RES}$ | Propagation delay from $\overline{MR}$ low to reset assertion | $V_{DD}$ ≥ $V_{IT-}$ + 0.2 V, $\overline{MR}$ = $V_{\overline{MR}_H}$ to $V_{\overline{MR}_L}$ | | 100 | | ns |
| $t_{\overline{MR}_tD}$ | Delay from $\overline{MR}$ release to reset deassert | $V_{DD}$ = 3.3 V, $\overline{MR}$ = $V_{\overline{MR}_L}$ to $V_{\overline{MR}_H}$ | | $t_D$ | | s |

(1) $t_{P_HL}$ measured from threshold trip point ($V_{IT-}$) to RESET assert. $V_{IT+}$ = $V_{IT-}$ + $V_{HYS}$
(2) Specified by design parameter. When VDD starts from less than the specified minimum $V_{DD}$ and then exceeds $V_{IT+}$, reset is deasserted after the startup delay ($t_{STRT}$) + $t_D$ delay.
(3) VDD voltage transitions from ($V_{IT-}$ - 10%) to ($V_{IT-}$ + 10%)

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## 7.8 Timing Diagrams




Devices with only RESET output, the output will be AND operation of RESET and WDO signals.

**図 7-1. Functional Timing Diagram**


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## 7.9 Typical Characteristics

all curves are taken at $T_A$ = 25°C (unless otherwise noted)

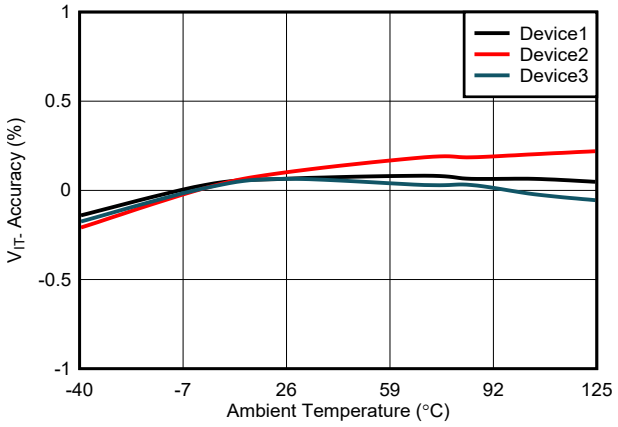



図 7-2. $V_{IT-}$ Accuracy vs Temperature

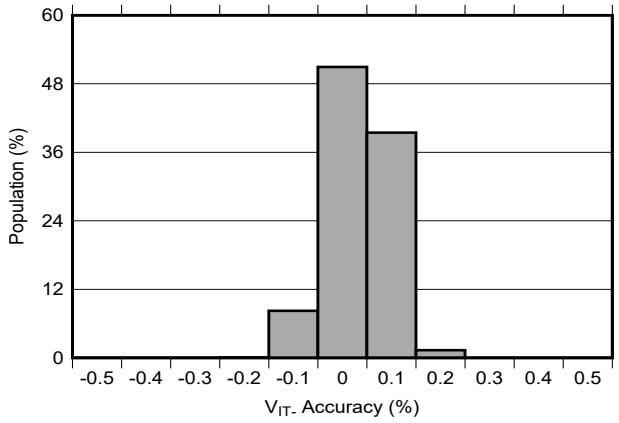



図 7-3. $V_{IT-}$ Accuracy Histogram

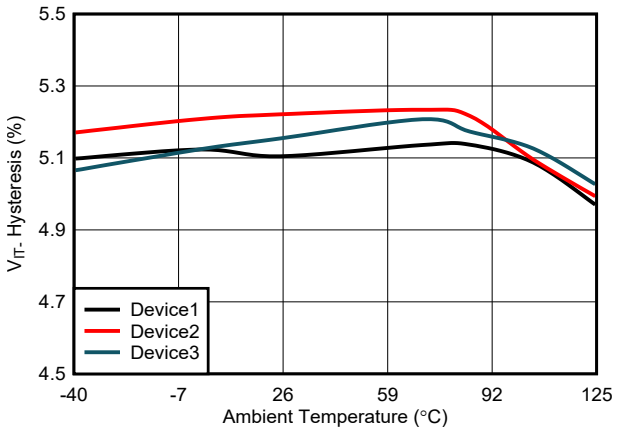



図 7-4. $V_{IT-}$ Hysteresis Vs Temperature

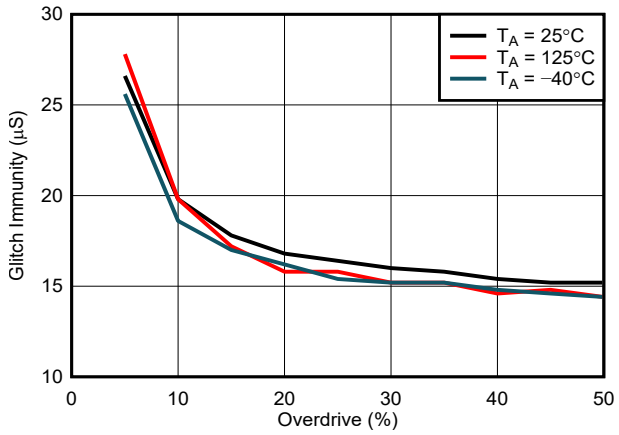



図 7-5. Supply Glitch Immunity vs Overdrive

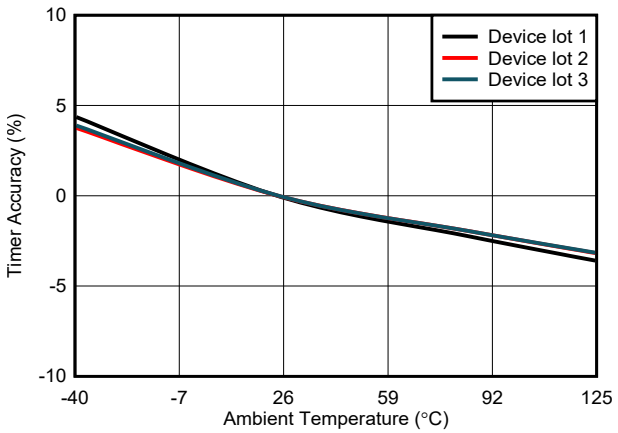



図 7-6. Timer Accuracy vs Temperature

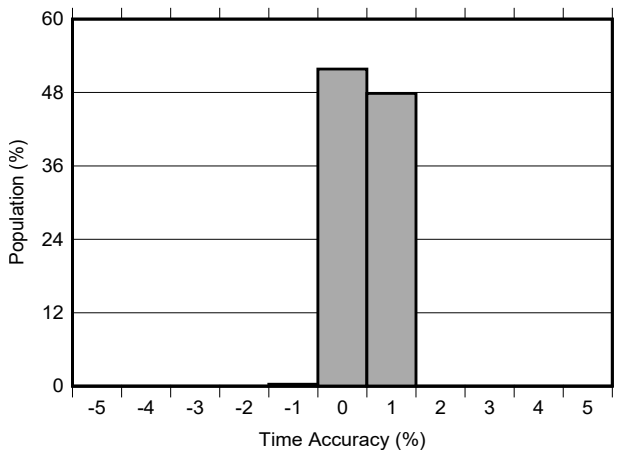



図 7-7. Timer Accuracy Histogram

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## 7.9 Typical Characteristics (continued)

all curves are taken at $T_A$ = 25°C (unless otherwise noted)

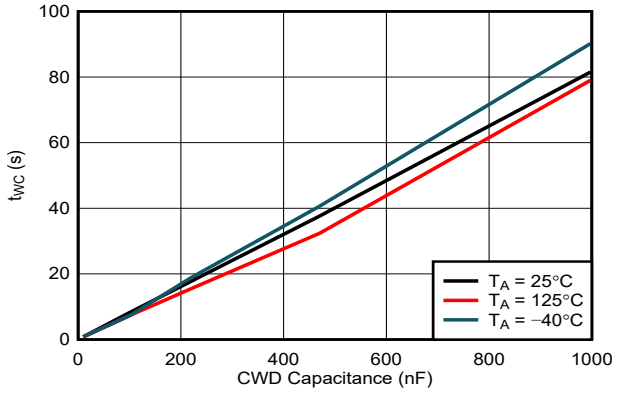



**図 7-8. $t_{WC}$ vs Capacitance**

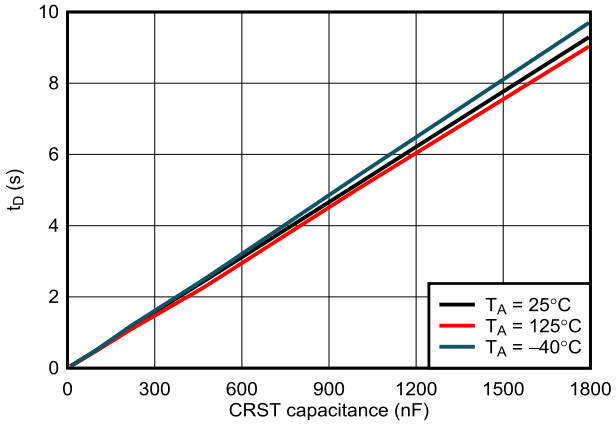



**図 7-9. $t_D$ vs Capacitance**

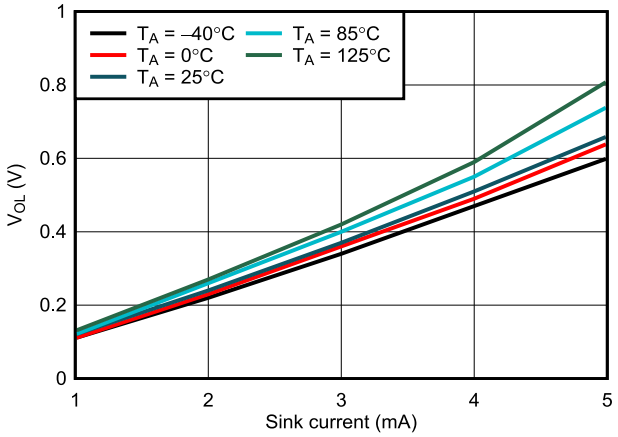



**図 7-10. RESET $V_{OL}$ vs $I_{sink}$, $V_{DD}$ = 1.5 V**

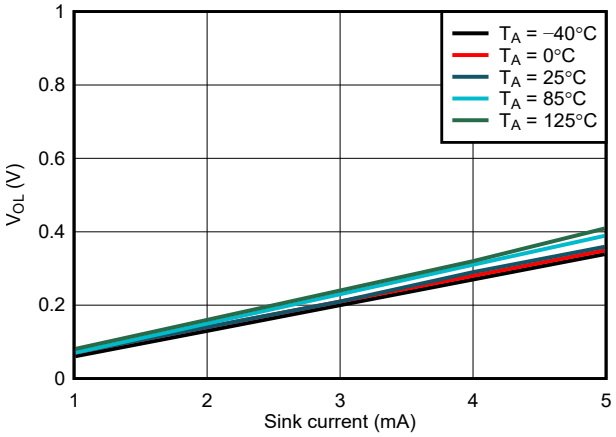



**図 7-11. WDO $V_{OL}$ vs $I_{sink}$, $V_{DD}$ = 1.5 V**

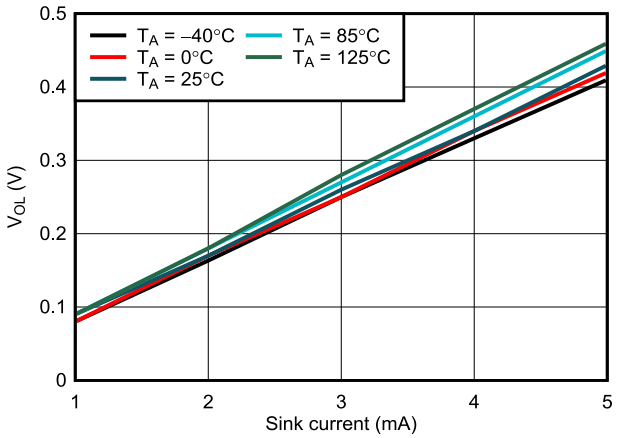



**図 7-12. RESET $V_{OL}$ vs $I_{sink}$, $V_{DD}$ = 3.3 V**

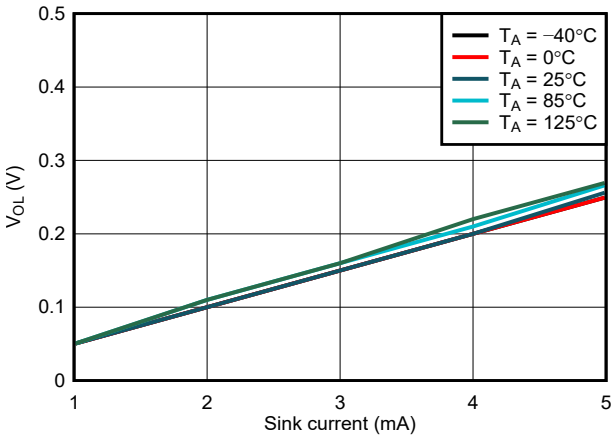



**図 7-13. WDO $V_{OL}$ vs $I_{sink}$, $V_{DD}$ = 3.3 V**


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## 7.9 Typical Characteristics (continued)

all curves are taken at $T_A$ = 25°C (unless otherwise noted)

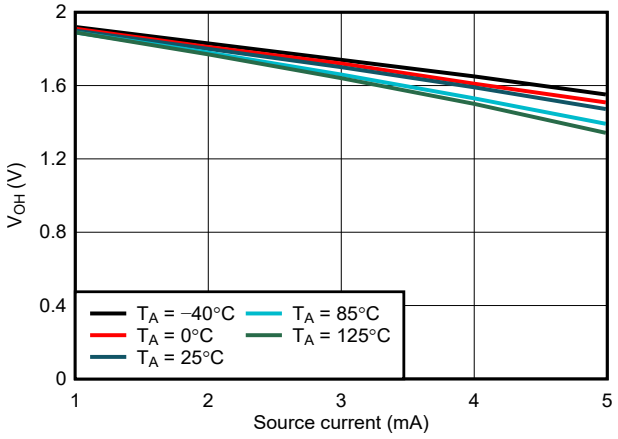



**図 7-14. RESET $V_{OH}$ vs $I_{source}$, $V_{DD}$ = 2.0 V**

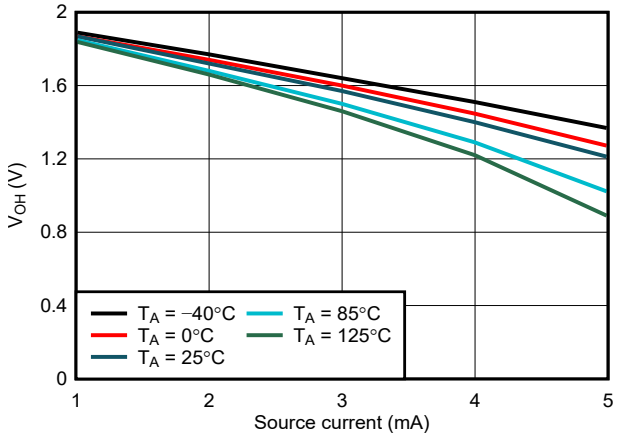



**図 7-15. WDO $V_{OH}$ vs $I_{source}$, $V_{DD}$ = 2.0 V**

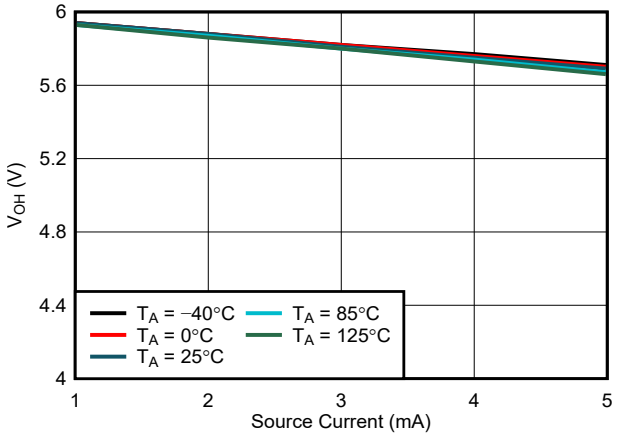



**図 7-16. RESET $V_{OH}$ vs $I_{source}$, $V_{DD}$ = 6.0 V**

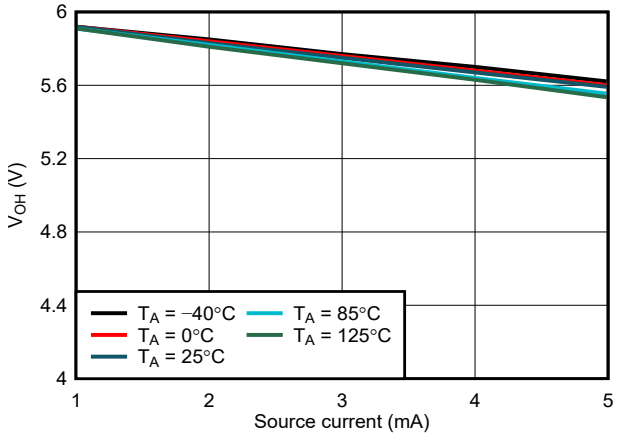



**図 7-17. WDO $V_{OH}$ vs $I_{source}$, $V_{DD}$ = 6.0 V**

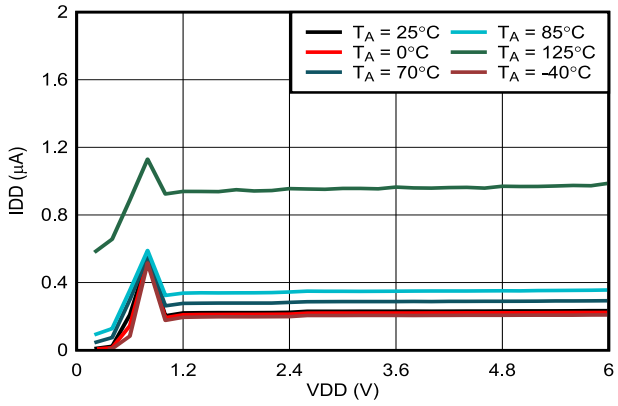



**図 7-18. Supply Current vs Power-Supply Voltage**

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# 8 Detailed Description

## 8.1 Overview

The TPS36-Q1 is a high-accuracy under voltage supervisor with an integrated window watchdog timer device. The device family supports multiple features related to watchdog operation in a compact 8 pin SOT23 package. The devices are available in 4 different pinout configurations. Each pinout offers access to different features to meet the various application requirements. The device family is rated for -Q100 applications.

## 8.2 Functional Block Diagrams

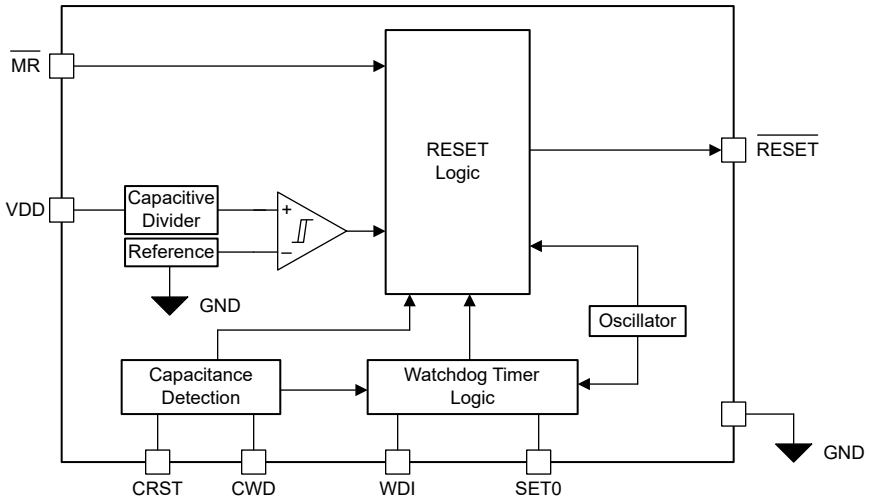



図 8-1. Pinout Option A

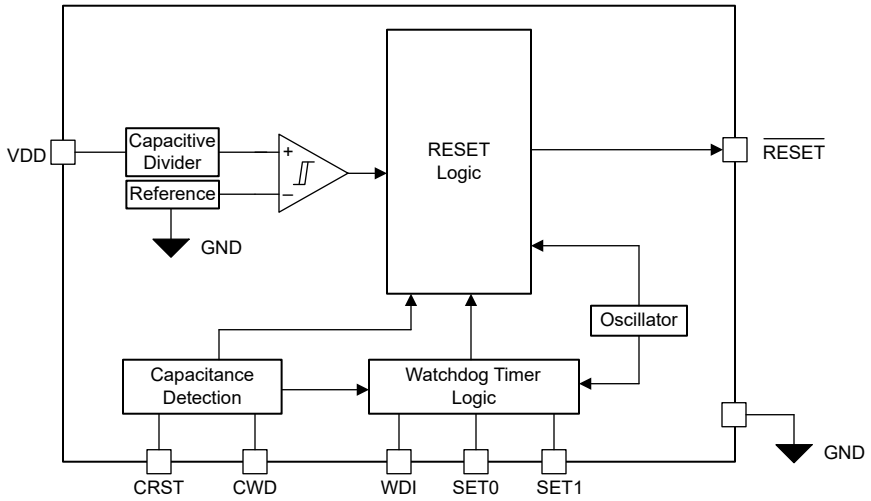



図 8-2. Pinout Option B


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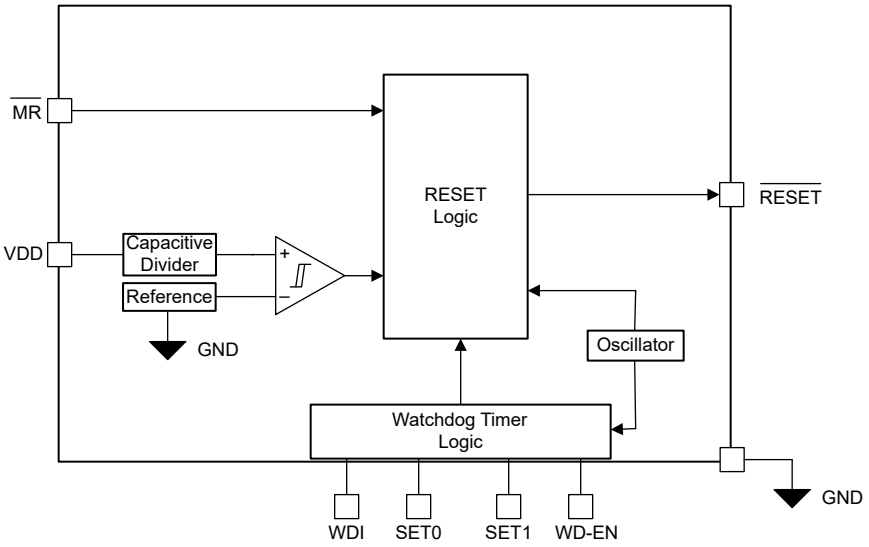



**図 8-3. Pinout Option C**

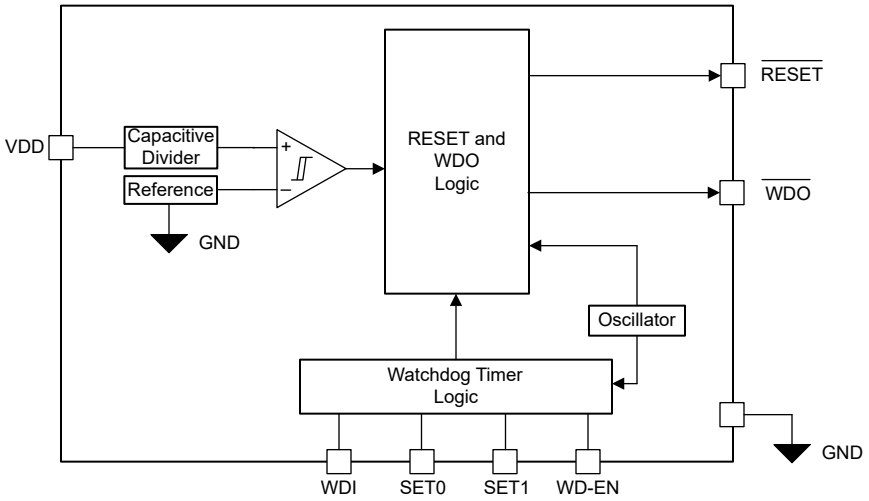



**図 8-4. Pinout Option D**

## 8.3 Feature Description

### 8.3.1 Voltage Supervisor

The TPS36-Q1 offers high accuracy under voltage supervisor function at very low quiescent current. The voltage supervisor function is always active. After the device powers up from VDD < $V_{POR}$, the RESET and WDO outputs will be actively driven when VDD is greater than $V_{POR}$. The device starts monitoring the supply level when the VDD voltage is greater than 1.04 V. The device will hold the RESET pin asserted for $t_{STRT}$ + $t_D$ time after the VDD > $V_{IT+}$ ($V_{IT-}$ + $V_{HYS}$). Refer *セクション 8.3.4* for the $t_D$ value computation. For a capacitor based $t_D$ delay option, the RESET will be asserted for $t_{STRT}$ + 2 msec time if the CRST pin is open.

Device pinout options A to C offer only RESET output. In these devices the internal RESET output from supervisor and WDO output from watchdog timer are ANDed together to drive the external RESET output.

The supervisor offers wide range of fixed monitoring thresholds ($V_{IT-}$) from 1.05 V to 5.40 V in steps of 50 mV. The device asserts the RESET output when the VDD signal falls below $V_{IT-}$ threshold. The device offers hysteresis functionality for voltage supervision. This ensures the supply has recovered above the monitoring threshold before the RESET output is deasserted. The TPS36-Q1 typical voltage hysteresis ($V_{HYS}$) is 5%. Along with the voltage hysteresis, the device keeps the RESET output asserted for time duration $t_D$ after the supply has

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risen above $V_{IT+}$. The RESET output assert duration changes from $t_D$ to $t_{STRT}$ + $t_D$ if the VDD signal is ramping from voltage < $V_{POR}$. The $t_D$ time duration can be programmable using an external capacitor or fixed time options offered by the device.

The typical timing behavior for a voltage supervisor and the RESET output is showcased in 図 8-5. The voltage supervisor monitoring output has higher priority over watchdog functionality. If the device voltage supervisor output is asserted, the watchdog functionality will be disabled including WDO assert control. The device resumes watchdog related functionality only after the supply is stable and the $t_D$ time duration has elapsed.

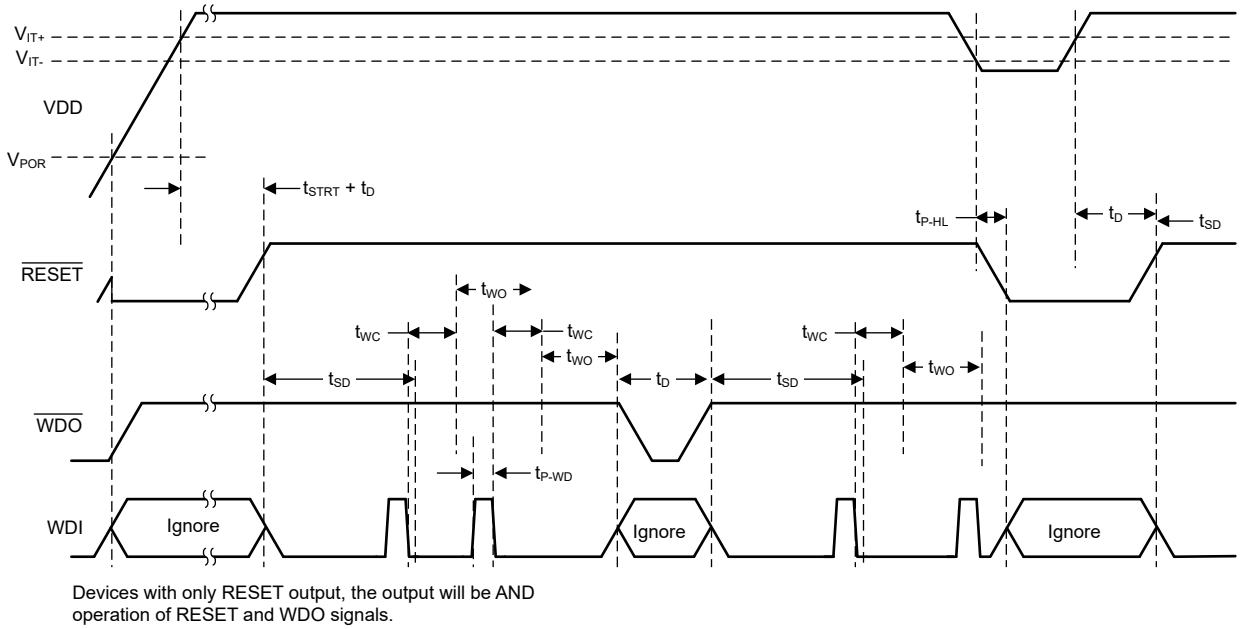



**図 8-5. Voltage Supervisor Timing Diagram**

### 8.3.2 Window Watchdog Timer

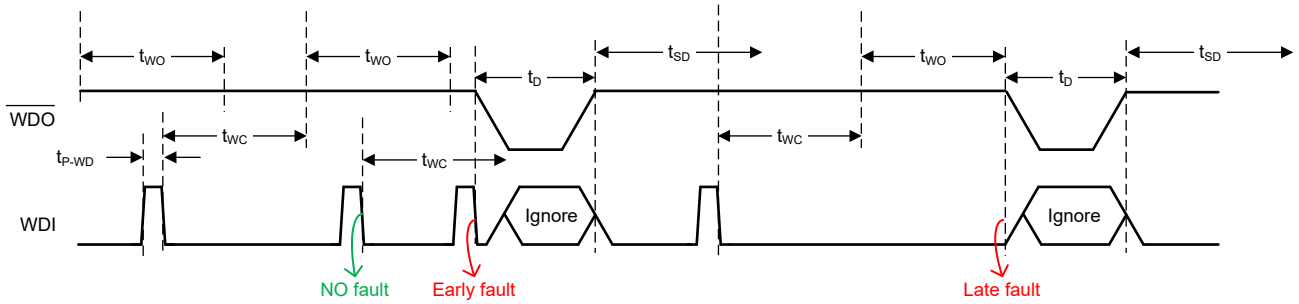
The TPS36-Q1 offers high precision window watchdog timer monitoring. The device is available in multiple pinout options A to D which support multiple features to meet ever expanding needs of various applications. Ensure a correct pinout is selected to meet the application needs.

The window watchdog is active when the VDD voltage is higher than the $V_{IT-}$ + $V_{HYS}$ and the RESET is deasserted after the $t_D$ time. The watchdog stays active as long as VDD > $V_{IT-}$ and watchdog is enabled. TPS36-Q1 family offers various startup time delay options to ensure enough time is available for the host to complete boot operation. Please refer *セクション 8.3.2.4* section for additional details.

The window watchdog timer frame consists of two windows namely close window ($t_{WC}$) followed by open window ($t_{WO}$). The device monitors the WDI pin for falling edge. User is expected to provide a valid falling edge on WDI pin in the open window. Refer *セクション 5* to arrive at the relevant close window and open window values needed for application. The timer value is reset when a valid falling edge is detected on WDI pin in the $t_{WO}$ time duration. An early fault is reported if a WDI falling edge is detected in close window. A late fault is reported if WDI falling edge is not detected in both close and open window. The device asserts RESET output for pinout options A, B and C or WDO output for pinout D for time $t_D$ in event of watchdog fault. Refer *セクション 8.3.4* to arrive at the relevant $t_D$ value needed for application.

図 8-6 shows the basic operation for window watchdog timer operation. The TPS36-Q1 watchdog functionality supports multiple features. Details are available in following sub sections.


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Devices with only RESET output, the RESET output will be asserted when watchdog error occurs.

**図 8-6. Window Watchdog Timer Operation**

### *8.3.2.1 $t_{WC}$ (Close Window) Timer*

The window watchdog frame consists of two sub frames $t_{WC}$ followed by $t_{WO}$. The host is not expected to drive valid WDI transition during $t_{WC}$ time. A valid WDI transition during $t_{WC}$ frame results in early fault condition and the WDO output is asserted. RESET output is asserted if pinout does not offer independent WDO output. The $t_{WC}$ timer for TPS36-Q1 can be set using an external capacitor connected between CWD pin and GND pin. This feature is available with pinout options A or B. Applications which are space constrained or need timer values which meet offered timer options, can benefit when using pinout options C or D. The TPS36-Q1 offers multiple fixed timer options ranging from 1 msec up-to 100 sec.

The TPS36-Q1 when using capacitance based timer, senses the capacitance value during the power up or after a RESET event. The capacitor is charged and discharged with known internal current source for one cycle to sense the capacitance value. The sensed value is used to arrive at $t_{WC}$ timer for the watchdog operation. This unique implementation helps reduce the continuous charge and discharge current for the capacitor, thus reducing overall current consumption. Continuous charge and discharge of capacitance creates wider dead time (no watchdog monitor functionality) when capacitor is discharging. The dead time is higher for high value of capacitance. The unique implementation of TPS36-Q1 helps avoid the dead time as the capacitance is not continuously charging or discharging under normal operation. Ensure $C_{CWD}$ is < 200 x $C_{CRST}$ for accurate calibration of capacitance. The close time window is decided based on SETx pin combination and the CWD capacitance. 表 8-1 to 表 8-3 highlights the relationship between $t_{WC}$ in second and CWD capacitance in farad. The $t_{WC}$ timer is 20% accurate for an ideal capacitor. Accuracy of the capacitance will have additional impact on the $t_{WC}$ time. Ensure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

**表 8-1. $t_{WC}$ Equation 1 SET Pin (Pin Configuration A)**

| SET pin value | Equation |
|---|---|
| 0 | $t_{WC}$ (sec) = 79.2 x $10^6$ x $C_{CWD}$ (F) |
| 1 | $t_{WC}$ (sec) = 39.6 x $10^6$ x $C_{CWD}$ (F) |

**表 8-2. $t_{WC}$ Equation 2 SET Pin, WD-EN = 1 (Pin Configuration C, D)**

| SET Pin Value | Equation |
|---|---|
| 00 | $t_{WC}$ (sec) = 79.2 x $10^6$ x $C_{CWD}$ (F) |
| 01 | $t_{WC}$ (sec) = 79.2 x $10^6$ x $C_{CWD}$ (F) |
| 10 | $t_{WC}$ (sec) = 39.6 x $10^6$ x $C_{CWD}$ (F) |
| 11 | $t_{WC}$ (sec) = 9.9 x $10^6$ x $C_{CWD}$ (F) |

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**表 8-3. $t_{WC}$ Equation 2 SET Pin, WD-EN Not Available (Pin Configuration B)**

| SET Pin Value | Equation |
|---|---|
| 00 | $t_{WC}$ (sec) = 79.2 x $10^6$ x $C_{CWD}$ (F) |
| 01 | Watchdog disabled |
| 10 | $t_{WC}$ (sec) = 39.6 x $10^6$ x $C_{CWD}$ (F) |
| 11 | $t_{WC}$ (sec) = 9.9 x $10^6$ x $C_{CWD}$ (F) |

The TPS36-Q1 also offers wide selection of high accuracy fixed $t_{WC}$ timer options starting from 1 msec to 100 sec including various industry standard values. The TPS36-Q1 fixed time options are ±10% accurate for $t_{WC}$ ≥ 10 msec. For $t_{WC}$ < 10 msec, the accuracy is ±20%. $t_{WC}$ value relevant to application can be identified from the orderable part number. Refer *セクション 5* to identify mapping of orderable part number to $t_{WC}$ value.

#### *8.3.2.2 $t_{WO}$ (Open Window) Timer*

The window watchdog frame consists of two sub frames $t_{WC}$ followed by $t_{WO}$. The host is expected to drive valid WDI transition during $t_{WO}$ time. A valid WDI transition before beginning of $t_{WO}$ frame causes early fault condition. Failure to offer valid WDI transition during $t_{WC}$ and $t_{WO}$ frames results in late fault condition. When a fault condition is detected the WDO output is asserted. RESET output is asserted if pinout does not offer independent WDO output.

The $t_{WO}$ value is derived using $t_{WC}$ value and the window open time ratio value *n*. Equation highlights the relationship between $t_{WO}$ and $t_{WC}$. Refer セクション 5 to select available ratio options.

$$t_{WO} = (n - 1) \times t_{WC} \quad (1)$$

Each orderable can offer up to 3 ratio options based on the available SET pins. Refer セクション 8.3.2.5 to identify mapping of ratio value to SET pin control. The maximum $t_{WO}$ value is limited to 640 second. Ensure selected $t_{WC}$ and ratio combination does not lead to $t_{WO}$ value greater than 640 second.

#### *8.3.2.3 Watchdog Enable Disable Operation*

The TPS36-Q1 supports watchdog enable or disable functionality. This functionality is critical for different use cases as listed below.

- Disable watchdog during firmware update to avoid host RESET.
- Disable watchdog during software step-by-step debug operation.
- Disable watchdog when performing critical task to avoid watchdog error interrupt.
- Keep watchdog disabled until host boots up.

The TPS36-Q1 supports watchdog enable or disable functionality through either WD-EN pin (pin configuration C,D) or SET[1:0] = 0b'01 (pin configuration B) logic combination. For a given pinout only one of these two methods is available for the user to disable watchdog operation.

For a pinout which offers a WD-EN pin, the watchdog enable disable functionality is controlled by the logic state of WD-EN pin. Drive WD-EN = 1 to enable the watchdog operation or drive WD-EN = 0 to disable the watchdog operation. The WD-EN pin can be toggled any time during the device operation. The 図 8-7 diagram shows timing behavior with WD-EN pin control.


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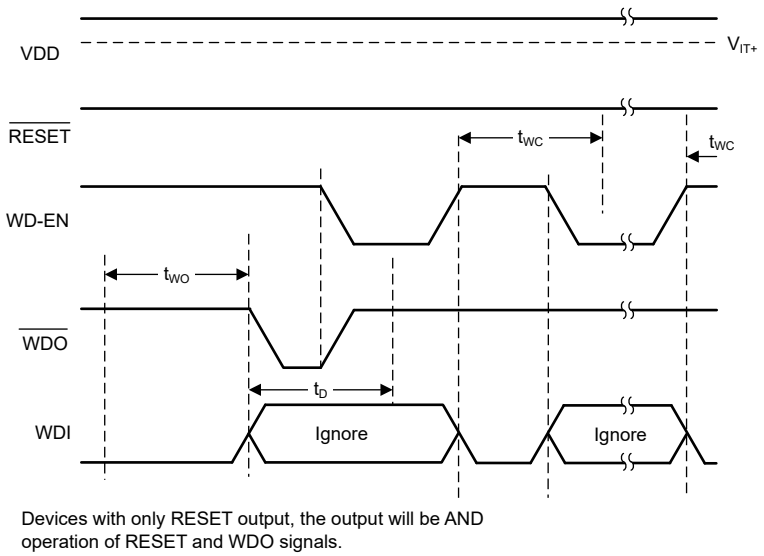



**図 8-7. Watchdog Enable: WD-EN Pin Control**

SET[1:0] = 0b'01 combination can be used to disable watchdog operation with a pinout which offers SET1 and SET0 pins, but does not include WD-EN pin. The SET pin logic states can be changed at any time during watchdog operation. Refer セクション 8.3.2.5 section for additional details regarding SET[1:0] pin behavior.

Pinout options A, B offer watchdog timer control using a capacitance connected between CWD and GND pin. A capacitance value higher than recommended or connect to GND leads to watchdog functionality getting disabled. Capacitance based disable operation overrides the other two options mentioned above. Changing capacitance on the fly does not enable or disable watchdog operation. A power supply recycle or device recovery after UV fault, $\overline{MR}$ low event is needed to detect change in capacitance.

Ongoing watchdog frame is terminated when watchdog is disabled. WDO stays deasserted when watchdog operation is disabled. For a pinout with only RESET output, the RESET can assert if supply supervisor error occurs. When enabled the device immediately enters $t_{WC}$ frame and start watchdog monitoring operation.

#### *8.3.2.4 $t_{SD}$ Watchdog Start Up Delay*

The TPS36-Q1 supports watchdog startup delay feature. This feature is activated after power up or after a RESET assert event or after WDO assert event. When $t_{SD}$ frame is active, the device monitors the WDI pin but the WDO output is not asserted. This feature allows time for the host complete boot process before watchdog monitoring can take over. The start up delay helps avoid unexpected WDO or RESET assert events during boot. The $t_{SD}$ time is predetermined based on the device part number selected. Refer *セクション 5* section for details to map the part number to $t_{SD}$ time. Pinout option A, B are available only in no delay or 10 sec start up delay options.

The $t_{SD}$ frame is complete when the time duration selected for $t_{SD}$ is over or host provides a valid transition on the WDI pin. The host must provide a valid transition on the WDI pin during $t_{SD}$ time. The device exits the $t_{SD}$ frame and enters watchdog monitoring phase after valid WDI transition. Failure to provide valid transition on WDI pin triggers the watchdog error by asserting the WDO output pin. For devices with only RESET output, the RESET pin is asserted.

The $t_{SD}$ frame is not initiated when the watchdog functionality is enabled using WD-EN pin or SET[1:0] pin or WDI float functionality as described in *セクション 8.3.2.3* section.

図 8-8 shows the operation for $t_{SD}$ time frame.

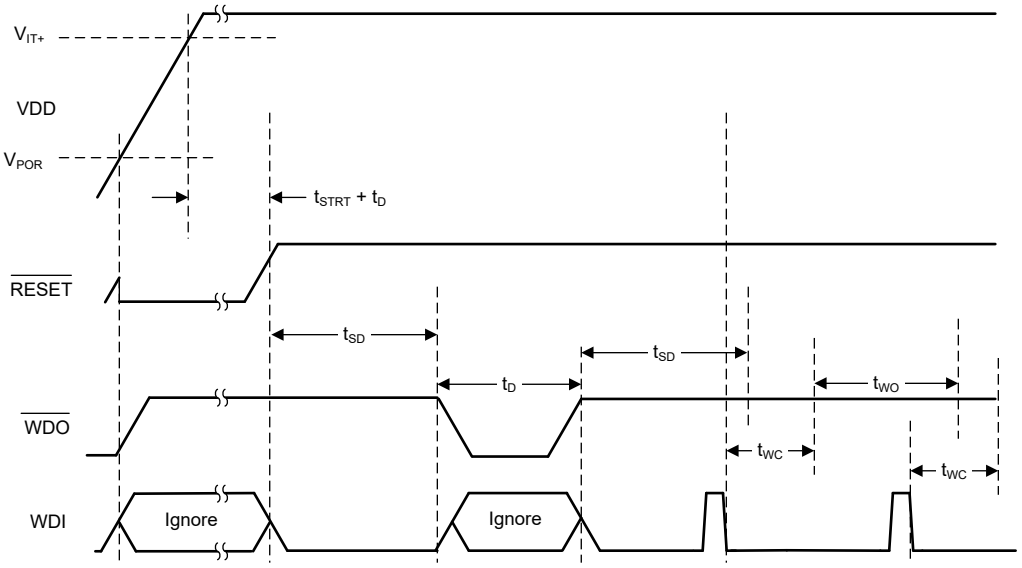



**図 8-8. $t_{SD}$ Frame Behavior**

### *8.3.2.5 SET Pin Behavior*

The TPS36-Q1 offers one or two SET pins based on the pinout option selected. SET pins offer flexibility to the user to program the $t_{WO}$ timer on the fly to meet various application requirements. Typical use cases where SET pin can be used are

- Use wide open window timer when host is in sleep mode, change to small timeout operation when host is operational. Watchdog can be used to wake up the host after long duration to perform the application related activities before going back to sleep.
- Change to wide open window timer when performing system critical tasks to ensure watchdog does not interrupt the critical task. Change timer to application specified interval after the critical task is complete.

The $t_{WO}$ timer value for the device is combination of $t_{WC}$ timer selection based on the CWD pin or fixed timer value along with SET pin logic level. The $t_{WC}$ timer value is decided based on the Watchdog Close Time selector in the *セクション 5* section. The SET pin logic level is decoded during the device power up. The SET pin value can be changed any time during the operation. SETx pin change which leads to change of watchdog timer value or enable disable state, terminates the ongoing watchdog frame immediately. SETx pins can be updated when WDO or RESET output is asserted as well. The updated $t_{WO}$ timer value will be applied after output is deasserted and the $t_{SD}$ timer is over or terminated.

For a pinout which offers only SET0 pin to the user, the $t_{WO}$ ratio value is decided based on the Watchdog Open Time Ratio selector field in the orderable part number. Refer *セクション 5* for available options. 表 8-4 showcases an example of the $t_{WO}$ values for different SET0 logic levels when using Watchdog Close Time setting as option D = 10 msec.


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**表 8-4. $t_{WO}$ Values with SET0 Pin Only (Pin Configuration A)**

| Watchdog Open Time Ratio Selection | $t_{WO}$ | |
|---|---|---|
| | SET0 = 0 | SET0 = 1 |
| A | 10 msec | 30 msec |
| B | 30 msec | 70 msec |
| C | 70 msec | 150 msec |
| D | 150 msec | 310 msec |
| E | 310 msec | 630 msec |
| F | 630 msec | 1270 msec |

Pinout which offer both SET0 & SET1 pins to the user, the $t_{WO}$ ratio value is decided based on the Watchdog Open Time Ratio selector field in the orderable part number. Refer *セクション 5* for available options. Two SETx pins offer 3 different time scaling options. The SET[1:0] = 0b'01 combination disables the watchdog operation. 表 8-5 showcases an example of the $t_{WO}$ values for different SET[1:0] logic levels when using Watchdog Close Time setting as option G = 100 msec. The package pin out selected does not offer WD-EN pin.

**表 8-5. $t_{WO}$ Values with SET0 & SET1 Pins, WD-EN Pin Not Available (Pin Configuration B)**

| Watchdog Open Time Ratio selection | $t_{WO}$ | | | |
|---|---|---|---|---|
| | SET[1:0] = 0b'00 | SET[1:0] = 0b'01 | SET[1:0] = 0b'10 | SET[1:0] = 0b'11 |
| A | 100 msec | Watchdog disable | 300 msec | 1500 msec |
| B | 300 msec | Watchdog disable | 700 msec | 3100 msec |
| C | 700 msec | Watchdog disable | 1500 msec | 6300 msec |
| D | 1500 msec | Watchdog disable | 3100 msec | 12700 msec |
| E | 3100 msec | Watchdog disable | 6300 msec | 25500 msec |
| F | 6300 msec | Watchdog disable | 12700 msec | 51100 msec |

1. Example for Watchdog Close Time setting = 100 msec.

Selected pinout option can offer WD-EN pin along with SET[1:0] pins (Pin Configuration C, D). With this pinout, the WD-EN pin controls watchdog enable and disable operation. The SET[1:0] = 0b'01 combination operates as SET[1:0] = 0b'00.

Ensure the $t_{WO}$ value with SETx ratio does not exceed 640 sec. If a selection of close window timer and ratio results in $t_{WO}$ > 640 sec, the timer value will be restricted to 640 sec.

図 8-9 to 図 8-11 show the timing behavior with respect to SETx status changes.

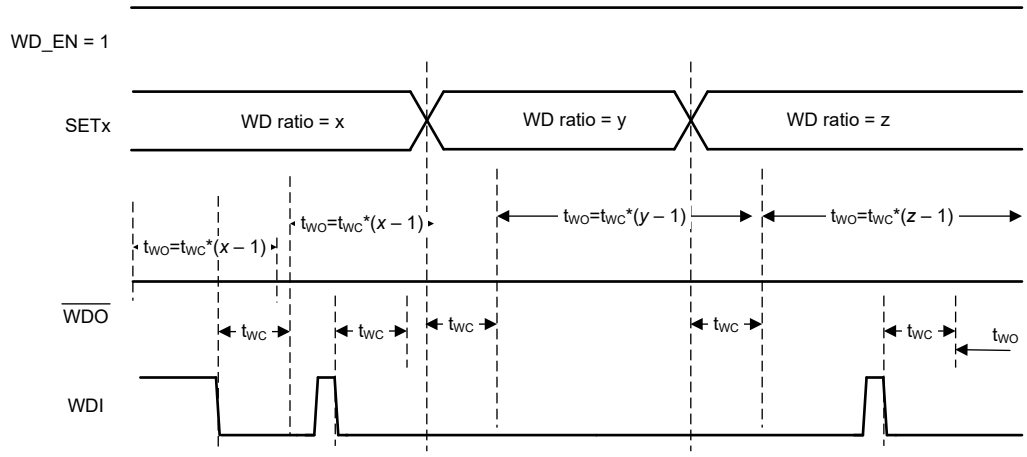



**図 8-9. Watchdog Behavior with SETx Pin Status**

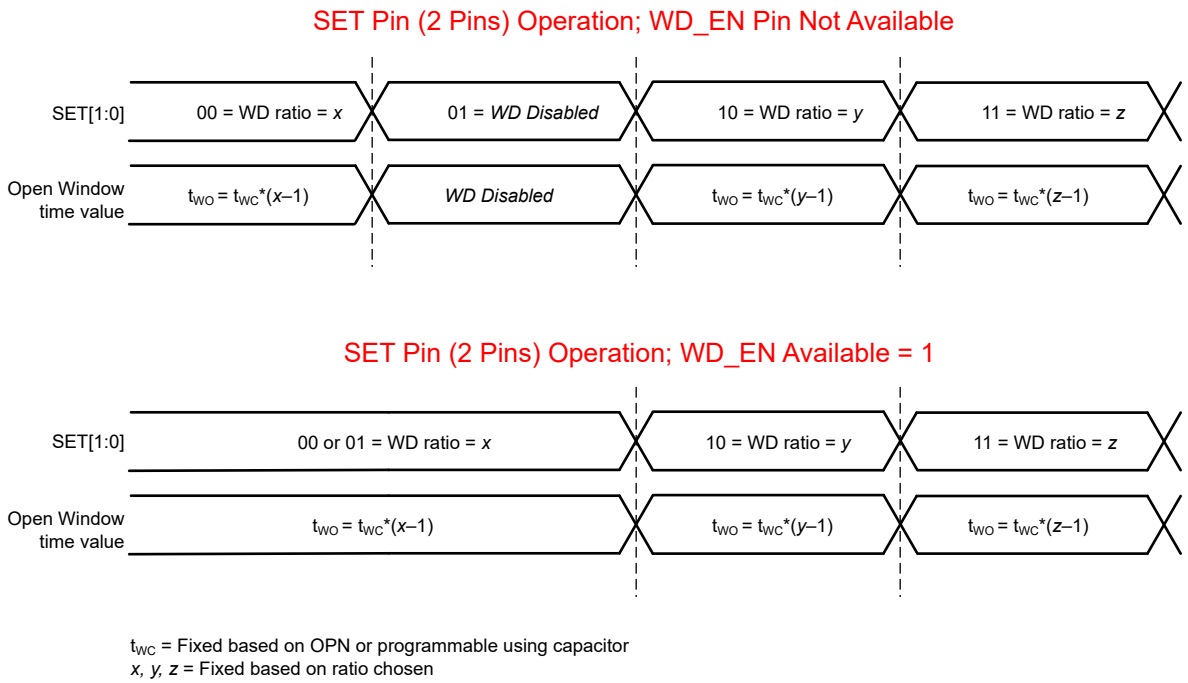



**図 8-10. Watchdog Operation with 2 SET Pins**

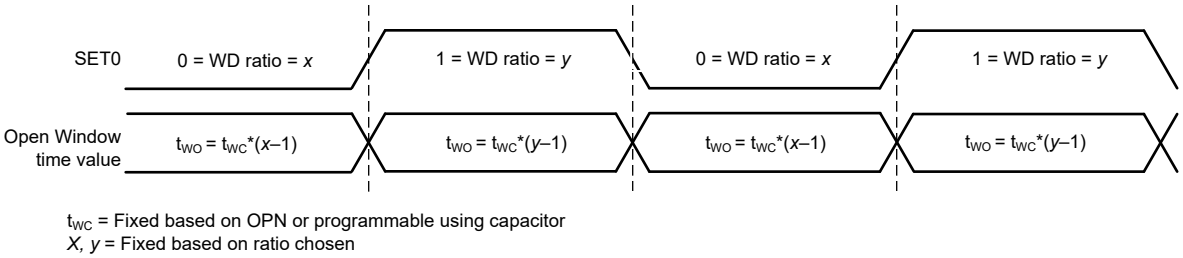



**図 8-11. Watchdog Operation with 1 SET Pin**

### 8.3.3 Manual RESET

The TPS36-Q1 supports manual reset functionality using $\overline{MR}$ pin. $\overline{MR}$ pin when driven with voltage lower than 0.3 x VDD, asserts the RESET output. The $\overline{MR}$ pin has 100 kΩ pull up to VDD. The $\overline{MR}$ pin can be left floating. The internal pull up will ensure the output is not asserted due to $\overline{MR}$ pin trigger.

The output is deasserted after $\overline{MR}$ pin voltage rises above 0.7 x VDD voltage and time $t_D$ is elapsed. Refer 図 8-12 for more details.

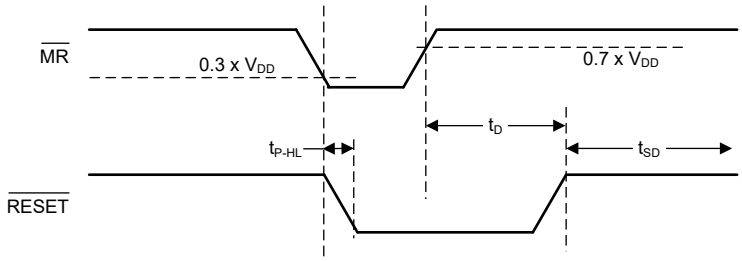



**図 8-12. $\overline{MR}$ Pin Response**


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### 8.3.4 RESET and WDO Output

The TPS36-Q1 device can offer RESET or RESET with independent WDO output pin. The output configuration is dependent on the pinout variant selected. For a pinout which has only RESET output, the RESET output is asserted when VDD voltage is below the monitored threshold or $\overline{MR}$ pin voltage is lower than threshold or watchdog timer error is detected. For a pinout which has independent RESET and WDO output pins, the RESET output is asserted when VDD voltage is below the monitored threshold or $\overline{MR}$ pin voltage is lower than threshold. WDO output is asserted only when watchdog timer error is detected. RESET error has higher priority than WDO error. If RESET is asserted when WDO is asserted, the device deasserts the WDO pin and watchdog is disabled until RESET pin is deasserted and startup delay frame is terminated.

The output will be asserted for $t_D$ time when any relevant events described above are detected. The time $t_D$ can be programmed by connecting a capacitor between CRST pin and GND or device will assert $t_D$ for fixed time duration as selected by orderable part number. Refer *セクション 5* section for all available options.

式 2 describes the relationship between capacitor value and the time $t_D$. Ensure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_D \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \quad (2)$$

TPS36-Q1 also offers a unique option of latched output. An orderable with latched output will hold the output in asserted state indefinitely until the device is power cycled or the error condition is addressed. If the output is latched due to voltage supervisor undervoltage detection, the output latch will be released when VDD voltage rises above the $V_{IT-} + V_{HYS}$ level. If the output is latched due to $\overline{MR}$ pin low voltage, the output latch will be released when $\overline{MR}$ pin voltage rises above 0.7 x $V_{DD}$ level. If the output is latched due to watchdog timer error, the output latch will be released when a WDI negative edge is detected or the device is shutdown and powered up again. 図 8-13 shows timing behavior of the device with latched output configuration.

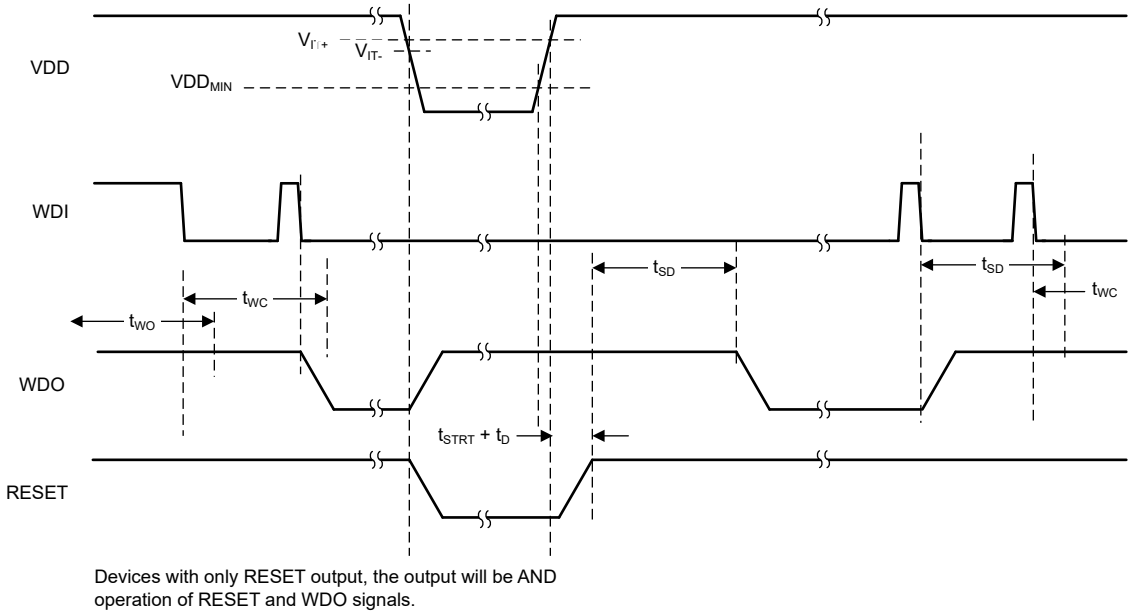



**図 8-13. Output Latch Timing Behavior**

## 8.4 Device Functional Modes

表 8-6 summarizes the functional modes of the TPS36-Q1.

**表 8-6. Device Functional Modes**

| VDD | WATCHDOG STATUS | WDI | $\overline{\text{WDO}}$ | $\overline{\text{RESET}}$ |
|---|---|---|---|---|
| $V_{DD} < V_{POR}$ | Not Applicable | — | Undefined | Undefined |
| $V_{POR} \le V_{DD} < V_{IT-}$ | Not Applicable | Ignored | High | Low |
| $V_{DD} \ge V_{IT+}$ | Disabled | Ignored | High | High |
| | Enabled | $t_{WC(max)} \le t_{pulse}$ [1] $\le t_{WC(max)} + t_{WO(min)}$ | High | High |
| | Enabled | $t_{WC(max)} > t_{pulse}$ [1] | Low | High |
| | Enabled | $t_{WC(max)} + t_{WO(max)} < t_{pulse}$ [1] | Low | High |

(1) Where $t_{pulse}$ is the time between falling edges on WDI.


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# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

### 9.1.1 CRST Delay

The TPS36-Q1 features two options for setting the reset delay ($t_D$): using a fixed timing and programming the timing through an external capacitor.

#### *9.1.1.1 Factory-Programmed Reset Delay Timing*

Fixed reset delay timings are available using pinouts C and D. Using these timings enables a high-precision, 10% accurate reset delay timing.

#### *9.1.1.2 Adjustable Capacitor Timing*

The TPS36-Q1 also offers programmable reset delay option when using pinout A and B. The TPS36-Q1 can be programmed to have a desired reset delay by connecting a capacitor between CRST pin and GND. The typical delay time resulting from a given external capacitance on the CRST pin can be calculated by 式 3 , where $t_D$ is the reset delay time in seconds and $C_{CRST}$ is the capacitance in farads.

$$t_D \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \quad (3)$$

To minimize the difference between the calculated reset delay time and the actual reset delay time, use a use a high-quality ceramic dielectric COG capacitor and minimize parasitic board capacitance around this pin. 表 9-1 lists the reset delay time ideal capacitor values for $C_{CRST}$.

**表 9-1. Reset Delay Time for Common Ideal Capacitor Values**

| $C_{CRST}$ | RESET DELAY TIME ($t_D$) | | | UNIT |
|---|---|---|---|---|
| | MIN (1) | TYP | MAX (1) | |
| 10 nF | 39.6 | 49.5 | 59.4 | ms |
| 100 nF | 396 | 495 | 594 | ms |
| 1 µF | 3960 | 4950 | 5940 | ms |

(1) Minimum and maximum values are calculated using ideal capacitors.

### 9.1.2 Watchdog Window Functionality

The TPS36-Q1 features two options for setting the close window watchdog timer ($t_{WC}$): using a fixed timing and programming the timing through an external capacitor.

#### *9.1.2.1 Factory-Programmed watchdog Timing*

Fixed watchdog window close timings are available using pinout C and D. Using these timings enables a high-precision, 10% accurate watchdog timer $t_{WC}$.

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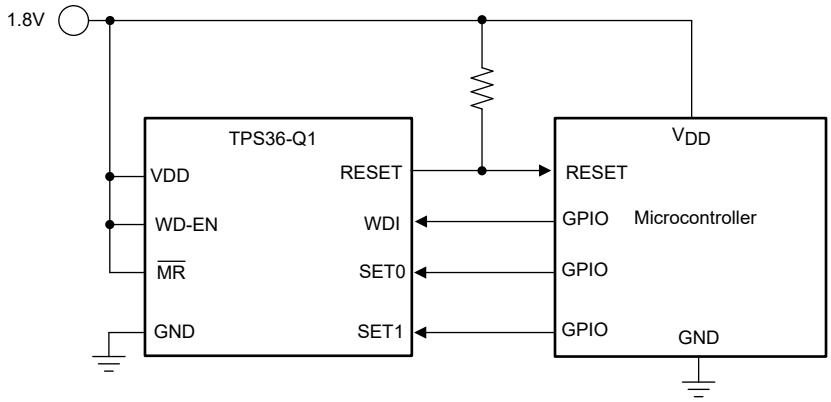
#### 9.1.2.2 Adjustable Capacitor Timing

Pinout options A and B support adjustable $t_{WC}$ timing. This is achievable by connecting a capacitor between CWD and GND pin. Consult 表 8-1, 表 8-2, and 表 8-3 for calculating typical $t_{WC}$ values using ideal capacitors. Capacitor tolerances will cause additional deviation. For the most accurate timing, use ceramic capacitors with COG dielectric material.

## 9.2 Typical Applications

### 9.2.1 Design 1: Monitoring Microcontroller Supply and Watchdog During Operational and Sleep Modes

The TPS36-Q1 can utilize high-accuracy voltage monitoring and on-the-fly SETx assigning to monitor a microcontroller that has both an operational and sleep mode.




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**図 9-1. Monitoring Microcontroller Supply and Watchdog During Operation and Sleep**

#### 9.2.1.1 Design Requirements

**表 9-2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT | DESIGN RESULT |
|---|---|---|
| Voltage Threshold | Typical Voltage Threshold of 1.65 V | Typical Voltage Threshold of 1.65 V |
| Window Close Time During Operation | Typical $t_{WC}$ of 50 ms during opertation | Typical $t_{WC}$ of 50 ms |
| Window Open Time During Operation | Typical $t_{WO}$ of 1.4 s during operation | Typical $t_{WO}$ of 1.55 s |
| Window Close Time During Sleep | Typical $t_{WC}$ of 50 ms during sleep | Typical $t_{WC}$ of 50 ms |
| Window Open Time During Sleep | Typical $t_{WO}$ of 12 s during operation | Typical $t_{WO}$ of 12.75 s |
| RESET Delay | 200 ms | 200 ms |
| Output Logic | Open-drain | Open-drain |
| Maximum Device Current Consumption | 20 µA | 250 nA typical, 3 µA maximum |

#### 9.2.1.2 Detailed Design Procedure

##### 9.2.1.2.1 Setting Voltage Threshold

The negative-going threshold voltage, $V_{IT-}$, is set by the device variant. 式 4 shows how to calculate the "Threshold Voltage" section of the orderable part number.

$$\text{OPN "Threshold Voltage" number} = (V_{IT-} - 1) / 0.05 \quad (4)$$


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In this example, the nominal supply voltage for the microcontroller is 1.8 V. The minimum supply voltage is 10% lower than the nominal supply voltage, or 1.62 V. Setting a 1.65 V threshold ensures that the device is reset just before the supply voltage reaches the minimum allowed. Thus a 1.65 V threshold is chosen and, using 式 4, the part number is reduced to TPS36xx13xxxxxxxQ1. The hysteresis is 5% typical, resulting in a positive-going threshold voltage, $V_{IT+}$, of 1.73 V.

#### 9.2.1.2.2 Determining Window Timings During Operation and Sleep Modes

The TPS36-Q1 allows for precise 10% accurate watchdog timings. This application requires two different window timings in order to maximize power efficiency: one for the microcontroller's operational state and one for its sleep state. To achieve this, the host can reassign the SETx pins when it transitions between states. A window close time, $t_{WC}$, of 50 ms typical is chosen because of the application's 50 ms typical $t_{WC}$ requirement. The application requires a minimum watchdog open time, $t_{WO}$, of 1.4 s during operation and a $t_{WO}$ of 12 s during sleep. Thus, the possible variant options are narrowed to TPS36xx13FExDDFRQ1.

#### 9.2.1.2.3 Meeting the Minimum Reset Delay

The TPS36-Q1 features two options for selecting reset delays: fixed delays and capacitor-programmable delays. The TPS36-Q1 supports only fixed watchdog timings and fixed reset delays or programmable watchdog timings and programmable reset delays. The application requires a 200 ms minimum reset delay, thus reset delay option G is used. Because of these requirements and no need for a startup delay, the TPS36CA13FEGDDFRQ1 is used.

#### 9.2.1.2.4 Setting the Watchdog Window

In this application, the watchdog timing options are based on the WDI signal that is provided to the TPS36-Q1. A watchdog WDI setting must be chosen such that a transition must always occur within the open watchdog window. There are several ways to achieve these window parameters. An external capacitor can be placed on the CWD pin and calculated to have a sufficient window close time. Another option is to use one of the factory-programmed timing options. An additional advantage of choosing one of the factory-programmed options is the ability to reduce the number of components required, thus reducing overall BOM cost.

#### 9.2.1.2.5 Calculating the $\overline{\text{RESET}}$ Pullup Resistor

The TPS36-Q1 uses an open-drain configuration for the $\overline{\text{RESET}}$ output, as shown in 図 9-2.When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET pulls the output to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that $V_{OL}$ is below its maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage ($V_{PU}$), the recommended maximum $\overline{\text{RESET}}$ pin current ($I_{RST}$), and $V_{OL}$. The maximum $V_{OL}$ is 0.3 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.3 V with $I_{RST}$ kept below 2 mA for $V_{DD}$ ≥ 3 V and 500 µA for $V_{DD}$ = 1.5 V. For this example, with a $V_{PU}$ =$V_{DD}$ = 1.5 V, a resistor must be chosen to keep $I_{RST}$ below 500 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 10 kΩ was selected, which sinks a maximum of 180 µA when $\overline{\text{RESET}}$ is asserted.

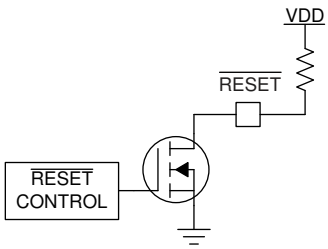



**図 9-2. Open-Drain $\overline{\text{RESET}}$ Configuration**

## 9.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.04 V and 6 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

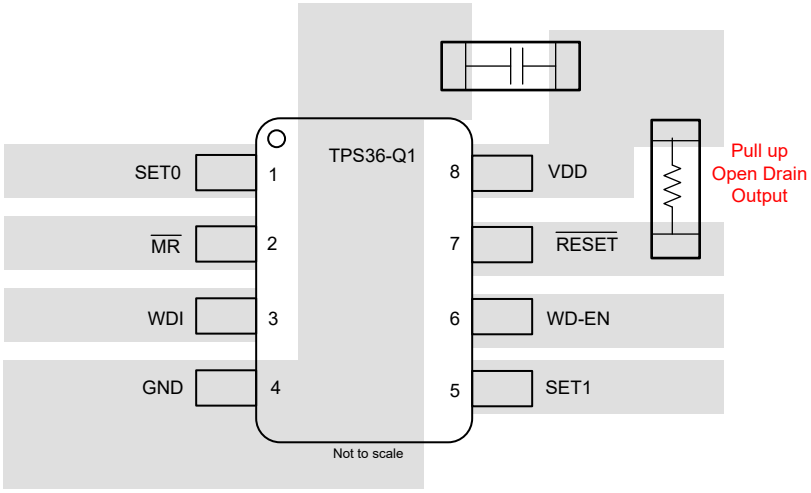
## 9.4 Layout

### 9.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{\text{RESET}}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- Place $C_{CRST}$ capacitor as close as possible to the CRST pin.
- Place $C_{CWD}$ capacitor as close as possible to the CWD pin.
- Place the pullup resistor on the $\overline{\text{RESET}}$ pin as close to the pin as possible.

### 9.4.2 Layout Example




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**図 9-3. Typical Layout for the pinout C of TPS36-Q1**

# 10 Device and Documentation Support

## 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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### 10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS36BA12ACADDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLLOA |
| TPS36BA12ACADDFRQ1.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLLOA |
| TPS36BA38ACADDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOB |
| TPS36BA38ACADDFRQ1.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOB |
| TPS36CA39EACDDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOO |
| TPS36CA39EACDDFRQ1.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOO |
| TPS36CA66BECDDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOD |
| TPS36CA66BECDDFRQ1.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOD |
| TPS36CB66EACDDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHO9 |
| TPS36CD40EACDDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOV |
| TPS36CD40EACDDFRQ1.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NLHOV |
| TPS36DD75HBCDDFRQ1 | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNLHO |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

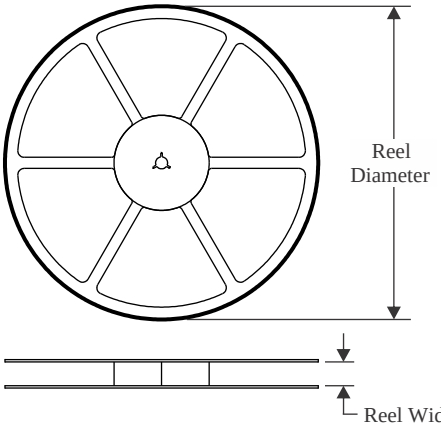
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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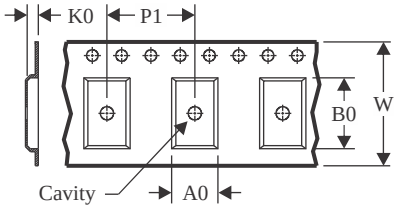
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

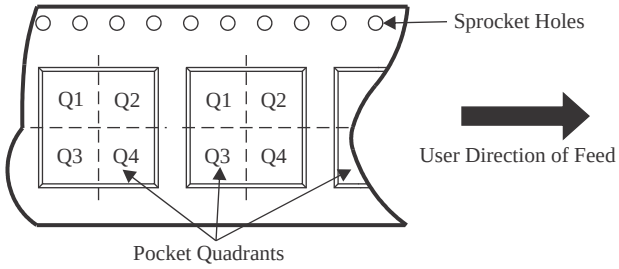



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

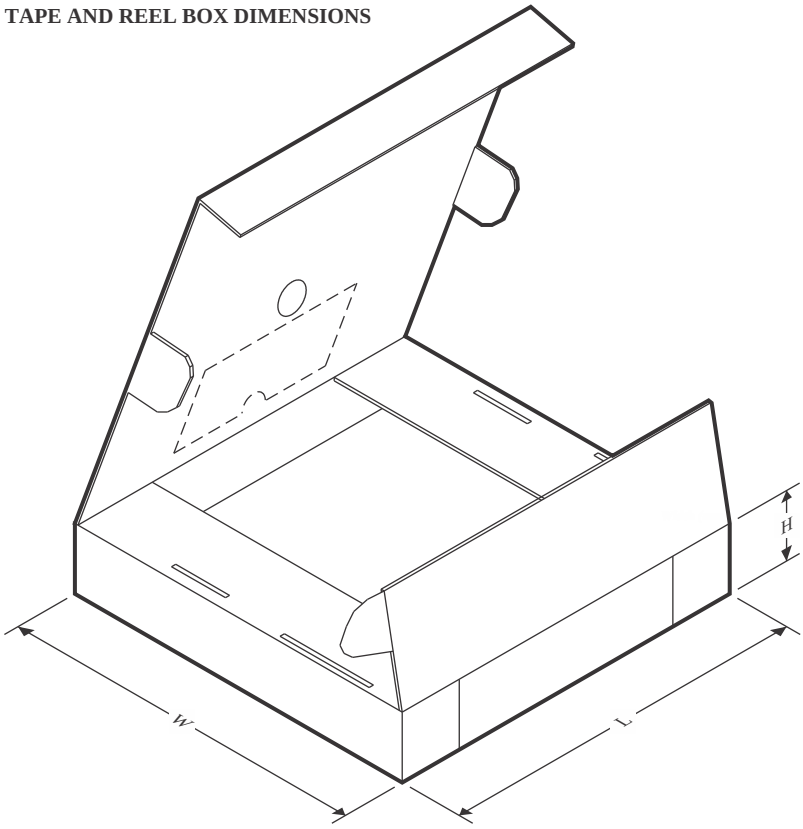
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS36BA12ACADDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS36BA38ACADDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS36CA39EACDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS36CA66BECDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS36CB66EACDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS36CD40EACDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS36DD75HBCDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

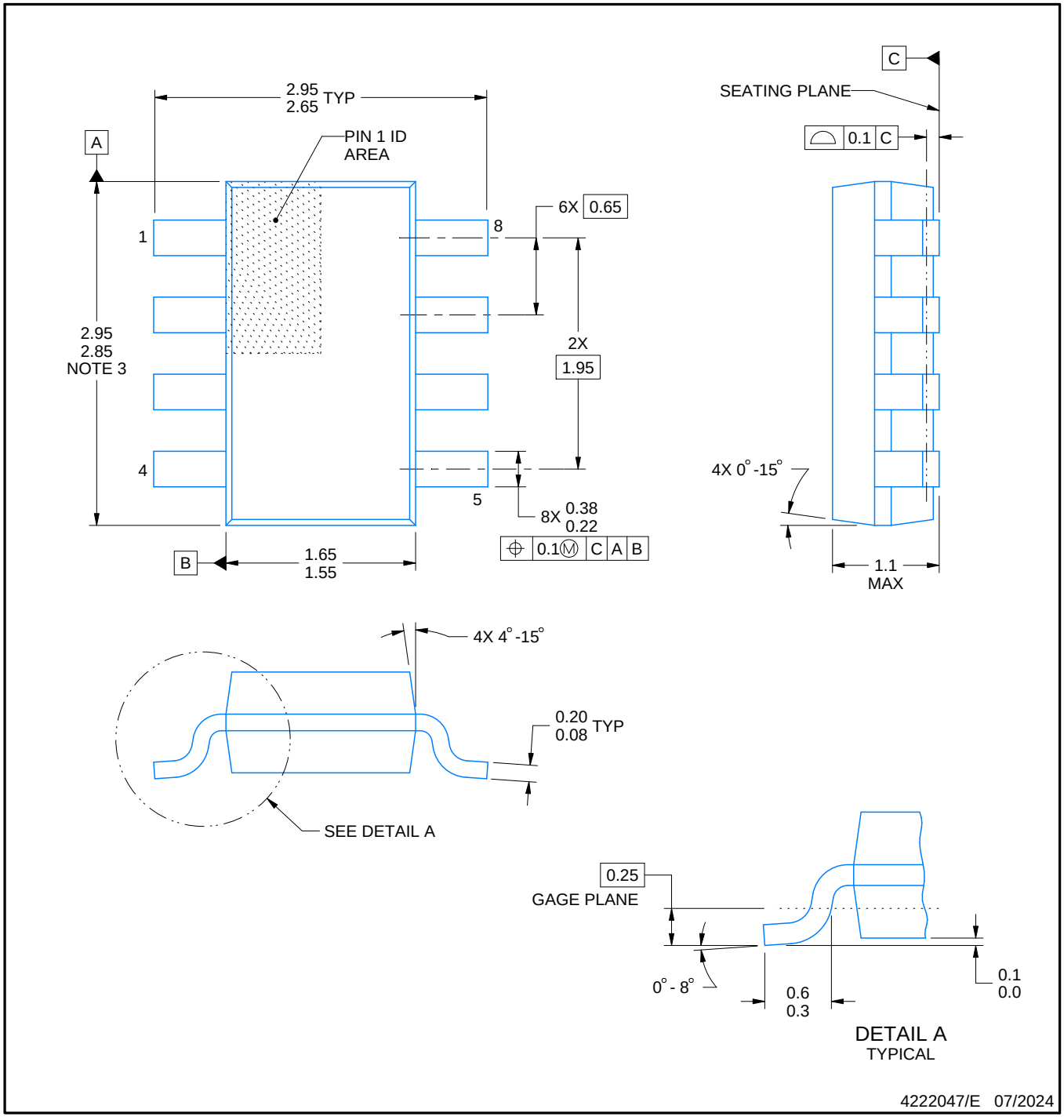
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS36BA12ACADDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS36BA38ACADDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS36CA39EACDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS36CA66BECDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS36CB66EACDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS36CD40EACDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS36DD75HBCDDFRQ1 | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DDF0008A

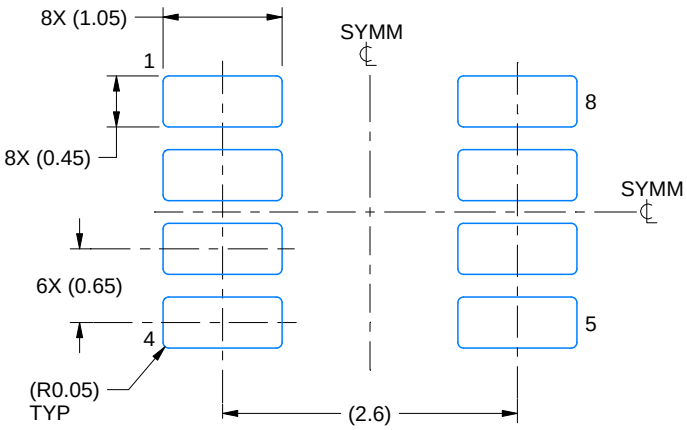
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

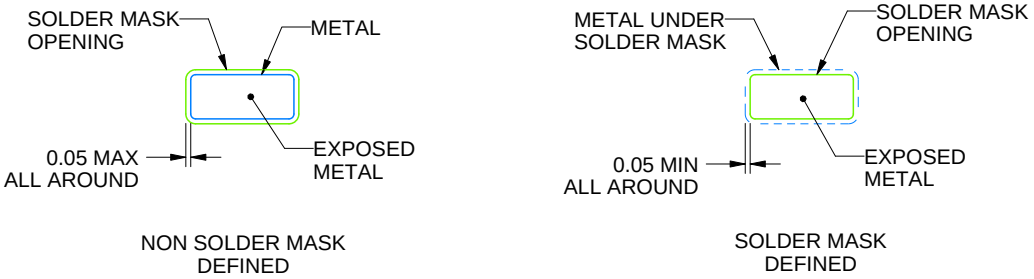



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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NOTES: (continued)

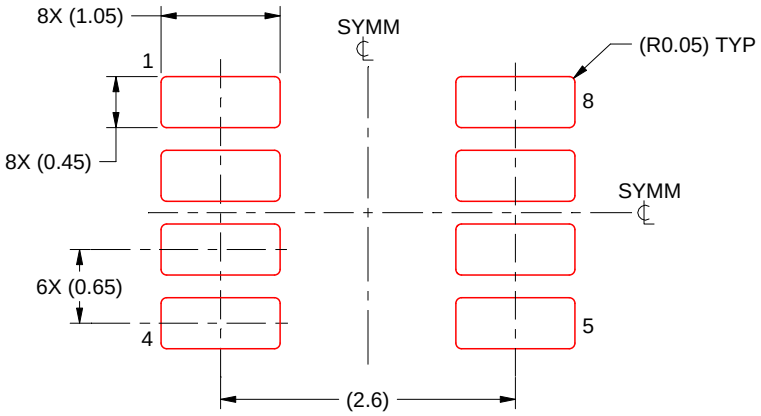
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DDF0008A

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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