TPS3700 過電圧および低電圧監視用の基準電圧を内蔵した 高電圧 (18V) ウィンドウ電圧検出器

1 特長

- 広い電源電圧範囲: 1.8V～18V
- スレッショルドを変更可能：最低 400mV
- スレッショルドの高い精度
  - 温度範囲全体で 1.0%
  - 0.25% (標準値)
- 低い静止電流： 5.5µA (標準値)
- 過電圧および低電圧検出用のオープン・ドレイン出力
- 内部ヒステリシス： 5.5mV (標準値)
- 温度範囲: -40°C～+125°C
- パッケージ:
  - SOT-6
  - 1.5mm×1.5mm WSON-6

2 アプリケーション

- 産業用制御システム
- 車載用システム
- 組み込みコンピューティング・モジュール
- DSP、マイクロコントローラ、マイクロプロセッサのアプリケーション
- ノート PC およびデスクトップ PC
- 携帯用およびバッテリ駆動の製品
- FPGA および ASIC アプリケーション

3 概要

TPS3700 は電源電圧範囲の広いウィンドウ電圧検出器で、1.8V～18V の範囲で動作します。このデバイスには高精度コンパレータが 2 つ、内部的な 400mV の基準電圧、および過電圧と低電圧検出用の 18V 定格のオープンドレイン出力が 2 つ内蔵されています。TPS3700 はウィンドウ電圧検出器としても、2 つの独立した電圧モニタとしても使用でき、監視対象の電圧は外付け抵抗により設定できます。

OUTAは、INA+の電圧が(V_{ITP} - V_{HYS})より低くなるとLOWに駆動され、対応するスレッショルド(V_{ITP})より高い電圧に戻るとHIGHに復帰します。OUTBは、INB-の電圧がV_{ITP}より高くなるとLOWに駆動され、対応するスレッショルド(V_{ITP} - V_{HYS})より低い電圧に戻るとHIGHに復帰します。TPS3700のコンパレータは両方とも、短時間のグリッチを除去するためヒステリシスが組み込まれているので、誤ったトリガが発生せず、安定した出力動作が保証されます。

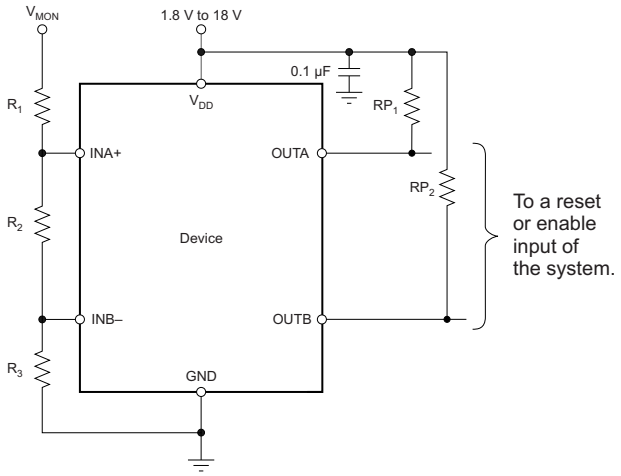
TPS3700はSOT-6および1.5mm×1.5mmのWSON-6パッケージで供給され、-40℃～125℃の接合部温度範囲で動作が規定されています。

製品情報(1)

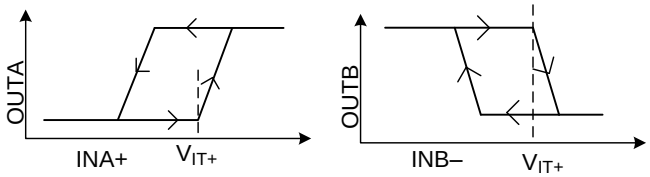
型番	パッケージ	本体サイズ(公称)
TPS3700	SOT (6)	2.90mm×1.60mm
	WSON (6)	1.50mm×1.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



出力と入力のスレッショルドとヒステリシスの関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 3
5 **Pin Configuration and Functions** ... 4
6 **Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Timing Requirements ... 7
6.7 Switching Characteristics ... 7
6.8 Typical Characteristics ... 8
7 **Detailed Description** ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 12
8 **Application and Implementation** ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 16
8.3 Do's and Don'ts ... 18
9 **Power-Supply Recommendations** ... 19
10 **Layout** ... 19
10.1 Layout Guidelines ... 19
10.2 Layout Example ... 19
11 デバイスおよびドキュメントのサポート ... 20
11.1 デバイス・サポート ... 20
11.2 ドキュメントのサポート ... 20
11.3 ドキュメントの更新通知を受け取る方法 ... 20
11.4 コミュニティ・リソース ... 20
11.5 商標 ... 20
11.6 静電気放電に関する注意事項 ... 20
11.7 Glossary ... 21
12 メカニカル、パッケージ、および注文情報 ... 21

Copyright © 2012–2019, Texas Instruments Incorporated

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (January 2018) から Revision G に変更 **Page**

- データシート全体を通してコンパレータを電圧検出器に 変更 1

Revision E (February 2017) から Revision F に変更 **Page**

- データシート全体を通してコンパレータをスーパーバイザに 変更 1

Revision D (January 2015) から Revision E に変更 **Page**

- Added maximum specification to *Start-up delay* parameter 6
- Changed *at least 150 µs* to *450 µs (max)* in footnote 2 of *Electrical Characteristics* table 6

Revision C (May 2013) から Revision D に変更 **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 5
- Changed HBM maximum specification from 2 kV to 2.5 kV in *ESD Ratings* 5
- Changed *Functional Block Diagram*; added hysteresis symbol 10

Revision B (April 2012) から Revision C に変更 **Page**

- 特長の箇条書きの「パッケージ」項目を 変更 1
- 「概要」セクションにSON-6パッケージ・オプションを 追加 1
- 表紙にDSEピン配置の図を 追加 1
- Added DSE pin out graphic 4
- Added DSE package to Thermal Information table 5

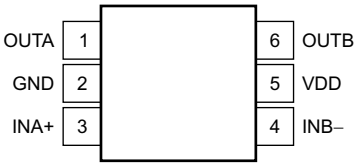
Revision A (February 2012) から Revision B に変更 **Page**

- 量産データに移行 1

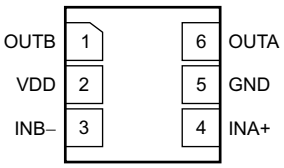
Copyright © 2012–2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

DDC Package
SOT-6
Top View



DSE Package
WSON-6
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DDC	DSE		
GND	2	5	—	Ground
INA+	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage (V_{ITP} – V_{HYS}), OUTA is driven low.
INB–	4	3	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), OUTB is driven low.
OUTA	1	6	O	INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below (V_{ITP} – V_{HYS}). The output goes high when the sense voltage returns above the respective threshold (V_{ITP}).
OUTB	6	1	O	INB– comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds V_{ITP}. The output goes high when the sense voltage returns below the respective threshold (V_{ITP} – V_{HYS}).
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.

Copyright © 2012–2019, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	V_{DD}	–0.3	20	V
	OUTA, OUTB	–0.3	20	V
	INA+, INB–	–0.3	7	V
Current	Output terminal current		40	mA
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.8		18	V
V_I	Input voltage	INA+, INB–	0		6.5	V
V_O	Output voltage	OUTA, OUTB	0		18	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS3700		UNIT
		DDC (SOT)	DSE (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.5	128.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	153.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.8	157.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2012–2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, and 1.8 V < V_{DD} < 18 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		18	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL}max = 0.2 V, $I_{(OUTA/B)}$ = 15 µA			0.8	V
V_{IT+}	Positive-going input threshold voltage	V_{DD} = 1.8 V	396	400	404	mV
		V_{DD} = 18 V	396	400	404	
$V_{IT–}$	Negative-going input threshold voltage	V_{DD} = 1.8 V	387	394.5	400	mV
		V_{DD} = 18 V	387	394.5	400	
V_{hys}	Hysteresis voltage (hys = V_{IT+} – $V_{IT–}$)			5.5	12	
$I_{(INA+)}$	Input current (at the INA+ terminal)	V_{DD} = 1.8 V and 18 V, V_I = 6.5 V	–25	1	25	nA
$I_{(INB–)}$	Input current (at the INB– terminal)	V_{DD} = 1.8 V and 18 V, V_I = 0.1 V	–15	1	15	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3 V, I_O = 0.4 mA			250	mV
		V_{DD} = 1.8 V, I_O = 3 mA			250	
		V_{DD} = 5 V, I_O = 5 mA			250	
$I_{lkg(OD)}$	Open-drain output leakage-current	V_{DD} = 1.8 V and 18 V, V_O = V_{DD}			300	nA
		V_{DD} = 1.8 V, V_O = 18 V			300	
I_{DD}	Supply current	V_{DD} = 1.8 V, no load		5.5	11	µA
		V_{DD} = 5 V		6	13	
		V_{DD} = 12 V		6	13	
		V_{DD} = 18 V		7	13	
	Start-up delay(2)			150	450	µs
UVLO	Undervoltage lockout(3)	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) During power on, V_{DD} must exceed 1.8 V for 450 µs (max) before the output is in a correct state.
(3) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below $V_{(POR)}$.

Copyright © 2012–2019, Texas Instruments Incorporated

6.6 Timing Requirements

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{PHL}	High-to-low propagation delay(1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV, see Figure 1		18		µs
t_{PLH}	Low-to-high propagation delay(1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV, see Figure 1		29		µs

(1) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB–).

6.7 Switching Characteristics

Over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		µs
t_f	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		µs

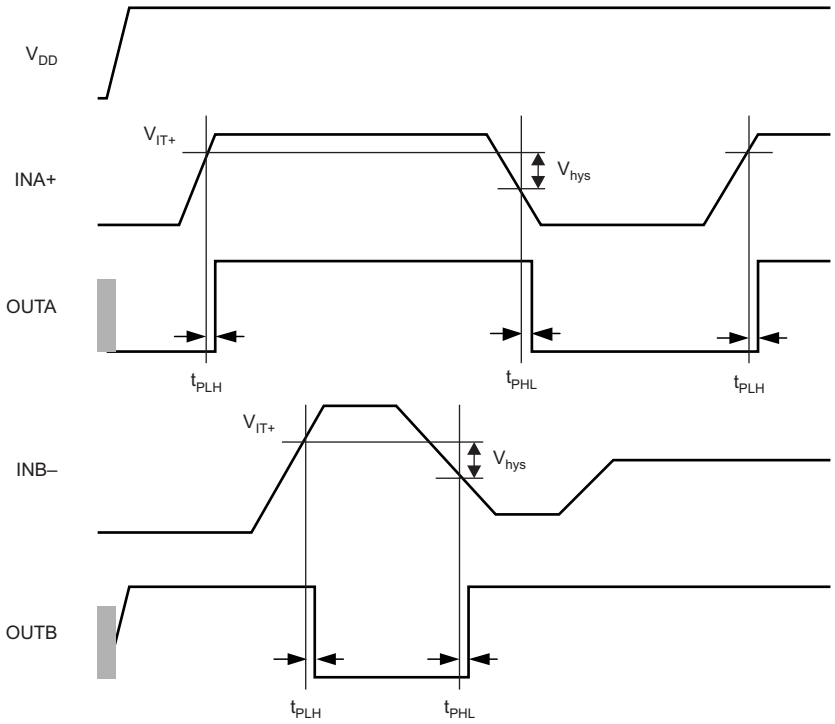


Figure 1. Timing Diagram

6.8 Typical Characteristics

at T_J = 25°C and V_{DD} = 5 V (unless otherwise noted)

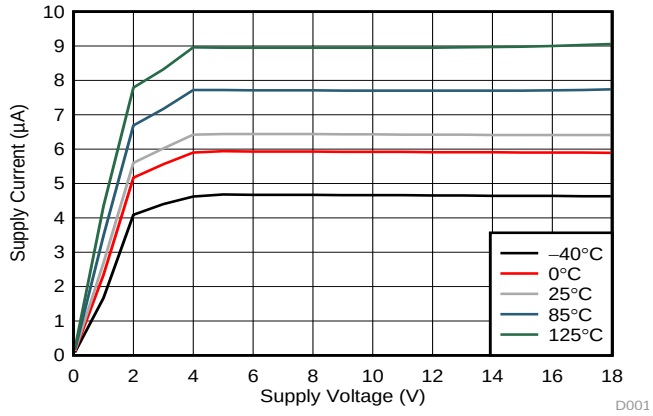


Figure 2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

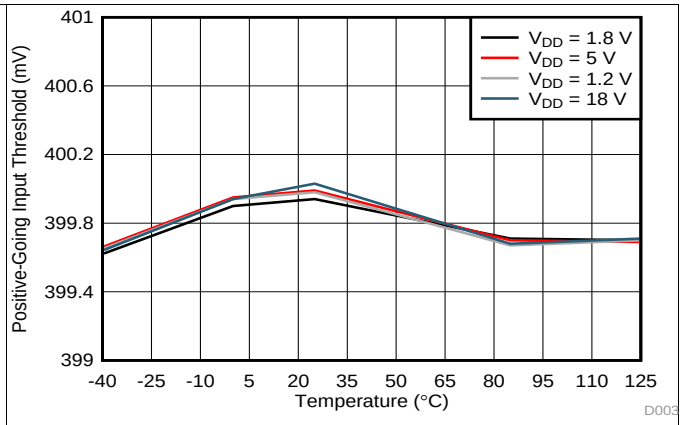


Figure 3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

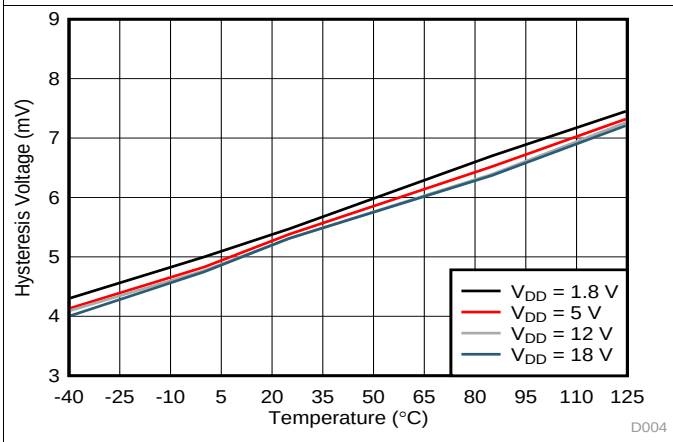


Figure 4. Hysteresis (V_{hys}) vs Temperature

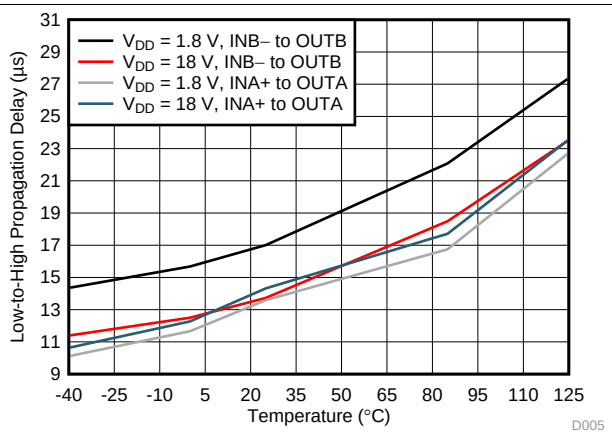


Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

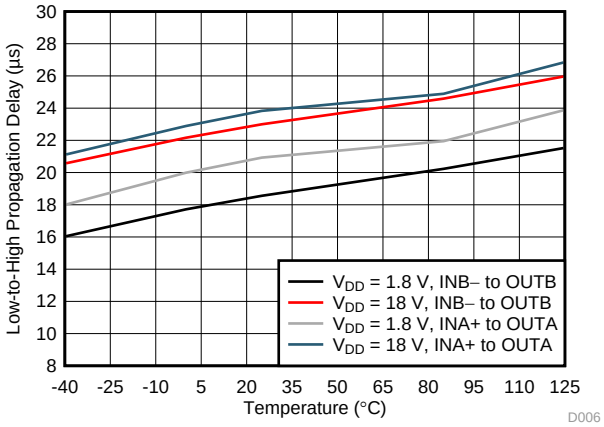
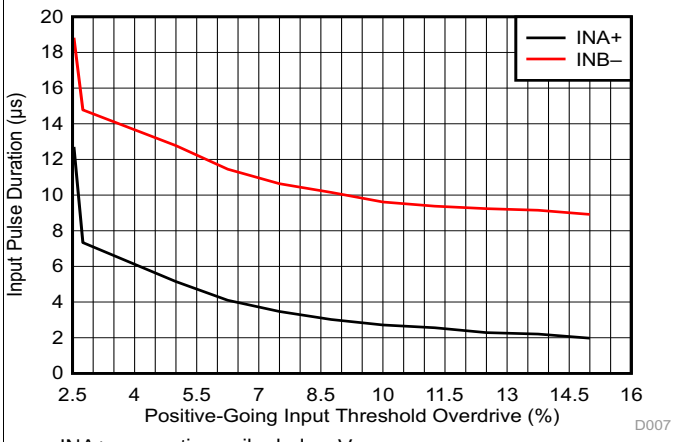


Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)



INA+ = negative spike below $V_{IT–}$

INB– = positive spike above V_{IT+}

Figure 7. Minimum Pulse Duration vs Threshold Overdrive Voltage

Copyright © 2012–2019, Texas Instruments Incorporated

Typical Characteristics (continued)

at T_J = 25°C and V_{DD} = 5 V (unless otherwise noted)

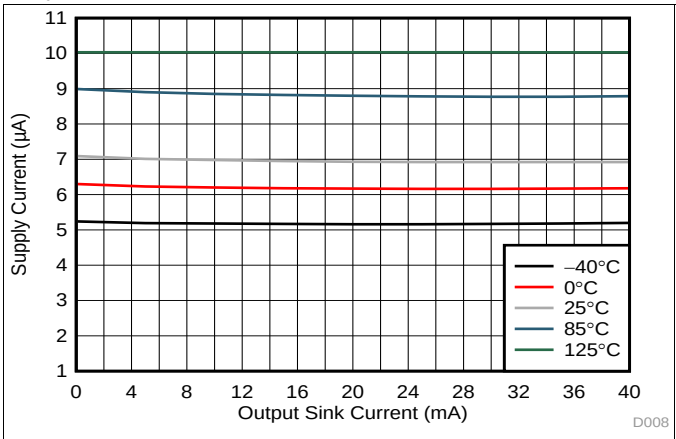


Figure 8. Supply Current (I_{DD}) vs Output Sink Current

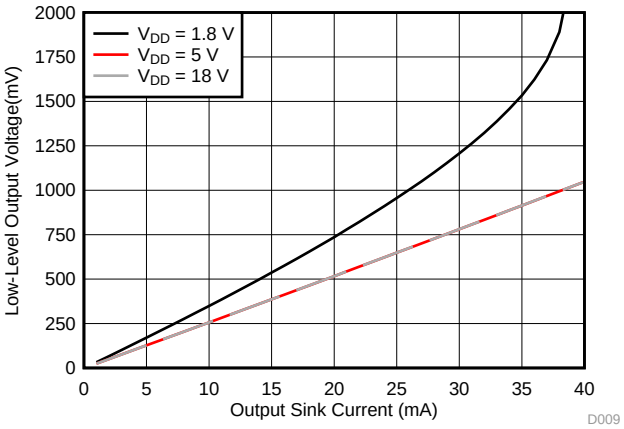


Figure 9. Output Voltage Low (V_{OL}) vs Output Sink Current (–40°C)

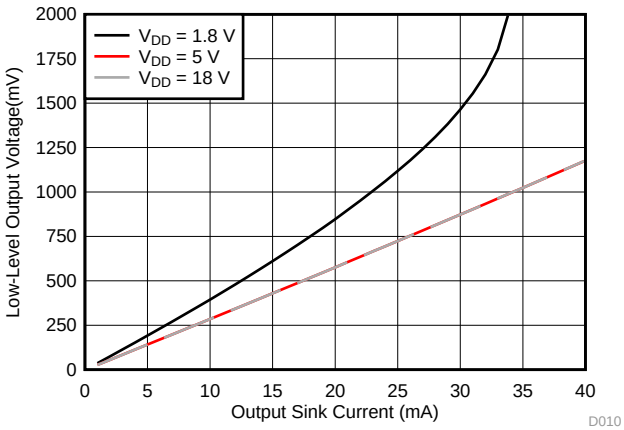


Figure 10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

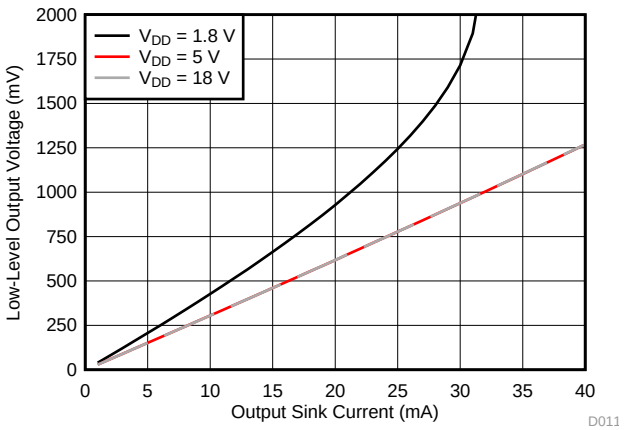


Figure 11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

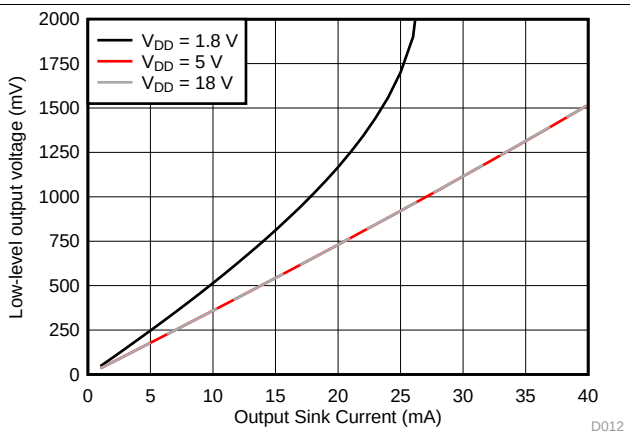


Figure 12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

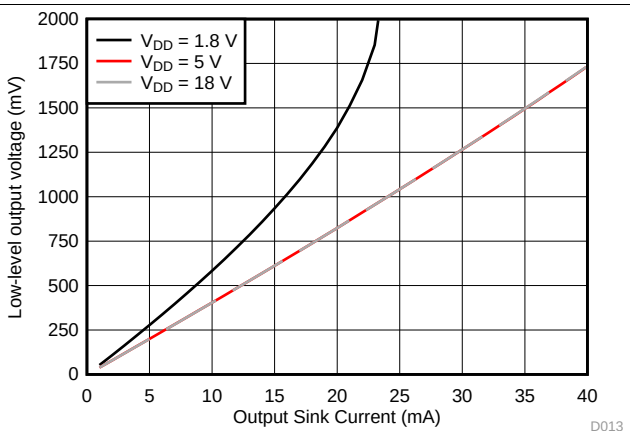


Figure 13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

Copyright © 2012–2019, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

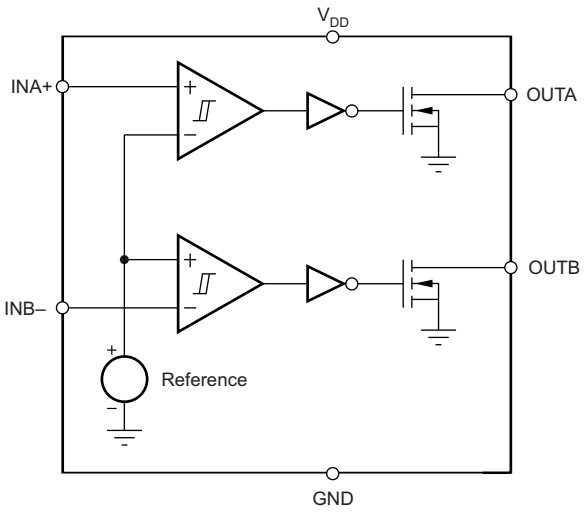
The TPS3700 device combines two voltage detectors for overvoltage and undervoltage detection. The TPS3700 device is a wide-supply voltage range (1.8 V to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V and can sink up to 40 mA.

The TPS3700 device is designed to assert the output signals, as shown in Table 1. Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. With the use of two input terminals of different polarities, the TPS3700 device forms a window voltage detector. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

Table 1. TPS3700 Truth Table

CONDITION	OUTPUT	STATUS
INA+ > V_{IT+}	OUTA high	Output A not asserted
INA+ < V_{IT-}	OUTA low	Output A asserted
INB– > V_{IT+}	OUTB low	Output B asserted
INB– < V_{IT-}	OUTB high	Output B not asserted

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inputs (INA+, INB–)

The TPS3700 device is a voltage detector that combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The INA+ and INB- inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below (V_{IT+} – V_{hys}). When the voltage exceeds V_{IT+}, the output (OUTA) goes to a high-impedance state; see Figure 1.

Copyright © 2012–2019, Texas Instruments Incorporated

Feature Description (continued)

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB– exceeds V_{IT+}. When the voltage drops below $V_{IT+} – V_{hys}$ the output (OUTB) goes to a high-impedance state; see Figure 1. Together, these comparators form a window-detection function as discussed in the *Window Voltage Detector* section.

7.3.2 Outputs (OUTA, OUTB)

In a typical TPS3700 application, the outputs are connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the outputs are connected to the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator [LDO]).

The TPS3700 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TPS3700 outputs can be pulled up to 18 V, independent of the device supply voltage. By using wired-OR logic, OUTA and OUTB can merge into one logic signal that goes low if either outputs are asserted because of a fault condition.

Table 1 and the *Inputs (INA+, INB–)* section describe how the outputs are asserted or deasserted. See Figure 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

7.3.3 Window Voltage Detector

The inverting and noninverting configuration of the comparators forms a window-voltage detection circuit using a resistor divider network, as illustrated in Figure 14 and Figure 15. The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB– terminals monitor for undervoltage and overvoltage conditions, respectively.

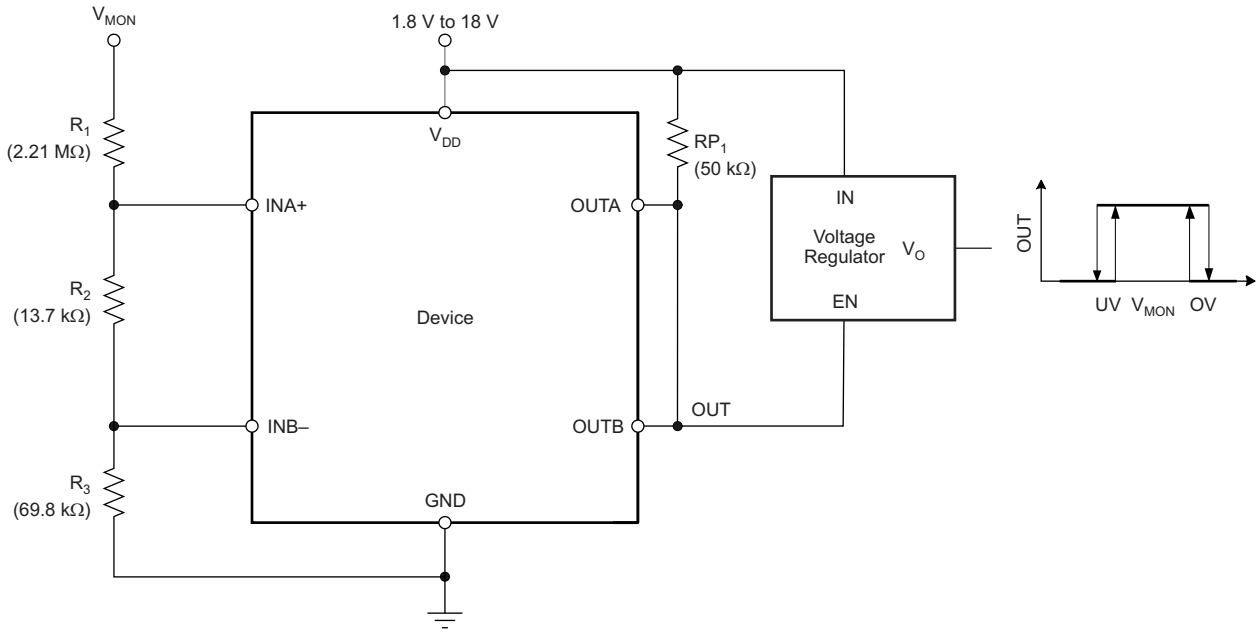


Figure 14. Window Voltage Detector Block Diagram

Feature Description (continued)

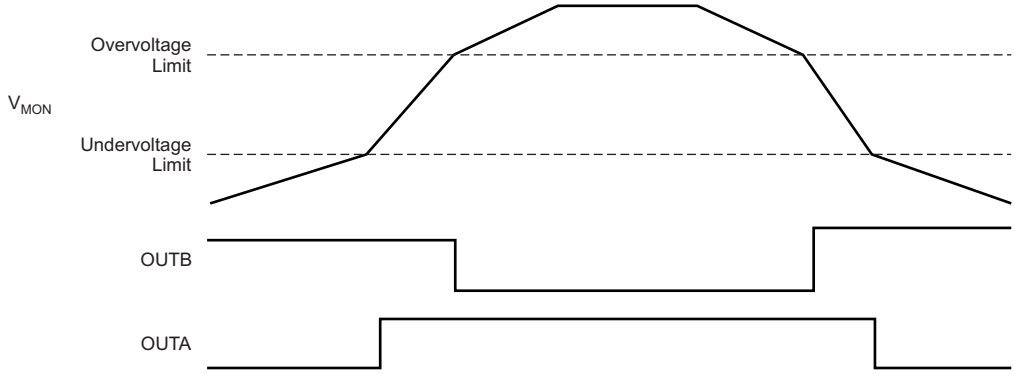


Figure 15. Window Voltage Detector Timing Diagram

7.3.4 Immunity to Input Terminal Voltage Transients

The TPS3700 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients depends on both transient duration and amplitude; see the *Minimum Pulse Duration vs Threshold Overdrive Voltage* curve (Figure 7) in the *Typical Characteristics* section.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on V_{DD} is greater than 1.8 V for at least 150 µs, the OUTA and OUTB signals correspond to the voltage on INA+ and INB– as listed in Table 1.

7.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD}$ < UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA+ and INB–.

7.4.3 Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on V_{DD} is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

Copyright © 2012–2019, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3700 device is a wide-supply window voltage detector that operates over a V_{DD} range of 1.8 V to 18 V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window voltage detector or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

8.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The outputs are often tied to V_{DD} through a resistor. However, some applications may require the outputs to be pulled up to a higher or lower voltage than V_{DD} to correctly interface with the reset and enable terminals of other devices.

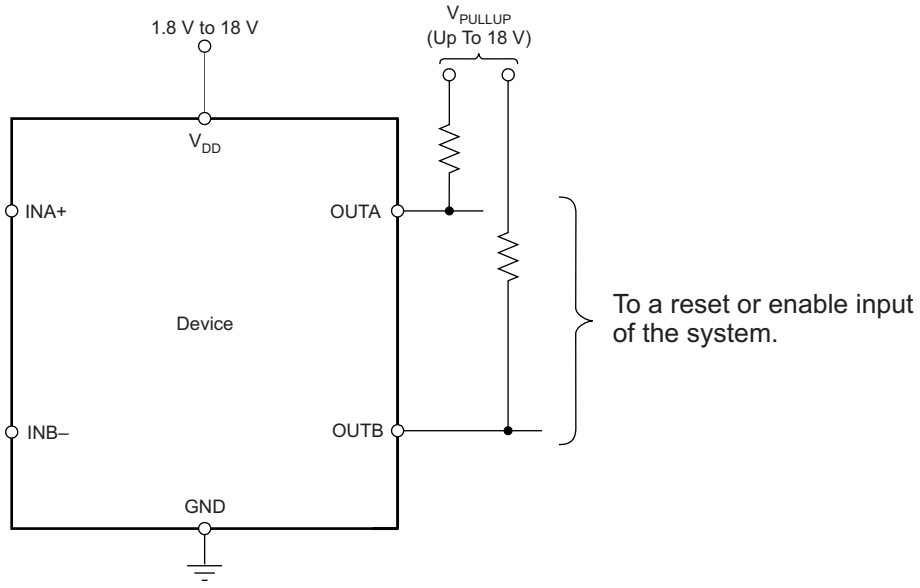


Figure 16. Interfacing to Voltages Other Than V_{DD}

Application Information (continued)

8.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD}. In these applications the resistor divider is simply connected to the V_{DD} rail.

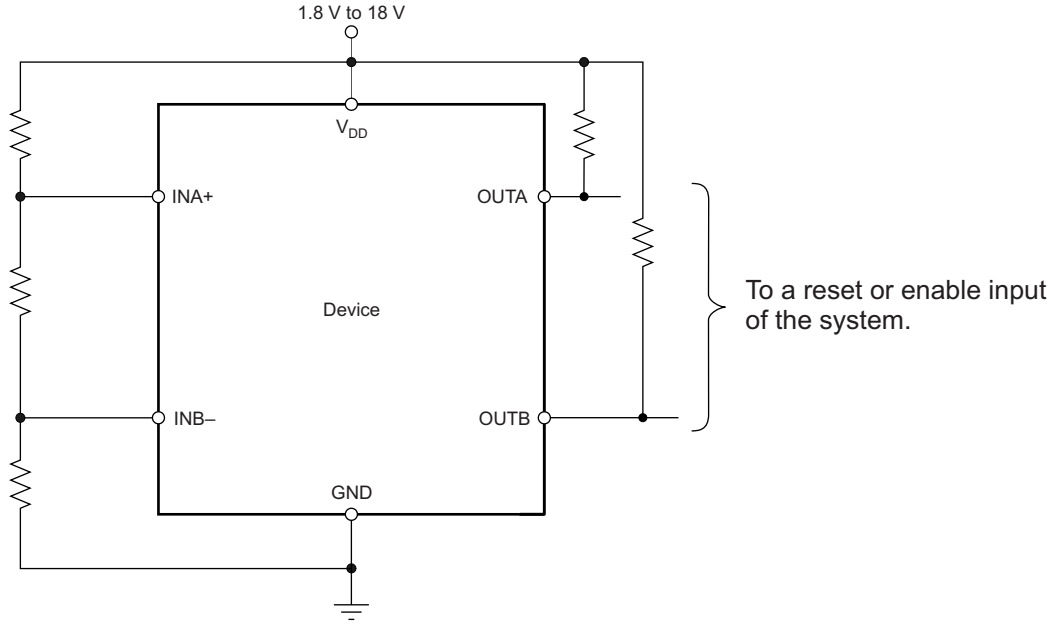
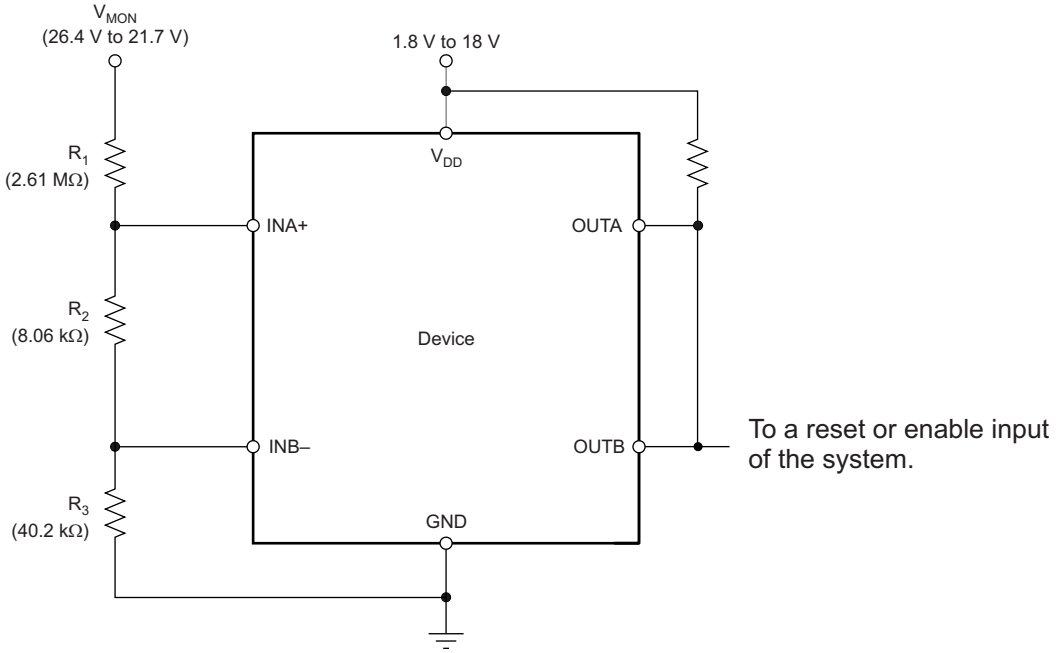


Figure 17. Monitoring the Same Voltage as V_{DD}

8.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD}. In these types of applications the resistor divider used to set the desired thresholds is connected to the rail that is being monitored.



NOTE: The inputs can monitor a voltage higher than V_{DD}max with the use of an external resistor divider network.

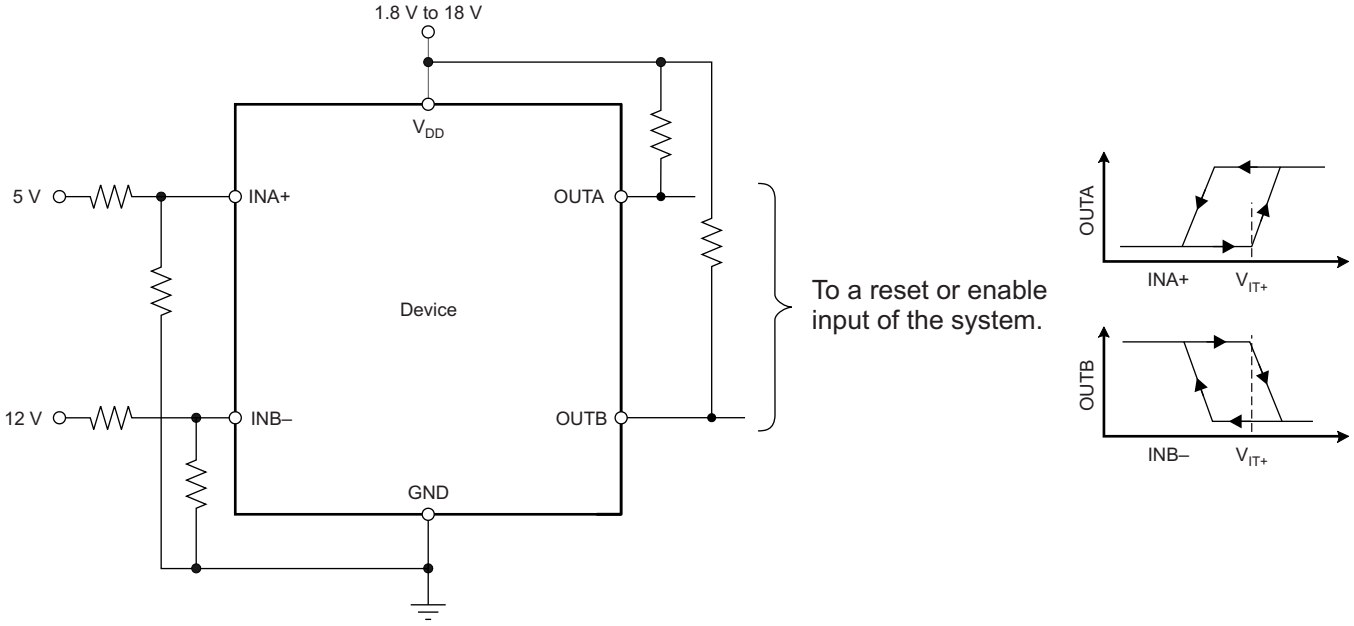
Figure 18. Monitoring a Voltage Other Than V_{DD}

Copyright © 2012–2019, Texas Instruments Incorporated

Application Information (continued)

8.1.4 Monitoring Overvoltage and Undervoltage for Separate Rails

Some applications may want to monitor for overvoltage conditions on one rail while also monitoring for undervoltage conditions on a different rail. In these applications two independent resistor dividers must be used.



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

Figure 19. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

Copyright © 2012–2019, Texas Instruments Incorporated

8.2 Typical Application

The TPS3700 device is a wide-supply window voltage detector that operates over a V_{DD} range of 1.8 to 18 V. The monitored voltages are set with the use of external resistors, so the device can be used either as a window voltage detector or as two independent overvoltage and undervoltage monitors.

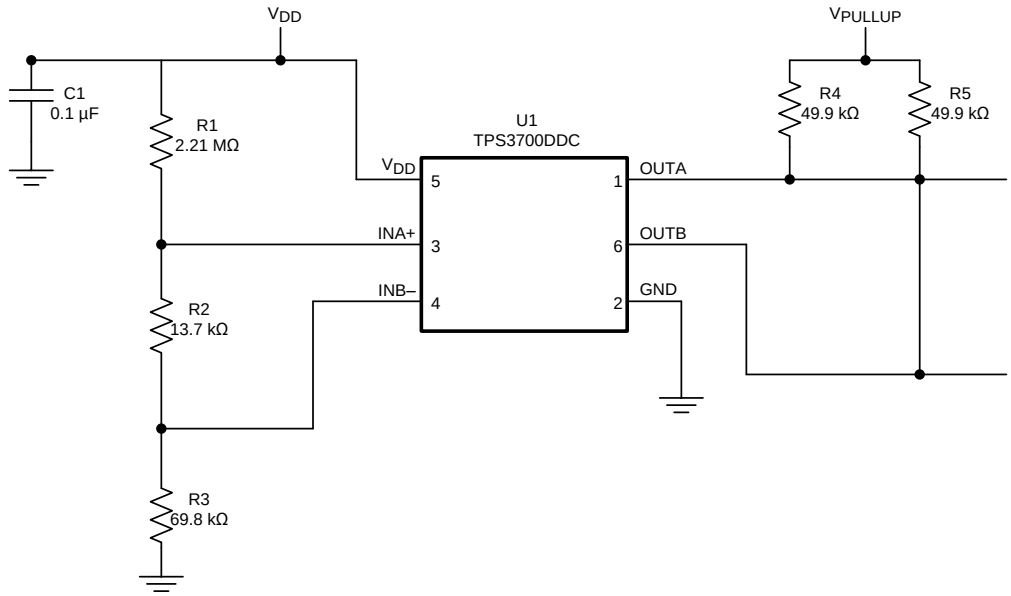


Figure 20. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the values summarized in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum rising and falling thresholds of ±10%	$V_{MON(UV)}$= 10.99 V (8.33%) ±2.94%, $V_{MON(OV)}$= 13.14 V (8.33%) ±2.94%

8.2.2 Detailed Design Procedure

8.2.2.1 Resistor Divider Selection

Use Equation 1 through Equation 4 to calculate the resistor divider values and target threshold voltages.

$$R_T = R_1 + R_2 + R_3 \quad (1)$$

Select a value for R_T such that the current through the divider is approximately 100 times higher than the input current at the INA+ and INB– terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for details on sizing input resistors.

Use Equation 2 to calculate the value of R_3.

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+} \quad (2)$$

where:

$V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected

Copyright © 2012–2019, Texas Instruments Incorporated

Use Equation 3 or Equation 4 to calculate the value of R_2.

$$R_2 = \left(\frac{R_T}{V_{MON}\,(\text{no UV})} \times V_{IT+} \right) - R_3$$

where:

$V_{MON(no\ UV)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises (3)

$$R_2 = \left(\frac{R_T}{V_{MON(UV)}} \times (V_{IT+} - V_{hys}) \right) - R_3$$

where:

$V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected (4)

The worst-case tolerance can be calculated by referring to Equation 13 in application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input* (available for download at www.ti.com). An example of the rising threshold error, $V_{MON(OV)}$, is given in Equation 5.

$$\%\ ACC = \%\ TOL(V_{IT+(INB)}) + 2 \times \left(1 - \frac{V_{IT+(INB)}}{V_{MON(OV)}} \right) \times \%\ TOL_R = 1\% + 2 \times \left(1 - \frac{0.4}{13.2} \right) \times 1\% = 2.94\% \quad (5)$$

8.2.2.2 Pullup Resistor Selection

To ensure proper voltage levels, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ($I_{lkg(OD)}$) multiplied by the resistor is greater the desired logic-high voltage. These values are specified in the *Electrical Characteristics* table.

Use Equation 6 to calculate the value of the pullup resistor.

$$\frac{(V_{HI} - V_{PU})}{I_{lkg(OD)}} \geq R_{PU} \geq \frac{V_{PU}}{I_O} \quad (6)$$

8.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, connecting a 0.1-µF low equivalent series resistance (ESR) capacitor across the V_{DD} terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

8.2.2.4 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB–) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.

Copyright © 2012–2019, Texas Instruments Incorporated

8.2.3 Application Curves

At T_J = 25°C

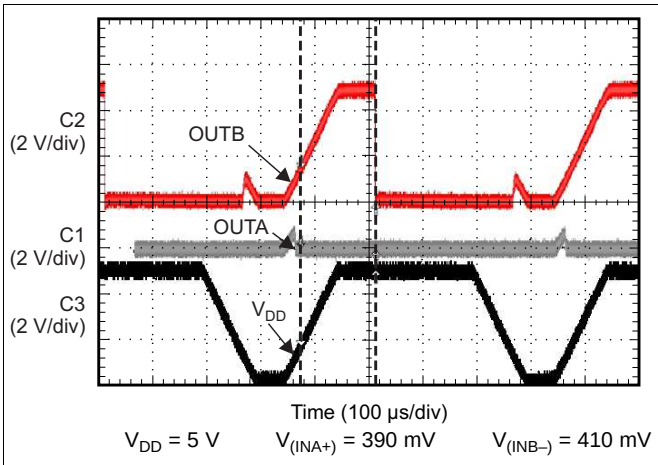


Figure 21. Start-Up Delay (Outputs Pulled Up to V_{DD})

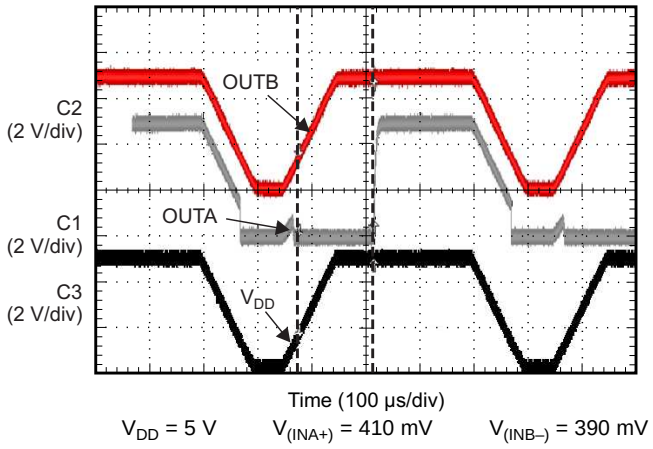


Figure 22. Start-Up Delay (Outputs Pulled Up to V_{DD})

8.3 Do's and Don'ts

It is good analog design practice to have a 0.1-µF decoupling capacitor from V_{DD} to GND.

If the monitored rail is noisy, connect decoupling capacitors from the comparator inputs to GND.

Do not use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparators without also accounting for the effect to the accuracy.

Do not use pullup resistors that are too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

Copyright © 2012–2019, Texas Instruments Incorporated

9 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.8 V and 18 V.

10 Layout

10.1 Layout Guidelines

Placing a 0.1-µF capacitor close to the V_{DD} terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (as shown in Figure 23) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.

10.2 Layout Example

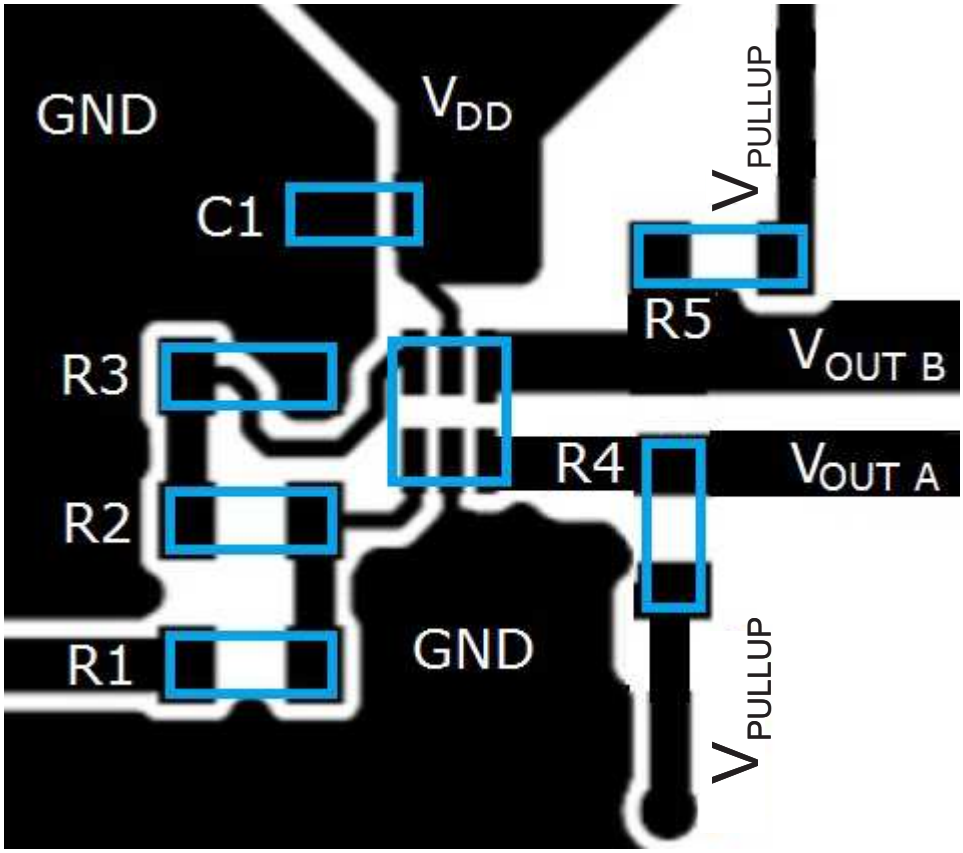


Figure 23. TPS3700 Layout Schematic

Copyright © 2012–2019, Texas Instruments Incorporated

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価基板

TPS3700を使用する回路の性能の初期評価に役立てるため、2つの評価基板(EVM)を利用可能です。TPS3700EVM-114評価基板およびTPS3700EVM-202評価基板(および関連するユーザー・ガイド)は、テキサス・インスツルメンツWebサイトのTPS3700製品フォルダで請求するか、TI eStoreから直接お求めになれます。

11.1.2 デバイスの項目表記

表 3. デバイスの項目表記

製品名	概要
TPS3700**yyyz**	**yyy**はパッケージ指定子 **z**はパッケージ数量

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『負のレールの過電圧と低電圧の検出器としてTPS3700を使用』*
- *『コンパレータ入力の分圧抵抗の最適化』*
- *『TPS3700EVM-114評価基板ユーザー・ガイド』*
- *『TPS3700EVM-202評価基板ユーザー・ガイド』*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

Copyright © 2012–2019, Texas Instruments Incorporated

11.7 Glossary

SLYZ022 — *TI Glossary*.

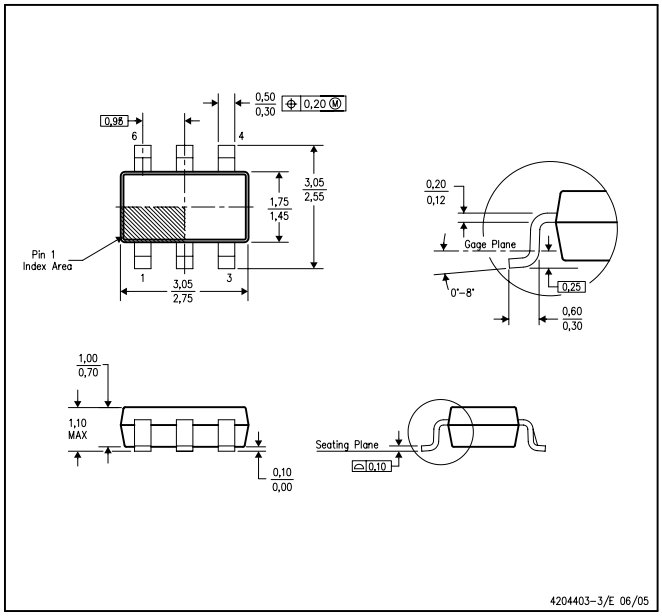
This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

MECHANICAL DATA

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE

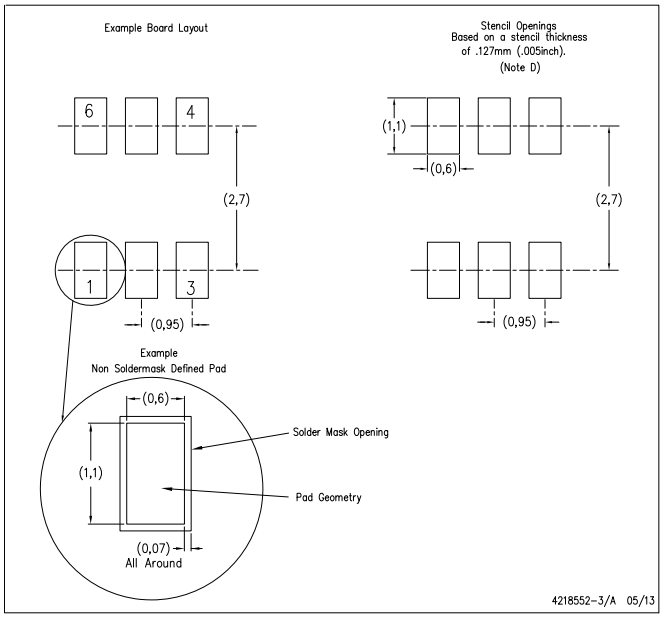


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

図 0. UNDEFINED

LAND PATTERN DATA

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



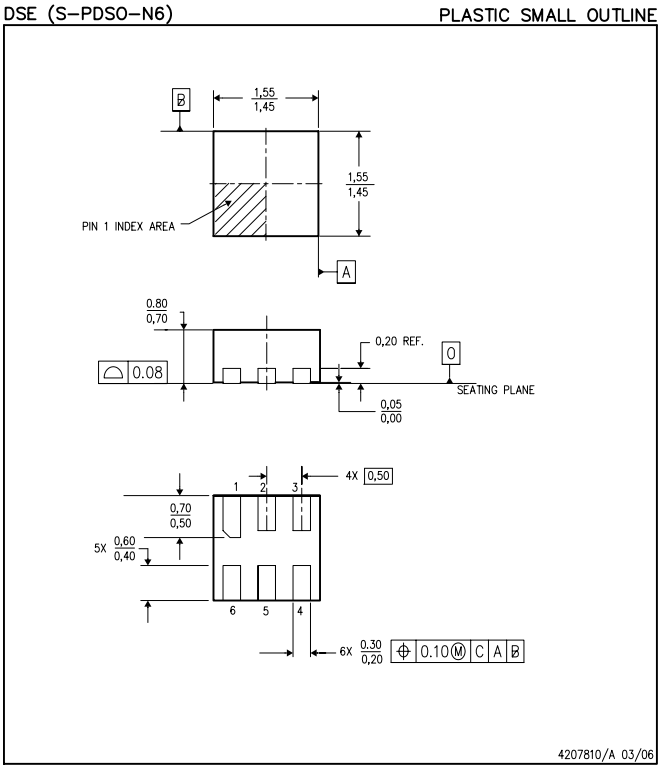
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

図 0. UNDEFINED

Copyright © 2012–2019, Texas Instruments Incorporated

MECHANICAL DATA

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE

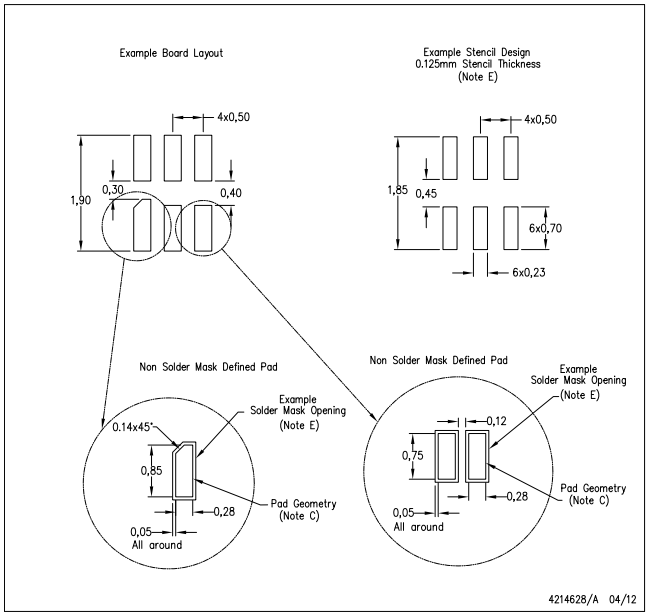


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

図 0. UNDEFINED

LAND PATTERN DATA

DSE (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.

図 0. UNDEFINED

Copyright © 2012–2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3700DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PXVQ
TPS3700DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ
TPS3700DDCR2	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PB4Q
TPS3700DDCR2.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PB4Q
TPS3700DDCR2G4	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PB4Q
TPS3700DDCR2G4.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PB4Q
TPS3700DDCRG4	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ
TPS3700DDCRG4.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ
TPS3700DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PXVQ
TPS3700DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ
TPS3700DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7I, BE)
TPS3700DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7I, BE)
TPS3700DSET	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7I, BE)
TPS3700DSET.A	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7I, BE)
TPS3700DSETG4	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7I
TPS3700DSETG4.A	Active	Production	WSON (DSE) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3700 :

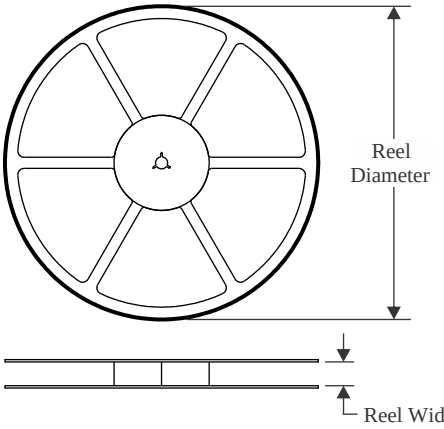
- Automotive : TPS3700-Q1

NOTE: Qualified Version Definitions:

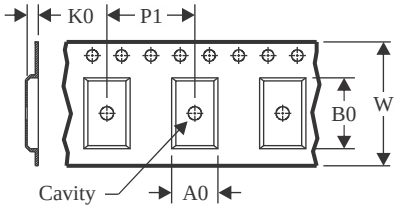
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

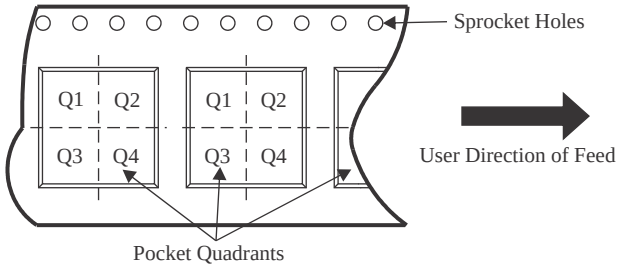


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

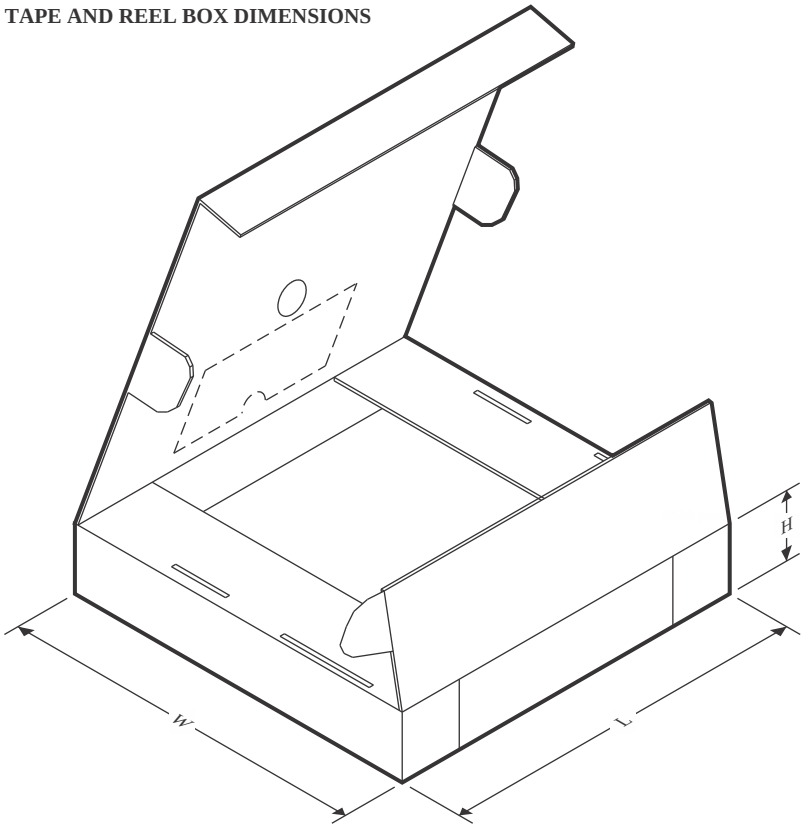
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3700DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DDCR2	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
TPS3700DDCR2G4	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
TPS3700DDCRG4	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DDCT	SOT-23-THIN	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3700DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3700DSETG4	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3700DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS3700DDCR2	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3700DDCR2G4	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3700DDCRG4	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3700DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0
TPS3700DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TPS3700DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3700DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS3700DSETG4	WSON	DSE	6	250	205.0	200.0	33.0

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月