TPS3701 過電圧および低電圧監視用の基準電圧を内蔵した高電圧 (36V) ウィンドウ電圧検出器

1 特長

- 広い電源電圧範囲: 1.8V～36V
- スレッショルドを変更可能：最小 400mV
- 過電圧および低電圧検出用のオープン・ドレイン出力
- 低い静止電流: 7μA (標準値)
- スレッショルドの高い精度
  - 温度範囲全体で 0.75%
  - 0.25% (標準値)
- 内部ヒステリシス: 5.5mV (標準値)
- 温度範囲: -40°C～+125°C
- パッケージ:
  - SOT-6

2 アプリケーション

- 産業用制御システム
- 組み込みコンピューティング・モジュール
- DSP、マイクロコントローラ、マイクロプロセッサ
- ノート PC およびデスクトップ PC
- 携帯用およびバッテリ駆動の製品
- FPGA および ASIC システム

3 概要

TPS3701 は広い電源電圧に対応するウィンドウ電圧検出器で、1.8V～36V の範囲で動作します。このデバイスには高精度コンパレータが 2 つ、400mV の内部基準電圧、および過電圧と低電圧検出用の 25V 定格のオープン・ドレイン出力が 2 つ (OUTA と OUTB) 内蔵されています。TPS3701 はウィンドウ電圧検出器としても、2 つの独立した電圧モニタとしても使用でき、監視対象の電圧は外付け抵抗により設定できます。

OUTAは、INAピンの電圧が負のスレッショルドを下回るとLOWに駆動され、正のスレッショルドを上回るとHIGHになります。OUTBは、INBピンの電圧が正のスレッショルドを上回るとLOWに駆動され、負のスレッショルドを下回るとHIGHになります。TPS3701のコンパレータは両方とも、ノイズ除去のためのヒステリシスが組み込まれているため、誤ったトリガが発生せず、安定した出力動作が確保されます。

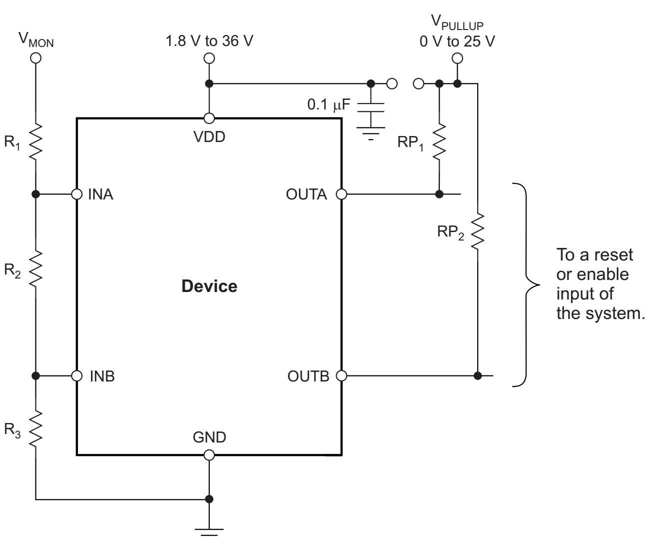
TPS3701はSOT-6パッケージで供給され、-40℃～125℃の接合部温度範囲で動作が規定されています。

製品情報(1)

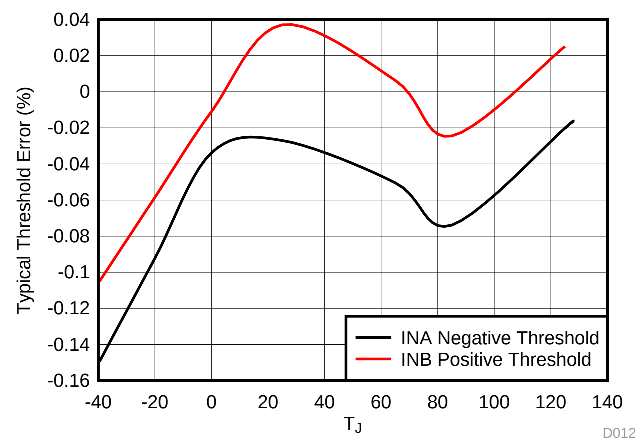
型番	パッケージ	本体サイズ(公称)
TPS3701	SOT (6)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



標準的な誤差と接合部温度との関係



English Data Sheet: SBVS240

目次

4 改訂履歴

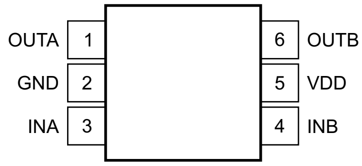
Revision B (June 2018) から Revision C に変更	Page
• テキスト「スーパーバイザ」を「電圧検出器」に 変更	1
• Changed "supervisor" to "voltage detector"	12

Revision A (November 2017) から Revision B に変更	Page
• データシート全体を通してテキスト「ウィンドウ・コンパレータ」を「ウィンドウ・スーパーバイザ」に 変更	1

2014年11月発行のものから更新	Page
• Changed input pin voltage maximum from: 1.7 V to: 6.5 V	4
• Added a tablenote for the input pin voltage maximum	4
• Changed Figure 19	12

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
INA	3	I	Comparator A input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage $V_{IT-(INA)}$, OUTA is driven low.
INB	4	I	Comparator B input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage $V_{IT+(INB)}$, OUTB is driven low.
OUTA	1	O	INA comparator open-drain output. OUTA is driven low when the voltage at this comparator is less than $V_{IT-(INA)}$. The output goes high when the sense voltage rises above $V_{IT+(INA)}$.
OUTB	6	O	INB comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{IT+(INB)}$. The output goes high when the sense voltage falls below $V_{IT-(INB)}$.
VDD	5	I	Supply voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.[1]

		MIN	MAX	UNIT
Voltage[2]	V_{DD}	–0.3	+40	V
	V_{OUTA}, V_{OUTB}	–0.3	+28	
	V_{INA}, V_{INB}	–0.3	+7	
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	–40	+125	°C
	Storage temperature, T_{stg}	–65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.8		36	V
V_{INA}, V_{INB}	Input pin voltage	0		6.5[1]	V
V_{OUTA}, V_{OUTB}	Output pin voltage	0		25	V
I_{OUTA}, I_{OUTB}	Output pin current	0		10	mA
T_J	Junction temperature	–40	+25	+125	°C

(1) Operating V_{INA} or V_{INB} at 2.4 V or higher and at 125°C continuously for 10 years or more would cause a degradation of accuracy spec to 1.5% maximum

6.4 Thermal Information

THERMAL METRIC[1]		TPS3701	UNIT
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V ≤ V_{DD} < 36 V, and pull-up resistors $RP_{1,2}$ = 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		36	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} ≤ 0.2 V			0.8	V
$V_{IT–(INA)}$	INA pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{IT+(INA)}$	INA pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	400	405.5	413	mV
$V_{HYS(INA)}$	INA pin hysteresis voltage (HYS = $V_{IT+(INA)}$ – $V_{IT–(INA)}$)		2	5.5	12	mV
$V_{IT–(INB)}$	INB pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	387	394.5	400	mV
$V_{IT+(INB)}$	INB pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{HYS(INB)}$	INB pin hysteresis voltage (HYS = $V_{IT+(INB)}$ – $V_{IT–(INB)}$)		2	5.2	12	mV
V_{OL}	Low-level output voltage	V_{DD} = 1.8 V, I_{OUT} = 3 mA		130	250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA		150	250	mV
I_{IN}	Input current (at INA, INB pins)	V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 6.5 V	–25	+1	+25	nA
		V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 0.1 V	–15	+1	+15	nA
$I_{D(leak)}$	Open-drain output leakage current	V_{DD} = 1.8 V and 36 V, V_{OUT} = 25 V		10	300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V – 36 V		8	11	µA
UVLO	Undervoltage lockout(2)	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. If less than $V_{(POR)}$, the output is undetermined.
(2) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined if less than $V_{(POR)}$.

6.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		9.9		µs
$t_{pd(LH)}$	Low-to-high propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		28.1		µs
$t_{d(start)}$(2)	Startup delay	V_{DD} = 5 V		155		µs
t_r	Output rise time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.1 to 0.9) × V_{DD}		2.7		µs
t_f	Output fall time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.9 to 0.1) × V_{DD}		0.12		µs

(1) High-to-low and low-to-high refers to the transition at the input pins (INA and INB).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs (typical) before the output state reflects the input condition.

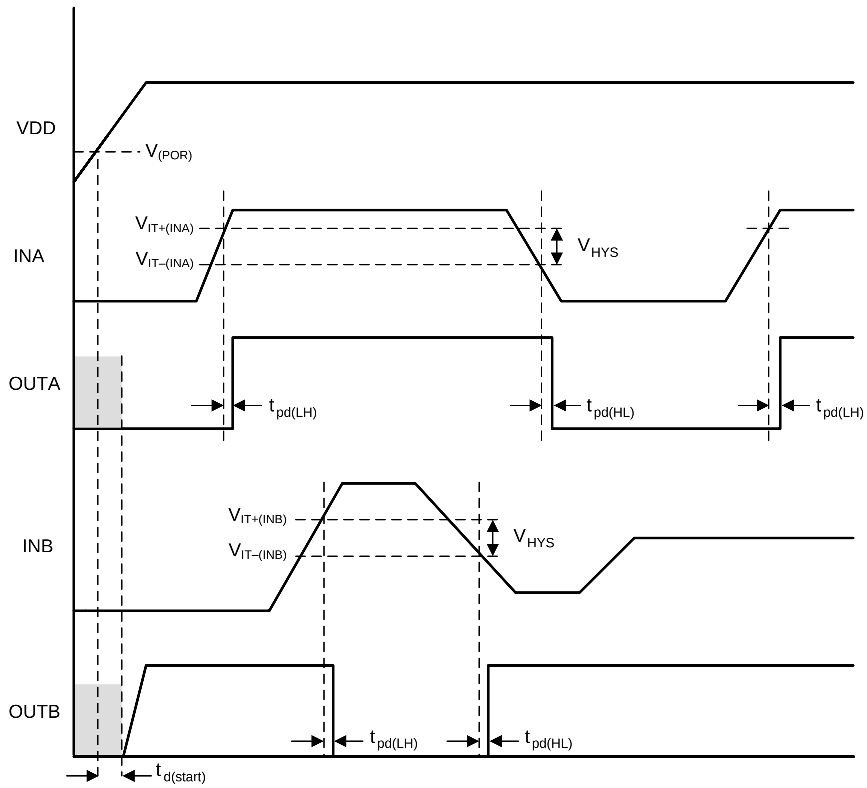


Figure 1. Timing Diagram

6.7 Typical Characteristics

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

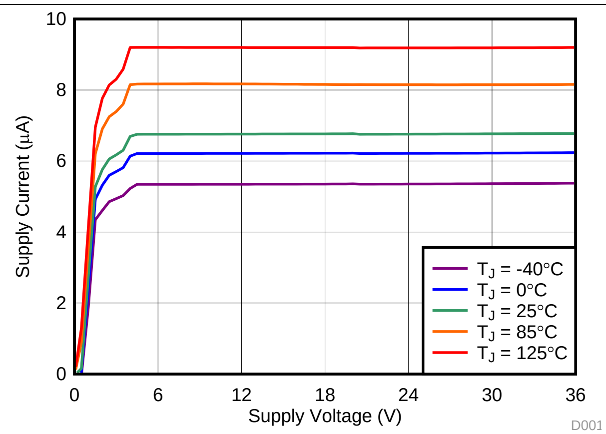
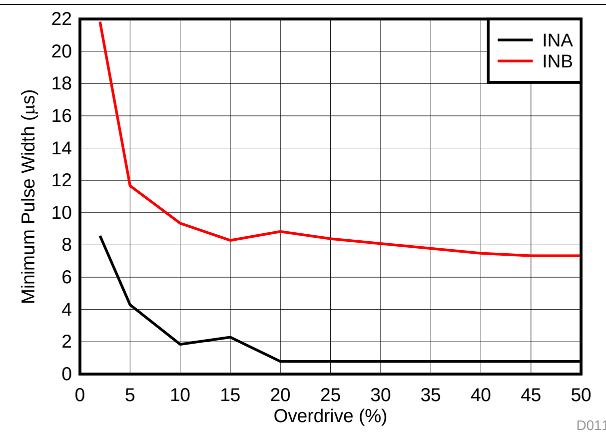


Figure 2. Supply Current vs Supply Voltage



V_{DD} = 24 V

Figure 3. Minimum Pulse Duration vs Threshold Overdrive Voltage(1) (1)

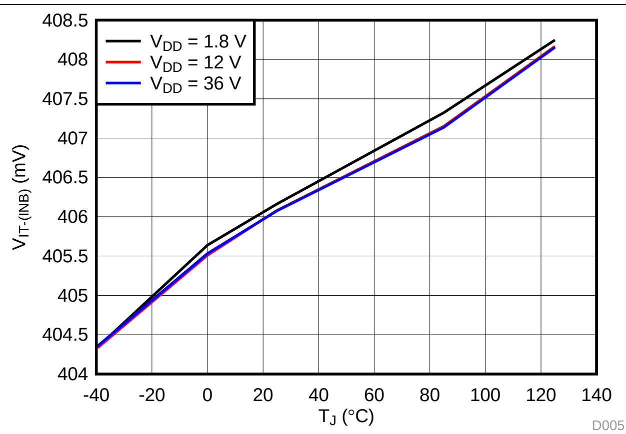


Figure 4. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) vs Temperature

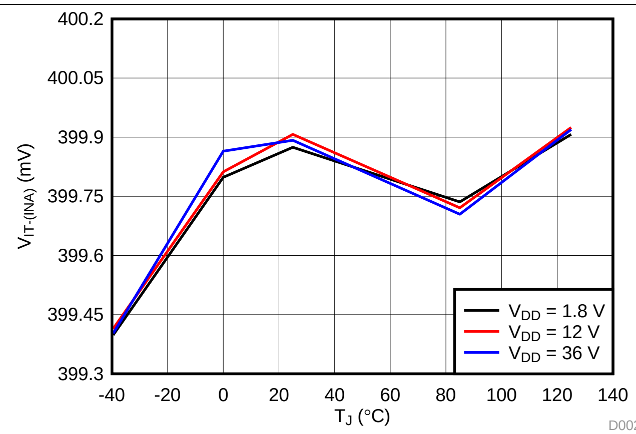


Figure 5. INA Negative Input Threshold Voltage ($V_{IT–(INA)}$) vs Temperature

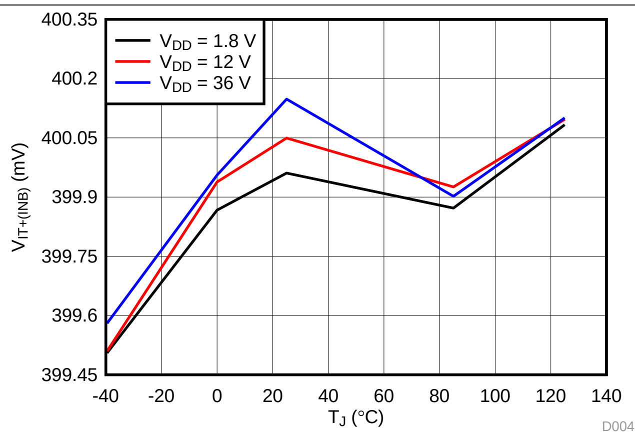


Figure 6. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) vs Temperature

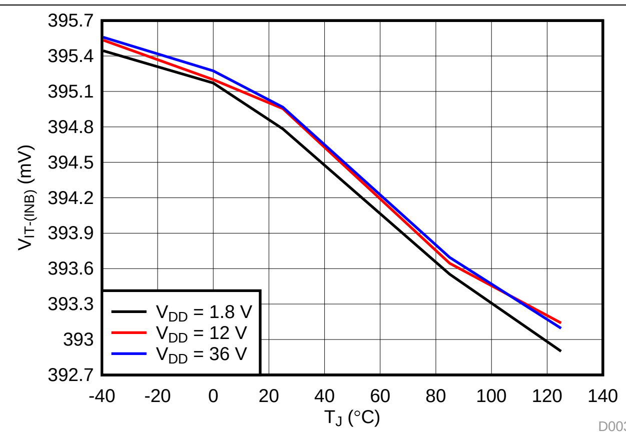


Figure 7. INB Negative Input Threshold Voltage ($V_{IT–(INB)}$) vs Temperature

(1) Minimum pulse duration required to trigger output high-to-low transition. INA = negative spike below $V_{IT–}$ and INB = positive spike above V_{IT+}.

Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

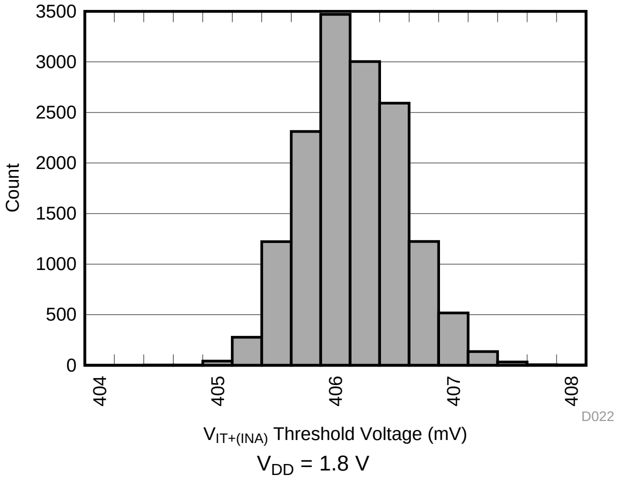


Figure 8. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) Distribution

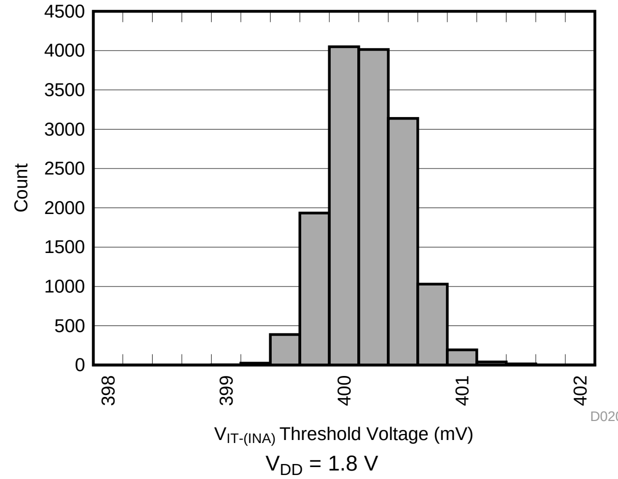


Figure 9. INA Negative Input Threshold Voltage ($V_{IT–(INA)}$) Distribution

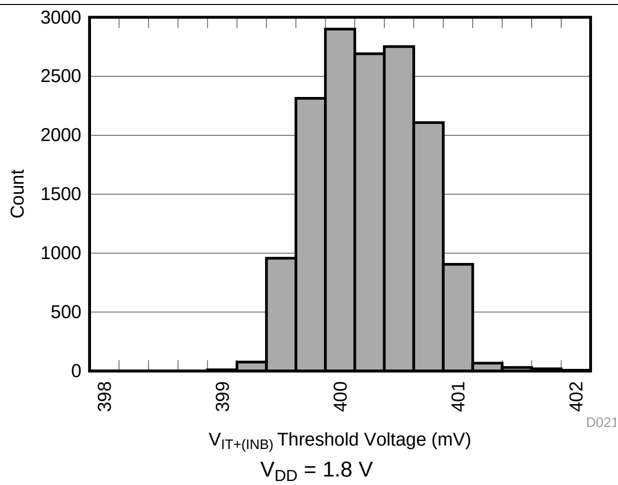


Figure 10. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) Distribution

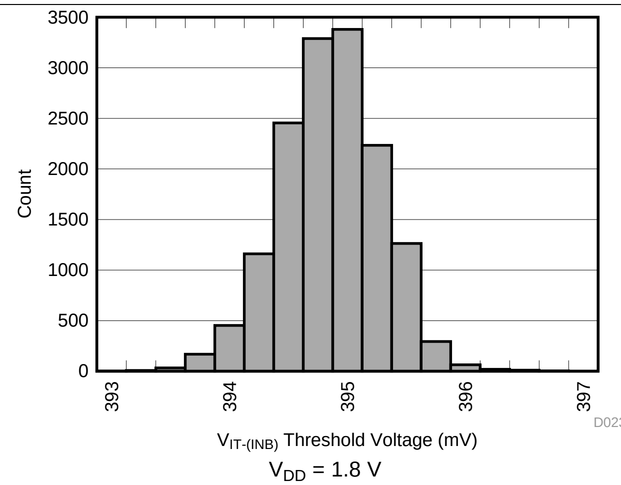


Figure 11. INB Negative Input Threshold Voltage ($V_{IT–(INB)}$) Distribution

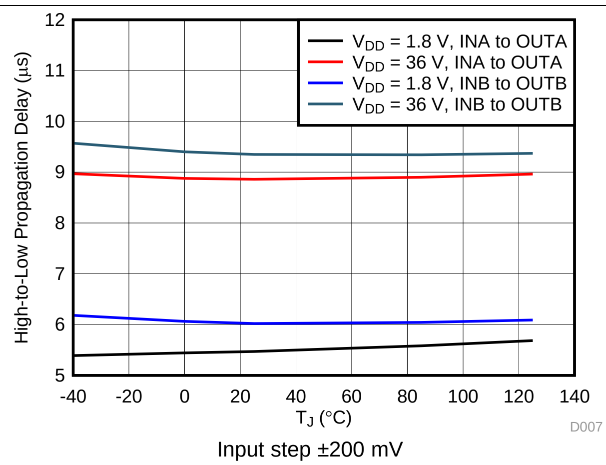


Figure 12. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

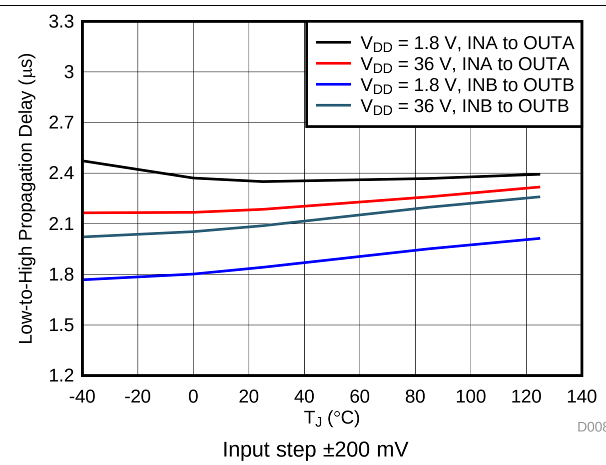
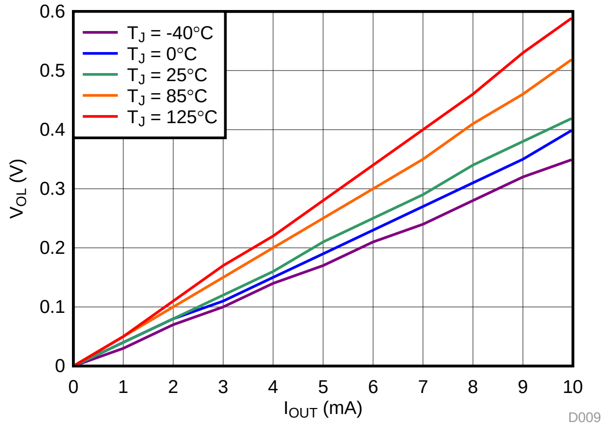


Figure 13. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)

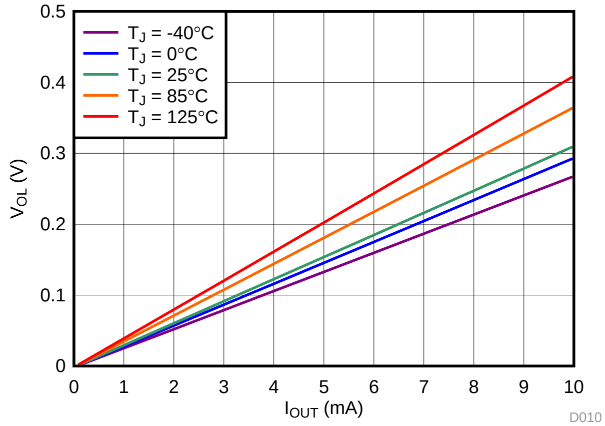
Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.



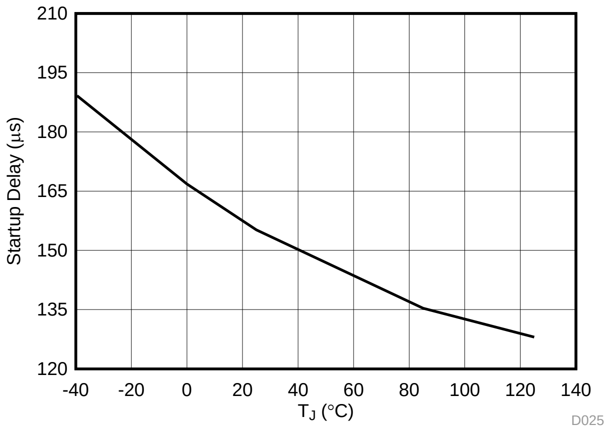
V_{DD} = 1.8 V

Figure 14. Output Voltage Low vs Output Sink Current



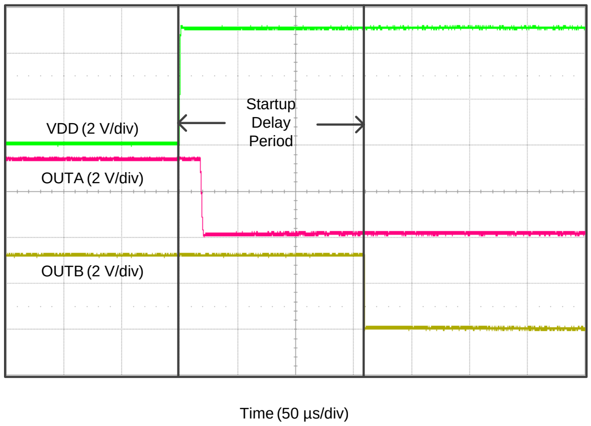
V_{DD} = 12 V

Figure 15. Output Voltage Low vs Output Sink Current



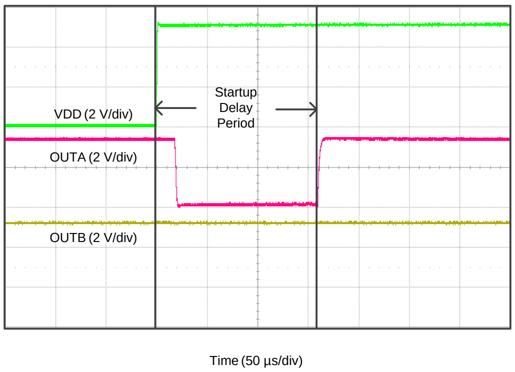
V_{DD} = 5 V

Figure 16. Start-Up Delay vs Temperature



V_{DD} = 5 V, V_{INA} = 390 mV, V_{INB} = 410 mV, $V_{PULL-UP}$ = 3.3 V

Figure 17. Start-Up Delay



V_{DD} = 5 V, V_{INA} = 410 mV, V_{INB} = 390 mV, $V_{PULL-UP}$ = 3.3 V

Figure 18. Start-Up Delay

7 Detailed Description

7.1 Overview

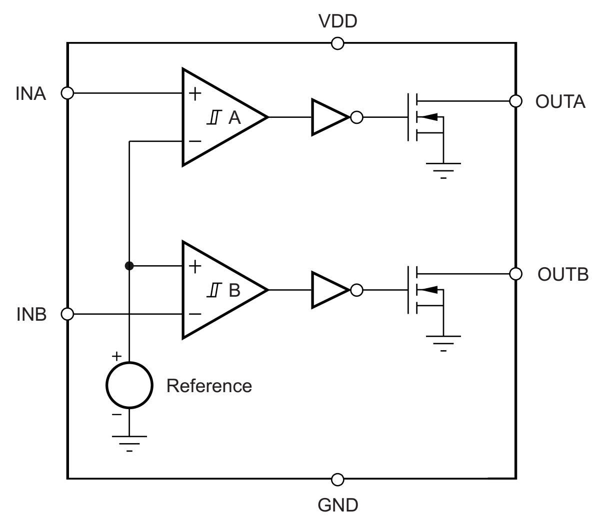
The TPS3701 combines two comparators (referred to as A and B) and a precision reference for over- and undervoltage detection. The TPS3701 features a wide supply voltage range (1.8 V to 36 V) and high-accuracy window threshold voltages of 400 mV (0.75% over temperature) with built-in hysteresis. The outputs are rated to 25 V and can sink up to 10 mA.

Set each input pin (INA, INB) to monitor any voltage above 0.4 V by using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. To form a window voltage detector, use the two input pins and three resistors (see the *Window Voltage Detector Considerations* section). In this configuration, the TPS3701 is designed to assert the output signals when the monitored voltage is within the window band. Each input can also be used independently. The relationship between the inputs and the outputs is shown in Table 1. Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

Table 1. Truth Table

CONDITION	OUTPUT	STATUS
INA > $V_{IT+(INA)}$	OUTA high	Output A high impedance
INA < $V_{IT-(INA)}$	OUTA low	Output A asserted
INB > $V_{IT+(INB)}$	OUTB low	Output B asserted
INB < $V_{IT-(INB)}$	OUTB high	Output B high impedance

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inputs (INA, INB)

The TPS3701 combines two comparators with a precision reference voltage. Each comparator has one external input; the other input is connected to the internal reference. The rising threshold on INB and the falling threshold on INA are designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy when used as a window voltage detector. Both comparators also have built-in hysteresis that proves immunity to noise and ensures stable operation.

The INA and INB inputs swings from ground to 1.7 V (7.0 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications in order to reduce sensitivity to transient voltage changes on the monitored signal.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA voltage drops below $V_{IT-(INA)}$. When the voltage exceeds $V_{IT+(INA)}$, OUTA goes to a high-impedance state; see Figure 1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB exceeds $V_{IT+(INB)}$. When the voltage drops below $V_{IT-(INB)}$ OUTB goes to a high-impedance state; see Figure 1. Together, these two comparators form a window voltage detector function as described in the *Window Voltage Detector Considerations* section.

7.3.2 Outputs (OUTA, OUTB)

In a typical TPS3701 application, the outputs are connected to a reset or enable input of the processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the outputs are connected to the enable input of a voltage regulator [such as a DC-DC converter or low-dropout regulator (LDO)].

The TPS3701 provides two open-drain outputs (OUTA and OUTB); use pull-up resistors to hold these lines high when the output goes to a high-impedance state. Connect pull-up resistors to the proper voltage rails to enable the outputs to be connected to other devices at correct interface voltage levels. The TPS3701 outputs can be pulled up to 25 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the *Electrical Characteristics* table. Use wired-OR logic to merge OUTA and OUTB into one logic signal.

Table 1 and the *Inputs (INA, INB)* section describe how the outputs are asserted or high impedance. See Figure 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than 1.8 V for at least 155 µs, the OUTA and OUTB signals correspond to the voltage on INA and INB as listed in Table 1.

7.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD}$ < UVLO)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on-reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA and INB.

7.4.3 Power-On-Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3701 is used as a precision dual-voltage detector in several different configurations. The monitored voltage (V_{MON}), VDD voltage, and output pull-up voltage can be independent voltages or connected in any configuration. The following sections show the connection configurations and the voltage limitations for each configuration.

8.1.1 Window Voltage Detector Considerations

The inverting and noninverting configuration of the comparators forms a window voltage detector circuit using a resistor divider network, as shown in Figure 19 and Figure 20. The input pins can monitor any system voltage above 400 mV with the use of a resistor divider network. INA and INB monitor for undervoltage and overvoltage conditions, respectively.

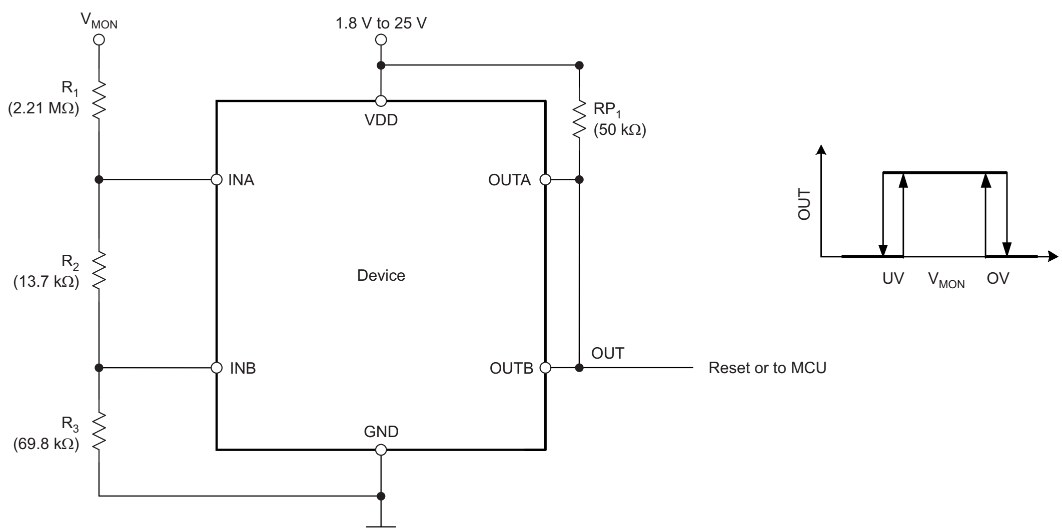


Figure 19. Window Voltage Detector Block Diagram

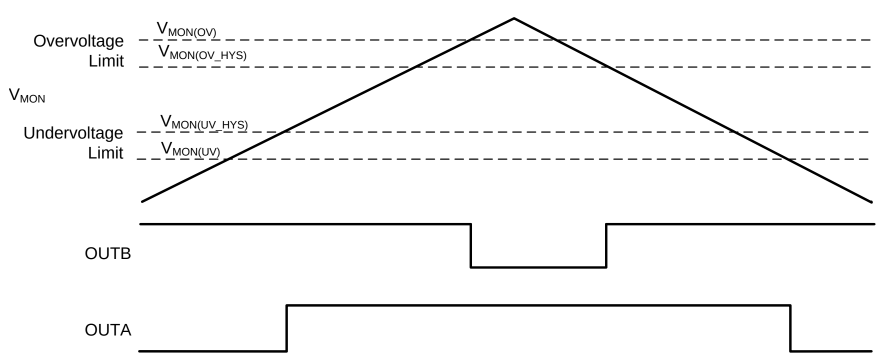


Figure 20. Window Voltage Detector Timing Diagram

Application Information (continued)

The TPS3701 flags the overvoltage or undervoltage condition with the greatest accuracy. The highest accuracy threshold voltages are $V_{IT-(INA)}$ and $V_{IT+(INB)}$, and correspond with the falling undervoltage flag, and the rising overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage is within the valid window (both OUTA and OUTB are in a high-impedance state), and correspond to the $V_{MON(UV)}$ and $V_{MON(OV)}$ trigger voltages, respectively. If the monitored voltage is outside of the valid window (V_{MON} is less than the undervoltage limit, $V_{MON(UV)}$, or greater than overvoltage limit, $V_{MON(OV)}$), then the input threshold voltages to re-enter the valid window are $V_{IT+(INA)}$ or $V_{IT-(INB)}$, and correspond with the $V_{MON(UV\_HYS)}$ and $V_{MON(OV\_HYS)}$ monitored voltages, respectively.

The resistor divider values and target threshold voltage can be calculated by using Equation 1 through Equation 4:

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Choose an R_{TOTAL} value so that the current through the divider is approximately 100 times higher than the input current at the INA and INB pins. Resistors with high values minimize current consumption; however, the input bias current degrades accuracy if the current through the resistors is too low. See application report *SLVA450, Optimizing Resistor Dividers at a Comparator Input* (SLVA450), for details on sizing input resistors.

R_3 is determined by Equation 2:

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)}$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected. (2)

R_2 is determined by either Equation 3 or Equation 4:

$$R_2 = \left[\frac{R_{TOTAL}}{V_{MON(UV\_HYS)}} \bullet V_{IT+(INA)} \right] - R_3$$

where

- $V_{MON(UV\_HYS)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises. (3)

$$R_2 = \left[\frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA)} \right] - R_3$$

where

- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected. (4)

8.1.2 Input and Output Configurations

Figure 21 to Figure 24 show examples of the various input and output configurations.

Application Information (continued)

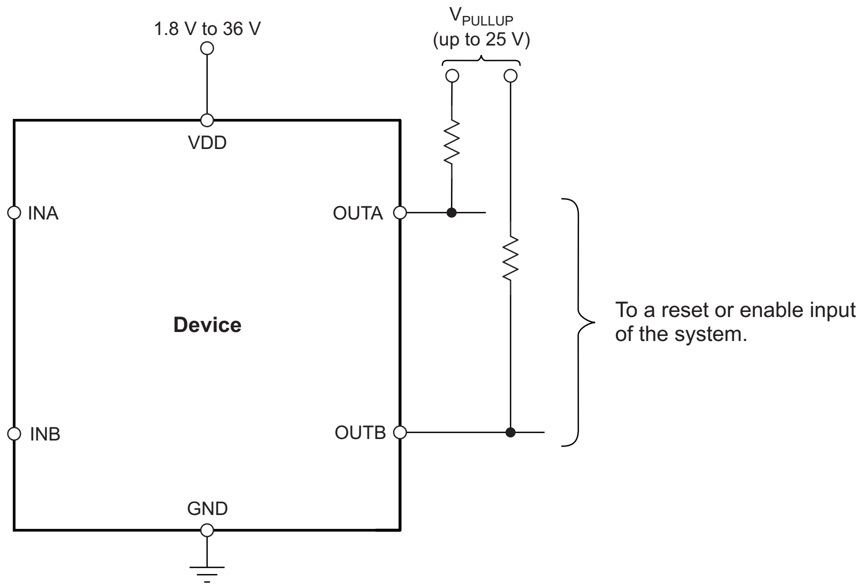


Figure 21. Interfacing to Voltages Other than V_{DD}

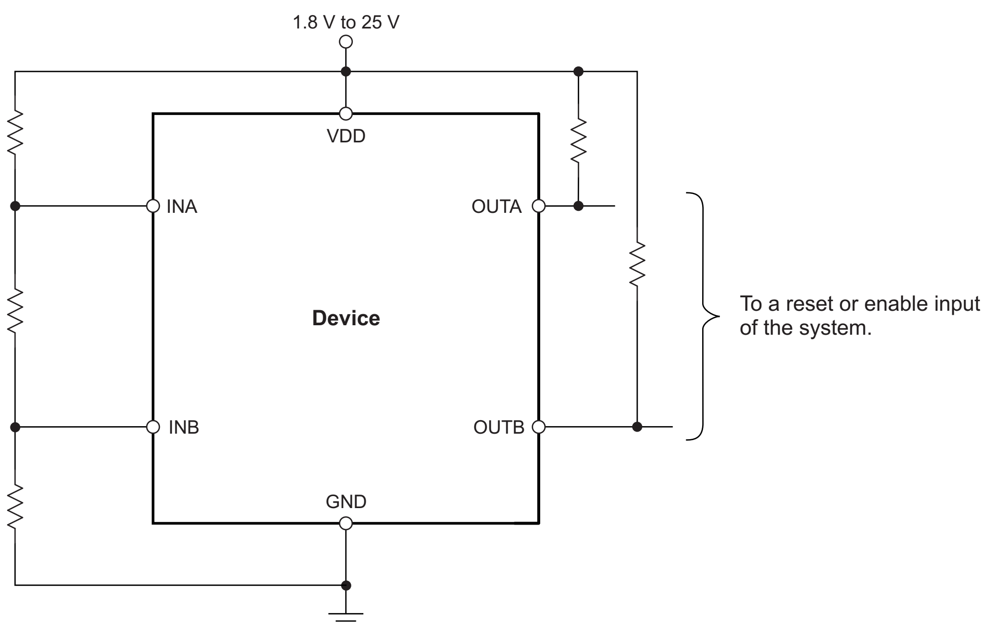
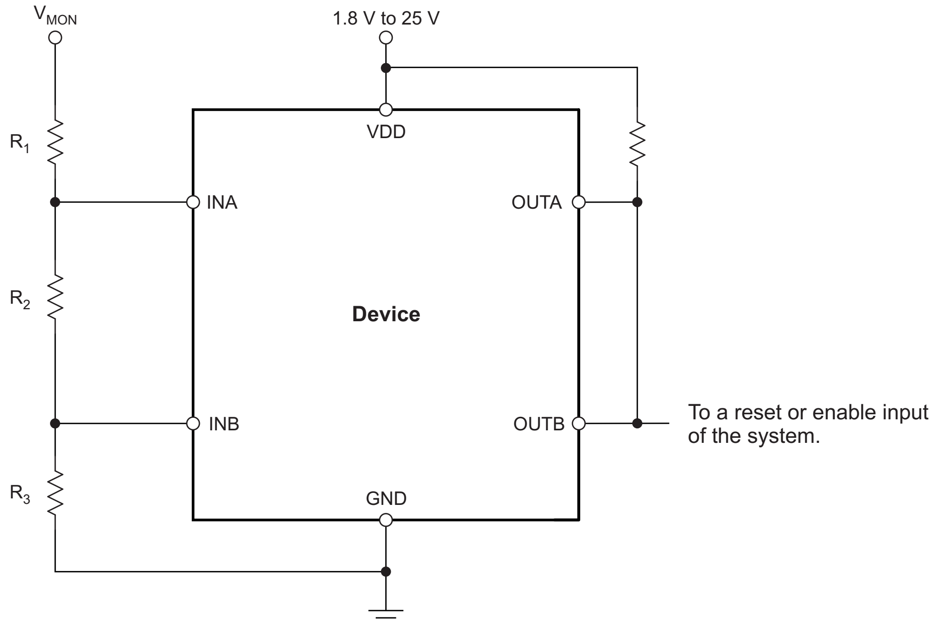


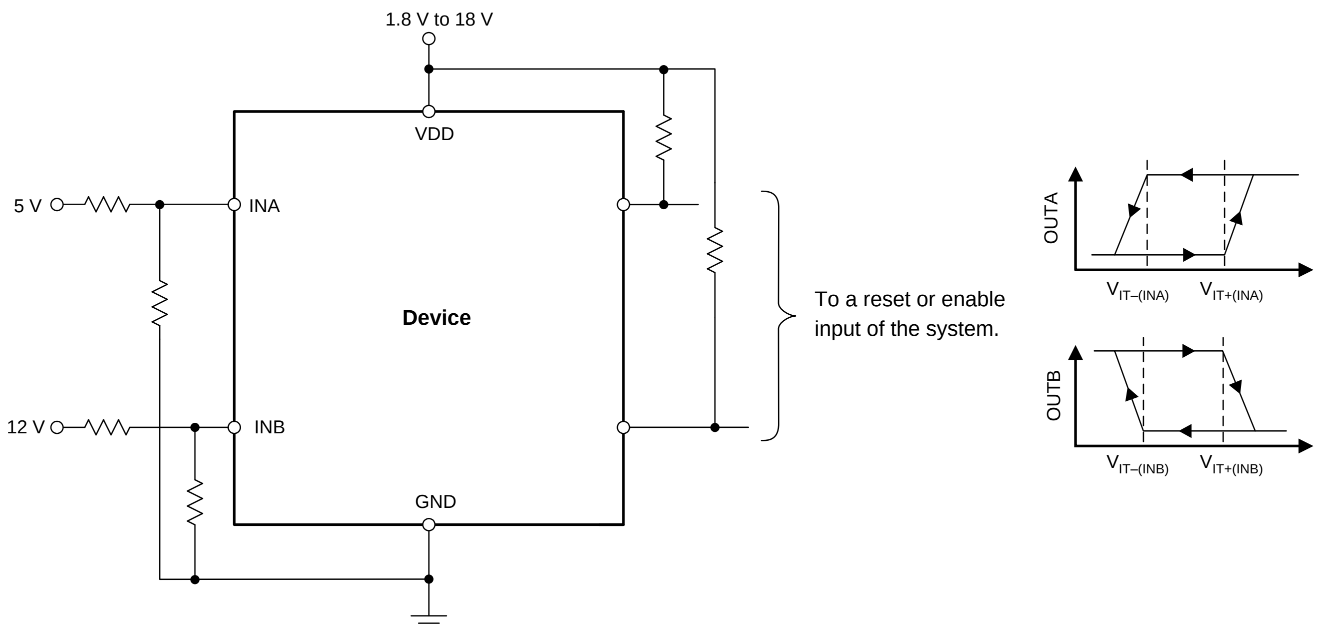
Figure 22. Monitoring the Same Voltage as V_{DD}

Application Information (continued)



NOTE: The inputs can monitor a voltage higher than V_{DD} (max) with the use of an external resistor divider network.

Figure 23. Monitoring a Voltage Other than V_{DD}



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

Figure 24. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

8.1.3 Immunity to Input Pin Voltage Transients

The TPS3701 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and amplitude; see Figure 3, *Minimum Pulse Duration vs Threshold Overdrive Voltage*.

8.2 Typical Application

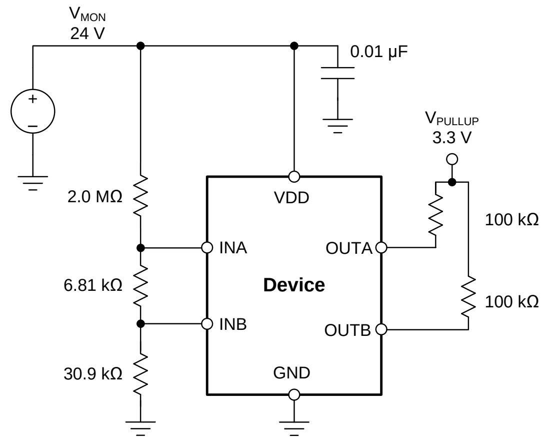


Figure 25. 24-V, 10% Window Voltage Detector

8.2.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, rising ($V_{MON(OV)}$) and falling ($V_{MON(UV)}$) threshold ±10% nominal (26.4 V and 21.6 V, respectively)	$V_{MON(OV)}$ = 26.4 V ±2.7%, $V_{MON(UV)}$ = 21.6 V ±2.7%
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 µA	24 µA

8.2.2 Detailed Design Procedure

1. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification by using Equation 1. For this example, the current flow through the resistor network was chosen to be 13 µA; a lower current can be selected. However, take care to avoid leakage currents that are artifacts of the manufacturing process. Leakage currents significantly impact the accuracy if they are greater than 1% of the resistor network current.

$$R_{TOTAL} = \frac{V_{MON(OV)}}{I} = \frac{26.4\ V}{13\ \mu A} = 2.03\ M\Omega$$

   where

   - $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected as V_{MON} rises.
   - I is the current flowing through the resistor network. (5)

2. After R_{TOTAL} is determined, R_3 can be calculated using Equation 6. Select the nearest 1% resistor value for R_3. In this case, 30.9 kΩ is the closest value.

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} = \frac{2.03\ M\Omega}{26.4\ V} \bullet 0.4\ V = 30.7\ k\Omega \quad (6)$$

3. Use Equation 7 to calculate R2. Select the nearest 1% resistor value for R_2. In this case, 6.81 kΩ is the closest value.

$$R_2 = \frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA+)} - R_3 = \frac{2.03\ M\Omega}{21.6\ V} \bullet 0.4\ V - 30.9\ k\Omega = 6.69\ k\Omega \quad (7)$$

4. Use Equation 8 to calculate R1. Select the nearest 1% resistor value for R_1. In this case, 2 MΩ is the closest value.

$$R_1 = R_{TOTAL} - R_2 - R_3 = 2.03\ M\Omega - 6.81\ k\Omega - 30.9\ k\Omega = 1.99\ M\Omega \quad (8)$$

5. The worst-case tolerance can be calculated by referring to Equation 13 in application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450). An example of the rising threshold error, $V_{MON(OV)}$, is given in Equation 9:

$$\%\ ACC = \%\ TOL(V_{IT+(INB)}) + 2 \cdot \left(1 - \frac{V_{IT+(INB)}}{V_{MON(OV)}}\right) \cdot \%\ TOL_R = 0.75\ \% + 2 \cdot \left(1 - \frac{0.4}{26.4}\right) \cdot 1\% = 2.72\ \%$$

where

- % TOL($V_{IT+(INB)}$) is the tolerance of the INB positive threshold.
- % ACC is the total tolerance of the $V_{MON(OV)}$ voltage.
- % TOL_R is the tolerance of the resistors selected. (9)

6. When the outputs switch to the high-Z state, the rise time of the OUTA or OUTB node depends on the pull-up resistance and the capacitance on the node. Choose pull-up resistors that satisfy the downstream timing requirements; 100-kΩ resistors are a good choice for low-capacitive loads.

8.2.3 Application Curve

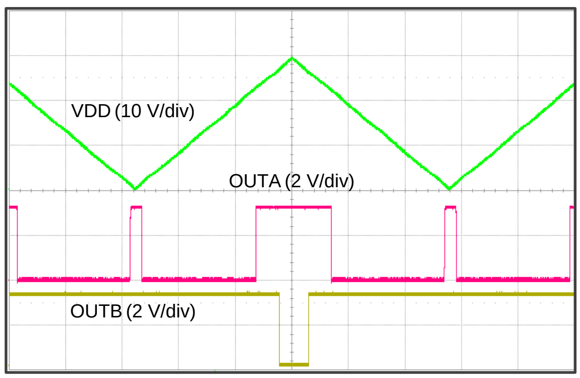


Figure 26. 24-V Window Monitor Output Response

9 Power Supply Recommendations

The TPS3701 has a 40-V absolute maximum rating on the VDD pin, with a recommended operating condition of 36 V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100-Ω resistor and 0.01-µF capacitor is required in these cases, as shown in Figure 27.

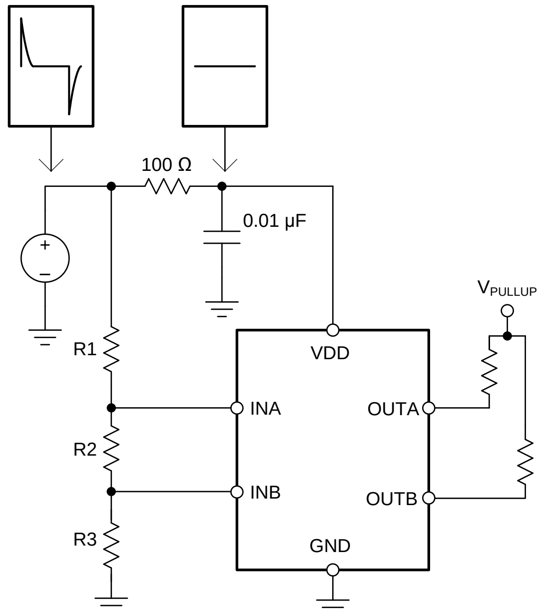


Figure 27. Using an RC Filter to Remove High-Frequency Disturbances on VDD

10 Layout

10.1 Layout Guidelines

- Place R_1, R_2, and R_3 close to the device to minimize noise coupling into the INA and INB nodes.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, may form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If this is unavoidable, see Figure 27 for an example of filtering VDD.

10.2 Layout Example

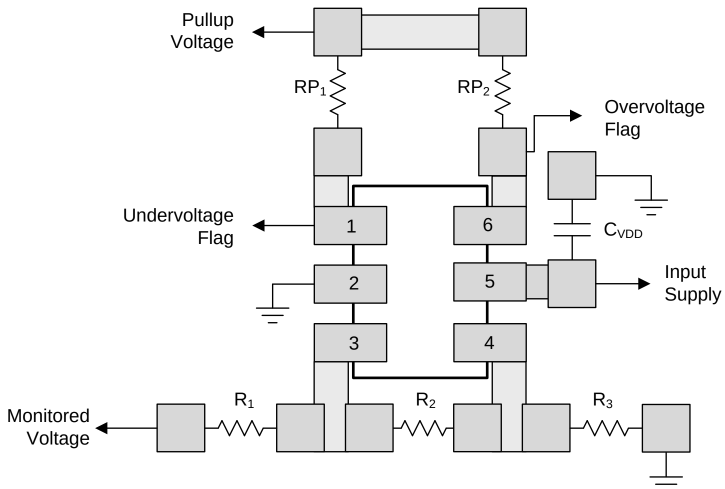


Figure 28. Recommended Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下のアプリケーション・レポートとユーザー・ガイドを参照してください(TI Webサイトからダウンロードできます)。

- アプリケーション・レポート『負のレールの過電圧と低電圧の検出器としてTPS3700を使用』(SLVA600)
- アプリケーション・レポート『コンパレータ入力における分圧抵抗の最適化』(SLVA450)
- ユーザー・ガイド『TPS3700EVM-114評価基板』(SLVU683)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

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11.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3701DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZABO	Samples
TPS3701DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		ZABO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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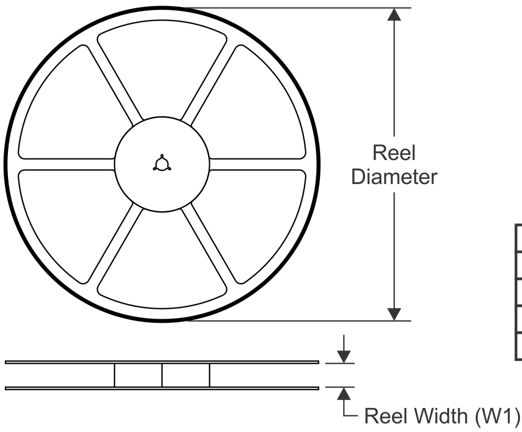
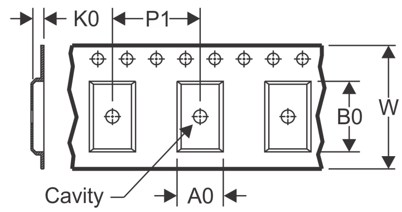
TAPE AND REEL INFORMATION

REEL DIMENSIONS

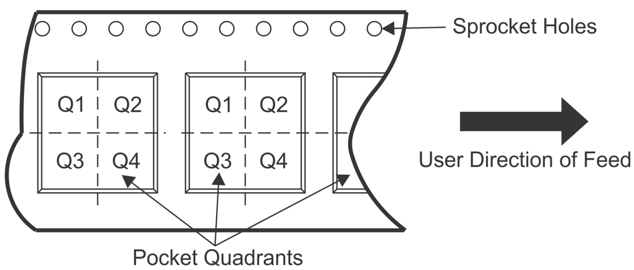


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

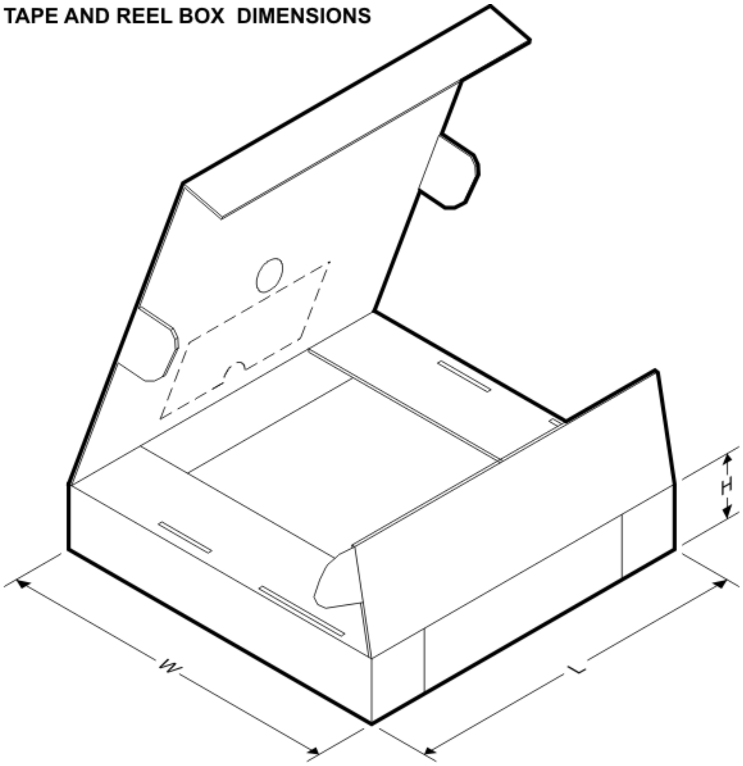
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3701DDCR	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3701DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



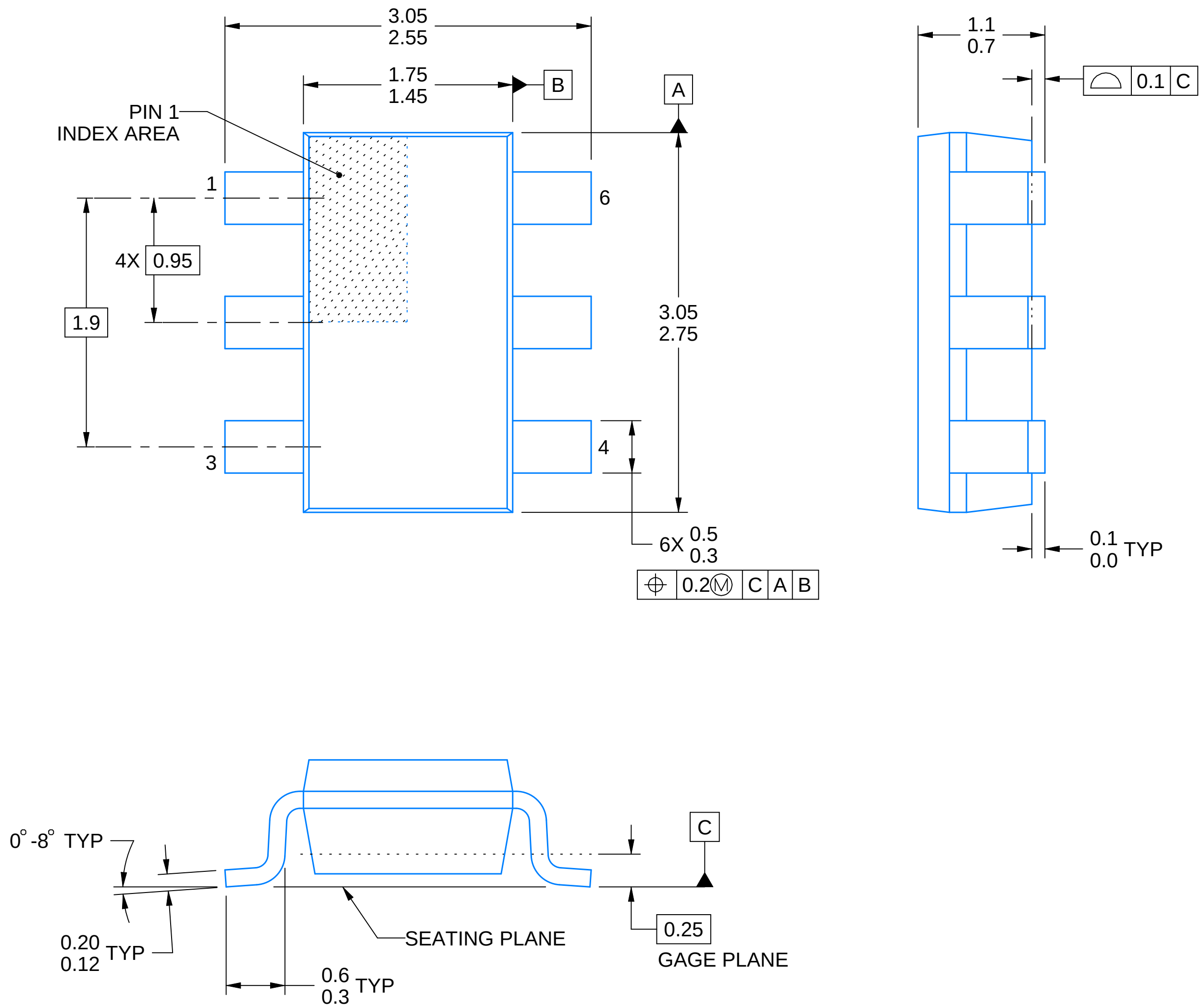
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3701DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3701DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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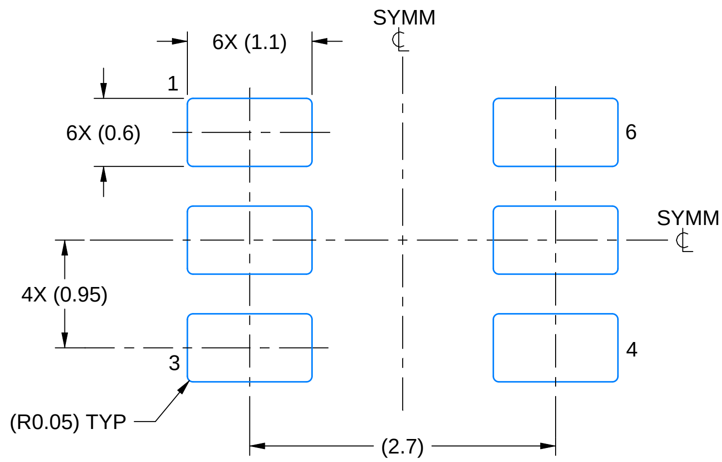
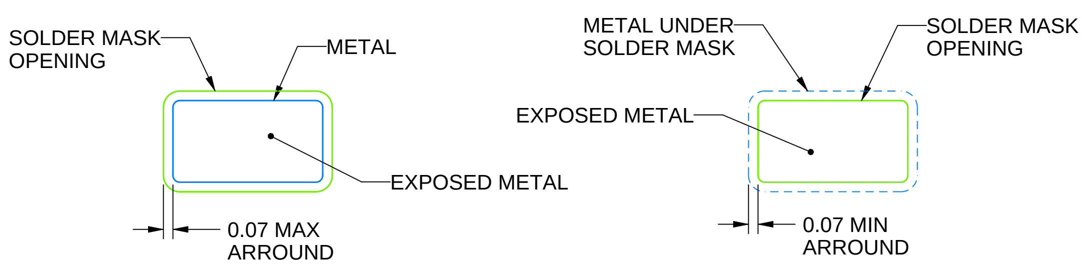
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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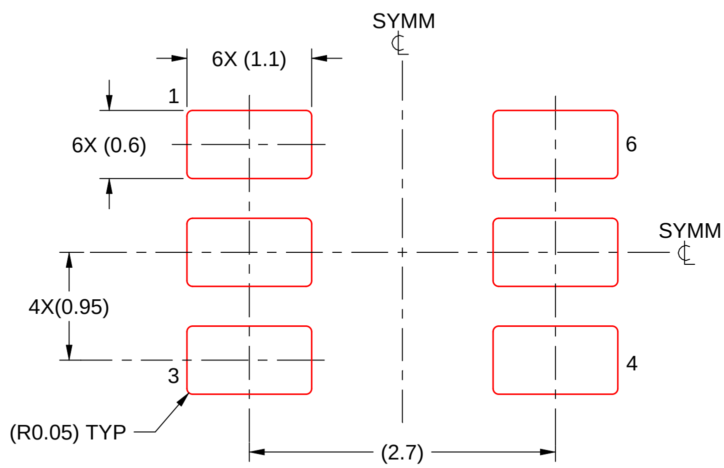
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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