TPS3705-30, TPS3705-33, TPS3705-50, TPS3707-30, TPS3707-50
JAJSQ83F – NOVEMBER 1998 – REVISED OCTOBER 2020

TPS370x-xx パワーフェイル付きプロセッサ・スーパーバイザ回路

1 特長

- 200ms の固定遅延時間を持つパワーオン・リセット・ジェネレータ (外付けコンデンサ不要)
- 高精度電源電圧モニタ:2.5V、3V、3.3V、5V
- MAX705～MAX708 シリーズとピン互換
- ウォッチドッグ・タイマ内蔵 (TPS3705-xx のみ)
- パワーフェイルまたはバッテリ電圧低下警告用電圧監視
- 最大消費電流:50μA
- 8 ピン MSOP および 8 ピン SOIC パッケージ
- 温度範囲:-40℃～85℃ (TPS3705-33 の場合 -40℃～125℃)

2 アプリケーション

- DSP、マイクロコントローラ、マイクロプロセッサを用いた設計
- 産業用機器
- プログラマブル制御
- 車載用システム
- 携帯機器またはバッテリ駆動機器
- インテリジェント機器
- ワイヤレス通信システム
- ノート PC およびデスクトップ PC

3 概要

TPS370x-xx ファミリの電源電圧監視 IC は、主に DSP やプロセッサを使用したシステムにおける回路の初期化およびタイミング監視に最適です。

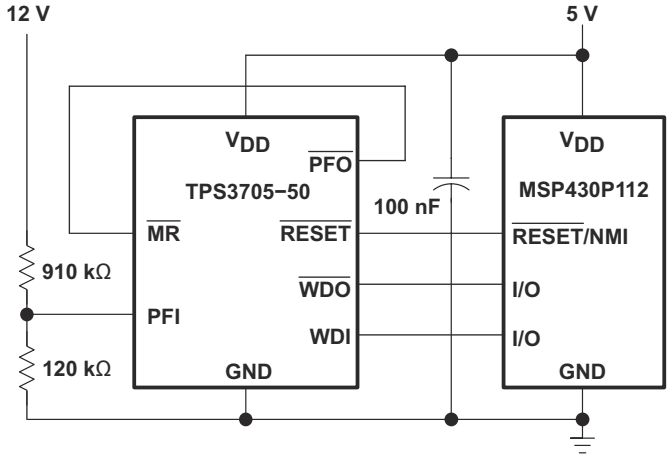
電源投入時には、電源電圧 V_{DD} が 1.1V を上回ると $\overline{RESET}$ ピンがアサートされます。その後、この電源電圧監視 IC が V_{DD} を監視し、V_{DD} がスレッショルド電圧 V_{IT+} を下回っている間は $\overline{RESET}$ ピンをアクティブに維持します。電源電圧がスレッショルド電圧 V_{IT-} を下回ると、出力は再びアクティブ (LOW) になります。外付け部品は不要です。このファミリのデバイスはすべて、内部分圧回路により検出スレッショルド電圧 V_{IT-} が固定値になっています。

この製品ファミリは、2.5V、3V、3.3V、5V の電源電圧用に設計されています。これらの回路は 8 ピンの MSOP パッケージまたは標準の SOIC パッケージで供給されます。TPS370x-xx デバイスは、-40℃～85℃の温度範囲で動作が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS3705-xx、TPS3707-xx	MSOP- PowerPAD ™ (8)	3.00mm × 3.00mm
	SOIC (8)	3.90mm × 4.90mm

(1) 利用可能なパッケージについては、データシートの末尾にある注文情報を参照してください。



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MSP430 の代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (July 2017) to Revision F (October 2020) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated Device Comparison Table by adding -40°C to 125°C for TPS3705-33D ... 3
- Updated Absolute Maximum Ratings table to include Operating Temperature of -40°C to 125°C for TPS3705-33D ... 5
- Added TPS3705-33 Electrical Table ... 8
- Added histograms ... 11

Changes from Revision D (May 2016) to Revision E (July 2017) — **Page**

- 「製品情報」表のパッケージ本体サイズを更新 ... 1

Changes from Revision C (December 2005) to Revision D (May 2016) — **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

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5 Device Comparison Table

T_A	THRESHOLD VOLTAGE	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
		SMALL OUTLINE (D)	POWER-PAD µ-SMALL OUTLINE (DGN)		
–40°C to 85°C	2.63 V	TPS3705−30D	TPS3705−30DGN	TIAAT	TPS3705-30Y
	4.55 V	TPS3705−50D	TPS3705−50DGN	TIAAV	TPS3705−50Y
	2.25 V	TPS3707−25D	TPS3707−25DGN	TIAAW	TPS3707−25Y
	2.63 V	TPS3707−30D	TPS3707−30DGN	TIAAX	TPS3707−30Y
	2.93 V	TPS3707−33D	TPS3707−33DGN	TIAAY	TPS3707−33Y
	4.55 V	TPS3707−50D	TPS3707−50DGN	TIAAZ	TPS3707−50Y
–40°C to 125°C	2.93 V	TPS3705−33D	TPS3705−33DGN	TIAAU	TPS3705−33Y

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6 Pin Configuration and Functions

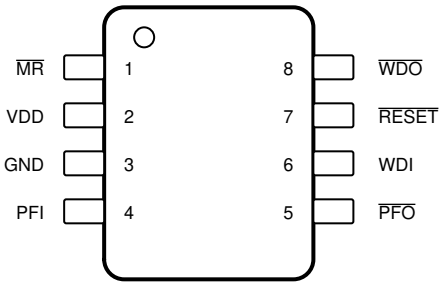


図 6-1. TPS3705-xx D Package 8-Pin SOIC Top View

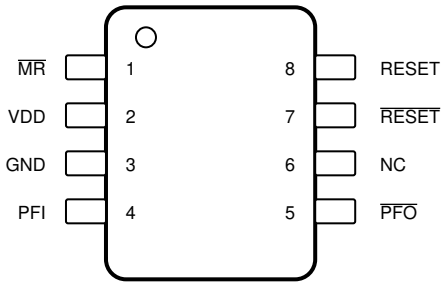


図 6-2. TPS3707-xx D Package 8-Pin SOIC Top View

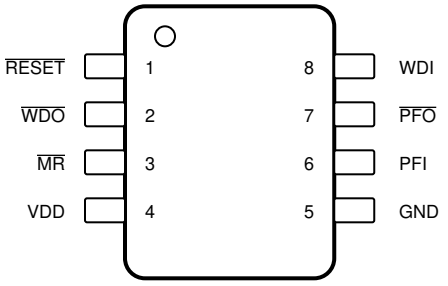


図 6-3. TPS3705-xx DGN Package 8-Pin MSOP-PowerPAD Top View

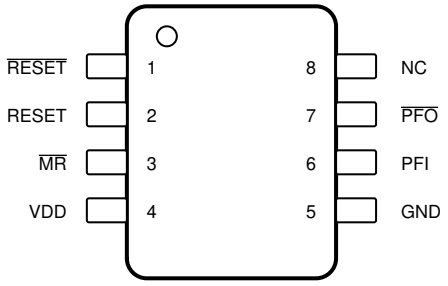


図 6-4. TPS3707-xx DGN Package 8-Pin MSOP-PowerPAD Top View

6.1 Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS3705-xx		TPS3707-xx			
	SOIC	MSOP-PowerPAD	SOIC	MSOP-PowerPAD		
GND	3	5	3	5	—	Ground
$\overline{MR}$	1	3	1	3	I	Manual reset
NC	—	—	6	8	—	No internal connection
PFI	4	6	4	6	I	Power-fail comparator input
$\overline{PFO}$	5	7	5	7	O	Power-fail comparator output
$\overline{RESET}$	7	1	7	1	O	Active-low reset output
RESET	—	—	8	2	O	Active-high reset output
V_{DD}	2	4	2	4	—	Supply voltage
WDI	6	8	—	—	I	Watchdog timer input
$\overline{WDO}$	8	2	—	—	O	Watchdog timer output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD} (2)		7	V
PFI voltage range, V_{PFI}	–0.3	V_{DD} + 0.3	V
All other pins(2)	–0.3	7	V
Maximum low output current, I_{OL}		5	mA
Maximum high output current, I_{OH}		–5	mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})		±20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})		±20	mA
Continuous total power dissipation	See セクション 7.9		
Soldering temperature		260	°C
Operating temperature, T_A	–40	85	°C
Operating temperature, T_A for TPS3705-33 only	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}			V
V_{IL}	Low-level input voltage			0.3 × V_{DD}	V
Δt/ΔV	Input transition rise and fall rate at $\overline{MR}$ or WDI			100	ns/V
T_A	Operating free-air temperature	–40		85	°C
T_A	Operating free-air temperature for TPS3705-33 only	–40		125	°C

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7.4 Thermal Information

THERMAL METRIC[1]		TPS3705-xx	TPS3707-xx	UNIT
		D (SOIC)	DGN (MSOP-PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	66.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.4	62.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	45.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.8	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	44.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	18.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	TPS370x-xx, V_{DD} = 1.1 V, I_{OH} = –4 µA	0.8			V
		TPS3707-25, TPS370x-30, TPS370x-33, V_{DD} = V_{IT+} + 0.2 V, I_{OH} = –500 µA	0.7 × V_{DD}			
		TPS370x-50, V_{DD} = V_{IT+} + 0.2 V, I_{OH} = –800 µA	V_{DD} – 1.5			
		TPS370x-xx, V_{DD} = 6 V, I_{OH} = –800 µA	V_{DD} – 1.5			
V_{OL}	Low-level output voltage	TPS3707-25, TPS370x-30, TPS370x-33, V_{DD} = V_{IT+} + 0.2 V, I_{OL} = 1 mA			0.3	V
		TPS370x-50, V_{DD} = V_{IT+} + 0.2 V, I_{OL} = 2.5 mA			0.4	
		TPS370x-xx, V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage(1)	V_{DD} ≥ 1.1 V, I_{OL} = 50 µA			0.3	V
$V_{IT–}$	Negative-going input threshold voltage(2)	TPS3707-25, T_A = 0°C to 85°C	2.2	2.25	2.3	V
		TPS370x-30, T_A = 0°C to 85°C	2.57	2.63	2.68	
		TPS370x-33, T_A = 0°C to 85°C	2.87	2.93	2.98	
		TPS370x-50, T_A = 0°C to 85°C	4.45	4.55	4.63	
		TPS3707-25, T_A = –40°C to 85°C	2.2	2.25	2.32	
		TPS370x-30, T_A = –40°C to 85°C	2.57	2.63	2.7	
		TPS370x-33, T_A = –40°C to 85°C	2.87	2.93	3	
		TPS370x-50, T_A = –40°C to 85°C	4.45	4.55	4.65	
	Negative-going input threshold voltage, PFI(2)	TPS370x-xx, V_{DD} ≥ 2 V, T_A = –40°C to 85°C	1.2	1.25	1.3	
V_{hys}	Hysteresis, V_{DD}	TPS3707-25		40		mV
		TPS370x-30		50		
		TPS370x-33		50		
		TPS370x-50		70		
	Hysteresis, PFI	TPS370x-xx		10		
$I_{IH(AV)}$	Average high-level input current, WDI	WDI = V_{DD} = 6 V, time average (dc = 88%)		100	150	µA
$I_{IL(AV)}$	Average low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V, time average (dc = 12%)		–15	–20	µA
I_{IH}	High-level input current, WDI	WDI = V_{DD} = 6 V		120	170	µA
	High-level input current, $\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		–130	–180	
I_{IL}	Low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V		–120	–170	µA
	Low-level input current, $\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	
I_I	Input current, PFI	V_{DD} = 6 V, 0 V ≤ V_I ≤ V_{DD}	–1	0	1	µA
I_{DD}	Supply current	TPS3705-xx, V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	µA
		TPS3707-xx, V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		20	50	
C_i	Input capacitance	V_I = 0 V to V_{DD}		5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active, $t_{r,VDD}$ ≥ 15 µs/V
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals

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7.6 Electrical Characteristics for TPS3705-33 Only

over operating free-air temperature range -40 to 125C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 1.1 V, I_{OH} = –4 µA	0.8			V
		V_{DD} = V_{IT+} + 0.2 V, I_{OH} = –500 µA	0.7 × V_{DD}			
		V_{DD} = 6 V, I_{OH} = –800 µA	V_{DD} – 1.5			
V_{OL}	Low-level output voltage	V_{DD} = V_{IT+} + 0.2 V, I_{OL} = 1 mA			0.3	V
		V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage(1)	V_{DD} ≥ 1.1 V, I_{OL} = 50 µA			0.3	V
$V_{IT–}$	Negative-going input threshold voltag	T_A = 0°C to 125°C	2.87	2.93	3	V
		T_A = –40°C to 125°C	2.87	2.93	3.02	
	Negative-going input threshold voltage, PFI(2)	V_{DD} ≥ 2 V	1.2	1.25	1.3	
V_{hys}	Hysteresis, V_{DD}			50		mV
	Hysteresis, PFI			10		
$I_{IH(AV)}$	Average high-level input current, WDI	WDI = V_{DD} = 6 V, time average (dc = 88%)		100	150	µA
$I_{IL(AV)}$	Average low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V, time average (dc = 12%)		–15	–20	µA
I_{IH}	High-level input current, WDI	WDI = V_{DD} = 6 V		120	170	µA
	High-level input current, $\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		–130	–180	
I_{IL}	Low-level input current, WDI	WDI = 0 V, V_{DD} = 6 V		–120	–170	µA
	Low-level input current, $\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	
I_I	Input current, PFI	V_{DD} = 6 V, 0 V ≤ V_I ≤ V_{DD}	–1	0	1	µA
I_{DD}	Supply current	V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	µA
C_i	Input capacitance	V_I = 0 V to V_{DD}		5		pF

7.7 Timing Requirements

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_w	Pulse width	At V_{DD}, V_{DD} = V_{IT+} + 0.2 V, V_{DD} = $V_{IT–}$ – 0.2 V	6			µs
		At $\overline{MR}$ and WDI, V_{DD} ≥ V_{IT+} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	100			ns

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7.8 Switching Characteristics

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out	$V_{DD} \geq V_{IT+}$ + 0.2 V, see 図 7-1	1.1	1.6	2.3	s
t_d	Delay time	$V_{DD} \geq V_{IT+}$ + 0.2 V, see 図 7-1	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay, $V_{DD} \geq V_{IT+}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		50	250	ns
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3707-xx only) $V_{DD} \geq V_{IT+}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		50	250	ns
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay		3	5	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3707-xx only)		3	5	µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	PFI to $\overline{PFO}$ delay, V_{DD} = 2 V to 6 V		0.5	1	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	PFI to $\overline{PFO}$ delay, V_{DD} = 2 V to 6 V		0.5	1	µs

7.9 Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

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7.10 Timing Diagram

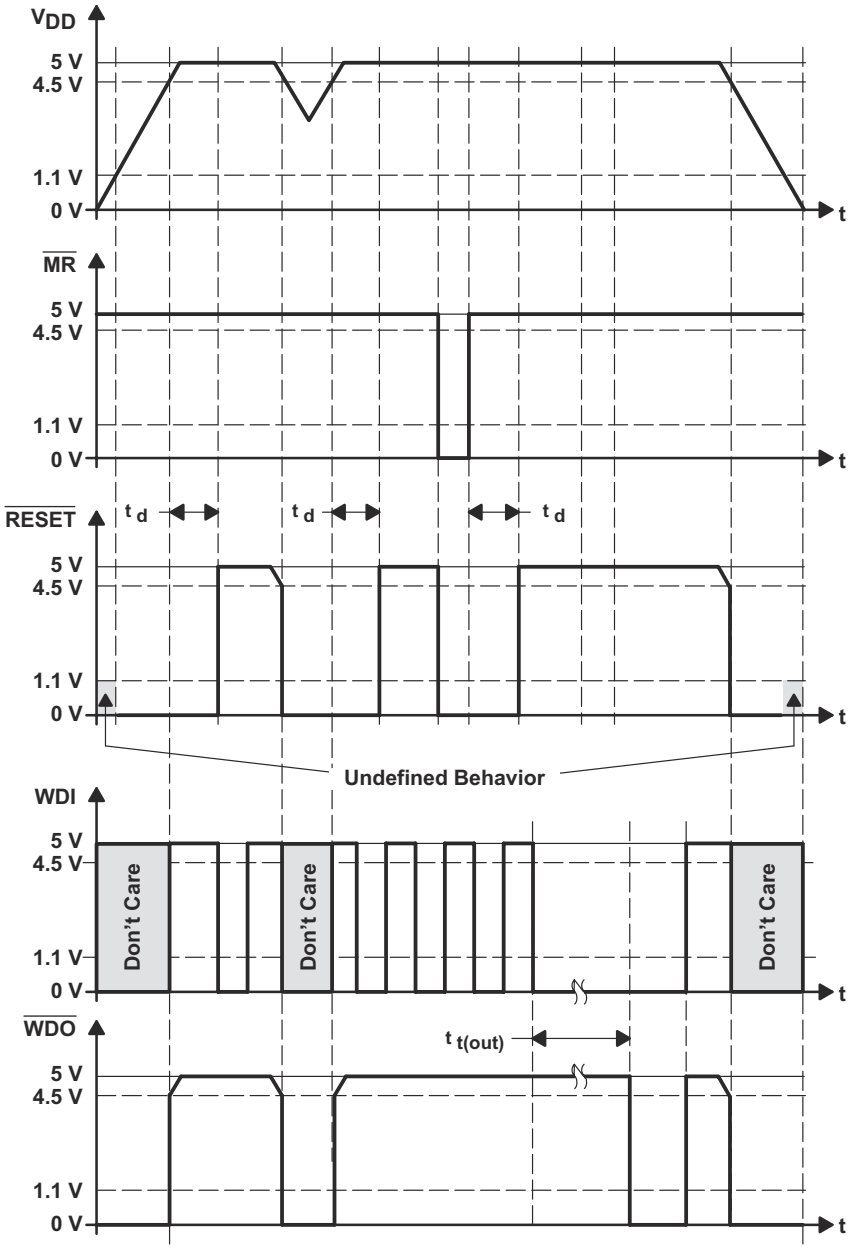


図 7-1. Timing Diagrams

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7.11 Typical Characteristics

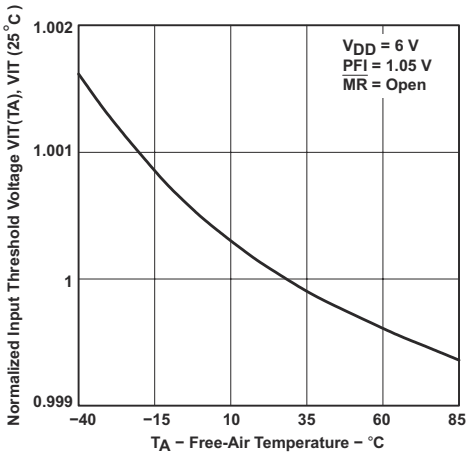


図 7-2. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

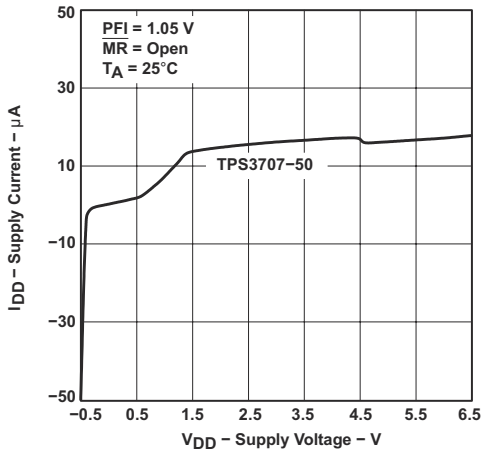


図 7-3. Supply Current vs Supply Voltage

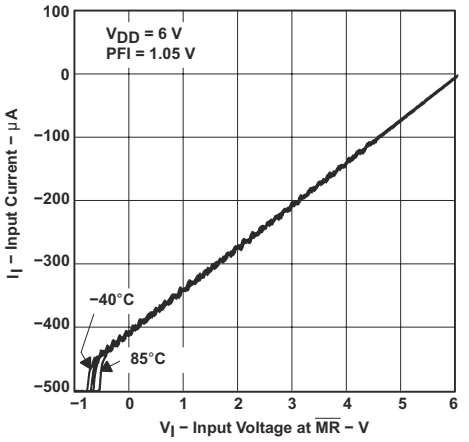


図 7-4. Input Current vs Input Voltage at $\overline{MR}$

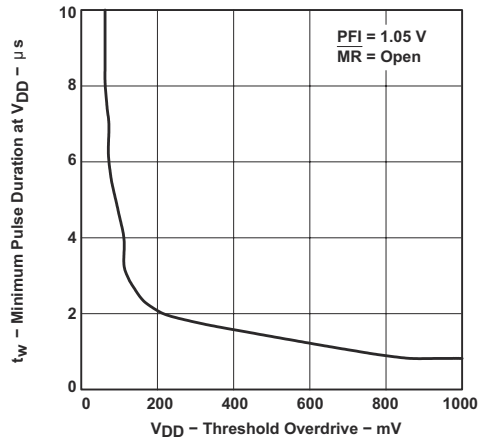


図 7-5. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

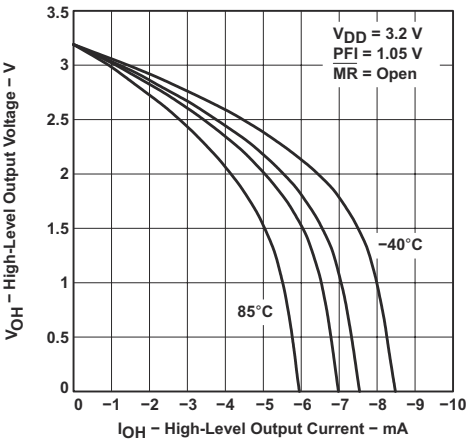


図 7-6. High-Level Output Voltage vs High-Level Output Current

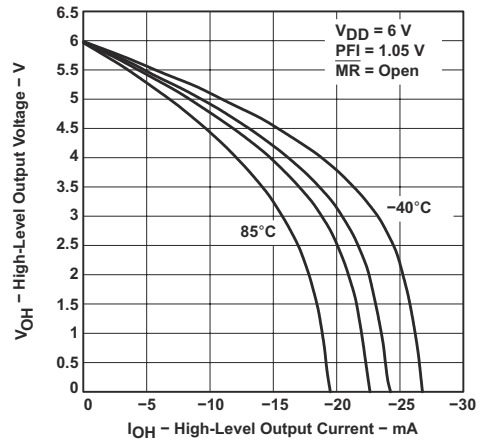


図 7-7. High-Level Output Voltage vs High-Level Output Current

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7.11 Typical Characteristics (continued)

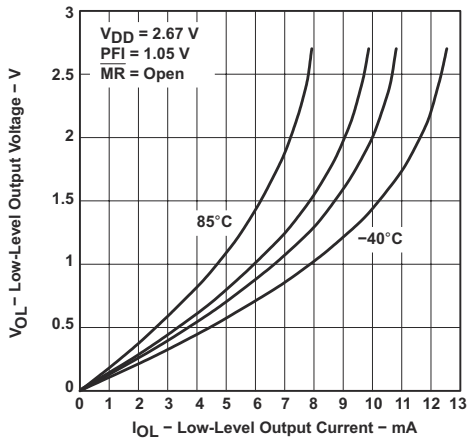


図 7-8. Low-Level Output Voltage vs Low-Level Output Current

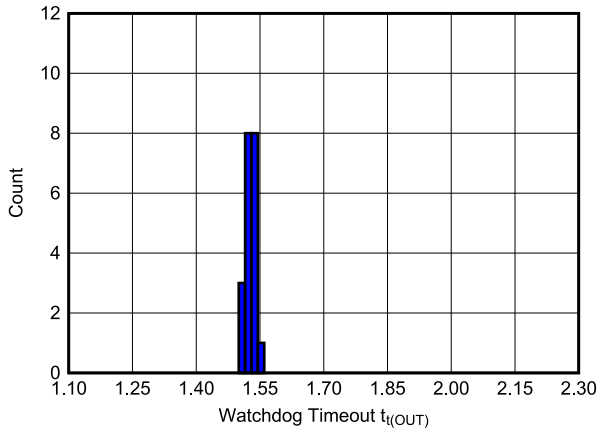


図 7-9. Watchdog Timeout Histogram for TSP3705-33 Devices at -40°C (Unit Count = 20)

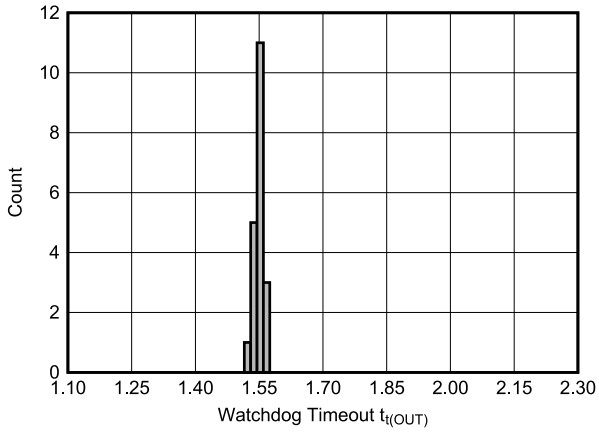


図 7-10. Watchdog Timeout Histogram for TSP3705-33 Devices at 25°C (Unit Count = 20)



図 7-11. Watchdog Timeout Histogram for TSP3705-33 Devices at 125°C (Unit Count = 20)

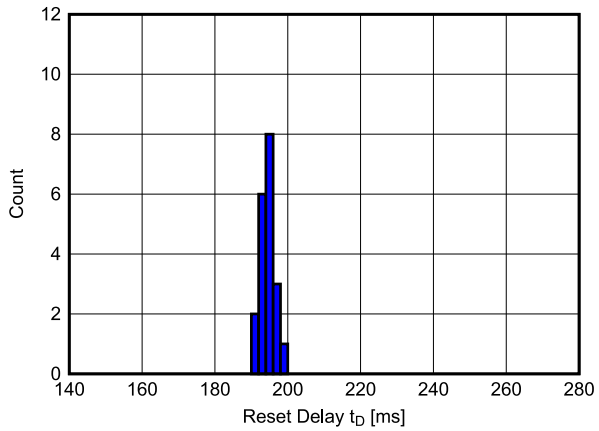


図 7-12. Reset Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)

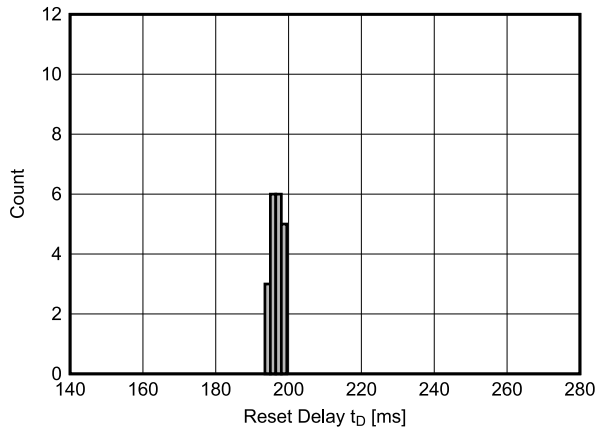


図 7-13. Reset Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)

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7.11 Typical Characteristics (continued)

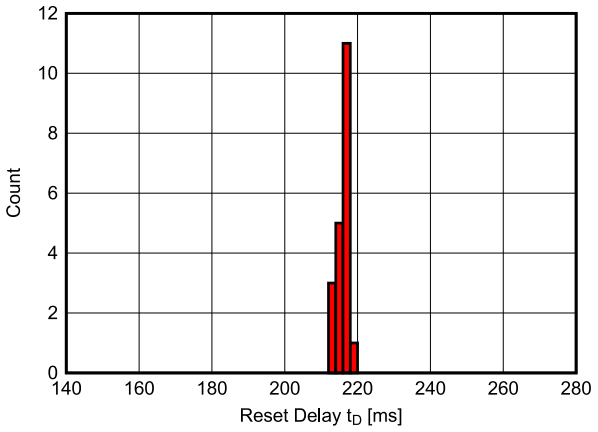


図 7-14. Reset Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)

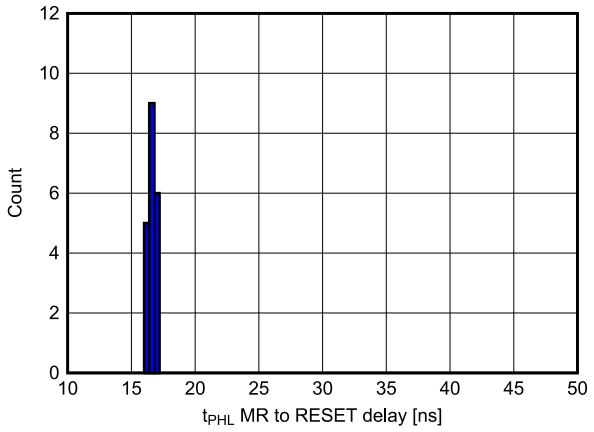


図 7-15. $\overline{MR}$ to $\overline{RESET}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)

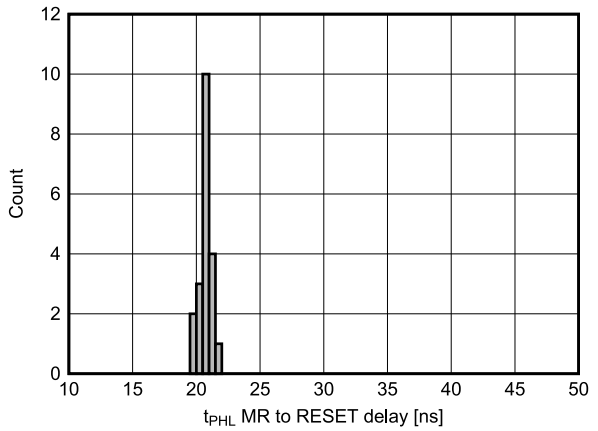


図 7-16. $\overline{MR}$ to $\overline{RESET}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)

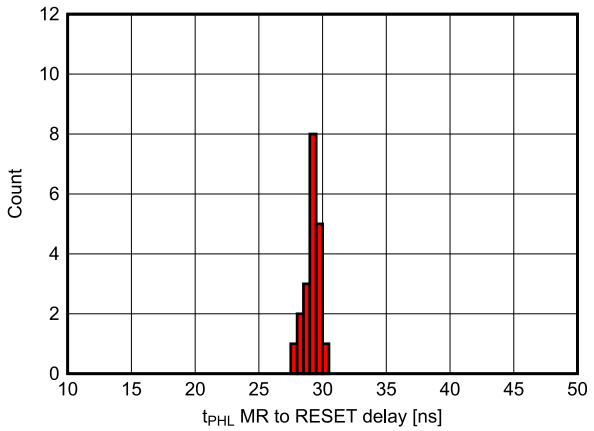


図 7-17. $\overline{MR}$ to $\overline{RESET}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)

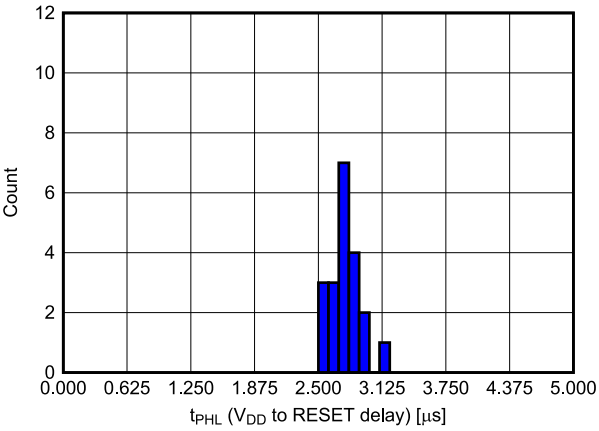


図 7-18. V_{DD} to $\overline{RESET}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)

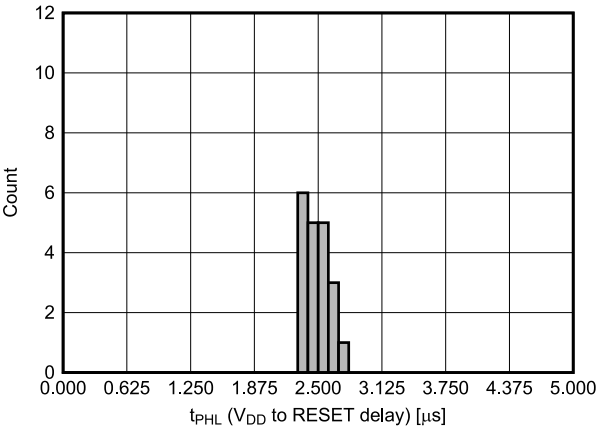


図 7-19. V_{DD} to $\overline{RESET}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)

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7.11 Typical Characteristics (continued)

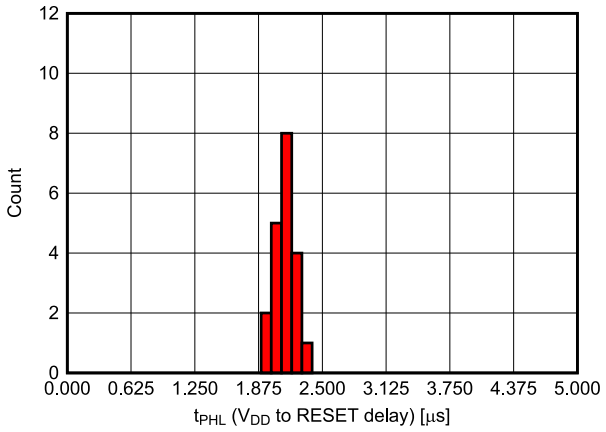


図 7-20. V_{DD} to $\overline{RESET}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)

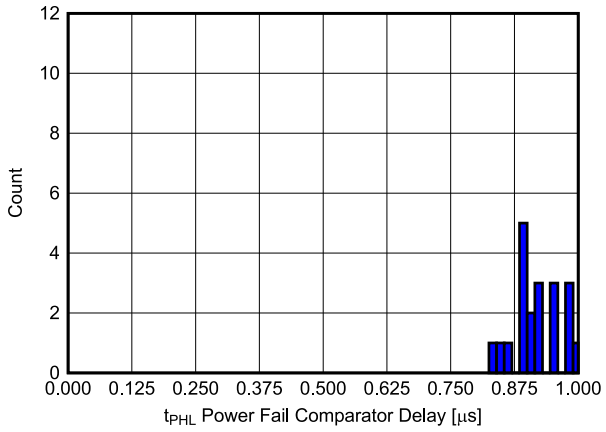


図 7-21. PFI to $\overline{PFO}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)

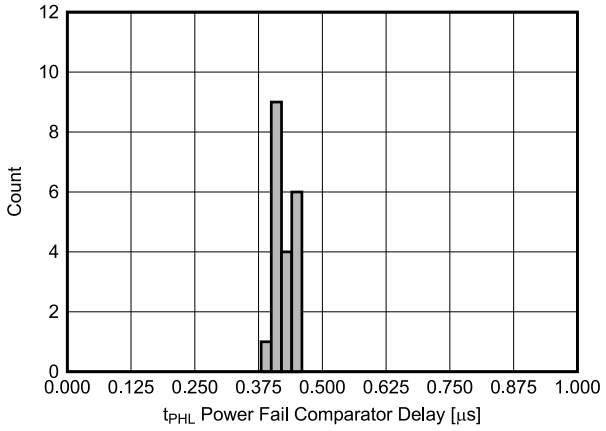


図 7-22. PFI to $\overline{PFO}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)

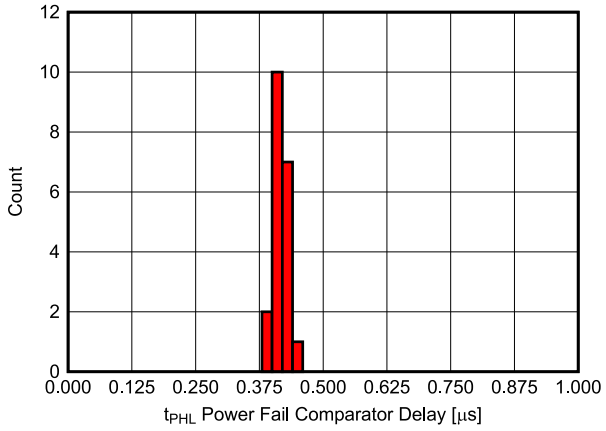


図 7-23. PFI to $\overline{PFO}$ (t_{PHL}) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)

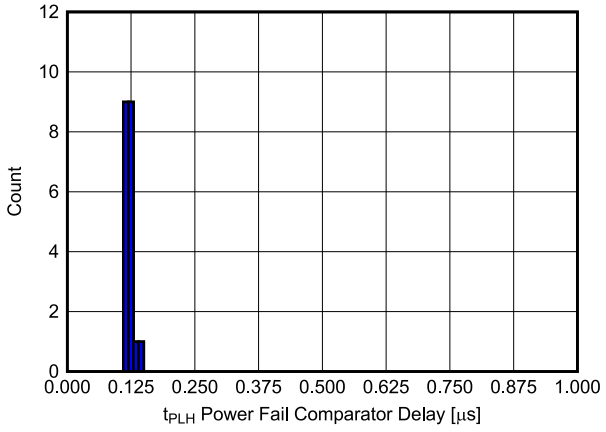


図 7-24. PFI to $\overline{PFO}$ (t_{PLH}) Delay Histogram for TPS3705-33 Devices at -40°C (Unit Count = 20)

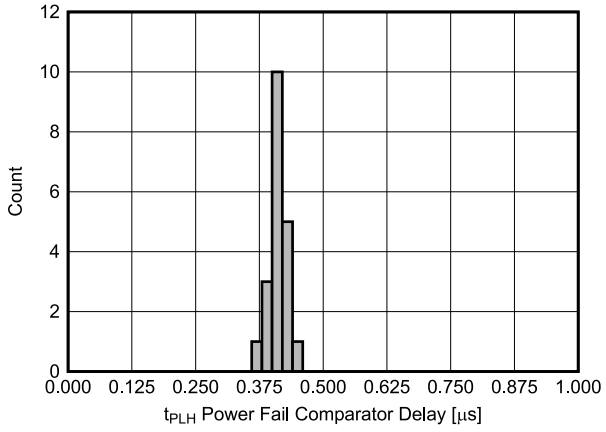


図 7-25. PFI to $\overline{PFO}$ (t_{PLH}) Delay Histogram for TPS3705-33 Devices at 25°C (Unit Count = 20)

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7.11 Typical Characteristics (continued)

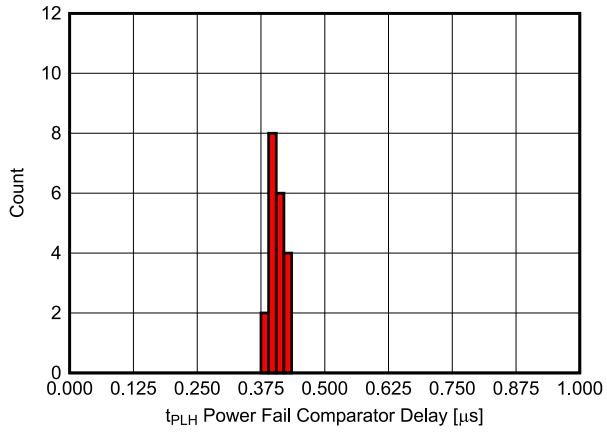


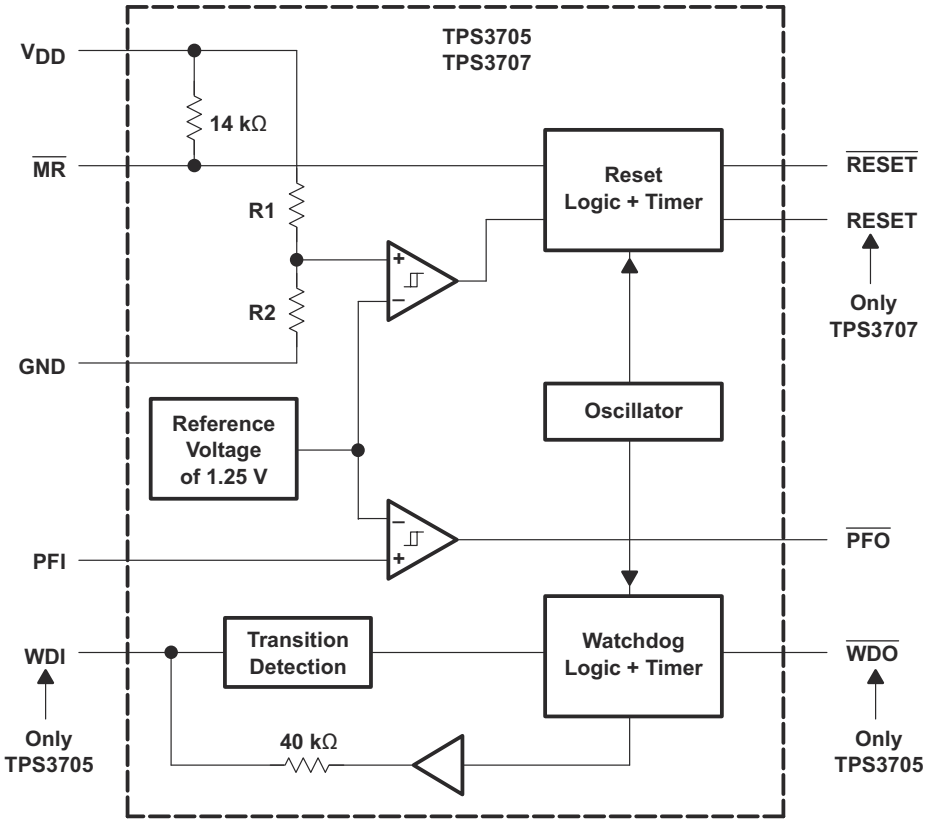
図 7-26. PFI to $\overline{PFO}$ (t_{PLH}) Delay Histogram for TPS3705-33 Devices at 125°C (Unit Count = 20)

8 Detailed Description

8.1 Overview

The TPS370x-xx family of supervisors feature an integrated reference and comparator for V_{DD} supervision, an additional power-fail supervisor, and a manual reset input. The TPS3705-xx devices feature a watchdog timer, where the TPS3707-xx devices feature a complimentary RESET output.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Manual Reset Input

The TPS370x-xx devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active.

8.3.2 Power-Fail Comparator

The TPS370x-xx family integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

8.3.3 Watchdog Timer

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the timeout interval, $t_{t(out)}$ = 1.6 s, $\overline{WDO}$ becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the watchdog function, but include a high-level output RESET.

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8.4 Device Functional Modes

8.4.1 V_{DD} < 1.1 V

When V_{DD} is less than 1.1 V, the status of the outputs cannot be determined.

8.4.2 1.1 V < V_{DD} ≤ 2 V

When V_{DD} is greater than 1.1 V but less than 2 V, the output states are valid. However, the specifications in *セクション 7.5* do not apply.

8.4.3 2 V < V_{DD} < 6 V

When V_{DD} is greater than 2 V but less than 6 V, the device is within the recommended operating conditions (see *セクション 7.3*). See 表 8-1, 表 8-2, and 表 8-3 for corresponding truth tables.

表 8-1. TPS3705 Truth Table

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	TYPICAL DELAY
H → L	1	H → L	30 ns
L → H	1	L → H	200 ms
H	1 → 0	H → L	3 µs
H	0 → 1	L → H	200 ms

表 8-2. TPS3707 Truth Table

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	RESET	TYPICAL DELAY
H → L	1	H → L	L → H	30 ns
L → H	1	L → H	H → L	200 ms
H	1 → 0	H → L	L → H	3 µs
H	0 → 1	L → H	H → L	200 ms

表 8-3. TPS370x Truth Table

PFI > V_{IT}	$\overline{PFO}$	TYPICAL DELAY
0 → 1	L → H	0.5 µs
1 → 0	H → L	0.5 µs

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9 Application and Implementation

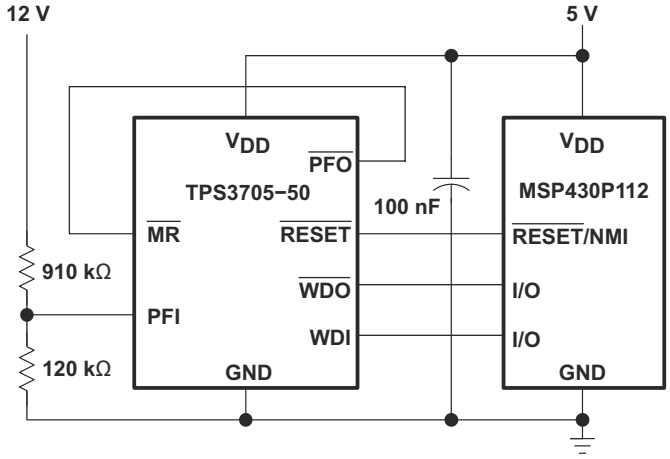
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9.1 Application Information

The TPS370x-xx family of devices offers several options for power monitoring. The TPS3705-xx offers a watchdog supervisor, V_{DD} rail monitoring, and a power-fail interrupt monitor. The TPS3707-xx offers V_{DD} rail monitoring with complimentary outputs and a power-fail interrupt monitor.

9.2 Typical Application



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図 9-1. Typical MSP430 Application

9.2.1 Design Requirements

表 9-1 lists the required design parameters for 図 9-1.

表 9-1. Application Parameters

DESIGN PARAMETER	VALUE
Monitored voltage 1	5 V
Monitored voltage 2	12 V

9.2.2 Detailed Design Procedure

To create two voltage monitoring rails, the PFI input can be used along with the MR pin to create a single output. The 5-V monitor is created by selecting a 5-V device option, giving threshold of 4.55 V. The PFI input is configured to any adjustable rail with a voltage divider. Use 式 1 to select resistors.

$$V_{TH} = \frac{R_1 + R_2}{R_2} \times V_{IT-} = \frac{910\,k + 120\,k}{120\,k} \times 1.25 = 10.73\ V \quad (1)$$

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9.2.3 Application Curves

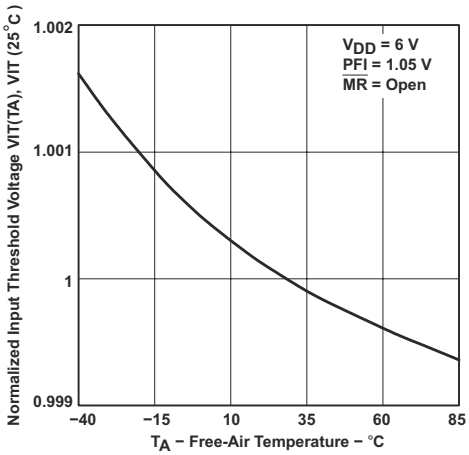


図 9-2. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

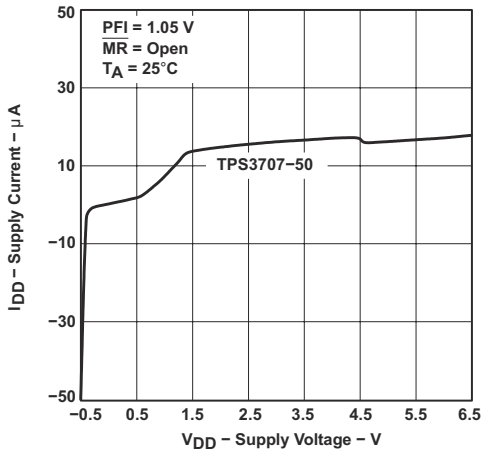


図 9-3. Supply Current vs Supply Voltage

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 2 V to 6 V.

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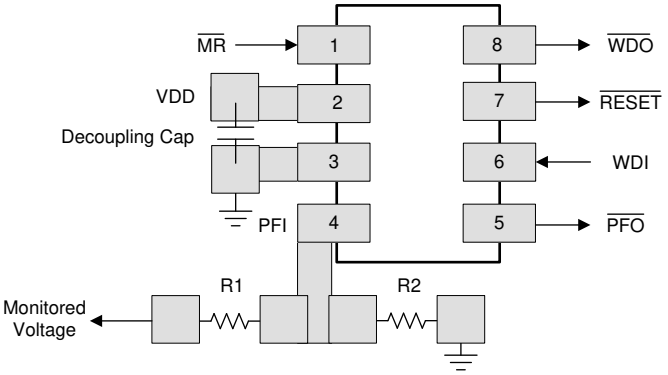
11 Layout

11.1 Layout Guidelines

Place a 0.1-µF decoupling capacitor as close to the device as possible.

If a resistor divider is used, place the resistors as close to the device as possible to minimize noise coupling.

11.2 Layout Example



TPS3705 D Package

図 11-1. TPS3705 Layout

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3705-30D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530
TPS3705-30D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530
TPS3705-30D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530
TPS3705-30DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAT
TPS3705-30DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAT
TPS3705-30DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAT
TPS3705-30DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530
TPS3705-30DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530
TPS3705-30DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70530
TPS3705-33D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-33D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-33D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-33DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-33DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU
TPS3705-33DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU
TPS3705-33DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU
TPS3705-33DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU
TPS3705-33DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU
TPS3705-33DGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAU
TPS3705-33DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-33DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-33DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	70533
TPS3705-50D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV
TPS3705-50DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV
TPS3705-50DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3705-50DGNG4	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV
TPS3705-50DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV
TPS3705-50DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV
TPS3705-50DGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAV
TPS3705-50DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3705-50DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70550
TPS3707-25D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725
TPS3707-25D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725
TPS3707-25DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW
TPS3707-25DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW
TPS3707-25DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW
TPS3707-25DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAW
TPS3707-25DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725
TPS3707-25DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70725
TPS3707-30D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730
TPS3707-30D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730
TPS3707-30DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX
TPS3707-30DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX
TPS3707-30DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX
TPS3707-30DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAX
TPS3707-30DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730
TPS3707-30DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70730
TPS3707-33D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733
TPS3707-33D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733
TPS3707-33DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY
TPS3707-33DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY
TPS3707-33DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY
TPS3707-33DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAY
TPS3707-33DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3707-33DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70733
TPS3707-50D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750
TPS3707-50D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750
TPS3707-50DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ
TPS3707-50DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ
TPS3707-50DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ
TPS3707-50DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAZ
TPS3707-50DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750
TPS3707-50DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	70750

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

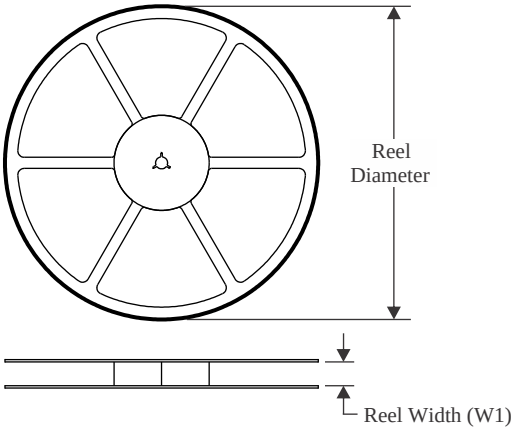
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

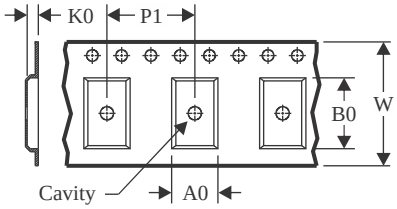
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

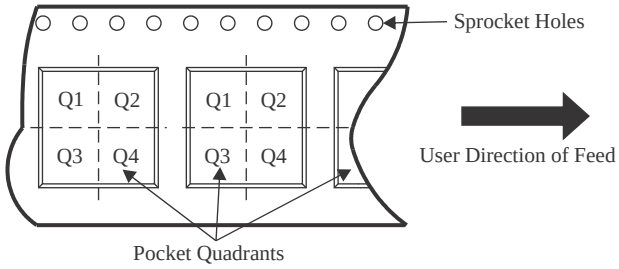


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

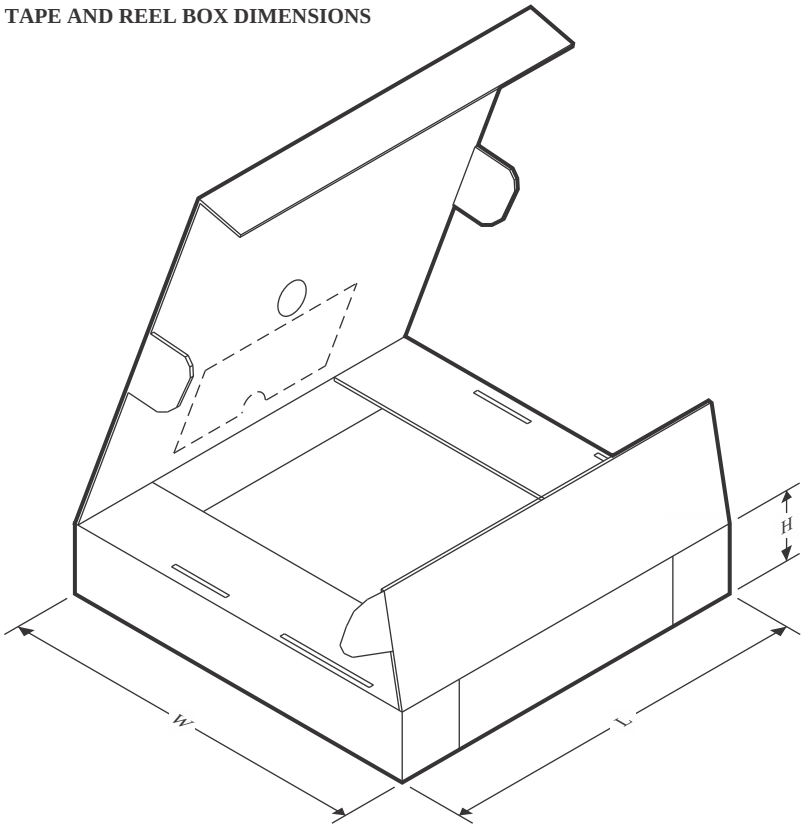
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3705-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3705-33DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3705-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3705-50DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3705-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-25DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-30DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-33DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3707-50DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3707-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

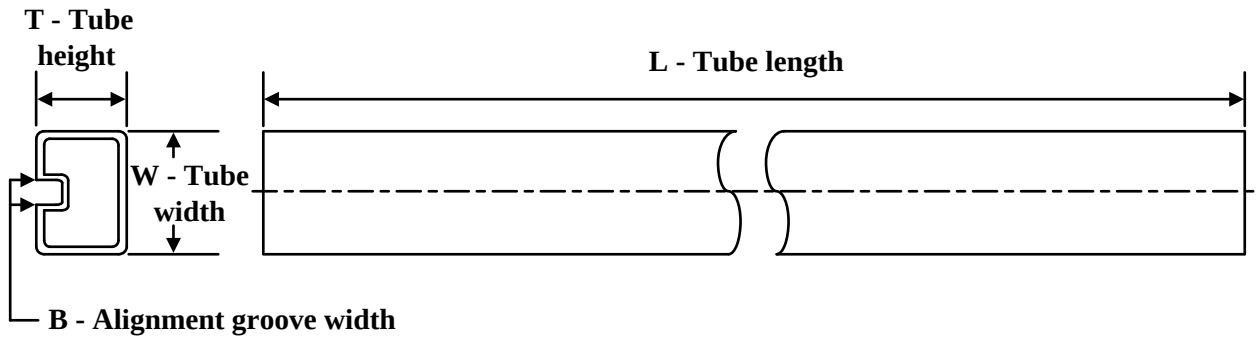
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3705-30DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3705-33DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3705-33DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3705-50DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3705-50DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3707-25DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3707-25DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3707-30DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3707-30DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS3707-33DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3707-33DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3707-50DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3707-50DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS3705-30D	D	SOIC	8	75	506.6	8	3940	4.32
TPS3705-30D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-30D.A	D	SOIC	8	75	506.6	8	3940	4.32
TPS3705-30D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-30D.B	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-30D.B	D	SOIC	8	75	506.6	8	3940	4.32
TPS3705-30DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-30DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-30DGN.B	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-33D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-33D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-33D.B	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-33DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-33DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-33DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-33DGN.B	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-50D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-50D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-50D.B	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-50DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS3705-50DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-50DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-50DGN.B	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3705-50DGNG4	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-25D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-25D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-25DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-25DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-30D	D	SOIC	8	75	506.6	8	3940	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS3707-30D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-30D.A	D	SOIC	8	75	506.6	8	3940	4.32
TPS3707-30D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-30DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-30DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-33D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-33D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-33DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-33DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-50D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-50D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3707-50DGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
TPS3707-50DGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5

GENERIC PACKAGE VIEW

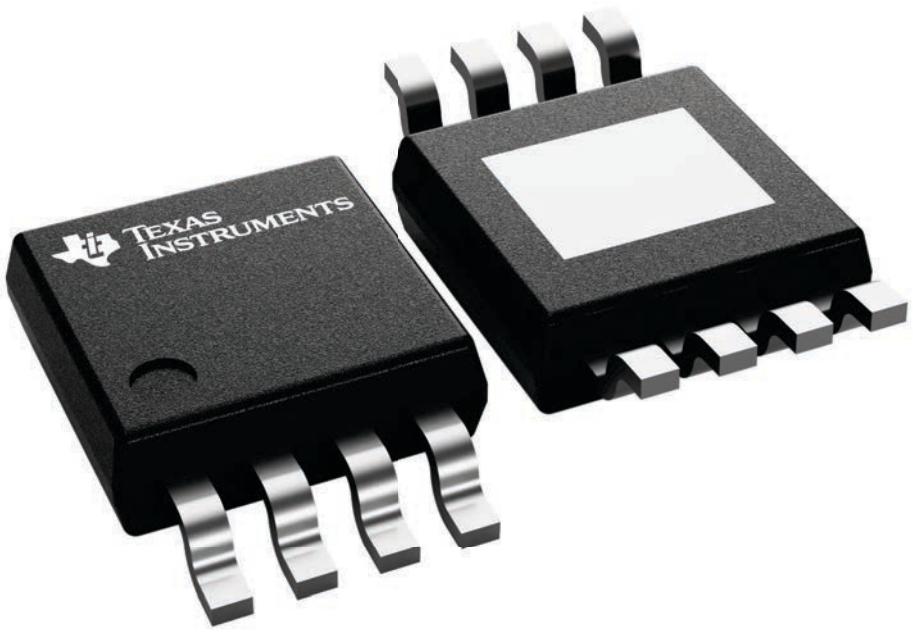
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

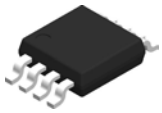
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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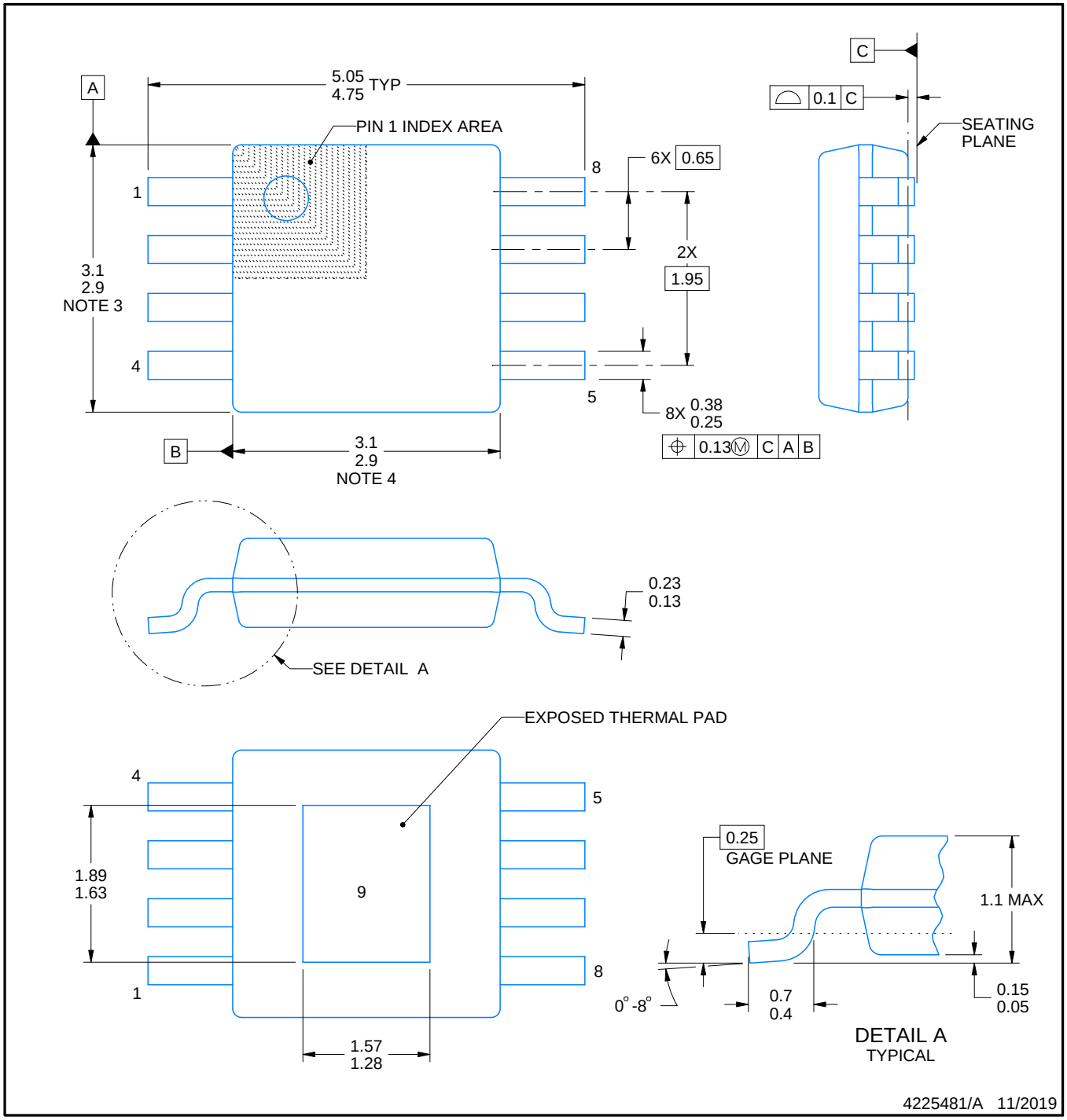
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

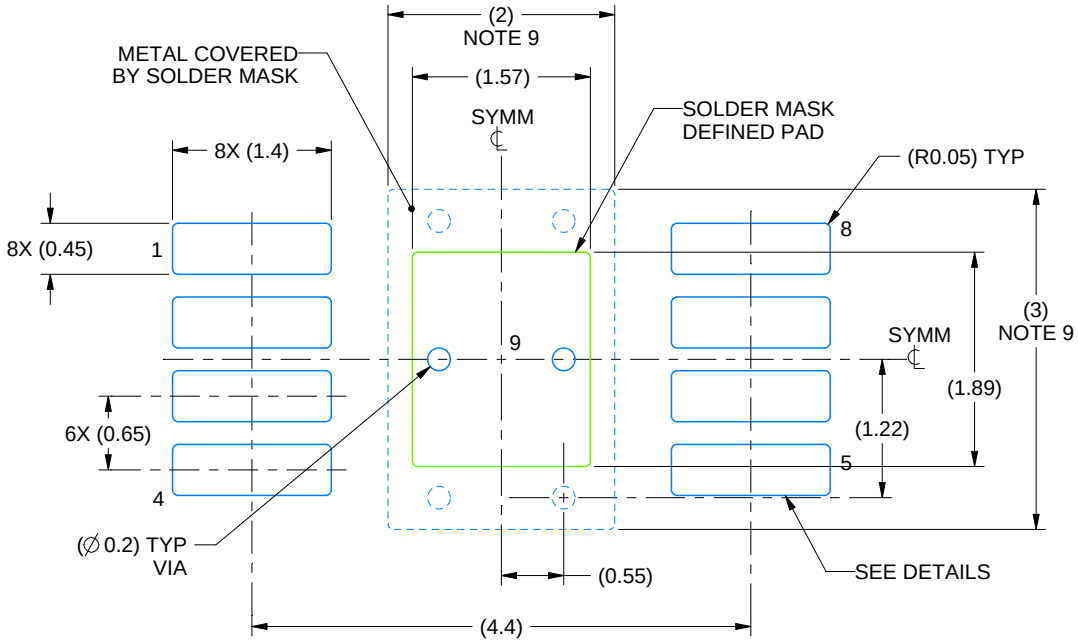
SMALL OUTLINE PACKAGE



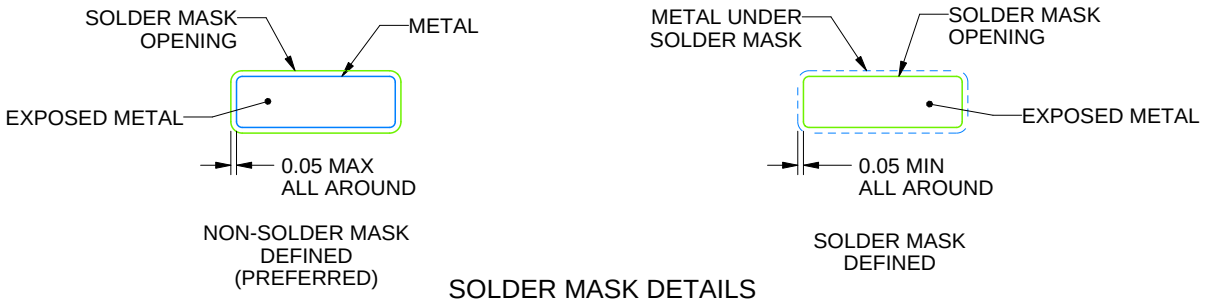
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

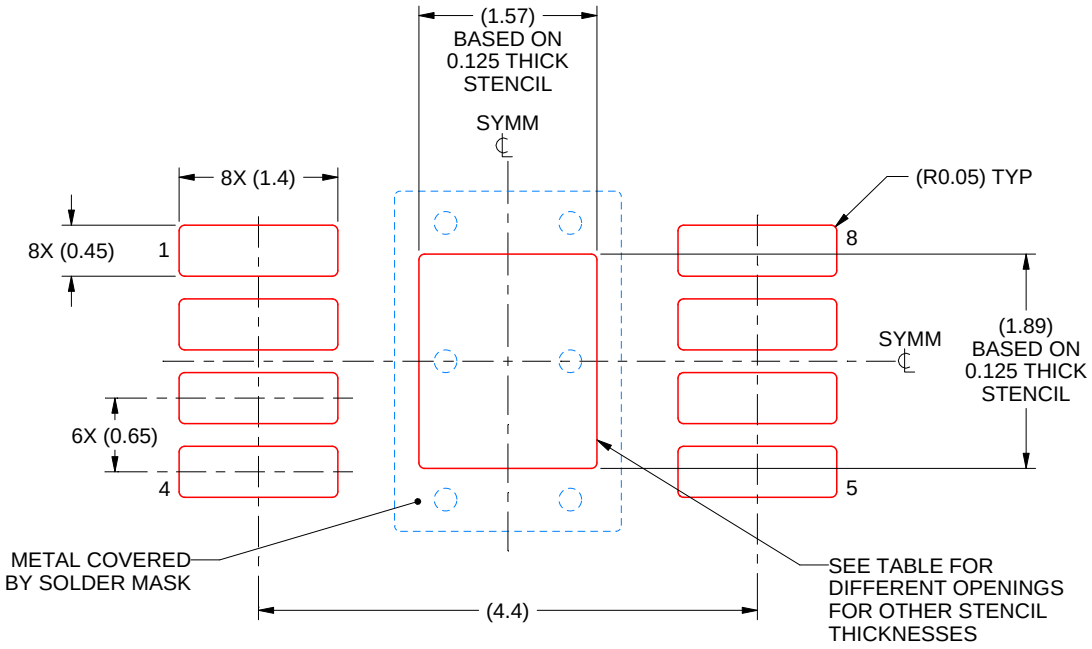


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



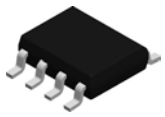
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

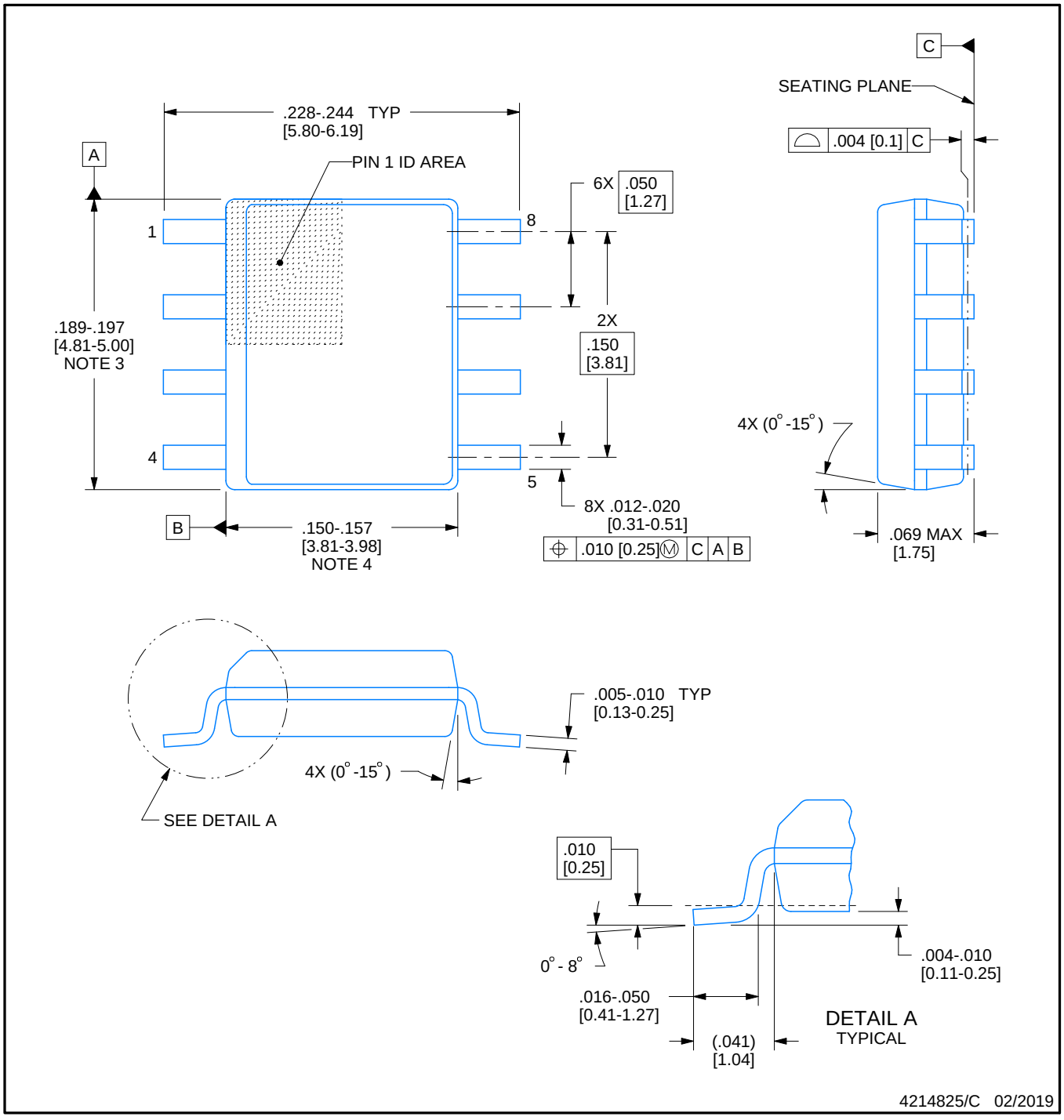


PACKAGE OUTLINE

D0008A

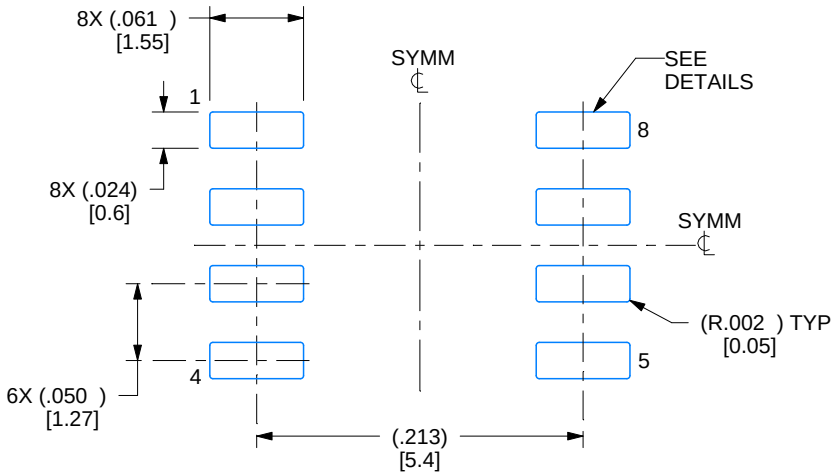
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

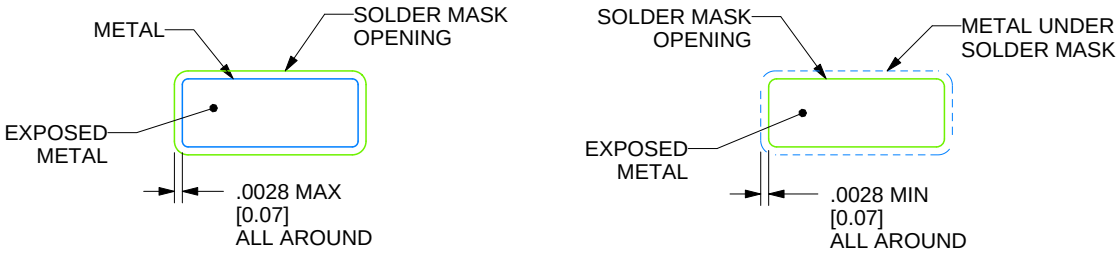


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

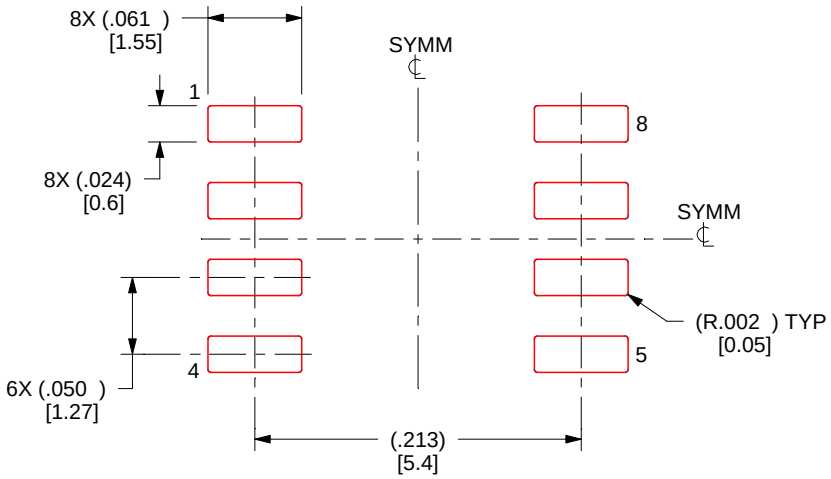
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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