TPS38700-Q1 最大 12 チャネルに対応する I²C を備えた電源シーケンサ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み：
  - デバイス温度グレード 1：-40℃ ~ +125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C7B
- 機能的安全性に準拠
  - 機能安全アプリケーション向けに開発
  - ISO 26262 システムの設計に役立つ資料をご要望に応じて提供
  - ASIL D までの決定論的対応能力
  - ASIL B までのハードウェア機能
- 入力電圧範囲：2.2V～5.5V
- 低電圧誤動作防止 (UVLO)：2.0V
- 低い静止電流：35µA (標準値)
- ウィンドウ ウォッチドッグ
- 独立した RESET
- 独立した NIRQ
- NVM エラー チェック
  - 1 ビット エラー訂正
  - 2 ビット エラー検出
- レジスタ マップでの CRC エラー チェック
- バッテリ バックアップ
- 水晶発振器オプション
- シーケンスを I²C でプログラム可能
- RTC クロック アラーム機能
- TPS389006/TPS389008 などのマルチチャネル スーパーバイザと組み合わせて使用し、完全なマルチチャネルの監視とシーケンシング状況を実現するように設計

2 アプリケーション

- 先進運転支援システム (ADAS)

3 概要

TPS38700-Q1 デバイスは、ウィンドウ ウォッチドッグを備え I²C でプログラム可能な統合型マルチチャネル電圧シーケンサで、24 ピンの 4mm × 4mm VQFN パッケージで供給されます。

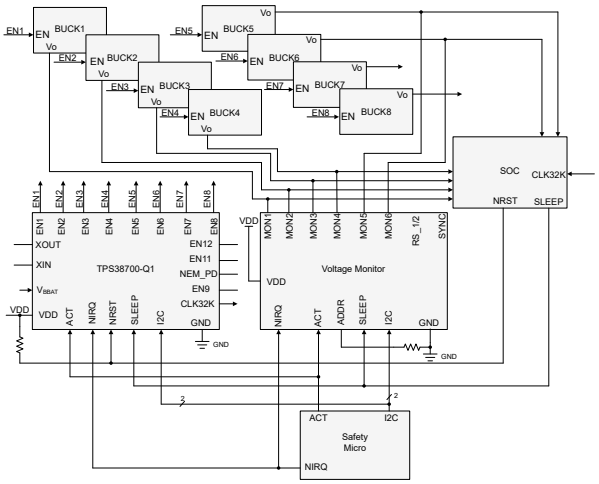
このマルチチャネル電圧シーケンサは、精密なパワーアップ / パワーダウン シーケンス動作を必要とするシステム向けに設計されておりで、マルチチャネル電圧スーパーバイザと接続できます。デフォルトで、このデバイスは事前プログラム済みの OTP オプションを利用できますが、必要に応じて、I²C を使用して、パワーアップ / パワーダウン シーケンス、ウォッチドッグの設定、シーケンス タイミングの各オプションを再プログラムすることもできます。

フレキシブルかつプログラマブルな電圧レール シーケンス機能、小さい静止電流、小さいフットプリントにより、このデバイスはほとんどのアプリケーションの要件を満たすことができます。TPS38700 は、TPS389006/TPS3890008 のような監視部品と組み合わせて使用するように設計されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TPS38700-Q1	VQFN (24)	4 mm × 4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



マルチチャネル電圧シーケンサおよびモニタ

このリソースの元の言語は英語です。 翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。 実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison

図 4-1 shows the device nomenclature of the TPS38700-Q1 device. See 表 9-2 for more information regarding device ordering codes. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

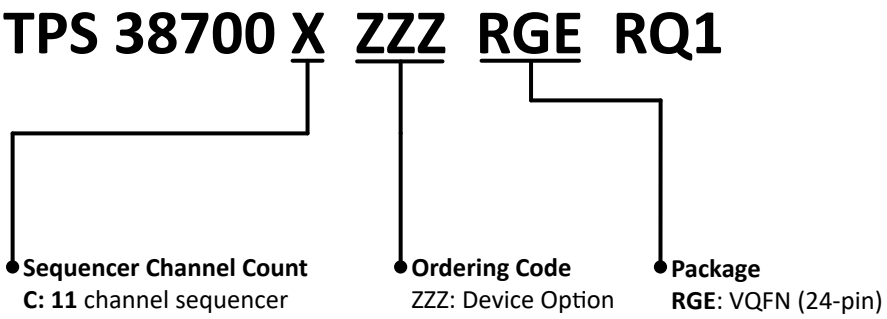


図 4-1. TPS38700-Q1 Device Nomenclature

5 Pin Configuration and Functions

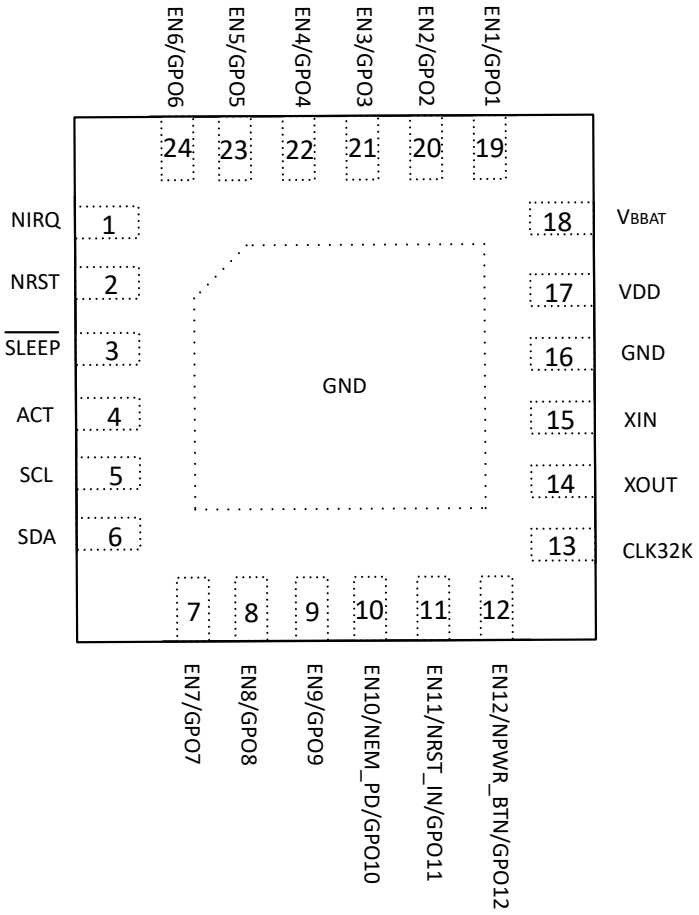


図 5-1. RGE Package
24-Pin VQFN
TPS38700 Top View

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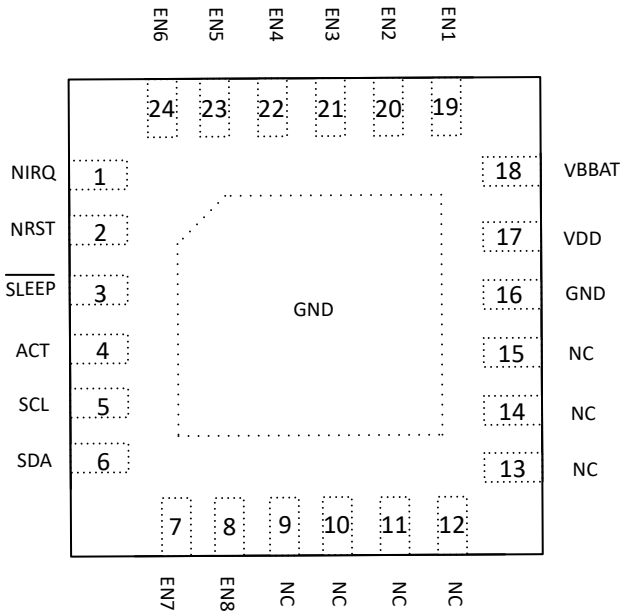


図 5-2. RGE Package
24-Pin VQFN
TPS387008 Top View

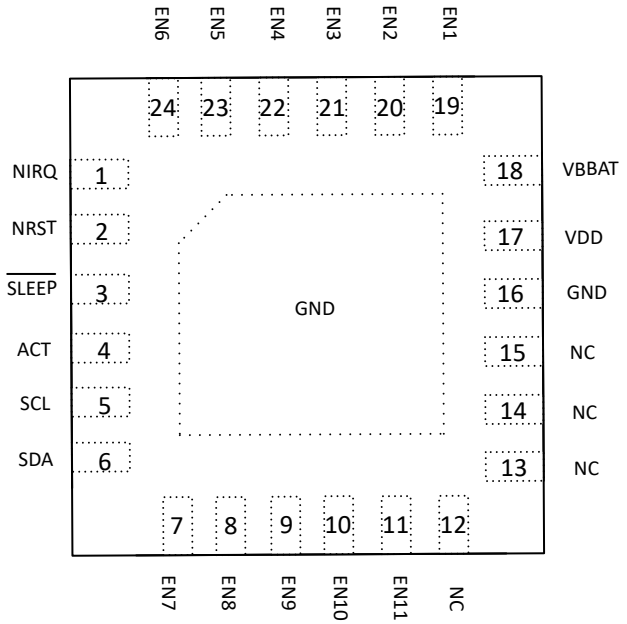


図 5-3. RGE Package
24-Pin VQFN
TPS38700B Top View

表 5-1. Pin Functions

PIN		I / O	DESCRIPTION
NO.	TPS38700-Q1 NAME		
1	NIRQ	O	Interrupt Pin (open-drain, active-low)
2	NRST	O	Reset Pin (open-drain, active-low)
3	$\overline{\text{SLEEP}}$	I	Sleep Pin (Logic high exits Sleep, logic low enters Sleep)
4	ACT	I	ACT pin (logic high starts power up SEQ, logic low starts power down SEQ)
5	SCL	I	I2C clock pin
6	SDA	I / O	I2C data pin
7	EN7 / GPO7	O	Enable 7 (open-drain / push-pull) / GPO7
8	EN8 / GPO8	O	Enable 8 (open-drain / push-pull) / GPO8
9	EN9 / GPO9	I / O	Enable 9 (open-drain/push-pull) / GPO9
10	EN10 / NEM_PD / GPO10	I / O	Enable 10 (open-drain / push-pull) / Emergency Power Down (open-drain) / GPO10
11	EN11 / NRST_IN / GPO11	I / O	Enable 11 (open-drain / push-pull) / Reset In (open-drain) / GPO11
12	EN12 / NPWR_BTN / GPO12	I / O	Enable 12 (open-drain / push-pull) / Power Button (open-drain) / GPO12
13	CLK32K	O	32.768kHZ clock output
14	XOUT	O	Crystal oscillator output
15	XIN	I	Crystal oscillator input
16	GND	-	Ground
17	VDD	-	Power supply
18	V_{BBAT}	-	Backup battery supply
19	EN1 / GPO1	O	Enable 1 (open-drain / push-pull) / GPO1
20	EN2 / GPO2	O	Enable 2 (open-drain / push-pull) / GPO2
21	EN3 / GPO3	O	Enable 3 (open-drain / push-pull) / GPO3
22	EN4 / GPO4	O	Enable 4 (open-drain / push-pull) / GPO4
23	EN5 / GPO5	O	Enable 5 (open-drain / push-pull) / GPO5
24	EN6 / GPO6	O	Enable 6 (open-drain / push-pull) / GPO6

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD, V_{BBAT}	–0.3	6	V
Voltage	NIRQ, NRST, $\overline{SLEEP}$, ACT, ENx, SDA, SCL	–0.3	6	V
Voltage	NEM_PD, NRST_IN, NPWR_BTN	-0.3	6	V
Voltage	XIN, XOUT, CLK32K	–0.3	2	V
Voltage	SCL, SDA (OTP=1.2V, 1.8V)	-0.3	2.2	V
Voltage	SCL, SDA (OTP=3.3V, 5.0V)	-0.3	5.5	V
Temperature (2)	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	125	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) As a result of the low dissipated power in this device, $T_J = T_A$.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	2.2		5.5	V
V_{BBAT}	Battery back up	1.8		5.5	V
NIRQ, NRST, ENx, $\overline{SLEEP}$, ACT	Pin voltage	0		5.5	V
I_{NRST}, I_{NIRQ}, I_{ENx}	Pin Currents	0		±1	mA
XIN, XOUT	Crystal pins	0		2	V
CLK32K	Clock output	0		2	V
NEM_PD, NRST_IN, NPWR_BTN	Pin voltage	0		5.5	V
SCL, SDA	Pin Voltage (OTP=3.3V, 5.0V)	0		5.5	V
SCL, SDA	Pin Voltage (OTP=1.2V, 1.8V)	0		2.0	V
R_{UP}	Pull-up resistor (Open Drain configuration)	10		100	kΩ
T_J	Junction temperature (free-air temperature)	-40		125	℃

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6.4 Thermal Information

THERMAL METRIC[1]		TPS38700x-Q1 RGE (VQFN) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 2.2V ≤ VDD ≤ 5.5V, NRST/NIRQ Voltage = 10kΩ to VDD, NRST/NIRQ load =10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD= 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Parameters						
VDD	Input supply voltage		2.2		5.5	V
V_{BBAT}	Backup battery voltage range		1.85		5.5	V
UVLO_VDDR	UVLO VDD	Rising threshold			2.2	V
UVLO_VDDF	UVLO VDD	Falling threshold/switch over to V_{BBAT}	1.90		2	V
UVLO_V_{BBAT}	UVLO Battery backup	Falling threshold			1.85	V
POR	Power ON reset voltage, all outputs stable above this value	Falling threshold			1.39	V
I_{DD}	Supply current into VDD pin ACT=High, $\overline{SLEEP}$=High, RTC=active	VDD ≤ 5.5V, power up sequence complete		45	75	µA
I_{DD}	Supply current into VDD pin ACT=Low, $\overline{SLEEP}$=Low, RTC=active	VDD ≤ 5.5V ,power down sequence complete		35	60	µA
I_{BBAT}	Supply current from V_{BBAT}	V_{BBAT} ≤ 5.5V		35	60	µA
I_{LKG_NRST}	Output leakage current (NRST)	VDD=V_{NRST} = 5.5V			300	nA
I_{LKG_NIRQ}	Output leakage current (NIRQ)	VDD=V_{NIRQ} = 5.5V			300	nA
ACT_L	Logic Low input				0.36	V
ACT_H	Logic high input		0.84		VDD - 0.2	V
$\overline{SLEEP}$_L	Logic Low input				0.36	V
$\overline{SLEEP}$_H	Logic high input		0.84		VDD - 0.2	V
ACT	Internal Pull down			100		kΩ
$\overline{SLEEP}$	Internal Pull down			100		kΩ
ENx	Output High	Push-Pull configuration, Io=1mA	VDD-0.2			V
	Output Low	Push-Pull or Open-Drain (10kΩ pull up)			0.1	V
R_ENx	Enable Output resistance	Push-Pull config			200	Ω
NRST	Output Low	Open-Drain (10kΩ pull up)			0.1	V
NIRQ	Output Low	Open-Drain (10kΩ pull up)			0.1	V

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6.5 Electrical Characteristics (続き)

At 2.2V ≤ VDD ≤ 5.5V, NRST/NIRQ Voltage = 10kΩ to VDD, NRST/NIRQ load =10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD= 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK32K	Leakage test	Open-Drain,4.7kΩ pull up to 1.8V, 10pF capacitive load			100	nA
	Output Low	Open-Drain, Io = -1mA, pull up to 1.8V, 10pF capacitive load			0.1	V
Acc_CLK32K	Accuracy Early Boot	t < 50ms, VDD > VDDmin	-10		10	%
	Accuracy Operating	t > 1s, VDD > VDDmin	-100		100	ppm
XTAL Fault	Crystal Frequency fault detection		-10		10	%
OSC	Internal oscillator tolerance		-5		5	%
$I_{lkg(BBAT)}$	Leakge current from V_{BBAT}	V_{BBAT} > 1.85V			300	nA
TSD	Thermal Shutdown			165		℃
TSD Hysterisis	Thermal Shutdown Hysteresis			25		℃
VIH_ALT	$\overline{NEM_PD}$, $\overline{NRST_IN}$, $\overline{NPWR_BTN}$	Pin 10,11,12 Active Low, Open-Drain	1.1			V
VIL_ALT	$\overline{NEM_PD}$, $\overline{NRST_IN}$, $\overline{NPWR_BTN}$	Pin 10,11,12 Active Low, Open-Drain			0.36	V
I2C Electrical Specifications						
C_B	Capacitive load for SDA and SCL				400	pF
SDA, SCL	Low Threshold, OTP = 1.2V				0.36	V
SDA, SCL	High Threshold, OTP = 1.2V		0.84			V
SDA, SCL	Low Threshold, OTP = 1.8V				0.54	V
SDA, SCL	High Threshold, OTP = 1.8V		1.26			V
SDA, SCL	Low Threshold, OTP = 3.3V	production variant			0.84	V
SDA, SCL	Low Threshold, OTP = 3.3V	production variant	2.31			V
SDA, SCL	Low Threshold, OTP = 5V				1.5	V
SDA, SCL	High Threshold, OTP = 5V		3.5			V
SDA	Output Low with 3mA sink current				0.2	V

6.6 Timing Requirements

At 2V ≤ VDD ≤ 5.5V, NIRQ/NRST Voltage = 10kΩ to VDD, NIRQ/NRST load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
Common parameters						
t_{D_ENx}	ENx toggle delay from start of time slot	From start of time slot			10	µs
t_{D_CLK32K}	CLK32K toggle delay from start of time slot	From start of time slot			10	µs
F_CLK32K	Frequency	Capacitive load = 12pF		32768		Hz
D_CLK32K	Duty cycle	Capacitive load = 12pF	40	50	60	%
Trf_CLK32K	Rise and fall time of CLK32K (Rpullup = 4.7kΩ)	Capacitive load = 12pF			50	ns
$t_{D_ENx,y}$	Delay between 2 subsequent EN in same time slot				1	µs
t_{NRST_EN}	ENx delay from NRST in Emergency Shutdown	Sequence 2 and 9	200			ns

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6.6 Timing Requirements (続き)

At 2V ≤ VDD ≤ 5.5V, NIRQ/NRST Voltage = 10kΩ to VDD, NIRQ/NRST load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
t_{D_NRST}	NRST assertion latency from falling edge of ACT pin below VIL or falling edge of VDD pin below VDD_{min}				25	µs
t_{D_NIRQ}	Fault detection to NIRQ assertion latency				25	µs
t_{BIST}	POR to ready with BIST	including OTP load with ECC			15	ms
t_{No_BIST}	POR to ready without BIST	including OTP load with ECC			2.5	ms
BIST time					12.5	ms
$t_{Startup_CLK32K}$	Clock 32k startup from UVLO at power ON				50	ms
Freq_fault	Crystal frequency fault detection time				1	ms
I2C Timing Characteristics						
f_{SCL}	Serial clock frequency (1)	Standard mode			100	kHz
f_{SCL}	Serial clock frequency (1)	Fast mode			400	kHz
f_{SCL}	Serial clock frequency (1)	Fast mode +			1	MHz
t_{LOW}	SCL low time (1)	Standard mode	4.7			µs
t_{LOW}	SCL low time (1)	Fast mode	1.3			µs
t_{LOW}	SCL low time (1)	Fast mode +	0.5			µs
t_{HIGH}	SCL high time (1)	Standard mode	4			µs
t_{HIGH}	SCL high time (1)	Fast Mode	1			µs
t_{HIGH}	SCL high time (1)	Fast mode +	0.26			µs
t_{SU_DAT}	Data setup time (1)	Standard mode	250			ns
t_{SU_DAT}	Data setup time (1)	Fast mode	100			ns
t_{SU_DAT}	Data setup time (1)	Fast mode +	50			ns
t_{HD_DAT}	Data hold time (1)	Standard mode	10		3450	ns
t_{HD_DAT}	Data hold time (1)	Fast mode	10		900	ns
t_{HD_DAT}	Data hold time (1)	Fast mode +	10			ns
t_{SU_STA}	Setup time for a Start or Repeated Start condition (1)	Standard mode	4.7			µs
t_{SU_STA}	Setup time for a Start or Repeated Start condition (1)	Fast mode	0.6			µs
t_{SU_STA}	Setup time for a Start or Repeated Start condition (1)	Fast mode +	0.26			µs
t_{HD_STA}	Hold time for a Start or Repeated Start condition (1)	Standard mode	4			µs
t_{HD_STA}	Hold time for a Start or Repeated Start condition (1)	Fast mode	0.6			µs
t_{HD_STA}	Hold time for a Start or Repeated Start condition (1)	Fast mode +	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition (1)	Standard mode	4.7			µs
t_{BUF}	Bus free time between a STOP and START condition (1)	Fast mode	1.3			µs
t_{BUF}	Bus free time between a STOP and START condition (1)	Fast mode +	0.5			µs
t_{SU_STO}	Setup time for a Stop condition (1)	Standard mode	4			µs
t_{SU_STO}	Setup time for a Stop condition (1)	Fast mode	0.6			µs
t_{SU_STO}	Setup time for a Stop condition (1)	Fast mode +	0.26			µs
t_{rDA}	Rise time of SDA signal (1)	Standard mode			1000	
t_{rDA}	Rise time of SDA signal (1)	Fast mode	20		300	ns
t_{rDA}	Rise time of SDA signal (1)	Fast mode +			120	ns
t_{fDA}	Fall time of SDA signal (1)	Standard mode			300	ns

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6.6 Timing Requirements (続き)

At 2V ≤ VDD ≤ 5.5V, NIRQ/NRST Voltage = 10kΩ to VDD, NIRQ/NRST load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
t_{fDA}	Fall time of SDA signal (1)	Fast mode	1.4		300	ns
t_{fDA}	Fall time of SDA signal (1)	Fast mode +	6.5		120	ns
t_{rCL}	Rise time of SCL signal (1)	Standard mode			1000	ns
t_{rCL}	Rise time of SCL signal (1)	Fast mode	20		300	ns
t_{rCL}	Rise time of SCL signal (1)	Fast mode +			120	ns
t_{fCL}	Fall time of SCL signal (1)	Standard mode			300	ns
t_{fCL}	Fall time of SCL signal (1)	Fast mode	6.5		300	ns
t_{fCL}	Fall time of SCL signal (1)	Fast mode +	6.5		120	ns
t_{SP}	Pulse width of SCL and SDA spikes that are suppressed (1)	Standard mode, Fast mode and Fast mode +			50	ns

(1) Characterized by design

6.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3V, and R_{PU} = 10kΩ, unless otherwise noted.

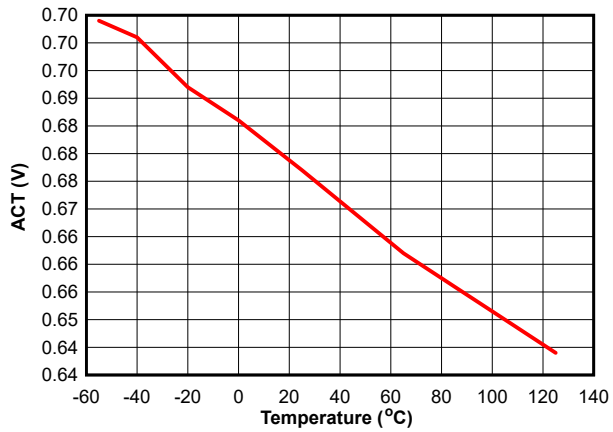


図 6-1. ACT Logic High Threshold Voltage vs. Temperature

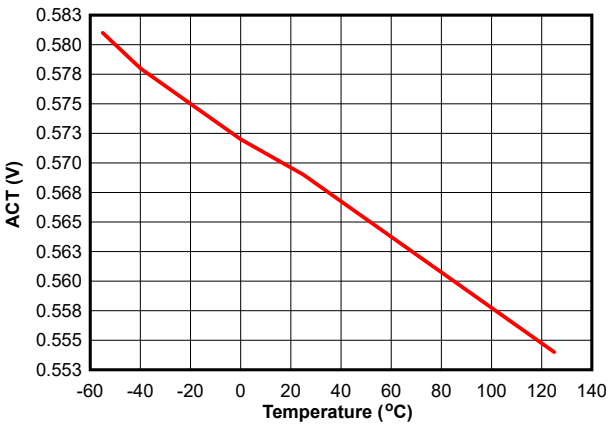


図 6-2. ACT Logic Low Threshold Voltage vs. Temperature

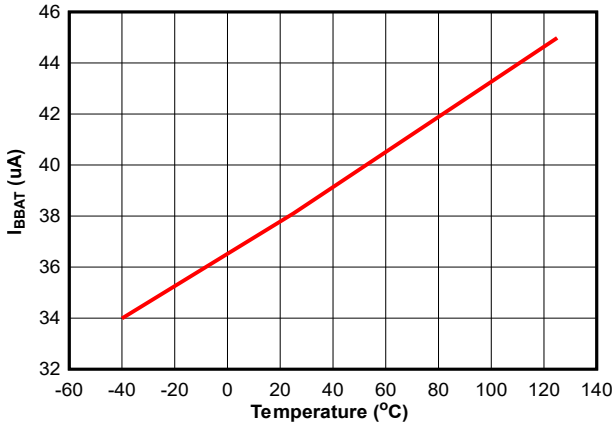


図 6-3. I_{BBAT} vs. Temperature

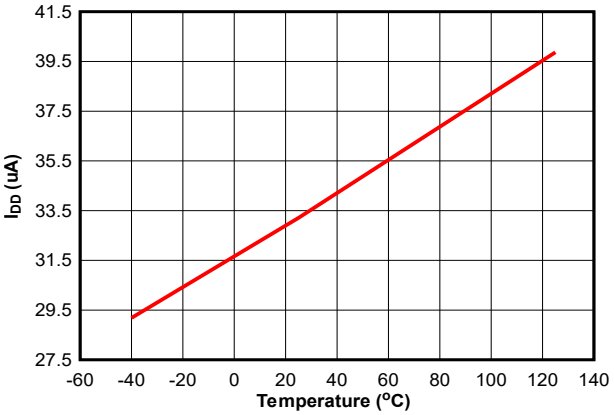


図 6-4. I_{DD} Shutdown Current vs. Temperature

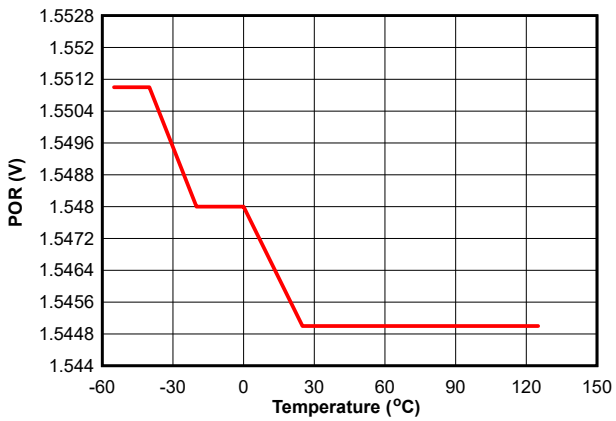


図 6-5. V_{POR} vs. Temperature

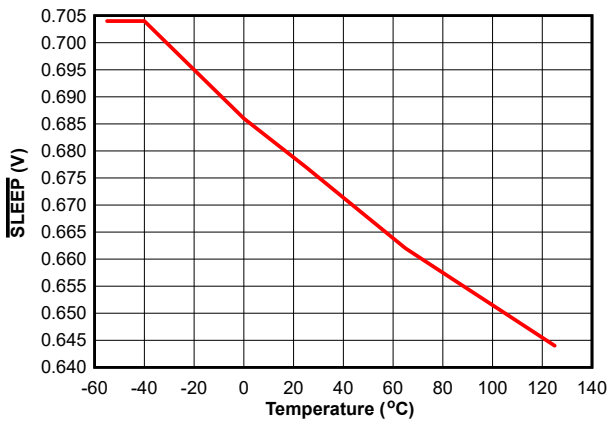


図 6-6. $\overline{SLEEP}$ Logic High Threshold Voltage vs. Temperature

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6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3V, and R_{PU} = 10kΩ, unless otherwise noted.

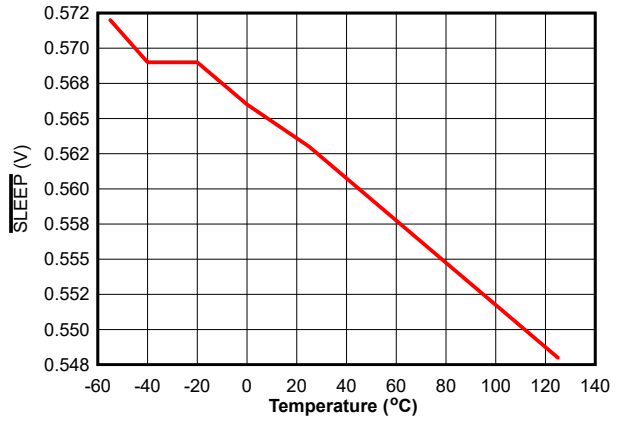


図 6-7. SLEEP Logic Low Threshold Voltage vs. Temperature

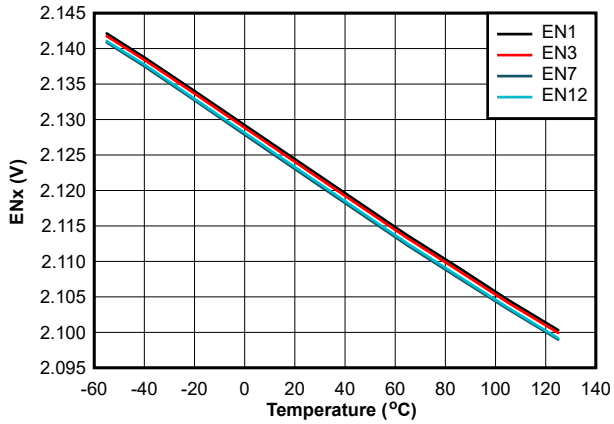


図 6-8. ENx Logic High Output Voltage vs. Temperature

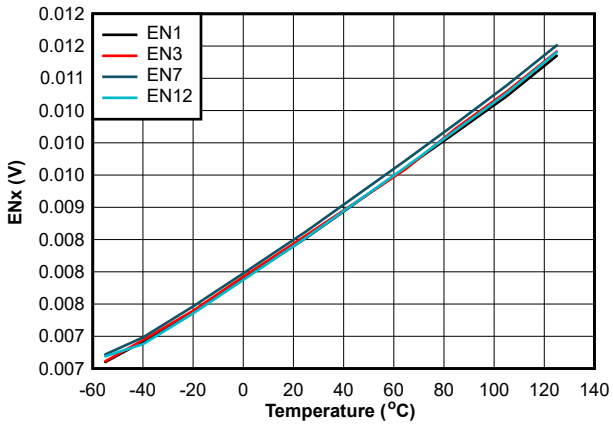


図 6-9. ENx Logic Low Output Voltage vs. Temperature

7 Detailed Description

7.1 Overview

TPS38700-Q1 is a versatile part that can be configured for multiple configurations. The part can be ordered as a pure sequencer, pure GPIO expander, or combination sequencer & GPIO outputs. The outputs can be factory configured as push-pull or open-drain. Sequencing outputs can be assigned to ACT pin and/or $\overline{\text{SLEEP}}$ pin. These sequencing outputs can be factory configured for default values and subsequently changed via I^2C on power-up before sending ACT pin high. The device also features a Built in Self-Test (BIST) function which runs automatically on power up.

TPS38700-Q1 features a precise Real Time Clock (RTC) CLK32K output with the aide of an external crystal (XTAL). The TPS38700-Q1 also has an RTC alarm feature and a window watchdog, all of which can be configured via I^2C. The TPS38700-Q1 is capable of various I^2C logic levels. A full featured Graphical User Interface (GUI) is available for download in the product folder. Contact a Texas Instruments representative for custom configured part queries.

TPS38700-Q1 can be configured to have up to twelve channels and has an emergency power down (NEM_PD) function that is activated once VDD falls below the UVLO threshold of the device. Once in the emergency power down sequence, the TPS38700-Q1 either turns off or enter into Backup state. If a voltage on V_{BBAT} is present and greater than 1.85V, then the TPS38700-Q1 enters into Backup state and the power supply for the device switches to V_{BBAT}.

The TPS38700-Q1 is AEC-Q100 qualified for automotive applications and has been characterized from -40ºC to +125ºC.

7.2 Functional Block Diagram

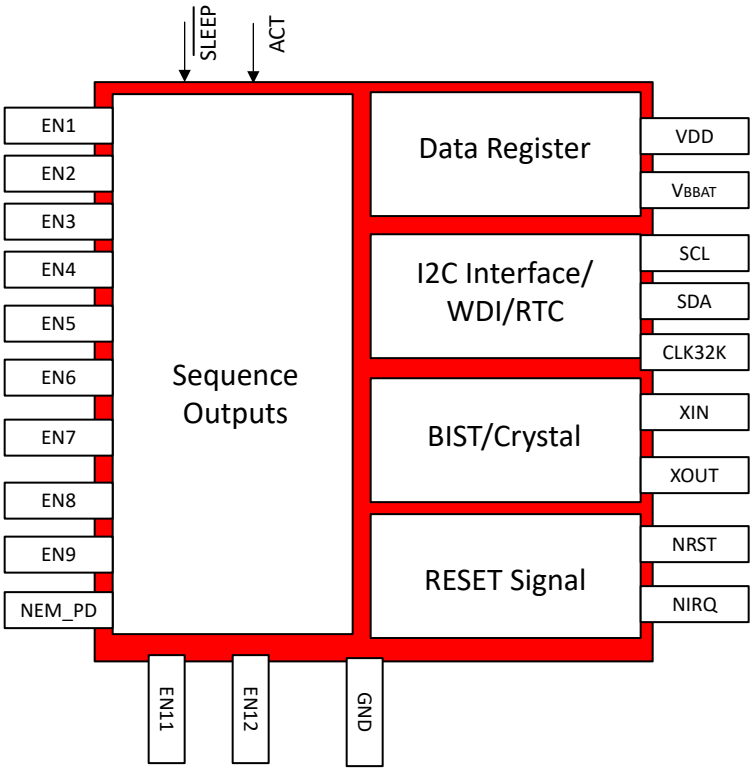


図 7-1. TPS38700-Q1 Block Diagram

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7.3 Feature Description

7.3.1 Device State Diagram

The TPS38700-Q1 state diagrams shown in 図 7-2 and 図 7-3 show the flow of operation.

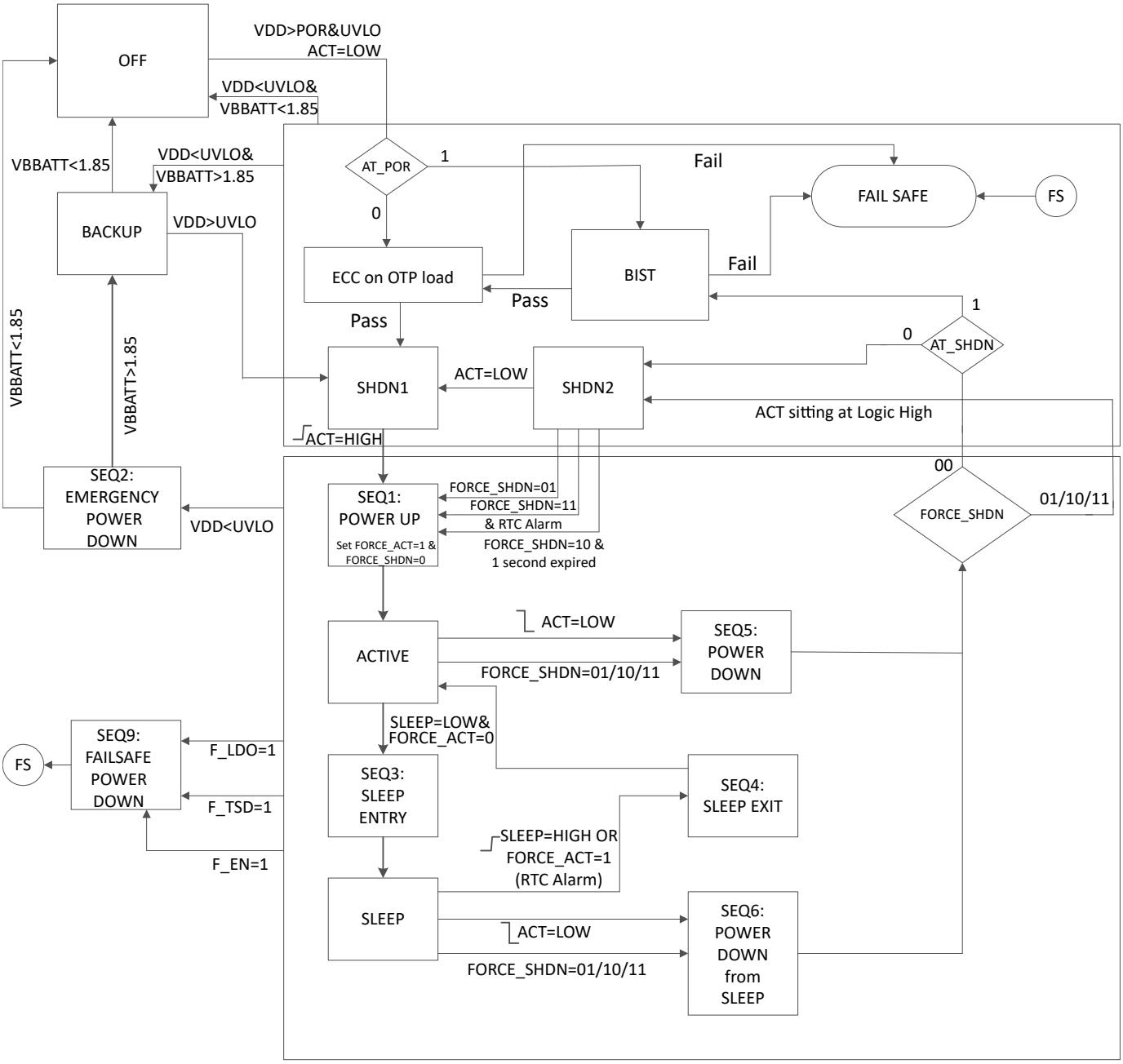


図 7-2. TPS38700-Q1 State Diagram

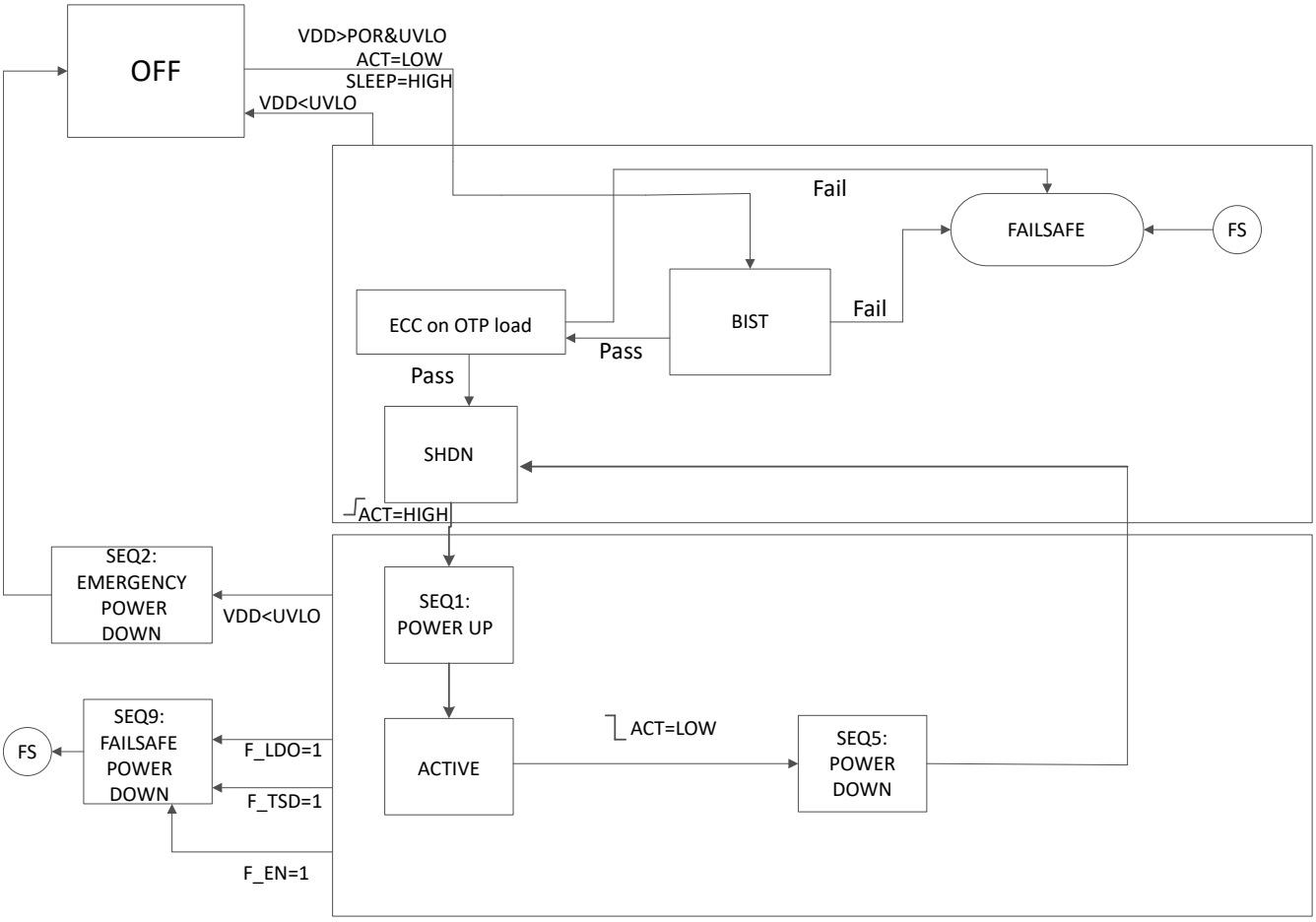


図 7-3. TPS38700-Q1 Simple Use Case

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7.3.2 Built-In Self Test and Configuration Load

Built-In Self Test (BIST) is performed:

- AT POR, if TEST_CFG_AT_POR = 1
- When exiting Sequence 5 or Sequence 6, if TEST_CFG_AT_SHDN = 1 and the power down is not initiated by CTL_1. FORCE_SHDN[1:0] being set to 01b, 10b, or 11b.

Configuration load from OTP is assisted by ECC (supporting SEC-DED). This is to protect against data integrity issues and to maximize sysetem availability.

During BIST, NIRQ is de-asserted (asserted in case of failure), NRST is held low, ENx pins are held low (including pins with alternate functions), CLK32K is held low, input pins are ignored, and the I^2C block is inactive with SDA and SCL de-asserted. Once BIST is completed without failure, I^2C is immediately active and the device enters SHDN1 state after loading the configuration data from OTP. If BIST fails and/or ECC reports Double-Error Detection (DED), NIRQ is asserted, the device enters the FAILSAFE state (inputs are ignored), and a best effort attempt is made to active I^2C. TEST_STAT register can provide additional information on the test results.

7.3.3 CLK32K

The TPS38700-Q1 is designed to give an accurate CLK32K output and is used internally for setting the RTC time and alarms. TPS38700-Q1 is configured to be used with a 32.768kHz crystal oscillator. To achieve a well-defined frequency of oscillations, all crystals oscillators are tuned at specific capacitive load such as 6.5pF, 12pF, or 20pF (during manufacturing stage), which becomes a part of the crystal specification. The task of a designer is to design within the crystal's specifications to achieve the correct specified frequency.

For these crystal oscillators, the need for loading capacitors are required because the capacitive load is effectively split between the output and input capacitance in a typical Pierce Oscillator scheme. These capacitors are essentially connected in series with the crystal oscillator. Therefore, if a chosen crystal oscillator has a capacitive load that is specified for 12.5pF load, then the need for two 12.5pF capacitors are required for proper frequency output from the crystal oscillator.

The TPS38700-Q1 is configured to be used without the need of loading capacitors, as long as the 6.5pF version of the external crystal oscillator is selected. External crystal oscillators typically specifies the internal capacitance such as 6.5pF, 9pF, 12.5pF etc. If the external crystal oscillator has load capacitance specification requirement not equal to 6.5pF, please contact the TI factory for an OTP (one time programming) configuration for the correct external capacitor loading.

The CLK32K signal can start as late as 50ms from when the input voltage VDD exits out of UVLO. The accuracy of CLK32K is within ±100ppm after one second of initial operation. If the frequency of CLK32K deviates for more than ±10%, a fault interrupt is asserted. The accuracy of the CLK32K also depends on the choice of external crystal oscillator and specification of temperature rating.

7.3.4 BACKUP State

In the BACKUP state only the battery is supplying power to the device, however the device must have gone through a VDD supplied state (and loaded configuration data) to enter this state. If no VDD supplied state has occurred, then the TPS38700-Q1 stays in the "OFF or Battery Installed" state, and only exits with a valid VDD supply.

When in BACKUP state, the TPS38700-Q1 pins are in the following state:

- ENx = Low (de-asserted)
- CLK32K = Low (output disabled)
- NRST = Low (asserted)
- ACT and $\overline{\text{SLEEP}}$ inputs are ignored.

Crystal oscillator and RTC remain active with Acc_CLK32K accuracy, but the crystal oscillator fault monitor is not active. RTC_T[31:0], interrupt, and status registers are maintained and updated. Registers configuration is

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maintained as set before entering the BACKUP state. PROT1 and PROT2 registers are cleared. All remaining blocks are inactive.

Upon exiting from the BACKUP state, the last configuration is active and the device enters the SHDN1 state.

7.3.5 FAILSAFE State

When in FAILSAFE state, ENx, CLK32K, NRST, NIRQ are all held Low, and a best effort attempt is made to keep I^2C active. ACT and $\overline{SLEEP}$ inputs are ignored.

To exit from FAILSAFE state, VDD has to be removed. Depending on V_{BBAT}, TPS38700-Q1 enters BACKUP or OFF state.

7.3.6 Transitioning Sequences

The sequences of the device are described here with timing diagrams showing the main signals involved in each sequence.

7.3.6.1 Sequence 1: Power Up

When NPWR_BTN is not enabled, power-up is controlled by ACT, shown in 図 7-4.

When ACT is high, the ENx output sequence starts and NRST is de-asserted RST_DLY[3:0] time after the last ENx. The power-up sequence is defined by PWR_ENx registers, for more information see 表 7-33.

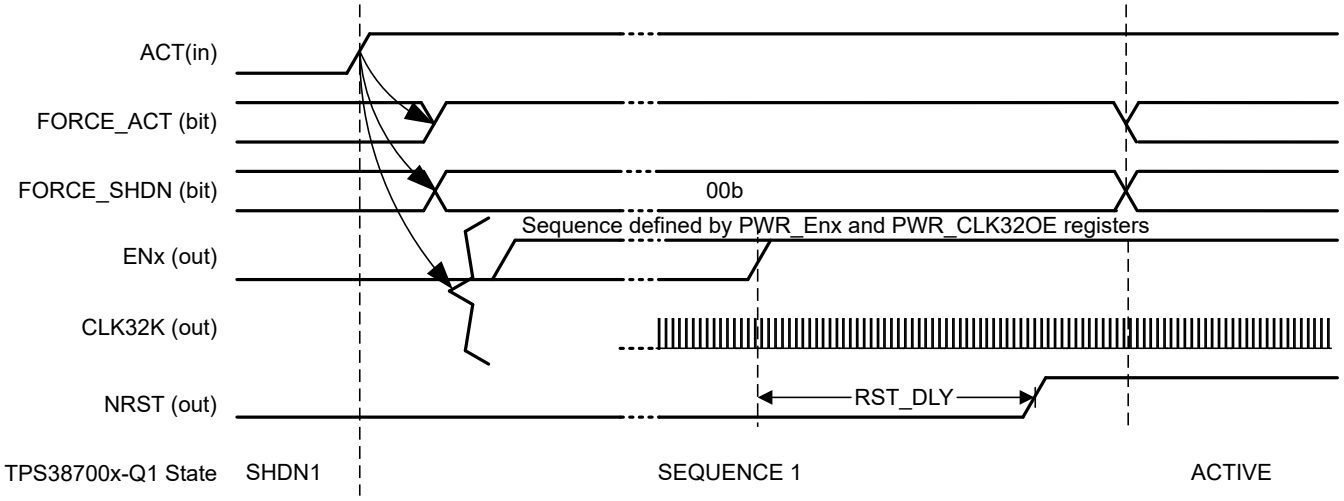


図 7-4. Power Up with NPWR_BTN Disabled - ACT controlled

When NPWR_BTN is enabled, ACT is used as AUTO/BUTTON power-on strap option. With ACT strapped to VDD, a short push on NPWR_BTN starts the power-up sequence; with ACT strapped to GND, the power-up sequence automatically starts once VDD is valid. From SHDN2 state a short push on NPWR_BTN is always required to start the power-up sequence. See 図 7-5 for details. When power-up is triggered, the ENx output sequence starts and NRST is de-asserted CTL_2.RST_DLY[3:0] time after the last ENx.

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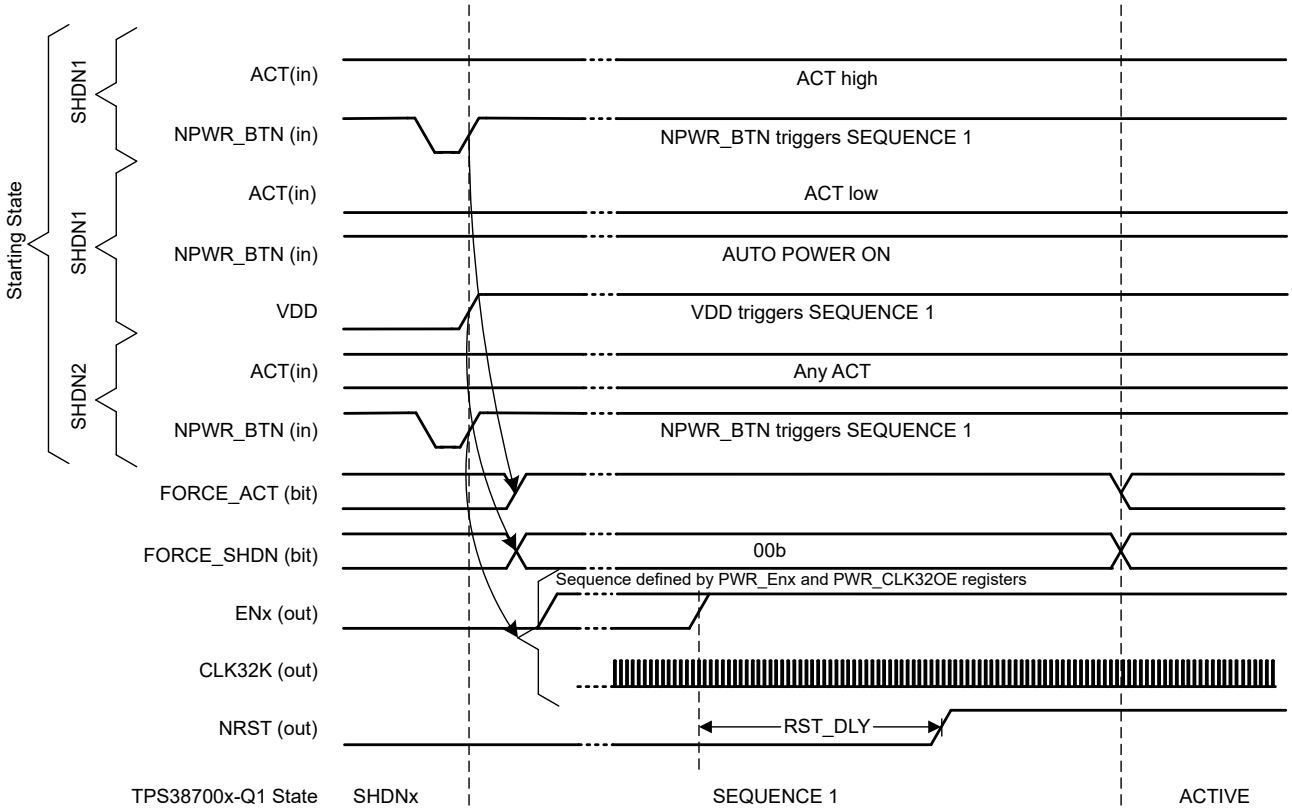


図 7-5. Power Up with NPWR_BTN Enabled

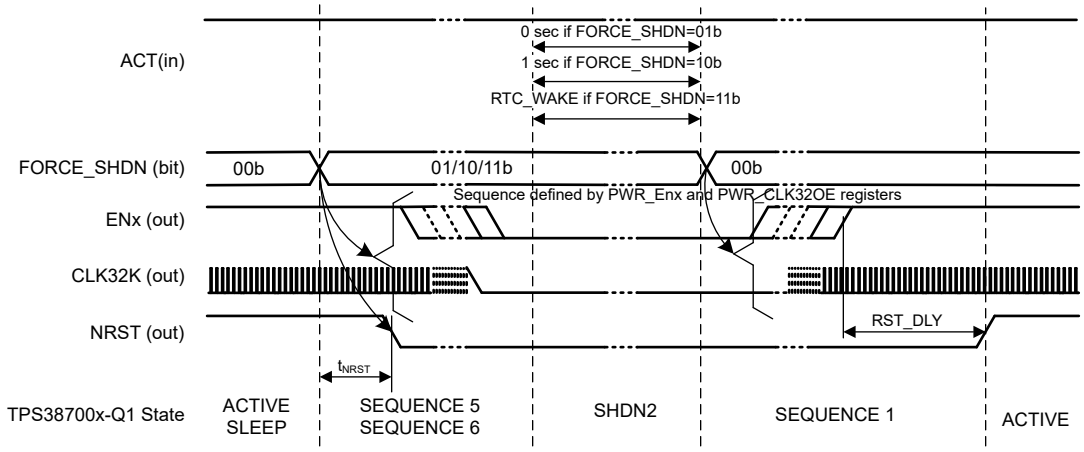


図 7-6. Power Up from SHDN2 - Software Shutdown with FORCE_SHDN ≠ 00b

7.3.6.2 Sequence 2: Emergency Power Down

In case of emergency power down (VDD drops below UVLO), a best effort approach is taken to assert NRST before pulling ENx, CLK32K, and NIRQ down.

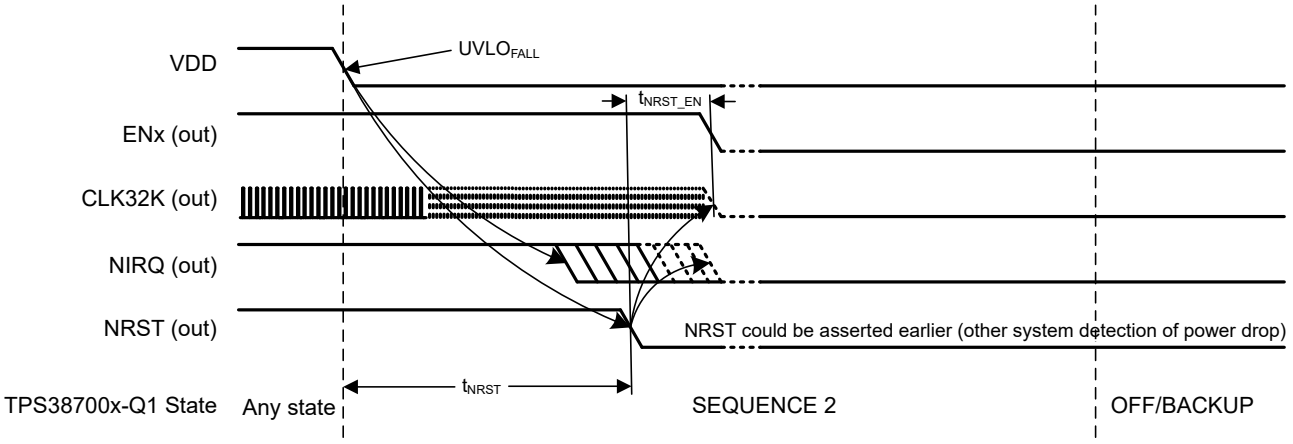


図 7-7. Emergency Power Down

7.3.6.3 Sequence 3: Sleep Entry

Sleep entry is controlled by $\overline{\text{SLEEP}}$ going low. This triggers the ENx pins to de-assert as per the configuration in SLP_ENx registers, 表 7-35 contains more information on SLP_ENx registers. See 図 7-8 for timing diagram details.

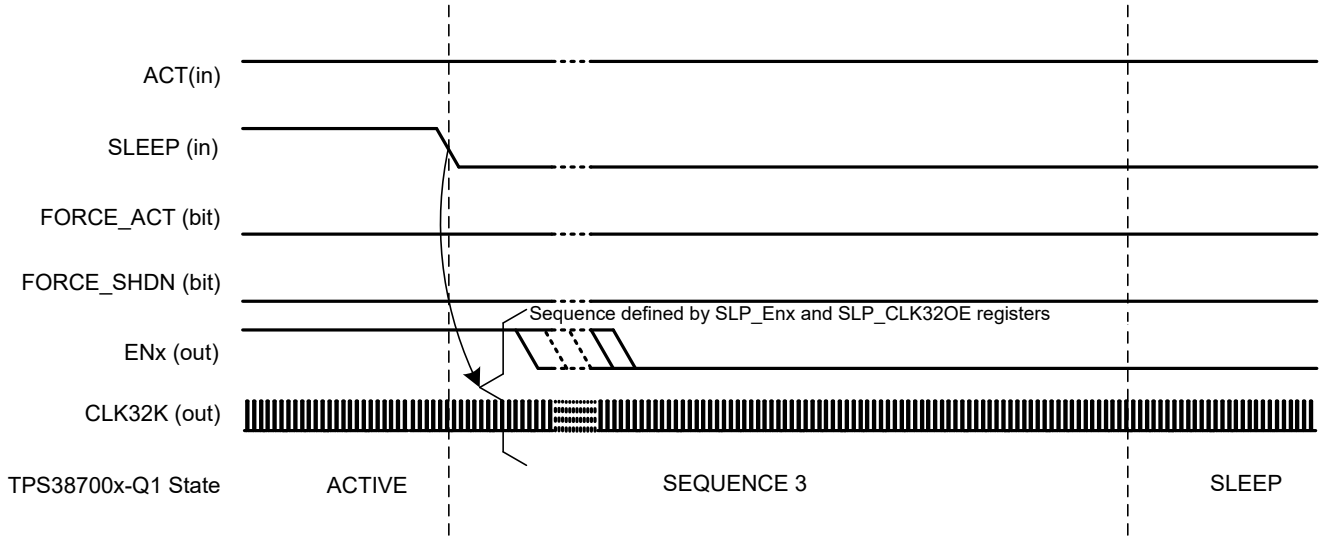


図 7-8. Sleep Entry

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7.3.6.4 Sequence 4: Sleep Exit

Sleep exit is controlled by $\overline{\text{SLEEP}}$ going high or by FORCE_ACT being set to 1 by an RTC alarm. This triggers the ENx pins to assert as per the configuration in SLP_ENx registers, consult 表 7-35 for more information on SLP_ENx registers.

In case of RTC alarm wake, the host sees the interrupt and asserts $\overline{\text{SLEEP}}$ and clear FORCE_ACT. See 図 7-9, 図 7-10, and 図 7-11 for signal details.

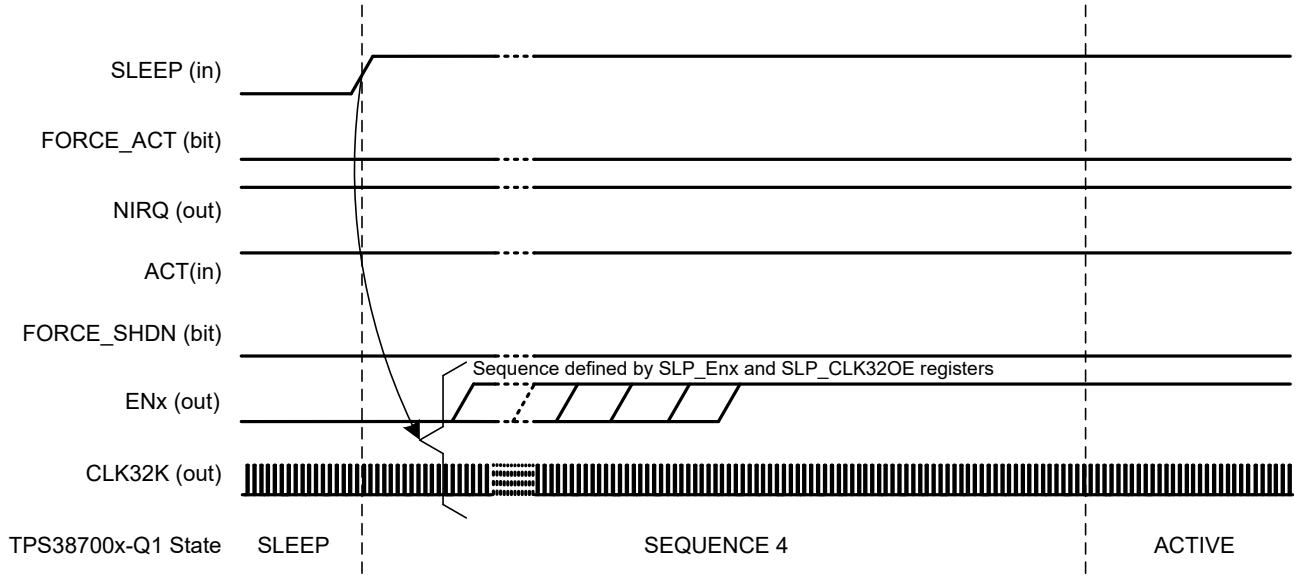


図 7-9. Sleep Exit $\overline{\text{SLEEP}}$ Triggered

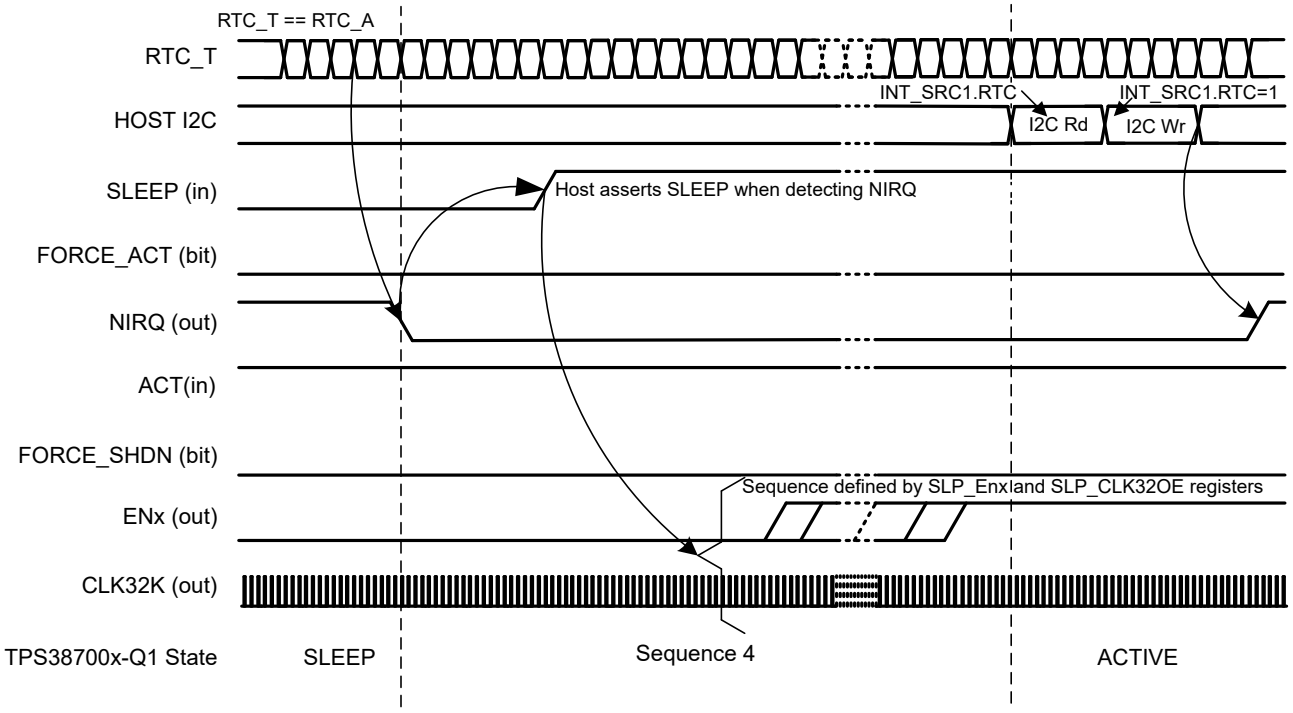


図 7-10. Sleep Exit RTC Triggered - $\overline{\text{SLEEP}}$ Sequencing

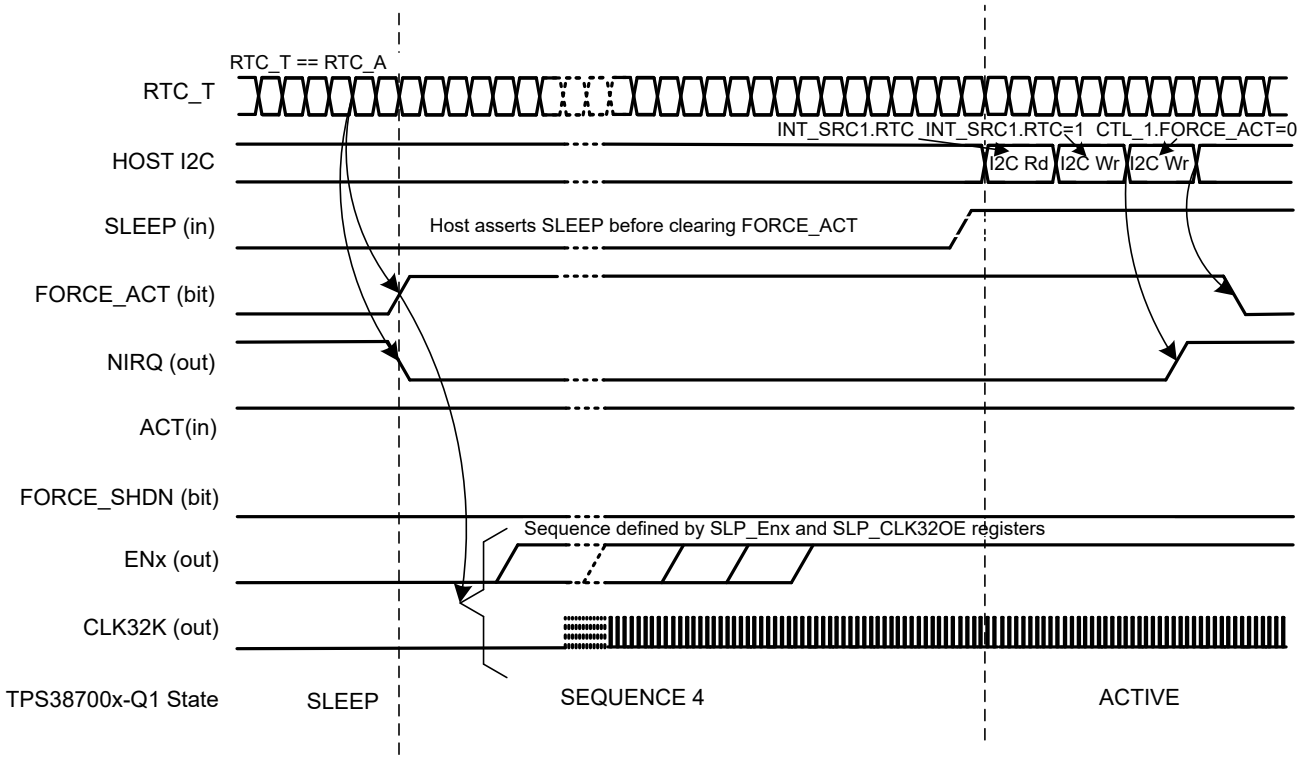


図 7-11. Sleep Exit RTC Triggered - Autonomous Sequencing

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7.3.6.5 Sequence 5 & 6: Power Down from Active and Sleep States

The power-down sequence can be triggered as depicted in 図 7-12. In all cases, NRST is asserted in the first sequencing slot, while ENx are de-asserted as per the configuration in PWR_ENx registers, see 表 7-33. In case of NPWR_BTN enabled, the "t long press" is determined as per register LP_TTSHLD shown in 表 7-23.

Power-down from sleep differs from power-down from active as some ENx can be already de-asserted as part of the sleep entry sequence. In the power-down from sleep sequence, the remaining ENx are de-asserted as per the configuration in PWR_ENx registers.

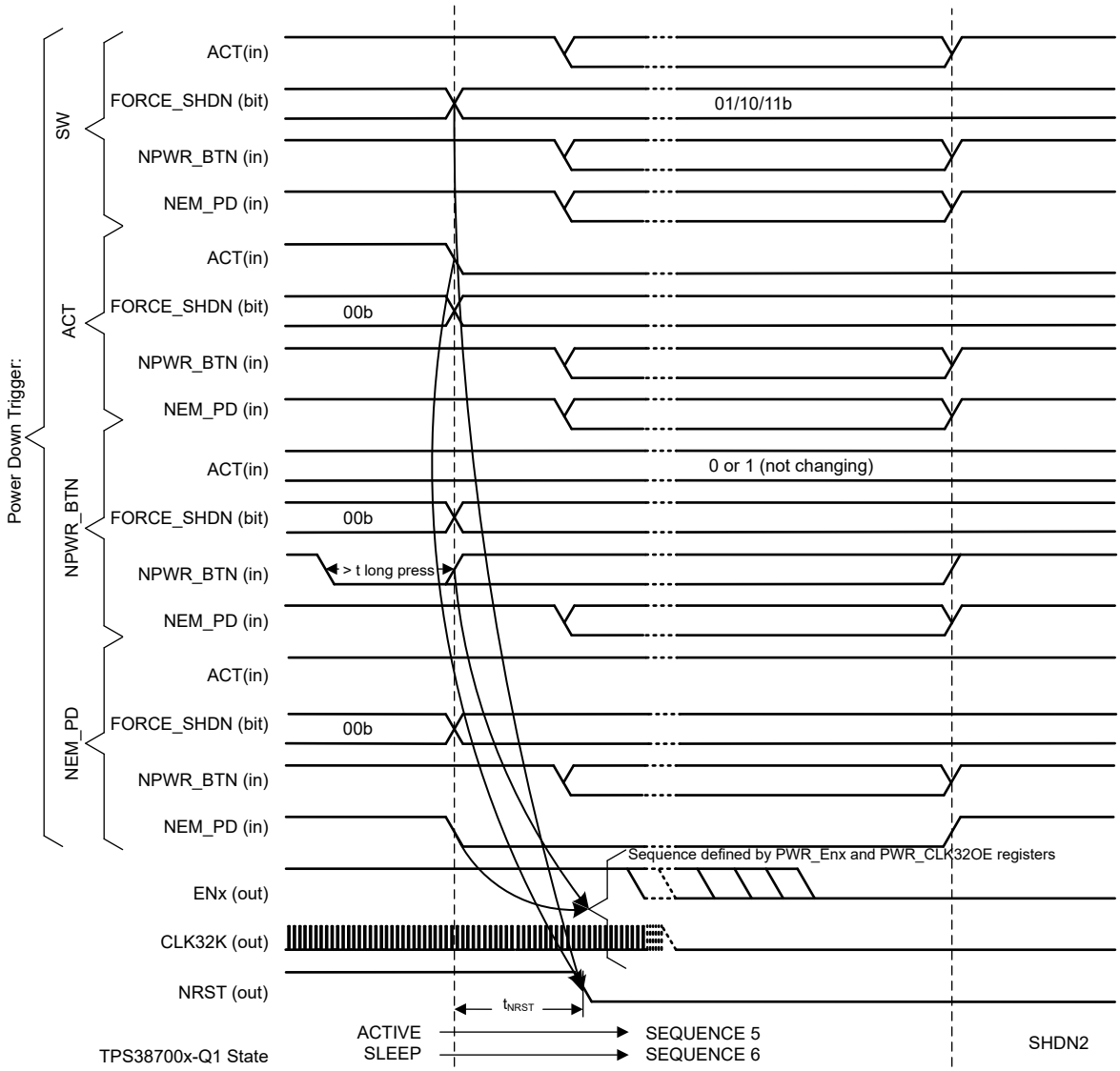


図 7-12. Power Down from Active and Sleep

7.3.6.6 Sequence 7: Sleep Exit Due to NRST_IN

If NRST_IN pin is enabled, assertion is possible while TPS38700-Q1 is in SLEEP state. To aid in proper power state synchronization with the rest of the system, TPS38700-Q1 asserts NRST while executing the Sleep exit sequence. The NRST signal is de-asserted when both RST_DLY delay time has passed since last ENx, and the NRST_IN signal is de-asserted (or the connected button is released).

Note that although not depicted in the TPS38700-Q1 State Diagram, 図 7-2, for clarity, this sequence applies also in case of WDT-initiated reset.

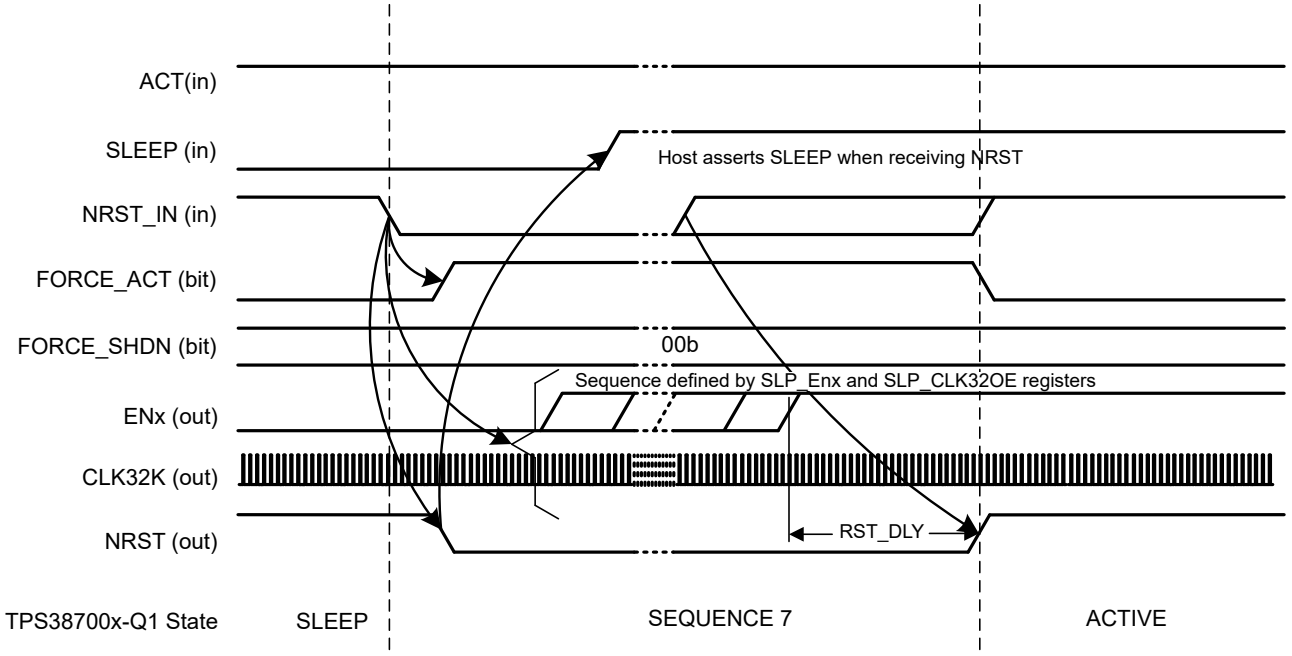


図 7-13. Sleep Exit due to NRST_IN

7.3.6.7 Sequence 8: RESET Due to NRST_IN

Note that although not depicted in the TPS38700-Q1 State Diagram,図 7-2, for clarity, this sequence applies also in case of WDT-initiated reset.

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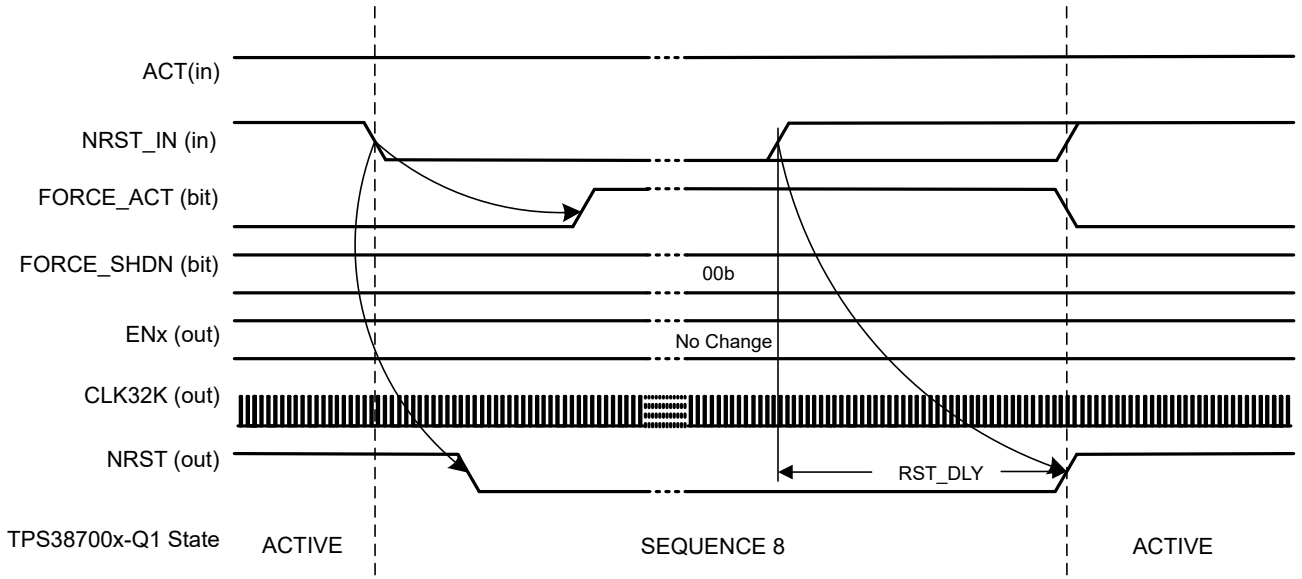


図 7-14. RESET due to NRST_IN

7.3.6.8 Sequence 9: Failsafe Power Down

F_TSD and F_LDO faults causes the TPS38700-Q1 to move to FAILSAFE State. The transition to FAILSAFE State is essentially the same as Sequence 2, with the trigger being the fault instead of the loss of VDD. A best effort approach is taken to assert NRST before pulling ENx, CLK32K, and NIRQ down.

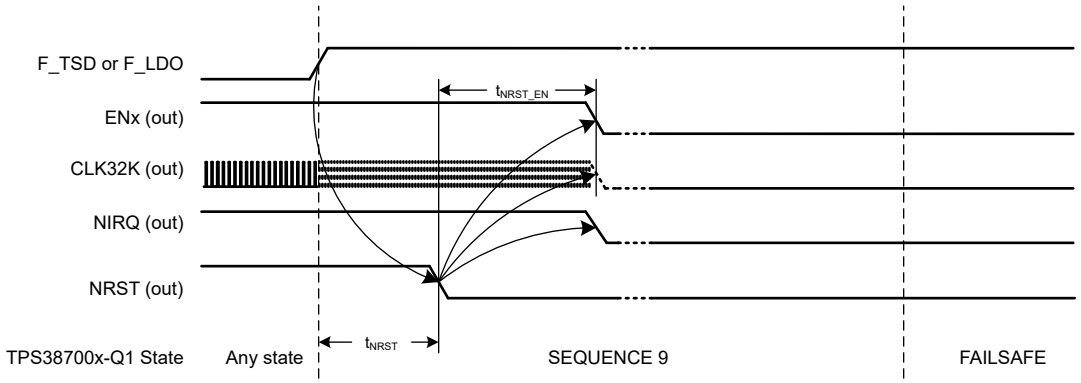


図 7-15. Failsafe Power Down

7.3.6.9 Output Sequencing

Output sequencing can be triggered by hardware or software through ACT, $\overline{\text{SLEEP}}$, RTC wake, FORCE_SHDN, NPWR_BTN (if enabled), NEM_PD (if enabled), and NRST_IN (if enabled).

Such events start sequencing the outputs (ENx and CLK32K) according to the settings in registers 表 7-29, 表 7-32, 表 7-33, 表 7-34, 表 7-35, and 表 7-36.

In those registers, Slot 1 is the earliest slot that can be selected and indicates that the ENx (or CLK32K) toggles in the first time slot after the triggering event. The example timing diagram in 図 7-16 shows the time delays specified in セクション 6.6 .

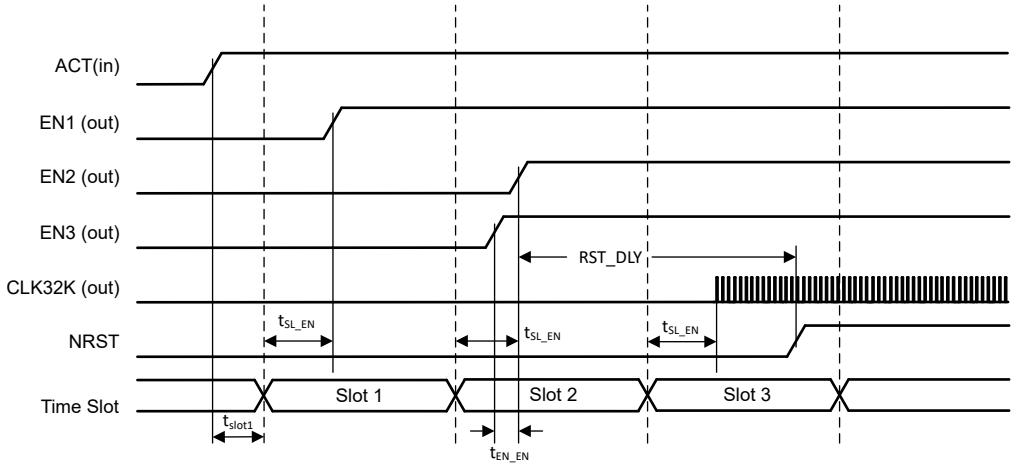


図 7-16. Output Sequencing Example

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7.3.7 I²C

Refer to 表 7-1 for the I²C register map overview. Note that "PSEQ" refers to TPS38700-Q1 and is used enhance table readability.

表 7-1. I²C Register Categories and Associated Details

TYPE	BITS	DESCRIPTION	RANGE / FUNCTION OR STATUS	WHO TOGGLES THEM?	WHO ELSE CAN WRITE TO THEM?	WHAT GETS AFFECTED DUE TO THIS BIT?
OTP bits R	VENDORID[7:0]	TI defined	TI defined	OTP option	None	None
	MODEL_REV[7:0]	TI defined	TI defined	OTP option	None	None
	TARGET_ID[7:0]	TI defined	TI defined	OTP option	None	I²C
Interrupt info bits RW1C	F_INTERR	Internal fault	No internal fault / Internal fault detected	Interrupt	Any of the interrupts generated; Can be cleared by writing 1	NIRQ
	EM_PD (1)	Emergency Power down	No emergency PD / shutdown caused by emergency PD	PSEQ	PSEQ; SOC	NRST; NIRQ
	WDT	Watchdog violation	Did not occur / occurred	Watchdog	WD; SOC	NIRQ; NRST (depends on if set in configuration register)
	F_PEC	Packet Error checking (PEC)	PEC error did not occur / occurred	I²C	I²C; SOC	NIRQ
	RTC	RTC alarm	has not triggered / triggered	RTC	RTC; SOC	NIRQ
	F_EN	Enable output pin fault	No faults detected / fault detected	EN readback-PSEQ	PSEQ; SOC	NIRQ; NRST
	F_OSC	Crystal oscillator fault	No faults detected / fault detected	Frequency detector	Frequency detector; SOC	NIRQ
	F_NRSTIRQ	Reset or Interrupt pin fault	No faults detected / fault detected	Reset readback-PSEQ	PSEQ; SOC	NIRQ
	F_BIST	Built-In self test fault	No faults detected / fault detected	BIST	BIST; SOC	NIRQ; NRST
	F_LDO	LDO fault	No faults detected / fault detected	BIST	BIST; SOC	NIRQ; NRST
	F_TSD	Thermal shutdown fault	No faults detected / fault detected	TSD	TSD; SOC	NIRQ; NRST
	F_RT_CRC	Runtime CRC register fault	No faults detected / fault detected	CRC	SOC	NIRQ
	F_ECC_DED	ECC double error deduction on OTP load	No ECC DED / ECC DED on OTP load	NVM_ECC; REG_CRC	NVM_ECC; REG_CRC; SOC	NIRQ; NRST
	F_PBSB (1)	NPWR_BTN short press	No short pulse / short pulse	PSEQ	PSEQ; SOC	NRST; NIRQ

表 7-1. I²C Register Categories and Associated Details (続き)

TYPE	BITS	DESCRIPTION	RANGE / FUNCTION OR STATUS	WHO TOGGLES THEM?	WHO ELSE CAN WRITE TO THEM?	WHAT GETS AFFECTED DUE TO THIS BIT?
Status bits R	ST_NIRQ	Current state of NIRQ output	NIRQ asserted / not asserted	Interrupt	None	None
	ST_NRST	Current state of NRST output	NRST asserted / not asserted	Interrupt; NRST state change	None	None
	ST_ACTSLP	Current state of $\overline{\text{SLEEP}}$ input	$\overline{\text{SLEEP}}$ pin driven Low or High	PSEQ	None	None
	ST_ACTSHDN	Current state of ACT input	ACT pin driven Low or High	PSEQ	None	None
	ST_PSEQ[1:0]	Current state of PSEQ	SHDNx, Power Up, Power Down, Sleep, Sleep entry, Sleep exit, invalid, Active	PSEQ	None	None
	STDR1	Current drive state of EN12 to EN9	Sequencer is driving EN Low or High	PSEQ	None	None
	STDR2	Current drive state of EN8 to EN1	Sequencer is driving EN Low or High	PSEQ	None	None
	OPEN	Watchdog Open Window	Watchdog update Window closed / open	WD	None	None
	WDUV	Watchdog Update Violation	No violation / WD updated too early	WD	None	None
	WDEXP	Watchdog close timer expired	WDT not expired / expired	WD	None	None
	BIST_C	BIST state	BIST not complete or executed / BIST complete	BIST	None	None
	ECC_SEC	Status of ECC single error correction	No error correction applied / SEC applied	NVM_ECC	None	None
	BIST_VM	Status of volatile memory test output from BIST	Volatile memory test pass / fail	REG_CRC	None	None
	BIST_NVM	Status of non-volatile memory test output from BIST	Non-Volatile memory test pass / fail	OTP covered	None	None
	BIST_L	Status of Logic test output from BIST	Logic test pass / fail	BIST	None	NIRQ/ NRST
	BIST_A	Status of Analog test ouput from BIST	Analog test pass / fail	BIST	None	NIRQ/ NRST
OTP bits R	EN_AF[12:9]	Enable AF for EN12, EN11, EN10, EN9	Disabled/ Enabled	OTP option	None	PSEQ
	AFIO[12:9]	Select AF for EN12, EN11, EN10, EN9	GPO or NPWR_BTN / NRST_IN/ NEM_PD	OTP option	None	PSEQ
	PP_EN[12:1]	ENx pin driver configuration	Open drain/ Push-Pull	OTP option	None	IO
	XTAL_LOAD	Crystal oscillator load capacitance	External/ Internal	OTP option	None	XTAL
	XTAL_EN	Crystal oscillator Enable	Crystal driver disabled/ enabled	OTP option	None	XTAL
	PP_CLK32K	CLK32K pin driver configuration	Open drain/ Push-Pull	OTP option	None	XTAL

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表 7-1. I²C Register Categories and Associated Details (続き)

TYPE	BITS	DESCRIPTION	RANGE / FUNCTION OR STATUS	WHO TOGGLES THEM?	WHO ELSE CAN WRITE TO THEM?	WHAT GETS AFFECTED DUE TO THIS BIT?
CONTROL R/W	GPIO[12:9]	General purpose input / outputs	Open drain / Push-Pull	SOC	None	PSEQ
	Debounce[3:0]	Debounce value for AF input pins	5ms to 80ms	SOC	None	PSEQ
	EN_DEB[12:9]	Enable debounce for AF input pins	Debounce disabled / enabled	SOC	None	PSEQ
	LP_TIME_TSHLD[7:0]	NPWR_BTN long press time threshold	100ms to 25.6s	SOC	None	PSEQ
	RELOAD	Reload OTP	Reload or do not Reload when SEQ5 / 6 is complete	SOC	SOC	OTP Register
	FORCE_INT	Force NIRQ low	NIRQ controlled by faults / register	SOC	SOC	NRST
	FORCE_ACT	Force PSEQ Active state	SLEEP pin controls exit / entry or is ignored	PSEQ	SOC can clear the bit; but not set the bit	PSEQ
	FORCE_SHDN[1:0]	Force PSEQ Shutdown state	ACT pin control or Force SHDN and resume ACT pin control after delay	SOC	SOC; WDT	PSEQ
	RST_DLY[3:0]	Reset Delay	0.1ms to 128ms	SOC	None	PSEQ
	RTC_WAKE	Autonomous wake alarm enable	Disabled / Enabled	SOC	None	RTC
	RTC_PU	Autonomous RTC power up from SHDN2 to ACTIVE	Disabled / Enabled	SOC	None	RTC
	REQ_PEC	Require PEC byte (if EN_PEC = 1)	Missing PEC is treated as good / bad	SOC	None	I2C
	EN_PEC	Packet Error checking (PEC)	PEC disabled / enabled	SOC	None	I2C
	AT_POR	Run BIST at POR	Skip / run BIST at POR	SOC	None	BIST
	AT_SHDN	Run BIST when exiting SEQ5 / 6	Default to not run BIST	SOC	None	BIST
PSEQ	USLOT[3:0]	Power Up / Sleep Exit time slots	125µs / 2.5s	SOC	None	PSEQ
	DSLOT[3:0]	Power down / Sleep Entry time slots	125µs / 2.5s	SOC	None	PSEQ
	SSTEP	Slot step multiplier	250µs / 1000µs	SOC	None	PSEQ
	PU[3:0][12:1]	Power Up Sequence	ENx not mapped / ENx mapped	SOC	None	PSEQ
	PD[3:0][12:1]	Power Down Sequence	ENx not mapped / ENx mapped	SOC	None	PSEQ
	SLP_EXT[3:0][12:1]	Sleep Exit Sequence	ENx not mapped / ENx mapped	SOC	None	PSEQ
	SLP_ENTRY[3:0] [12:1]	Sleep Entry Sequence	ENx not mapped / ENx mapped	SOC	None	PSEQ
RTC (2)	RTC_T[31:0]	RTC time setting	1sec to 136years	XTAL; internal oscillator	None	RTC
	RTC_A[31:0]	RTC alarm setting	1sec to 136years	SOC	None	RTC

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表 7-1. I²C Register Categories and Associated Details (続き)

TYPE	BITS	DESCRIPTION	RANGE / FUNCTION OR STATUS	WHO TOGGLES THEM?	WHO ELSE CAN WRITE TO THEM?	WHAT GETS AFFECTED DUE TO THIS BIT?
WDT	WDT_EN[1:0]	Watchdog configuration	Disabled / Enabled	SOC	None	WDT
	SLP_EN	Automatic disable in Sleep mode	Watchdog disabled / enabled in Sleep	SOC	None	WDT
	WDT_DLY[2:0]	Delay in number of Watchdog periods	1 or 8 WDT period	SOC	None	WDT
	PDMD[1:0]	Power down mode for WDT force power down	Value written to CTL_1.FORCE_SHDN on WDT power down	SOC	None	PSEQ
	CLOSE[7:0]	WDT close window configuration	1ms to 864ms	SOC	None	WDT
	OPEN[7:0]	WDT open window configuration	1ms to 864ms	SOC	None	WDT
	KEY[7:0]	WDT key to reset	0 / 1	SOC	None	WDT
PROT	WRK	Work set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	SEQS	SEQS set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	SEQP	SEQP set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	SEQC	SEQC set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	WDT	WDT set register lock	0 / 1	SOC only 1	None	Write function to those reg groups
	RTC	RTC set register lock	0 / 1	SOC only 1	None	Write function to those reg groups
	CTL	CTL set register lock	0 / 1	SOC only 1	None	Write function to those reg groups

(1) Presence of fault reporting functionality dependent on part configuration.
(2) Register RTC_T must be written to before writing a value in register RTC_A.

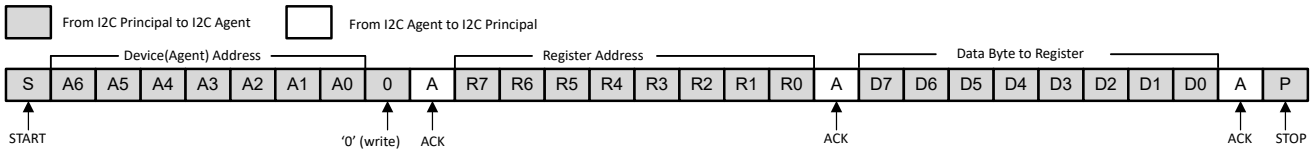


図 7-17. I2C Single Byte Write

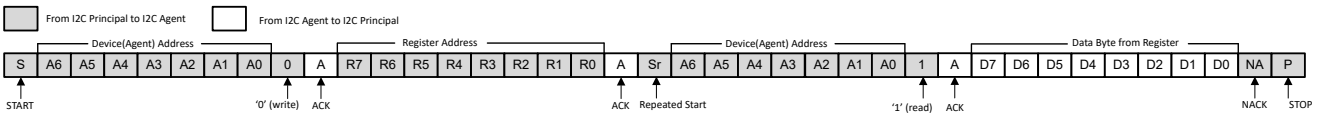


図 7-18. I2C Single Byte Read

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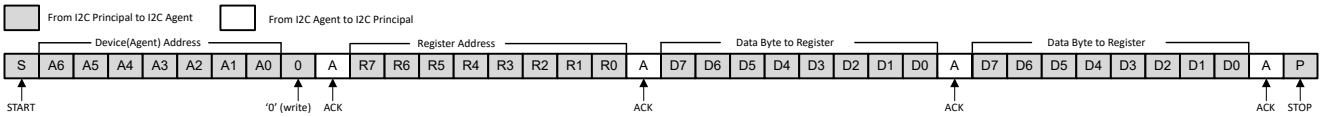


図 7-19. I2C Sequential Write

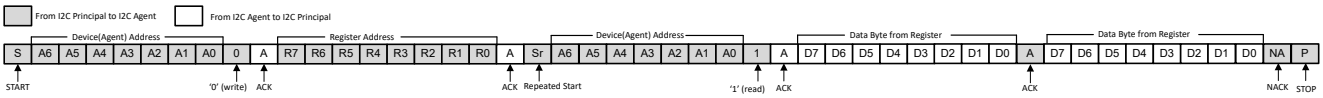


図 7-20. I2C Sequential Read

7.3.7.1 Packet Error Checking (PEC)

TPS38700-Q1 supports Packet Error Checking (PEC) as a way to implement Cyclic Redundancy Checking (CRC). PEC is a dynamic CRC that happens only during read or write transactions if enabled. With the initial value of CRC set to 0x00, the PEC uses a CRC-8 represented by the polynomial:

$$C(x) = x^8 + x^2 + x + 1 \quad (1)$$

The polynomial is meant to catch any bit flips or noise in I2C communication which cause data and PEC byte to have a mismatch. The PEC calculation includes all bytes in the transmission, including address, command and data. The PEC calculation does not include ACK or NACK bits or START, STOP or REPEATED START conditions. If PEC is enabled, and the TPS38700-Q1 is transmitting data, then the TPS38700-Q1 is responsible for sending the PEC byte. If PEC is enabled, and the TPS38700-Q1 is receiving data from the MCU, then the MCU is responsible for sending the PEC byte. In case of faster communications needs like servicing the watchdog the required PEC feature can be effectively used to handle missing PEC information and to avoid triggering faults. 図 7-21 and 図 7-22 highlight the communication protocol flow when PEC is required and which device controls SDA line at various instances during active communication.

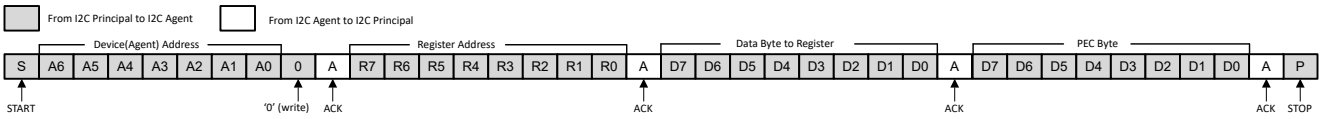


図 7-21. Single Byte Write with PEC

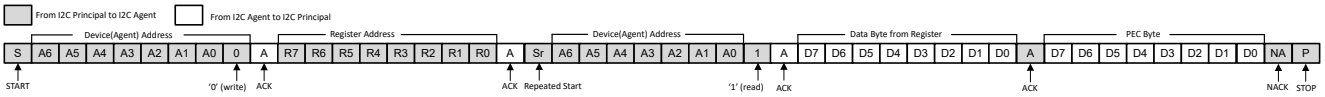


図 7-22. Single Byte Read with PEC

表 7-2 explains the registers associated with a PEC Write command and resulting device behavior. 表 7-3 explains the registers associated with a PEC Read command and resulting device behavior.

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表 7-2. PEC Write Summary

EN_PEC	REQ_PEC	PEC_INT	Interrupt Status
0	x	x	PEC byte is not required in write operation, NO NIRQ assertion.
1	0	x	A write command missing a PEC byte is treated as OK, the write command executes and results in a I2C ACT. A write command with an incorrect PEC is treated as an error, the write command does not execute and results in a I2C NACK. NO NIRQ assertion.
1	1	0	A missing PEC is treated as an error, a write command only executes if the correct PEC byte is provided. I2C communication still responds with an ACT although write command did not execute. A write command with an incorrect PEC is treated as an error, the write command does not execute and result in a I2C NACK. NO NIRQ assertion.
1	1	1	A missing PEC is treated as an error, a write command executes only if the correct PEC byte is provided. I2C communication still responds with an ACT although write command did not execute. A write command with an incorrect PEC is treated as an error, the write command does not execute and results in a I2C NACK. NIRQ is asserted when a write command with a incorrect or missing PEC byte is attempted.

表 7-3. PEC Read Summary

EN_PEC	REQ_PEC	PEC_INT	Interrupt Status
0	x	x	I2C read operation responds with data stored in register, I2C read command does not respond with registers corresponding PEC byte.
1	x	x	I2C read operation responds with data stored in register and corresponding PEC byte.

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7.4 Register Map Table

表 7-4. Register Map Table

RSVD = Reserved

ADDR	NAME	R/W	MSB	6	5	4	3	2	1	LSB	DEFAULT	GROUP
0x00 - 0x0F: Vendor info and vendor usage registers												
0x00	Model Rev	R	Device Model (Bits 3-7)					Vendor ID (Bits 0-2)				
0x01	Revision	R	Silicon_Rev		OTP_Rev							
0x02 … 0x0F	RSVD		Vendor defined or other IC information									
0x10 - 0x1F: Interrupts and Status registers												
0x10	INT_SRC1	RW1C	F_INTERNAL	EM_PD	WDT	F_PEC	RTC	F_EN	F_OSC	F_NRSTIRQ	0x00	
0x11	INT_SRC2	RW1C	F_VENDOR	RSVD	F_RT_CRC	F_BIST	F_LDO	F_TSD	F_ECC_DED	F_PBSP	0x00	
0x12	INT_VENDOR	RW1C	Vendor specific internal fault flags								0x00	
0x13	CTL_STAT	R	RSVD	ST_VBBAT	ST_NIRQ	ST_NRST	ST_ACTSLP	ST_ACTSHDN	ST_PSEQ[1:0]		0x00	
0x14	EN_STDR1	R	RSVD				STDR_EN12	STDR_EN11	STDR_EN10	STDR_EN9	0x00	
0x15	EN_STDR2	R	STDR_EN8	STDR_EN7	STDR_EN6	STDR_EN5	STDR_EN4	STDR_EN3	STDR_EN2	STDR_EN1	0x00	
0x16	EN_STRD1	R	RSVD				STRD_EN12	STRD_EN11	STRD_EN10	STRD_EN9	0x00	
0x17	EN_STRD2	R	STRD_EN8	STRD_EN7	STRD_EN6	STRD_EN5	STRD_EN4	STRD_EN3	STRD_EN2	STRD_EN1	0x00	
0x18	WDT_STAT	R	RSVD				OPEN	RSVD	WDUV	WDEXP	0x00	
0x19	TEST_STAT	R	RSVD	BIST_C	ECC_SEC	RSVD	BIST_VM	BIST_NVM	BIST_L	BIST_A	0x00	
0x1A	LAST_RST	R	NRST_IN	WDT_RST	LP_NPWR_BTN	NEM_PD	ACTSHDN	WDT_SHDN	FORCE_SHDN[1:0]		0x00	
0x1B … 0x1F	RSVD		RSVD									
0x20 - 0x2F: Configuration registers												
0x20	EN_ALT_F	R	RSVD				EN_AF12	EN_AF11	EN_AF10	EN_AF9	NVM	
0x21	AF_IN_OUT	R	RSVD				AFIO12	AFIO11	AFIO10	AFIO9	NVM	
0x22	EN_CFG1	R	RSVD				PP_EN12	PP_EN11	PP_EN10	PP_EN9	NVM	
0x23	EN_CFG2	R	PP_EN8	PP_EN7	PP_EN6	PP_EN5	PP_EN4	PP_EN3	PP_EN2	PP_EN1	NVM	
0x24	CLK_CFG	R	XTAL_LOAD	XTAL_EN	RSVD	PP_CLK32K	RSVD				NVM	
0x25	GP_OUT	R/W	GPO4	GPO3	GPO2	GPO1	GPO12	GPO11	GPO10	GPO9	NVM	WRK
0x26	DEB_IN	R/W	DEBOUNCE[3:0]				EN_DEB12	EN_DEB11	EN_DEB10	RSVD	NVM	CTL
0x27	LP_TTSHLD	R/W	LP_TIME_TSHLD[7:0]								NVM	CTL

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表 7-4. Register Map Table (続き)

RSVD = Reserved

ADDR	NAME	R/W	MSB	6	5	4	3	2	1	LSB	DEFAULT	GROUP
0x28	CTL_1	R/W	RSVD				FORCE_INT	FORCE_ACT	FORCE_SHDN[1:0]		NVM	WRK
0x29	CTL_2	R/W	RST_DLY[3:0]				RTC_WAKE	RTC_PU	REQ_PEC	EN_PEC	NVM	CTL
0x2A	TEST_CFG	R/W	RSVD					AT_SHDN	AT_POR[1:0]		NCM	CTL
0x2B	IEN_VENDOR	R/W	Vendor specifc internal fault enables								NVM	CTL
0x2C … 0x2F	RSVD		RSVD									
0x30 - 0x6F: Sequencing registers												
0x30	SEQ_CFG	R/W	GPO8	GPO7	GPO6	GPO5	RSVD	RSVD	RSVD	SSTEP	NVM	SEQC
0x31	SEQ_USLOT	R/W	TIME[7:0]								NVM	SEQC
0x32	SEQ_DSLOT	R/W	TIME[7:0]								NVM	SEQC
0x33	PWR_EN1	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x34	PWR_EN2	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x35	PWR_EN3	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x36	PWR_EN4	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x37	PWR_EN5	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x38	PWR_EN6	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x39	PWR_EN7	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x3A	PWR_EN8	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x3B	PWR_EN9	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x3C	PWR_EN10	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x3D	PWR_EN11	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x3E	PWR_EN12	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x3F	PWR_CLK32OE	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x40 … 0x4F	RSVD		RSVD									
0x50 … 0x52	RSVD		RSVD									
0x53	SLP_EN1	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x54	SLP_EN2	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x55	SLP_EN3	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x56	SLP_EN4	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x57	SLP_EN5	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS

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表 7-4. Register Map Table (続き)

RSVD = Reserved

ADDR	NAME	R/W	MSB	6	5	4	3	2	1	LSB	DEFAULT	GROUP
0x58	SLP_EN6	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x59	SLP_EN7	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x5A	SLP_EN8	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x5B	SLP_EN9	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x5C	SLP_EN10	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x5D	SLP_EN11	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x5E	SLP_EN12	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x5F	SLP_CLK32OE	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				NVM	SEQS
0x60 … 0x6F	RSVD		RSVD									
0x70 - 0x7F: Real Time Clock (RTC) registers												
0x70	RTC_T3	R/W	RTC_T[31:24]								0x00	RTC
0x71	RTC_T2	R/W	RTC_T[23:16]								0x00	RTC
0x72	RTC_T1	R/W	RTC_T[15:8]								0x00	RTC
0x73	RTC_T0	R/W	RTC_T[7:0]								0x00	RTC
0x74	RTC_A3	R/W	RTC_A[31:24]								0xFF	RTC
0x75	RTC_A2	R/W	RTC_A[23:16]								0xFF	RTC
0x76	RTC_A1	R/W	RTC_A[15:8]								0xFF	RTC
0x77	RTC_A0	R/W	RTC_A[7:0]								0xFF	RTC
0x78 … 0x7F	RSVD		RSVD									
0x80 - 0x8F: Watchdog Timer (WDT) registers												
0x80	WDT_CFG	R/W	WDTEN[1:0]		SLP_EN		WDTDLY[2:0]		PDMD[1:0]		0x00	WDT
0x81	WDT_CLOSE	R/W	CLOSE[7:0]								0x00	WDT
0x82	WDT_OPEN	R/W	OPEN[7:0]								0x00	WDT
0x83	WDTKEY	R/W	KEY[7:0]								0x00	None
0x84 … 0x8F	RSVD		RSVD									
0x90 … 0xEF	Unused		Unused									
0xF0 - 0xFF: Protection registers												
0xF0	PROT1	R/W	RSVD	WRK	SEQS	SEQP	SEQC	WDT	RTC	CTL	0x00	

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表 7-4. Register Map Table (続き)

RSVD = Reserved

ADDR	NAME	R/W	MSB	6	5	4	3	2	1	LSB	DEFAULT	GROUP
0xF1	PROT2	R/W	RSVD	WRK	SEQS	SEQP	SEQC	WDT	RTC	CTL	0x00	
0xF2 … 0xF8	RSVD		RSVD									
0xF9	I2CADDR	R	RSVD	ADDR_NVM[6:0]							NVM	
0xFA	DEV_CFG	R	RSVD						SOC_IF[1:0]		NVM	
0xFB … 0xFF	RSVD		RSVD									

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7.4.1 Register Descriptions

表 7-5. INT_SRC1

Address: 0x10

Description: Interrupt Source register. If F_INTERNAL, then INT_SRC2 register provides further information.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	F_INTERNAL	Internal Fault (ORed value of all bits in INT_SRC2): 0 = No internal fault detected 1 = Internal fault detected. Further detail flagged in INT_SRC2. This bit is cleared by clearing the bits in INT_SRC2.
6	EM_PD	Emergency Power Down: 0 = No emergency power-down event 1 = Shutdown caused by emergency power-down (Sequence 2). Write-1-to-clear clears the bit. The bit is set again on next emergency power-down.
5	WDT	0 = WDT violation did not occur (or WDT_CFG.WDTEN[1:0] = 00b). 1 = WDT violation occurred. This bit is valid only if WDT_CFG.WDTEN[1:0] is enabled. Write-1-to-clear clears the bit. The bit is set again on next WDT violation.
4	PEC	Packet Error Checking: 0 = PEC miscompare has not occurred (or CTL_2.EN_PEC = 0). 1 = PEC miscompare has occurred. This bit is valid only if CTL_2.EN_PEC is enabled. Write-1-to-clear clears the bit. The bit is set again on next PEC miscompare.
3	RTC	0 = RTC alarm has not triggered (or alarm function is disabled). 1 = RTC alarm has triggered. This bit is invalid if the alarm function is disabled (CTL_2.RTC_WAKE and CTL_2.RTC_PU are both clear, and RTC_A[31:0] is set to 0xFFFFFFFF.) Write-1-to-clear clears the bit. The bit is set again on next RTC alarm.
2	F_EN	Enable Output Pin Fault: 0 = No short to supply or ground detected. 1 = Short to supply or ground detected. Write-1-to-clear clears the bit only if the fault condition is also removed.
1	F_OSC	Crystal Oscillator Fault: 0 = No fault detected on Crystal Oscillator (or CLK_CFG.XTAL_EN = 0, disabled). 1 = Fault detected on Crystal Oscillator. Write-1-to-clear clears the bit only if the fault condition is also removed.
0	F_NRSTIRQ	Reset or Interrupt Pin Fault: 0 = No fault detected on NRST or NIRQ. 1 = Low resistance path to supply detected on either NRST or NIRQ. Write-1-to-clear clears the bit only if the fault condition is also removed.

INT_SRC1 represents the reason that NIRQ was asserted. When the host processor receives NIRQ, the host reads this register to quickly determine the source of the interrupt. If this register is clear, then TPS38700-Q1 did not assert NIRQ.

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表 7-6. INT_SRC2

Address: 0x11

Description: Interrupt Source register for internal errors.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	F_VENDOR	Vendor specific internal fault. Details reported in INT_VENDOR. This bit represents the ORed value of all bits in INT_VENDOR. 0 = No fault reported in INT_VENDOR 1 = Fault reported in INT_VENDOR This bit is cleared by clearing the bits in INT_VENDOR.
6	RSVD	Reserved
5	F_RT_CRC	Runtime register CRC Fault: 0 = No fault detected. 1 = Register CRC fault detected. Write-1-to-clear clears the bit. The bit is set again during next register CRC check if a fault is detected.
4	F_BIST	Built-In Self Test Fault: 0 = No fault detected. 1 = BIST fault detected. Note that clearing this bit does not clear the results in TEST_STAT register. Write-1-to-clear clears the bit. The bit is set again during next BIST execution if a fault is detected.
3	F_LDO	LDO Fault: 0 = No LDO fault detected. 1 = LDO fault detected. If internal LDO is used, this flag is to indicate fault. If internal LDO is not used, this flag must be reserved. Write-1-to-clear clears the bit only if the fault condition is also removed.
2	F_TSD	Thermal Shutdown: 0 = No thermal shutdown. 1 = Thermal shutdown occurred since last read. Write-1-to-clear clears the bit only if the fault condition is also removed.
1	F_ECC_DED	ECC Double-Error Detection on OTP configuration load: 0 = No ECC-DED on OTP load. 1 = ECC-DED on OTP load. Write-1-to-clear clears the bit. The bit is set again during next OTP configuration load if a fault is detected.
0	F_PBSP	NPWR_BTN Short Pulse: 0 = No short pulse on NPWR_BTN (or NPWR_BTN is not enabled). 1 = Short pulse detected on NPWR_BTN. This bit is valid only if NPWR_BTN is enabled through EN_AF12 and AFIO12 bits. Write-1-to-clear clears the bit. The bit is set again during next short pulse detected on NPWR_BTN.

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表 7-7. INT_VENDOR

Address: 0x12

Description: Vendor Specific Internal Interrupt Status register.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	FAULTS[7:0]	Vendor specific internal faults flags.

表 7-8. CTL_STAT

Address: 0x13

Description: TPS38700-Q1 Status register for control pins and internal state.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:6	RSVD	Reserved
5	ST_NIRQ	Current state of NIRQ Output: 0 = NIRQ pin asserted low by TPS38700-Q1. 1 = NIRQ pin not asserted low by TPS38700-Q1.
4	ST_NRST	Current state of NRST Output: 0 = NRST pin asserted low by TPS38700-Q1. 1 = NRST pin not asserted low by TPS38700-Q1.
3	ST_ACTSLP	Current state of $\overline{\text{SLEEP}}$ input: 0 = $\overline{\text{SLEEP}}$ pin driven low (Sleep) by system. 1 = $\overline{\text{SLEEP}}$ pin driven high (Active) by system.
2	ST_ACTSHDN	Current state of ACT input: 0 = ACT pin driven low (Shutdown) by system. 1 = ACT pin driven high (Active) by system.
1:0	ST_PSEQ[1:0]	00b: SHDNx, Power Up, Power Down 01b: SLEEP, Sleep Entry, Sleep Exit 10b: Invalid combination 11b: ACTIVE

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表 7-9. EN_STDR1

Address: 0x14

Description: Current drive status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3:0	STDR_EN[12:9]	Current drive state of EN[X]: 0 = TPS38700-Q1 is driving EN[X] Low. 1 = TPS38700-Q1 is driving or allowing to float EN[X] High

表 7-10. EN_STDR2

Address: 0x15

Description: Current drive status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	STDR_EN[8:1]	Current drive state of EN[X]: 0 = TPS38700-Q1 is driving EN[X] Low. 1 = TPS38700-Q1 is driving or allowing to float EN[X] High

表 7-11. EN_STRD1

Address: 0x16

Description: Current read status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3:0	STRD_EN[12:9]	Current read state of EN[X]: 0 = TPS38700-Q1 is reading EN[X] Low. 1 = TPS38700-Q1 is reading EN[X] High

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表 7-12. EN_STRD2

Address: 0x17

Description: Current read status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	STRD_EN[8:1]	Current read state of EN[X]: 0 = TPS38700-Q1 is reading EN[X] Low. 1 = TPS38700-Q1 is reading EN[X] High

表 7-13. WDT_STAT

Address: 0x18

Description: WDT status register.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3	OPEN	Watchdog Open Window: 0 = Watchdog update window closed. 1 = Watchdog update window open.
2	RSVD	Reserved
1	WDUV	Watchdog Update Violation. Clear on read. 0 = No violation detected. 1 = Watchdog updated too early.
0	WDEXP	Watchdog close timer expired without update to WDKEY. Clear on read. 0 = WDT Not Expired. 1 = WDT Expired.

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表 7-14. TEST_STAT

Address: 0x19

Description: Internal Self-Test and ECC status register.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	RSVD	Reserved
6	BIST_C	BIST state: 0 = BIST running or not executed since last POR. Check also TEST_CFG register. 1 = BIST complete.
5	ECC_SEC	Status of ECC Single-Error Correction on OTP configuration load. 0 = no error correction applied. 1 = Single-Error Correction applied.
4	RSVD	Reserved
3	BIST_VM	Status of Volatile Memory test output from BIST. 0 = Volatile Memory test pass. 1 = Volatile Memory test fail.
2	BIST_NVM	Status of Non-Volatile Memory test output from BIST. 0 = Non-Volatile Memory test pass. 1 = Non-Volatile Memory test fail.
1	BIST_L	Status of Logic test output from BIST. 0 = Logic test pass. 1 = Logic test fail.
0	BIST_A	Status of Analog test output from BIST. 0 = Analog test pass. 1 = Analog test fail.

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表 7-15. LAST_RST

Address: 0x1A

Description: Reason of last NRST assertion or shutdown. NRST assertion and shutdown occur in Sequence 2, Sequence 5, Sequence 6, Sequence 7, and Sequence 8.

The register is maintained as long as VDD and/or VBBAT is present. An emergency shutdown triggering Sequence 2 is already recorded in INT_SRC1.EM_PD register bit, so is not stored in this register. The host is expected to read this register as part of the first actions taken upon power ON.

The register is overwritten with new relevant data on next NRST assertion or shutdown.

POR Value: 0x00

Access: Read Only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	NRST_IN	NRST assertion due to NRST_IN (if enabled in EN_ALT_F and AF_IN_OUT registers). 0 = Last NRST assertion was not due to NRST_IN. 1 = Last NRST assertion was due to NRST_IN.
6	WDT_RST	NRST assertion due to WDT (see also 表 7-39). 0 = Last NSRT assertion was not due to WDT. 1 = Last NSRT assertion was due to WDT.
5	RSVD	Reserved
4	NEM_PD	NRST/Shutdown due to NEM_PD (if enabled in EN_ALT_F and AF_IN_OUT registers). 0 = Last NRST/Shutdown assertion was not due to NEM_PD. 1 = Last NRST/Shutdown assertion was due to NEM_PD.
3	ACTSHDN	NRST/Shutdown due to ACT asserted Low (shutdown). 0 = Last NRST/Shutdown assertion was not due to ACT Low. 1 = Last NRST/Shutdown assertion was due to ACT Low.
2	WDT_SHDN	NRST/Shutdown due to WDT (see also 表 7-39). 0 = Last NRST/Shutdown assertion was not due to ACT/ SHDN Low. 1 = Last NRST/Shutdown assertion was due to ACT/ SHDN Low. If this bit is set, LAST_RST.FORCE_SHDN[1:0] contains WDT_CFG.PDMD[1:0] value.
1:0	FORCE_SHDN[1:0]	NRST/Shutdown due to CTL_1.FORCE_SHDN[1:0] ≠00b. Value is the same as CTL_1.FORCE_SHDN[1:0] that initiated the last NRST/Shutdown. If WDT_SHDN bit is set, this bitfield contains WDT_CFG.PDMD[1:0] value.

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表 7-16. EN_ALT_F

Address: 0x20

Description: Enable Alternate Function for sequencing pins EN[12:9] (AF is selected in AF_IN_OUT register).

POR Value: Loaded from NVM

Access: Read only once loaded from NVM

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3	EN_AF12	Enable alternate function of EN[12]: 0 = Disabled. 1 = AF Enabled (GPO12 or NPWR_BTN).
2	EN_AF11	Enable alternate function of EN[11]: 0 = Disabled. 1 = AF Enabled (GPO11 or NRST_IN).
1	EN_AF10	Enable alternate function of EN[10]: 0 = Disabled. 1 = AF Enabled (GPO10 or NEM_PD).
0	EN_AF9	Enable alternate function of EN[9]: 0 = Disabled. 1 = AF Enabled (GPO9).

The alternate function can be enabled only if the corresponding PU/ PD/ SLP_EXIT/ SLP_ENTRY registers fields are all set to 0. If any of those bit fields are non-zero, the corresponding pin is locked to EN[X] sequencing function.

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表 7-17. AF_IN_OUT

Address: 0x21

Description: Select Alternate Function for sequencing pins EN[12:9] (AF is enabled in EN_ALT_F register).

POR Value: Loaded from NVM.

Access: Read only once loaded from NVM.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3	AFIO12	Select alternate function of EN12: 0 = General Purpose Output (GPO) - GPO12. 1 = AF NPWR_BTN (power button input).
2	AFIO11	Select alternate function of EN11: 0 = GPO11. 1 = AF NRST_IN (reset input).
1	AFIO10	Select alternate function of EN10: 0 = GPO10. 1 = AF NEM_PD (emergency power-down input).
0	AFIO9	Select alternate function of EN9: 0 = GPO9. 1 = Invalid. EN9 can only be selected as GPO9 through EN_ALT_F.EN_AF9, and does not have an alternate function. Therefore, this bit is always read-only and always read 0.

表 7-18. EN_CFG1

Address: 0x22

Description: Drive mode configuration for EN[12:9]

POR Value: Loaded from NVM.

Access: Read only once loaded from NVM

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3:0	PP_EN[12:9]	ENx pin driver configuration: 0 = Open drain. 1 = Push pull.

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表 7-19. EN_CFG2

Address: 0x23

Description: Drive mode configuration for EN[8:1].

POR Value: Loaded from NVM.

Access: Read only once loaded from NVM.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	PP_EN[8:1]	ENx pin driver configuration: 0 = Open drain. 1 = Push pull.

表 7-20. CLK_CFG

Address: 0x24

Description: Oscillator configuration.

POR Value: Loaded from NVM.

Access: Read only once loaded from NVM.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	XTAL_LOAD	Crystal oscillator load capacitance: 0 = external. 1 = internal (value specified by the vendor).
6	XTAL_EN	Crystal oscillator enable: 0 = Crystal driver disabled. 1 = Crystal driver enabled.
5	RSVD	Reserved
4	PP_CLK32K	CLK32K pin driver configuration: 0 = Open drain. 1 = Push pull. Note that Push-Pull configuration for CLK32K output is optional and not a requirement.
3:0	RSVD	Reserved

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表 7-21. GP_OUT

Address: 0x25

Description: Set General Purpose Output state for sequencing pins EN[12:9]. GPO is enabled through AF_IN_OUT and EN_ALT_F registers.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	GPO4	General Purpose Output. Only used when both PWR_EN4 and SLP_EN4 are clear. 0 = GPO4 pin driven low. 1 = GPO4 pin driven high.
6	GPO3	General Purpose Output. Only used when both PWR_EN3 and SLP_EN3 are clear. 0 = GPO3 pin driven low. 1 = GPO3 pin driven high.
5	GPO2	General Purpose Output. Only used when both PWR_EN2 and SLP_EN2 are clear. 0 = GPO2 pin driven low. 1 = GPO2 pin driven high.
4	GPO1	General Purpose Output. Only used when both PWR_EN1 and SLP_EN1 are clear. 0 = GPO1 pin driven low. 1 = GPO1 pin driven high.
3	GPO12	General Purpose Output. Only used when both PWR_EN12 and SLP_EN12 are clear. 0 = GPO12 pin driven low. 1 = GPO12 pin driven high.
2	GPO11	General Purpose Output. Only used when both PWR_EN11 and SLP_EN11 are clear. 0 = GPO11 pin driven low. 1 = GPO11 pin driven high.
1	GPO10	General Purpose Output. Only used when both PWR_EN10 and SLP_EN10 are clear. 0 = GPO10 pin driven low. 1 = GPO10 pin driven high.
0	GPO9	General Purpose Output. Only used when both PWR_EN9 and SLP_EN9 are clear. 0 = GPO9 pin driven low. 1 = GPO9 pin driven high.

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表 7-22. DEB_IN

Address: 0x26

Description: Debounce configuration for AF input pins.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	DEBOUNCE[3:0]	Debounce value for AF input pins: 0000b = 5ms 0001b = 10ms 0010b = 15ms 0011b = 20ms nnnnb = 5(N+1)ms 1111b = 80ms
3:1	EN_DEB[12:10]	Enable debounce for AF input pins: 0 = debounce disabled. 1 = debounce enabled.
0	RSVD	Reserved

表 7-23. LP_TTSHLD

Address: 0x27

Description: NPWR_BTN Long Press time threshold configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	LP_TIME_TSHLD	If NPWR_BTN is enabled, this value, in 100ms increments, determines the minimum duration of the NPWR_BTN pulse to be detected as "Long Press" (shorter is detected as "Short Press") 00h = 100ms 01h = 200ms ... FEh = 25.5s FFh = 25.6s

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表 7-24. CTL_1

Address: 0x28

Description: Interrupt and State SW control.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3	FORCE_INT (1)	Force NIRQ low: 0 = NIRQ pin controlled by INT_SRCx register faults. 1 = NIRQ pin forced low.
2	FORCE_ACT (2)	Force TPS38700-Q1 active state: 0 (cleared only by I^2C writes) = $\overline{SLEEP}$ pin controls sleep entry/ exit. 1 (set only by HW) = $\overline{SLEEP}$ is ignored.
1:0	FORCE_SHDN[1:0]	Force TPS38700-Q1 to shutdown state. With NPWR_BTN disabled (EN_ALT_F.EN_AF12 = 0): 00b = Normal ACT pin control. 01b = Force power-down sequence, then resume normal ACT pin control immediately. 10b = Force power-down sequence, then resume normal ACT pin control after 1 second delay. 11b = Force power-down sequence, then resume normal ACT pin control when ACT = Low or when RTC alarm occurs as per configuration in registers CTL_2, RTC_T, and RTC_A. With NPWR_BTN enabled (EN_ALT_F.EN_AF12 = 1): 00b = Normal NPWR_BTN pin control. 01b = Force power-down sequence, then move to Sequence 1 immediately (proceed as if ACT = High). 10b = Force power-down sequence, then move to Sequence 1 after 1 second (proceed as if ACT = High). If NPWR_BTN is pressed before 1 second expires, then the TPS38700-Q1 moves to Sequence 1 at that time. 11b = Force power-down sequence, then move to Sequence 1 when RTC alarm occurs as per configuration in registers CTL_2, RTC_T, and RTC_A (proceed as if ACT = High). If NPWR_BTN is pressed before the RTC alarm, then the TPS38700-Q1 moves to Sequence 1 at that time.

(1) FORCE_INT is used by software for periodic check for internal or external short to VDD on NIRQ pin.
(2) FORCE_ACT is automatically set by HW when entering the Power Up sequence (SEQUENCE 1). As the TPS38700-Q1 performs the power-up sequence, ACT can be undefined. FORCE_ACT being set prevents a bad ACT level from causing a transition directly into SLEEP before the application processor has booted. I^2C commands are allowed to clear this bit but not set the bit.

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表 7-25. CTL_2

Address: 0x29

Description: Miscellaneous configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION	
7:4	RST_DLY[3:0]	Power up sequence: NRST remains asserted until RST_DLY[3:0] after last ENx assert.	
		0000b = 0.1ms 0001b = 0.2ms 0010b = 0.4ms 0011b = 0.8ms 0100b = 1.6ms 0101b = 3.2ms 0110b = 6.4ms 0111b = 12.8ms	1000b = 1ms 1001b = 2ms 1010b = 4ms 1011b = 8ms 1100b = 16ms 1101b = 32ms 1110b = 64ms 1111b = 128ms
		Power down sequence: NRST asserted within t_{NRST} of ACT= Low.	
3	RTC_WAKE	Autonomous RTC wake alarm enable: 0 = Disabled (CTL_1.FORCE_ACT = 0 on RTC alarm). 1 = Enabled (CTL_1.FORCE_ACT = 1 on RTC alarm). If RTC_T == RTC_A, a wake event is generated which sets INT_SRC1.RTC. If this bit is enabled, then also CTL_1.FORCE_ACT is set to 1, triggering the automatic exit from SLEEP state to ACTIVE.	
2	RTC_PU	Autonomous RTC Power Up from SHDN2 to ACTIVE: 0 = Disabled. 1 = Enabled. If RTC_T == RTC_A, a power-up event is generated.	
1	REQ_PEC	Require PEC byte (valid only if EN_PEC is 1): 0 = missing PEC byte is treated as good PEC. 1 = missing PEC byte is treated as bad PEC, triggering a fault.	
0	EN_PEC	Packet Error Checking (PEC): 0 = PEC disabled (Default). 1 = PEC Enabled. Disables support for register address auto-increment.	

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表 7-26. TEST_CFG

Address: 0x2A

Description: Built-In Self Test (BIST) execution configuration.

Default: Loaded from NVM (only AT_POR[1:0])

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:3	RSVD	Reserved
2	AT_SHDN	0 = Do not run BIST when exiting Sequence 5 or Sequence 6. 1 = Run BIST when exiting Sequence 5 or Sequence 6 if CTL_1.FORCE_SHDN[1:0] = 00b. Device ready after t_{CFG_WB}. This bit cannot be set in OTP. Always defaults to 0 when loading configuration from OTP.
1:0	AT_POR[1:0]	Run BIST at POR. Device ready after t_{CFG_WB}. 00b = Valid OTP configuration, skip BIST at POR 01b = Corrupt OTP configuration, run BIST at POR. 10b = Corrupt OTP configuration, run BIST at POR. 11b = Valid OTP configuration, run BIST at POR.

表 7-27. IEN_VENDOR

Address: 0x2B

Description: Vendor Specific Internal Interrupt Enable register.

POR Value: 0x00 or load from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	FAULTS[7:0]	Vendor specific internal faults enables.

表 7-28. SEQ_CFG

Address: 0x30

Description: Sequencing configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	GPO8	General Purpose Output. Only used when both PWR_EN8 and SLP_EN8 are clear. 0 = GPO8 pin driven low. 1 = GPO8 pin driven high.

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表 7-28. SEQ_CFG (続き)

Address: 0x30

Description: Sequencing configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
6	GPO7	General Purpose Output. Only used when both PWR_EN7 and SLP_EN7 are clear. 0 = GPO7 pin driven low. 1 = GPO7 pin driven high.
5	GPO6	General Purpose Output. Only used when both PWR_EN6 and SLP_EN6 are clear. 0 = GPO6 pin driven low. 1 = GPO6 pin driven high.
4	GPO5	General Purpose Output. Only used when both PWR_EN5 and SLP_EN5 are clear. 0 = GPO5 pin driven low. 1 = GPO5 pin driven high.
3	RSVD	Reserved
2	RSVD	Reserved
1	RSVD	Reserved
0	SSTEP	Sequencing time slot step size selection for SEQ_USLOT and SEQ_DSLOT: 0 = Time slot step size t_{SSTEP} = 250µs 1 = Time slot step size t_{SSTEP}= 1000µs

表 7-29. SEQ_USLOT

Address: 0x31

Description: Power Up / Sleep Exit sequencing time slot configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	TIME[7:0]	Sets time slot between sequencing points on power-up / sleep-exit: t_{USLOT} = SEQ_USLOT.TIME[7:0] × t_{SSTEP} + t_{SMIN} with t_{SSTEP} set by SEQ_CFG.SSTEP and t_{SMIN} = t_{SSTEP}/2 For the case where SEQ_CFG.SSTEP = 0, refer to 表 7-30. For the case where SEQ_CFG.SSTEP = 1, refer to 表 7-31.

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表 7-30. SEQ_CFG.SSTEP = 0

PARAMETER	SYMBOL	MIN (-6%)	TYPICAL	MAX (+6%)	UNIT
Slot step size	t_{SSTEP}	235	250	265	µs
Min slot time (0x00)	t_{SMIN}	117.5	125	132.5	µs
Max slot time (0xFF)	t_{SMAX}	60042.5	63875	67707.5	µs

表 7-31. SEQ_CFG.SSTEP = 1

PARAMETER	SYMBOL	MIN (-6%)	TYPICAL	MAX (+6%)	UNIT
Slot step size	t_{SSTEP}	940	1000	1060	µs
Min slot time (0x00)	t_{SMIN}	470	500	530	µs
Max slot time (0xFF)	t_{SMAX}	240170	255500	270830	µs

表 7-32. SEQ_DSLOT

Address: 0x32

Description: Power Down / Sleep Entry sequencing time slot configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	TIME[7:0]	Sets time slot between sequencing points on power-down / sleep-entry: t_{DSLOT} = SEQ_DSLOT.TIME[7:0] × t_{SSTEP} + t_{SMIN} with t_{SSTEP} set by SEQ_CFG.SSTEP and t_{SMIN} = t_{SSTEP}/2 See 表 7-29 for setting details.

表 7-33. PWR_EN[12:1]

Address: PWR_EN1 (0x33) - PWR_EN12 (0x3E) (Twelve 8-bit registers).

Description: Power Up/ Down sequence definition by assignment of EN[12:1] to one of fifteen time slots.

Slot=1 is the earliest slot that can be selected and indicates that the ENx pin toggles in the first SEQ_USLOT.TIME or SEQ_DSLOT.TIME after the triggering event. See セクション 7.3.6.9.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	PU[3:0]	Power Up Sequence: 0 = ENx pin not mapped to sequence. ENx maintains previous state, unless entering BACKUP or FAILSAFE state (ENx is pulled low in those states). 1 = ENx pin mapped to first time slot (first up). 15 = ENx pin mapped to last time slot (last up).

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表 7-33. PWR_EN[12:1] (続き)

Address: PWR_EN1 (0x33) - PWR_EN12 (0x3E) (Twelve 8-bit registers).

Description: Power Up/ Down sequence definition by assignment of EN[12:1] to one of fifteen time slots.

Slot=1 is the earliest slot that can be selected and indicates that the ENx pin toggles in the first SEQ_USLOT.TIME or SEQ_DSLOT.TIME after the triggering event. See セクション 7.3.6.9.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
3:0	PD[3:0]	Power Down Sequence: 0 = ENx pin not mapped to sequence. ENx maintains previous state, unless entering BACKUP or FAILSAFE state (ENx is pulled low in those states). 1 = ENx pin mapped to first time slot (first down). 15 = ENx pin mapped to last time slot (last down).

表 7-34. PWR_CLK32OE

Address: 0x3Fh

Description: Power Up/ Down (PU/ PD) sequence assignment of 32kHz clock output to one of fifteen time slots.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	PU[3:0]	0 = CLK32 not mapped to PU sequence. CLK32 maintains previous state, unless entering BACKUP or FAILSAFE state (CLK32 is pulled low in those states). 1 = Enable CLK32 on first PU time slot. 15 = Enable CLK32 on last PU time slot.
3:0	PD[3:0]	0 = CLK32 not mapped to PD sequence. CLK32 maintains previous state, unless entering BACKUP or FAILSAFE state (CLK32 is pulled low in those states). 1 = Disable CLK32 on first PD time slot. 15 = Disable CLK32 on last PD time slot.

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表 7-35. SLP_EN[12:1]

Address: SLP_EN1 (0x53) - SLP_EN12 (0x5E) (Twelve 8-bit registers).

Description: Sleep Exit/Entry sequence definition by assignment of EN[12:1] to one of fifteen time slots.

Slot=1 is the earliest slot that can be selected and indicates that the ENx pin toggles in the first SEQ_USLOT.TIME or SEQ_DSLOT.TIME after the triggering event. See セクション 7.3.6.9.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	SLP_EXIT[3:0]	Sleep Exit Sequence: 0 = ENx pin not mapped to sequence. ENx maintains previous state, unless entering BACKUP or FAILSAFE state (ENx is pulled low in those states). 1 = ENx pin mapped to first time slot (first up). 15 = ENx pin mapped to last time slot (last up).
3:0	SLP_ENTRY[3:0]	Sleep Entry Sequence: 0 = ENx pin not mapped to sequence. ENx maintains previous state, unless entering BACKUP or FAILSAFE state (ENx is pulled low in those states). 1 = ENx pin mapped to first time slot (first down). 15 = ENx pin mapped to last time slot (last down).

表 7-36. SLP_CLK32OE

Address: 0x5F

Description: Sleep Exit/Entry sequence assignment of 32kHz clock output to one of fifteen time slots.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	SLP_EXIT[3:0]	0 = CLK32 not mapped to Sleep Exit sequence. CLK32 maintains previous state, unless entering BACKUP or FAILSAFE state (CLK32 is pulled low in those states). 1 = Enable CLK32 on first Sleep Exit time slot. 15 = Enable CLK32 on last Sleep Exit time slot.
3:0	SLP_ENTRY[3:0]	0 = CLK32 not mapped to Sleep Entry sequence. CLK32 maintains previous state, unless entering BACKUP or FAILSAFE state (CLK32 is pulled low in those states). 1 = Disable CLK32 on first Sleep Entry time slot. 15 = Disable CLK32 on last Sleep Entry time slot.

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表 7-37. RTC_T[31:0]

Address: RTC_T[31:24] (0x70) - RTC_T[7:0] (0x73) (Four 8-bit registers).

Description: RTC time setting. Although no provision is specified to maintain data coherency across the four registers,the expectation is that accessing these registers in a single transaction makes sure data coherency is maintained. RTC_T register values must be written prior to RTC_A values.

POR Value: 0x00000000

Access: Read/Write. Read-only if RTC group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
31:24	RTC_T3	RTC Time Byte 3 Address 0x70
23:16	RTC_T2	RTC Time Byte 2 Address 0x71
15:8	RTC_T1	RTC Time Byte 1 Address 0x72
7:0	RTC_T0	RTC Time Byte 0 Address 0x73

32-bit unsigned value representing 136 years of 1 second ticks since power-on. Can be used to keep POSIX time. Must be set with correct value on each power-up

表 7-38. RTC_A[31:0]

Address: RTC_A[31:24] (0x74) - RTC_A[7:0] (0x77) (Four 8-bit registers).

Description: RTC alarm setting. Although no provision is specified to maintain data coherency across the four registers, TI expects that accessing these registers in a single transaction is best for data coherency.

POR Value: 0xFFFFFFFF

Access: Read/Write. Read-only if RTC group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
31:24	RTC_A3	RTC Alarm Byte 3 Address 0x74
23:16	RTC_A2	RTC Alarm Byte 2 Address 0x75
15:8	RTC_A1	RTC Alarm Byte 1 Address 0x76
7:0	RTC_A0	RTC Alarm Byte 0 Address 0x77

Assert Alarm when RTC_T[31:0]==RTC_A[31:0]. See CTL_2.RTC_WAKE and CTL_2.RTC_PU for wake events.

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表 7-39. WDT_CFG

Address: 0x80

Description: WDT configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if WDT group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:6	WDTEN[1:0]	00b = Watchdog disabled. 01b = On successive expires, first interrupt, then reset, then power-down according to WDT_CFG.PDMD. 10b = On successive expires, first reset, then power-down according to WDT_CFG.PDMD. 11b = Power-down according to WDT_CFG.PDMD on expire.
5	SLP_EN	Automatic disable in sleep mode: 0 = Watchdog disabled automatically in sleep mode. 1 = Watchdog enabled in sleep mode.
4:2	WDTDLY[2:0]	Delay, in number of WDT periods (WDT_CLOSE + WDT_OPEN), from de-assertion of NRST (if exiting SHDN1 or SHDN2 states), or from value written to WDT_CFG.WDTEN[1:0], or from Sleep state exit (if WDT_CFG.SLP_EN=0), to first close window. 000b = 1 WDT period. 111b = 8 WDT periods.
1:0	PDMD[1:0]	Power Down Mode for WDT force power-down. Value written to CTL_1.FORCE_SHDN[1:0] on WDT power-down event.

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表 7-40. WDT_CLOSE

Address: 0x81

Description: WDT close window configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if WDT group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION		
7:0	CLOSE[7:0]	WDT close window duration: LSB increment value		
		1ms (00h-1Fh)	2ms (20h-3Fh)	4ms (40h-FFh)
		00h = 1ms 01h = 2ms 02h = 3ms 03h = 4ms 04h = 5ms ... 1Dh = 30ms 1Eh = 31ms 1Fh = 32ms	20h = 34ms 21h = 36ms 22h = 38ms 23h = 40ms 24h = 42ms ... 3Dh = 92ms 3Eh = 94ms 3Fh = 96ms	40h = 100ms 41h = 104ms 42h = 108ms 43h = 112ms 44h = 116ms ... FDh = 856ms FEh = 860ms FFh = 864ms

表 7-41. WDT_OPEN

Address: 0x82

Description: WDT open window configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if WDT group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION		
7:0	OPEN[7:0]	WDT open window duration: LSB increment value		
		1ms (00h-1Fh)	2ms (20h-3Fh)	4ms (40h-FFh)
		00h = 1ms 01h = 2ms 02h = 3ms 03h = 4ms 04h = 5ms ... 1Dh = 30ms 1Eh = 31ms 1Fh = 32ms	20h = 34ms 21h = 36ms 22h = 38ms 23h = 40ms 24h = 42ms ... 3Dh = 92ms 3Eh = 94ms 3Fh = 96ms	40h = 100ms 41h = 104ms 42h = 108ms 43h = 112ms 44h = 116ms ... FDh = 856ms FEh = 860ms FFh = 864ms

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表 7-42. WDTKEY

Address: 0x83

Description: WDT key to reset.

POR Value: 0x00

Access: Read/Write.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	KEY[7:0]	Watchdog key register.

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表 7-43. PROT1, PROT2

Address: 0xF0, 0xF1

Description: Protection selection registers. To write-protect a register group, the host must set the relevant bit in both registers.

POR Value: 0x00

Access: Read/Write.

For security, these registers need to have POR value=0x00 and become read-only once set until power cycle.

Once set to 1, the bits cannot be cleared to 0 by the host; a power cycle (VDD=0) is required to write different registers configurations.

These registers are cleared also if BIST is executed on exiting Sequence 5 or Sequence 6 (TEST_CFG.AT_SHDN=1).

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	RSVD	Reserved
6	WRK	0 = Working registers are writable. 1 = Writes to working registers are ignored.
5	SEQS	0 = Sleep Sequence registers are writable. 1 = Writes to Sleep Sequence registers are ignored.
4	SEQP	0 = Power Sequence registers are writable. 1 = Writes to Power Sequence registers are ignored.
3	SEQC	0 = Sequence slot configuration registers are writable. 1 = Writes to Sequence slot configuration registers are ignored.
2	WDT	0 = WDT registers are writable. 1 = Writes to WDT registers are ignored.
1	RTC	0 = RTC registers are writable. 1 = Writes to RTC registers are ignored.
0	CTL	0 = Control registers are writable. 1 = Writes to control registers are ignored.

表 7-44. I2CADDR

Address: 0xF9

Description: I^2C address.

POR Value: Loaded from NVM.

Access: Read-Only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	RSVD	Reserved
6:0	ADDR_NVM[6:0]	I^2C target device address. Set in NVM.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Modern SOC and FPGA devices typically have multiple power rails to provide power to the different blocks within the IC. Accurate voltage level and timing requirements are common and must be met to make sure proper operation of these devices. By utilizing TPS38700-Q1 along with a multichannel voltage supervisor, the power up and power down sequencing requirements as well as the core voltage requirements of the target SOC or FPGA device can be met. This design focuses on meeting the timing requirements for an SOC by using the TPS38700-Q1.

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8.2 Typical Application

8.2.1 Automotive Multichannel Sequencer and Monitor

A typical application for the TPS38700-Q1 is shown in 図 8-1. TPS38700-Q1 is used to provide the proper voltage sequencing for the target SOC device by providing enable signals to the DC/DC converters shown. These DC/DC converters are used to generate the appropriate voltage rails for the SOC. A mulitchannel voltage monitor is used to monitor the voltage rails as these rails power up and power down to verify that the correct sequence occurs in both occasions. A safety microcontroller is also used to provide ACT, NIRQ, and I^2C commands to the TPS38700-Q1 and the multichannel voltage monitor. The ACT signal from the safety microcontroller determines when the TPS38700-Q1 enters into ACTIVE or SHDN states while the NIRQ pin of the TPS38700-Q1 acts as an interrupt pin that is set when a fault has occurred. For instance, if an external device pulls the NRST pin low, then the TPS38700-Q1 triggers an interrupt through the NIRQ pin. I^2C is used to communicate the type of fault to the host microcontroller. The host microcontroller can clear the fault by writing 1 to the affected register. The power rails for the safety microcontroller are not shown in 図 8-1 for simplicity.

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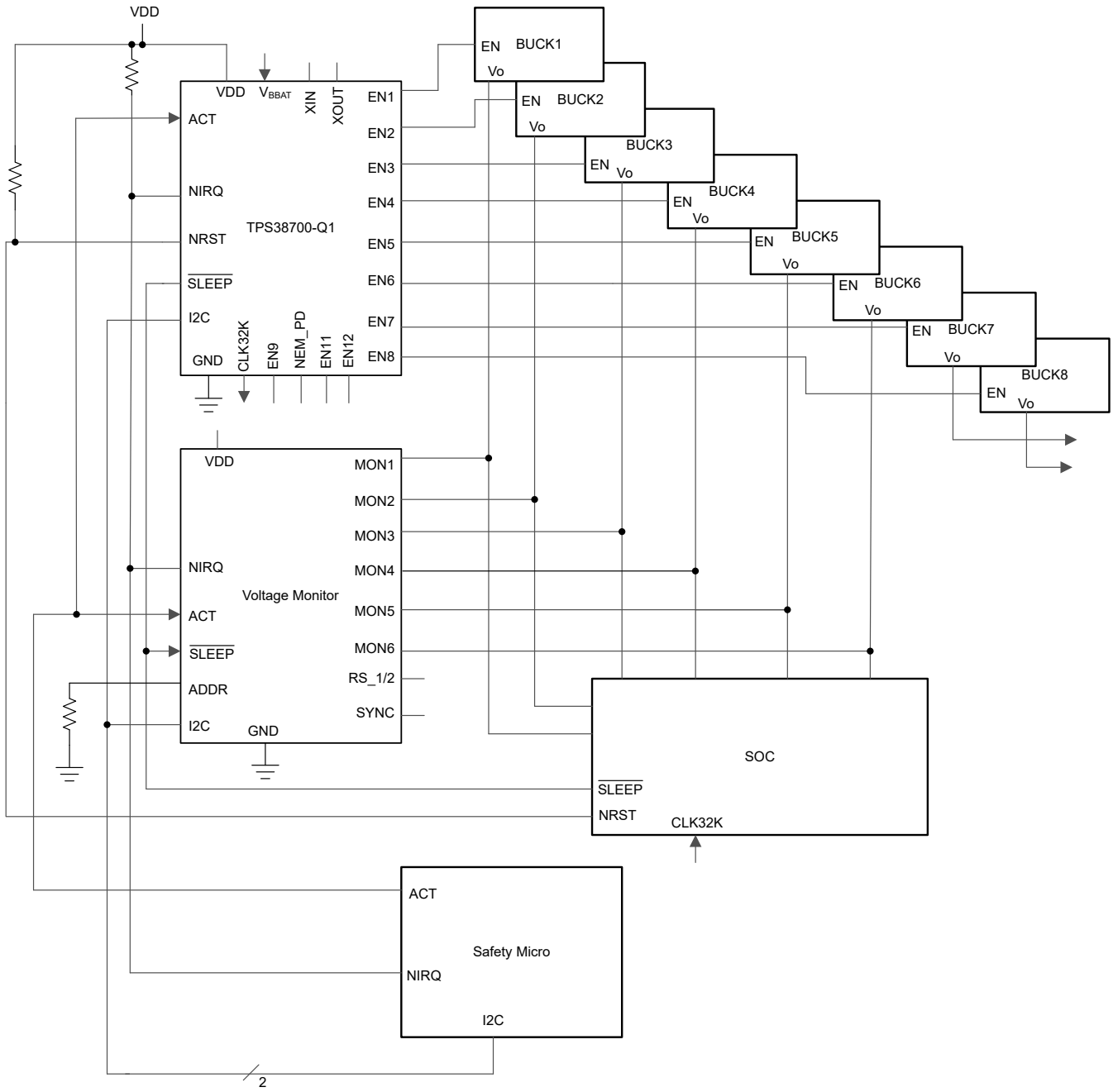


図 8-1. TPS38700-Q1 Voltage Sequencer Design Block Diagram

8.2.2 Design Requirements

- Eight different voltage rails supplied by DC/DC converters need to be properly sequenced in this design. The sequence order and timing requirements are outlined in 表 8-1 and 表 8-2.
- Emergency power down functionality is optional.
- Backup battery power supply required. This must be stepped down to a maximum value of 5.5V to comply with the absolute maximum ratings of the V_{BBAT} pin.
- All detected failures in sequencing must be reported via an external hardware interrupt signal.
- All detected failures must be logged in internal registers and be accessible to an external processor via I^2C.

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表 8-1. Power Up and Power Down Sequence Requirement

ENABLE CHANNEL	POWER UP SEQUENCE POSITION	POWER DOWN SEQUENCE POSITION	TIME BETWEEN POWER UP SIGNALS (µs)	TIME BETWEEN POWER DOWN SIGNALS (µs)
EN1	1	5	625	625
EN2	1	1	625	625
EN3	2	4	625	625
EN4	2	4	625	625
EN5	4	2	625	625
EN6	6	1	625	625
EN7	1	1	625	625
EN8	2	4	625	625

表 8-2. Sleep Entry and Sleep Exit Sequence Requirement

ENABLE CHANNEL	SLEEP EXIT SEQUENCE POSITION	SLEEP ENTRY SEQUENCE POSITION	TIME BETWEEN SLEEP EXIT SIGNALS (µs)	TIME BETWEEN SLEEP ENTRY SIGNALS (µs)
EN1	0	0	625	625
EN2	1	3	625	625
EN3	3	2	625	625
EN4	0	0	625	625
EN5	0	0	625	625
EN6	2	1	625	625
EN7	1	3	625	625
EN8	3	2	625	625

8.2.3 Detailed Design Procedure

- TPS38700-Q1 device comes preprogrammed with the power up, power down, sleep entry, and sleep exit sequences shown in 表 8-1 and 表 8-2.
- NIRQ and NRST pins both require a pull up resistor in the range of 10kΩ to 100kΩ.
- SDA and SCL lines require pull up resistors in the range of 10kΩ.
- The ACT pin is driven by an external safety microcontroller. When the ACT pin is driven high, the device enters into ACTIVE mode as described in セクション 7.3.6.1. When the ACT pin is driven low, the device enters into SHDN mode as described in セクション 7.3.6.5.
- The safety microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT_SCR1 and INT_SCR2 registers. The interrupt flags can only be cleared by the host microcontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.
- The SLEEP pin is driven by the SOC. When the $\overline{\text{SLEEP}}$ pin is driven low, the device enters into Sleep mode as shown in セクション 7.3.6.3. When the $\overline{\text{SLEEP}}$ pin is driven high, the device exits Sleep mode as shown in セクション 7.3.6.4.
- The safety microcontroller must be connected to the NEM_PD input pin of the TPS38700-Q1 device to enable emergency power down functionality. When this pin is driven low, the TPS38700-Q1 device enters into power down sequence. Power down due to NEM_PD is shown in 図 7-12.

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8.2.4 Application Curves

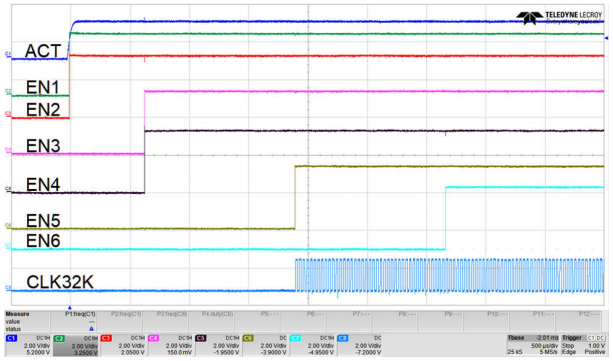


図 8-2. Power Up Sequence

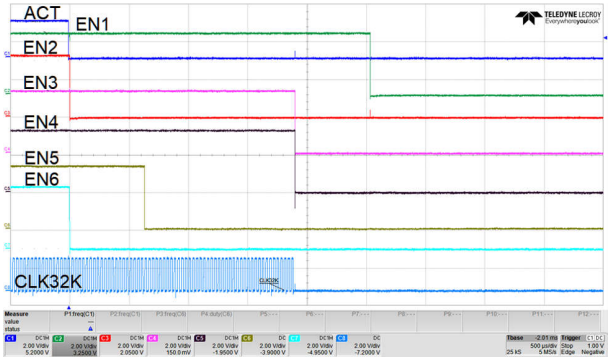


図 8-3. Power Down Sequence

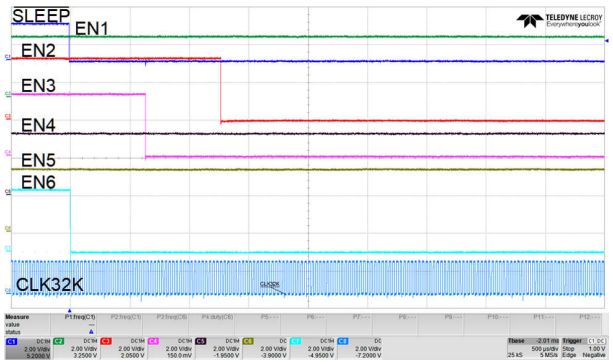


図 8-4. Sleep Entry Sequence

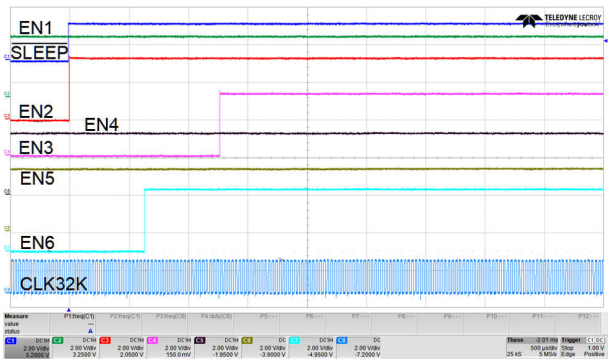


図 8-5. Sleep Exit Sequence

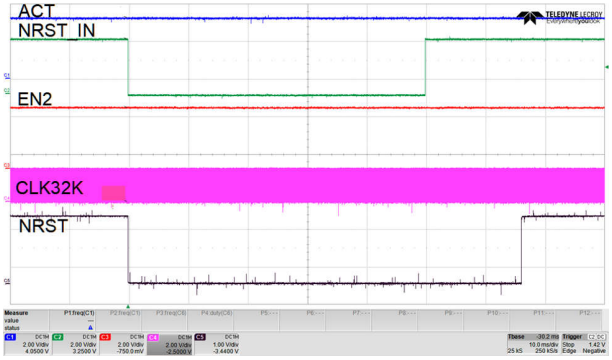


図 8-6. RESET Triggered by NRST_IN

図 8-2 depicts the power up sequencing order listed in 表 8-1. Notice EN1 rises at the same time as the ACT signal due to the number 1 slot selection. Additonally, notice EN3 and EN4 rise 625us after EN1 due to the number two slot selection. The TPS38700-Q1 timing tool found under the "Design tool's & simulation" section of the TPS38700-Q1 web page can be used to assist in implementing a desired slot selection.

8.3 Power Supply Recommendations

8.3.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 2.2V to 5.5V. There is a 6V absolute maximum rating on the VDD pin as well as on the V_{BBAT} pin. Good analog practice places a 0.1µF to 1µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the

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voltage supply providing power to VDD is susceptible to any large voltage transients that exceed maximum specifications, additional precautions must be taken.

8.4 Layout

8.4.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Do not use long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Do not use long traces of voltage to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

8.4.2 Layout Example

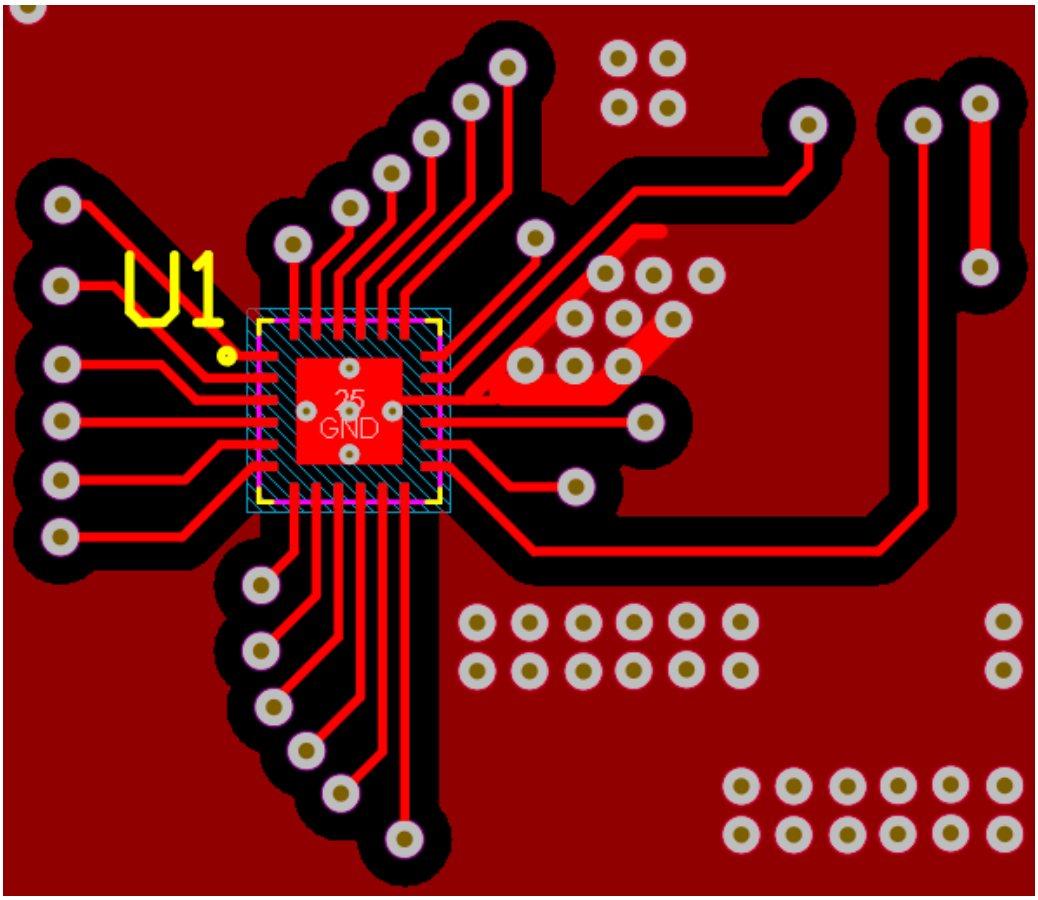


図 8-7. Recommended Layout

9 Device and Documentation Support

9.1 Device Nomenclature

表 9-1 shows how to decode the function of the device based on the device ordering code, while 表 9-2 shows the sequence configuration based on the device ordering code. See 図 4-1 for more information regarding how to decode the device part number.

表 9-1. Device Comparison Table

ORDERING CODE	FUNCTIONS	EN PINS DEFAULT	ALT FUNC. PINS	TIME SLOT (µsec)	I²C ADDR.	RESET DELAY (msec)	WATCHDOG	PEC (1)	I²C PULL-UP VOLTAGE (V)
TPS38700C03NRGERQ1	Sequencer, NEM_PD	Push-Pull Low	Open-Drain	625	3C	16	Disabled	Enabled	3.3
	Sequencer	Push-Pull Low	N/A	10500	3C	16	Disabled	Disabled	1.2
	Sequencer	Push-Pull Low	N/A	10500	3C	16	Disabled	Disabled	1.2

(1) For parts with PEC enabled:
- a. PEC calculation is based on initializing to 0x00.
- b. In case of a PEC violation there needs to be a subsequent I²C transaction before NIRQ is asserted.
- c. If incorrect PEC is given NIRQ is asserted.
- d. If there is an extra byte after successfully writing the correct PEC byte, NIRQ is asserted and the write fails.

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表 9-2. Sequence Configuration Table

ORDERING CODE	PINS	SEQUENCE UP	SEQUENCE DOWN
03N	PWR_EN1	Power Up Slot 1	Power Down Slot 5
	PWR_EN2	Power Up Slot 1	Power Down Slot 1
	PWR_EN3	Power Up Slot 2	Power Down Slot 4
	PWR_EN4	Power Up Slot 2	Power Down Slot 4
	PWR_EN5	Power Up Slot 4	Power Down Slot 2
	PWR_EN6	Power Up Slot 6	Power Down Slot 1
	PWR_EN7	Power Up Slot 1	Power Down Slot 1
	PWR_EN8	Power Up Slot 2	Power Down Slot 4
	PWR_EN9	Power Up Slot 4	Power Down Slot 2
	PWR_EN10	Power Up Slot 0	Power Down Slot 0
	PWR_EN11	Power Up Slot 4	Power Down Slot 2
	PWR_EN12	Power Up Slot 0	Power Down Slot 0
	PWR_CLK32	Power Up Slot 4	Power Down Slot 4
		Sequence Down	Sequence Up
	SLP_EN1	Sleep Exit Slot 0	Sleep Entry Slot 0
	SLP_EN2	Sleep Exit Slot 1	Sleep Entry Slot 3
	SLP_EN3	Sleep Exit Slot 3	Sleep Entry Slot 2
	SLP_EN4	Sleep Exit Slot 0	Sleep Entry Slot 0
	SLP_EN5	Sleep Exit Slot 0	Sleep Entry Slot 0
	SLP_EN6	Sleep Exit Slot 2	Sleep Entry Slot 1
	SLP_EN7	Sleep Exit Slot 1	Sleep Entry Slot 3
	SLP_EN8	Sleep Exit Slot 3	Sleep Entry Slot 2
	SLP_EN9	Sleep Exit Slot 4	Sleep Entry Slot 1
	SLP_EN10	Sleep Exit Slot 0	Sleep Entry Slot 0
	SLP_EN11	Sleep Exit Slot 1	Sleep Entry Slot 1
	SLP_EN12	Sleep Exit Slot 0	Sleep Entry Slot 0
	SLP_CLK32	Sleep Exit Slot 0	Sleep Entry Slot 0

表 9-3. Sequence Configuration Table

ORDERING CODE	PINS	SEQUENCE UP	SEQUENCE DOWN
03N	PWR_EN1	Power Up Slot 5	Power Down Slot 4
	PWR_EN2	Power Up Slot 3	Power Down Slot 6
	PWR_EN3	Power Up Slot 1	Power Down Slot 8
	PWR_EN4	Power Up Slot 6	Power Down Slot 3
	PWR_EN5	Power Up Slot 8	Power Down Slot 1
	PWR_EN6	Power Up Slot 7	Power Down Slot 2
	PWR_EN7	Power Up Slot 4	Power Down Slot 5
	PWR_EN8	Power Up Slot 2	Power Down Slot 7

表 9-4. Sequence Configuration Table

ORDERING CODE	PINS	SEQUENCE UP	SEQUENCE DOWN
03N	PWR_EN1	Power Up Slot 1	Power Down Slot 1
	PWR_EN2	Power Up Slot 2	Power Down Slot 2
	PWR_EN3	Power Up Slot 2	Power Down Slot 2
	PWR_EN4	Power Up Slot 3	Power Down Slot 3
	PWR_EN5	Power Up Slot 3	Power Down Slot 3
	PWR_EN6	Power Up Slot 4	Power Down Slot 4
	PWR_EN7	Power Up Slot 4	Power Down Slot 4
	PWR_EN8	Power Up Slot 4	Power Down Slot 4
	PWR_EN9	Power Up Slot 4	Power Down Slot 4
	PWR_EN10	Power Up Slot 5	Power Down Slot 5
	PWR_EN11	Power Up Slot 5	Power Down Slot 5

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2022) to Revision D (March 2025)	Page
• Added seperate PEC section	32
• Added register info to 0x30	34
• Fixed typo in 0x21 and added details for 0x30	38

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Changes from Revision B (October 2022) to Revision C (December 2022)	Page
• Updated Electrical Characteristics	8
• Added various orderables for I2C logic levels	8

Changes from Revision A (July 2021) to Revision B (October 2022)	Page
• 量産データのリリース	1
•	4
• Added 0801N,0B01N variants into the Device Comparison Table	68

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

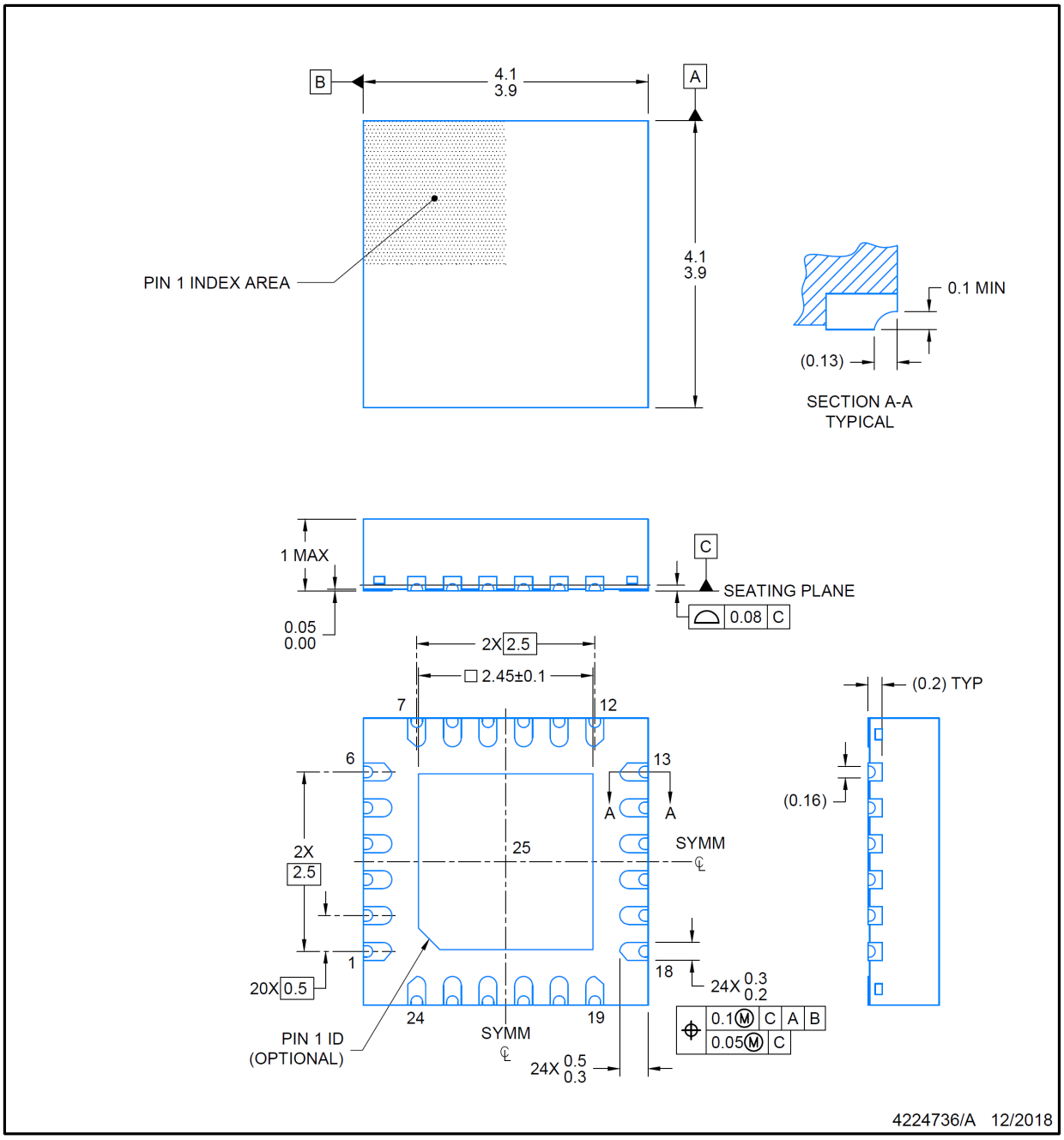
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PACKAGE OUTLINE

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

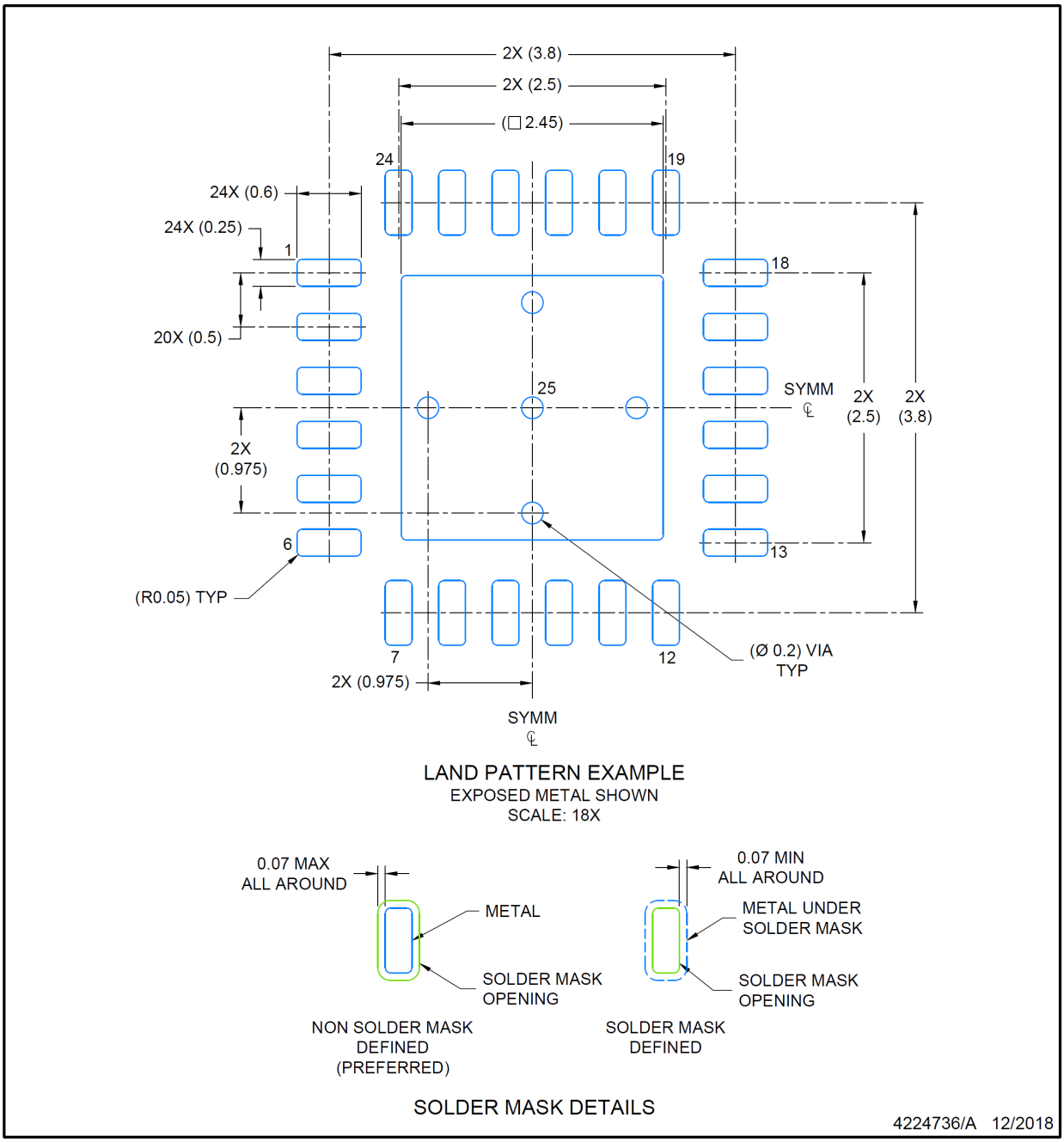
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EXAMPLE BOARD LAYOUT

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

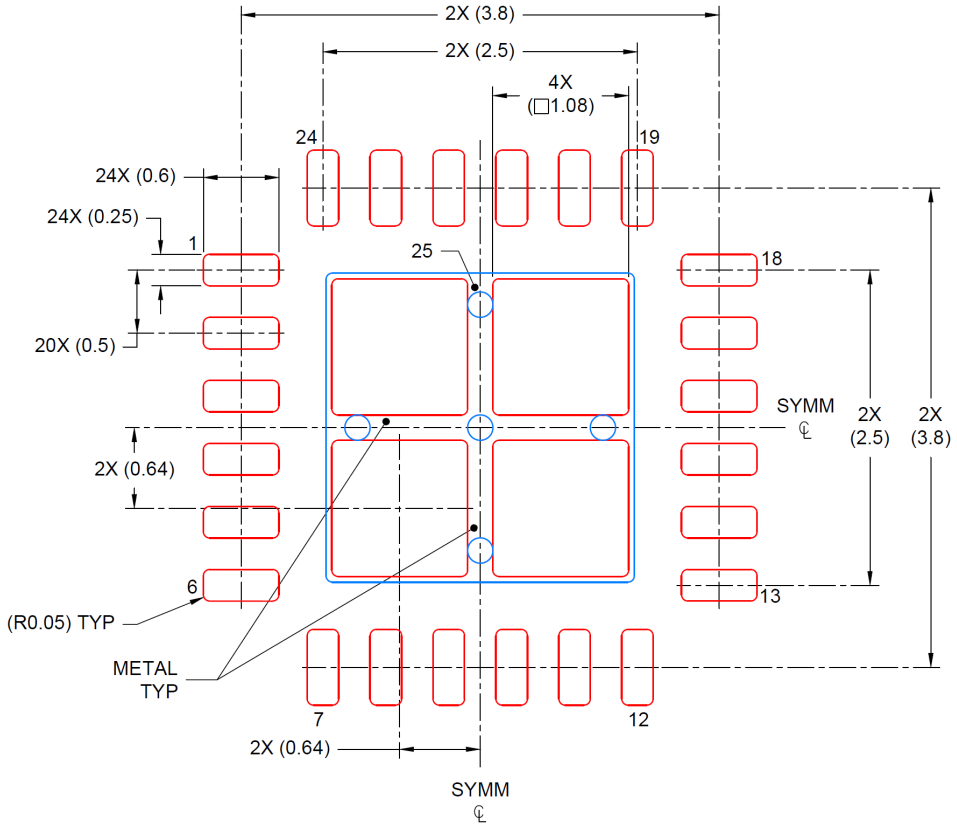
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS38700BN31RGERQ1	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T38700B N31Q1
TPS38700BN31RGERQ1.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T38700B N31Q1
TPS38700C03NRGERQ1	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T38700C 03NQA1
TPS38700C03NRGERQ1.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T38700C 03NQA1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS38700-Q1 :

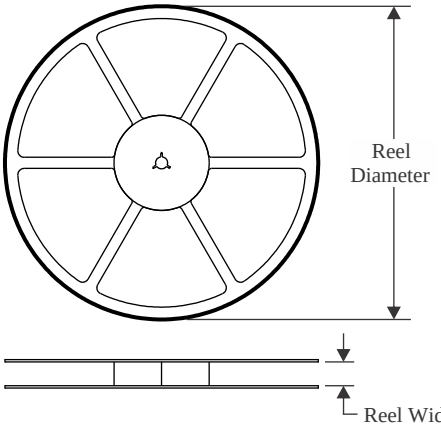
- Catalog : TPS38700

NOTE: Qualified Version Definitions:

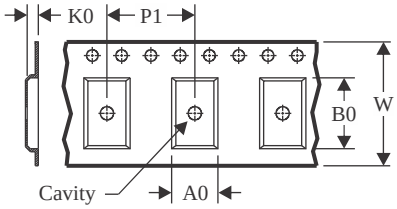
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

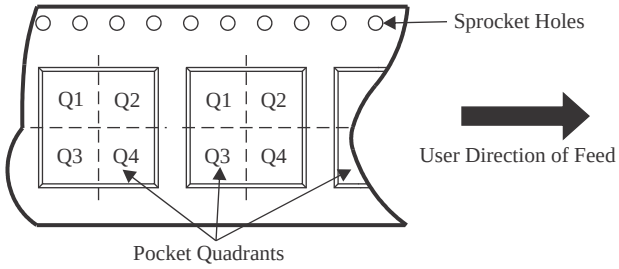


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

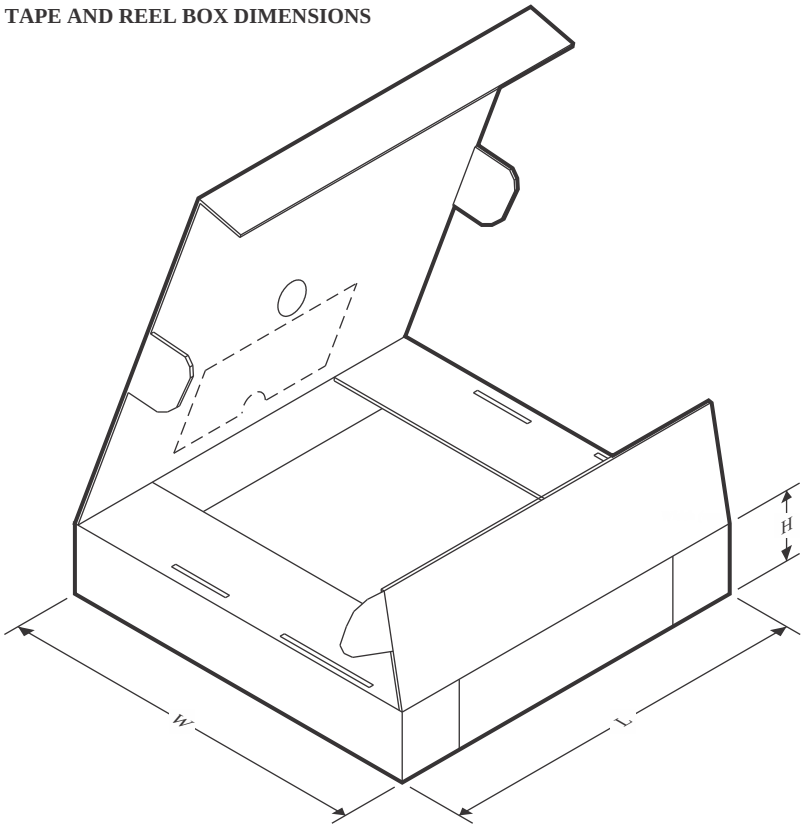
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS38700BN31RGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS38700C03NRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



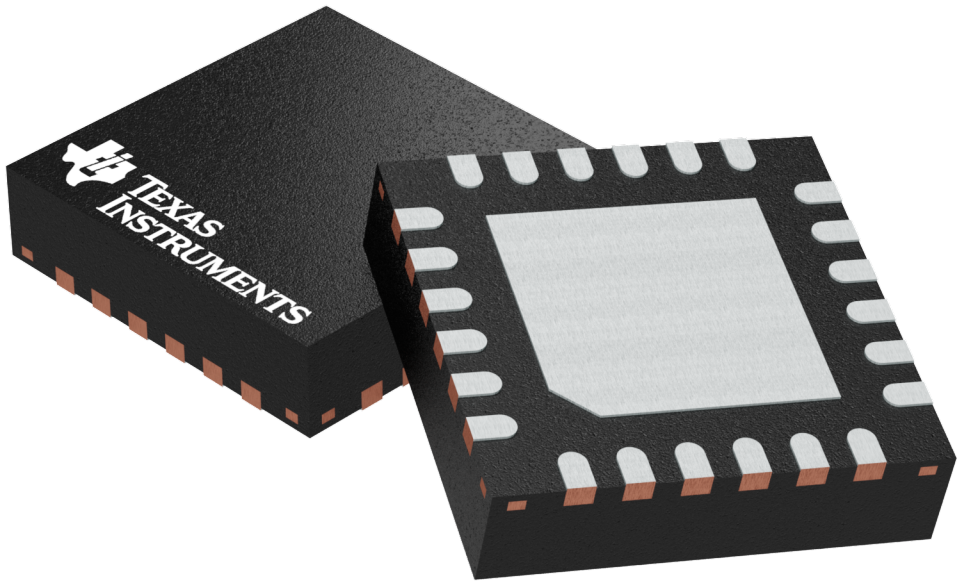
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS38700BN31RGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS38700C03NRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

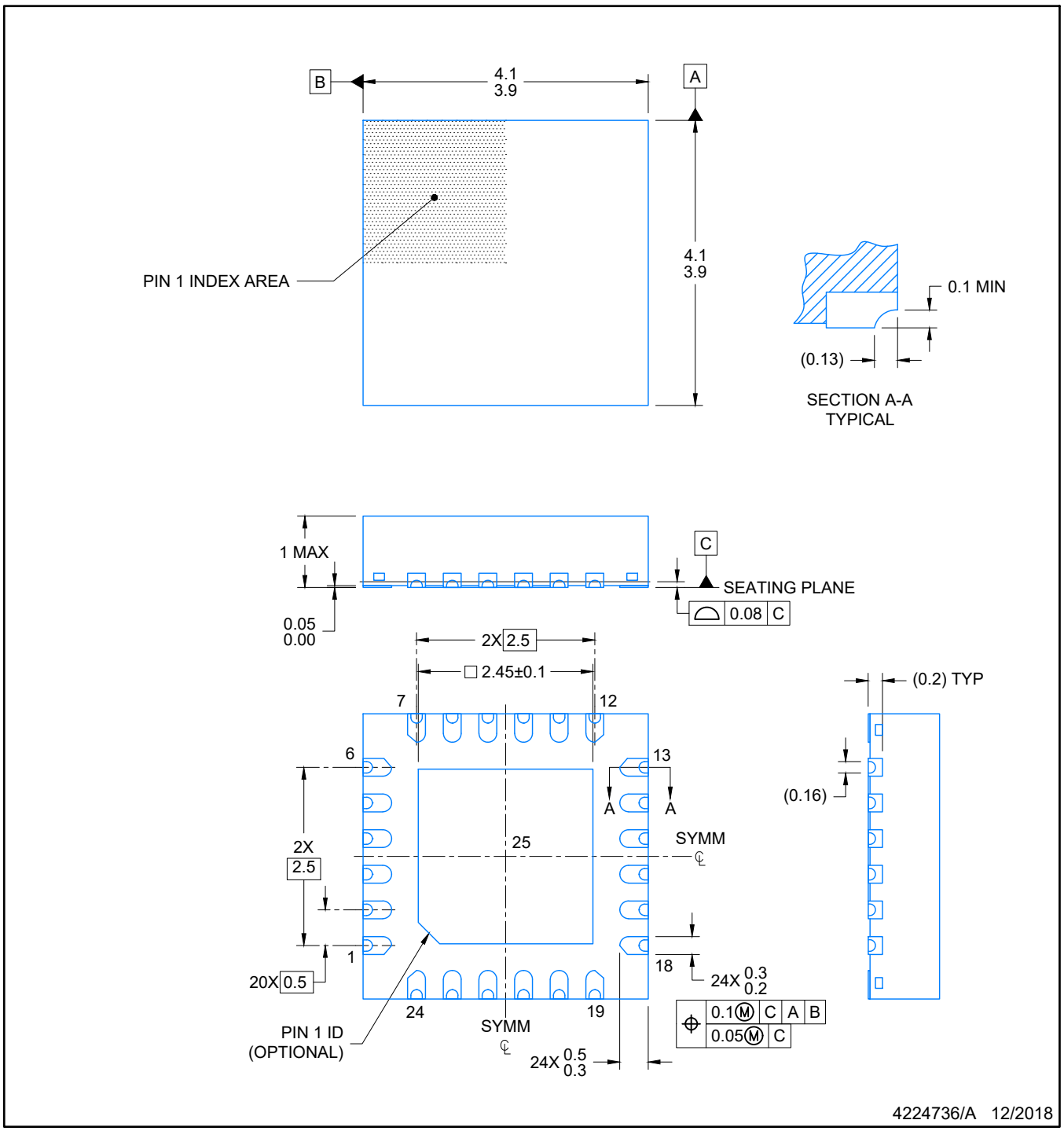
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



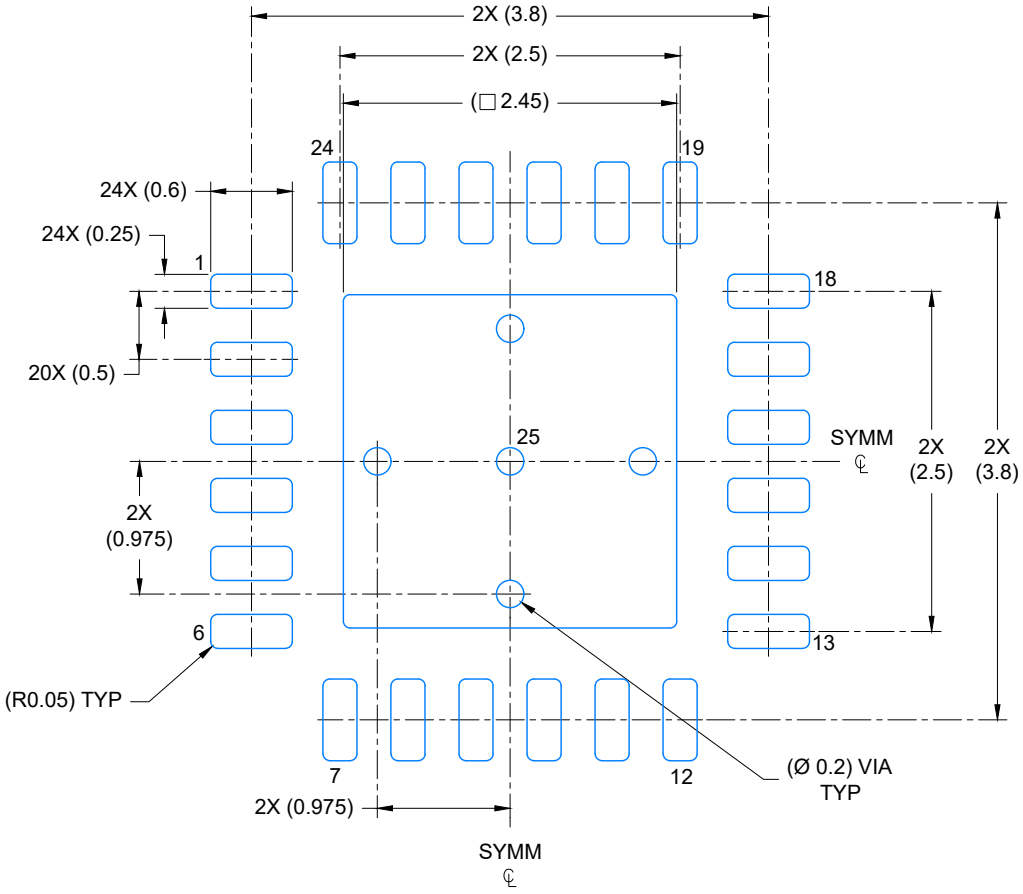
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

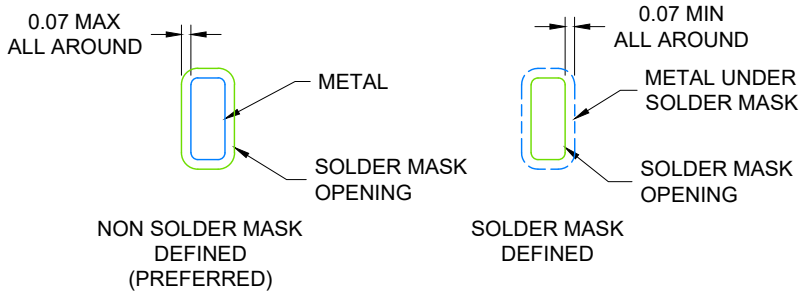


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

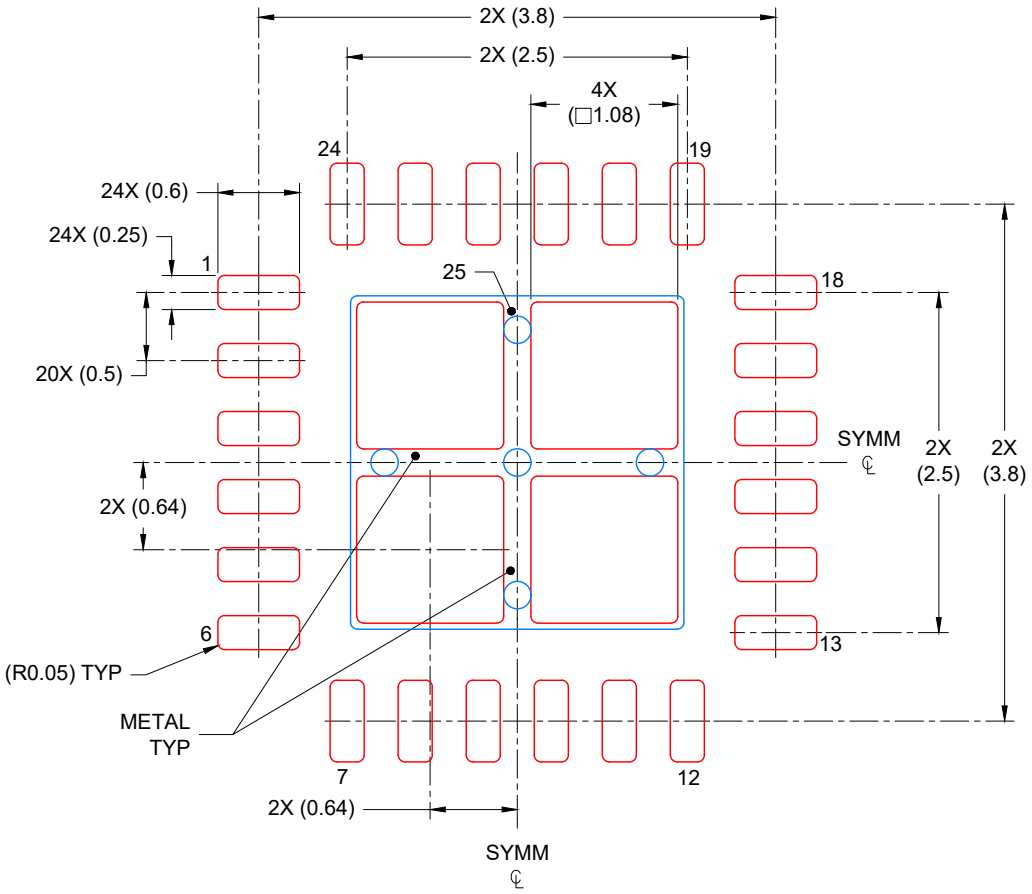


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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