



TPS3890

低静止電流、1%精度のスーパーバイザ、遅延プログラム可能

1 特長

- ・ パワーオン・リセット(POR)ジェネレータを搭載、遅延時間を40 μ s～30sの範囲で変更可能
- ・ 非常に低い静止電流: 2.1 μ A (標準値)
- ・ 高いスレッシュホールド精度: 1% (最大値)
- ・ 高精度のヒステリシス
- ・ 固定および可変のスレッシュホールド電圧
 - 標準レールの固定スレッシュホールド:
1.2V～3.3V
 - 最低1.15Vまで調整可能
- ・ マニュアル・リセット(MR)入力
- ・ オープン・ドレインRESET出力
- ・ 温度範囲: -40 $^{\circ}$ C～+125 $^{\circ}$ C
- ・ パッケージ: 1.5mm×1.5mm WSON

2 アプリケーション

- ・ DSPまたはマイクロコントローラ
- ・ FPGAおよびASIC
- ・ ノートブックおよびデスクトップ・コンピュータ
- ・ スマートフォン、ハンドヘルド製品
- ・ 携帯用のバッテリー駆動製品
- ・ ソリッドステート・ドライブ
- ・ セットトップ・ボックス
- ・ 産業用制御システム

3 概要

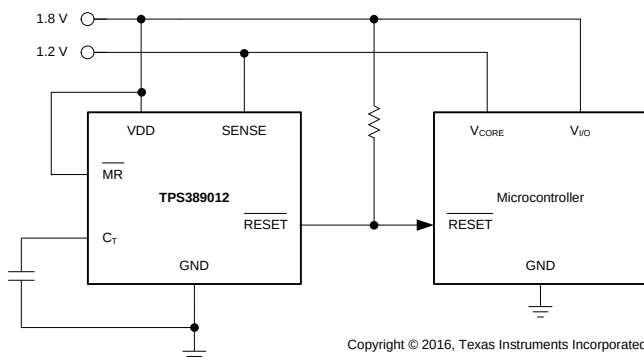
TPS3890は高精度の電圧スーパーバイザで、静止電流が低く、最低1.15Vのシステム電圧を監視でき、SENSE電圧がプリセットされたスレッシュホールドより低下したとき、またはマニュアル・リセット(MR)ピンが論理LOWに低下したとき、オープン・ドレインのRESET信号をアサートします。RESET出力は、SENSE電圧とマニュアル・リセット(MR)がそれぞれのスレッシュホールド以上に復帰した後も、ユーザーが設定した遅延時間だけLOWに維持されます。TPS3890ファミリは、高精度の基準電圧を使用して、1%のスレッシュホールド精度を実現しています。リセットの遅延時間は、CTピンを外付けのコンデンサへ接続することで、40 μ s～30sの範囲に設定できます。TPS3890は静止電流が2.1 μ Aと非常に低く、小形の1.5mm×1.5mmパッケージで供給されるため、バッテリー駆動および実装面積の制限されるアプリケーションに適しています。このデバイスは、-40 $^{\circ}$ C～+125 $^{\circ}$ Cの温度範囲(T_J)にわたって完全に動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS3890	WSON (6)	1.50mm×1.50mm

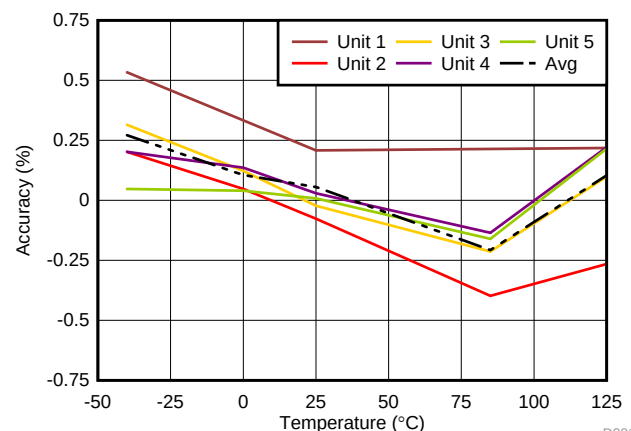
(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



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V_{ITN}の精度と温度との関係



D001



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年3月発行のものから更新

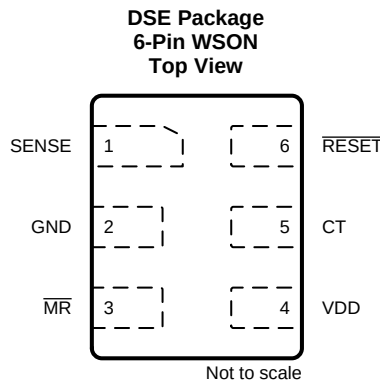
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5 Device Comparison Table

PART NUMBER	NOMINAL SUPPLY VOLTAGE	NEGATIVE THRESHOLD (V _{ITN})	POSITIVE THRESHOLD (V _{ITP})
TPS389001	Adjustable	1.15 V	1.157 V
TPS389012	1.2 V	1.15 V	1.157 V
TPS389015	1.5 V	1.44 V	1.449 V
TPS389018	1.8 V	1.73 V	1.740 V
TPS389020	2.0 V	1.90 V	1.911 V
TPS389025	2.5 V	2.40 V	2.414 V
TPS389030	3.0 V	2.89 V	2.907 V
TPS389033	3.3 V	3.17 V	3.189 V

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
5	CT	—	The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the RESET delay time to deassert. $t_{PD(r)} \text{ (sec)} = C_{CT} \text{ (}\mu\text{F)} \times 1.07 + 25 \mu\text{s (nom)}$.
2	GND	—	Ground
3	MR	I	Driving the manual reset pin (MR) low causes RESET to go low (assert).
6	RESET	O	RESET is an open-drain output that is driven to a low-impedance state when either the MR pin is driven to a logic low or the monitored voltage on the SENSE pin is lower than the negative threshold voltage (V _{ITN}). RESET remains low (asserted) for the delay time period after both MR is set to a logic high and the SENSE input is above V _{ITP} . A pullup resistor from 10 kΩ to 1 MΩ can be used on this pin.
1	SENSE	I	This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage V _{ITN} , RESET goes low (asserts). When the voltage on SENSE rises above the positive threshold voltage V _{ITP} , RESET goes high (deasserts).
4	VDD	I	Supply voltage pin. Good analog design practice is to place a 0.1-μF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	VDD	−0.3	7	V
	SENSE	−0.3	7	
	RESET	−0.3	7	
	MR	−0.3	7	
	V _{CT}	−0.3	7	
Current	RESET	−20	20	mA
Temperature	Operating junction temperature, T _J	−40	125	°C
	Storage temperature, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Power-supply voltage	1.5		5.5	V
V _{SENSE}	SENSE voltage	0		5.5	V
V _{RESET}	RESET pin voltage	0		5.5	V
I _{RESET}	RESET pin current	−5		5	mA
C _{IN}	Input capacitor, VDD pin	0	0.1		μF
C _{CT}	Reset timeout capacitor, CT pin	0		22	μF
R _{PU}	Pullup resistor, RESET pin	1		1000	kΩ
T _J	Junction temperature (free-air temperature)	−40	25	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3890	UNIT
		DSE (WSN)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	321.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	207.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	281.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	42.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	284.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	142.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over the operating junction temperature range of -40°C to $+125^{\circ}\text{C}$, $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, and $\overline{\text{MR}} = V_{\text{DD}}$ (unless otherwise noted); typical values are at $V_{\text{DD}} = 5.5\text{ V}$ and $T_{\text{J}} = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply voltage		1.5		5.5	V
V_{POR}	Power-on reset voltage	$V_{\text{OL(max)}} = 0.2\text{ V}$, $I_{\text{RESET}} = 15\text{ }\mu\text{A}$			0.8	V
I_{DD}	Supply current (into VDD pin)	$V_{\text{DD}} = 3.3\text{ V}$, $I_{\text{RESET}} = 0\text{ mA}$, $-40^{\circ}\text{C} < T_{\text{J}} < 85^{\circ}\text{C}$		2.09	3.72	μA
		$V_{\text{DD}} = 3.3\text{ V}$, $I_{\text{RESET}} = 0\text{ mA}$, $-40^{\circ}\text{C} < T_{\text{J}} < 105^{\circ}\text{C}$			4.5	
		$V_{\text{DD}} = 3.3\text{ V}$, $I_{\text{RESET}} = 0\text{ mA}$			5.8	
		$V_{\text{DD}} = 5.5\text{ V}$, $I_{\text{RESET}} = 0\text{ mA}$, $-40^{\circ}\text{C} < T_{\text{J}} < 85^{\circ}\text{C}$		2.29	4	
		$V_{\text{DD}} = 5.5\text{ V}$, $I_{\text{RESET}} = 0\text{ mA}$, $-40^{\circ}\text{C} < T_{\text{J}} < 105^{\circ}\text{C}$			5.2	
		$V_{\text{DD}} = 5.5\text{ V}$, $I_{\text{RESET}} = 0\text{ mA}$			6.5	
V_{ITN} , V_{ITP}	SENSE input threshold voltage accuracy		-1%	$\pm 0.5\%$	1%	
V_{HYST}	Hysteresis ⁽¹⁾		0.325%	0.575%	0.825%	
I_{SENSE}	Input current	$V_{\text{SENSE}} = 5\text{ V}$			8	μA
		$V_{\text{SENSE}} = 5\text{ V}$, TPS389001, TPS389012		10	100	nA
I_{CT}	CT pin charge current		0.90	1.15	1.35	μA
V_{CT}	CT pin comparator threshold voltage		1.17	1.23	1.29	V
R_{CT}	CT pin pulldown resistance	When $\overline{\text{RESET}}$ is deasserted		200		Ω
V_{IL}	Low-level input voltage ($\overline{\text{MR}}$ pin)			$0.25 \times V_{\text{DD}}$		V
V_{IH}	High-level output voltage		$0.7 \times V_{\text{DD}}$			V
V_{OL}	Low-level output voltage	$V_{\text{DD}} \geq 1.5\text{ V}$, $I_{\text{RESET}} = 0.4\text{ mA}$			0.25	V
		$V_{\text{DD}} \geq 2.7\text{ V}$, $I_{\text{RESET}} = 2\text{ mA}$			0.25	
		$V_{\text{DD}} \geq 4.5\text{ V}$, $I_{\text{RESET}} = 3\text{ mA}$			0.3	
$I_{\text{LKG(OD)}}$	Open-drain output leakage	High impedance, $V_{\text{SENSE}} = V_{\text{RESET}} = 5.5\text{ V}$			250	nA

(1) $V_{\text{HYST}} = [(V_{\text{ITP}} - V_{\text{ITN}}) / V_{\text{ITN}}] \times 100\%$.

7.6 Timing Requirements

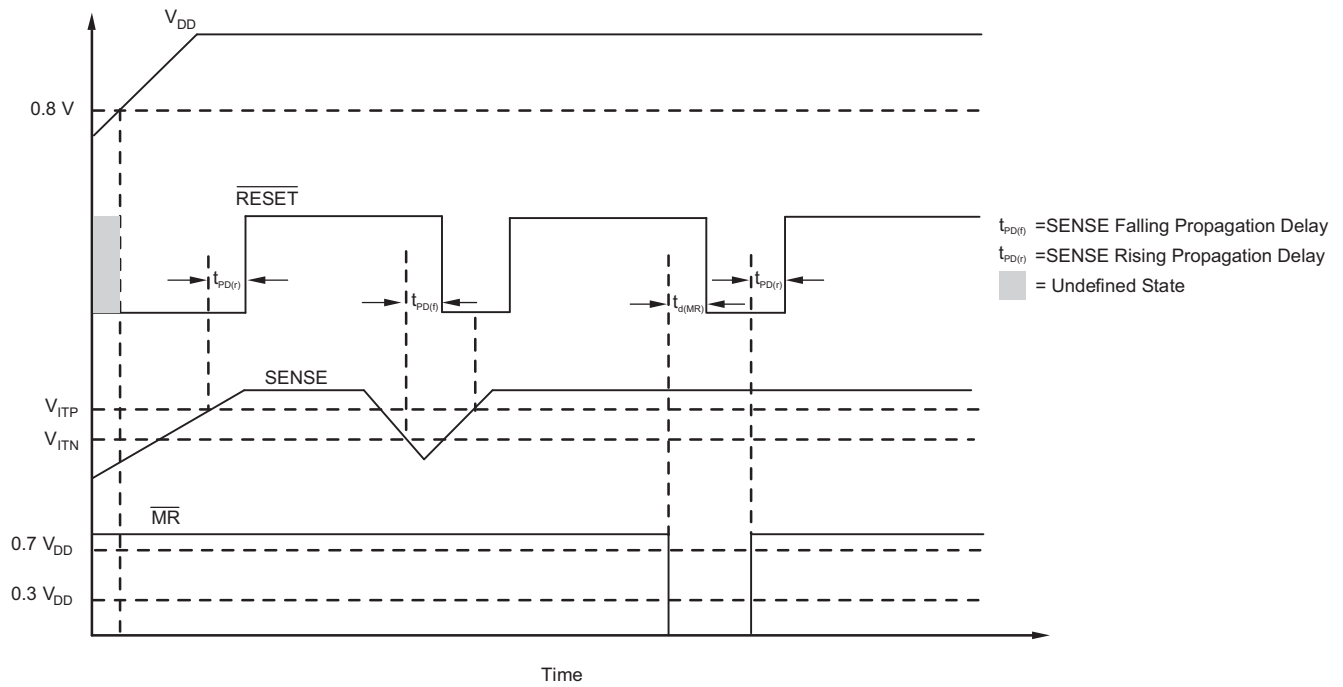
over the operating junction temperature range of -40°C to $+125^{\circ}\text{C}$, $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, $\overline{\text{MR}} = V_{\text{DD}}$, and 5% input overdrive⁽¹⁾ (unless otherwise noted); typical values are at $V_{\text{DD}} = 5.5\text{ V}$ and $T_{\text{J}} = 25^{\circ}\text{C}$

		MIN	NOM	MAX	UNIT
$t_{\text{PD(f)}}$	SENSE (falling) to $\overline{\text{RESET}}$ propagation delay	$C_{\text{T}} = \text{open}$, $V_{\text{DD}} = 3.3\text{ V}$	18		μs
		$C_{\text{T}} = \text{open}$, $V_{\text{DD}} = 5.5\text{ V}$	8		
$t_{\text{PD(r)}}$	SENSE (rising) to $\overline{\text{RESET}}$ propagation delay	$C_{\text{T}} = \text{open}$, $V_{\text{DD}} = 3.3\text{ V}$	25		μs
$t_{\text{GI(SENSE)}}$	SENSE pin glitch immunity	$V_{\text{DD}} = 5.5\text{ V}$	9		μs
$t_{\text{GI(MR)}}$	$\overline{\text{MR}}$ pin glitch immunity	$V_{\text{DD}} = 5.5\text{ V}$	100		ns
t_{MRW}	$\overline{\text{MR}}$ pin pulse duration to assert $\overline{\text{RESET}}$	1			μs
$t_{\text{d(MR)}}$	$\overline{\text{MR}}$ pin low to out delay		250		ns
t_{STRT}	Startup delay		325		μs

(1) Overdrive = $| (V_{\text{IN}} / V_{\text{THRESH}} - 1) \times 100\% |$.

TPS3890

JAJST5A – MARCH 2016 – REVISED MAY 2016

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1. Timing Diagram

7.7 Typical Characteristics

over the operating junction temperature range of -40°C to $+125^{\circ}\text{C}$, $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, and $\overline{\text{MR}} = V_{\text{DD}}$ (unless otherwise noted)

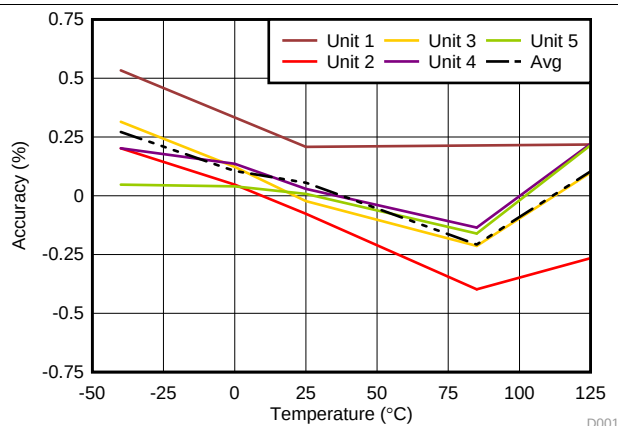


Figure 2. V_{ITN} Accuracy vs Temperature

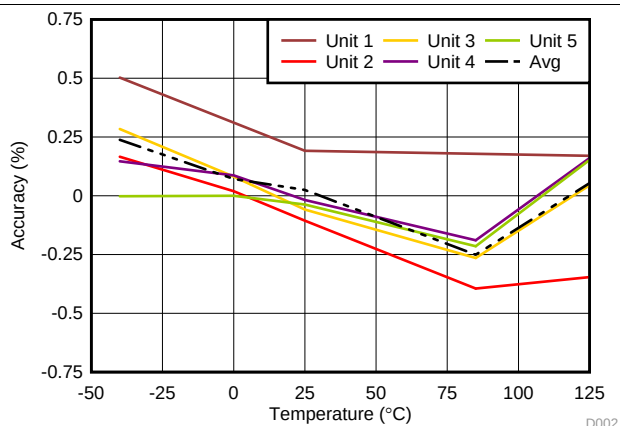
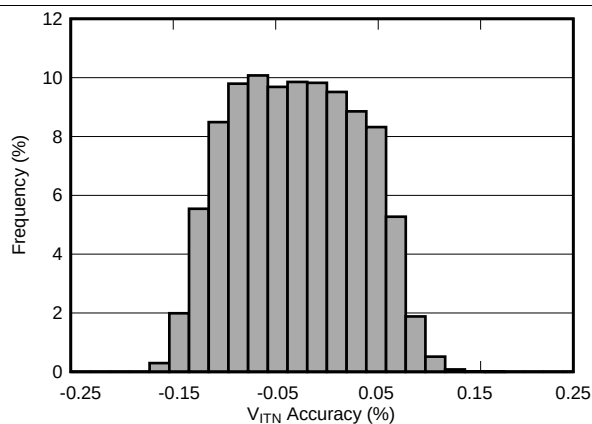
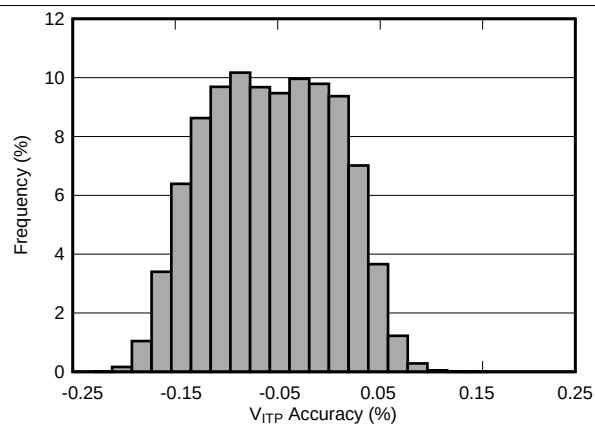


Figure 3. V_{ITP} Accuracy vs Temperature



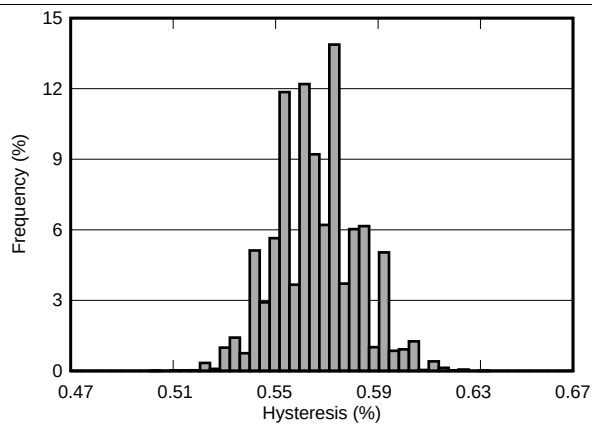
Tested at $V_{\text{DD}} = 1.5\text{ V}$ and $V_{\text{DD}} = 5.5\text{ V}$, total tests = 136,348

Figure 4. V_{ITN} Accuracy Histogram



Tested at $V_{\text{DD}} = 1.5\text{ V}$ and $V_{\text{DD}} = 5.5\text{ V}$, total tests = 136,348

Figure 5. V_{ITP} Accuracy Histogram



Tested at $V_{\text{DD}} = 1.5\text{ V}$ and $V_{\text{DD}} = 5.5\text{ V}$, total tests = 136,348

Figure 6. Hysteresis Histogram

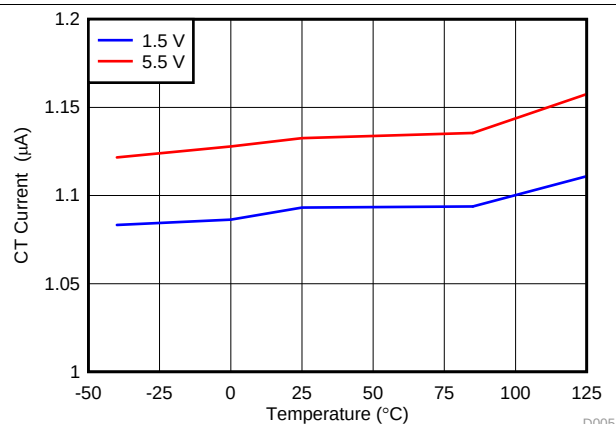


Figure 7. CT Current vs Temperature

Typical Characteristics (continued)

over the operating junction temperature range of -40°C to $+125^{\circ}\text{C}$, $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, and $\overline{\text{MR}} = V_{\text{DD}}$ (unless otherwise noted)

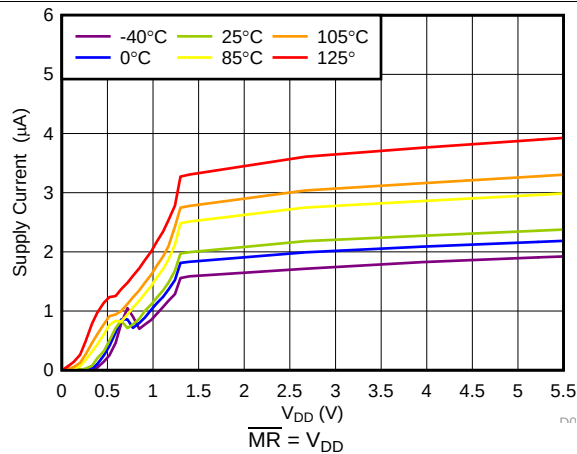


FIG 8. Supply Current vs Power-Supply Voltage

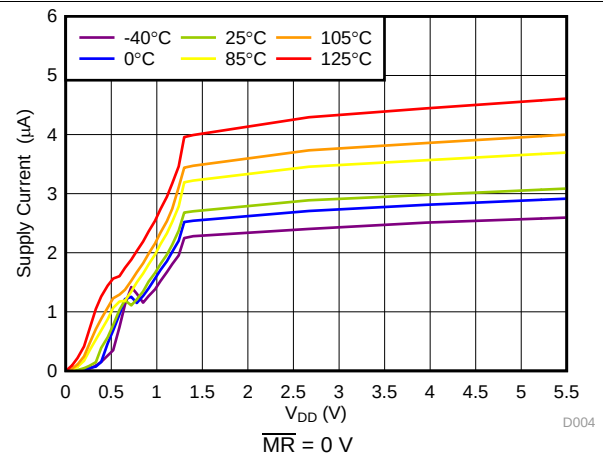


FIG 9. Supply Current vs Power-Supply Voltage

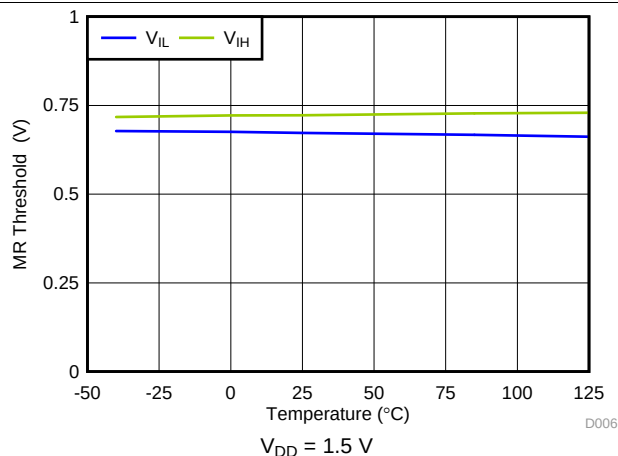


FIG 10. $\overline{\text{MR}}$ Threshold vs Temperature

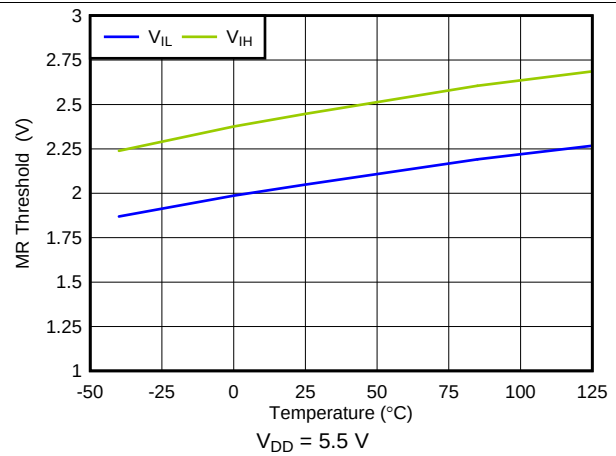


FIG 11. $\overline{\text{MR}}$ Threshold vs Temperature

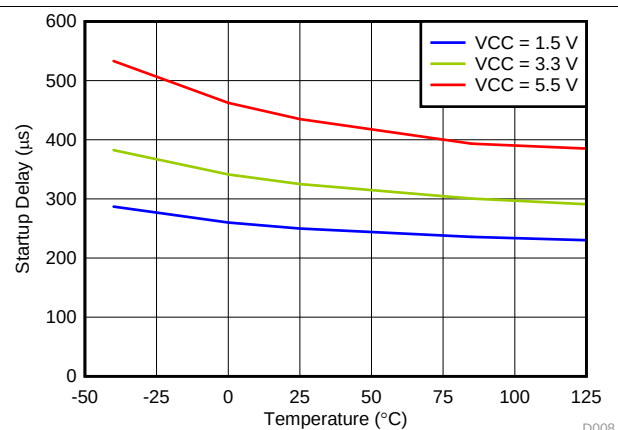


FIG 12. Startup Delay vs Temperature

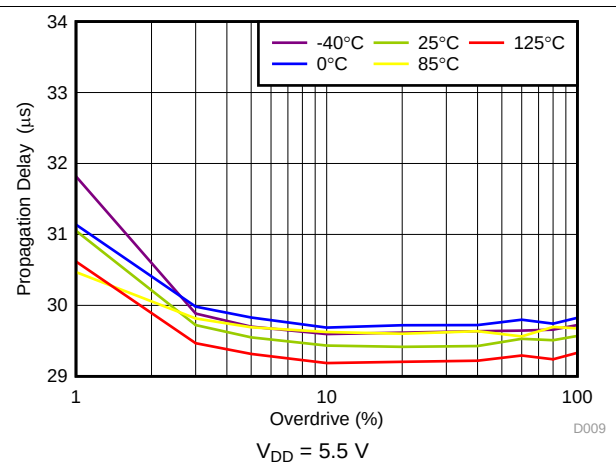


FIG 13. Propagation Delay ($t_{\text{PD}(r)}$) vs Overdrive

Typical Characteristics (continued)

over the operating junction temperature range of -40°C to $+125^{\circ}\text{C}$, $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, and $\overline{\text{MR}} = V_{\text{DD}}$ (unless otherwise noted)

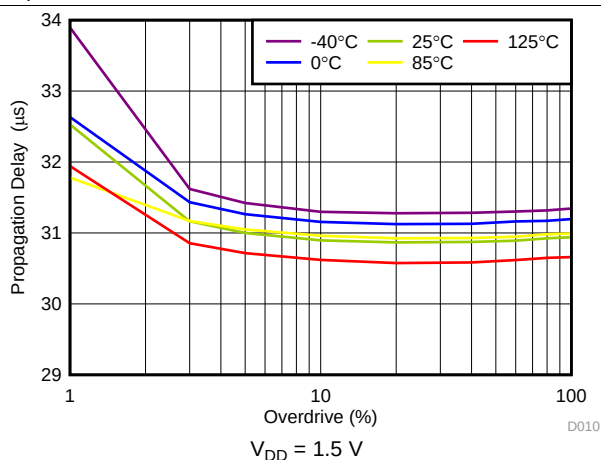


Figure 14. Propagation Delay ($t_{\text{PD}(n)}$) vs Overdrive

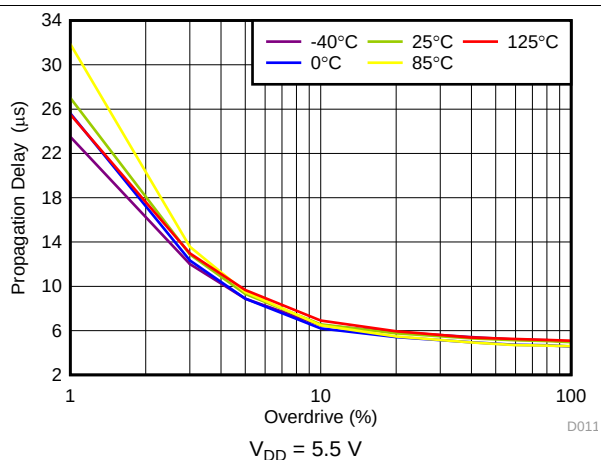


Figure 15. Propagation Delay ($t_{\text{PD}(n)}$) vs Overdrive

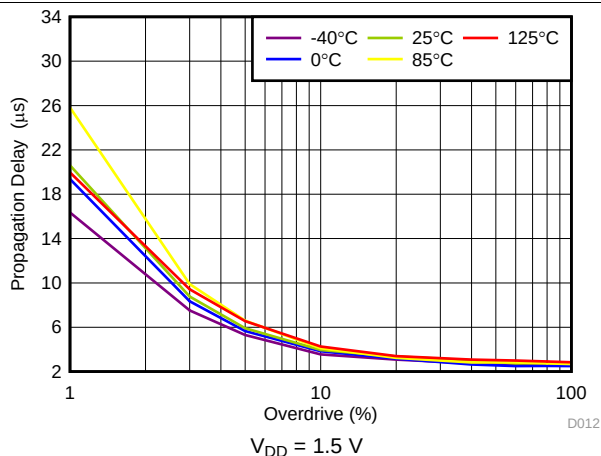


Figure 16. Propagation Delay ($t_{\text{PD}(n)}$) vs Overdrive

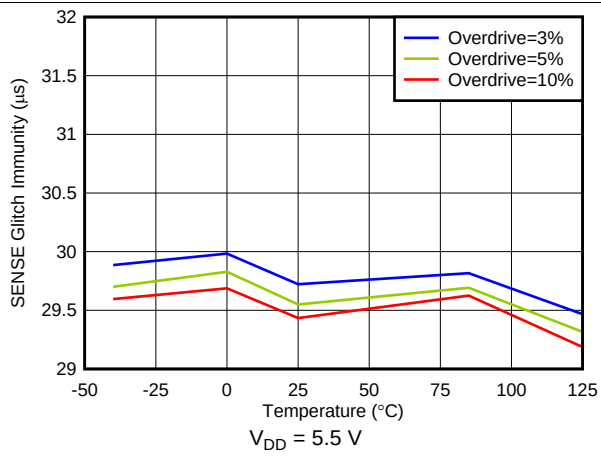


Figure 17. Low-to-High Glitch Immunity vs Temperature

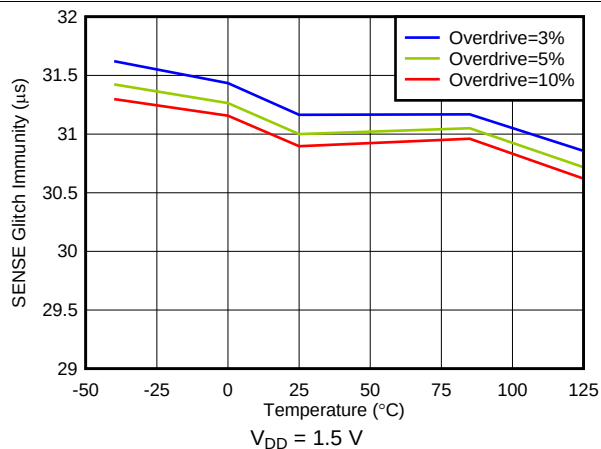


Figure 18. Low-to-High Glitch Immunity vs Temperature

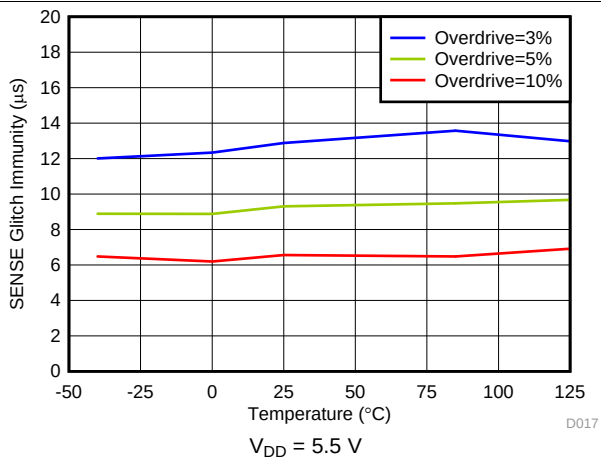


Figure 19. High-to-Low Glitch Immunity vs Temperature

Typical Characteristics (continued)

over the operating junction temperature range of -40°C to $+125^{\circ}\text{C}$, $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, and $\overline{\text{MR}} = V_{\text{DD}}$ (unless otherwise noted)

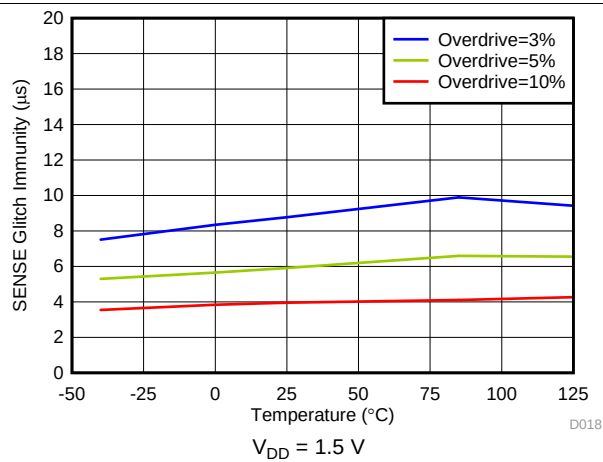


Figure 20. High-to-Low Glitch Immunity vs Temperature

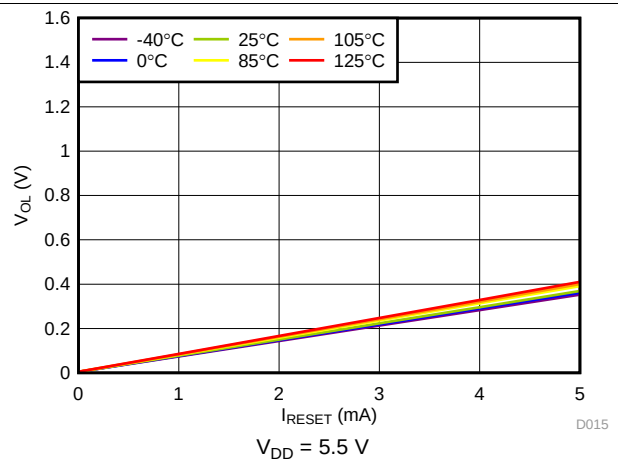


Figure 21. Low-Level Output Voltage vs RESET Current

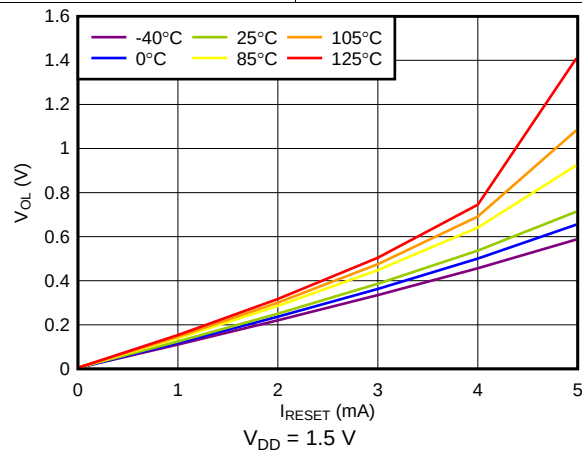


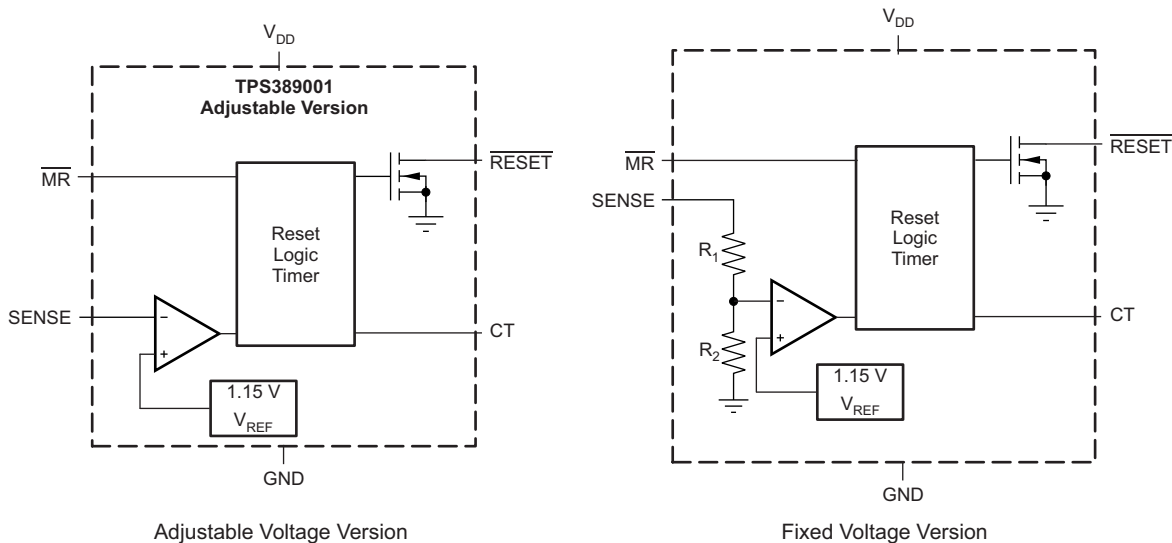
Figure 22. Low-Level Output Voltage vs RESET Current

8 Detailed Description

8.1 Overview

The TPS3890 supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{ITN} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above their respective thresholds.

8.2 Functional Block Diagram



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8.3 Feature Description

The combination of user-adjustable reset delay time with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages (V_{ITN}) can be factory set from 1.15 V to 3.17 V (see the [Device Comparison Table](#) for available options), and the adjustable device can be used to customize the threshold voltage for other application needs by using an external resistor divider. The CT pin allows the reset delay to be set between 25 μs and 30 s with the use of an external capacitor.

8.3.1 User-Configurable $\overline{\text{RESET}}$ Delay Time

The rising $\overline{\text{RESET}}$ delay time ($t_{\text{PD}(r)}$) can be configured by installing a capacitor connected to the CT pin. The TPS3890 uses a CT pin charging current (I_{CT}) of 1.15 μA to help counter the effect of capacitor and board-level leakage currents that can be substantial in certain applications. The rising $\overline{\text{RESET}}$ delay time can be set to any value between 25 μs (no C_{CT} installed) and 30 s ($C_{\text{CT}} = 26 \mu\text{F}$).

The capacitor value needed for a given delay time can be calculated using [式 1](#):

$$t_{\text{PD}(r)} (\text{sec}) = C_{\text{CT}} \times V_{\text{CT}} \div I_{\text{CT}} + t_{\text{PD}(r)(\text{nom})} \quad (1)$$

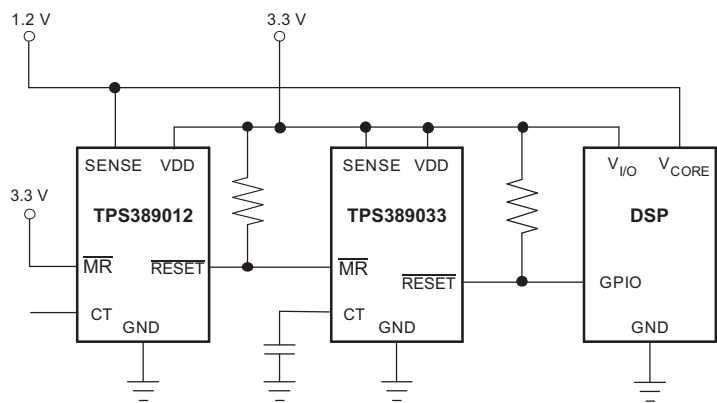
The slope of [式 1](#) is determined by the time that the CT charging current (I_{CT}) takes to charge the external capacitor up to the CT comparator threshold voltage (V_{CT}). When $\overline{\text{RESET}}$ is asserted, the capacitor is discharged through the internal CT pulldown resistor (R_{CT}). When the $\overline{\text{RESET}}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor and when the voltage on this capacitor reaches 1.22 V, $\overline{\text{RESET}}$ is deasserted. Note that in order to minimize the difference between the calculated $\overline{\text{RESET}}$ delay time and the actual $\overline{\text{RESET}}$ delay time, use a low-leakage type capacitor (such as a ceramic capacitor) and minimize parasitic board capacitance around this pin.

Feature Description (continued)

8.3.2 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above V_{ITP} , $\overline{\text{RESET}}$ is deasserted after the user-defined reset delay. If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ must be connected to V_{DD} . Note that if the logic signal driving $\overline{\text{MR}}$ is not greater than or equal to V_{DD} , then some additional current flows into V_{DD} and out of $\overline{\text{MR}}$ and the difference is apparent when comparing [Figure 8](#) and [Figure 9](#).

[Figure 23](#) shows how $\overline{\text{MR}}$ can be used to monitor multiple system voltages when only a single CT capacitor is needed to set the $\overline{\text{RESET}}$ delay time.



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Figure 23. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages

8.3.3 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$ remains high (deasserted) as long as SENSE is above the positive threshold (V_{ITP}) and the manual reset signal ($\overline{\text{MR}}$) is logic high. If SENSE falls below the negative threshold (V_{ITN}) or if $\overline{\text{MR}}$ is driven low, then $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

When $\overline{\text{MR}}$ is again logic high and SENSE is above V_{ITP} , a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period ($t_{\text{PD}(f)}$). When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{\text{RESET}}$ can be pulled up to any voltage up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL} , the output capacitive loading, and the output leakage current ($I_{\text{LKG(OD)}}$).

8.3.4 SENSE Input

The SENSE input can vary from ground to 5.5 V (7.0 V, absolute maximum), regardless of the device supply voltage used. The SENSE pin is used to monitor the critical voltage rail. If the voltage on this pin drops below V_{ITN} , then $\overline{\text{RESET}}$ is asserted. When the voltage on the SENSE pin exceeds the positive threshold voltage, $\overline{\text{RESET}}$ deasserts after the user-defined $\overline{\text{RESET}}$ delay time.

The internal comparator has built-in hysteresis to ensure well-defined $\overline{\text{RESET}}$ assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3890 device is relatively immune to short transients on the SENSE pin. Glitch immunity is dependent on threshold overdrive, as illustrated in [Figure 19](#) for V_{ITN} and [Figure 18](#) for V_{ITP} . Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

Feature Description (continued)

The adjustable version (TPS389001) can be used to monitor any voltage rail down to 1.15 V using the circuit shown in [Figure 24](#).

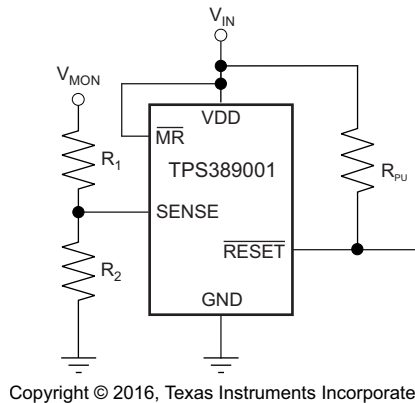


Figure 24. Using the TPS389001 to Monitor a User-Defined Threshold Voltage

The target threshold voltage for the monitored supply ($V_{ITX(MON)}$) and the resistor divider values can be calculated by using [Equation 2](#) and [Equation 3](#), respectively:

$$V_{ITX(MON)} = V_{ITX} \times (1 + R_1 \div R_2) \quad (2)$$

[Equation 3](#) can be used to calculate either the negative threshold or the positive threshold by replacing V_{ITX} with either V_{ITN} or V_{ITP} , respectively.

$$R_{TOTAL} = R_1 + R_2 \quad (3)$$

Resistors with high values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an R_{TOTAL} value so that the current through the resistor divider is at least 100 times larger than the SENSE input current is simplest. See application report *Optimizing Resistor Dividers at a Comparator Input* ([SLVA450](#)) for more details on sizing input resistors.

8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3702 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (that is, undervoltage and overvoltage). Threshold overdrive is calculated as a percent of the threshold in question, as shown in [Equation 4](#).

$$\text{Overdrive} = | (V_{SENSE} / V_{ITX} - 1) \times 100\% | \quad (4)$$

[Figure 17](#) to [Figure 20](#) illustrate the glitch immunity that the TPS3890 has versus temperature with three different overdrive voltages. The propagation delay versus overdrive curves ([Figure 13](#) to [Figure 16](#)) can be used to determine how sensitive the TPS3890 family of devices are across an even wider range of overdrive voltages.

8.4 Device Functional Modes

表 1 summarizes the various functional modes of the device.

表 1. Truth Table

V_{DD}	$\overline{MR}$	SENSE	$\overline{RESET}$
$V_{DD} < V_{POR}$	—	—	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}^{(1)}$	—	—	L
$V_{DD} \geq V_{DD(MIN)}$	L	—	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} < V_{ITN}$	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} > V_{ITP}$	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{RESET}$ is held low until V_{DD} falls below V_{POR} .

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by the voltage on the SENSE pin and the logic state of $\overline{MR}$.

- $\overline{MR}$ high: when the voltage on V_{DD} is greater than 1.5 V, the $\overline{RESET}$ signal corresponds to the voltage on the SENSE pin relative to the threshold voltage.
- $\overline{MR}$ low: in this mode, $\overline{RESET}$ is held low regardless of the voltage on the SENSE pin.

8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than V_{POR} , the device does not have enough voltage to internally pull the asserted output low and $\overline{RESET}$ is undefined and must not be relied upon for proper device function.

9 Application and Implementation

注

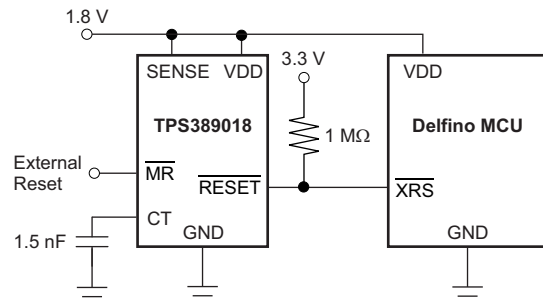
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

A typical application for the TPS389018 is shown in [Figure 25](#). The TPS389018 can be used to monitor the 1.8-V VDD rail required by the TI Delfino™ microprocessor family. The open-drain RESET output of the TPS389018 is connected to the XRS input of the microprocessor. A reset event is initiated when the VDD voltage is less than V_{ITN} or when MR is driven low by an external source.



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Figure 25. TPS3890 Monitoring the Supply Voltage for a Delfino Microprocessor

9.2.1 Design Requirements

The TPS3890 RESET output can be used to drive the reset (XRS) input of a microprocessor. The RESET pin of the TPS3890 is pulled high with a 1-MΩ resistor; the reset delay time is controlled by the CT capacitor and is set depending on the reset requirement times of the microprocessor. During power-up, XRS must remain low for at least 1 ms after VDD reaches 1.5 V for the C2000™ Delfino family of microprocessors. For 100-MHz operation, the Delfino TMS320F2833x microcontroller uses a supply voltage of 1.8 V that must be monitored by the TPS3890.

9.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS389018 has a negative threshold of 1.73 V and a positive threshold of 1.74 V, making the device suitable for monitoring a 1.8-V rail. The secondary constraint for this application is the reset delay time that must be at least 1 ms to allow the Delfino microprocessor enough time to startup up correctly. Because a minimum time is required, the worst-case scenario is a supervisor with a high CT charging current (I_{CT}) and a low CT comparator threshold (V_{CT}). For applications with ambient temperatures ranging from -40°C to $+125^{\circ}\text{C}$, C_{CT} can be calculated using $I_{CT(\text{Max})}$, $V_{CT(\text{Min})}$, and solving for C_{CT} in [Equation 1](#) such that the minimum capacitance required at the CT pin is 1.149 nF. If standard capacitors with $\pm 20\%$ tolerances are used, then the CT capacitor must be 1.5 nF or larger to ensure that the 1-ms delay time is met.

A 0.1-μF decoupling capacitor is connected to the VDD pin as a good analog design practice and a 1-MΩ resistor is used as the RESET pullup resistor to minimize the current consumption when RESET is asserted. The MR pin can be connected to an external signal if desired or connected to VDD if not used.

Typical Application (continued)

9.2.3 Application Curve

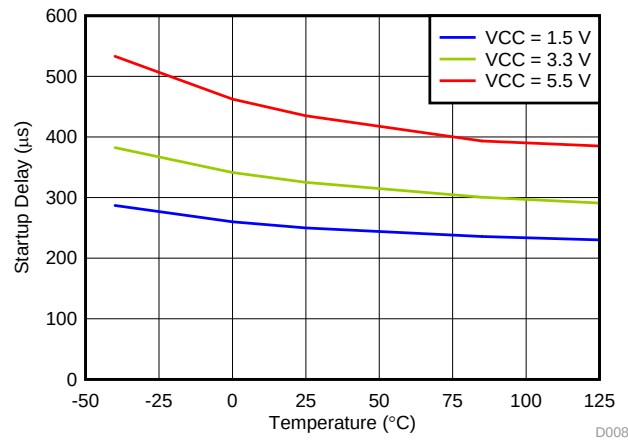


Figure 26. Startup Delay vs Temperature

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-μF capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

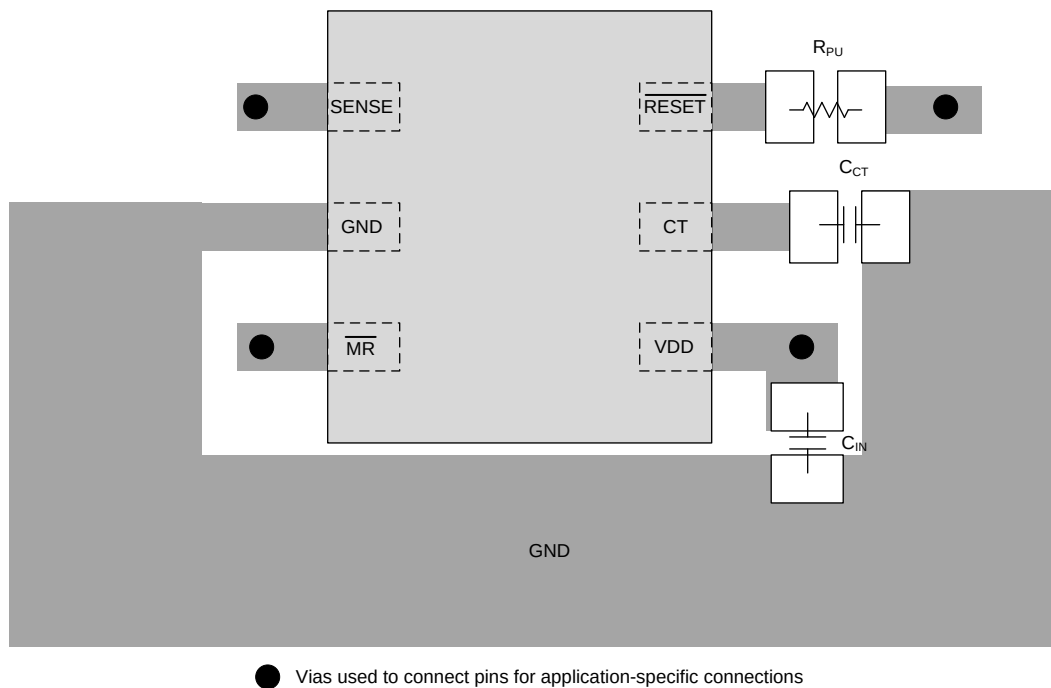
11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1- μ F ceramic capacitor near the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the RESET delay time is not adversely affected.

11.2 Layout Example

The layout example in shows how the TPS3890 is laid out on a printed circuit board (PCB) with a user-defined delay.



27. Recommended Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

以下に示す関連ドキュメントは、www.ti.comからダウンロードできます。

- 『コンパレータ入力における分割抵抗の最適化』、[SLVA450](#)
- 『電源設計用の感度分析』、[SLVA481](#)
- 『TMS320C28x デジタル信号コントローラの基礎』、[SPRAAM0](#)
- 『TPS3890EVM-775 評価モジュール・ユーザー・ガイド』、[SBVU030](#)
- 『C2000 Delfino ファミリのマイクロプロセッサ』
- 『TMS320F2833x マイクロコントローラ』、[SPRS439](#)

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商標

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12.4 静電気放電に関する注意事項



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12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS389001DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2V
TPS389001DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2V
TPS389001DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2V
TPS389001DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2V
TPS389012DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2W
TPS389012DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2W
TPS389012DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2W
TPS389012DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2W
TPS389015DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2X
TPS389015DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2X
TPS389015DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2X
TPS389015DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2X
TPS389018DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389018DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389018DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389018DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389020DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389020DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389020DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389020DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y
TPS389025DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Z
TPS389025DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Z
TPS389025DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Z
TPS389025DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Z
TPS389030DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3A
TPS389030DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3A
TPS389030DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3A
TPS389030DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3A
TPS389033DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3B

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS389033DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3B
TPS389033DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3B
TPS389033DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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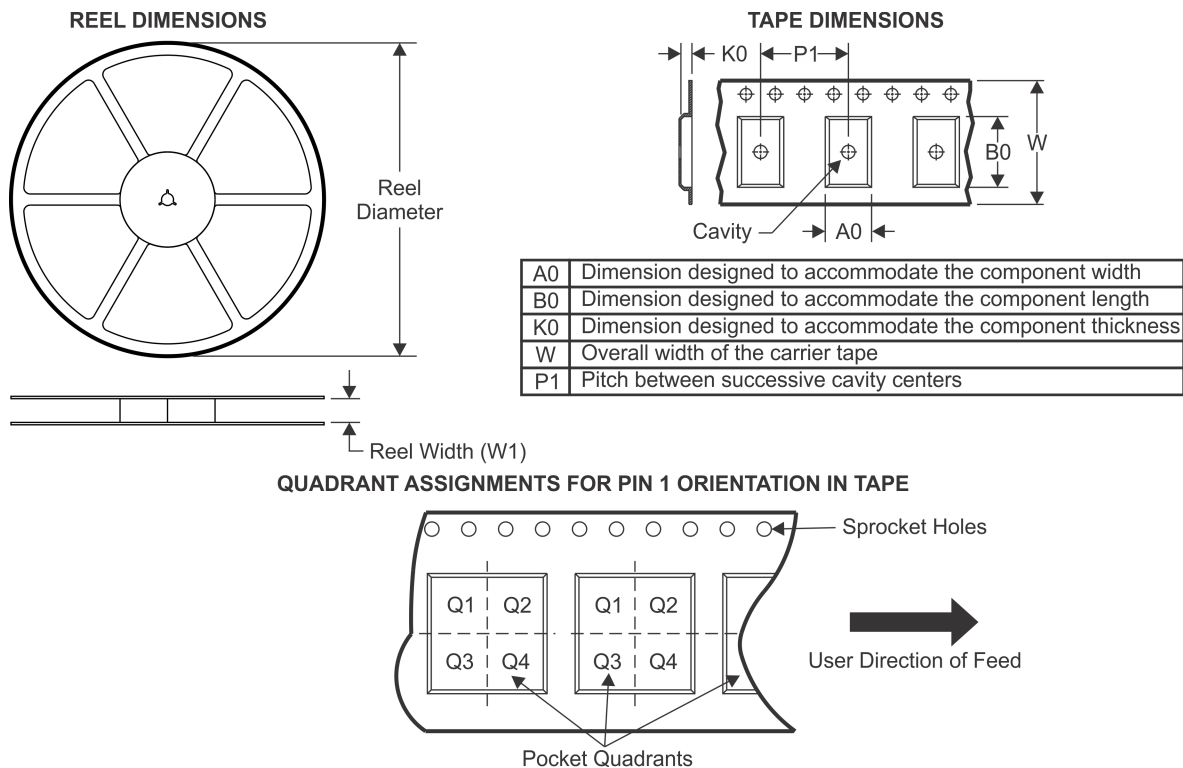
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3890 :

- Automotive : [TPS3890-Q1](#)

NOTE: Qualified Version Definitions:

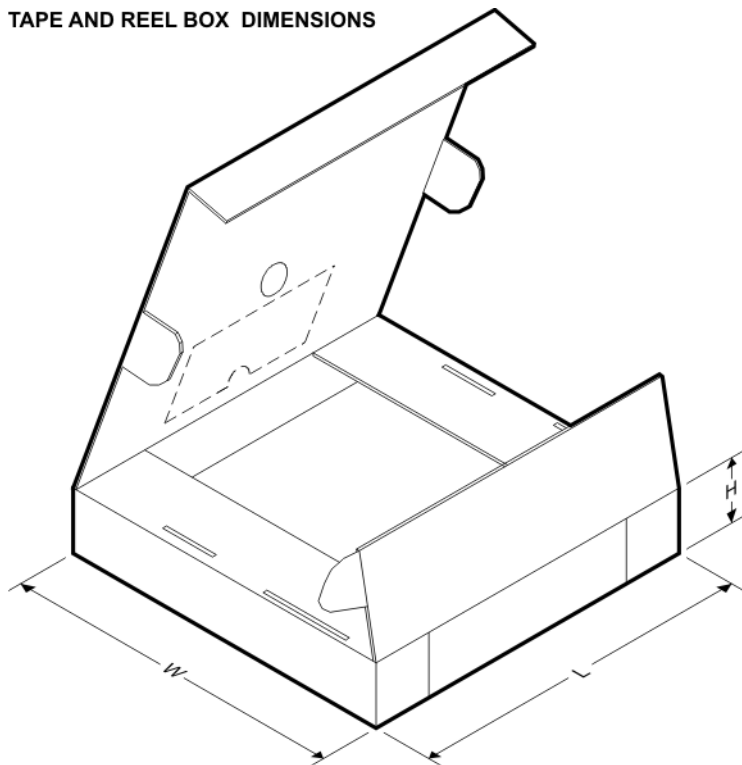
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

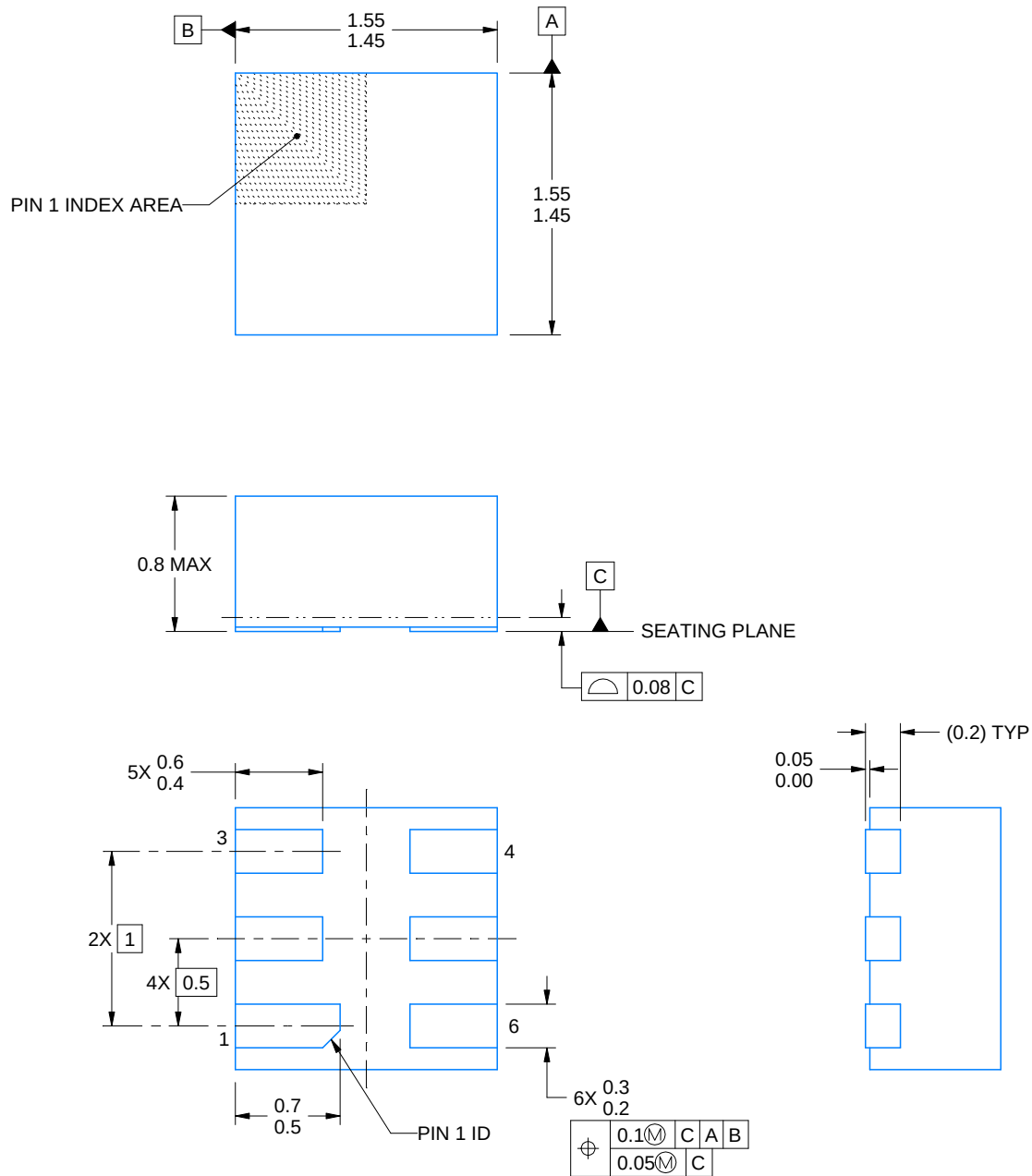
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS389001DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389001DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389012DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389012DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389015DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389015DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389018DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389018DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389020DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389020DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389025DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389025DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389030DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389030DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS389001DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389001DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389012DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389012DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389015DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389015DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389018DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389018DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389020DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389020DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389025DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389025DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389030DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389030DSET	WSN	DSE	6	250	183.0	183.0	20.0
TPS389033DSER	WSN	DSE	6	3000	183.0	183.0	20.0
TPS389033DSET	WSN	DSE	6	250	183.0	183.0	20.0



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NOTES:

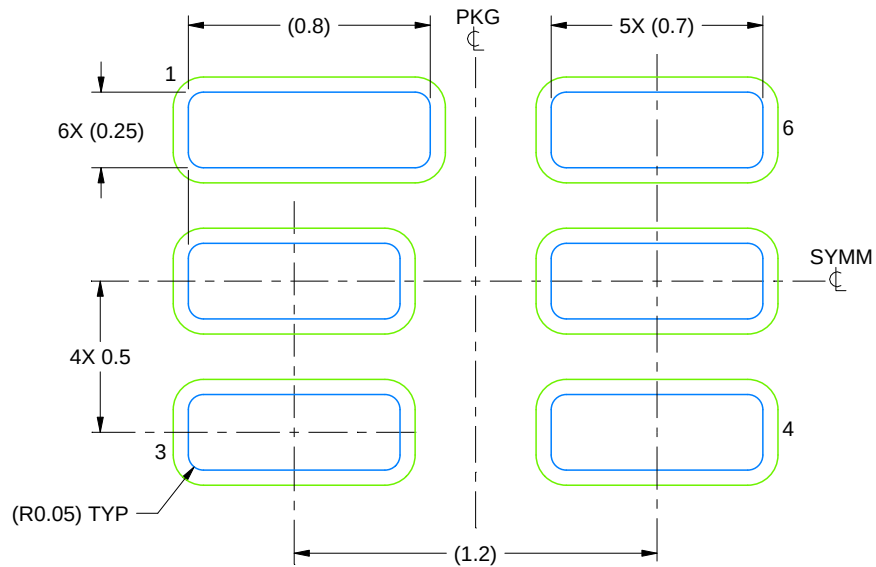
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

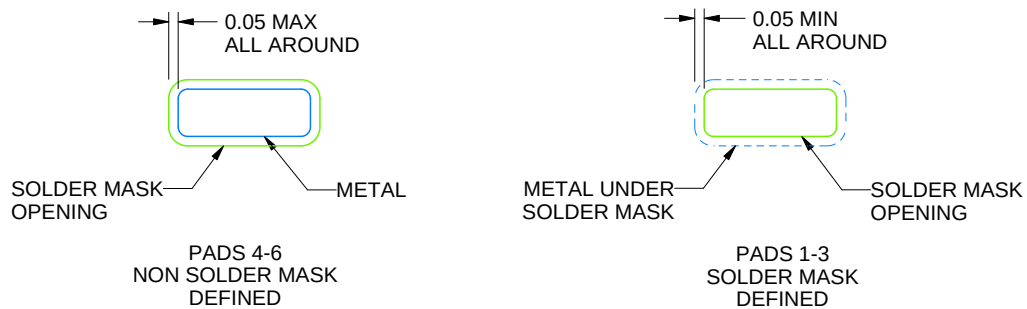
DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

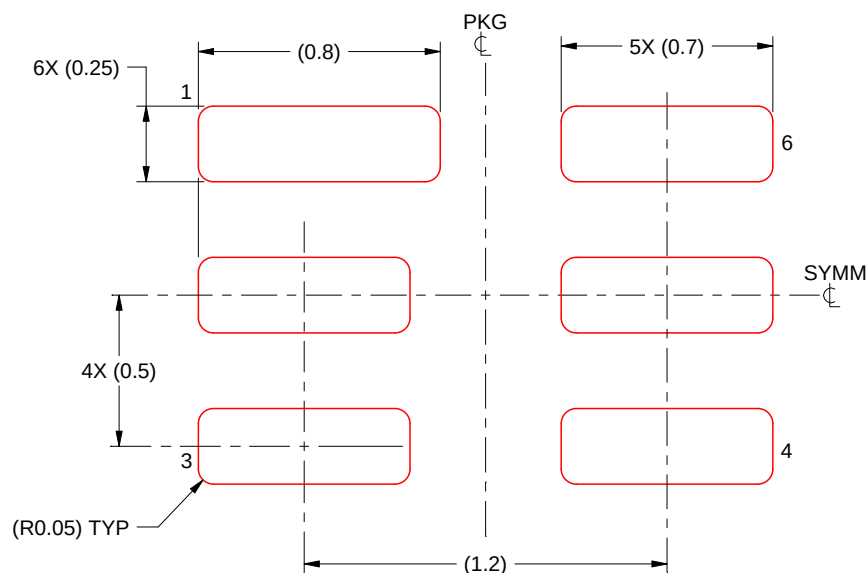
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月