# TPS40422 PMBus™ インターフェイスを備えたデュアル出力または二相同期整流降圧コントローラ

## 1 特長

- 単電源動作 4.5V～20V
- 出力電圧:0.6V～5.6V
- デュアル出力または二相同期整流降圧コントローラ
- PMBus™ インターフェイス機能
  - 2mV 刻みのマージン・アップまたはダウン
  - フォルト制限および応答をプログラム可能
  - 出力電圧、出力電流の監視
  - 2N3904 トランジスタによる外部温度の監視
  - UVLO オン / オフのスレッショルドをプログラム可能
  - ソフトスタート時間、ターンオン遅延、ターンオフ遅延をプログラム可能
- オンチップの NVM (不揮発性メモリ) にカスタム構成を保存
- 180° の位相差により入力リップルを低減
- 0℃～85℃で ±0.5% 精度の 600mV 基準電圧
- インダクタ DCR 電流センシング
- プログラマブルなスイッチング周波数:200kHz～1MHz
- 電圧モード制御、入力フィード・フォワード付き
- マルチフェーズ動作のための電流共有
- プリバイアス出力をサポート
- 差動リモート・センシング
- 外部との同期
- BPEXT ピンを使って外部バイアス電源スイッチ・オーバーをサポートすることで効率を向上
- OC、OV、UV、OT フォルト保護
- 40 ピン、6mm × 6mm、0.5mm ピッチの VQFN パッケージ
- 40 ピン、5mm × 5mm、0.4mm ピッチの WQFN パッケージ
- WEBENCH® Power Designer により、TPS40422 デバイスを使用するカスタム設計を作成

## 2 アプリケーション

- マルチ・レール・システム
- テレコム基地局
- スイッチャ / ルータ・ネットワーク
- サーバーおよびストレージ・システム

## 3 概要

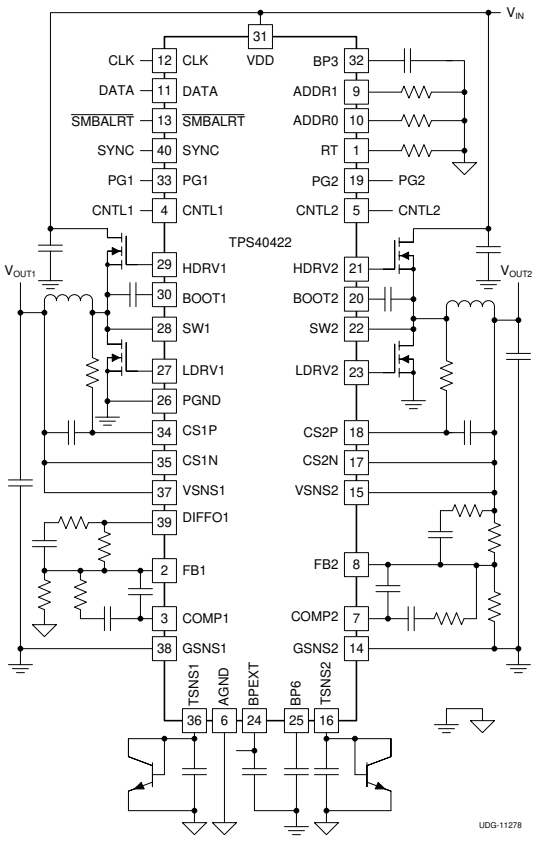
TPS40422 は 2 出力の PMBus プロトコル同期整流降圧コントローラです。本デバイスは、1 つの 2 相出力用に構成することもできます。

広い入力範囲は、5V と 12V の中間バスをサポートします。高精度の基準電圧は、最新 ASIC に供給するための高精度電圧の要件を満たしており、出力容量を低減できる可能性があります。電圧モード制御を使うと、ノイズ感度を低減でき、低デューティ比変換を確実に行うこともできます。

**製品情報**

| 部品番号 | パッケージ (1) | 本体サイズ (公称) |
|---|---|---|
| TPS40422 | VQFN (40) | 6.00mm × 6.00mm |
| | WQFN (40) | 5.00mm × 5.00mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**アプリケーション概略**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision F (January 2017) to Revision G (September 2022) | Page |
|---|---|
| • 文書全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • Added セクション 7.4 | 5 |

| Changes from Revision E (September 2016) to Revision F (January 2017) | Page |
|---|---|
| • 「*製品情報*」表に WQFN パッケージを追加 | 1 |
| • Added WQFN package drawing | 3 |

## 5 概要 (続き)

本デバイスのマージニング機能、基準電圧、フォルト制限値、UVLO スレッショルド、ソフトスタート時間、ターンオン遅延、ターンオフ遅延は、PMBus プロトコルを使って設定できます。

また、各チャネルの出力電圧、電流、温度を監視するため、高精度測定システムが実装されています。


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# 6 Pin Configuration and Functions

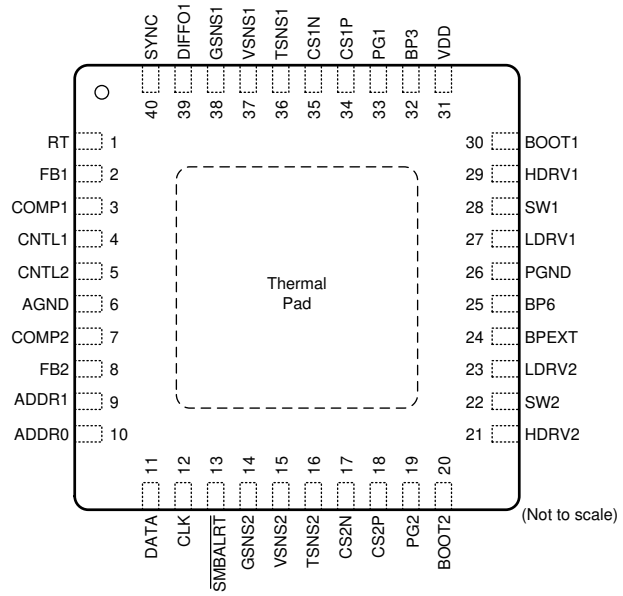



**図 6-1. RHA Package 40-Pin VQFN Top View**

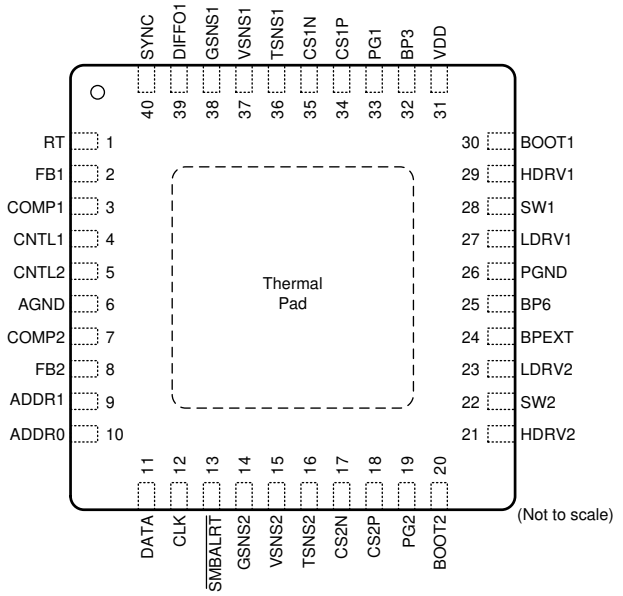



**図 6-2. RSB Package 40-Pin WQFN Top View**

**表 6-1. Pin Functions**

| PIN | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| ADDR0 | 10 | I | Low-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to AGND to select the low-order octal digit in the PMBus address. |
| ADDR1 | 9 | I | High-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to AGND to select the high-order octal digit in the PMBus address. |
| AGND | 6 | — | Low-noise ground connection to the controller. Connections should be arranged so that power level currents do not flow through the AGND path. |
| BOOT1 | 30 | I | Bootstrapped supply for the high-side FET driver for channel 1 (CH1). Connect a capacitor (100 nF typical) from BOOT1 to SW1 pin. |
| BOOT2 | 20 | I | Bootstrapped supply for the high-side FET driver for channel 2 (CH2). Connect a capacitor (100 nF typical) from BOOT2 to SW2 pin. |
| BP3 | 32 | O | Output bypass for the internal 3.3-V regulator. Connect a 100 nF or larger capacitor from this pin to AGND. The maximum suggested capacitor value is 10 µF. |
| BP6 | 25 | O | Output bypass for the internal 6.5-V regulator. Connect a low ESR, 1 µF or larger ceramic capacitor from this pin to PGND. The maximum suggested capacitor value is 10 µF. |
| BPEXT | 24 | I | External voltage input for BP6 switchover function. If the BPEXT function is not used, connect this pin to PGND via a 10-kΩ resistor. Otherwise connect a 100-nF or larger capacitor from this pin to PGND. The maximum suggested capacitor value is 10 µF. |
| CLK | 12 | I | Clock input for the PMBus interface. Pull up to 3.3 V with a resistor. |
| CNTL1 | 4 | I | Logic level input which controls startup and shutdown of CH1, determined by PMBus options. When floating, the pin is pulled up to BP6 by an internal 6-µA current source. |
| CNTL2 | 5 | I | Logic level input which controls startup and shutdown of CH2, determined by PMBus options. When floating, the pin is pulled up to BP6 by an internal 6-µA current source. |
| COMP1 | 3 | O | Output of the error amplifier for CH1 and connection node for loop feedback components. |
| COMP2 | 7 | O | Output of the error amplifier for CH2 and connection node for loop feedback components. For two-phase operation, use COMP1 for loop feedback and connect COMP1 to COMP2. |
| CS1N | 35 | I | Negative terminal of current sense amplifier for CH1. |
| CS2N | 17 | I | Negative terminal of current sense amplifier for CH2. |
| CS1P | 34 | I | Positive terminal of current sense amplifier for CH1. |

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**表 6-1. Pin Functions (continued)**

| PIN | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| CS2P | 18 | I | Positive terminal of current sense amplifier for CH2. |
| DATA | 11 | I/O | Data input/output for the PMBus interface. Pull up to 3.3 V with a resistor. |
| DIFFO1 | 39 | O | Output of the differential remote sense amplifier for CH1. |
| FB1 | 2 | I | Inverting input of the error amplifier for CH1. Connect a voltage divider to FB1 between DIFFO1 and AGND to program the output voltage for CH1. |
| FB2 | 8 | I | Inverting input of the error amplifier for CH2. Connect a voltage divider to FB2 between VOUT2 and GND to program the output for CH2. For two-phase operation, use FB1 to program the output voltage and connect FB2 to BP6 before applying voltage to VDD. |
| GSNS1 | 38 | I | Negative terminal of the differential remote sense amplifier for CH1. |
| GSNS2 | 14 | I | Negative terminal of the differential remote sense amplifier for CH2. |
| HDRV1 | 29 | O | Bootstrapped gate drive output for the high-side N-channel MOSFET for CH1. |
| HDRV2 | 21 | O | Bootstrapped gate drive output for the high-side N-channel MOSFET for CH2. |
| LDRV1 | 27 | O | Gate drive output for the low side synchronous rectifier N-channel MOSFET for CH1. |
| LDRV2 | 23 | O | Gate drive output for the low-side synchronous rectifier N-channel MOSFET for CH2. |
| PGND | 26 | — | Power GND. |
| PG1 | 33 | O | Open drain power good indicator for CH1 output voltage. |
| PG2 | 19 | O | Open drain power good indicator for CH2 output voltage. |
| RT | 1 | I | Frequency programming pin. Connect a resistor from this pin to AGND to set the oscillator frequency. |
| $\overline{\text{SMBALRT}}$ | 13 | O | Alert output for the PMBus interface. Pull up to 3.3 V with a resistor. |
| SW1 | 28 | I | Return of the high-side gate driver for CH1. Connect to the switched node for CH1. |
| SW2 | 22 | I | Return of the high-side gate driver for CH2. Connect to the switched node for CH2. |
| SYNC | 40 | I | Logic level input for external clock synchronization. When an external clock is applied to this pin, the controller oscillator is synchronized to the external clock and the switching frequency is one half of the external clock frequency. When an external clock is not used, tie this pin to AGND. |
| TSNS1 | 36 | I | External temperature sense input for CH1. |
| TSNS2 | 16 | I | External temperature sense input for CH2. |
| VDD | 31 | I | Power input to the controller. Connect a low ESR, 100 nF or larger ceramic capacitor from this pin to AGND. |
| VSNS1 | 37 | I | Positive terminal of the differential remote sense amplifier for CH1. |
| VSNS2 | 15 | I | Positive terminal of the differential remote sense amplifier for CH2. |


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage range(2) | VDD | –0.3 | 22 | V |
| | BOOT1 , BOOT2, HDRV1, HDRV2 | –0.3 | 30 | |
| | BOOT1 - SW1, BOOT2 - SW2 | –0.3 | 7 | |
| | CLK, DATA, SYNC | –0.3 | 5.5 | |
| | BPEXT, CNTL1, CNTL2, CS1N, CS2N, CS1P, CS2P, FB1, FB2, GSNS1, GSNS2, VSNS1, VSNS2 | –0.3 | 7 | |
| Output voltage range(3) | BP6, COMP1, COMP2, DIFFO1, LDRV1, LDRV2, PG1, PG2 | –0.3 | 7 | V |
| | $\overline{\text{SMBALRT}}$ | –0.3 | 5.5 | |
| | SW1, SW2 | –1 | 30 | |
| | ADDR0, ADDR1, BP3, RT, TSNS1, TSNS2 | –0.3 | 3.6 | |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin unless otherwise noted.
(3) Voltage values are with respect to the SW pin.

## 7.2 ESD Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –55 | 155 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 2 | | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 1.5 | | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD | Input operating voltage | 4.5 | 20 | V |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TPS40422 | | UNIT |
|---|---|---|---|---|
| | | RSB | RHA | |
| | | 40 PINS | 40 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 34.5 | 31.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 17.8 | 18.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 6.4 | 6.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 6.4 | 6.0 | °C/W |

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## 7.4 Thermal Information (continued)

| THERMAL METRIC(1) | | TPS40422 | | UNIT |
|---|---|---|---|---|
| | | RSB | RHA | |
| | | 40 PINS | 40 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.1 | 1.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 7.5 Electrical Characteristics

$T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{DD}$ = 12 V, $f_{SW}$ = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| $V_{VDD}$ | Input supply voltage range | | 4.5 | | 20 | V |
| $I_{VDD}$ | Input operating current | Switching, no driver load | | 18 | 25 | mA |
| | | Not switching | | 15 | 20 | |
| **UVLO** | | | | | | |
| $V_{IN(on)}$ | Input turn on voltage(2) | Default settings | | 4.25 | | V |
| $V_{IN(off)}$ | Input turn off voltage(2) | Default settings | | 4 | | V |
| $V_{INON(rng)}$ | Programmable range for turn on voltage | | 4.25 | | 16 | V |
| $V_{INOFF(rng)}$ | Programmable range for turn off voltage | | 4 | | 15.75 | V |
| $V_{IN\ ONOFF(acc)}$ | Turn on and turn off voltage accuracy(1) | 4.5 V ≤ $V_{VDD}$ ≤ 20 V, all VIN_ON and VIN_OFF settings | –5% | | 5% | |
| **ERROR AMPLIFIER** | | | | | | |
| $V_{FB}$ | Feedback pin voltage | 0°C ≤ $T_J$ ≤ 85°C | 597 | 600 | 603 | mV |
| | | –40°C ≤ $T_J$ ≤ 125°C | 594 | 600 | 606 | |
| $A_{OL}$ | Open-loop gain(1) | | 80 | | | dB |
| $G_{BWP}$ | Gain bandwidth product(1) | | | 24 | | MHz |
| $I_{FB}$ | FB pin bias current (out of pin) | $V_{FB}$ = 0.6 V | | | 50 | nA |
| $I_{COMP}$ | Sourcing | $V_{FB}$ = 0 V | 1 | 3 | | mA |
| | Sinking | $V_{FB}$ = 1 V | 3 | 9 | | |
| **BP6 REGULATOR** | | | | | | |
| $V_{BP6}$ | Output voltage | $I_{BP6}$ = 10 mA | 6.2 | 6.5 | 6.8 | V |
| | Dropout voltage | $V_{VIN}$ – $V_{BP6}$, $V_{VDD}$ = 4.5 V, $I_{BP6}$ = 25 mA | | 70 | 120 | mV |
| $I_{BP6}$ | Output current | $V_{VDD}$ = 12 V | 120 | | | mA |
| $V_{BP6UV}$ | Regulator UVLO voltage(1) | | 3.3 | 3.55 | 3.8 | V |
| $V_{BP6UV(hyst)}$ | Regulator UVLO voltage hysteresis(1) | | 230 | 255 | 270 | mV |
| **BPEXT** | | | | | | |
| $V_{BPEXT(swover)}$ | BPEXT switch-over voltage | | 4.5 | 4.6 | | V |
| $V_{hys(swover)}$ | BPEXT switch-over hysteresis | | 100 | | 200 | mV |
| $V_{BPEXT(do)}$ | BPEXT dropout voltage | $V_{BPEXT}$–$V_{BP6}$, $V_{BPEXT}$ = 4.8 V, $I_{BP6}$ = 25 mA | | | 100 | mV |
| **BOOTSTRAP** | | | | | | |
| $V_{BOOT(drop)}$ | Bootstrap voltage drop | $I_{BOOT}$ = 5 mA | | 0.7 | 1.0 | V |
| **BP3 REGULATOR** | | | | | | |
| $V_{BP3}$ | Output voltage | $V_{VDD}$ = 4.5 V, $I_{BP3}$ ≤ 5 mA | 3.1 | 3.3 | 3.5 | V |
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Adjustment range | | 100 | | 1000 | kHz |
| | Switching frequency | $R_{RT}$ = 40 kΩ | 450 | 500 | 550 | kHz |
| $V_{RMP}$ | Ramp peak-to-peak(1) | | | $V_{VDD}$/8.2 | | V |
| $V_{VLY}$ | Valley voltage(1) | | 0.7 | 0.8 | 1.0 | V |

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## 7.5 Electrical Characteristics (continued)

$T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{DD}$ = 12 V, $f_{SW}$ = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SYNCHRONIZATION** | | | | | | |
| $V_{SYNCH}$ | SYNC high-level threshold | | 2.0 | | | V |
| $V_{SYNCL}$ | SYNC low level threshold | | | | 0.8 | V |
| $t_{SYNC}$ | Minimum SYNC pulse width | | | | 100 | ns |
| $f_{SYNC(max)}$ | Maximum SYNC frequency(4) | | 2000 | | | kHz |
| $f_{SYNC(min)}$ | Minimum SYNC frequency(4) | | | | 200 | |
| | SYNC frequency range (increase from nominal oscillator frequency) | | –20% | | 20% | |
| **PWM** | | | | | | |
| $t_{OFF(min)}$ | Minimum off time | | 90 | 100 | | ns |
| $t_{ON(min)}$ | Minimum on pulse(1) | | | 90 | 130 | ns |
| $t_{DEAD}$ | Output driver dead time | HDRV off to LDRV on | 15 | 30 | 45 | ns |
| | | LDRV off to HDRV on | 15 | 30 | 45 | |
| **SOFT START** | | | | | | |
| $t_{SS}$ | Soft-start time | Factory default settings | 2.4 | 2.7 | 3.0 | ms |
| | Accuracy over range(1) | 600 µs ≤ $t_{SS}$ ≤ 9 ms | –15% | | 15% | |
| $t_{ON(delay)}$ | Turn-on delay time(3) | Factory default settings | | 0 | | ms |
| $t_{OFF(delay)}$ | Turn-off delay time | Factory default settings | | 0 | | ms |
| **REMOTE SENSE AMPLIFIER** | | | | | | |
| $V_{DIFFO(err)}$ | Error voltage from DIFFO1 to ($V_{SNS1}$– $G_{SNS1}$) | ($V_{SNS1}$– $G_{SNS1}$) = 0.6 V | –5 | | 5 | mV |
| | | ($V_{SNS1}$– $G_{SNS1}$) = 1.2 V | –8 | | 8 | |
| | | ($V_{SNS1}$– $G_{SNS1}$) = 3.0 V | –17 | | 17 | |
| BW | Closed-loop bandwidth(1) | | 2 | | | MHz |
| $V_{DIFFO(max)}$ | Maximum DIFFOx output voltage | | $V_{BP6}$-0.2 | | | V |
| $I_{DIFFO}$ | Sourcing | | 1 | | | mA |
| | Sinking | | 1 | | | |
| **DRIVERS** | | | | | | |
| $R_{HS(up)}$ | High-side driver pull-up resistance | ($V_{BOOT}$–$V_{SW}$) = 6.5 V, $I_{HS}$ = -40 mA | 0.8 | 1.5 | 2.5 | Ω |
| $R_{HS(dn)}$ | High-side driver pull-down resistance | ($V_{BOOT}$–$V_{SW}$) = 6.5 V, $I_{HS}$ = 40 mA | 0.5 | 1.0 | 1.5 | |
| $R_{LS(up)}$ | Low-side driver pull-up resistance | $I_{LS}$ = -40 mA | 0.8 | 1.5 | 2.5 | |
| $R_{LS(dn)}$ | Low-side driver pull-down resistance | $I_{LS}$ = 40 mA | 0.35 | 0.70 | 1.40 | |
| $t_{HS(rise)}$ | High-side driver rise time (1) | $C_{LOAD}$ = 5 nF | | 15 | | ns |
| $t_{HS(fall)}$ | High-side driver fall time (1) | $C_{LOAD}$ = 5 nF | | 12 | | |
| $t_{LS(rise)}$ | Low-side driver rise time (1) | $C_{LOAD}$ = 5 nF | | 15 | | |
| $t_{LS(fall)}$ | Low-side driver fall time (1) | $C_{LOAD}$ = 5 nF | | 10 | | |
| **CURRENT SENSING AMPLIFIER** | | | | | | |
| $V_{CS(rng)}$ | Differential input voltage range | $V_{CSxP}$-$V_{CSxN}$ | -60 | | 60 | mV |
| $V_{CS(cmr)}$ | Input common-mode range | | 0 | | $V_{BP6}$–0.2 | V |
| $V_{CS(os)}$ | Input offset voltage | $V_{CSxP}$ = $V_{CSxN}$ = 0 V | -3 | | 3 | mV |
| $A_{CS}$ | Current sensing gain | | | 15.00 | | V/V |
| $V_{CS(out)}$ | Amplfier output | ($V_{CSxP}$-$V_{CSxN}$) = 20 mV | 270 | 300 | 330 | mV |
| $f_{C0}$ | Closed-loop bandwidth(1) | | 3 | 5 | | MHz |
| $V_{CS(chch)}$ | Amplifier output difference between CH1, CH2 | ($V_{CS1P}$– $V_{CS1N}$) = ($V_{CS2P}$–$V_{CS2N}$) = 20 mV, $T_J$ = 25°C | -5.00% | | 5.00% | |
| | | ($V_{CS1P}$– $V_{CS1N}$) = ($V_{CS2P}$–$V_{CS2N}$) = 20 mV, $T_J$ = 85°C | -6.67% | | 6.67% | |


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## 7.5 Electrical Characteristics (continued)

$T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{DD}$ = 12 V, $f_{SW}$ = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | | |
| $t_{OFF(oc)}$ | Off-time between restart attempts | Hiccup mode | | 7×$t_{SS}$ | | ms |
| DCR | Inductor DCR current sensing calibration value | Factory default settings | | 0.488 | | mΩ |
| | | Programmable range | 0.240 | | 15.500 | |
| $I_{OC(flt)}$ | Output current overcurrent fault threshold | Factory default settings | | 30 | | A |
| | | Programmable range | 3 | | 50 | |
| $I_{OC(warn)}$ | Output current overcurrent warning threshold | Factory default settings | | 27 | | A |
| | | Programmable range | 2 | | 49 | |
| $I_{OC(tc)}$ | Output current fault/warning temperature coefficient(1) | | 3900 | 4000 | 4100 | ppm/°C |
| $I_{OC(acc)}$ | Output warning and fault accuracy | ($V_{CSxP}$-$V_{CSxN}$) = 30 mV | –15% | | 15% | |
| **PGOOD** | | | | | | |
| $V_{FBPGH}$ | FB PGOOD high threshold | Factory default settings | | 675 | | mV |
| $V_{FBPGL}$ | FB PGOOD low threshold | Factory default settings | | 525 | | mV |
| $V_{PG(acc)}$ | PGOOD accuracy over range | 4.5 V ≤ $V_{VDD}$ ≤ 20 V, 468 mV ≤ $V_{PGOOD}$ ≤ 675 mV | –4% | | 4% | |
| $V_{pg(hyst)}$ | FB PGOOD hysteresis voltage | | | 25 | 40 | mV |
| $R_{PGOOD}$ | PGOOD pulldown resistance | $V_{FB}$ = 0, $I_{PGOOD}$ = 5 mA | | 40 | 70 | Ω |
| $I_{PGOOD(lk)}$ | PGOOD pin leakage current | No fault, $V_{PGOOD}$ = 5 V | | | 20 | µA |
| **OUTPUT OVERVOLTAGE/UNDERVOLTAGE** | | | | | | |
| $V_{FBOV}$ | FB pin over voltage threshold | Factory default settings | | 700 | | mV |
| $V_{FBUV}$ | FB pin under voltage threshold | Factory default settings | | 500 | | mV |
| $V_{UVOV(acc)}$ | FB UV/OV accuracy over range | 4.5 V ≤ $V_{VDD}$ ≤ 20 V | –4% | | 4% | |
| **OUTPUT VOLTAGE TRIMMING AND MARGINING** | | | | | | |
| $V_{FBTM(step)}$ | Resolution of FB steps with trim and margin | | | 2 | | mV |
| $t_{FBTM(step)}$ | Transition time per trim or margin step | After soft-start time | | 30 | | µs |
| $V_{FBTM(max)}$ | Maximum FB voltage with trim and/or margin | | | 660 | | mV |
| $V_{FBTM(min)}$ | Minimum FB voltage with trim or margin only | | | 480 | | mV |
| | Minimum FB voltage range with trim and margin combined | | | 420 | | |
| $V_{FBMH}$ | Margin high FB pin voltage | Factory default settings | | 660 | | mV |
| $V_{FBML}$ | Margin low FB pin voltage | Factory default settings | | 540 | | mV |
| **TEMPERATURE SENSE AND THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Junction thermal shutdown temperature(1) | | 135 | 145 | 155 | °C |
| $T_{HYST}$ | Thermal shutdown hysteresis(1) | | 15 | 20 | 25 | °C |
| $I_{TSNS(ratio)}$ | Ratio of bias current flowing out of TSNS pin, state 2 to state 1 | | 9.7 | 10.0 | 10.3 | |
| $I_{TSNS}$ | State 1 current out of TSNSx pin(1) | | | 10 | | µA |
| $I_{TSNS}$ | State 2 current out of TSNSx pin(1) | | | 100 | | µA |
| $V_{TSNS}$ | Voltage range on TSNSx pin(1) | | 0 | | 1.00 | V |
| $T_{SNS(acc)}$ | External temperature sense accuracy(1) | 0°C ≤ $T_J$ ≤ 125°C | –5 | | 5 | °C |
| $T_{OT(flt)}$ | Overtemperature fault limit(1) | Factory default settings | | 145 | | °C |
| | OT fault limit range(1) | | 120 | | 165 | °C |
| $T_{OT(warn)}$ | Overtemperature warning limit(1) | Factory default settings | | 125 | | °C |
| | OT warning limit range(1) | | 100 | | 140 | °C |
| $T_{OT(step)}$ | OT fault/warning step | | | 5 | | °C |
| $T_{OT(hys)}$ | OT fault/warning hysteresis(1) | | 15 | 20 | 25 | °C |

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## 7.5 Electrical Characteristics (continued)

$T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{DD}$ = 12 V, $f_{SW}$ = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **MEASUREMENT SYSTEM** | | | | | | |
| $M_{VOUT(rng)}$ | Output voltage measurement range(1) | | 0.5 | | 5.8 | V |
| $M_{VOUT(acc)}$ | Output voltage measurement accuracy | $V_{OUT}$ = 1.0 V | –2.0% | | 2.0% | |
| $M_{IOUT(rng)}$ | Output current measurement signal range(1) | $V_{CSxP}$–$V_{CSxN}$, 0.2440 mΩ ≤ IOUT_CAL_GAIN ≤ 0.5795 mΩ | 0 | | 24 | mV |
| | | $V_{CSxP}$–$V_{CSxN}$, 0.5796 mΩ ≤ IOUT_CAL_GAIN ≤ 1.1285 mΩ | 0 | | 40 | |
| | | $V_{CSxP}$–$V_{CSxN}$, 1.1286 mΩ ≤ IOUT_CAL_GAIN ≤ 15.5 mΩ | 0 | | 60 | |
| $M_{IOUT(acc)}$ | Output current measurement accuracy | $I_{OUT}$ ≥ 20 A, DCR = 0.5 mΩ | –1.0 | | 1.0 | A |
| **PMBus ADDRESSING** | | | | | | |
| $I_{ADD}$ | Address pin bias current | | 9.24 | 10.50 | 11.76 | µA |
| **PMBus INTERFACE** | | | | | | |
| $V_{IH}$ | Input high voltage, CLK, DATA, CNTLx | | 2.1 | | | V |
| $V_{IL}$ | Input low voltage, CLK, DATA, CNTLx | | | | 0.8 | V |
| $I_{IH}$ | Input high level current, CLK, DATA | | –10 | | 10 | µA |
| $I_{IL}$ | Input low level current, CLK, DATA | | –10 | | 10 | mA |
| $I_{CTNL}$ | CNTL pin pull-up current | | | 6 | | µA |
| $V_{OL}$ | Low-level output voltage, DATA, (1) | 4.5 V ≤ $V_{VDD}$ ≤ 20 V, $I_{OUT}$ = 4 mA | | | 0.4 | V |
| $I_{OH}$ | High-level output open-drain leakage current, DATA, $\overline{SMBALRT}$ | $V_{OUT}$ = 5.5 V | 0 | | 10 | µA |
| $C_{OUT}$ | Output capacitance, CLK, DATA(1) | | | | 1 | pF |
| $F_{PMB}$ | PMBus operating frequency range(1) | Slave mode | 10 | | 400 | kHz |
| $t_{BUF}$ | Bus free time between START and STOP(1) | | 1.3 | | | µs |
| $t_{HD:STA}$ | Hold time after repeated START(1) | | 0.6 | | | µs |
| $t_{SU:STA}$ | Repeated START setup time(1) | | 0.6 | | | µs |
| $t_{SU:STO}$ | STOP setup time(1) | | 0.6 | | | µs |
| $t_{HD:DAT}$ | Data hold time(1) | Receive mode | 0 | | | ns |
| | | Transmit mode | 300 | | | |
| $t_{SU:DAT}$ | Data setup time(1) | | 100 | | | ns |
| $t_{TIMEOUT}$ | Error signal/detect(1) | | 25 | | 35 | ms |
| $t_{LOW:MEXT}$ | Cumulative clock low master extend time(1) | | | | 10 | ms |
| $t_{LOW:SEXT}$ | Cumulative clock low slave extend time(1) | | | | 25 | µs |
| $t_{LOW}$ | Clock low time(1) | | 1.3 | | | µs |
| $t_{HIGH}$ | Clock high time(1) | | 0.6 | | | µs |
| $t_{FALL}$ | CLK/DATA fall time(1) | | | | 300 | ns |
| $t_{RISE}$ | CLK/DATA rise time(1) | | | | 300 | ns |

(1) Specified by design. Not production tested.
(2) Hysteresis of at least 150 mV is specified by design.
(3) The minimum turn-on delay is 50 µs, when TON_DELAY is set to a factor of zero.
(4) When using SYNC, the switching frequency is set to one-half the SYNC frequency.


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## 7.6 Typical Characteristics

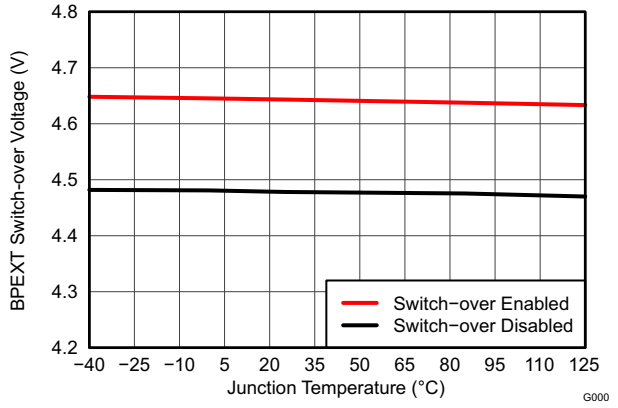



図 7-1. BPEXT Switch-over Voltage vs. Junction Temperature

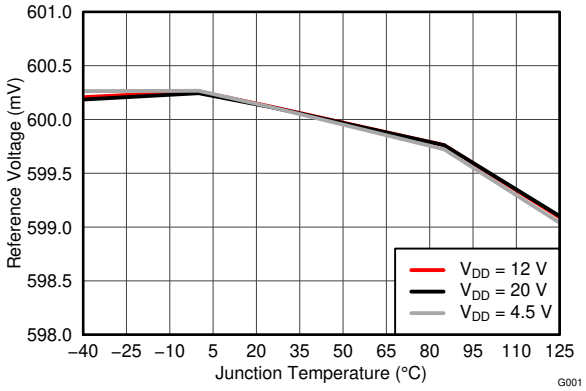



図 7-2. Reference Voltage vs. Junction Temperature

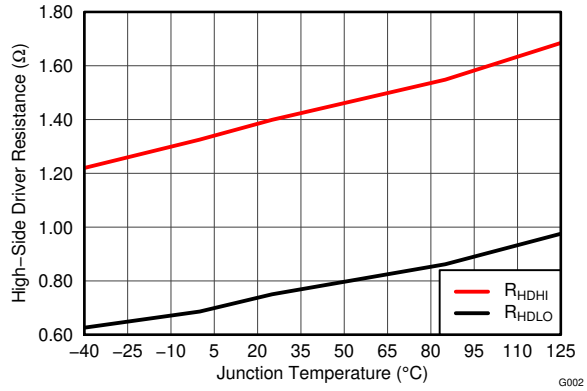



図 7-3. High-Side Driver Resistance vs. Junction Temperature

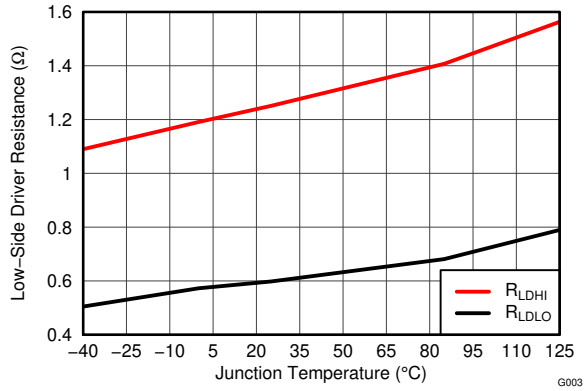



図 7-4. Low-Side Driver Resistance vs. Junction Temperature

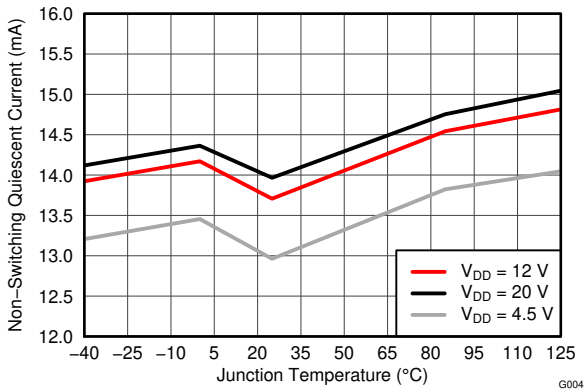



図 7-5. Non-Switching Quiescent Current vs. Junction Temperature

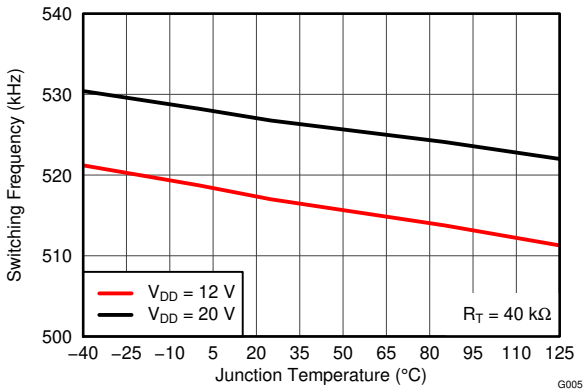



図 7-6. Switching Frequency vs. Junction Temperature

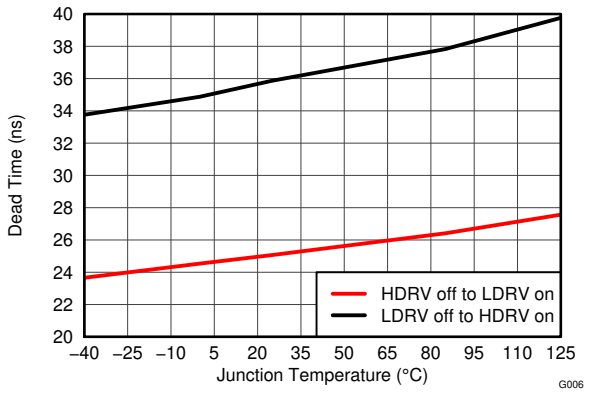



**図 7-7. Dead Time vs. Junction Temperature**

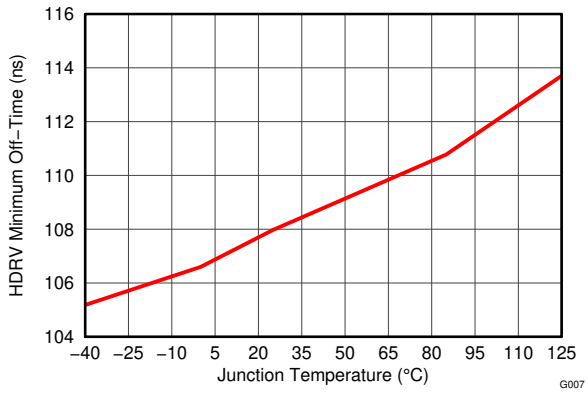



**図 7-8. HDRV Minimum Off-Time vs. Junction Temperature**


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# 8 Detailed Description

## 8.1 Overview

The TPS4022 device is a flexible synchronous buck controller. It can be used as a dual-output controller, or as a two-phase single-output controller. It operates with a wide input range from 4.5 V to 20 V and generates accurate regulated output as low as 600 mV.

In dual output mode, voltage mode control with input feed-forward architecture is implemented. With this architecture, the benefits are less noise sensitivity, no control instability issues for small DCR applications, and a smaller minimum controllable on-time, often desired for high conversion ratio applications.

In two-phase single-output mode, a current-sharing loop is implemented to ensure a balance of current between phases. Because the induced error current signal to the loop is much smaller when compared to the PWM ramp amplitude, the control loop is modeled as voltage mode with input feed-forward.

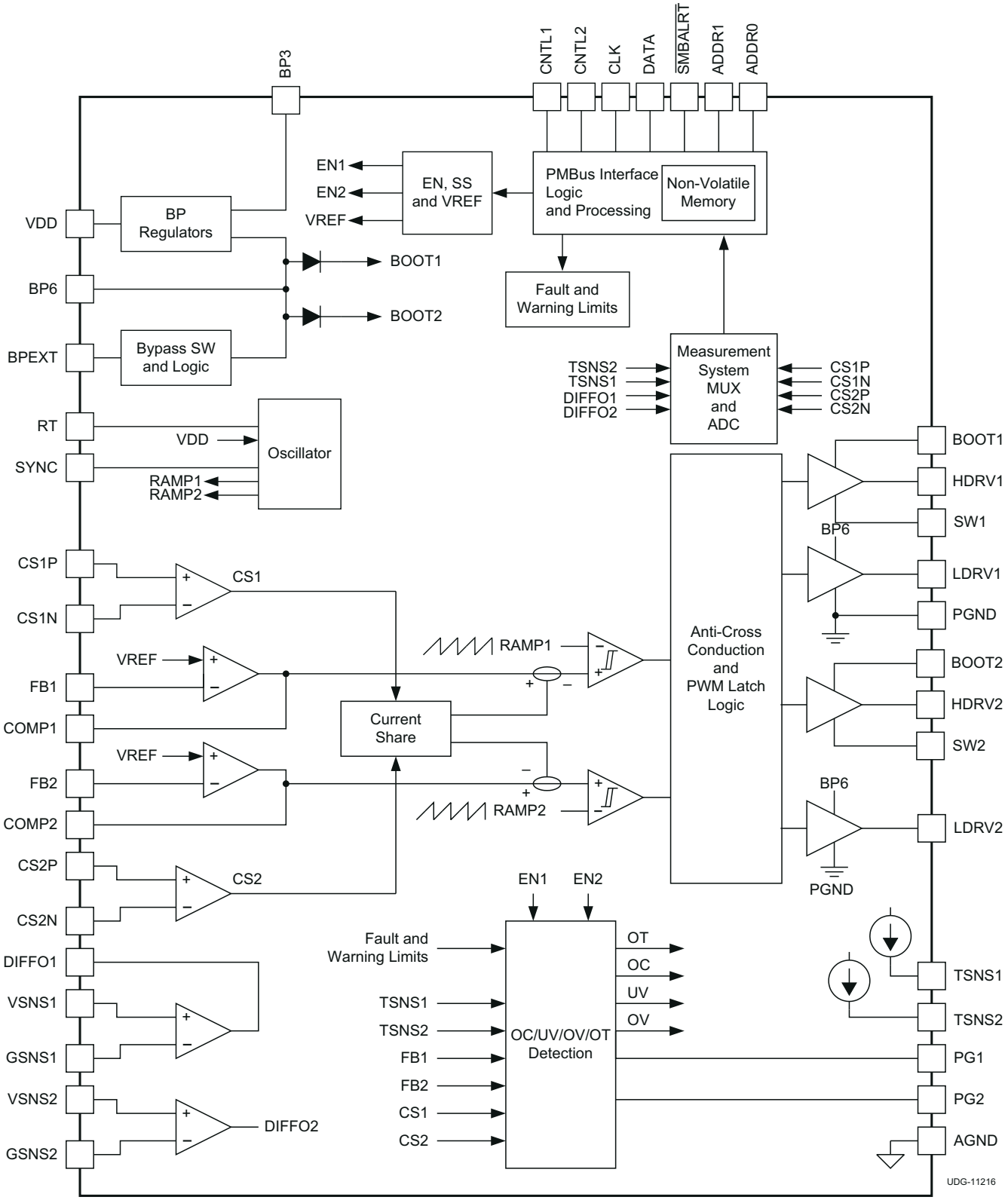
注

To operate the device in two-phase mode, tie the FB2 pin to the BP6 pin and tie the COMP1 pin to the COMP2 pin. These connections must be made before applying voltage to the VDD pin.

(See the セクション *8.4.4* section for more information)

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## 8.2 Functional Block Diagram





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## 8.3 Feature Description

### 8.3.1 PMBus Interface Protocol General Description

Timing and electrical characteristics of the PMBus protocol can be found in the PMB Power Management Protocol Specification, Part 1, revision 1.1 available at http://pmbus.org. The TPS4022 device supports both the 100 kHz and 400 kHz bus timing requirements. The device does not stretch pulses on the PMBus interface when communicating with the master device.

Communication over the PMBus interface can either support the Packet Error Checking (PEC) scheme or not. If the master supplies CLK pulses for the PEC byte, it is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The TPS4022 device supports a subset of the commands in the PMBus 1.1 specification. Most controller parameters can be programmed using the PMBus interface and stored as defaults for later use. All commands that require data input or output use the linear format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the device. See the *セクション 8.6.1* section for specific details.

The TPS4022 device also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the TPS4022 device) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The device uses non-volatile memory to store configuration settings and scale factors. However, the device does not automatically save the programmed settings into this non-volatile memory. The STORE_USER_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The detailed description of each setting notes if it is able to be stored in non-volatile memory.

### 8.3.2 Voltage Reference

The 600-mV bandgap cell connects internally to the non-inverting input of the error amplifier. The device trims the reference voltage by using the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 0.5-% tolerance on the reference voltage allows the user to design a very accurate power supply.

### 8.3.3 Output Voltage

The TPS4022 device sets the output voltage in a way that is very similar to a traditional analog controller by using a voltage divider from the output to the FB (feedback) pin. The output voltage must be divided down to the nominal reference voltage of 600 mV. 図 8-1 shows the typical connections for the controller. The device senses the voltage at the load by using the unity gain differential voltage sense amplifier. This functionality provides better load regulation for output voltages lower than 5-V nominal (see the *セクション 7.5* table for the maximum output voltage specification for the differential sense amplifier). For output voltages above this level, connect the output voltage directly to the junction of R1 and C1, leave DIFFO1 open, and do not connect the VSNS1 pin to the output voltage. The differential amplifier may also be used elsewhere in the overall system as a voltage buffer, provided the electrical specifications are not exceeded.

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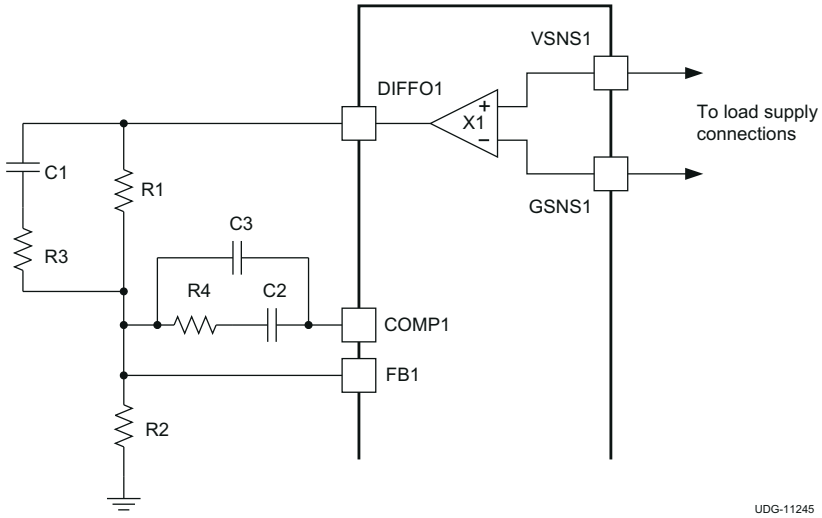



**図 8-1. Setting the Output Voltage**

The components shown in 図 8-1 that determine the nominal output voltage are R1 and R2. In most cases, choose a value for R to ensure the feedback compensation values (R3, R4, C1, C2 and C3) come close to readily available standard values. A value for R2 is then calculated in 式 1.

$$R2 = V_{FB} \times \left( \frac{R1}{(V_{OUT} - V_{FB})} \right) \quad (1)$$

where

- $V_{FB}$ is the feedback voltage
- $V_{OUT}$ is the desired output voltage
- R1 and R2 are in the same unit

注

There is no DIFFO2 pin. In dual-output mode, VSNS2 and GSNS2 are connected to the load for channel 2 and the device uses the DIFFO2 signal internally to provide voltage monitoring. Connect the output directly to the junction of R1 and C1 for channel 2 to set the output voltage and for feedback.

The DIFFO1 pin operates at voltages up to ($V_{BP6}$–0.2 V). If the voltage between the VSNS1 and GSNS1 pins is higher than ($V_{BP6}$–0.2 V) during any condition, the output voltage moves out of regulation because the DIFFO1 voltage is limited by BP6. To prevent this from happening, the BP6 voltage must be pre-biased before the PWM turns on, and ($V_{BP6}$–0.2 V) must remain higher than the voltage between the VSNS1 and GSNS1 pins until the PWM turns off.

The feedback voltage can be changed to a value between –30% and +10% from the nominal 600 mV using PMBus commands. This adjustment allows the output voltage to vary by the same percentage. See the *セクション 8.5.1* section for more details.

### 8.3.4 Voltage Feed Forward

The TPS4022 device uses input-voltage feed-forward topology that maintains a constant power stage gain when the input voltage varies. It also provides for very good response to input voltage transient disturbances. The constant power stage gain of the controller greatly simplifies feedback loop design because loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feed-forward topology. For modeling purposes, the gain from the COMP pin to the average voltage at the input of the L-C filter is 8.2 V/V.


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### 8.3.5 Current Sensing

The TPS4022 device uses a differential current-sense scheme to sense the output current. The sense element can be either the series resistance of the power stage filter inductor or a separate current sense resistor. When using the inductor series resistance as in 図 8-2, a filter must be used to remove the large AC component of voltage across the inductor and leave only the component of the voltage that appears across the resistance of the inductor. The values of R5 and C4 for the ideal case can be found using 式 2. The time constant of the R-C filter should be equal to or greater than the time constant of the inductor itself. If the time constants are equal, the voltage appearing across C4 is the current in the inductor multiplied the inductor resistance. The voltage across C4 perfectly reflects the inductor ripple current. Therefore, there is no need to have a shorter R-C time constant.

Extending the R-C filter time constant beyond the inductor time constant lowers the AC ripple component of voltage present at the current sense pins of the device, but allows the correct DC current information to remain intact. This extension also delays slightly the response to an overcurrent event, but reduces noise in the system leading to cleaner overcurrent performance and current reporting data over the PMBus interface.

$$R5 \times C4 \geq \left( \frac{L}{R_{DCR}} \right) \tag{2}$$

where (from 図 8-2)

- R5 and $R_{ESR}$ are in Ω
- C4 is in F (suggest 100 nF, $10^{-7}$F)
- L is in H

TPS4022 device is designed to accept a maximum voltage of 60 mV across the current-sense pins. Most inductors have a copper conductor which results in a fairly large temperature coefficient of resistance. Because of this large temperature coefficient, the resistance of the inductor and the current through the inductor should make a peak voltage less than 60 mV when the inductor is at the maximum temperature for the converter. This situation also applies for the external resistor in 図 8-3. The full-load output current multiplied by the sense resistor value, must be less than 60 mV at the maximum converter operating temperature.

In all cases, C4 should be placed as close to the current sense pins as possible to help avoid problems with noise.

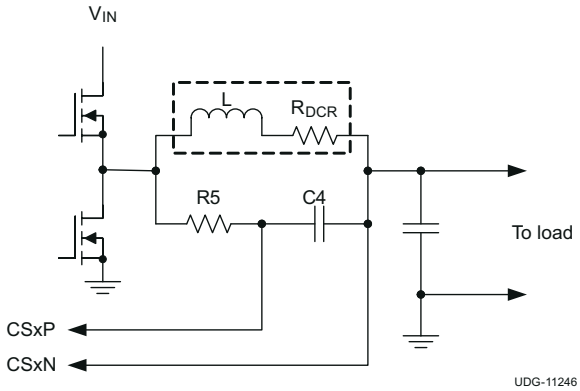



**図 8-2. Current Sensing Using Inductor Resistance**

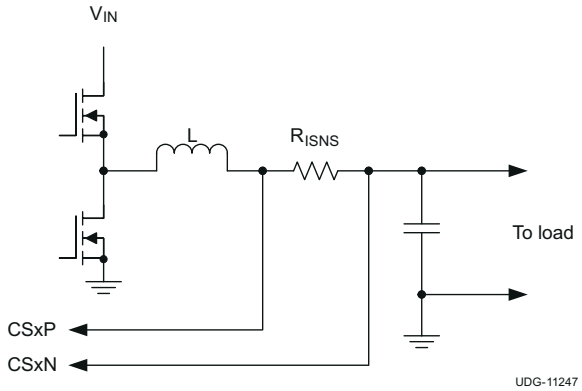



**図 8-3. Current Sensing Using Sense Resistor**

After choosing the current sensing method, set the current-sense element resistance. This value allows the proper calculation of thresholds for the overcurrent fault and warning, as well as more accurate reporting of the actual output current. The IOUT_CAL_GAIN command is used to set the value of the sense element resistance of the device. IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT set the levels for the overcurrent warning and fault levels respectively. (See the *セクション 8.5.1* section for more details.)

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### 8.3.6 Overcurrent Protection

The TPS4022 device has overcurrent fault and warning thresholds for each channel which can be independently set, when operating in dual-output mode. When operating in two-phase mode, both channels share the same overcurrent fault and warning thresholds. The overcurrent thresholds are set via the PMBus interface using the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT commands. (See the セクション 8.5.1 section for more details.)

The device generates an internal voltage corresponding to the desired overcurrent threshold, using the IOUT_OC_FAULT_LIMIT threshold and the IOUT_CAL_GAIN setting, and adjusting for temperature using the measured external temperature value. The current sense amplifier amplifies the sensed current signal with a fixed gain of 15 and then compares that value to this internal voltage threshold. The device uses a similar structure to activate an overcurrent warning based on the IOUT_OC_WARN_LIMIT threshold.

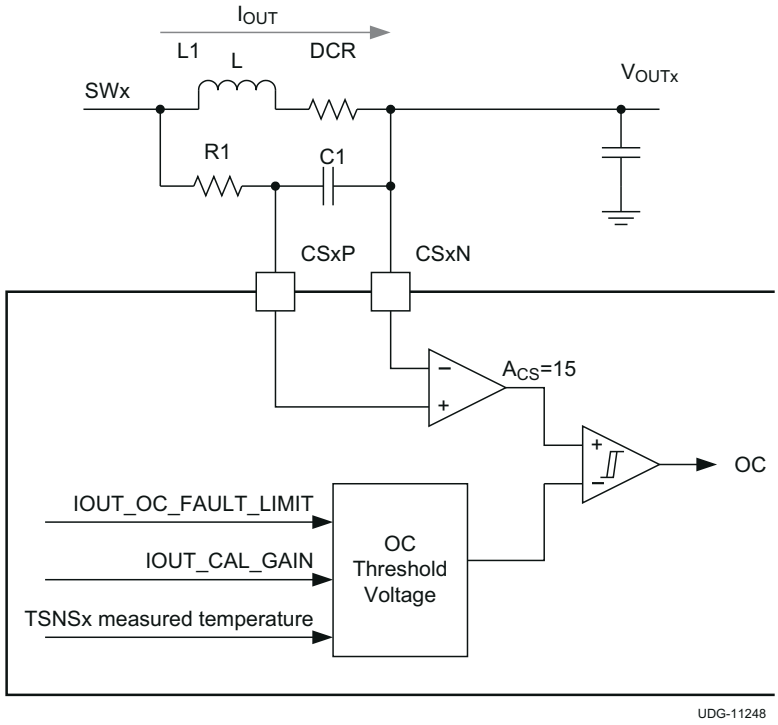



**図 8-4. Overcurrent Protection**

The programmable range of the overcurrent fault and warning voltage thresholds places a functional limit on the input voltage of the current sense amplifier. The minimum overcurrent fault and warning thresholds correspond to a voltage from CSxP to CSxN of 6 mV and 4.7 mV, respectively. If the voltage across these pins does not exceed the minimum thresholds, then overcurrent fault and warning cannot be tripped, regardless of the setting of IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT. There is also maximum overcurrent fault and warning thresholds corresponding to a voltage from CSxP to CSxN of 60 mV and 59 mV, respectively. If the voltage across these pins exceeds this maximum threshold, the overcurrent fault or warning will be tripped, regardless of the setting of IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT. The result is that for higher values of inductor DCR, a resistor across the current sensing capacitor may be required to create a voltage divider into the current sensing inputs.

The TPS4022 device implements cycle-by-cycle current limit when the peak sensed current exceeds the set threshold. In a time constant matched current sensor network, the signal across the CSxP and CSxN pins has both dc and ac inductor current information, so an overcurrent fault trips when the dc current plus half of the ripple current exceeds the set threshold. When the time constant is not well-matched, the dc current which trips the overcurrent changes accordingly.


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When the controller counts three consecutive clock cycles of an overcurrent condition, the high-side and low-side MOSFETs are turned off and the controller enters hiccup mode or latches the output off, depending on the IOUT_OC_FAULT_RESPONSE register. In continuous restart hiccup mode, after seven soft-start cycles, normal switching is attempted. If the overcurrent has cleared, normal operation resumes; otherwise, the sequence repeats.

### 8.3.7 Current Sharing

See the *セクション 8.4.4* section for more information on current sharing.

### 8.3.8 Linear Regulators

The TPS4022 device has two on-board linear regulators to provide suitable power for the internal circuitry of the device. These pins, BP3 and BP6 must be properly bypassed in function properly. BP3 needs a minimum of 100 nF connected to AGND and BP6 should have approximately 1 µF of capacitance connected to PGND.

It is permissible to use the external regulator to power other circuits if desired, but ensure that the loads placed on the regulators do not adversely affect operation of the controller. The main consideration is to avoid loads with heavy transient currents that can affect the regulator outputs. Transient voltages on these outputs could result in noisy or erratic operation of the device.

Current limits must also be observed. Shorting the BP3 pin to GND damages the BP3 regulator. The BP3 regulator input comes from the BP6 regulator output. The BP6 regulator can supply 120 mA so the total current drawn from both regulators must be less than that. This total current includes the device operating current $I_{VDD}$ plus the gate drive current required to drive the power FETs. The total available current from two regulators is described in 式 3 and 式 4:

$$I_{L(in)} = I_{BP6} - \left(I_{VDD} + I_{GATE}\right) \tag{3}$$

$$I_{GATE} = f_{SW} \times \left(Q_{gHIGH} + Q_{gLOW}\right) \tag{4}$$

where

- $I_{L(in)}$ is the total current that can be drawn from BP3 and BP6 in aggregate
- $I_{BP6}$ is the current limit of the BP6 regulator (120-mA minimum)
- $I_{VDD}$ is the quiescent current of the TPS4022 (15-mA maximum)
- $I_{GATE}$ is the gate drive current required by the power FETs
- $f_{SW}$ is the switching frequency
- $Q_{gHIGH}$ is the total gate charge required by the high-side FETs
- $Q_{gLOW}$ is the total gate charge required by the low-side FETs

### 8.3.9 BP Switch-over

If the voltage on the BPEXT pin is lower than the switch-over voltage, $V_{BPEXT(swover)}$, then the internal BP6 regulator is used. If the voltage on the BPEXT pin exceeds this switch-over voltage, then the internal BP6 regulator is bypassed and the BP6 pin follows BPEXT, until the voltage on the BPEXT pin falls by the BPEXT switch-over hysteresis amount, $V_{HYS(swover)}$.

If the BPEXT function is not used, it is recommended to connect the BPEXT pin to GND via a 10 kΩ resistor to increase noise immunity.

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### 8.3.10 Switching Frequency Setting

The switching frequency is set by the value of the resistor connected from the RT pin to AGND. The RT resistor value is calculated in 式 5.

$$R_{RT} = \frac{20 \times 10^9}{f_{SW}} \tag{5}$$

where

- $R_{RT}$ is the resistor from RT pin to AGND, in Ω
- $f_{SW}$ is the desired switching frequency, in Hz

When the TPS4022 device is synchronized to an external clock, the external clock frequency should be two times the free running frequency that is set by RT resistor. The variation of the external clock frequency should be within ±20%, and the switching frequency is one half of the actual clock frequency.

### 8.3.11 Switching Node and BOOT Voltage

The maximum voltage rating of the switching node and BOOT pins is 30 V. The limit of 30 V on the BOOT1 and BOOT2 pin voltage should be strictly enforced. If the voltage spike of BOOT1 or BOOT2 is above 30 V during operation, the internal boot diode might be damaged and result in permanent failure. To reduce the voltage spike on the switching node, the R-C snubber can be added. Furthermore, the BOOT resistor can be added to slow down the turn-on of high-side switch. If the voltage spike remains above 30 V with an R-C snubber and a boot resistor, add a gate resistor as shown in 図 8-5 to slow down the turn-on time of the high-side switch and to further reduce voltage spikes. To eliminate the impact of the gate resistor to the turn-off time of the high-side switch, place a Schottky diode in parallel with the gate resistor.

If the approaches described in this section do not reduce the BOOTx voltage to within 30 V, add an external BOOT diode between the BP6 pin and the BOOTx pin. The forward voltage of the external BOOT diode must be less than that of internal BOOT diode and the voltage rating should be higher than the BOOT voltage spike.

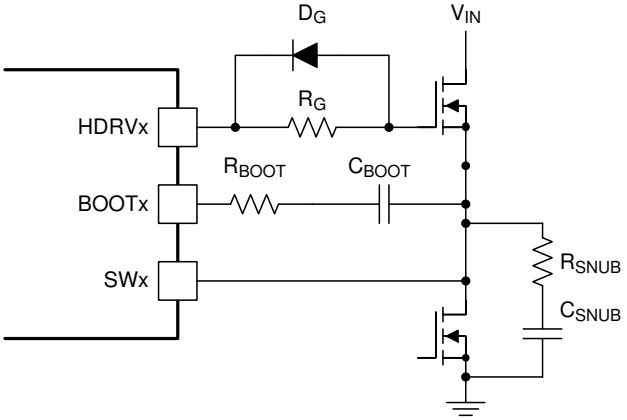



**図 8-5. Adding a BOOT Resistor and Gate Resistor**

### 8.3.12 Reading the Output Current

the READ_IOUT command reads the average output current of the device. The results of this command support only positive current or current sourced from the converter. When the converter is sinking current, the result of this command is a reading of 0 A.

### 8.3.13 Soft-Start Time

The TPS4022 device supports several soft-start times between 600 µs and 9 ms. Use the TON_RISE PMBus command to select the soft-start time. See the セクション 8.6.1.19 command description for full details on the levels and implementation. When selecting the soft-start time, carefully consider the charging current for the


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output capacitors. In some applications (for example, those with large amounts of output capacitance) this current level can lead to problems with nuisance tripping of the overcurrent protection circuitry. To ensure that this does not happen, include a consideration of the output capacitor charging current when choosing the overcurrent threshold setting. Use 式 6 to calculate the output capacitor charging current.

$$I_{CAP} = \left( \frac{(V_{OUT} \times C_{OUT})}{t_{SS}} \right) \quad (6)$$

where

- $I_{CAP}$ is the startup charging current of the output capacitance in A
- $V_{OUT}$ is the output voltage of the converter in V
- $C_{OUT}$ is the total output capacitance in F
- $t_{SS}$ is the selected soft-start time in seconds

After calculating the charging current, the overcurrent threshold can then be calibrated to the sum of the maximum load current and the output capacitor charging current plus some margin. The amount of margin required depends on the individual application, but 25% is a suggested starting point. Individual applications may require more or less than 25%.

### 8.3.14 Turn-On/Turn-Off Delay and Sequencing

The TPS4022 device provides many sequencing options. Using the ON_OFF_CONFIG command, each rail can be configured to start up whenever the input is not in undervoltage lockout or to additionally require a signal on the CNTLx pin and/or receive an update to the OPERATION command via the PMBus interface.

When the gating signal as specified by ON_OFF_CONFIG is reached for that rail, a programmable turn-on delay can be set with TON_DELAY. The rise time can be programmed with TON_RISE. When the specified signal(s) are set to turn the output off, a programmable turn-off delay set by TOFF_DELAY is used before switching is inhibited. More information can be found in the PMBus command descriptions.

When the output voltage reaches the PGOOD threshold after the start-up period, the PGOOD pin is asserted. This pin can be connected to the CNTL pin of another rail in dual-output mode or on another device to control turn-on and turn-off sequencing.

### 8.3.15 Pre-Biased Output Start-Up

A circuit in the TPS4022 device prevents current from being pulled from the output during the start-up sequence in a pre-biased output condition. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FBx pin), if the output is pre-biased. As soon as the soft-start voltage exceeds the error amplifier input, the device slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage start-up and ramp-to-regulation sequences are smooth and controlled.

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During the soft-start sequence, when the PWM pulse width is shorter than the minimum controllable on-time, which is generally caused by the PWM comparator and gate driver delays, pulse skipping may occur and the output might show larger ripple voltage.

### 8.3.16 Undervoltage Lockout

The TPS4022 device provides flexible user adjustment of the undervoltage lockout threshold and the hysteresis. Two PMBus commands VIN_ON and VIN_OFF allow the user to set these input voltage turn on and turn off thresholds independently, with a minimum of 4-V turn off to a maximum 16-V turn on. See the individual command descriptions for more details.

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### 8.3.17 Overvoltage and Undervoltage Fault Protection

The TPS4022 device has output overvoltage protection and undervoltage protection capability. The comparators that regulate the overvoltage and undervoltage conditions use the FBx pin as the output sensing point so the filtering effect of the compensation network connected from COMPx to FBx has an effect on the speed of detection. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FBx to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the overvoltage threshold ($V_{OVP}$) or the undervoltage threshold ($V_{UVP}$) .

When an undervoltage fault is detected, the device enters hiccup mode and resumes normal operation when the fault is cleared.

When an overvoltage fault is detected, the device turns off the high-side MOSFET and latches on the low-side MOSFET to discharge the output current to the regulation level (within the power good window). After the output voltage comes into PG window, the controller resumes normal operation. If the OV condition still exists, the above procedure repeats.

When operating in dual-channel mode, both channels have identical but independent protection schemes which means one channel would not be affected when the other channel is in fault mode.

When operating in two-phase mode, only the FB1 pin is detected for overvoltage and undervoltage fault. Therefore both channels take action together during a fault.

### 8.3.18 Power Good

User-selectable, power good thresholds determine at what voltage the PGOOD pin is allowed to go high and the associated PMBus flags are cleared. There are three possible settings that can be had. See the POWER_GOOD_ON and POWER_GOOD_OFF command descriptions for complete details. These commands establish symmetrical values above and below the nominal voltage. Values entered for each threshold should be the voltages corresponding to the threshold below the nominal output voltage. For instance, if the nominal output voltage is 3.3 V, and the desired power good on thresholds are ±5%, the POWER_GOOD_ON command is issued with 2.85 V as the desired threshold. The POWER_GOOD_OFF command must be set to a lower value (higher percentage) than the POWER_GOOD_ON command as well.

The FB pin senses the output voltage for the purposes of power good detection. This sensing results in the inherent filtering action provided by the compensation network connected from the COMP pin to the FB pin. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force the FB pin to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the power good threshold. For this reason the network from the COMP pin to the FB pin should have no purely resistive path.

Power good de-asserts during all startups, after any fault condition is detected or whenever the device is turned off or in a disabled state (OPERATION command or CNTLx pins put the device into a disabled or off state). The PGOOD pin acts as a diode to GND when the device has no power applied to the VDD pin.

### 8.3.19 Overtemperature Fault Protection

The TPS4022 device uses measurements from the external temperature sensors connected on the TSNSx pins for each rail to provide programmable over-temperature fault and warning thresholds. See the *セクション 8.6.1.17* and *セクション 8.6.1.18* sections for more information about the command descriptions.

### 8.3.20 Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 150°C, the PWMs and the oscillators are turned off and HDRVs and LDRVs are driven low. When the junction cools to the required level (130°C typical), the PWM initiates soft start as during a normal power-up cycle.

### 8.3.21 Programmable Fault Responses

The IOUT_OC_FAULT_RESPONSE command programs the overcurrent and output undervoltage response. See the *セクション 8.6.1.15* section for more information about this command description.


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### 8.3.22 User Data

The MFR_SPECIFIC_00 command functions as a scratchpad to store 16 bits of arbitrary data. These bits can represent any information that the application requires and can be stored in EEPROM for non-volatility.

### 8.3.23 Adjustable Anti-Cross Conduction Delay

The MFR_SPECIFIC_21 command allows provides two anti-cross conduction delay (dead-time) options for each channel. Bit 0 of this command selects between two dead-time settings for channel 1, and bit 1 of this command selects between two dead-time settings for channel 2. In each case, writing this bit to a 1 selects the longer dead-time option. The particular option required for a given application depends upon several things such as FET total gate charge, FET gate resistance, PCB layout quality, and temperature. The proper setting for a given design is highly application-dependent, however, for FETs above 25-nC gate charge, the longer dead-time setting is generally considered. The shorter dead-time setting allows for higher efficiency in applications where FETs are generally small and switch very quickly. In applications with larger and slower switching FETs, a shorter dead-time leads to small amounts of cross conduction. Conversely, using the longer dead-time settings with smaller, faster switching FETs leads to excessive body diode conduction in the low-side FET, leading to a drop in overall converter efficiency.

### 8.3.24 Connection of Unused Pins

In some case, it is possible that some pins are not used. For example, if only channel 1 is used, then pins for channel 2 needs to be properly connected as well. The unused pin connections are summarized in 表 8-1.

**表 8-1. Unused Pin Connections**

| PIN NAME | CONNECTION |
|---|---|
| BOOTx | Floating |
| BPEXT | Connect to ground |
| CLK | Pull up to BP3 via 100-kΩ resistor |
| CNTLx | Connect to ground or high logic level whichever turns PWM off |
| COMPx | Floating |
| CSxN | Connect to ground |
| CSxP | Connect to ground |
| DATA | Pull up to BP3 via 100-kΩ resistor |
| DIFFO1 | Floating |
| FBx | Connect to ground |
| GSNSx | Connect to ground |
| HDRVx | Floating |
| LDRVx | Floating |
| PGx | Connect to ground |
| $\overline{\text{SMBALERT}}$ | Pull up to BP3 via 100-kΩ resistor |
| SWx | Connect to ground |
| SYNC | Connect to ground |
| TSNSx | Floating |
| VSNSx | Connect to ground is recommended. Connect to output voltage is also allowed. |

## 8.4 Device Functional Modes

### 8.4.1 Control Signal

The value in the ON_OFF_CONFIG register commands the TPS4022 device to use the control pin to enable or disable regulation, regardless of the state of the OPERATION command. The minimum input high threshold for the control signal is 2.1 V, and the maximum input low threshold for the control pin is 0.8 V. The control pin can be configured as either active high or active low logic.

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### 8.4.2 OPERATION Command

The value in the ON_OFF_CONFIG register, commands the TPS4022 device to use the OPERATION command to enable or disable regulation, regardless of the state of the control signal.

### 8.4.3 Control Signal and OPERATION Command

The value in the ON_OFF_CONFIG register commands the TPS4022 device to require both control signal and the OPERATION command to enable or disable regulation.

### 8.4.4 Two-Phase Mode Operation

The TPS4022 device can be configured to operate in single-output two-phase mode for high-current applications. With proper selection of the external MOSFETs, this device can support up to 50-A of load current in a two-phase configuration. 図 8-6 shows the TPS4022 device configured for two-phase mode with the FB2 pin tied to the BP6 pin. In this mode, COMP1 must be connected to COMP2 to ensure current sharing between the two phases. For high-current applications, the remote sense amplifier compensates for the parasitic offset to provide an accurate output voltage. The DIFFO1 pin, the output of the remote sensing amplifier, is connected to the resistor divider of the feedback network.

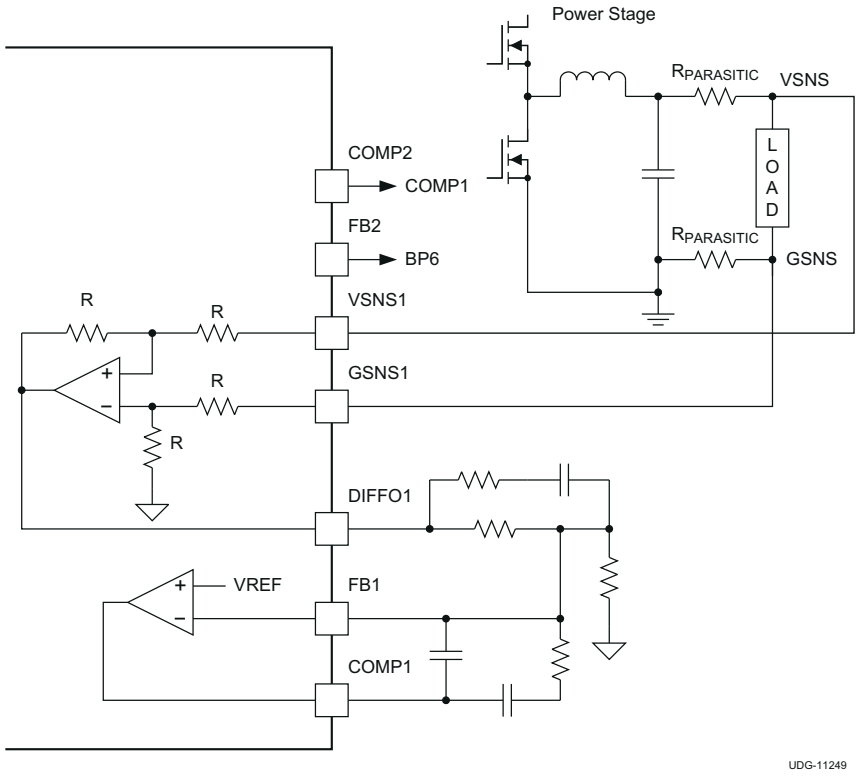



**図 8-6. Connections in a Two-Phase Mode Configuration**

表 8-2 summaries the channel 2 related pin connection in two-phase mode. 図 8-7 shows a typical a two-phase mode application using the TPS4022 device.


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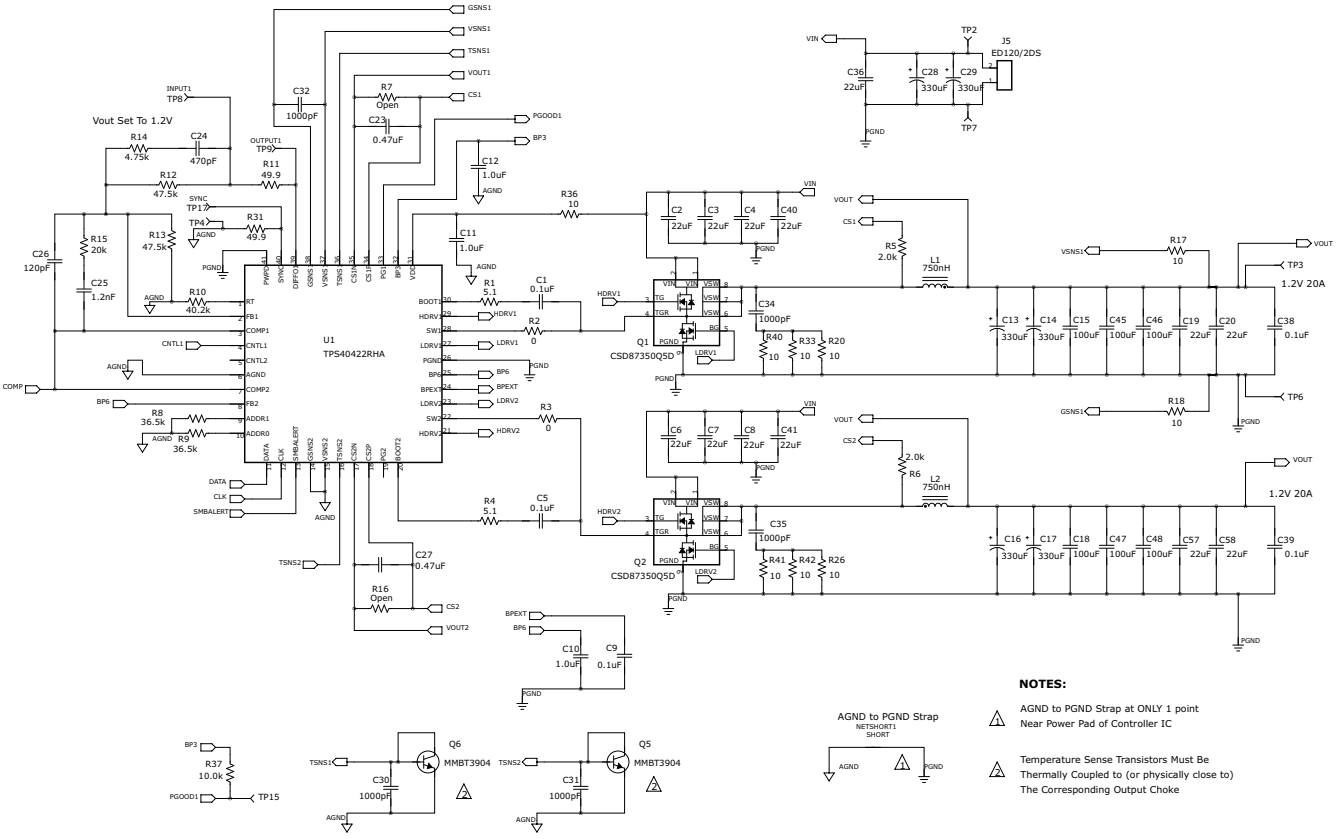



**図 8-7. Using the TPS4022 in a Two-Phase Mode Application**

**表 8-2. Channel 2 Pin Connections in Two-Phase Mode**

| PIN NAME | CONNECTION |
|---|---|
| CNTL2 | Floating or connect to ground |
| COMP2 | Connect to COMP1 |
| FB2 | Connect to BP6 |
| GSNS2 | Connect to ground |
| PG2 | Floating or connect to ground |
| VSNS2 | Connect to ground is recommended. Connect to output voltage is also allowed. |

When the device operates in two-phase mode, a current sharing loop as shown in 図 8-8 is designed to maintain the current balance between phases. Both phases share the same comparator voltage (COMP1). The sensed current in each phase is compared first in a current share block, then compared to an error current and then fed into the COMP pin. The resulting error voltage is compared with the voltage ramp to generate the PWM pulse.

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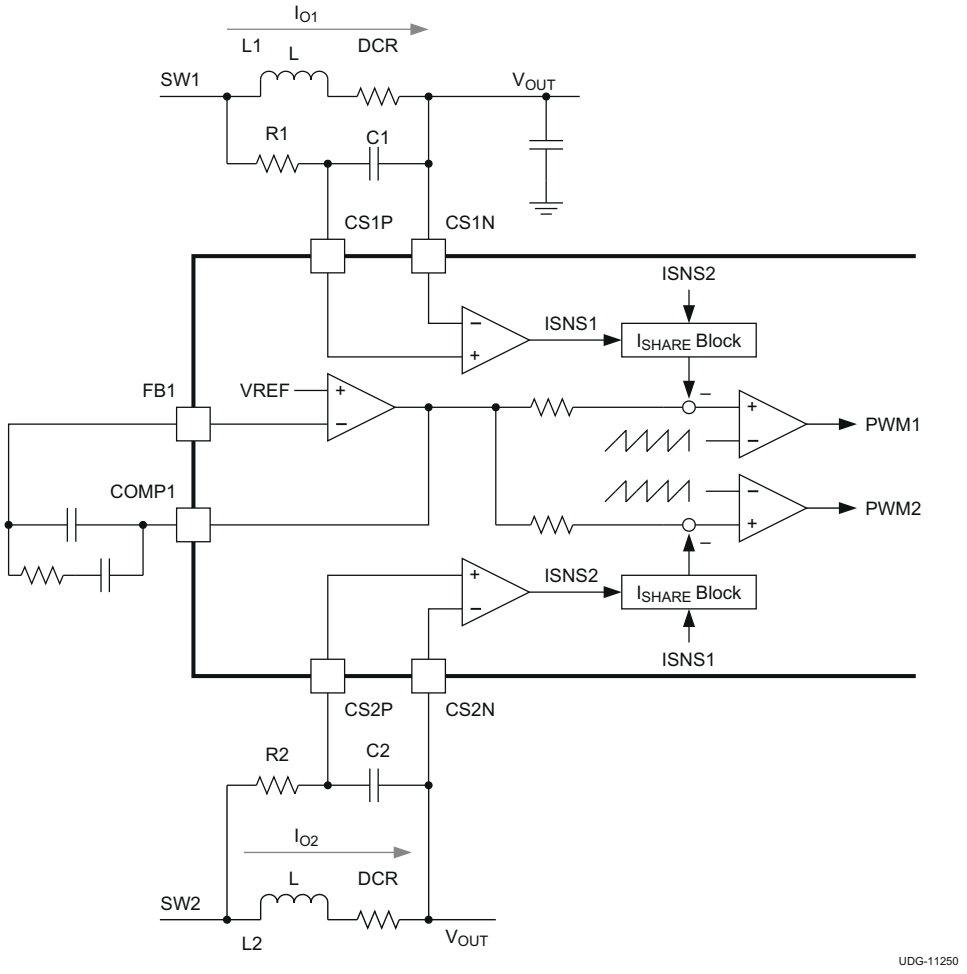



**図 8-8. Two-Phase Mode Current Share Loop**


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## 8.5 Programming

### 8.5.1 Supported PMBus Commands

#### *8.5.1.1 PMBus Address*

The PMBus protocol specification requires that each device connected to the PMBus interface have a unique address on the bus. The TPS4022 device has 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to AGND. The device sets the address in the form of two octal (0-7) digits, one digit for each pin. The ADDR1 pin is the high-order digit and the ADDR0 pin is the low-order digit.

The E48 series resistors suggested for each digit value are shown in 表 8-3.

**表 8-3. E48 Series Resistors**

| DIGIT | RESISTANCE (kΩ) |
|---|---|
| 0 | 11 |
| 1 | 18.7 |
| 2 | 27.4 |
| 3 | 38.3 |
| 4 | 53.6 |
| 5 | 82.5 |
| 6 | 127 |
| 7 | 187 |

The TPS4022 device also detects values that are out of range on the ADDR0 and ADDR1 pins. If either pin is detected as having an out of range resistance connected to it, the device continues to respond to PMBus commands, but at address 127, which is outside of the possible programmed addresses. It is possible but not recommended to use the device in this condition, especially if other TPS4022 devices are present on the bus or if another device could possibly occupy the 127 address.

#### *8.5.1.2 PMBus Connections*

The TPS4022 device supports both 100-kHz and 400-kHz bus speeds. Connection for the PMBus interface should follow the *High Power DC* specifications given in section 3.1.3 on the System Management Bus (SMBus) Specification V2.0 for the 400-kHz bus speed or the *Low Power DC* specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

#### *8.5.1.3 PMBus Data Format*

There are three data formats supported in the PMBus protocol commands that require representation of a literal number as their argument (commands that set thresholds, voltages or report such). A compatible device needs to support only one of these formats. The TPS4022 device supports the *Linear* data format only for these commands. In this format, the data argument consists of two parts, a mantissa and an exponent. The number represented by this argument can be expressed as shown in 式 7.

$$\text{Value} = \text{Mantissa} \times 2^{\text{exponent}} \tag{7}$$

#### 8.5.1.4 PMBus Interface Output Voltage Adjustment

The nominal output voltage of the converter can be adjusted using the VREF_TRIM command. See the VREF_TRIM command description for the format of this command as used in the TPS4022 device . The adjustment range is between -20% and +10% from the nominal output voltage. The VREF_TRIM command is typically used to trim the final output voltage of the converter without relying on high precision resistors being used in 図 8-1. The resolution of the adjustment is 2 mV. The combination of margining and VREF_TRIM is limited to the range between –30% and +10% from the nominal output voltage. Exceeding this range is not supported.

The TPS4022 device operates in three states that determine the actual output voltage:

- No output margin
- Margin high
- Margin low

These output states are set using the OPERATION command. The FB pin reference voltage is calculated as follows in each of these states.

No margin voltage:

$$V_{FB} = VREF_TRIM + 0.6 \tag{8}$$

Margin high voltage state:

$$V_{FB} = STEP_VREF_MARGIN_HIGH + VREF_TRIM + 0.6 \tag{9}$$

Margin low state:

$$V_{FB} = STEP_VREF_MARGIN_LOW + VREF_TRIM + 0.6 \tag{10}$$

where

- $V_{FB}$ is the FB pin voltage
- VREF_TRIM is the offset voltage in volts to be applied to the output voltage
- VREF_MARGIN_HIGH is the requested margin high voltage
- VREF_MARGIN_LOW is the requested margin low voltage

#### 8.5.1.5

For these conditions, the output voltage is shown in 式 11.

$$V_{OUT} = V_{FB} \times \left( \frac{(R2 + R1)}{R2} \right) \tag{11}$$

where

- $V_{FB}$ is the pin voltage calculated in 式 8, 式 9 or 式 10 depending on the output state
- R2 and R1 are in consistent units from 図 8-1
- $V_{OUT}$ is the output voltage

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The device limits the combination of margining and VREF_TRIM to the range between –30% and +10% of the nominal output voltage. The FB pin voltage can deviate no more that this from the nominal 600 mV.


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## 8.6 Register Maps

The TPS4022 device supports commands from the PMBus 1.1 specification as shown in 表 8-4.

**表 8-4. PMBus Command Summary**

| CODE | COMMAND NAME | WORD/ BYTE | DESCRIPTION: PMBus Command | USER WRITABLE | FACTORY DEFAULT VALUE |
|---|---|---|---|---|---|
| 00h | PAGE | Byte | Locates separate PMBus command lists in multiple output environments | Yes | 0XXX XXX0 |
| 01h | OPERATION | Byte | Turn the unit on and off in conjunction with the input from the CONTROL pin. Set the output voltage to the upper or lower MARGIN VOLTAGES. | Yes | 0X00 00XX |
| 02h | ON_OFF_CONFIG | Byte | Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied. | Yes | XXX1 0110 |
| 03h | CLEAR_FAULTS | Byte | Clears all fault status registers to 0x00. The "Unit is Off" bit in the status byte is not cleared when this command is issued. | Yes(1) | NONE |
| 10h | WRITE_PROTECT | Byte | Prevents unwanted writes to the device. | Yes | 000X XXXX |
| 15h | STORE_USER_ALL | Byte | Saves the current configuration into the User Store. Note: This command writes to Non-Volatile Memory. | Yes(1) | NONE |
| 16h | RESTORE_USER_ALL | Byte | Restores all parameters to the settings saved in the User Store. | Yes(1) | NONE |
| 19h | CAPABILITY | Byte | PEC,SPD,ALRT | No | 1011 0000 |
| 20h | VOUT_MODE | Byte | Read-Only Mode Indicator. The data format is linear with an exponent of -9 | No | 0001 0111 |
| 35h | VIN_ON | Word | Sets the value of the input voltage at which the unit should start power conversion | Yes | 1111 0000 0001 0001 |
| 36h | VIN_OFF | Word | Sets the value of the input voltage at which the unit should stop power conversion. | Yes | 1111 0000 0001 0000 |
| 38h | IOUT_CAL_GAIN | Word | Sets the ratio of the voltage at the current sense pins to the sensed current. | Yes | 1000 1000 0001 0000 |
| 39h | IOUT_CAL_OFFSET | Word | Nulls any offsets in the output current sensing circuit. | Yes | 1110 0000 0000 0000 |
| 46h | IOUT_OC_FAULT_LIMIT | Word | Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. | Yes | 1111 1000 0011 1100 |
| 47h | IOUT_OC_FAULT_RESPONSE | Byte | Instructs the device on what action to take in response to an output overcurrent fault. | Yes | 0011 1100 |
| 4Ah | IOUT_OC_WARN_LIMIT | Word | Sets the value of the output current that causes an output overcurrent warning. | Yes | 1111 1000 0011 0110 |
| 4Fh | OT_FAULT_LIMIT | Word | Overtemperature Fault Threshold | Yes | 0000 0000 1001 0001 |
| 5Ih | OT_WARN_LIMIT | Word | Overtemperature Warning Threshold | Yes | 0000 0000 0111 1101 |
| 61h | TON_RISE | Word | Target Soft-Start Rise Time | Yes | 1110 0000 0010 1011 |
| 78h | STATUS_BYTE | Byte | Single byte status indicator | No | 0x00 0000 |

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表 8-4. PMBus Command Summary (continued)

| CODE | COMMAND NAME | WORD/ BYTE | DESCRIPTION: PMBus Command | USER WRITABLE | FACTORY DEFAULT VALUE |
|---|---|---|---|---|---|
| 79h | STATUS_WORD | Word | Full 2-byte status indicator | No | 0000 0000 0x00 0000 |
| 7Ah | STATUS_VOUT | Byte | Output Voltage Fault Status Detail | No | 0000 0000 |
| 7Bh | STATUS_IOUT | Byte | Output Current Fault Status Detail | No | 0000 0000 |
| 7Dh | STATUS_TEMPERATURE | Byte | Temperature Fault Status Detail | No | 0000 0000 |
| 7Eh | STATUS_CML | Byte | Communication, Memory, and Logic Fault Status Detail | No | 0000 0000 |
| 80h | STATUS_MFR_SPECIFIC | Byte | Manufacturer Specific Fault Status Detail. | No | 0000 0000 |
| 8Bh | READ_VOUT | Word | Read output voltage | No | 0000 0000 0000 0000 |
| 8Ch | READ_IOUT | Word | Read output current | No | 1110 0000 0000 0000 |
| 8Eh | READ_TEMPERATURE_2 | Word | Read off-chip temp sensor | No | 0000 0000 0001 1001 |
| 98h | PMBUS_REVISION | Byte | PMBus Revision Information | No | 0001 0001 |
| D0h | MFR_SPECIFIC_00 | Word | User scratch pad | Yes | 0000 0000 0000 0000 |
| D4h | MFR_SPECIFIC_04 | Word | VREF_TRIM | Yes | 0000 0000 0000 0000 |
| D5h | MFR_SPECIFIC_05 | Word | STEP_VREF_MARGIN_HIGH | Yes | 0000 0000 0001 1110 |
| D6h | MFR_SPECIFIC_06 | Word | STEP_VREF_MARGIN_LOW | Yes | 1111 1111 1110 0010 |
| D7h | MFR_SPECIFIC_07 | Byte | PCT_VOUT_FAULT_PG_LIMIT | Yes | 0000 0000 |
| D8h | MFR_SPECIFIC_08 | Byte | SWQUENCE_TON_TOFF_DELAY | Yes | 0000 0000 |
| E5h | MFR_SPECIFIC_21 | Word | IC options | Yes | 0000 0000 0000 0100 |
| FCh | MFR_SPECIFIC_44 | Word | Device Code, Unique Code to ID part number | No | 0000 0000 0111 0100 |

(1) No data bytes are sent, only the command code is sent.

### 8.6.1 Supported Commands

The TPS4022 device supports the following commands from the PMBus protocol 1.1 specification.

#### *8.6.1.1 PAGE (00h)*

The PAGE command provides the ability to configure, control, and monitor both channels (outputs) of the TPS4022 device through only one physical address.

| COMMAND | PAGE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r | r | r | r | r | r | r/w |
| Function | PA | X | X | X | X | X | X | P0 |
| Default Value | 0 | X | X | X | X | X | X | 0 |

表 8-5. PAGE Command Truth Table

| PA | P0 | LOGIC RESULTS |
|---|---|---|
| 0 | 0 | All commands address the first channel |
| 0 | 1 | All commands address the second channel |


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**表 8-5. PAGE Command Truth Table (continued)**

| PA | P0 | LOGIC RESULTS |
|---|---|---|
| 1 | 0 | Illegal input. Ignore this write, take no action |
| 1 | 1 | All commands address both channels |

If PAGE = 11, then any read commands only affect the first channel. Any value written to read-only registers is ignored.

### *8.6.1.2 OPERATION (01h)*

OPERATION is a paged register. The OPERATION command turns the device output on or off in conjunction with input from the CNTLx pins. It is also used to set the output voltage to the upper or lower MARGIN voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CNTLx pins instructs the device to change to another mode.

| COMMAND | OPERATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r | r/w | r/w | r/w | r/w | r | r |
| Function | ON | X | Margin | | | | X | X |
| Default Value | 0 | X | 0 | 0 | 0 | 0 | X | X |

#### 8.6.1.2.1 On

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled. The device is allowed to begin power conversion assuming no fault conditions exist.

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#### 8.6.1.2.2 Margin

If Margin Low is enabled, load the value from the VOUT_MARGIN_LOW command. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH command. (See PMBus specification for more information)

- 00XX: Margin Off
- 0101: Margin Low (Ignore on Fault)
- 0110: Margin Low (Act on Fault)
- 1001: Margin High (Ignore on Fault)
- 1010: Margin High (Act on Fault)

### *8.6.1.3 ON_OFF_CONFIG (02h)*

ON_OFF_CONFIG is a paged register. The ON_OFF_CONFIG command configures the combination of CNTLx pins input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

| COMMAND | ON_OFF_CONFIG | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r/w | r/w | r/w | r/w | r |
| Function | X | X | X | pu | cmd | cpr | pol | cpa |
| Default Value | X | X | X | 1 | 0 | 1 | 1 | 0 |

#### 8.6.1.3.1 pu

The pu bit sets the default to either operate any time power is present or for the on/off to be controlled by CNTLx pins and PMBus OPERATION command. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up.

| Bit Value | ACTION |
|---|---|
| 0 | Channel powers up any time power is present regardless of state of the CNTLx pins. |
| 1 | Channel does not power up until commanded by the CNTLx pins and OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register. |

#### 8.6.1.3.2 cmd

The cmd bit controls how the device responds to the OPERATION command.

| Bit Value | ACTION |
|---|---|
| 0 | Channel ignores the “on” bit in the OPERATION command. |
| 1 | Channel responds to the “on” bit in the OPERATION command. |

#### 8.6.1.3.3 CPR

The CPR bit sets the CNTLx pins response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up.

| Bit Value | ACTION |
|---|---|
| 0 | Channel ignores the CNTLx pins. On/off is controlled only by the OPERATION command. |
| 1 | Channel requires the CNTLx pins to be asserted to start the unit. |

#### 8.6.1.3.4 pol

The pol bit controls the polarity of the CNTLx pins. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to non-volatile memory using the STORE_USER_ALL command and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTLx pins.


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| Bit Value | ACTION |
|---|---|
| 0 | CNTLx pins is active low. |
| 1 | CNTLx pins is active high. |

#### 8.6.1.3.5 CPA

The CPA bit sets the CNTLx pins action when turning the controller off. This bit is read internally and cannot be modified by the user.

| Bit Value | ACTION |
|---|---|
| 0 | Turn off the output using the programmed delay. |

### *8.6.1.4 CLEAR_FAULTS (03h)*

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers in the selected page simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{SMBALERT}}$ signal output if the device is asserting the $\overline{\text{SMBALERT}}$ signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

### *8.6.1.5 WRITE_PROTECT (10h)*

The WRITE_PROTECT command is used to control writing to the PMBus interface device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

| COMMAND | WRITE_PROTECT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | X | X | X | X | X |
| Function | bit7 | bit6 | bit5 | X | X | X | X | X |
| Default Value | 0 | 0 | 0 | X | X | X | X | X |

#### 8.6.1.5.1 bit5

| Bit Value | ACTION |
|---|---|
| 0 | Enable all writes as permitted in bit6 or bit7 |
| 1 | Disable all writes except the WRITE_PROTECT, PAGE, OPERATION and ON_OFF_CONFIG. (bit6 and bit7 must be 0 to be valid data) |

#### 8.6.1.5.2 bit6

| Bit Value | ACTION |
|---|---|
| 0 | Enable all writes as permitted in bit5 or bit7 |
| 1 | Disable all writes except for the WRITE_PROTECT, PAGE and OPERATION commands. (bit5 and bit7 must be 0 to be valid data) |

#### 8.6.1.5.3 bit7

| Bit Value | ACTION |
|---|---|
| 0 | Enable all writes as permitted in bit5 or bit6 |
| 1 | Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data) |

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In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the CML bit in STATUS_WORD being set.

#### *8.6.1.6 STORE_USER_ALL (15h)*

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

EEPROM programming faults cause the device to NACK and set the 'cml' bit in the STATUS_BYTE and the 'oth' bit in the STATUS_CML registers.

#### *8.6.1.7 RESTORE_USER_ALL (16h)*

The RESTORE_USER_ALL command restores all of the storable register settings from EEPROM memory.

This command should not be used while the device is actively switching. If this is done, the device stops switching the output drivers and the output voltage drops. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but it is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. It is strongly recommended that the device be stopped before issuing this command.

#### *8.6.1.8 CAPABILITY (19h)*

The CAPABILTY command provides a way for a host system to determine some key capabilities of this PMBus interface device.

| COMMAND | CAPABILITY | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | PEC | SPD | | ALRT | Reserved | | | |
| Default Value | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

The default values indicate that the TPS4022 device supports Packet Error Checking (PEC), a maximum bus speed of 400 kHz (SPD) and the SMBus Alert Response Protocol using a $\overline{\text{SMBALERT}}$ pin (ALRT).

#### *8.6.1.9 VOUT_MODE (20h)*

The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are set and do not permit the user to change the values.

| COMMAND | VOUT_MODE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | Mode | | | Exponent | | | | |
| Default Value | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

**8.6.1.9.1 Mode:**

Value fixed at 000, linear mode.

**8.6.1.9.2 Exponent**

Value fixed at 10111, Exponent for Linear mode values is –9.


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#### *8.6.1.10 VIN_ON (35h)*

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The supported VIN_ON values are:

| | | | | |
|---|---|---|---|---|
| **4.25 (default)** | 4.5 | 4.75 | 5 | 5.25 |
| 5.5 | 5.75 | 6 | 6.25 | 6.5 |
| 6.75 | 7 | 7.25 | 7.5 | 8 |
| 8.25 | 8.5 | 8.75 | 9 | 9.25 |
| 9.5 | 10 | 10.5 | 11 | 11.5 |
| 12 | 12.5 | 13 | 14 | 15 |
| 16 | | | | |

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

| **COMMAND** | **VIN_ON** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

##### 8.6.1.10.1 Exponent

–2 (dec), fixed.

##### 8.6.1.10.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 17 (dec). This corresponds to a default of 4.25 V.

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### *8.6.1.11 VIN_OFF (36h)*

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_OFF remains unchanged during an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The supported VIN_OFF values are:

| | | | | |
|---|---|---|---|---|
| **4 (default)** | 4.25 | 4.5 | 4.75 | 5 |
| 5.25 | 5.5 | 5.75 | 6 | 6.25 |
| 6.5 | 6.75 | 7 | 7.25 | 7.5 |
| 8 | 8.25 | 8.5 | 8.75 | 9 |
| 9.25 | 9.75 | 10.25 | 10.75 | 11.25 |
| 11.75 | 12 | 13.75 | 14.75 | 15.75 |

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

| **COMMAND** | **VIN_OFF** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

#### 8.6.1.11.1 Exponent

–2 (dec), fixed.

#### 8.6.1.11.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 16 (dec). This corresponds to a default value of 4.0 V.

### *8.6.1.12 IOUT_CAL_GAIN (38h)*

IOUT_CAL_GAIN is a paged register. The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are Ohms (Ω). The effective current sense element can be the DC resistance of the inductor or a separate current sense resistor. The default setting is 0.488 mΩ, and the resolution is 30.5 µΩ. The range is 0.244 mΩ to 15.5 mΩ. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL or STORE_DEFAULT_CODE commands.

| **COMMAND** | **IOUT_CAL_GAIN** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |


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#### 8.6.1.12.1 Exponent

–15 (dec), fixed.

#### 8.6.1.12.2 Mantissa

The upper two bits are fixed at 0.
The lower nine bits are programmable with a default value of 16 (dec).

Depending on the value of IOUT_CAL_GAIN, the current sense amplifier used for current monitoring (but not overcurrent or current sharing) changes, as shown in 表 8-6.

**表 8-6. Current Sense Amplifier Settings**

| IOUT_CAL_GAIN (mΩ) RANGE | | CSA GAIN (V/V) |
|---|---|---|
| MIN | MAX | |
| 0.244 | 0.5795 | 25 |
| 0.5796 | 1.1285 | 15 |
| 1.1286 | 15.5 | 10 |

### *8.6.1.13 IOUT_CAL_OFFSET (39h)*

IOUT_CAL_OFFSET is a paged register. The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amperes. The default setting is 0 A. The resolution of the argument for this command is 62.5 mA and the range is +3937.5 mA to -4000 mA. Values written outside of this range alias into the supported range. For example, 1110 0100 0000 0001 has an expected value of –63.9375 A, but results in 1110 0111 1111 0001 which is –3.9375 A. This occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

| COMMAND | IOUT_CAL_OFFSET | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r/w | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.6.1.13.1 Exponent

–4 (dec), fixed.

#### 8.6.1.13.2 Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (dec).

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### 8.6.1.14 IOUT_OC_FAULT_LIMIT (46h)

IOUT_OC_FAULT_LIMIT is a paged register. The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. The IOUT_OC_FAULT_LIMIT should be set equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALRT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as shown below:

| COMMAND | IOUT_OC_FAULT_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

#### 8.6.1.14.1 Exponent

–1 (dec), fixed.

#### 8.6.1.14.2 Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 60 (dec).

The actual output current for a given mantissa and exponent is shown in 式 12.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \tag{12}$$

The default output fault current setting is 30 A. Values of $I_{OUT(oc)}$ can range between 3 A and 50 A in 500-mA increments.

### 8.6.1.15 IOUT_OC_FAULT_RESPONSE (47h)

IOUT_OC_FAULT_RESPONSE is a paged register. The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or an output voltage undervoltage (UV) fault. The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the IOUT OC Fault bit in the STATUS_IOUT register
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

| COMMAND | IOUT_OC_FAULT_RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r/w | r/w | r/w | r | r | r |
| Function | X | X | RS[2] | RS[1] | RS[0] | X | X | X |
| Default Value | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

#### 8.6.1.15.1 RS[2:0]

000: A zero value for the Retry Setting means that the device does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus specification.)


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111: A one value for the Retry Setting means that the device goes through a normal startup (soft-start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert $\overline{\text{SMBALERT}}$ along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

### *8.6.1.16 IOUT_OC_WARN_LIMIT (4Ah)*

IOUT_OC_WARN_LIMIT is a paged register. The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. When this current level is exceeded the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the IOUT overcurrent Warning (OCW) bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALRT}}$

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALRT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as shown below:

| COMMAND | IOUT_OC_WARN_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

#### 8.6.1.16.1 Exponent

–1 (dec), fixed.

#### 8.6.1.16.2 Mantissa

The upper four bits are fixed at 0.
Lower seven bits are programmable with a default value of 54 (dec).

The actual output warning current level for a given mantissa and exponent is:

$$I_{OUT(OCW)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (13)$$

The default output warning current setting is 27 A. Values of $I_{OUT(OCW)}$ can range from 2 A to 49 A in 500-mA increments.

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### *8.6.1.17 OT_FAULT_LIMIT (4Fh)*

OT_FAULT_LIMIT is a paged register. The OT_FAULT_LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature fault condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the following actions are taken:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Fault bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the over-temperature fault is tripped, the output is latched off until the external sensed temperature falls 20°C below the OT_FAULT_LIMIT, at which point the output goes through a normal startup (soft-start).

The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as asserts the $\overline{\text{SMBALERT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The OT_FAULT_LIMIT takes a two byte data word formatted as shown below.

| COMMAND | OT_FAULT_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

#### 8.6.1.17.1 Exponent

0 (dec), fixed.

#### 8.6.1.17.2 Mantissa

The upper three bits are fixed at 0.
Lower eight bits are programmable with a default value of 145 (dec).

The default over-temperature fault setting is 145°C. Values can range from 120°C to 165°C in 1°C increments.

### *8.6.1.18 OT_WARN_LIMIT (51h)*

OT_WARN_LIMIT is a paged register. The OT_ WARN _LIMIT command sets the value of the temperature, in degrees Celsius, that causes an over-temperature warning condition, when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature warning, the following actions are taken:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Warning bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the over-temperature warning is tripped, warning is latched until the external sensed temperature falls 20°C below the OT_WARN_LIMIT.

The OT_WARN_LIMIT must always be less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than or equal to OT_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALERT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.


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The OT_WARN_LIMIT takes a two byte data word formatted as shown below:

| COMMAND | OT_WARN_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

#### 8.6.1.18.1 Exponent

0 (dec), fixed.

#### 8.6.1.18.2 Mantissa

The upper three bits are fixed at 0.
Lower eight bits are programmable with a default value of 125 (dec).

The default over-temperature fault setting is 125°C. Values can range from 100°C to 140°C in 1°C increments.

### *8.6.1.19 TON_RISE (61h)*

TON_RISE is a paged register. The TON_RISE command sets the time in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. It also determines the rate of the transition of the reference voltage (either due to VREF_TRIM or STEP_VREF_MARGIN_x commands) when this transition is executed during the soft-start period. There are several discrete settings that this command supports. Commanding a value other than one of these values results in the nearest supported value being selected.

The supported TON_RISE times via the PMBus interface are:

- 600 µs
- 900 µs
- 1.2 ms
- 1.8 ms
- **2.7 ms (default value)**
- 4.2 ms
- 6.0 ms
- 9.0 ms

A value of 0 ms instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The TON_RISE command is formatted as a linear mode two’s complement binary integer.

| COMMAND | TON_RISE | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

#### 8.6.1.19.1 Exponent

–4 (dec), fixed.

#### 8.6.1.19.2 Mantissa

The upper two bits are fixed at 0.
The lower eight bits are programmable with a default value of 43 (dec).

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### 8.6.1.20 STATUS_BYTE (78h)

STATUS_BYTE is a paged register. The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults. Three fault bits are flagged in this particular command: output overvoltage, output overcurrent, and over-temperature. The STATUS_BYTE reports communication faults in the CML bit. Other communication faults set the NONE OF THE ABOVE bit.

| COMMAND | STATUS_BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | X | OFF | VOUT_OV | IOUT_OC | VIN_UV | TEMPERATURE | CML | NONE OF THE ABOVE |
| Default Value | 0 | x | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of these bit positions indicates that:

**OFF:**

The device is not providing power to the output, regardless of the reason. In TPS4022 device , this flag means that the converter is not enabled.

**VOUT_OV:**

An output overvoltage fault has occurred.

**IOUT_OC:**

An output over current fault has occurred.

**VIN_UV:**

An input undervoltage fault has occurred.

**TEMPERATURE:**

A temperature fault or warning has occurred.

**CML:**

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

**NONE OF THE ABOVE:**

A fault or warning not listed in bit1 through bits 1-7 has occurred, for example an undervoltage condition or an over current warning condition

### 8.6.1.21 STATUS_WORD (79h)

STATUS_WORD is a paged register. The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

| COMMAND | STATUS_WORD (low byte) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | X | OFF | VOUT_OV | IOUT_OC | VIN_UV | TEMPERATURE | CML | NONE OF THE ABOVE |
| Default Value | 0 | x | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of the low byte (STATUS_BYTE) bit positions indicates that:

**OFF:**

The device is not providing power to the output, regardless of the reason. In TPS4022 device , this flag means that the converter is not enabled.

**VOUT_OV:**

An output overvoltage fault has occurred.


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**IOUT_OC:**

An output over current fault has occurred.

**VIN_UV:**

An input undervoltage fault has occurred.

**TEMPERATURE:**

A temperature fault or warning has occurred.

**CML:**

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

**NONE OF THE ABOVE:**

A fault or warning not listed in bits 1-7 has occurred

| COMMAND | STATUS_WORD (high byte) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | VOUT | IOUT/POUT | X | MFR | $\overline{\text{POWER_GOOD}}$ | X | X | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of the high byte bit positions indicates that:

**VOUT:**

An output voltage fault or warning has occurred

**IOUT/POUT:**

An output current warning or fault has occurred. The PMBus specification states that this also applies to output power. TPS4022 device does not support output power warnings or faults.

**MFR:**

An internal thermal shutdown (TSD) fault has occurred in the device.

**$\overline{\text{POWER_GOOD}}$:**

The power good signal has not transitioned from high-to-low. This is not implemented in two-phase operation.

### *8.6.1.22 STATUS_VOUT (7Ah)*

STATUS_VOUT is a paged register. The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The only bits of this register supported are:

- VOUT_OV Fault
- VOUT_UV Fault

| COMMAND | STATUS_VOUT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | VOUT OV Fault | X | X | VOUT UV Fault | X | X | X | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of these bit positions indicates that:

**VOUT OV Fault:**

The device has seen the output voltage rise above the output overvoltage threshold.

**VOUT UV Fault:**

The device has seen the output voltage fall below the output undervoltage threshold.

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### 8.6.1.23 STATUS_IOUT (7Bh)

STATUS_IOUT is a paged register. The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The only bits of this register supported are .

- IOUT_OC Fault
- IOUT_OC Warning

| COMMAND | STATUS_IOUT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | IOUT_OV Fault | X | IOUT OC Warning | X | X | X | X | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of these bit positions indicates that:

**IOUT_OV Fault:**

The device has seen the output current rise above the level set by IOUT_OC_FAULT_LIMIT.

**VOUT_UV Fault:**

The device has seen the output current rise relating to the level set by IOUT_OC_WARN_LIMIT.

### 8.6.1.24 STATUS_TEMPERATURE (7Dh)

STATUS_TEMPERATURE is a paged register. The STATUS_TEMPERATURE command returns one byte of information relating to the status of the external temperature related faults. The only bits of this register supported are:

- OT Fault
- OT Warning

| COMMAND | STATUS_TEMPERATURE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | OT Fault | OT Warning | X | X | X | X | X | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of these bit positions indicates that:

**OT Fault:**

The measured external temperature has exceeded the level set by OT_FAULT_LIMIT.

**OT Warning:**

The measured external temperature has exceeded the level set by OT_WARN_LIMIT.

### 8.6.1.25 STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the converter's communication related faults. The bits of this register supported by the TPS4022 device are:

- Invalid/Unsuppported Command
- Invalid/Unsupported Data
- Packet Error Check Failed
- Memory Fault Detected
- Other Communication Fault.


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| COMMAND | STATUS_CML | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | Invalid/ Unsuppported Command | Invalid/ Unsupported Data | Packet Error Check Failed | Memory Fault Detected | X | X | Other Communication Fault | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of these bit positions indicates that:

**Invalid/Unsupported Command:**

An invalid or unsupported command has been received.

**Invalild/Unsupported Data**

Invalid or unsupported data has been received

**Packet Error Check Failed**

A packet has failed the CRC error check.

**Memory Fault Detected**

A fault has been detected with the internal memory.

**Other Communication Fault**

Some other communication fault or error has occurred

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### 8.6.1.26 STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command returns one byte of information relating to the status of manufacturer-specific faults or warnings.

| COMMAND | STATUS_MFR_SPECIFIC | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Function | OTFI | X | X | IVADDR | X | X | X | TWOPH_EN |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

A "1" in any of these bit positions indicates that:

**OTFI:**

The internal temperature is above the thermal shutdown (TSD) fault threshold

**IVADDR:**

The PMBus address detection circuit is not resolving to a valid address. In this event, the device responds to the address 127 (dec).

**TWOPH_EN:**

The part has detected that it is in two-phase mode (by pulling FB2 high). This bit does not trigger $\overline{\text{SMBALERT}}$.

### 8.6.1.27 READ_VOUT (8Bh)

READ_VOUT is a paged register. The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the controller. The output voltage is sensed at the remote sense amplifier output pin so voltage drop to the load is not accounted for. The data format is as shown below:

| COMMAND | READ_VOUT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |
| Function | Mantissa | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The setting of the VOUT_MODE affects the results of this command as well. In the TPS4022 device , VOUT_MODE is set to linear mode with an exponent of –9 and cannot be altered. The output voltage calculation is shown in 式 14.

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{14}$$


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### *8.6.1.28 READ_IOUT (8Ch)*

READ_IOUT is a paged register. The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the controller. The output current is sensed across the CSxP and CSxN pins. The data format is as shown below:

| COMMAND | READ_IOUT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The output current is scaled before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA. The IOUT_CAL_GAIN and IOUT_CAL_OFFSET parameters must be set correctly in order to obtain accurate results. The output current can be found by using 式 15.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (15)$$

#### 8.6.1.28.1 Exponent

Fixed at -4.

#### 8.6.1.28.2 Mantissa

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative current is reported as 0 A..

### *8.6.1.29 READ_TEMPERATURE_2 (8Eh)*

READ_TEMPERATURE_2 is a paged register. The READ_TEMPERATURE_2 command returns the external temperature in degrees Celsius of the current channel.

| COMMAND | READ_TEMPERATURE_2 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |
| Function | Exponent | | | | | Mantissa | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

#### 8.6.1.29.1 Exponent

0 (dec), fixed.

#### 8.6.1.29.2 Mantissa

The lower 11 bits are the result of the ADC conversion of the external temperature. The default reading is 25 (dec) corresponding to a temperature of 25°C.

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### 8.6.1.30 PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that the TPS4022 device is compatible with the 1.1 revision of the PMBus protocol specification.

| COMMAND | PMBUS_REVISION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r |
| Default Value | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

### 8.6.1.31 MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 register is dedicated as a user scratch pad.

| COMMAND | MFR_SPECIFIC_00 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | User scratch pad | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

### 8.6.1.32 VREF_TRIM (MFR_SPECIFIC_04) (D4h)

VREF_TRIM is a paged register. The VREF_TRIM command is used to apply a fixed offset voltage to the reference voltage. It is most typically used by the end user to trim the output voltage at the time the PMBus interface device is assembled into the end user system. The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

$$V_{REF\,(offset\,)} = \text{VREF_TRIM} \times 2\ \text{mV} \tag{16}$$

The maximum trim range is -20% to +10% of the nominal reference voltage (600 mV) in 2 mV steps. Permissible values range from -120 mV to +60 mV. If a value outside this range is given with this command, the TPS4022 device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts $\overline{\text{SMBALERT}}$ and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is -180 mV to +60 mV (-30% to +10%). If a value outside this range is given with this command, the TPS4022 device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts $\overline{\text{SMBALERT}}$ and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.


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The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the rate determined by the highest programmable TON_RISE.

| COMMAND | VREF_TRIM | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | | Low Byte | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### *8.6.1.33 STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05) (D5h)*

STEP_VREF_MARGIN_HIGH is a paged register. The STEP_VREF_MARGIN_HIGH command sets the target voltage which the reference voltage changes to when the OPERATION command is set to "Margin High". The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The actual reference voltage commanded by a margin high command can be found by:

$$V_{REF\,(MH)} = (STEP_VREF_MARGIN_HIGH + VREF_TRIM) \times 2\ mV \quad (17)$$

The margin high range is 0% to 10% of the nominal reference voltage (600 mV) in 2-mV steps. Permissible values range from 0 mV to 60 mV. If a value outside this range is given with this command, the TPS4022 device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts $\overline{\text{SMBALERT}}$ and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is -180 mV to 60 mV (-30% to 10%). If a value outside this range is given with this command, the TPS4022 device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts $\overline{\text{SMBALERT}}$ and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the rate determined by the highest programmable TON_RISE.

| COMMAND | STEP_VREF_MARGIN_HIGH | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | | Low Byte | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

The default value of STEP_VREF_MARGIN_HIGH is 30 (dec). This corresponds to a default margin high voltage of 60 mV (±10%) .

### *8.6.1.34 STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06) (D6h)*

STEP_VREF_MARGIN_LOW is a paged register. The STEP_VREF_MARGIN_LOW command sets the target voltage which the reference voltage changes to when the OPERATION command is set to "Margin Low". The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

The actual output voltage commanded by a margin high command is shown in 式 18.

$$V_{REF\,(ML)} = (STEP_VREF_MARGIN_LOW + VREF_TRIM) \times 2\ mV \quad (18)$$

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The margin low range is -20% to 0% of the nominal reference voltage (600 mV) in 2-mV steps. Permissible values range from -120 mV to 0 mV. If a value outside this range is given with this command, the TPS4022 device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts $\overline{\text{SMBALERT}}$ and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible reference voltage adjustment range is -180 mV to 60 mV (-30% to +10%). If a value outside this range is given with this command, the TPS4022 device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts $\overline{\text{SMBALERT}}$ and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The reference voltage transition occurs at the rate determined by the TON_RISE command if the transition is executed during soft-start. Any transition in the reference voltage after soft-start is complete occurs at the rate determined by the highest programmable TON_RISE.

| COMMAND | STEP_VREF_MARGIN_LOW | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w | r/w | r/w | r/w |
| Function | High Byte | | | | | | | | Low Byte | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

The default value of STEP_VREF_MARGIN_LOW is -30 (dec). This corresponds to a default margin low voltage of -60 mV (±10%).

### *8.6.1.35 PCT_VOUT_FAULT_PG_LIMIT (MFR_SPECIFIC_07) (D7h)*

PCT_VOUT_FAULT_PG_LIMIT is a paged register. The PCT_VOUT_FAULT_PG_LIMIT command is used to set the PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) limits as a percentage of nominal.

In two-phase mode, the user can write to PAGE 0 (channel 1) only. Any writes to PAGE 1 are not acknowledged.

The PCT_VOUT_FAULT_PG_LIMIT takes a one byte data word formatted as shown below:

| COMMAND | PCT_VOUT_FAULT_PG_LIMIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r/w | r/w |
| Function | X | X | X | X | X | X | PCT_MSB | PCT_LSB |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) settings are shown in 表 8-7, as a percentage of nominal reference voltage on the FBx pins.

**表 8-7. Protection Settings**

| PCT_MSB | PCT_LSB | UV | PGL LOW | PGL HIGH | PGH HIGH | PGH LOW | OV |
|---|---|---|---|---|---|---|---|
| 0 | 0 | -16.67% | -12.5% | -8.33% | 12.50% | 8.33% | 16.67% |
| 0 | 1 | -12.50% | -8.33% | -4.17% | 8.33% | 4.17% | 12.50% |
| 1 | 0 | -29.17% | -20.83% | -16.67% | 8.33% | 4.17% | 12.50% |
| 1 | 1 | -41.67% | -37.50% | -33.33% | 8.33% | 4.17% | 12.50% |

### *8.6.1.36*

The PGOOD pin can be tripped if the output voltage is too high (using PGH high) or too low (using PGL low). Additionally, the PGOOD pin has hysteresis. When the output trips PGOOD going low (at PGL low), the output


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must rise past PGL high before PGOOD is reset. Likewise, when the output trips PGOOD going high (at PGH high), the output must lower past PGH low before PGOOD is reset.

Additionally, when output overvoltage (OV) is tripped, the output must lower below the PGH low threshold, before PGOOD and OV are reset. Likewise, when output undervoltage (UV) is tripped, the output must rise above the PGOOD high threshold, before PGOOD and UV are reset.

### *8.6.1.37 SEQUENCE_TON_TOFF_DELAY (MFR_SPECIFIC_08) (D8h)*

SEQUENCE_TON_TOFF_DELAY is a paged register. The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and turning off the device as a ratio of TON_RISE.

In two-phase mode, the user can only write to PAGE 0 (channel 1). Any writes to PAGE 1 is not acknowledged.

The SEQUENCE_TON_TOFF_DELAY takes a one byte data word formatted as shown below:

| COMMAND | SEQUENCE_TON_TOFF_DELAY | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r/w | r/w | r/w | r | r/w | r/w | r/w | r |
| Function | TON_DELAY | | | X | TOFF_DELAY | | | X |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### *8.6.1.38*

**TON_DELAY:**

This parameter selects the delay from when the output is enabled until soft-start beings, as a multiple of the TON_RISE time. The default value is 0. Values can range from 0 to 7 in increments of 1.

**TOFF_DELAY:**

This parameter selects the delay from when the output is disabled until the output stops switching, as a multiple of the TON_RISE time. The default value is 0. Values can range from 0 to 7 in increments of 1.

### *8.6.1.39 OPTIONS (MFR_SPECIFIC_21) (E5h)*

The OPTIONS register can be used for setting user selectable options, as shown below.

| COMMAND | OPTIONS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r/w | r/w | r/w |
| Function | X | X | X | X | X | X | X | X | X | X | X | X | X | EN_ADC_CNTL | CH2_DTC | CH1_DTC |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

The contents of this register can be stored to non-volatile memory using the STORE_USER_ALL command.

A “1” in any of these bit positions indicates that:

**EN_ADC_CNTL:**

Enables ADC operation used for voltage, current and temperature monitoring.

**CH2_DTC:**

Increases the non-overlap dead time for gate drivers on channel 2.

**CH1_DTC:**

Increases the non-overlap dead time for gate drivers on channel 1.

### *8.6.1.40 DEVICE_CODE (MFR_SPECIFIC_44) (FCh)*

The DEVICE_CODE command returns a two byte unsigned binary 12-bit device identifier code and 4-bit revision code in the following format.

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| COMMAND | MFR_SPECIFIC_44 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Linear, two's complement binary | | | | | | | | | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |
| Function | Identifier Code | | | | | | | | | | | | Revision Code | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

This command is oriented toward providing similar information to the DEVICE_ID command but for devices that do not support block read and write functions.

#### 8.6.1.40.1 Identifier Code

Fixed at 7 (dec).

#### 8.6.1.40.2 Revision Code

Fixed at 4 (dec).


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# 9 Application and Implementation

注

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## 9.1 Application Information

This design example describes the design process and component selection for a dual-output, synchronous buck, DC/DC converter using the TPS4022 device. The design goal parameters are listed in 表 9-1.

The design procedure provides calculations for channel 1 only.

## 9.2 Typical Application

### 9.2.1 Dual-Output Converter

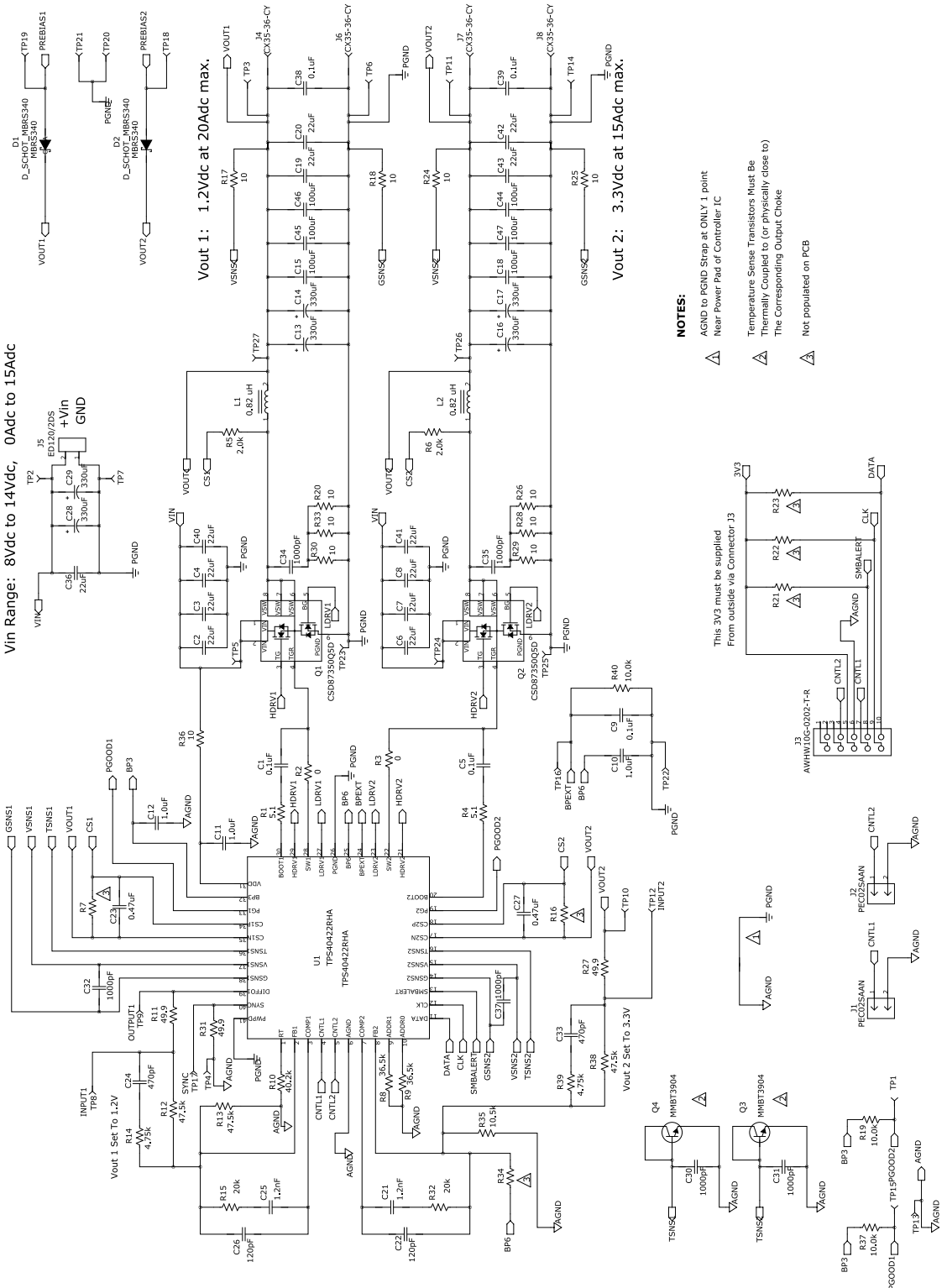



**図 9-1. Typical Application Schematic, TPS4022**

### *9.2.1.1 Design Requirements*

For this design example, use the following input parameters.


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**表 9-1. Design Parameters**

| PARAMETER | | TEST CONDITION | MIN | TYPE | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | | 8 | 12 | 14 | V |
| $V_{IN(ripple)}$ | | $I_{OUT}$ = 20 A | | 0.2 | | V |
| $V_{OUT}$ | Output voltage | | | 1.2 | | V |
| | Line regulation | 8 V ≤ $V_{IN}$ ≤ 14 V | | | 0.5% | |
| | Load regulation | 0 A ≤ $I_{OUT}$ ≤ 20 A | | | 0.5% | |
| $V_{P-P}$ | Output ripple voltage | $I_{OUT}$ = 20 A | | 30 | | mV |
| $\Delta V_{OUT}$ | Output voltage deviation during load transient | $V_{IN}$ = 12 V, $I_{OUT}$ = 10 A | | 60 | | mV |
| $I_{OUT}$ | Output current | 8 V ≤ $V_{IN}$ ≤ 14 V | | | 20 | A |
| $t_{SS}$ | Soft-start time | | | 2.7 | | ms |
| η | Efficiency | $V_{IN}$ = 12 V, $I_{OUT}$ = 20 A | | 88% | | |
| $f_{SW}$ | Switching frequency | | | 500 | | kHz |

### *9.2.1.2 Detailed Design Procedure*

#### 9.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS40422 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

- The WEBENCH Power Designer provides a customized schematic along with a list of materials with real time pricing and component availability. In most cases it offers the ability to:
- In most cases, these actions are available:
  - Run electrical simulations to see important waveforms and circuit performance
  - Run thermal simulations to understand board thermal performance
  - Export customized schematic and layout into popular CAD formats
  - Print PDF reports for the design, and share design with colleagues
- Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 9.2.1.2.2 Step 1: Inductor Selection

The inductor is determined by the desired ripple current. The required inductor is calculated using 式 19.

$$L = \frac{V_{IN\,(max)} - V_{OUT}}{I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN\,(max)}} \times \frac{1}{f_{SW}} = \frac{14\ V - 1.2\ V}{0.2 \times 20A} \times \frac{1.2}{14\ V} \times \frac{1}{500\ kHz} = 0.55\ \mu H \quad (19)$$

Usually the peak-to-peak inductor current $I_{RIPPLE}$ is selected to be approximately 20% of the maximum rated output current. Considering the variation and derating of inductance, the practical inductor choice specifications are:

- Inductance: 0.82 µH
- Current rating: 27 A
- DCR: 0.9 mΩ
- Manufacturer: Wurth

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN\,(max)} \times f_{SW}} \times \frac{V_{IN\,(max)} - V_{OUT}}{L} = \frac{1.2\ V}{14\ V \times 500\ kHz} \times \frac{14\ V - 1.2\ V}{0.82\ \mu H} = 2.68\ A \quad (20)$$

Using the chosen inductor, the real inductor ripple current is 2.68 A. 式 21 calculates the inductor RMS current which is 20.02 A based on $I_{OUT}$ = 20 A and $I_{RIPPLE}$ = 2.68 A.

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$$I_{L(rms)} = \sqrt{I_{OUT(max)}{}^2 + \left(\frac{1}{12}\right) \times (I_{RIPPLE})^2} = \sqrt{(20\ A)^2 + \left(\frac{1}{12}\right) \times (2.68\ A)^2} = 20.02\ A \quad (21)$$

式 22 computes the peak current.

$$I_{L(peak)} = I_{OUT} + \frac{1}{2} \times I_{RIPPLE} = 20\ A + \frac{1}{2} \times 2.68\ A = 21.34\ A \quad (22)$$


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#### 9.2.1.2.3 Step 2: Output Capacitor Selection

The output capacitor is typically selected by the output load transient-response requirement and by allowable output voltage ripple.

- The output capacitor must supply the load with the required current when it is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor affects the magnitude of voltage deviation during the transient.
- The ripple voltage developed across the output capacitor is due to the ripple current in the capacitor and in turn the ripple current is usually due to either the ESR or the value of the capacitor. The ESR of aluminum electrolytics and most tantalums are too high to allow for effective ripple reduction. Often, a combination of several electrolytic capacitors have to be paralleled to obtain large enough value of capacitance with low enough ESR in addition to several ceramic capacitors that offer much lower ESR but at the price of lower capacitance value.

式 23 calculates the minimum output capacitance needed to satisfy overvoltage and undervoltage requirements during the load step. In practical design to account for de-rating and variation it is strongly recommended to multiply the calculated capacitance value by a factor between 1.5 and 5 based on the tests in the actual circuit. In this example, two 330-µF polymer capacitors with ESR of 15 mΩ were chosen as well as three 100-µF ceramic capacitor with ESR of 3 mΩ. The total equivalent capacitance $C_{OUT}$ is 1004 µF. The additional 0.1-µF capacitor ($C_{38}$ and $C_{39}$) is used for filtering of high frequency noise.

$$C_{OUT\,(min)} = \frac{\left(I_{TRAN\,(min)}\right)^2 \times L}{2 \times V_{OUT} \times \Delta V_{OUT}} = \frac{(10\ A)^2 \times 0.82\ \mu H}{2 \times 1.2\ V \times 60\ mV} = 569.4\ \mu F \tag{23}$$

where

- $I_{TRAN(min)}$ is the load transient step
- $\Delta V_{OUT}$ is the output voltage deviation during load transient
- $C_{OUT(min)}$ is the minimum required capacitance

Using the known target output capacitance value, 式 24 calculates the maximum ESR allowed to meet the output voltage ripple specification.

$$ESR_{MAX} = \frac{V_{OUT\,(ripple)} - \left(\frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}\right)}{I_{RIPPLE}} = \frac{30\ mV - \left(\frac{2.68\ A}{8 \times 500\ kHz \times 1004\ \mu F}\right)}{2.68\ A} = 11\ m\Omega \tag{24}$$

#### 9.2.1.2.4 Step 3: Input Capacitance Selection

The input capacitance is selected to handle the ripple current of the buck stage, when the high-side MOSFET switches on, while maintaining the ripple voltage on the supply line low. The input voltage ripple depends on input capacitance and ESR. The minimum capacitor and the maximum ESR can be estimated using the 式 25 and 式 26 because the input ripple is composed of a capacitive portion,$V_{RIPPLE(CIN)}$, and a resistive portion, $V_{RIPPLE(ESR)}$ . In this case, the allowed ripple for the capacitive portion is 0.1 V and for the resistive portion is 0.1 V.

$$C_{IN\,(min)} = \frac{I_{OUT\,(max)} \times V_{OUT}}{V_{RIPPLE\ (CIN)} \times V_{IN\,(max)} \times f_{SW}} = \frac{20\ A \times 1.2\ V}{0.1\ V \times 14\ V \times 500\ kHz} = 34\ \mu F \tag{25}$$

$$ESR_{CIN\,(max)} = \frac{V_{RIPPLE\ (ESR)}}{I_{OUT} + \left({}^{1}/_{2}\right) \times I_{RIPPLE}} = \frac{0.1\ V}{20A + \left({}^{1}/_{2}\right) \times 2.68A} = 4.68\ m\Omega \tag{26}$$

For this design example, five 22-µF, 25-V ceramic capacitors and two 330-µF, 25-V electrolytic capacitors were selected in parallel for the power stage with sufficient margin. The electrolytic capacitors provide better stability during load transients by supplying enough current to the controller.

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#### 9.2.1.2.5 Step 4: MOSFET Selection

The MOSFET selection determines the converter efficiency. In this design, the duty cycle is very small so that the high-side MOSFET is dominated in switching losses and the low-side MOSFET is dominated with conduction losses. To optimize efficiency, choose smaller gate charge for the high-side MOSFET and smaller $R_{DS(on)}$ for the low-side MOSFET.

The MOSFETs were selected and their parameters are listed in 表 9-2.

**表 9-2. MOSFET Selection**

| MOSFET | DEVICE NUMBER | V-RATING (V) | ON-RESISTANCE $R_{DS(on)}$ (mΩ) | GATE CHARGE QG (nC) |
|---|---|---|---|---|
| High-side | CSD87350Q5D | 30 | 5 | 8.4 |
| Low-side | CSD87350Q5D | 30 | 1.2 | 20 |

#### 9.2.1.2.6 Step 5: Snubber Circuit Design

The purpose of the snubber network is to damp the high frequency ringing on the switch node and reduce the peak voltage stress on the low-side FET. A quick and efficient way to design a snubber network is to base it off the allowable power budget to be dissipated. A best practice is to target power dissipation in the output snubber between 0.25% and 0.5% of total power. Normally, the R-C time constant is designed to be short enough such that the capacitor is fully charged or discharged before the next switching edge. In this case, the power dissipation in the snubber resistor is determined only by the capacitor value and independent of the resistor value.

$$E = \left({}^{1}/_{2}\right) \times C_S \times (V_P)^2, \qquad P = \frac{2 \times E}{t_S} = C_S \times \frac{(V_P)^2}{t_S} = C_S \times f_{SW} \times (V_P)^2 \tag{27}$$

where

- peak voltage stored on the capacitors between pulse edges
- $t_S$ is the period
- $f_{SW}$ is the switching frequency
- $C_S$ is the snubber capacitor

The power budget is 1.2 V × 20 A × 0.25% = 60 mW and because the switching frequency is 500 kHz with peak voltage of 14 V, the calculated effective snubber capacitor is 612pF. In this example, to make sure that the ringing is critically damped, a practical value is chosen to be 1000pF for $C_{34}$ and $C_{35}$.

In order to determine the resistor value, the fully charge and discharge time 5 × R × C is set to 10% of the shortest pulse width. Shortest pulse width can be determined using 式 28.

$$t_{ON} = \frac{V_{OUT}}{V_{IN\,(max)}} \times \frac{1}{f_{SW}} = \frac{1.2\ V}{14\ V} \times \frac{1}{500\ kHz} = 171.4\ ns \tag{28}$$

In this design example, three 10-Ω resistors were chosen in parallel to obtain the calculated value and desired form factor. In the EVM schematic, the resistors are $R_{30}$, $R_{33}$, $R_{20}$ and $R_{29}$, $R_{28}$, $R_{26}$.

#### 9.2.1.2.7 Step 6: Soft-Start Time

The TON_RISE command sets the time in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Charging current for the output capacitors needs to be considered when selecting the soft-start time. Based on the output capacitance and output voltage in this example, use 式 29 to calculate the output capacitor charging current.

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.2\ V \times 1004\ \mu F}{2.7\ ms} = 0.45\ A \tag{29}$$


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#### 9.2.1.2.8 Step 7: Peripheral Component Design

##### *9.2.1.2.8.1 RT (Pin 1) Switching Frequency Setting*

$$R_{RT} = \frac{20 \times 10^9}{f_{SW}} = \frac{20 \times 10^9}{500 \times 10^3} = 4\ k\Omega \tag{30}$$

In the PWR091EVM schematic, a practical value of 40.2 kΩ was chosen to set the frequency.

##### *9.2.1.2.8.2 FB1 (Pin 2) and FB2 (Pin 8) Output Voltage Setting*

A feedback divider between the DIFFO pin and AGND sets the output voltage. The components in 図 8-1 that determine the nominal output voltage are $R_1$ and $R_2$.

Calculation for 1.2-V output: Select the high-side resistor ($R_1$) to be 47.5 kΩ and use 式 31 to calculate low-side resistor $R_2$.

$$R_2 = V_{FB} \times \frac{R_1}{V_{OUT} - V_{FB}} = 0.6\ V \times \frac{47.5\ k\Omega}{1.2\ V - 0.6\ V} = 47.5\ k\Omega \tag{31}$$

where

- $V_{FB}$ is the feedback voltage of 600 mV
- $V_{OUT}$ is the desired output voltage of 1.2 V
- $R_1$ and $R_2$ are resistors for the voltage divider from the output to the feedback

##### *9.2.1.2.8.3 Compensation Network Using COMP1 (Pin 3) , COMP2 (Pin 7), FB1 (Pin 2) FB2 DIFFO1 (Pin 8) (Pin 39)*

The TPS4022 device uses voltage mode control topology in a single phase dual-output configuration. In this example, a Type III compensation network is implemented to compensate for the double pole, close the loop and stabilize the system. TI provides a compensation calculator tool to streamline the compensation design process.

The TPS4022 Loop Compensation Tool (SLUC263) provides the recommended compensation components as a starting point and approximate bode plots. It is always recommended to measure the real system bode plot after the design and adjust the compensation values accordingly. The chosen compensation values are derived from the tool calculation along with the Venable K-factor method and optimization based on the measured data.

- $R_1 = R_2 = 47.5\ k\Omega$
- $R_3 = 4.75\ k\Omega$
- $R_4 = 20\ k\Omega$
- $C_1 = 470\ pF$
- $C_2 = 1.2\ nF$
- $C_3 = 120\ pF$

In this design example, the desired crossover frequency chosen is approximately 4 × $f_{DP}$ (20 kHz). Use 式 32 to calculate the double pole frequency formed by the output inductor and capacitor bank.

$$f_{DP} = \frac{1}{2\pi \times \sqrt{LC}} = \frac{1}{2\pi \times \sqrt{820\ nH \times 1004\ \mu F}} = 5547\ Hz \tag{32}$$

Because the Venable K-factor method was used to derive these compensation values, it is important to ensure that the poles and zeroes are coincident. A way to confirm that the poles and zeroes are coincident is to calculate the poles and zeroes from the gain of the Type-III compensation network.

$$GAIN_{TYPE-3} = \frac{R_1 + R_3}{R_1 \times R_3 \times C_3} \times \frac{\left(s + \frac{1}{R_4 \times C_2}\right) \times \left(s + \frac{1}{(R_1 + R_3) \times C_1}\right)}{s \times \left(s + \frac{C_2 + C_3}{R_4 \times C_3 \times C_2}\right) \times \left(s + \frac{1}{R_3 \times C_1}\right)} \tag{33}$$

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The first and second zeroes should yield approximately equal frequency values of 6480 Hz and 6631 Hz.

$$f_{Z1} = \frac{1}{2\pi \times (R_1 + R_3) \times C_1} = \frac{1}{2\pi \times (47.5\ k\Omega + 4.75\ k\Omega) \times 470\ pF} = 6480\ Hz \quad (34)$$

$$f_{Z2} = \frac{1}{2\pi \times R_4 \times C_2} = \frac{1}{2\pi \times 20\ k\Omega \times 1.2\ nF} = 6631\ Hz \quad (35)$$

Analogous to the zeroes being coincident, the first and second poles are coincident as well and are shown in 式 36 and 式 37.

$$f_{P1} = \frac{1}{2\pi \times R_3 \times C_1} = \frac{1}{2\pi \times 4.75\ k\Omega \times 470\ pF} = 71290\ Hz \quad (36)$$

$$f_{P2} = \frac{1}{2\pi \times \left(\frac{R_4 \times C_2 \times C_3}{C_2 + C_3}\right)} = \frac{120\ pF + 1.2\ nF}{2\pi \times 20\ k\Omega \times 120pF \times 1.2\ nF} = 72946\ Hz \quad (37)$$

The resulting compensated system Bode plot is shown in 図 9-4 and the PWR091 EVM user guide (SLVU638). A more comprehensive discussion is presented in *Under the Hood of Low-Voltage DC/DC Converters* from the 2003 TI Power Supply Seminar (SLUP206).

#### *9.2.1.2.8.4 Remote Sensing Using VSNS1 (Pin 37), GSNS1 (Pin 38) , VSNS2 (Pin 15), and GSNS2 (Pin 14)*

The integrated differential amplifier facilitates remote sensing when VSNSx pin(s) and GSNSx pin(s) are configured as the positive and negative inputs. Connect these pins remotely to the load through low-value resistors to the output connector. Including these resistors prevents damage due to potential large negative voltage on output. Standard values chosen for these resistors are between 10 Ω and 50 Ω, depending on the upper and lower values which are based on error in the bias current and power dissipation. The capacitor between the positive and negative sense lines of 1000 pF is added for additional filtering of the noise that could form because the sense lines are typically long.

#### *9.2.1.2.8.5 Temperate Sensing Using TSNS1 (Pin36) and TSNS2 (Pin 16)*

The temperature sensing is accomplished using the relationship between base-emitter voltage and collector current. Local bypass capacitors are recommended for both TSNSx pins. In this design example, the recommended value for both bypass capacitors ($C_{30}$ and $C_{31}$) is 1000 pF.

#### *9.2.1.2.8.6 Current Sensing Network Design Using CS1P (Pin 34), CS1N (Pin 35) , CS2P (Pin 18), and CS2N (Pin 17)*

In this design, current sensing is accomplished using the series resistance of the inductor. In order to do this, a large AC switching voltage forced across the inductor must be filtered out so that the measured voltage is only a DC drop. This filter is implemented via an R-C network directly across the output inductor. The R-C network is chosen such that it provides enough filtering for the application, but in this case the resistor value cannot exceed 2 kΩ in order to keep the error from the CSxN and CSxP pin bias current to a minimum. Also, the time constant of the filter has to match the time constant of the output inductor. Based on the component labels in 図 8-2, the following equation computes the capacitor value.

$$C_4 = \frac{L}{R_{DCR} \times R_5} = \frac{0.82\ \mu H}{0.9\ m\Omega \times 2\ k\Omega} = 0.455\ \mu F \quad (38)$$

A practical capacitor value for the EVM was chosen to be 0.47 µF. The capacitor $C_{27}$ and $C_{23}$ should be placed as close to the CSxP and CSxN pins as possible to provide good bypass filtering. $R_5$ and $R_6$ should be placed close to the inductor to prevent traces with the switch node voltage from being propagated across the board and getting close to sensitive pins.


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#### 9.2.1.2.8.7 PMBus Address ADDR1 (Pin 9) , and ADDR0 (Pin 10)

These two pins are tied to resistors shown in Table 1 based on the desired digit combination that sets specific address for the PMBus protocol to read it. In this design example, a practical resistor value of 36.5kΩ ($R_8$ and $R_9$) was chosen to set the address.

#### 9.2.1.2.8.8 Voltage Decoupling Capacitors

This device offers four pins that are available for DC bias voltage and each requires a small decoupling capacitor for proper functionality

#### 9.2.1.2.8.8.1 VDD (Pin 31)

This device offers four pins that are available for DC bias voltage and each requires a small decoupling capacitor for proper functionality

#### 9.2.1.2.8.8.2 BP3 (Pin 32)

This application requires a 1-µF ceramic capacitor ($C_{12}$) for the internal regulator that supplies to the internal control of the device. Minimum allowed capacitance is 100 nF.

#### 9.2.1.2.8.8.3 BNEXT (Pin 24)

This application requires a 0.1-µF ceramic capacitor ($C_9$) and a 10 kΩ resistor ($R_{40}$) places in parallel to discharge the capacitor.

#### 9.2.1.2.8.8.4 BP6 (Pin 25)

This application requires a 1-µF ceramic capacitor ($C_{10}$) for the internal regulator that supplies power to the gate drivers.

#### 9.2.1.2.8.8.5 Power Good PGOOD1 (Pin 33), PGOOD2 (Pin 19)

This application requires the PGOODx pin to be connected to the BP3 pin with a 10-kΩ resistor ($R_{37}$ and $R_{19}$)

#### 9.2.1.2.8.8.6 Bootstrap Capacitors BOOT1 (Pin 30), and BOOT2 (Pin 20)

This application requires a bootstrap capacitor connected between the BOOT1 pin and the SW1 pin and between the BOOT2 pin and the SW2 pin. The value of the bootstrap capacitor depends on the total gate charge of the high-side MOSFET and the amount of droop allowed on the bootstrap capacitor.

$$C_{BOOT} = \frac{Q_G}{\Delta V} = \frac{8.4\ nC}{0.2\ V} = 42\ nF \tag{39}$$

For this application, a standard value of 100 nF is chosen for the capacitors $C_1$ and $C_5$. In addition, series resistors (R1 and R4) are added to reduce the turn on speed of the high-side MOSFET and control the ringing. This resistor has only a limited effect because at the beginning of the HDRVx gate pulse, when the absolute value of gate voltage is still less than BP6, most of the gate current comes directly from BP6 instead of from the BOOT capacitor.

#### 9.2.1.2.8.8.7 High-Side MOSFET (Gate) Resistor

In order to reduce the voltage spike on switching node further, it is recommended to add a high-side gate resistor and use a Schottky diode in parallel with the resistor (connect anode to gate, and connect cathode to driver) to maintain fast turn off. This application requires a Schottky diode If the gate resistor is more than 3 Ω, so as not to interfere with the anti-cross-conduction circuit.

The MOSFET resistor and Schottky diode are not presented on design sample, but they are recommended if the voltage spike on switching node or BOOT pin is above the absolute maximum rating and need to be reduced to avoid device failure.

#### 9.2.1.2.8.8 Synchronization Setting SYNC (Pin 40)

This pin serves as a logic level input for external clock synchronization. A standard resistor value of 49.9 Ω is chosen for measurement purposes between TP17 and TP4.

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#### *9.2.1.2.8.8.9 BP6 (Pin 25)*

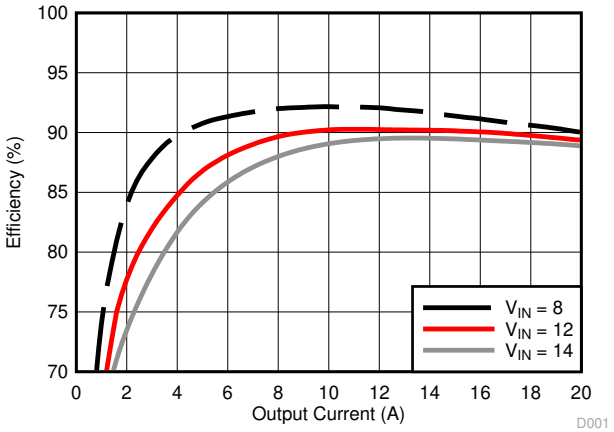
The place holder for R34 resistor is used in the case of two-phase mode. This resistor ties the FB2 pin to the BP6 pin.

#### *9.2.1.2.8.8.10 DIFFO (Pin 39)*

Connected a 49.9-Ω series resistor within in the feedback loop to the DIFFO pin, This resistor is for loop response analysis and it is accessible at the test points for $V_{OUT1}$ (test points TP9 and TP8) and $V_{OUT2}$ (test points TP10 and TP9).

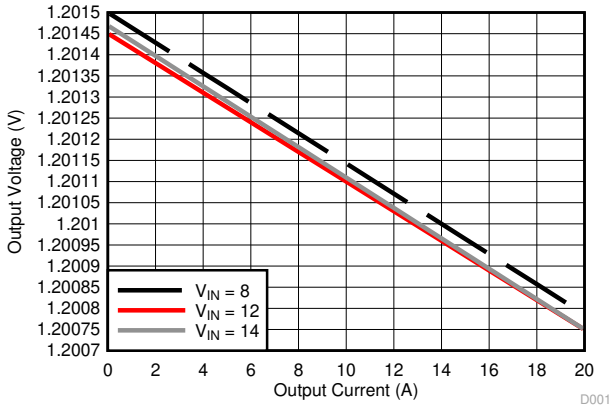

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### 9.2.1.3 Application Curves



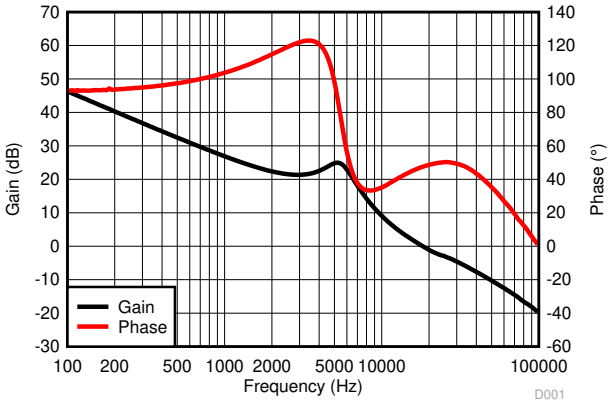

$V_{OUT}$ = 1.2 V

**図 9-2. Efficiency vs Output Current**



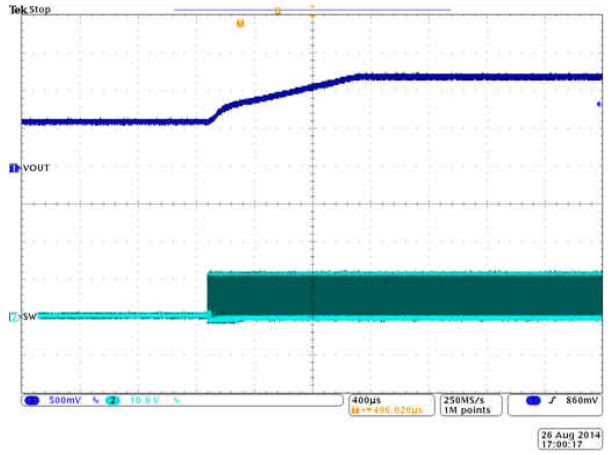

$V_{OUT}$ = 1.2 V

**図 9-3. Line Regulation**



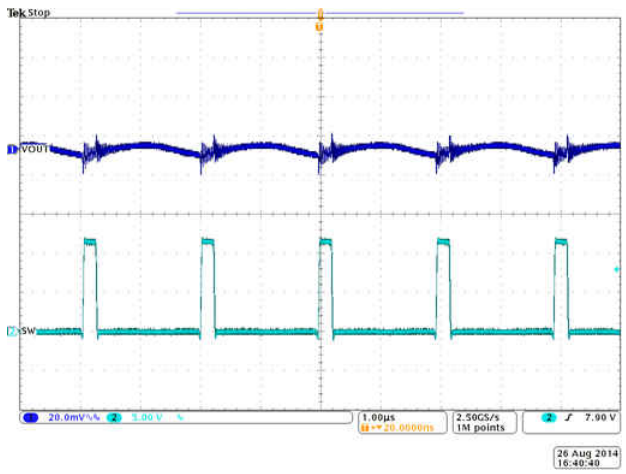

$V_{IN}$ = 12 V $V_{OUT}$ = 1.2 V $I_{OUT}$ = 10 A

**図 9-4. Bode Plot**



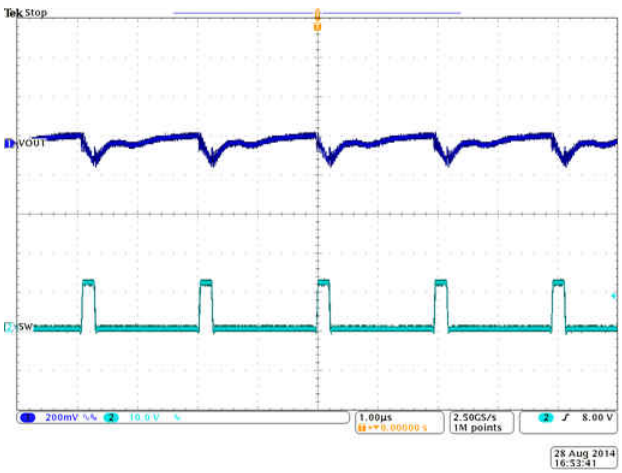

$V_{IN}$ = 12 V $I_{OUT}$ = 0 A

**図 9-5. Prebias Start-Up**



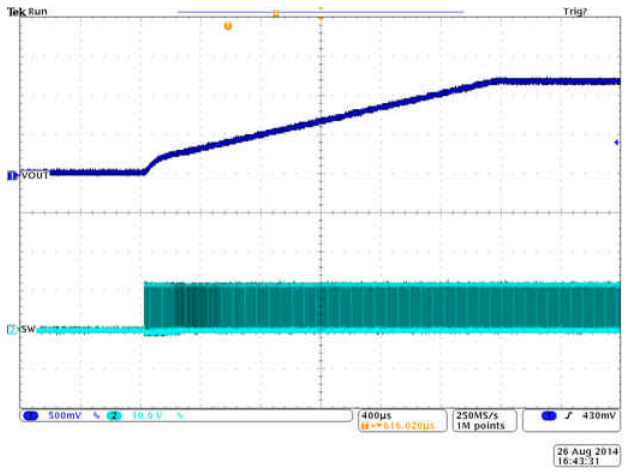

$V_{IN}$ = 12 V $I_{OUT}$ = 20 A

**図 9-6. Output Voltage Ripple**



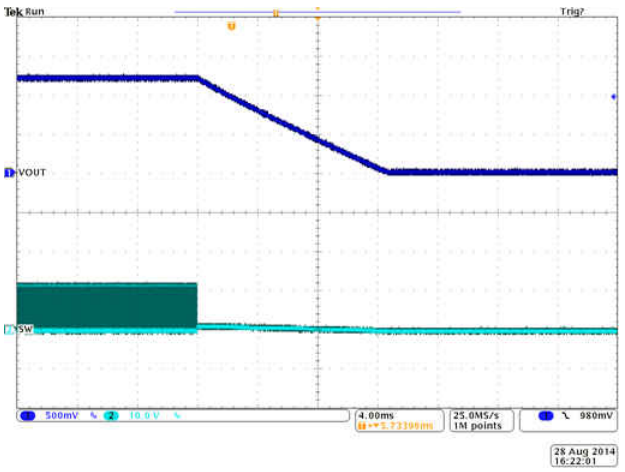

$V_{IN}$ = 12 V $I_{OUT}$ = 20 A

**図 9-7. Input Voltage Ripple**



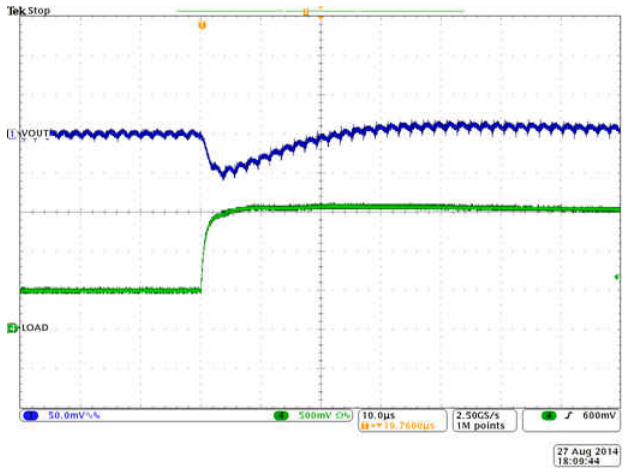

$V_{IN}$ = 12 V $I_{OUT}$ = 0 A

**図 9-8. Start-Up from CNTL**



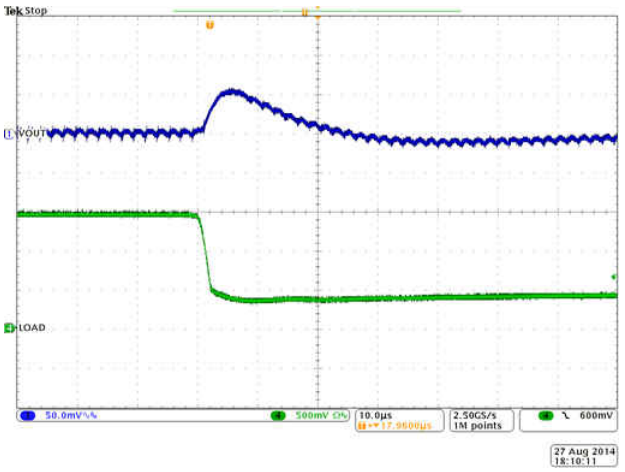

$V_{IN}$ = 12 V $I_{OUT}$ = 0.1 A

**図 9-9. Shutdown from CNTL**




$V_{IN}$ = 12 V $V_{OUT}$ = 1.2 V
$I_{OUT}$ rising from 5 A to 15 A, 5 A/µs

**図 9-10. Load Step-up**




$V_{IN}$ = 12 V $V_{OUT}$ = 1.2 V
$I_{OUT}$ falling from 15 A to 5 A, 5 A/µs

**図 9-11. Load Step-down**

## 10 Power Supply Recommendations

This device is designed to operate from an input voltage supply between 4.5 V and 20 V. There is also input voltage and switch node voltage limitation from MOSFET. The proper bypassing of input supplies is critical for noise performance. See the MOSFET data sheet for more information.


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# 11 Layout

## 11.1 Layout Guidelines

### 11.1.1 PCB Layout Guidelines

Layout is a critical portion of good power supply design. Below are the PCB layout considerations for TPS4022 device .

- If the analog ground (AGND) and power ground (PGND) are separated on the board, the power stage and related components should be terminated or bypassed to the power ground. Signal components of TPS4022 device should be terminated or bypassed to the analog ground. Connect the thermal pad of the TPS4022 device to power ground plane through sufficient vias. Connect AGND and PGND pins of the TPS4022 device to the thermal pad directly. The connection between AGND pin and thermal pad serves as the only connection between analog ground and power ground.
- If one common ground is used on the board, the TPS4022 device and related components must be placed on a noise quiet area which is isolated from fast switching voltage and current paths.
- Maintain placement of signal components and regulator bypass capacitors local to the TPS4022 device. Place them as close as possible to the pins to which they are connected. These components include the feedback resistors, frequency compensation, the RT resistor, ADDR0 and ADDR1 resistors, as well as bypass capacitors for BP3, BP6, and VDD.
- The VSNSx and GSNSx are remotely connected to the load through low ohm resistors, and they must be routed as a differential pair on noise quiet area. Place a high-frequency bypass capacitor between the VSNSx pin and the GSNSx pin, and place the capacitor close to the TPS4022 device.
- The CSxP pin and CSxN pin must be routed as a differential pair on noise quiet area. The resistor of R-C network should be placed close to inductor. The capacitor between CSxP pin and CSxN pin must be placed as close as possible to the TPS4022 device.
- Place the thermal transistor close to the inductor. A bypass capacitor with a value of 1-nF or larger must be placed close to the transistor. Use a separate ground trace for the transistor.

### 11.1.2 MOSFET Layout Guidelines

Below are the MOSFET layout considerations for. Please refer to the data sheet of the MOSFET for more layout information.

- Input bypass capacitors should be physically as close as possible to the VIN and GND pins of the MOSFET device. In addition, a high-frequency bypass capacitor on the MOSFET input voltage pins can help to reduce switching ringing.
- Minimize the SW copper area for best noise performance. Route sensitive traces away from SW, as it contains fast switching voltage and lends easily to capacitive coupling.

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## 11.2 Layout Example

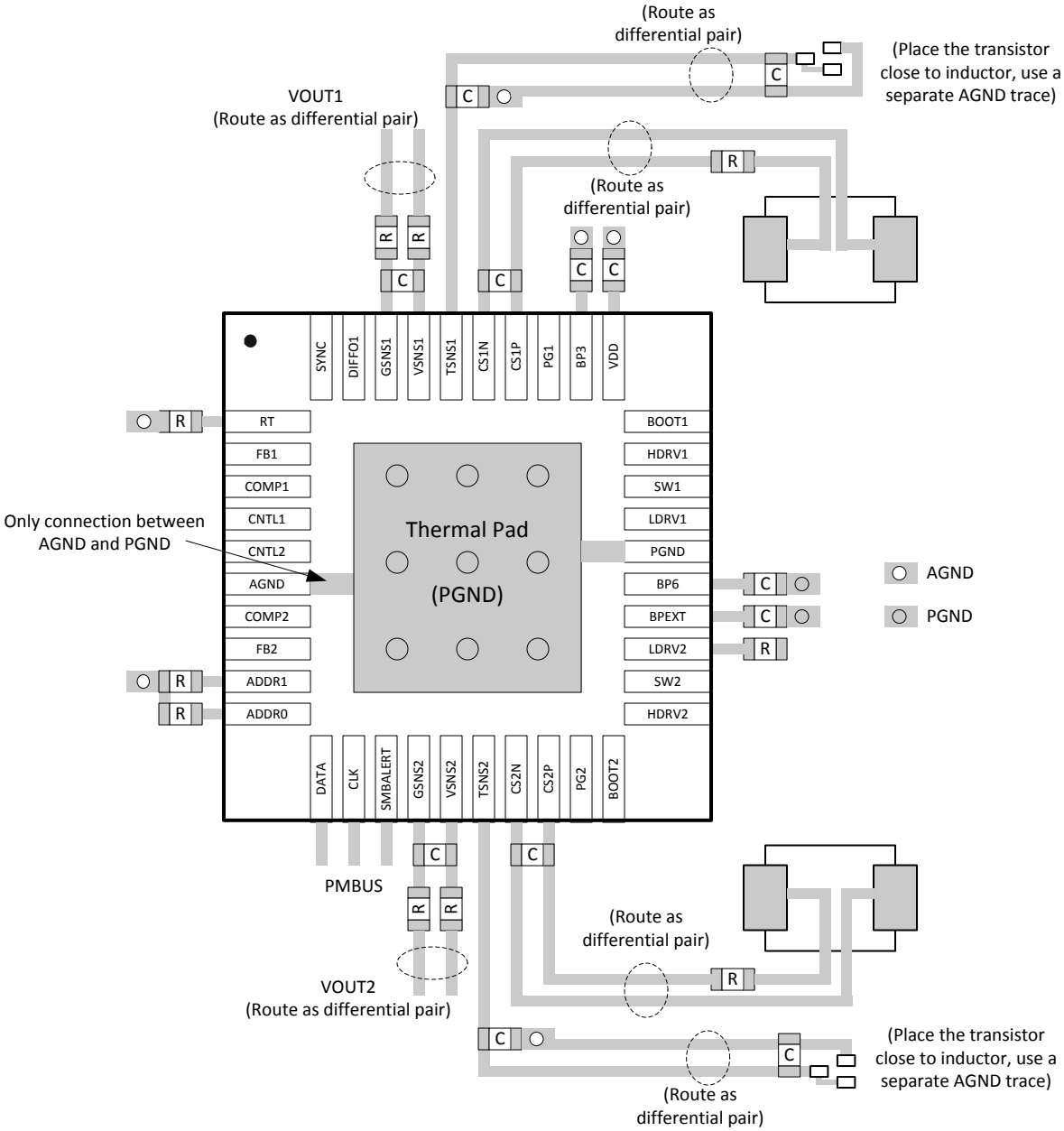



**図 11-1. PCB Layout Recommendation**


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# 12 Device and Documentation Support

## 12.1 Device Support

- *System Management Bus (SMBus) Specification*, Version 2.0, SBS Implementers Forum, August 3, 2000 (http://smbus.org/)

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 サポート・リソース

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## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS40422RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 40422 |
| TPS40422RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 40422 |
| TPS40422RHAT | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 40422 |
| TPS40422RHAT.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 40422 |
| TPS40422RHATG4 | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 40422 |
| TPS40422RHATG4.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 40422 |
| TPS40422RSBR | Active | Production | WQFN (RSB) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS 40422 |
| TPS40422RSBR.A | Active | Production | WQFN (RSB) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS 40422 |
| TPS40422RSBT | Active | Production | WQFN (RSB) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS 40422 |
| TPS40422RSBT.A | Active | Production | WQFN (RSB) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS 40422 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

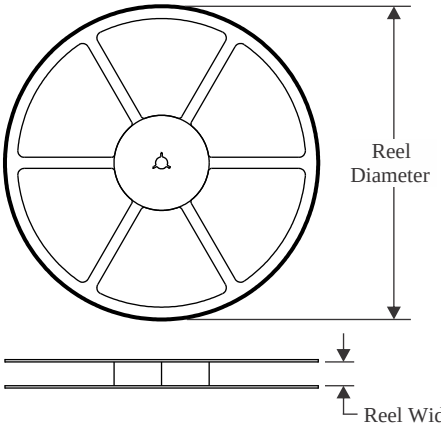
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

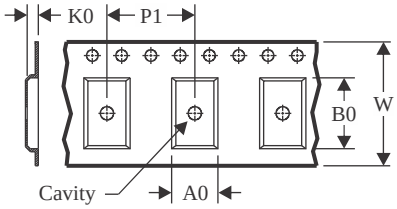
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

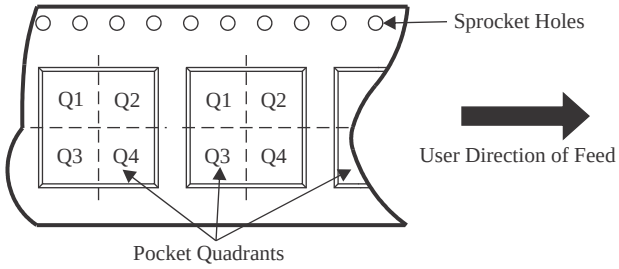



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

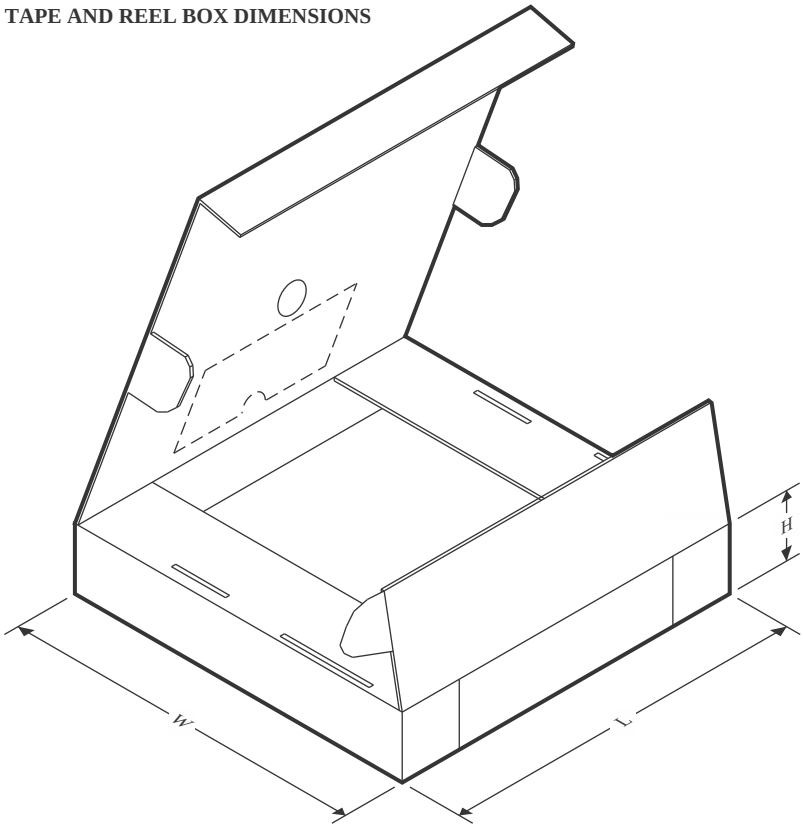
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS40422RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS40422RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS40422RHATG4 | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS40422RSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.25 | 5.25 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS40422RSBT | WQFN | RSB | 40 | 250 | 330.0 | 12.4 | 5.25 | 5.25 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS40422RHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS40422RHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| TPS40422RHATG4 | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| TPS40422RSBR | WQFN | RSB | 40 | 3000 | 338.0 | 355.0 | 35.0 |
| TPS40422RSBT | WQFN | RSB | 40 | 250 | 338.0 | 355.0 | 35.0 |

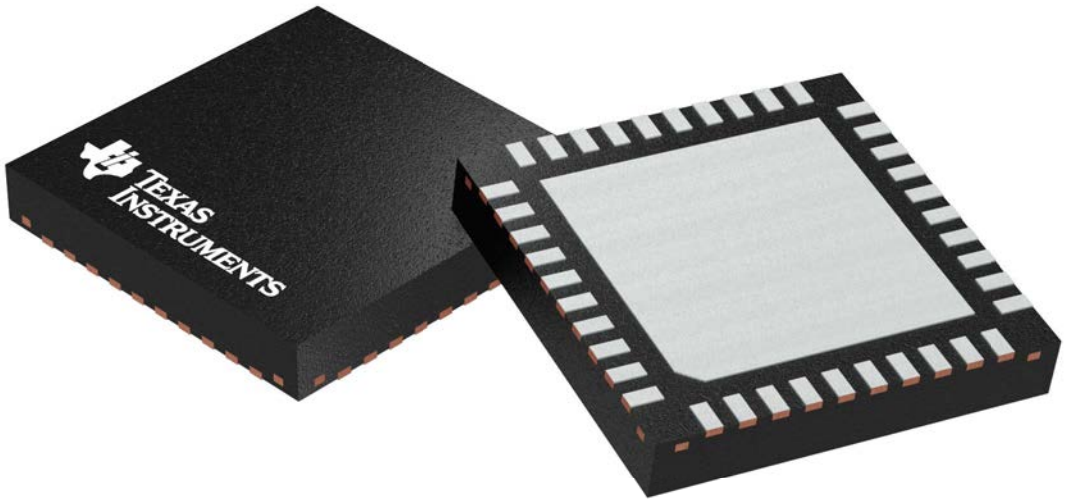
# GENERIC PACKAGE VIEW

## RSB 40

## WQFN - 0.8 mm max height

**5 x 5 mm, 0.4 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# GENERIC PACKAGE VIEW

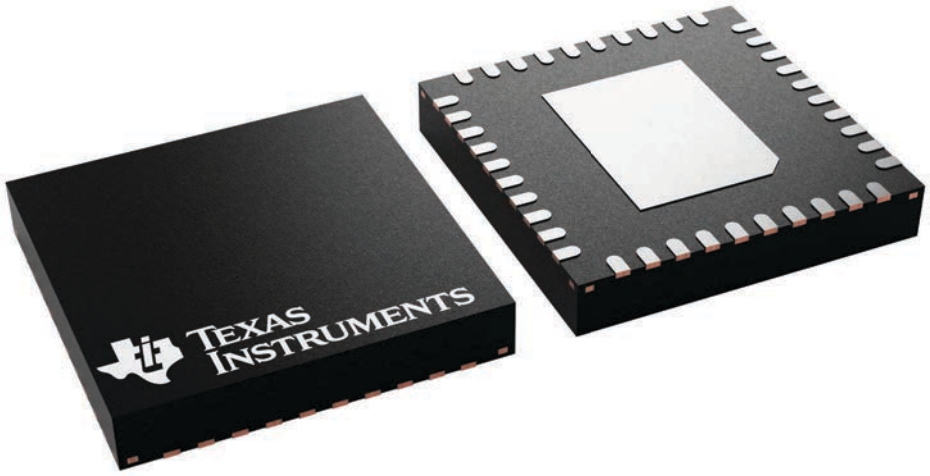
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225870/A

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