TPS50301A-HT 1.6V～6.3V 入力、3A 同期整流降圧型コンバータ

1 特長

- ピーク効率：95% (V_O = 3.3V)
- 55mΩ/50mΩ の MOSFET を内蔵
- 分割電源レール：PVIN 上で 1.6～6.3V
- 電源レール：VIN 上で 3～6.3V
- 3A
- フレキシブルなスイッチング周波数オプション:
  - 100kHz～1MHzの可変内部発振回路
  - 外部同期機能: 100kHz～1MHz
  - マスタ/スレーブ・アプリケーション用に SYNC ピンを 500kHz 出力として構成可能
- 25℃ で 0.795V ±1.258% の基準電圧
- プリバイアスされた出力への単調スタートアップ
- 調整可能なスロー・スタートと電源シーケンス
- 低電圧および過電圧用のパワーグッド出力モニタ
- 可変の入力低電圧誤動作防止(UVLO)
- 20 ピンの熱的に強化されたセラミック・フラットパック・パッケージ (HKH)
- 「ツールとソフトウェア」タブを参照
- WEBENCH® Power Designer により、TPS50301-HT を使用するカスタム設計を作成

2 アプリケーション

- ポイント・オブ・ロード・レギュレーション
- ダウンホール・ドリル
- 過酷な動作環境向け
- 極めて広い温度範囲(－55℃～210℃)で利用可能(1)
- TI の高温動作製品は、高度に最適化されたシリコン (ダイ) ソリューションの採用と、設計およびプロセスの拡張により、拡張温度範囲で最大限の性能を実現

3 概要

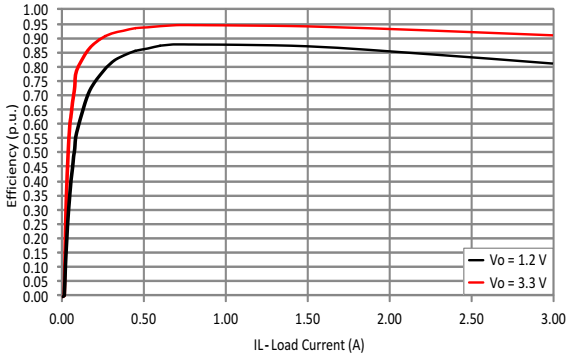
TPS50301-HT は 6.3V、3A 同期整流降圧型コンバータであり、高効率とハイサイド/ローサイド MOSFET 内蔵により、小型設計向けに最適化されています。電流モード制御による部品数の削減と、高いスイッチング周波数によるインダクタ・サイズの縮小により、さらに省スペースを実現できます。これらのデバイスは、放熱特性を強化した 20 ピンのセラミック・デュアル・インライン・フラットパック・パッケージに封止されています。

製品情報(2)

型番	パッケージ	本体サイズ(公称)
TPS50301-HT	CFP (20)	7.38×12.70mm
	KGD(3)	N/A(4)

(1) 温度範囲をカスタマイズ可能。
(2) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(3) 品質保証のベア・ダイ。
(4) ワッフル・パックのベア・ダイ。

効率と負荷電流との関係：V_{IN} = 5V



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision J (December 2016) から Revision K に変更 **Page**

- 編集上の変更のみ、技術上の変更なし ... 1
- WEBENCH のリンクを追加 ... 1

Revision I (December 2015) から Revision J に変更 **Page**

- タイトルから 6A を 削除 ... 1
- データシート全体を通して、出力電流 6A の記述を 3A に 変更 ... 1
- 追加「*ドキュメントの更新通知を受け取る方法*」セクション ... 39

Revision H (July 2015) から Revision I に変更 **Page**

- データシートから型番を削除 ... 1
- Updated EN and PWRGD pin description ... 4
- Removed the ψ_{JT} thermal metric ... 9

Revision G (December 2014) から Revision H に変更 **Page**

- Updated backside potential to ground ... 5
- Updated bare die image ... 5
- Corrected test condition from "90% to 90%" to "10% to 90%" ... 10
- Added test conditions for 5962R1022102V9A part maximums ... 10
- Added information for the 5962R1022102V9A enable threshold, voltage reference, internally set frequency, minimum on time, and SS/TR to VSENSE matching ... 10
- Corrected test condition from "90% to 90%" to "10% to 90%" ... 10
- Updated hysteresis for VIN UVLO threshold to 50 mV typical ... 18
- Added parameter units to Equation 6 ... 20

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- Updated Iss value to 2.5 µA typical 32
- Updated Ontimemin for Equation 32 from "135" to "175" ns maximum 33

Revision F (November 2013) から Revision G に変更 **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 1
- Added *Bare Die Information* and Bond Pad Coordinates in Microns table 5

Revision E (May 2013) から Revision F に変更 **Page**

- 「*特長*」セクション 変更 1

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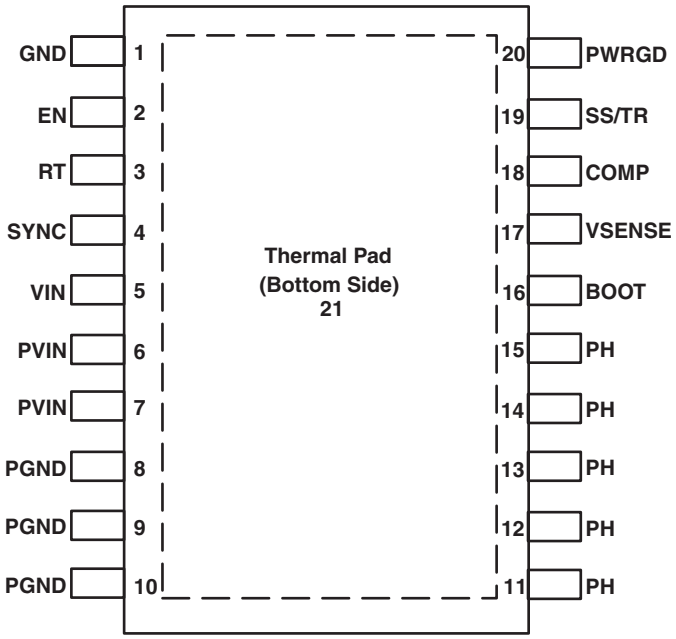
5 概要（続き）

出力電圧のスタートアップ・ランプは SS/TR ピンにより制御されるため、スタンドアロンの電源またはトラッキング状況で動作できます。イネーブルおよびオープン・ドレインのパワーグッド・ピンを適切に構成することにより、電源シーケンシングも可能です。

ハイサイドFETにサイクル単位の電流制限を適用することで過負荷状況からデバイスを保護し、ローサイドのソース電流制限により電流暴走を防止して、さらに保護が強化されています。また、ローサイドのシンク電流制限によりローサイドMOSFETをオフにすることで、過度な逆方向電流を防止します。ダイの温度がサーマル・シャットダウン温度を超えると、サーマル・シャットダウンによりデバイスがディセーブルになります。

6 Pin Configuration and Functions

HKH Package
20-Pin CFP
Bottom View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	GND	Return for control circuitry (1).
2	EN	EN pin has an internal pullup thus EN pin can be floated to enable the device. As an option external pullup can also be added if desired. Adjust the input undervoltage lockout (UVLO) with two resistors.
3	RT	In internal oscillation mode, a resistor is connected between the RT pin and GND to set the switching frequency.
4	SYNC	Optional 1-MHz external system clock input. The device operates with an internal oscillator if this pin is left open.
5	VIN	Supplies the power to the output FET controllers.
6	PVIN	Power input. Supplies the power switches of the power converter.
7		
8	PGND	Return for low-side power MOSFET.
9		
10		

(1) GND (pin 1 - analog ground) must be connected to PGND external to the package. Thermal pad must be connected to a heat dissipating layer. Thermal pad is internally connected to the seal ring and GND.

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Pin Functions (continued)

PIN		DESCRIPTION
NO.	NAME	
11	PH	Switch node.
12		
13		
14		
15		
16	BOOT	A bootstrap capacitor is required between BOOT and PH. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET.
17	VSENSE	Inverting input of the gm error amplifier.
18	COMP	Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.
19	SS/TR	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
20	PWRGD	Power Good fault pin is an open-drain connection. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during slow start.

Table 1. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Ground	Al5TiN	557.5 nm

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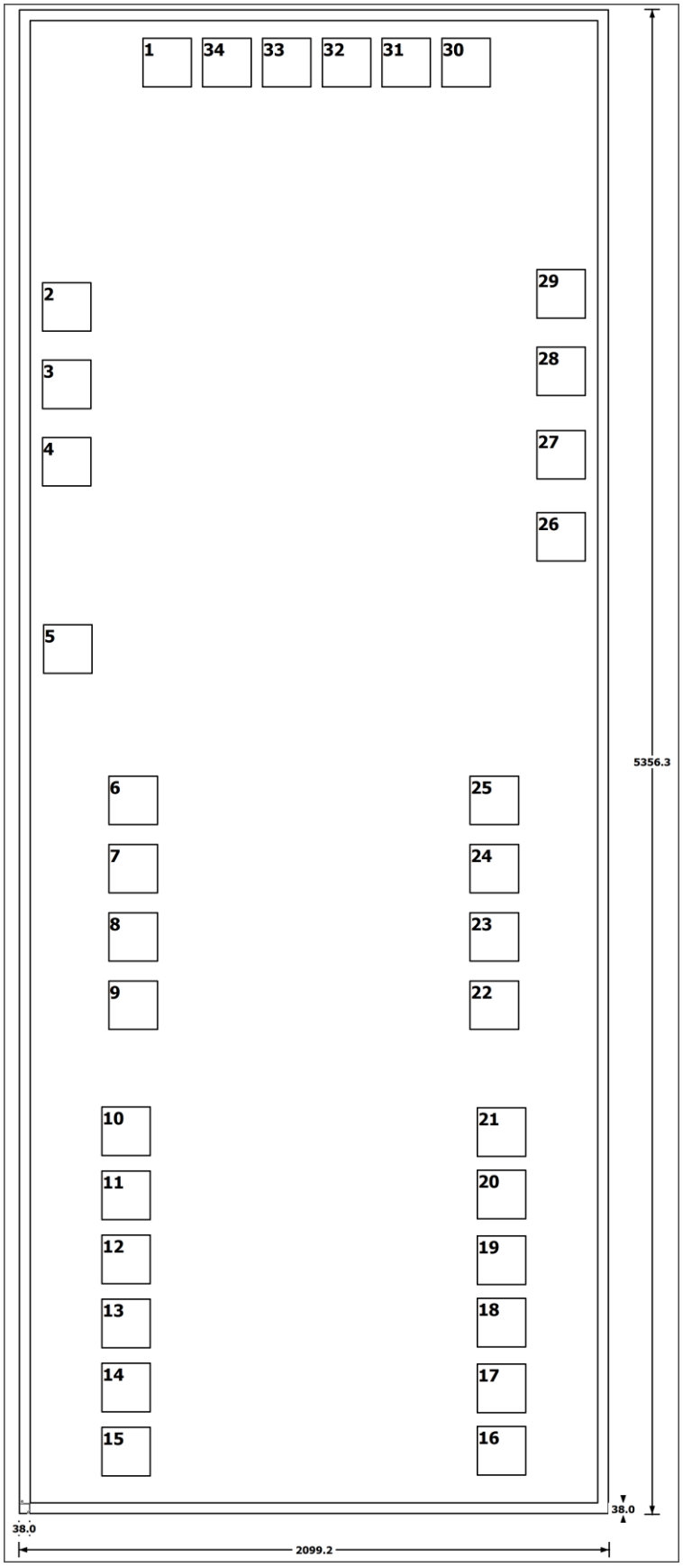

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Table 2. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
GND	1	400.77	5039.325	578.07	5216.625
EN	2	44.19	4169.79	221.49	4347.09
RT	3	44.19	3894.21	221.49	4071.51
SYNC	4	44.19	3618.63	221.49	3795.93
VIN	5	47.565	2952.27	224.865	3129.57
PVIN	6	280.215	2414.115	457.515	2591.415
PVIN	7	280.215	2170.665	457.515	2347.965
PVIN	8	280.215	1928.115	457.515	2105.415
PVIN	9	280.215	1684.665	457.515	1861.965
PGND	10	254.52	1236.285	431.82	1413.585
PGND	11	254.52	1008.315	431.82	1185.615
PGND	12	254.52	780.345	431.82	957.645
PGND	13	254.52	552.375	431.82	729.675
PGND	14	254.52	324.405	431.82	501.705
PGND	15	254.52	96.435	431.82	273.735
PH	16	1590.12	99.405	1767.42	276.705
PH	17	1590.12	321.435	1767.42	498.735
PH	18	1590.12	555.345	1767.42	732.645
PH	19	1590.12	777.375	1767.42	954.675
PH	20	1590.12	1011.285	1767.42	1188.585
PH	21	1590.12	1233.315	1767.42	1410.615
PH	22	1564.335	1684.665	1741.635	1861.965
PH	23	1564.335	1928.115	1741.635	2105.415
PH	24	1564.335	2170.665	1741.635	2347.965
PH	25	1564.335	2414.115	1741.635	2591.415
BOOT	26	1801.71	3352.14	1979.01	3529.44
VSENSE	27	1801.71	3644.145	1979.01	3821.445
COMP	28	1801.71	3940.92	1979.01	4118.22
SS/TR	29	1801.71	4216.5	1979.01	4393.8
PWRGD	30	1463.67	5039.325	1640.97	5216.625
GND	31	1251.09	5039.325	1428.39	5216.625
GND	32	1038.51	5039.325	1215.81	5216.625
GND	33	825.93	5039.325	1003.23	5216.625
GND	34	613.35	5039.325	790.65	5216.6

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7	V
	PVIN	–0.3	7	
	EN	–0.3	5.5	
	BOOT	–0.3	14	
	VSENSE	–0.3	3.3	
	COMP	–0.3	3.3	
	PWRGD	–0.3	5.5	
	SS/TR	–0.3	5.5	
	SYNC	–0.3	7	
Output voltage	BOOT-PH	0	7	V
	PH	–1	7	
	PH 10-ns transient	–3	7	
Vdiff	(GND - Analog Ground to PGND)	–0.2	0.2	V
Output current			3	A
Source current	PH	Current limit		A
	RT		±100	µA
Sink current	PH	Current limit		A
	PVIN	Current limit		A
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature		–55	220	°C
Storage temperature, T_{stg}		–65	220	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction operating temperature range	–55		125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		TPS50301-HT HKH (CFP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.929	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.066	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.445	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.514	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –55°C to 210°C, VIN = 3 to 6.3 V, PVIN = 1.6 to 6.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)						
PVIN operating input voltage			1.6		6.3	V
VIN operating input voltage			3		6.3	V
VIN internal UVLO threshold	V_{IN} rising			2.75	3	V
VIN internal UVLO hysteresis				50		mV
VIN shutdown supply current	EN = 0 V			2.5	8	mA
VIN operating – non-switching supply current	$V_{SENSE} = V_{BG}$			5	10	mA
ENABLE AND UVLO (EN PIN)						
Enable threshold	Rising			1.13	1.19	V
Enable threshold	Falling		0.97	1.03		V
Input current	V_{EN} = 1.1 V			3.2		µA
Hysteresis current	V_{EN} = 1.3 V			3		µA
VOLTAGE REFERENCE						
Voltage reference	0 A ≤ Iout ≤ 3 A	–55°C	0.767	0.795	0.805	V
		25°C	0.785	0.795	0.805	
		210°C	0.785	0.795	0.830	
MOSFET						
High-side switch resistance	BOOT-PH = 2.2 V			55		mΩ
High-side switch resistance(1)(2)	BOOT-PH = 6.3 V			50		mΩ
Low-side switch resistance(1)(2)	V_{IN} = 3 V			50		mΩ
ERROR AMPLIFIER						
Error amplifier transconductance (gm)(2)	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V			1300		µS
Error amplifier dc gain(2)	V_{SENSE} = 0.8 V			39000		V/V
Error amplifier source/sink(2)	$V_{(COMP)}$ = 1 V, 40 mV input overdrive			±125		µA
Start switching threshold(2)				0.25		V
COMP to Iswitch gm(2)				18		A/V
CURRENT LIMIT						
High-side switch current limit threshold	V_{IN} = 6.3 V		7.8	11		A
Low-side switch sourcing current limit	V_{IN} = 6.3 V		6	10		A
Low-side switch sinking current limit	V_{IN} = 6.3 V			3		A
INTERNAL SWITCHING FREQUENCY						
Internally set frequency	RT = Open		395	500	585	kHz

(1) Measured at pins
(2) Ensured by design only. Not tested in production.

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Electrical Characteristics (continued)

T_J = –55°C to 210°C, VIN = 3 to 6.3 V, PVIN = 1.6 to 6.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Externally set frequency	RT = 100 kΩ (1%)		480		kHz
	RT = 485 kΩ (1%)		100		
	RT = 47 kΩ (1%)		1000		
EXTERNAL SYNCHRONIZATION					
SYNC out low-to-high rise time (10%/90%)	Cload = 25 pF		25	126	ns
SYNC out high-to-low fall time (90%/10%)	Cload = 25 pF		3	15	ns
Falling edge delay time(3)			180		°
SYNC out high-level threshold	I_{OH} = 50 µA	2			V
SYNC out low-level threshold	I_{OL} = 50 µA			600	mV
SYNC in low-level threshold		800			mV
SYNC in high-level threshold				1.85	V
SYNC in frequency range	Percent of program frequency	–5%		5%	
		100		1000	kHz
PH (PH PIN)					
Minimum on time	Measured at 10% to 90% of VIN, 25°C, I_{PH} = 2 A		94	236	ns
Minimum off time	BOOT-PH ≥ 2.2 V		500		ns
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.2	3	V
SLOW START AND TRACKING (SS/TR PIN)					
SS charge current			2.5		µA
SS/TR to V_{SENSE} matching	$V_{(SS/TR)}$ = 0.4 V		30	90	mV
POWER GOOD (PWRGD PIN)					
V_{SENSE} threshold	V_{SENSE} falling (fault)		91		% Vref
	V_{SENSE} rising (good)		94		% Vref
	V_{SENSE} rising (fault)		109		% Vref
	V_{SENSE} falling (good)		106		% Vref
Output high leakage	V_{SENSE} = Vref, $V_{(PWRGD)}$ = 5 V		0.03	2.9	µA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum V_{IN} for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.4	V

(3) Bench verified. Not tested in production.

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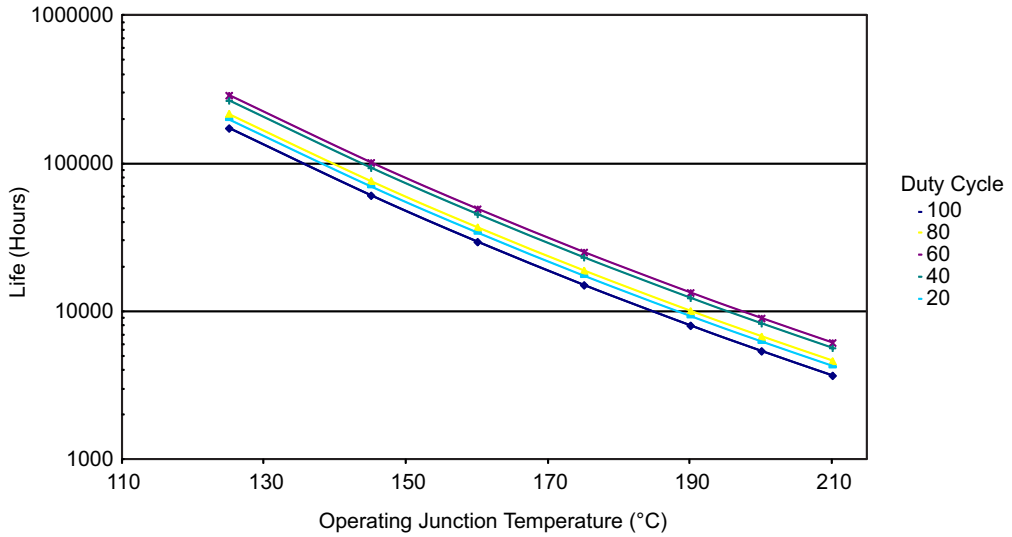
7.6 Dissipation Ratings

See (1)(2)(3)(4)(5)

PACKAGE	$R_{\theta JA}$ THERMAL IMPEDANCE, JUNCTION TO AMBIENT	$R_{\theta JC}$ THERMAL IMPEDANCE, JUNCTION TO CASE (THERMAL PAD)	$R_{\theta JB}$ THERMAL IMPEDANCE, JUNCTION TO BOARD
HKH	39.9°C/W	0.52°C/W	43.1°C/W

(1) Maximum power dissipation may be limited by overcurrent protection
(2) Power rating at a specific ambient temperature, T_A, should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See power dissipation estimate in *Application and Implementation* for more information.
(3) Test board conditions:
  (a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
  (b) 2-oz. copper traces located on the top of the PCB
  (c) 2-oz. copper ground planes on the 2 internal layers and bottom layer
  (d) 40.010-inch thermal vias located under the device package
(4) For information on thermal characteristics, see SPRA953.
(5) Use polyimide PCB and thermal management to ensure operation below maximum T_J operation.



A. See data sheet for absolute maximum and minimum recommended operating conditions.
B. Silicon operating life design goal is 10 years at 125°C junction temperature (does not include package interconnect life).
C. The predicted operating lifetime versus junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.
D. This device is rated for 1000 hours of continuous operation at maximum rated temperature at 210°C.

Figure 1. 3-A Continuous Current Estimated Device Life

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7.7 Typical Characteristics

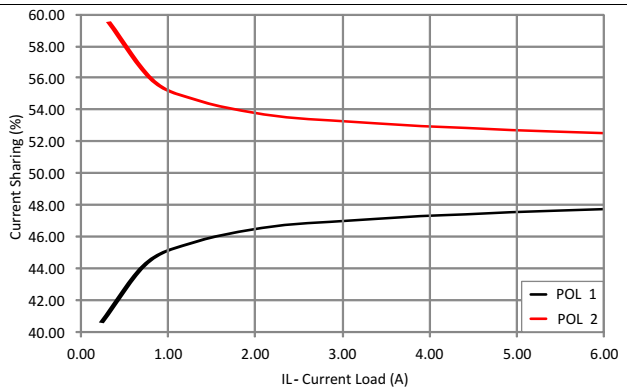

Figure 2. Current Sharing vs Load Current

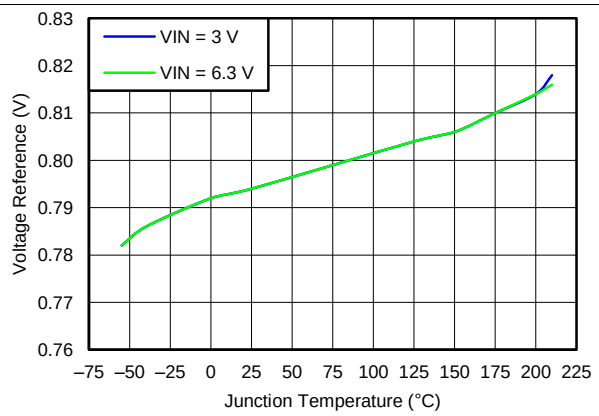

Figure 3. Voltage Reference vs Temperature

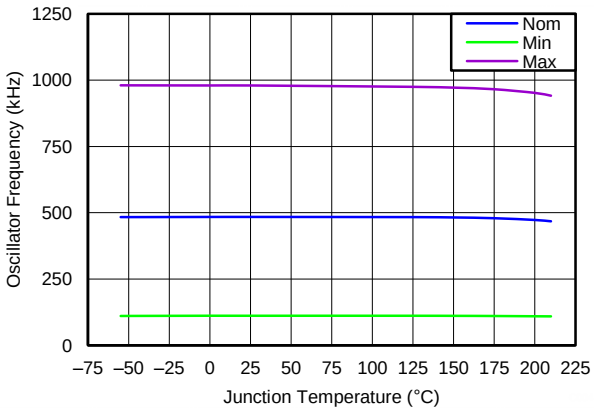

Figure 4. Oscillator Frequency vs Temperature

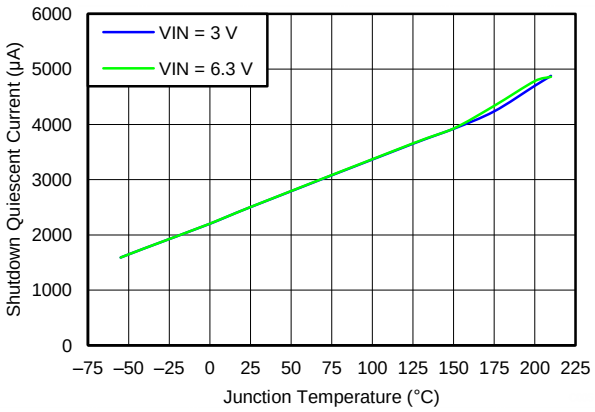

Figure 5. Shutdown Quiescent Current vs Temperature

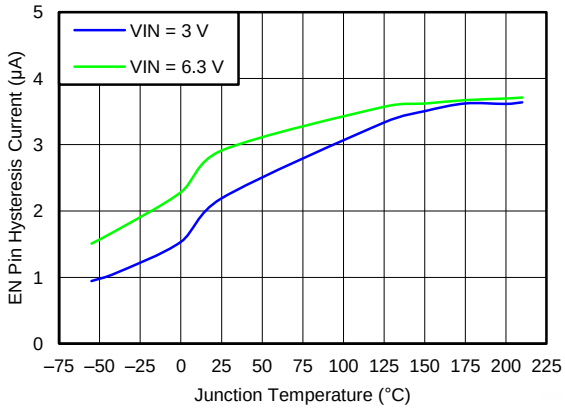

Figure 6. EN Pin Hysteresis Current vs Temperature

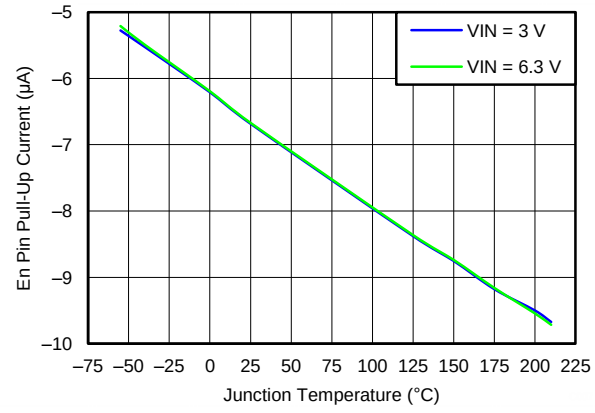

Figure 7. EN Pin Pullup Current vs Temperature

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Typical Characteristics (continued)

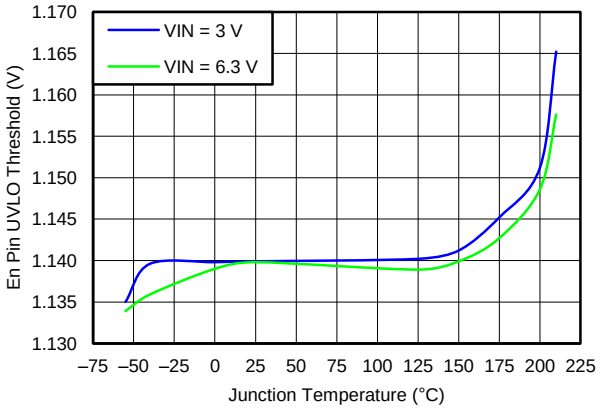

Figure 8. EN Pin UVLO Threshold vs Temperature

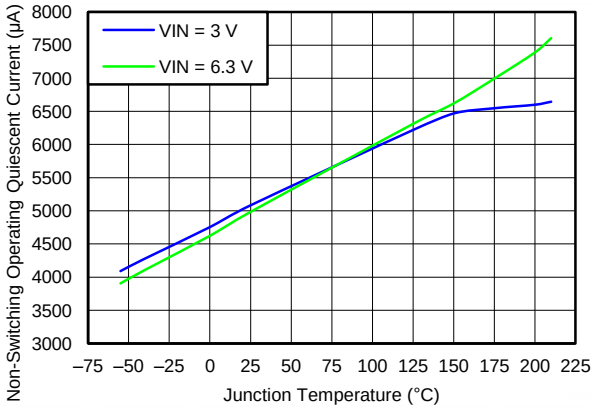

Figure 9. Non-Switching Operating Quiescent Current (VIN) vs Temperature

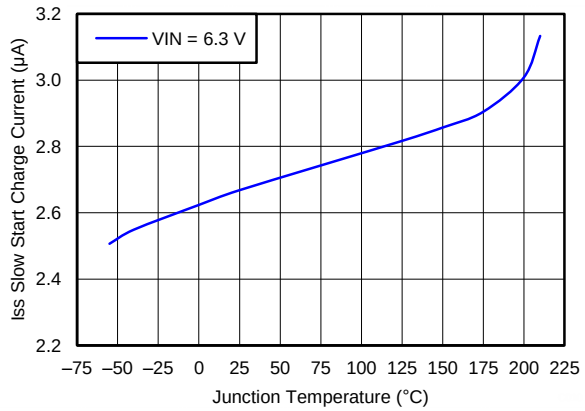

Figure 10. Slow Start Charge Current vs Temperature

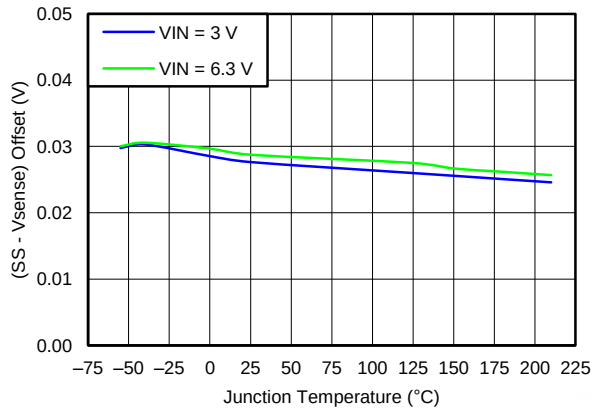

Figure 11. (SS-V_{SENSE}) Offset vs Temperature

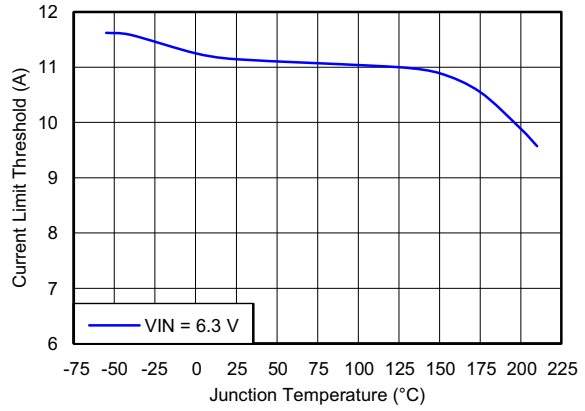

Figure 12. High-Side Current Limit Threshold vs Temperature

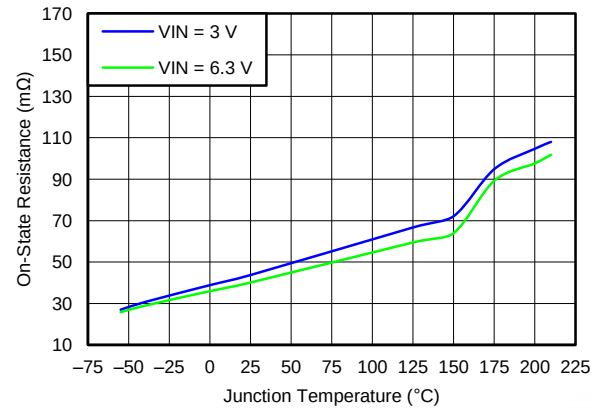

Figure 13. Low-Side $R_{DS(On)}$ vs Temperature

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Typical Characteristics (continued)

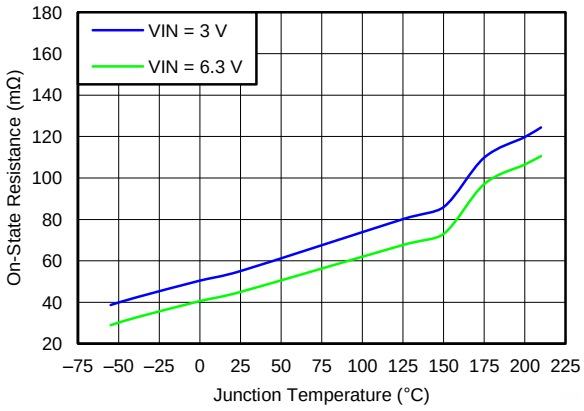

Figure 14. High-Side $R_{DS(On)}$ vs Temperature

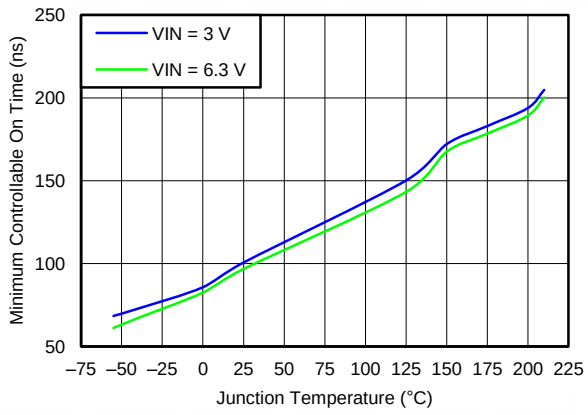

Figure 15. Minimum Controllable On-Time vs Temperature

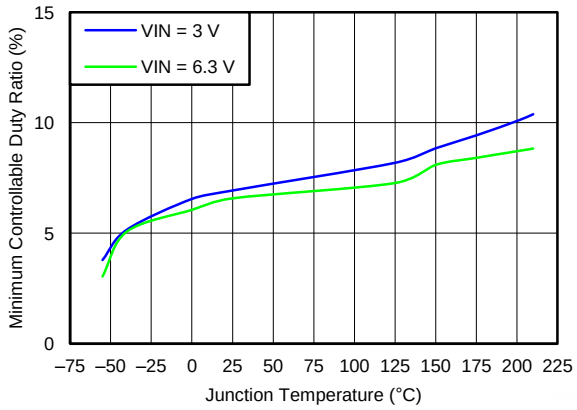

Figure 16. Minimum Controllable Duty Ratio vs Temperature

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8 Detailed Description

8.1 Overview

The device is a 6.3-V, 3-A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control, which also simplifies external frequency compensation. The wide switching frequency, 100 kHz to 1 MHz, allows for efficiency and size optimization when selecting the output filter components.

The device is designed for safe monotonic startup into prebiased loads. The default start up is when VIN is typically 3 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. The total operating current for the device is approximately 5 mA when not switching and under no load. When the device is disabled, the supply current is typically less than 2.5 mA.

The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 3 A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing the PH pin to be pulled low to recharge the boot capacitor. The device can operate over duty cycle range per Equation 2 and Equation 3 as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold, which is typically 2.2 V. The output voltage can be stepped down to as low as the 0.795-V voltage reference (Vref).

The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open-drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage Vref and asserts high when the VSENSE pin voltage is 94% to 106% of the Vref.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power-up. A small-value capacitor or resistor divider should be coupled to the pin for slow start or critical power-supply sequencing requirements.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections, which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C typical below the thermal shutdown trip point.

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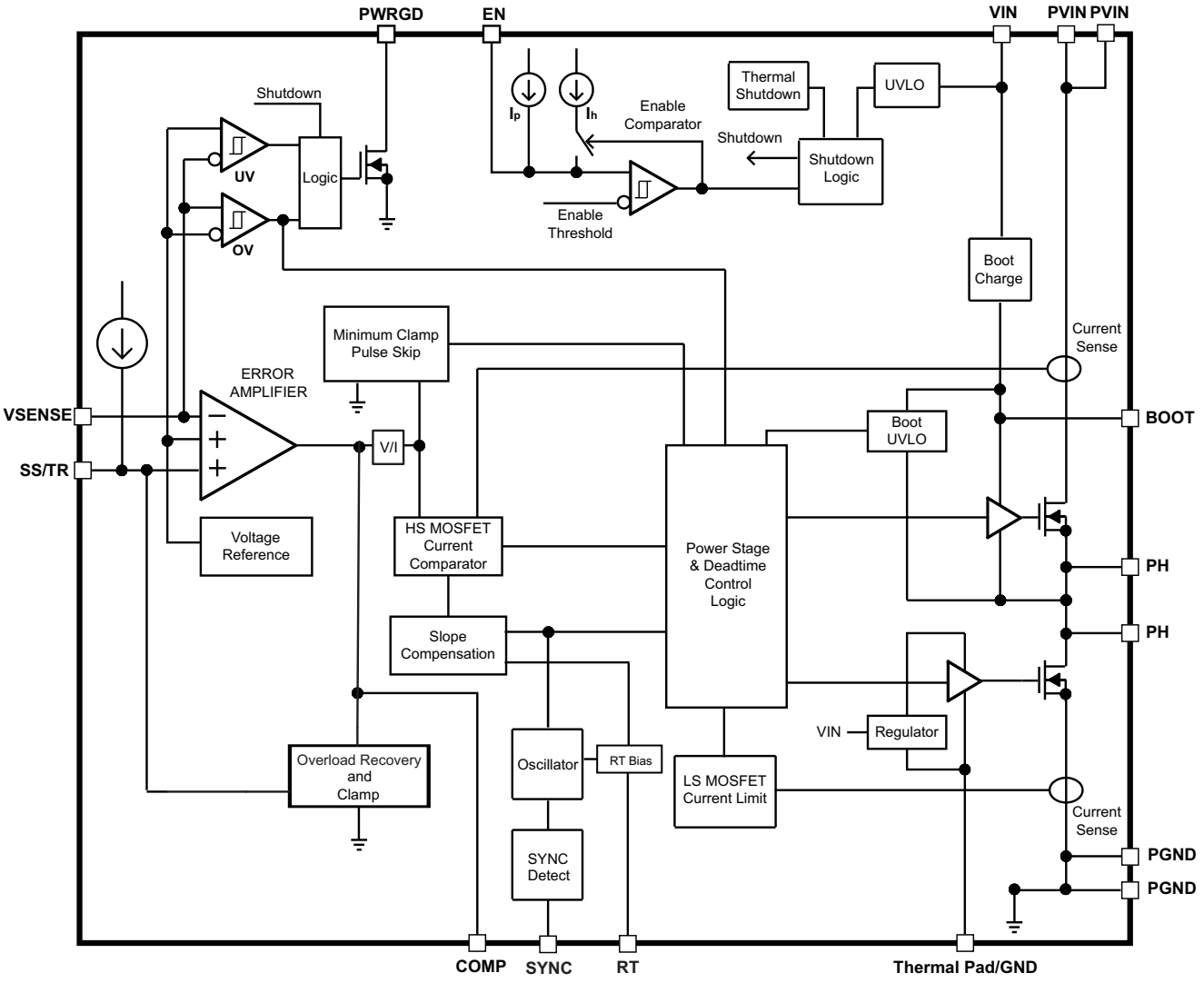
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.

If tied together, the input voltage for VIN and PVIN can range from 3 to 6.3 V. If using the VIN separately from PVIN, the VIN pin must be between 3 and 6.3 V, and the PVIN pin can range from as low as 1.6 to 6.3 V. A voltage divider connected to the EN pin can adjust the input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power-up behavior.

8.3.2 PVIN vs Frequency

With VIN tied to PVIN, minimum off-time determines what output voltage is achievable over frequency range.

8.3.3 Voltage Reference

The voltage reference system produces a precise voltage reference as indicated in *Electrical Characteristics*.

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Feature Description (continued)

8.3.4 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output to the VSENSE pin. TI recommends to use 1% tolerance or better divider resistors. Start with a 10 kΩ for R15 (top resistor) and use Equation 1 to calculate R38 (bottom resistor divider). To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R38 = \frac{Vref}{Vo - Vref} R15 \quad (1)$$

where

- Vref = 0.795 V

The minimum output voltage and maximum output voltage can be limited by the minimum on-time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. For more information, see *Bootstrap Voltage (BOOT) and Low Dropout Operation*.

8.3.5 Maximum Duty Cycle Limit

The TPS50301-HT can operate at duty cycle per Equation 2 and Equation 3 as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold, which is typically 2.2 V.

Duty cycle can be calculated based on Equation 2.

$$D(V_{IN}) = \frac{V_{OUT} + I_{OUT_max} \bullet R_{Tesr} + I_{OUT_max} \bullet R_{ds_low}}{V_{IN} - I_{OUT_max} \bullet R_{ds_high} + I_{OUT_max} \bullet R_{ds_low}} \quad (2)$$

where

- $R_{Tesr} = R_{dcr} + R_{trace}$
- R_{dcr} is the dc resistance of the inductor.
- R_{trace} is the dc trace resistance (miscellaneous drop).
- R_{ds_high} is the maximum R_{DS} of the high-side MOSFET.
- R_{ds_low} is the maximum R_{DS} of the low-side MOSFET.

8.3.6 PVIN vs Frequency

With VIN tied to PVIN, minimum off-time determines the output voltage that is achievable over frequency range. For V_{IN} = PV_{IN} must be ≥ 3 V. For V_{IN} = 3 V, PV_{IN} can vary from 1.6 to 6.3 V as highlighted in *Electrical Characteristics*.

This is given by Equation 3.

$$PV_{in_min}(f_{SW}) = \frac{V_O + I_O(R_{ds_onLS} + R_{misc})}{1 - T_{off_min} \bullet f_{SW}} \quad (3)$$

where

- R_{ds_onLS} = Low-side $R_{ds\text{-}on}$
- R_{misc} = Miscellaneous trace drops
- T_{off_min} = Minimum off time

Using this approach, the designer can calculate minimum PV_{IN} required for specific V_{OUT} as indicated in the example in Figure 17.

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Feature Description (continued)

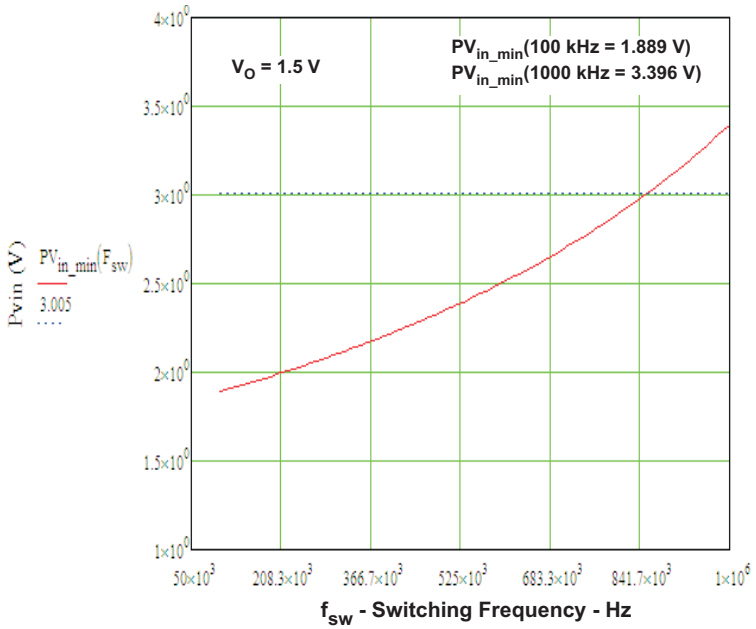

Figure 17. PV_{IN} vs Frequency

8.3.7 Safe Start-Up into Prebiased Outputs

The device is designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased startup, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.4 V.

8.3.8 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.795-V voltage reference. The transconductance of the error amplifier is 1300 μA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground. Error amplifier dc gain is typically 39000 V/V with minimum value of 22000 V/V per design.

8.3.9 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

8.3.10 Enable and Adjust UVLO

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state. If an external Schottky diode is used from V_{IN} to boot, then a bleeder may be required < 1 mA to ensure output is low when the unit is disabled by EN pin.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 50-mV typical.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN in split-rail applications, then the EN pin can be configured as shown in Figure 18, Figure 19, and Figure 20.

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Feature Description (continued)

The EN pin has a small pullup current, Ip, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by Ih after the EN pin crosses the enable threshold. Calculate the UVLO thresholds with Equation 4 and Equation 5.

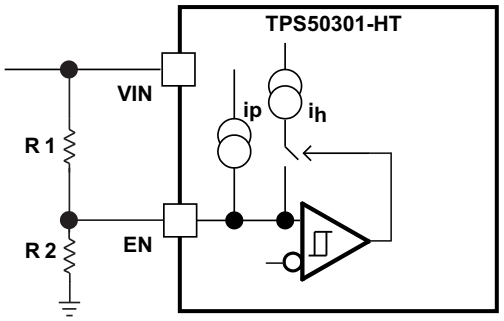

Figure 18. Adjustable VIN UVLO

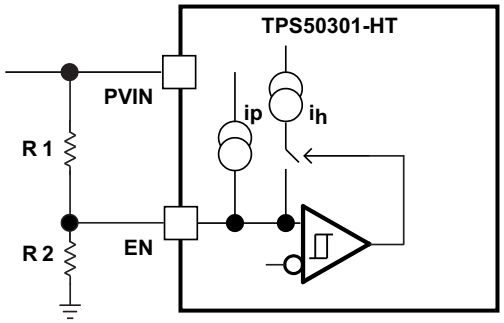

Figure 19. Adjustable PVIN UVLO, VIN ≥ 3 V

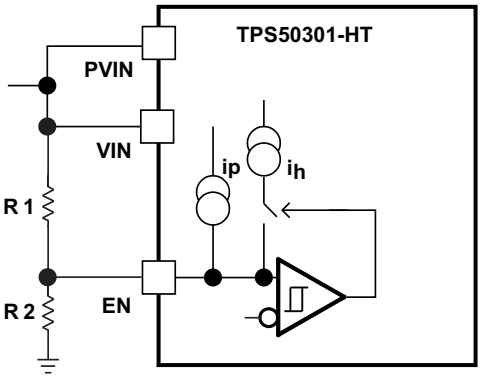

Figure 20. Adjustable VIN and PVIN UVLO

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \qquad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \qquad (5)$$

where

- I_h = 3 µA
- I_p = 3.2 µA
- $V_{ENRISING}$ = 1.131 V
- $V_{ENFALLING}$ = 1.09 V

8.3.11 Adjustable Switching Frequency and Synchronization (SYNC)

The switching frequency of the device supports three modes of operations. The modes of operation are set by the conditions on the RT and SYNC pins. At a high level, these modes can be described as master, internal oscillator, and external synchronization modes.

In master mode, the RT pin should be left floating; the internal oscillator is set to 500 kHz, and the SYNC pin is set as an output clock. The SYNC output is in phase with respect to the internal oscillator. SYNC out signal level is the same as V_{IN} level with 50% duty cycle. SYNC signal feeding the slave module—which is in phase with the master clock—gets internally inverted (180° out of phase with the master clock) internally in the slave module.

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Feature Description (continued)

In internal oscillator mode, a resistor is connected between the RT pin and GND. The SYNC pin requires a 10-kΩ resistor to GND for this mode to be effective. The switching frequency of the device is adjustable from 100 kHz to 1 MHz by placing a maximum of 510 kΩ and a minimum of 47 kΩ respectively. To determine the RT resistance for a given switching frequency, use Equation 6 or the curve in Figure 21. To reduce the solution size, the designer should set switching frequency as high as possible, but consider the tradeoffs of supply efficiency and minimum controllable on-time.

$$RT(F_{SW}) = 67009 \times F_{SW}^{-1.0549} \quad (6)$$

where

- RT in kΩ
- F_{SW} in kHz

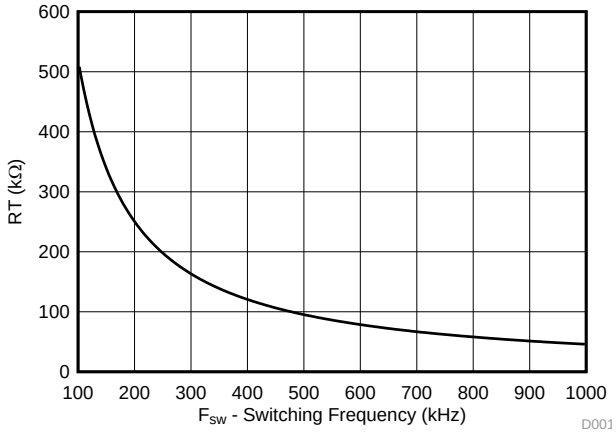

Figure 21. RT vs Switching Frequency

When operating the converter in internal oscillator mode (internal oscillator determines the switching frequency; 500 kHz default), the synchronous pin becomes the output and there is a phase inversion. When trying to parallel with another converter, the RT pin of the second (slave) converter must have its RT pin populated such that the converter frequency of the slave converter must be within ±5% of the master converter. This is required because the RT pin also sets the proper operation of slope compensation.

In external synchronization mode, a resistor is connected between the RT pin and GND. The SYNC pin requires a toggling signal for this mode to be effective. The switching frequency of the device goes 1:1 with that of SYNC pin. External system clock-user supplied sync clock signal determines the switching frequency. If no external clock signal is detected for 20 µs, then TPS50301-HT transitions to its internal clock, which is typically 500 kHz. An external synchronization using an inverter to obtain phase inversion is necessary. RT values of the master and slave converter must be within ±5% of the external synchronization frequency. This is necessary for proper slope compensation. A resistance in the RT pin is required for proper operation of the slope compensation circuit. To determine the RT resistance for a given switching frequency, use Equation 6 or the curve in Figure 21. To reduce the solution size, the designer should set switching frequency as high as possible, but consider the tradeoffs of supply efficiency and minimum controllable on-time.

These modes are described in Table 3.

Table 3. Switching Frequency, SYNC and RT Pin Usage Table

RT PIN	SYNC PIN	SWITCHING FREQUENCY	DESCRIPTION AND NOTES
Float	Generates an output signal	500 kHz	SYNC pin behaves as an output. SYNC output signal is 180° out of phase to the internal 500-kHz switching frequency.

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Feature Description (continued)

Table 3. Switching Frequency, SYNC and RT Pin Usage Table (continued)

RT PIN	SYNC PIN	SWITCHING FREQUENCY	DESCRIPTION AND NOTES
47- to 485-kΩ resistor to AGND	10-kΩ resistor to AGND	100 kHz to 1 MHz	Internally generated switching frequency is based upon the resistor value present at the RT pin.
	User-supplied sync clock	Internally synchronized to external clock	Set value of RT that corresponds to the externally supplied sync frequency.

8.3.12 Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The device has an internal pullup current source of 5 mA that charges the external slow-start capacitor. Equation 7 shows the calculations for the slow-start time (Tss, 10% to 90%) and slow-start capacitor (Css). The voltage reference (Vref) is 0.795 V and the slow-start charge current (Iss) is 2.5 μA.

$$t_{SS}\ (ms) = \frac{Css\ (nF) \times Vref\ (V)}{Iss\ (\mu A)} \tag{7}$$

When the input UVLO is triggered, the EN pin is pulled below 1.032 V, or a thermal shutdown event occurs the device stops switching and enters low current operation. At the subsequent power-up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

8.3.13 Power Good (PWRGD)

The PWRGD pin is an open-drain output. When the VSENSE pin is between 94% and 106% of the internal voltage reference, the PWRGD pin pull-down is deasserted and the pin floats. TI recommends to use a pullup resistor between 10 to 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state when the VIN input voltage is greater than 1 V but has reduced current sinking capability. The PWRGD achieves full current sinking capability when the VIN input voltage is above 3 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is below 1.4 V.

8.3.14 Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 μF. TI recommends a ceramic capacitor with an X7R- or X5R-grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the device is designed to operate at a high duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold, which is typically 2.1 V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split-input voltage rails, high duty cycle operation can be achieved as long as (V_{IN} – PV_{IN}) > 4 V.

Maximum switching frequency is also limited by minimum on-time (specified in *Electrical Characteristics*) as indicated by Equation 8. Switching frequency will be worst case at no load conditions.

$$F_{SW} = \frac{1}{T} = \frac{V_O + R_{ds_on} \bullet (I_O)}{V_{IN} \bullet (T_{on_max})} \tag{8}$$

8.3.15 Sequencing (SS/TR)

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins.

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The sequential method is shown in Figure 22 using two TPS50301-HT devices. The power good of the first device is coupled to the EN pin of the second device, which enables the second power supply after the primary supply reaches regulation.

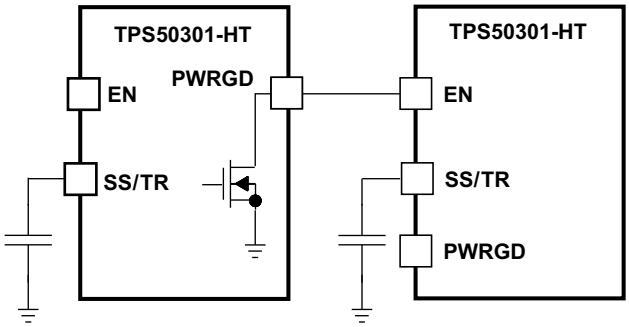

Figure 22. Sequential Start-Up Sequence

Figure 23 shows the method implementing ratiometric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in Equation 7.

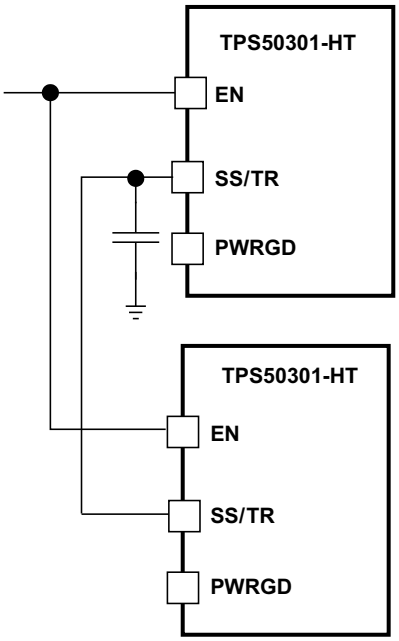

Figure 23. Ratiometric Start-Up Sequence

Ratiometric and simultaneous power-supply sequencing can be implemented by connecting the resistor network of R1 and R2 (shown in Figure 24) to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 9 and Equation 10, the tracking resistors can be calculated to initiate the Vout2 slightly before, after, or at the same time as Vout1. Equation 11 is the voltage difference between Vout1 and Vout2.

To design a ratiometric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 9 and Equation 10 for ΔV. Equation 11 results in a positive number for applications where the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved.

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The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset, 29 mV) in the slow-start circuit and the offset created by the pullup current source (Iss, 2 μA) and tracking resistors, the Vssoffset and Iss are included as variables in the equations.

To ensure proper operation of the device, the calculated R1 value from Equation 9 must be greater than the value calculated in Equation 12.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \quad (9)$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \quad (10)$$

$$\Delta V = Vout1 - Vout2 \quad (11)$$

$$R1 > 2800 \times Vout1 - 180 \times \Delta V \quad (12)$$

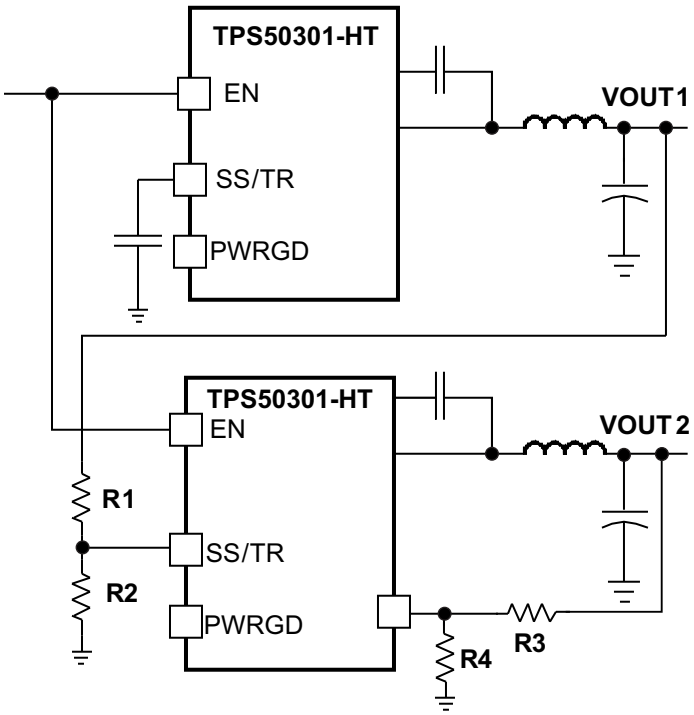

Figure 24. Ratiometric and Simultaneous Start-Up Sequence

8.3.16 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.17 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and low-side MOSFET.

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8.3.17.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

8.3.17.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

When the low-side MOSFET turns off, the switch node increases and forward biases the high-side MOSFET parallel diode (the high-side MOSFET is still off at this stage).

8.3.18 TPS50301-HT Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 165°C typically.

8.3.19 Turn-On Behavior

Minimum on-time specification determines the maximum operating frequency of the design. As the unit starts up and goes through its soft-start process, the required duty-cycle is less than the minimum controllable on-time. This can cause the converter to skip pulses. Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is only evident when operating at high frequency with high bandwidth. When the minimum on-pulse is greater than the minimum controllable on-time, the turn-on behavior is normal. When operating at low frequencies (100 kHz or less), the turn-on behavior does not exhibit any ringing at initial startup.

8.3.20 Small Signal Model for Loop Response

Figure 25 shows an equivalent model for the device control loop, which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 μA/V. The error amplifier can be modeled using an ideal voltage-controlled current source. The resistor, Roea (30 MΩ), and capacitor, Coea (20.7 pF), model the open-loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load-step amplitude and step rate in a time domain analysis.

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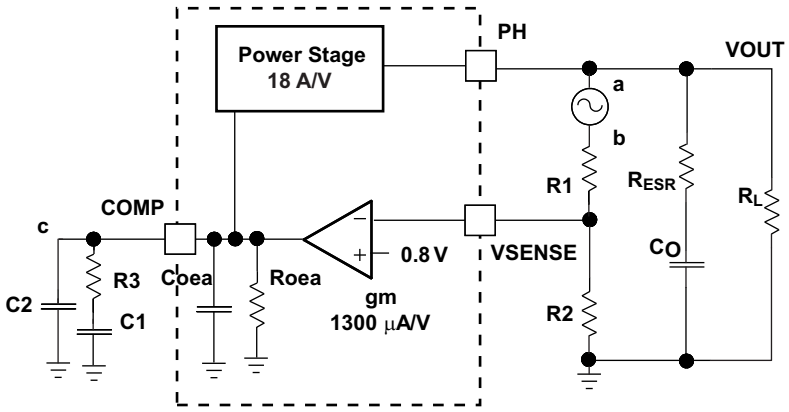

Figure 25. Small Signal Model For Loop Response

8.3.21 Simple Small Signal Model for Peak Current Mode Control

Figure 26 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. Equation 13 shows the control to output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 25) is the power stage transconductance (gm_{ps}), which is 18 A/V for the device. The dc gain of the power stage is the product of gm_{ps} and the load resistance (R_L) as shown in Equation 14 with resistive loads. As the load current increases, the dc gain decreases. This variation with load may seem problematic at first glance, but fortunately, the dominant pole moves with load current (see Equation 15). The combined effect is highlighted by the dashed line in Figure 27. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation.

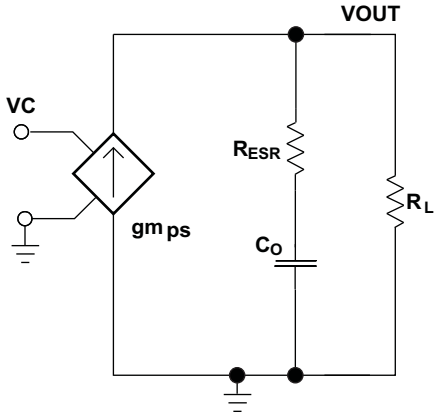

Figure 26. Simplified Small Signal Model for Peak Current Mode Control

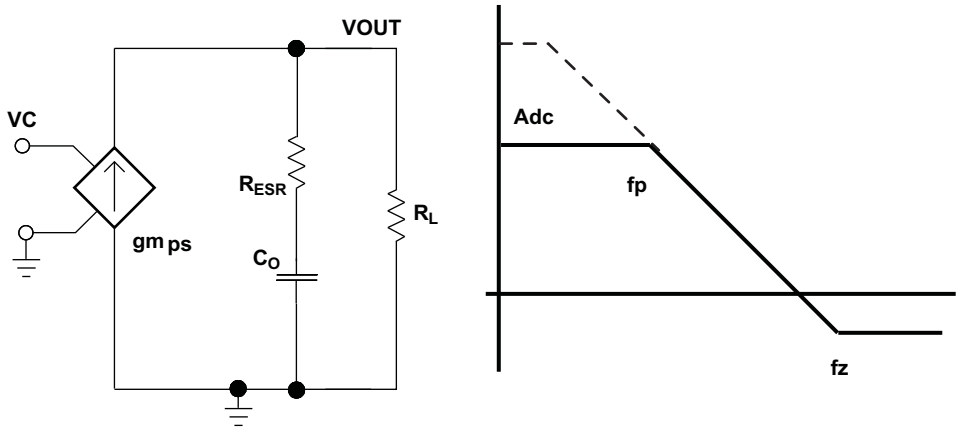

Figure 27. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times fz}\right)}{\left(1 + \frac{s}{2\pi \times fp}\right)} \quad (13)$$

$$Adc = gm_{ps} \times R_L \quad (14)$$

$$fp = \frac{1}{C_O \times R_L \times 2\pi} \quad (15)$$

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$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi}$$

where

- gm_{ea} is the GM amplifier gain (1300 μA/V).
- gm_{ps} is the power stage gain (18 A/V).
- R_L is the load resistance.
- C_O is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor. (16)

8.3.22 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits shown in Figure 28. In Type 2A, one additional high-frequency pole is added to attenuate high-frequency noise.

The following design guidelines are provided for advanced users who prefer to compensate using the general method. The step-by-step design procedure described in *Detailed Design Procedure* may also be used.

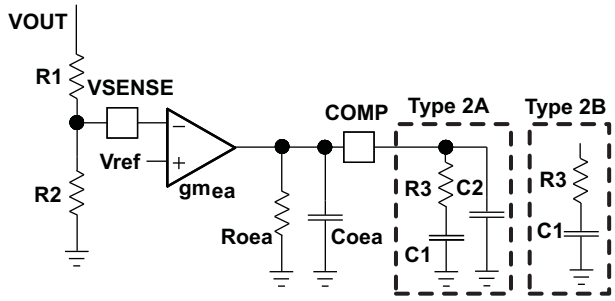

Figure 28. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency fc. A good starting point is one-tenth of the switching frequency, f_{SW}.
2. R3 can be determined by:

$$R3 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}}$$

where

- gm_{ea} is the GM amplifier gain (1300 μA/V).
- gm_{ps} is the power stage gain (18 A/V).
- Vref is the reference voltage (0.795 V) (17)

3. Place a compensation zero at the dominant pole $\left(fp = \frac{1}{C_O \times R_L \times 2\pi} \right)$.
   C1 can be determined by

$$C1 = \frac{R_L \times Co}{R3}$$ (18)

4. C2 is optional. It can be used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor Co.

$$C2 = \frac{R_{ESR} \times Co}{R3}$$ (19)

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NOTE

For PSpice models and WEBENCH design tool, see the *Tools & Software* tab.

1. PSpice average model (stability – bode plot)
2. PSpice transient model (switching waveforms)
3. WEBENCH design tool www.ti.com/product/TPS50301-HT/toolssoftware

8.4 Device Functional Modes

8.4.1 Fixed-Frequency PWM Control

The device uses fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

8.4.2 Continuous Current Mode (CCM) Operation

As a synchronous buck converter, the device normally works in CCM under all load conditions.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS50301-HT device is a highly-integrated synchronous step-down DC-DC converter. The device is used to convert a higher DC-DC input voltage to a lower DC output voltage with a maximum output current of 3 A.

9.2 Typical Application

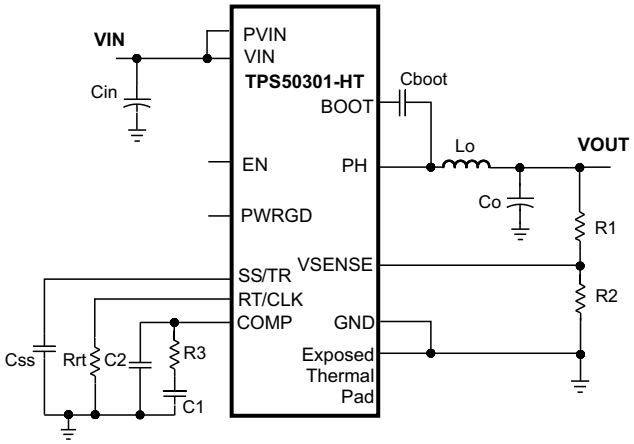

Figure 29. Typical Application Schematic

9.2.1 Design Requirements

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	3.3 V
Output current	3 A
Transient response 1-A load step	ΔVout = 5%
Input voltage	5-V nominal, 4.5 V to 6.3 V
Output voltage ripple	33 mV p-p
Start input voltage (rising Vin)	4.425 V
Stop input voltage (falling Vin)	4.234 V
Switching frequency	480 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS50301-HT device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

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3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance. In this design, a moderate switching frequency of 480 kHz is selected to achieve both a small solution size and a high efficiency operation.

9.2.2.3 Output Inductor Selection

To calculate the value of the output inductor, use Equation 20. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value (Iout x Kind) is at the discretion of the designer.

$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw} \tag{20}$$

For this design example, use KIND = 0.3 and the inductor value is calculated to be 2.7 µH. For this design, a nearest standard value was chosen: 3.3 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 22 and Equation 23.

$$Iripple = \frac{Vinmax - Vout}{L1} \cdot \frac{Vout}{Vinmax \cdot fsw} \tag{21}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \cdot \left(\frac{V_o \cdot (Vinmax - Vo)}{Vinmax \cdot L1 \cdot fsw} \right)^2} \tag{22}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{23}$$

For this design, the RMS inductor current is 3.01 A and the peak inductor current is 3.49 A. The chosen inductor is a Coilcraft MSS1048 series 3.3 µH. It has a saturation current rating of 7.38 A and a RMS current rating of 7.22 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.4 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria

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The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 24 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout} \tag{24}$$

Where ΔIout is the change in output current, Fsw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in Vout for a load step of 1 A. For this example, ΔIout = 1 A and ΔVout = 0.05 × 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 25 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 25 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 33 mV. Under this requirement, Equation 25 yields 8.2 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{Voripple}{Iripple}} \tag{25}$$

Equation 26 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 26 indicates the ESR should be less than 33 mΩ. In this case, the ceramic caps' ESR is much smaller than 33 mΩ.

$$Resr < \frac{Voripple}{Iripple} \tag{26}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, a 47-µF 6.3-V X5R ceramic capacitor with 3 mΩ of ESR is be used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 27 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 27 yields 286mA.

$$Icorms = \frac{Vout \cdot (Vinmax - Vout)}{\sqrt{12} \cdot Vinmax \cdot L1 \cdot fsw} \tag{27}$$

9.2.2.5 Input Capacitor Selection

The TPS50301-HT requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins and 4.7 µF on the Vin input voltage pin. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS50301-HT. The input ripple current can be calculated using Equation 28.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vinmin} \cdot \frac{(Vinmin - Vout)}{Vinmin}} \tag{28}$$

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The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this example, one 10 µF and one 4.7-µF 25-V capacitors in parallel have been selected as the VIN and PVIN inputs are tied together so the TPS50301-HT may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 29. Using the design example values, Ioutmax = 3 A, Cin = 14.7 µF, F_{SW} = 480 kHz, yields an input voltage ripple of 106 mV and a RMS input ripple current of 1.33 A.

$$\Delta Vin = \frac{Ioutmax \cdot 0.25}{Cin \cdot fsw} \tag{29}$$

9.2.2.6 Slow Start Capacitor Selection

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS50301-HT reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using Equation 30. For the example circuit, the soft start time is not too critical since the output capacitor value is 47 µF which does not require much current to charge to 3.3 V. The example circuit has the soft start time set to an arbitrary value of 3.5 ms which requires a 10-nF capacitor. In TPS50301-HT, Iss is 2.5 µA typical, and Vref is 0.795 V.

$$C5(nF) = \frac{Tss(ms) \text{ x } Iss(\mu A)}{Vref(V)} \tag{30}$$

9.2.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a voltage rating of 10 V or higher.

9.2.2.8 Undervoltage Lockout (UVLO) Set Point

The UVLO can be adjusted using the external voltage divider network of R6a and R7a. R6a is connected between VIN and the EN pin of the TPS50301-HT and R7a is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above selected voltage (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below (UVLO stop or disable) voltage. Equation 4 and Equation 5 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified the nearest standard resistor value for R6a is 10.0 kΩ and for R7a is 3.4 kΩ.

9.2.2.9 Output Voltage Feedback Resistor Selection

The resistor divider network R5 and R6 is used to set the output voltage. For the example design, 10 kΩ was selected for R6. Using Equation 31, R5 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ.

$$R5 = \frac{Vref}{Vo - Vref} \times R6 \tag{31}$$

9.2.2.9.1 Minimum Output Voltage

Due to the internal design of the TPS50301-HT, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 32.

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$V_{OUT}min = Ontimemin \times fsmax (V_{IN}max + I_{OUT}min (R_{DS2}min - R_{DS1}min)) – I_{OUT}min (R_L + R_{DS2}min)$

where

- $V_{OUT}min$ = Minimum achievable output voltage
- Ontimemin = Minimum controllable on-time (175 ns maximum)
- $fsmax$ = Maximum switching frequency including tolerance
- $V_{IN}max$ = Maximum input voltage
- $I_{OUT}min$ = Minimum load current
- $R_{DS1}min$ = Minimum high-side MOSFET on-resistance (36-32 mΩ typical)
- $R_{DS2}min$ = Minimum low-side MOSFET on-resistance (19 mΩ typical)
- R_L = Series resistance of output inductor (32)

9.2.2.10 Compensation Component Selection

There are several industry techniques used to compensate DC-DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. The method presented here ignores the effects of the slope compensation that is internal to the TPS50301-HT. Since the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations. Use WEBENCH, Pspice model for simulation.

First, the modulator pole, fpmod, and the esr zero, fzmod must be calculated using Equation 33 and Equation 34. For Cout, use a derated value of 22.4 µF. use Equation 35 and Equation 36 to estimate a starting point for the closed loop crossover frequency fco. Then the required compensation components may be derived. For this design example, fpmod is 12.9 kHz and fzmod is 2730 kHz. Equation 35 is the geometric mean of the modulator pole and the esr zero and Equation 36 is the geometric mean of the modulator pole and one half the switching frequency. Use a frequency near the lower of these two values as the intended crossover frequency fco. In this case Equation 35 yields 175 kHz and Equation 36 yields 55.7 kHz. The lower value is 55.7 kHz. A slightly higher frequency of 60.5 kHz is chosen as the intended crossover frequency.

$$fpmod = \frac{Iout}{2 \cdot \pi \cdot Vout \cdot Cout} \quad (33)$$

$$fzmod = \frac{1}{2 \cdot \pi \cdot RESR \cdot Cout} \quad (34)$$

$$fco = \sqrt{fpmod \cdot fzmod} \quad (35)$$

$$fco = \sqrt{fpmod \cdot \frac{fsw}{2}} \quad (36)$$

Now the compensation components can be calculated. First calculate the value for R2 which sets the gain of the compensated network at the crossover frequency. Use Equation 37 to determine the value of R2.

$$R2 = \frac{2\pi \cdot fc \cdot Vout \cdot Cout}{gm_{ea} \cdot Vref \cdot gm_{ps}} \quad (37)$$

Next calculate the value of C3. Together with R2, C3 places a compensation zero at the modulator pole frequency. Equation 38 to determine the value of C3.

$$C3 = \frac{Vout \cdot Cout}{Iout \cdot R2} \quad (38)$$

Using Equation 37 and Equation 38 the standard values for R2 and C3 are 1.69 kΩ and 8200 pF.

An additional high frequency pole can be used if necessary by adding a capacitor in parallel with the series combination of R2 and C3. The pole frequency is given by Equation 39. This pole is not used in this design.

$$fp = \frac{1}{2 \cdot \pi \cdot R2 \cdot Cp} \quad (39)$$

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9.2.3 Parallel Operation

Configuring two TPS50601-SP in order to provide 12-A output current.

Design procedure is as follows - An example, Figure 30, shows parallel configuration using two TPS50601-SP in Master/Slave.

Important design steps are detailed as follows:

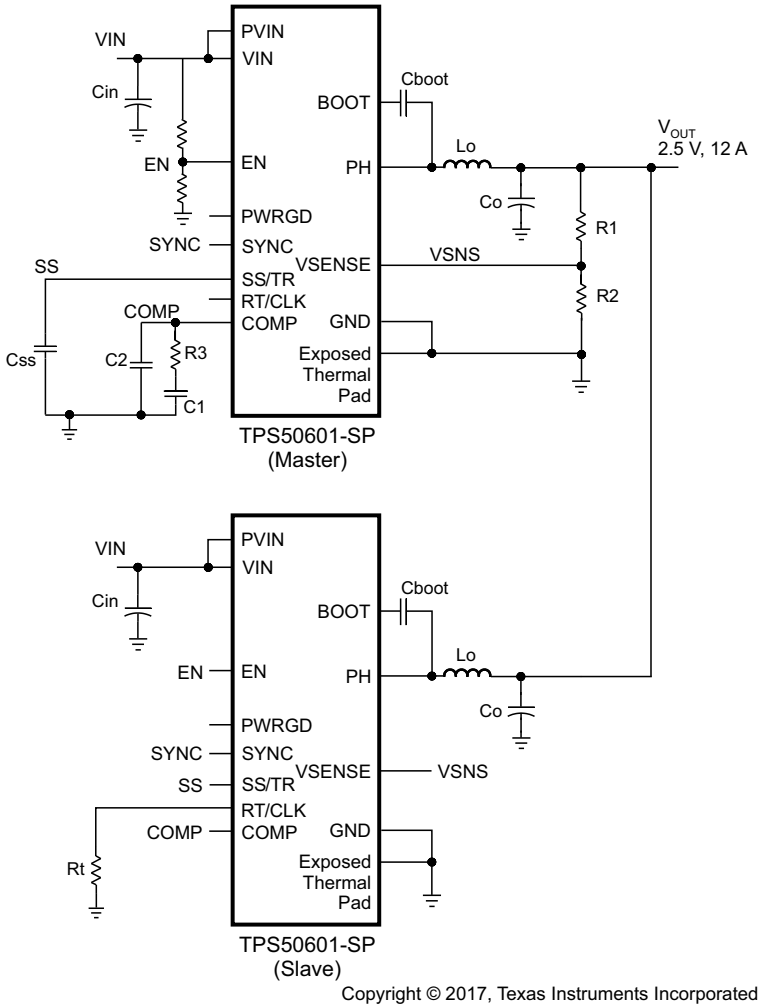

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Figure 30. Parallel Configuration Showing Master and Slave

For the master - RT pin must be left floating and this will set the frequency to 500 kHz.

In order to parallel two current mode control POLs (TPS50601-SP) one needs to do the following:

1. RT pin on master must be left open (switching frequency 500-kHz typical (395-kHz minimum to 585-kHz maximum)) as highlighted in the data sheet frequency internally generated. For more details, see *Adjustable Switching Frequency and Synchronization (SYNC)* section.
   a. When RT pin is left open then sync pin becomes output.
2. RT pin on slave should be selected within 5% of master ie RT = 96-kHz typical.
3. Have a single feedback loop.
4. Sync pins of master must be connected to sync pins of slave.
5. Connect comp pins of two POLs together.
6. Connect Vsense pins of two POLs together.
7. Connect SS pins together.

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8. Connect enable pins together thus there is one enable.

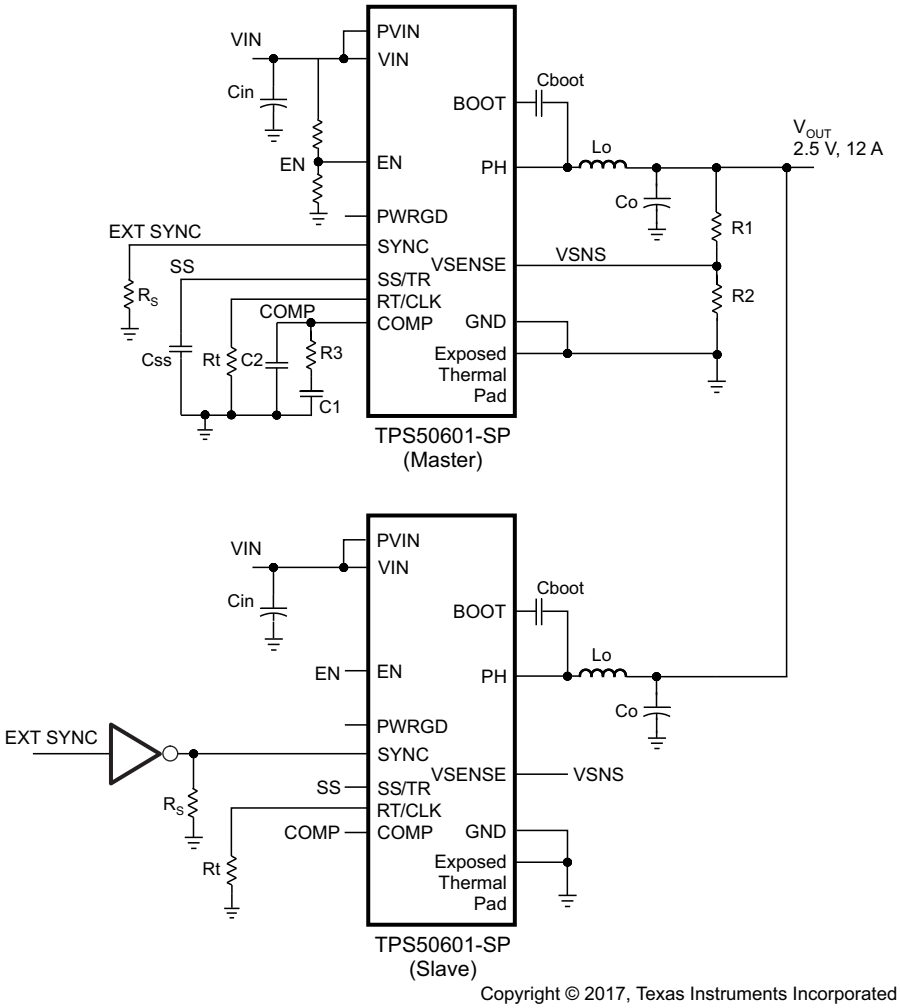
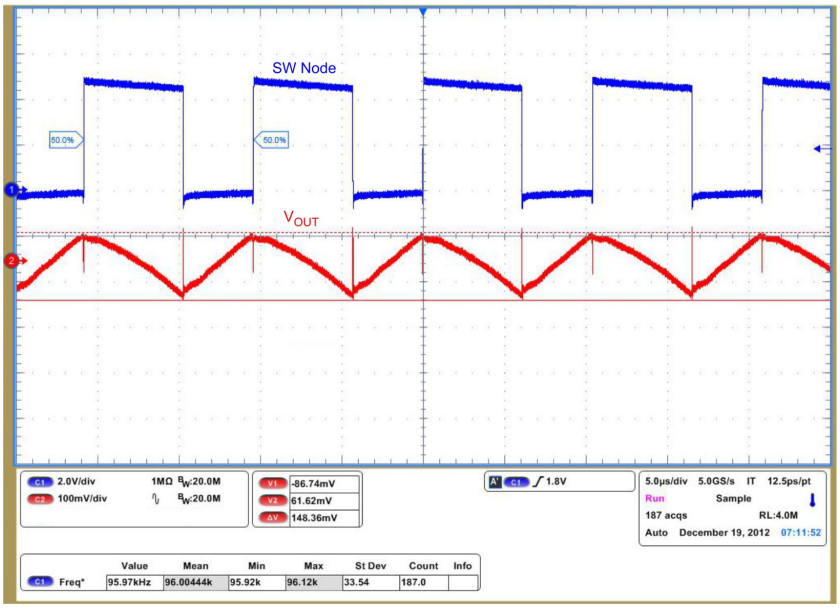


Figure 31. Parallel Configuration With External Sync

Configuration when using an external clock is as follows: Refer to Figure 31.

1. Master/slave configuration can also be achieved if desired using external clock ie if operating at 100 kHZ or any other customer selected frequency.
   a. External user supplied clock signal is required.
   b. RT pins of both master and slave must be populated with appropriate resistor value ie 475 kΩ (for 100 kHZ).
   c. Slave signal feeding the sync pin must be inverter.
2. RT pin on both master and slave must be populated for 100 kHz operation RT = 495 kΩ.
3. External user supplied clock signal is required.
4. Connect comp pins of two POLs together.
5. Connect Vsense pins of two POLs together.
6. Connect SS pins together.
7. Connect enable pins together thus there is one enable.

9.2.4 Application Curve



NOTE: Per EVM - for additional details see the User's Guide, SLVU499.

Figure 32. Typical Switching Waveform for 100-kHz Switching Operation

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10 Power Supply Recommendations

The TPS50301-HT is designed to operate from an input voltage supply range between 3 V and 6.3 V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7 µF (after de-rating) ceramic capacitor, type X5R or better from PVIN to GND, and from VIN to GND. Additional local ceramic bypass capacitance may be required in systems with small input ripple specifications, in addition to bulk capacitance if the TPS50301-HT device is located more than a few inches away from its input power supply. In systems with an auxiliary power rail available, the power stage input, PVIN, and the analog power input, VIN, may operate from separate input supplies. See *Layout Example* (layout recommendation) for recommended bypass capacitor placement.

11 Layout

11.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See *Layout Example* for a PCB layout example.
- The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS50301-HT and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS50301-HT device to provide a thermal path from the exposed thermal pad land to ground
- Thermal Pad can be electrically floating or connected externally. If electrically connected externally then it must be connected to GND. Customer should evaluate their system when themal pad is electrically isolated and thermally conductive.
- Preferred approach is that GND pin should be tied directly to the power pad under the IC and the PGND.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.
- To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
- The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.
- Make sure to connect this capacitor to the quite analog ground trace rather than the power ground trace of the PVIn bypass capacitor.
- Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor.
- Try to minimize this conductor length while maintaining adequate width.
- The small signal components should be grounded to the analog ground path as shown.
- The RT pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
- It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.
- Land pattern and stencil information is provided in the data sheet addendum.

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11.2 Layout Example

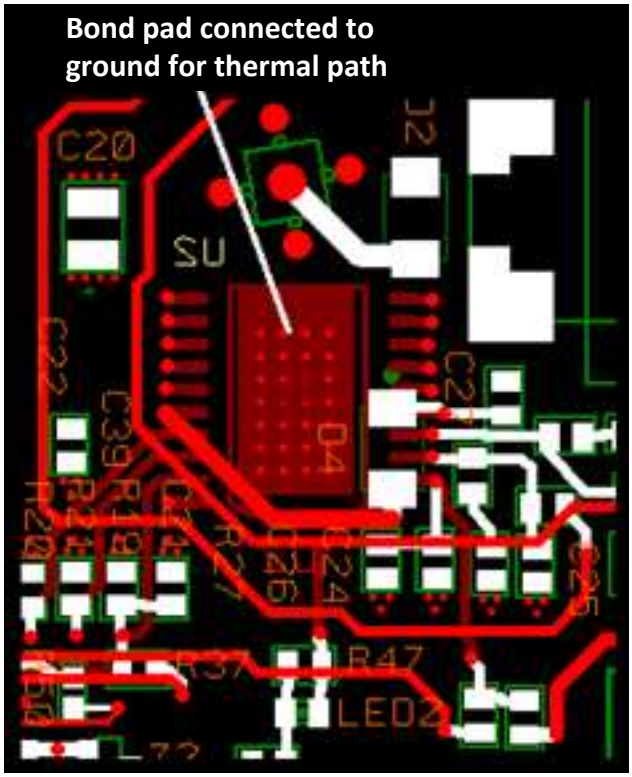

Figure 33. PCB Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designer により、TPS50301-HT デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

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12.3 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 メカニカル、パッケージ、および注文情報

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13.1 デバイスの項目表記

KGD 品質保証のベア・ダイ

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS50301SHKH	Active	Production	CFP (HKH) | 20	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 210	TPS50301SHKH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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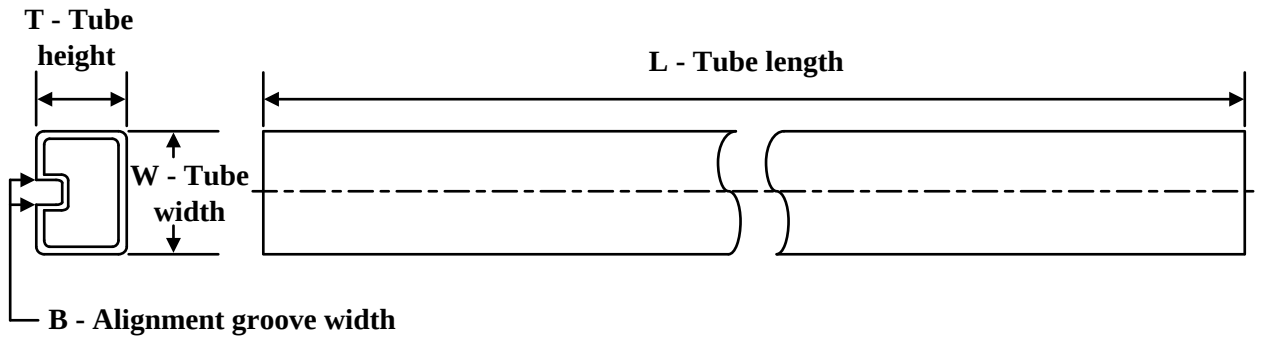
TUBE



*All dimensions are nominal

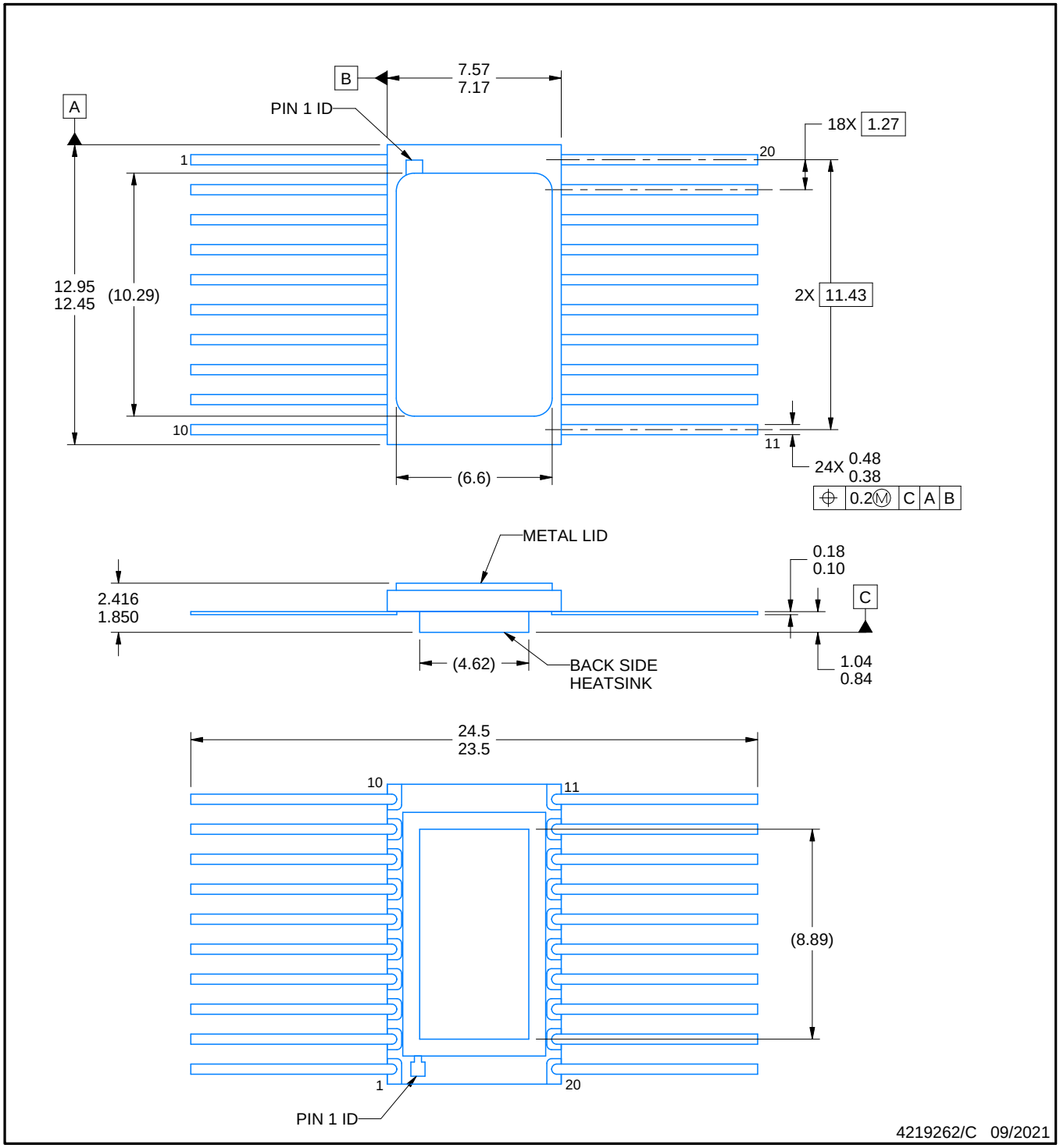
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS50301SHKH	HKH	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKH0020A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



NOTES:

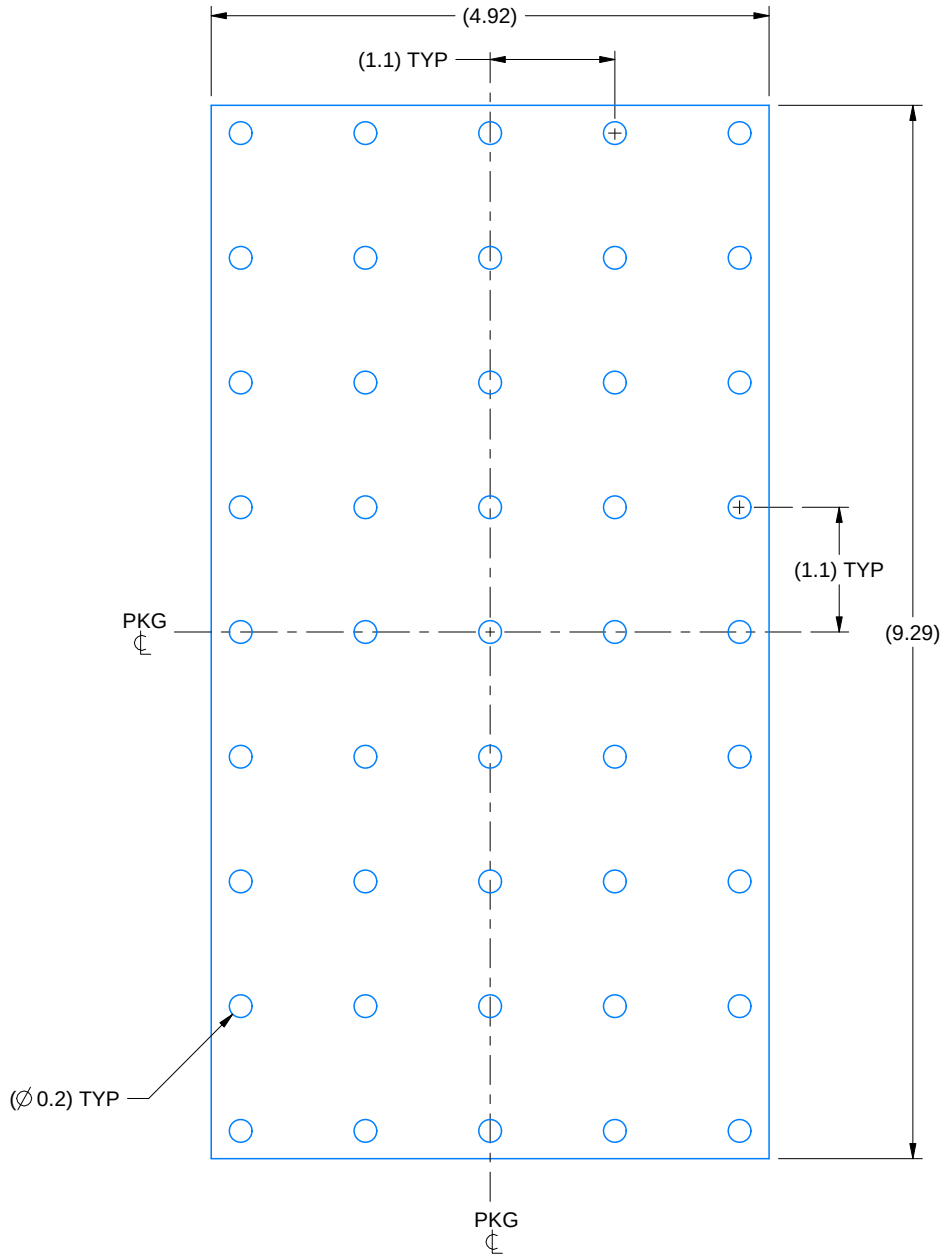
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.

EXAMPLE BOARD LAYOUT

HKH0020A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SCALE	SIZE		REV	PAGE
3X	A	4219262	C	3 OF 4

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