TEXAS INSTRUMENTS
TPS51397A
JAJSJP3A – SEPTEMBER 2020 – REVISED OCTOBER 2020

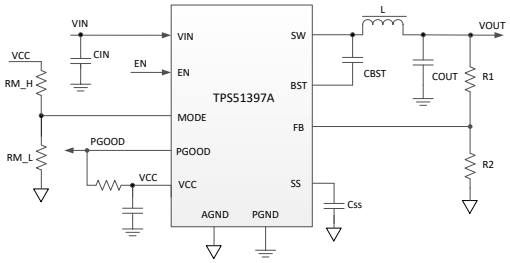
TPS51397A 4.5V～24V、10A 同期整流降圧コンバータ、ULQ™ 動作

1 特長

- 入力電圧範囲:4.5V～24V
- 出力電圧範囲:0.6V～5.5V
- 10A の連続出力電流をサポート
- D-CAP3™ アーキテクチャ制御による高速過渡応答
- 0.6V±1% の帰還電圧精度 (25°C)
- 17mΩ および 5.9mΩ の FET を内蔵
- ULQ™ 動作 (110 µA) により、システムのスタンバイ中のバッテリ動作時間を延長
- MODE ピンで選択可能な Eco-mode™ と Out-of-Audio™
- 500kHz と 800kHz のスイッチング周波数を選択可能
- ソフトスタート時間を変更可能、デフォルトは 内部 1.2ms
- 大きいデューティ・サイクル動作
- パワーグッド・インジケータを内蔵
- 出力放電機能を内蔵
- サイクル単位の過電流保護
- ラッチ付きの出力 OV および UV 保護
- ラッチなしの UVLO および OT 保護
- 動作時接合部温度:-40°C～125°C
- 20 ピン、3.0mm × 3.0mm の HotRod™ VQFN パッケージ
- 12A の TPS56C230 とピン互換
- WEBENCH® Power Designer により、TPS51397A を使用するカスタム設計を作成

2 アプリケーション

- ノート PC およびデスクトップ PC
- ウルトラブック、ハンドヘルド・タブレット
- 産業用 PC 、シングル・ボード・コンピュータ
- 非軍事用ドローン
- 分散電源システム



概略回路図

3 概要

このデバイスは、モノリシックな 10A 同期整流降圧コンバータで、高効率を実現する MOSFET が内蔵されており、また、必要な外付け部品数が最小であるため、スペースの制約が厳しい電力システムでも使いやすくなっています。

TPS51397A は、内部補償により高速な過渡応答と非常に優れたラインおよび負荷レギュレーションを実現する D-CAP3™ 制御を採用しています。低消費電力動作で長いバッテリ寿命を実現しようとする場合、ULQ™ (超低静止電流) 機能は非常に有益です。デューティ比の大きい動作により、入力電圧が低いときは負荷過渡性能が大幅に向上します。

MODE ピンを使って、軽負荷動作向けの Eco-mode™ または Out-of-Audio™ (OOA) モードに設定できます。さらに、500kHz または 800kHz のスイッチング周波数を選択できます。Eco-mode™ は、軽負荷動作時に高効率を維持します。OOA モードは、効率の低下を最小限に抑えながら、スイッチング周波数を可聴周波数より高く維持します。

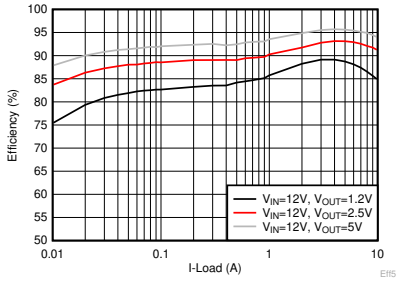
このデバイスは、内部ソフトスタート時間と外部ソフトスタート時間を選択できます。内部ソフトスタート時間は 1.2ms に固定されています。アプリケーションでこれより長いソフトスタート時間が必要な場合、外付けのコンデンサを SS ピンに接続して、長いソフトスタート時間を実現できます。

TPS51397A はパワーグッド・インジケータを内蔵しており、出力放電機能を備えています。また、OVP、UVP、OCP、OTP、UVLO を含む完全な保護機能を備えています。このデバイスは、20 ピンの 3.0mm × 3.0mm HotRod™ パッケージで供給され、-40℃～125℃ の接合部温度で動作が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS51397A	VQFN (20)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係 (500kHz、ECO-mode)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2020) to Revision A (September 2020)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

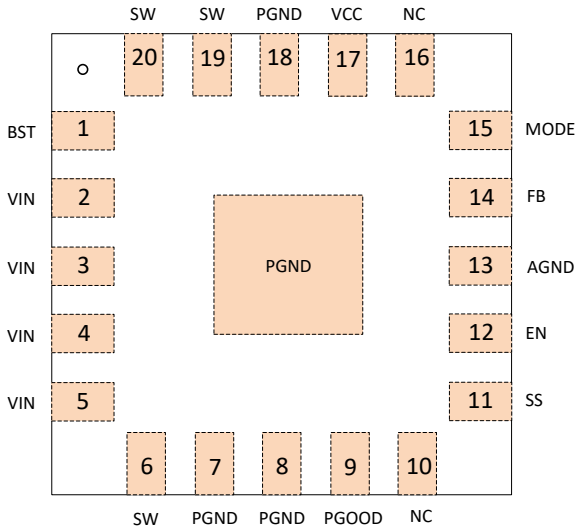


図 5-1. 20-Pin VQFN RJE Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	1	O	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW. 0.1 µF is recommended.
VIN	2,3,4,5	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
SW	6,19,20	O	Switching node connection to the inductor and bootstrap capacitor for buck. This pin voltage swings from a diode voltage below the ground up to input voltage of buck.
PGND	7,8,18, Thermal Pad	G	Power GND terminal for the controller circuit and the internal circuitry
PGOOD	9	O	Open-drain power-good indicator. It is asserted low if output voltage is out of PG threshold, over voltage, or if the device is under thermal shutdown, EN shutdown, or during soft start.
SS	11	O	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the soft-start time is about 1.2 ms.
NC	10,16		Not connect. Can be connected to GND plane for better thermal achieved.
EN	12	I	Enable input of buck converter
AGND	13	G	Ground of internal analog circuitry. Connect AGND to GND plane with a short trace.
FB	14	I	Feedback sensing pin for Buck output voltage. Connect this pin to the resistor divider between output voltage and AGND.
MODE	15	I	Switching frequency and light load operation mode selection pin. Connect this pin to a resistor divider from VCC and AGND for different MODE options shown in 表 7-1.
VCC	17	O	The driver and control circuits are powered from this voltage. Decouple with a minimum 1-µF ceramic capacitor as close to VCC as possible.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	VIN	–0.3	26	V
		VBST	–0.3	31	V
		VBST-SW	–0.3	6	V
		EN, MODE, FB, SS, VCC	–0.3	6	V
		PGND, AGND	–0.3	0.3	V
	Output voltage	SW	–1	26	V
		SW (10-ns transient)	–3	29	V
		PGOOD	–0.3	6	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- V C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	VIN	4.5	24	V
		VBST	–0.3	29.5	V
		VBST-SW	–0.3	5.5	V
		EN, MODE, FB, SS, VCC	–0.3	5.5	V
		PGND, AGND	–0.3	0.3	V
	Output voltage	SW	–1	24	V
		PGOOD	–0.3	5.5	V
I_{OUT}	Output current			10	A
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS51397A RJE (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance (4-layer custom board)(2)	39.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W

THERMAL METRIC(1)		TPS51397A RJE (VQFN) 20 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(2) 70 mm x 70 mm, 4 layers, thickness: 1.5 mm. 2 oz. copper traces located on the top and bottom of the PCB. 4 thermal vias in the PowerPAD area under the device package.

6.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		4.5		24	V
I_{VIN}	Non-switching supply current	No load, V_{EN} = 5V	90	110	150	µA
I_{VINSDN}	Shutdown supply current	No load, V_{EN} = 0V	1	2	4	µA
VCC OUTPUT						
V_{CC}	VCC output voltage	V_{IN} > 5.0V	4.85	5	5.15	V
		V_{IN} = 4.5V		4.5		
I_{CC}	VCC current limit		20			mA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C	591	600	609	mV
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	V_{OUT} = 2.5V	450	500	550	kHz
$t_{ON(MIN)}$	SW minumum on time		30	60	100	ns
$t_{OFF(MIN)}$	SW minimum off time	V_{FB} = 0.5V		130	180	ns
OOA Function						
T_{OOA}	Mode Operation Period		22	30	42	us
MOSFET and DRIVERS						
$R_{DS(ON)H}$	High side switch resistance	T_J = 25°C		17		mΩ
$R_{DS(ON)L}$	Low side switch resistance	T_J = 25°C		5.9		mΩ
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge resistance	V_{EN} = 0V	300	350	400	Ω
t_{SS}	Soft start time	Internal soft-start time, SS pin floating	0.5	1.2	2.5	ms
I_{SS}	Soft start charge current			5		µA
POWER GOOD						
t_{PGDLY}	PG start-up delay	PG from low to high		1		ms
V_{PGTH}	PG threshold	VFB falling (fault)		85		%
		VFB rising (good)		90		%
		VFB rising (fault)		115		%
		VFB falling (good)		110		%
V_{PG_L}	PG sink current capability	I_{OL} = 4mA			0.4	V
I_{PGLK}	PG leak current	V_{PGOOD} = 5.5V			1	µA
CURRENT LIMIT						

T_J = -40°C to 125°C, V_{IN} = 12 V, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{OCL}	Over current threshold (valley)	T_J = 25°C	11	12	13	A
		T_J = -40°C to 125°C	10.5	12	14	A
I_{NOCL}	Negative over current threshold			3.2		A
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage		1.2	1.3	1.4	V
V_{ENL}	EN low-level input voltage		0.9	1.1	1.2	V
I_{EN}	Enable internal pull down current	V_{EN} = 0.8V		2		µA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold			125		%
t_{OVPDLY}	OVP prop deglitch			120		us
V_{UVP}	UVP trip threshold			60		%
t_{UVPDLY}	UVP prop deglitch			256		us
UVLO						
V_{UVLO}	VIN UVLO threshold	Wake up	4.1	4.2	4.4	V
		Shutdown	3.6	3.7	3.9	V
		Hysteresis		0.5		V
OVER TEMPERATURE PROTECTION						
T_{OTP}	OTP trip threshold(1)	Shutdown temperature		150		°C
T_{OTPHSY}	OTP hysteresis(1)	Hysteresis		20		°C

(1) Not production tested.

6.6 Typical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V, unless otherwise noted.

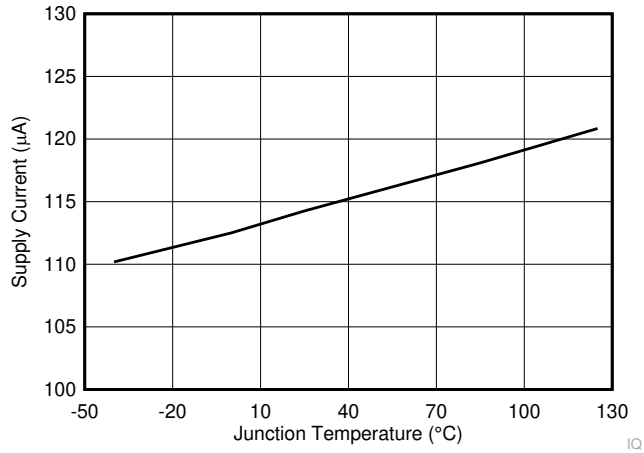


図 6-1. Supply Current vs Junction Temperature

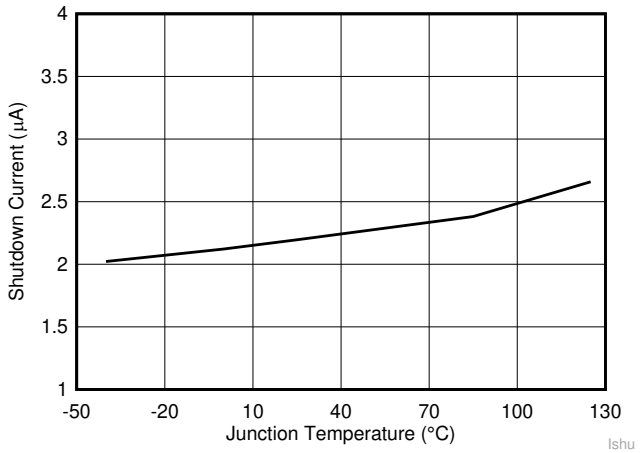


図 6-2. Shutdown Current vs Junction Temperature

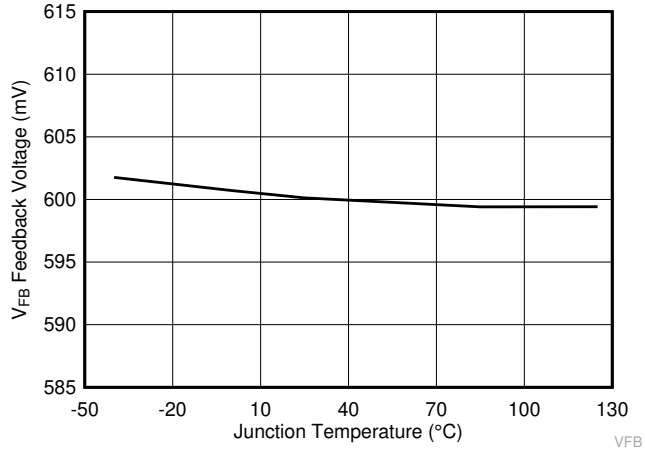


図 6-3. Feedback Voltage vs Junction Temperature

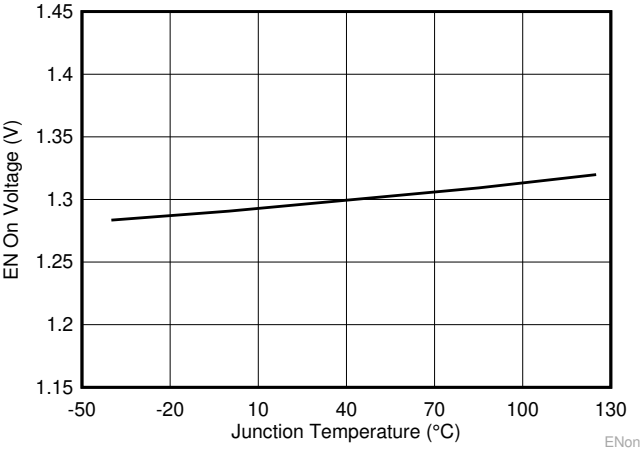


図 6-4. Enable On Voltage vs Junction Temperature

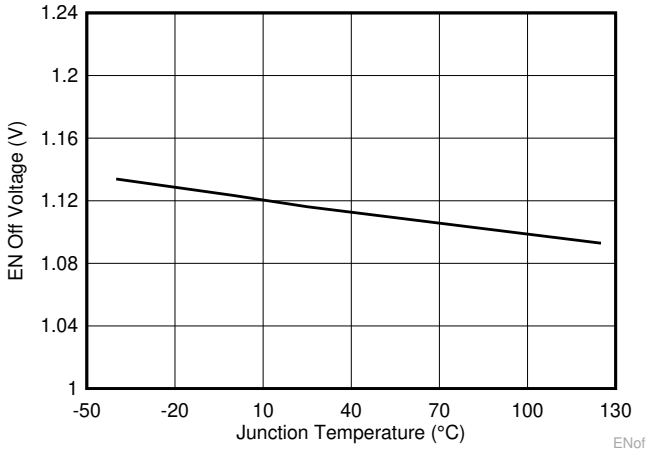


図 6-5. Enable Off Voltage vs Junction Temperature

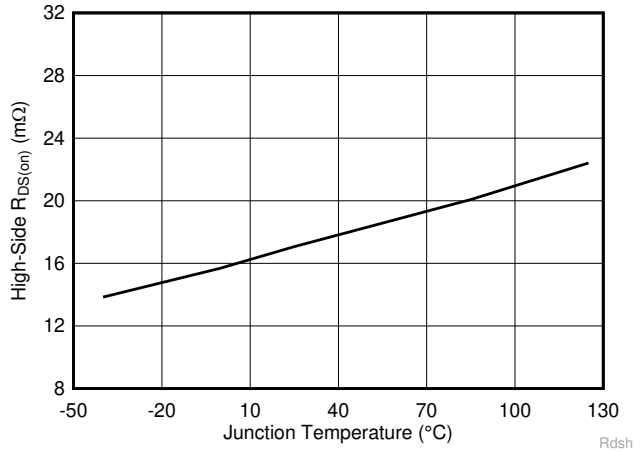


図 6-6. High-Side $R_{DS(on)}$ vs Junction Temperature

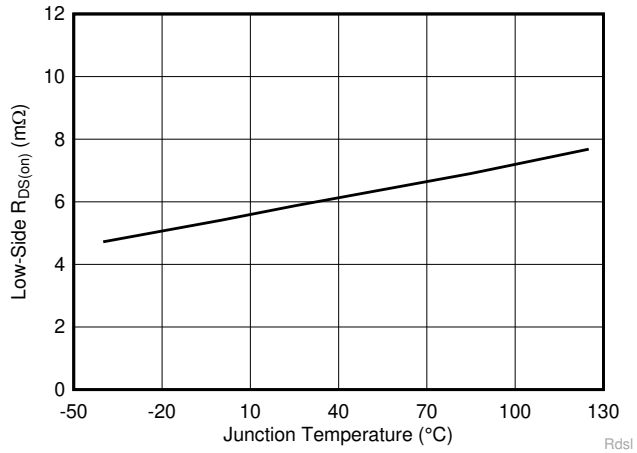


図 6-7. Low-Side $R_{DS(on)}$ vs Junction Temperature

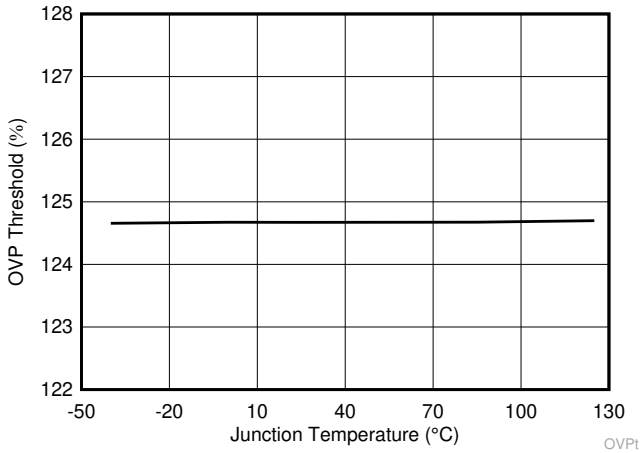


図 6-8. OVP Threshold vs Junction Temperature

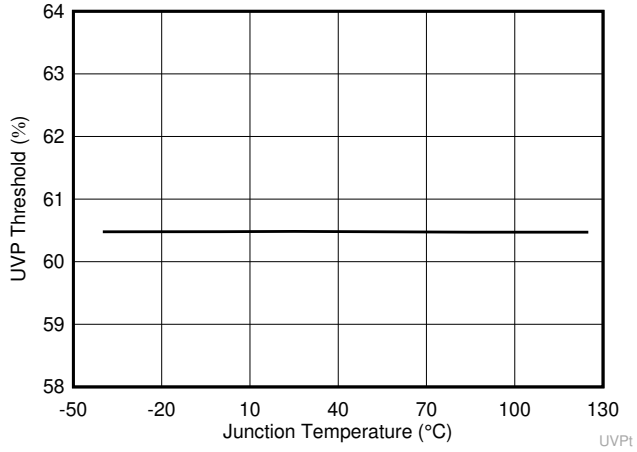


図 6-9. UVP Threshold vs Junction Temperature

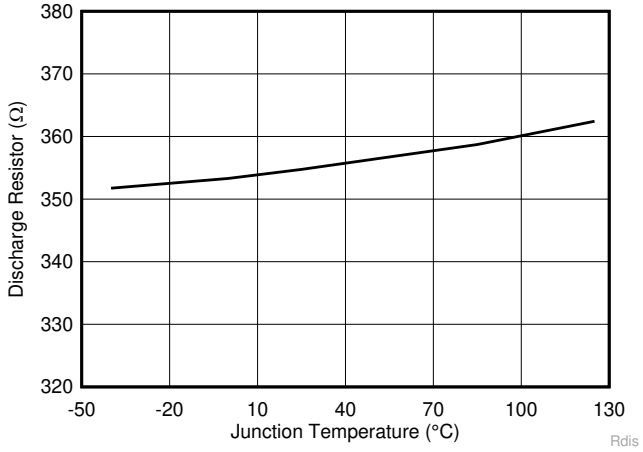


図 6-10. Discharge Resistor vs Junction Temperature

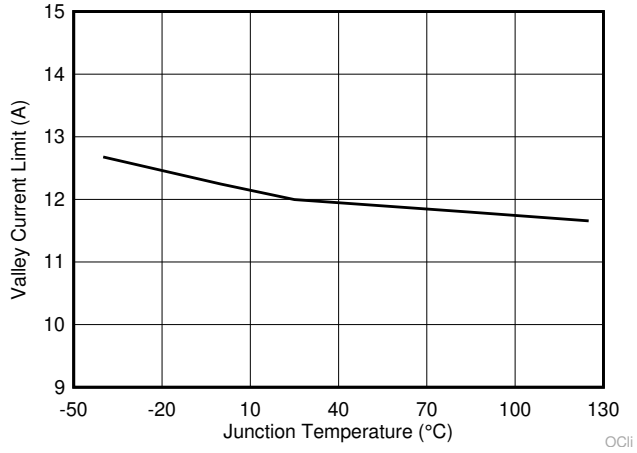


図 6-11. Valley Current Limit vs Junction Temperature

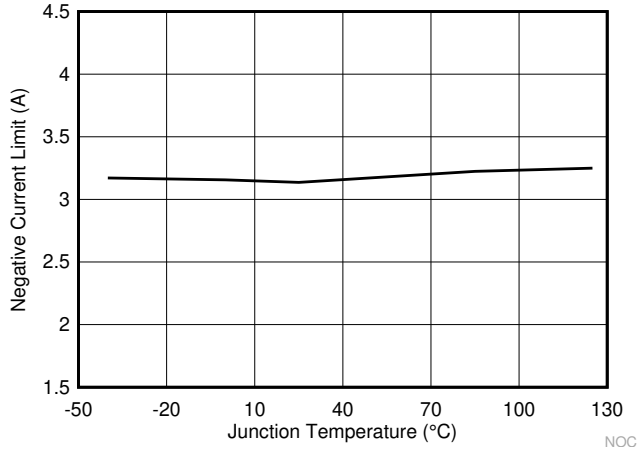


図 6-12. Negative Current Limit vs Junction Temperature

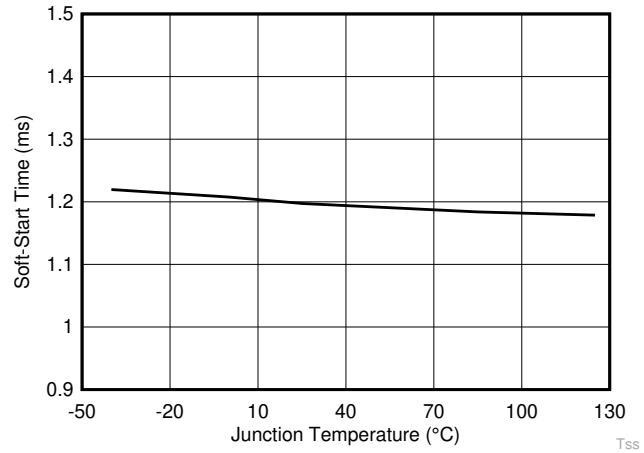


図 6-13. Soft-Start Time vs Junction Temperature

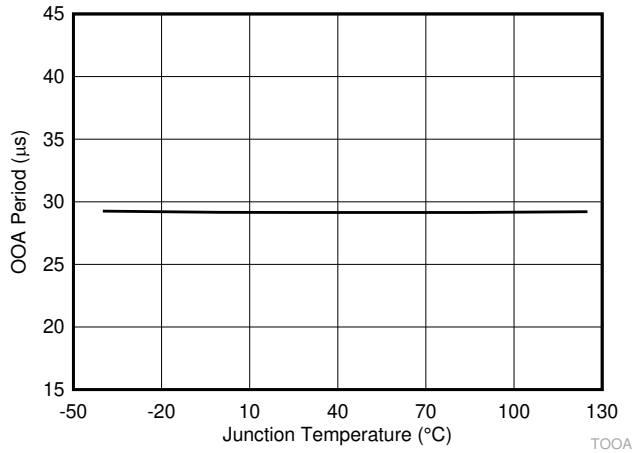


図 6-14. OOA Period vs Junction Temperature

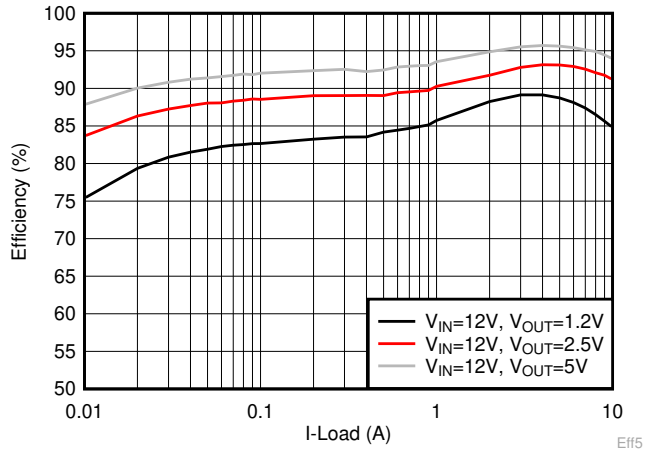


図 6-15. Efficiency vs Load Current, F_{SW} = 500 kHz, Eco-mode

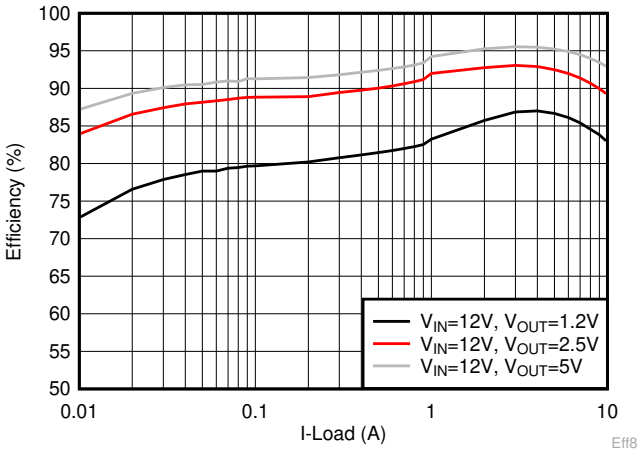


図 6-16. Efficiency vs Load Current, F_{SW} = 800 kHz, Eco-mode

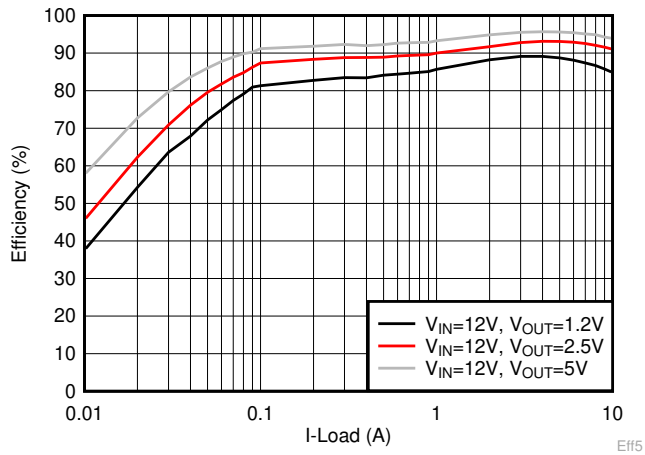


図 6-17. Efficiency vs Load Current, F_{SW} = 500 kHz, OOA

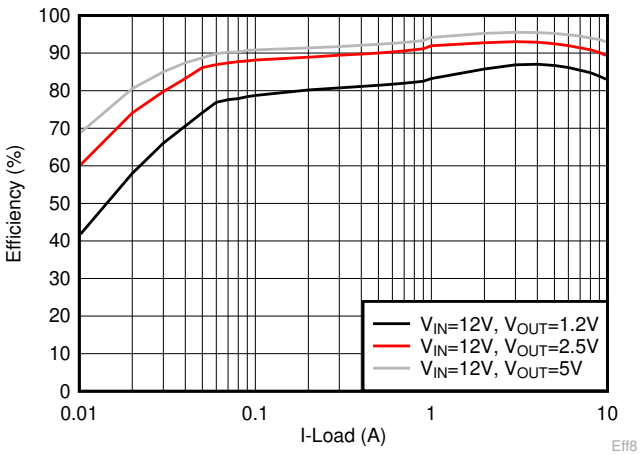


図 6-18. Efficiency vs Load Current, F_{SW} = 800 kHz, OOA

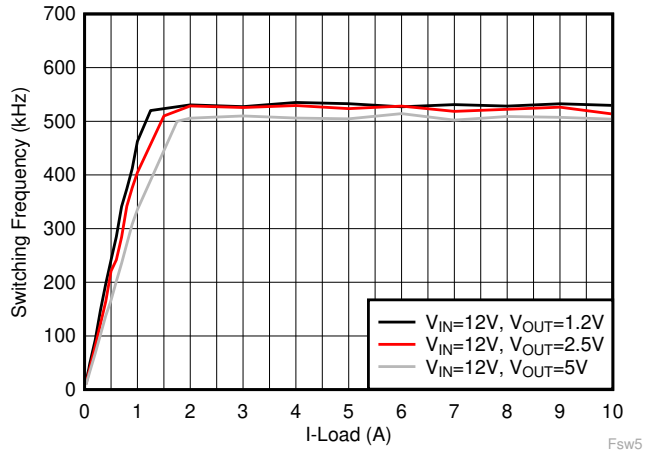


図 6-19. Switching Frequency vs Load Current, F_{SW} = 500 kHz, Eco-mode

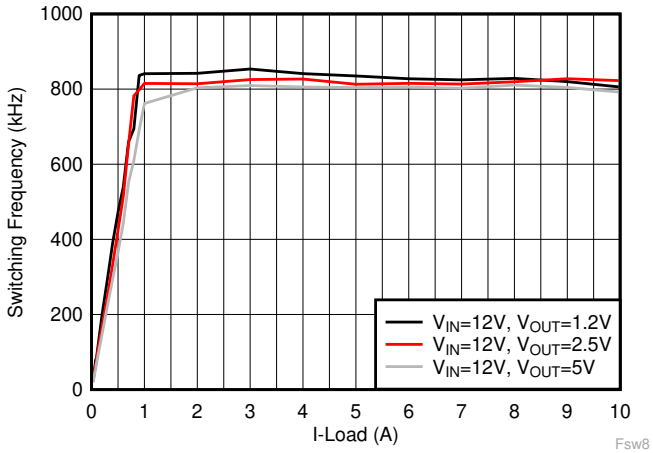


図 6-20. Switching Frequency vs Load Current, F_{SW} = 800 kHz, Eco-mode

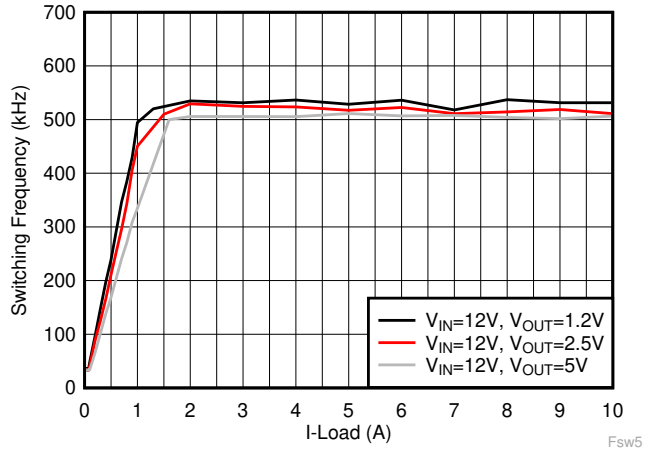


図 6-21. Switching Frequency vs Load Current, F_{SW} = 500 kHz, OOA

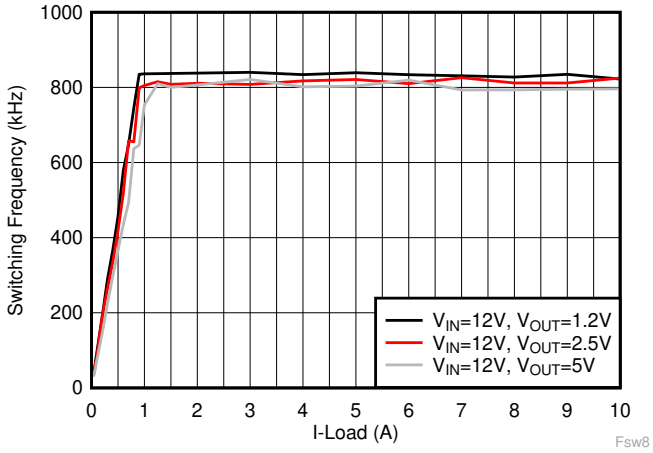


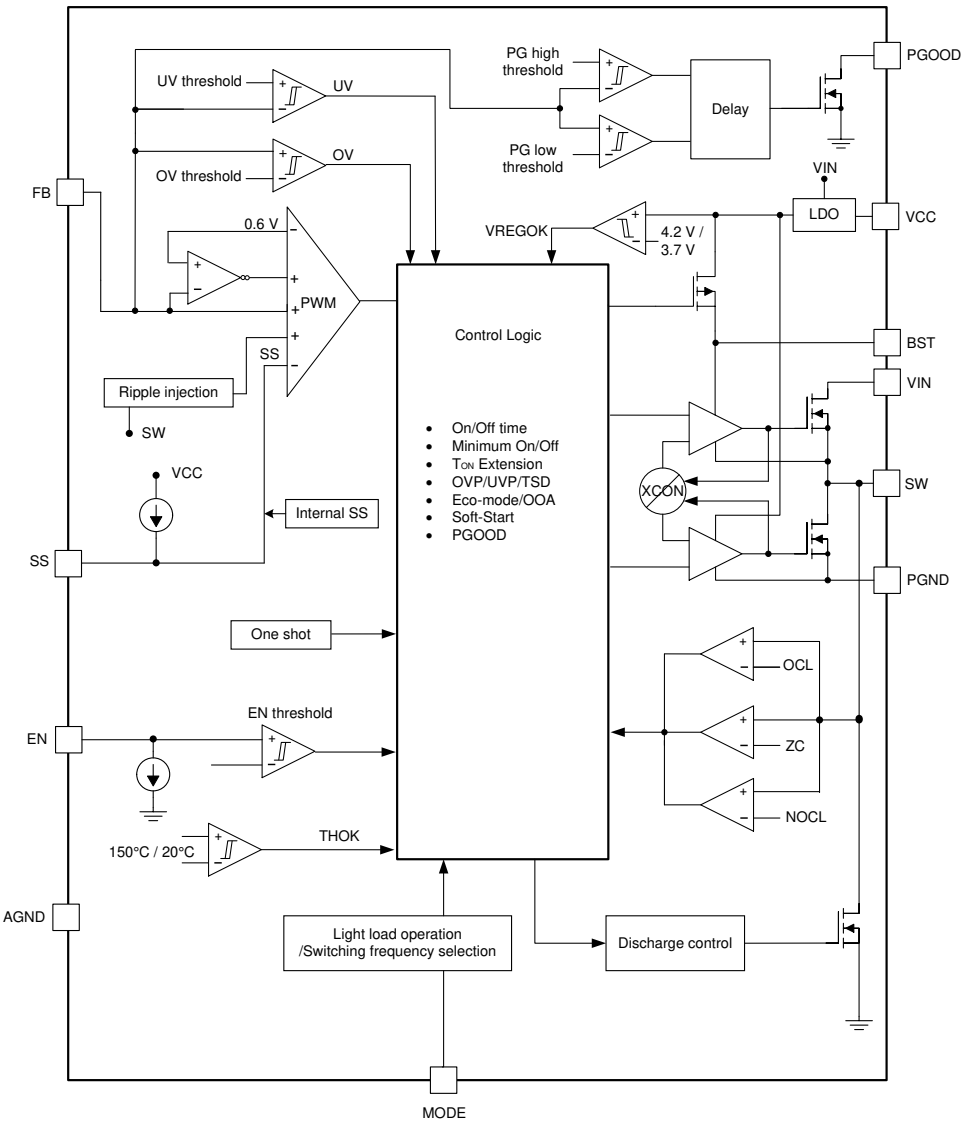
図 6-22. Switching Frequency vs Load Current, F_{SW} = 800k Hz, OOA

7 Detailed Description

7.1 Overview

TheTPS51397A is a high density synchronous buck converter that operates from 4.5-V to 24-V input voltage, and 0.6-V to 5.5-V output voltage range. It has 17-mΩ and 5.9-mΩ integrated MOSFETs that enable high efficiency up to 10 A. The ULQ™ (Ultra Low Quiescent) feature is extremely beneficial for long battery life in low power operation. The large duty operation greatly improves the load transient performance when input voltage is low. The device employs DCAP3™ mode control that enables low external component count, ease of design, optimization of the power design for cost, size, and efficiency, and provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology supports seamless transition between CCM mode at heavy load conditions and DCM operation at light load conditions. Eco-mode™ allows the TPS51397A to maintain high efficiency at light load and OOA mode makes switching frequency above audible frequency (20 kHz), even there is no loading at output side. The TPS51397A is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and DCAP3™ Control

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS51397A also includes an error amplifier that makes the output voltage high accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage, V_{IN}, and is inversely proportional to the output voltage, V_{OUT}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple. This enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS51397A is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in 式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the external output set-point resistor divider network and the internal gain of the TPS51397A. The low-frequency L-C double pole has a 180 degree lag in-phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a mid-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase to 90 degree one decade above the zero frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the mid-frequency zero so that the phase boost provided by this mid-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (F_{SW}).

7.3.2 Soft Start

The TPS51397A has an internal 1.2-ms soft start. An external SS pin is provided for setting higher soft-start time if needed. When the EN pin becomes high, the soft-start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a higher soft-start time, it can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in 式 2:

$$T_{ss}(ms) = \frac{C_{ss}\ (nF) \times V_{REF}\,(V)}{I_{ss}\,(uA)} \quad (2)$$

where

- V_{REF} is 0.6 V and I_{SS} is 5 µA

7.3.3 Large Duty Operation

The TPS51397A can support large duty operation by its internal T_{ON} extension function. When V_{IN}/V_{OUT} < 1.6 and the V_{FB} keeps lower than internal V_{REF}, T_{ON} is extended to implement the large duty operation which greatly improves the load transient performance.

7.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. A pullup resistor of 100 kΩ is recommended to pull the voltage up to VCC. Once V_{FB} is between 90% and 110% of the target output voltage, the PGOOD is pulled high after a 1-ms de-glitch time. The PGOOD pin is pulled low when:

- FB pin voltage is lower than 85% or greater than 115% of the target output voltage,
- In OVP, UVP, or thermal shutdown event, or
- During the soft-start period.

7.3.5 Overcurrent Protection and Undervoltage Protection

The TPS51397A has overcurrent protection and undervoltage protection. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the output current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, and the device is shut off after a wait time of 256 µs. This protection is a latched function. The fault latching can be reset by EN going low or VCC power cycling.

The TPS51397A also implements negative overcurrent protection, which can prevent inductor current runaway when IC works in OOA mode. When the inductor valley current hits the negative overcurrent threshold (NOCL = –3.2 A typical), the low-side FET turns off, then high-side FET turns on.

7.3.6 Overvoltage Protection

The TPS51397A has an overvoltage protection feature, which has the same implementation. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, and the output will be discharged and latched after a wait time of 120 µs. This function is a latching operation, so it needs to reset by EN going low or VCC power cycling.

7.3.7 UVLO Protection

The VIN undervoltage lockout (UVLO) protection monitors the VCC pin voltage to protect the internal circuitry from low input voltage. When the VCC voltage is lower than the UVLO threshold voltage, the device shuts off and outputs are discharged to prevent mis-operation of the device. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 500 mV (typical). This is a non-latch protection.

7.3.8 Output Voltage Discharge

The TPS51397A has a discharge function by using internal MOSFET about 350 Ω, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET.

7.3.9 Thermal Shutdown

The TPS51397A monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device is shut off and the output is discharged. This is a non-latch protection. The device restarts operation when the temperature goes below the thermal shutdown threshold.

7.4 Device Functional Modes

7.4.1 Light Load Operation

The TPS51397A has a MODE pin that can control two different states of operation at light load. The light load operation includes advanced Eco-mode and OOA mode.

7.4.2 Advanced Eco-mode Control

The advanced Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in continuous conduction mode so that it takes longer to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$) can be calculated from 式 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 40% of $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

7.4.3 Out-of-Audio

Out-of-Audio (OOA) light-load mode is a unique control feature that keeps the switching frequency above audible frequency with minimum reduction in efficiency. It prevents audio noise generation from the output capacitors and inductor. During Out-of-Audio operation, the OOA control circuit monitors the states of both high-side and low-side MOSFETs and forces them to switch. When both high-side and low-side MOSFETs are off for more than 30 µs during a light-load condition, the low-side FET will discharge until output voltage drops to trigger the high-side FET on or inductor current hits negative OC limit.

If the MODE pin is selected to operate in OOA mode, when the device works at light load, the minimum switching frequency is above 20 kHz which avoids the audible noise in the system. When the device works in OOA mode, TI recommends setting the peak value of inductor current above –1 A by choosing appropriate inductor.

7.4.4 Mode Selection

The device detects the voltage on the MODE pin during start-up and latches onto one of the MODE options listed in 表 7-1. The voltage on the MODE pin is recommended to be set by connecting this pin to the center tap of a resistor divider connected between VCC and AGND. A guideline for the top resistor (R_{M_H}) and the bottom resistor (R_{M_L}) as 1% resistors is shown in 表 7-1. It is recommended to choose the resistor to set the voltage at around the middle value of each range. It is important that the voltage for the MODE pin is derived from the VCC rail only since internally this voltage is referenced to detect the MODE option, and not to leave the mode pin floating. The MODE pin setting can be reset only by a VIN power cycling or EN toggle.

表 7-1. MODE Pin Resistor Settings

VOLTAGE ON MODE	R_{M_H}(kΩ)	R_{M_L} (kΩ)	LIGHT LOAD OPERATION	FREQUENCY (kHz)
(0~10%)*VCC	330	15	Eco-mode	500
(10%~20%)*VCC	180	33	OOA	500
(20%~30%)*VCC	160	51	Eco-mode	800
(30%~50%)*VCC	75	51	OOA	800

図 7-1 shows the typical start-up sequence of the device once the enable signal crosses the EN turnon threshold. After the voltage on VCC crosses the rising UVLO threshold, it takes about 500 µs to finish the working mode and frequency selection. The output voltage starts ramping after about 0.2*T_{SS} delay time.

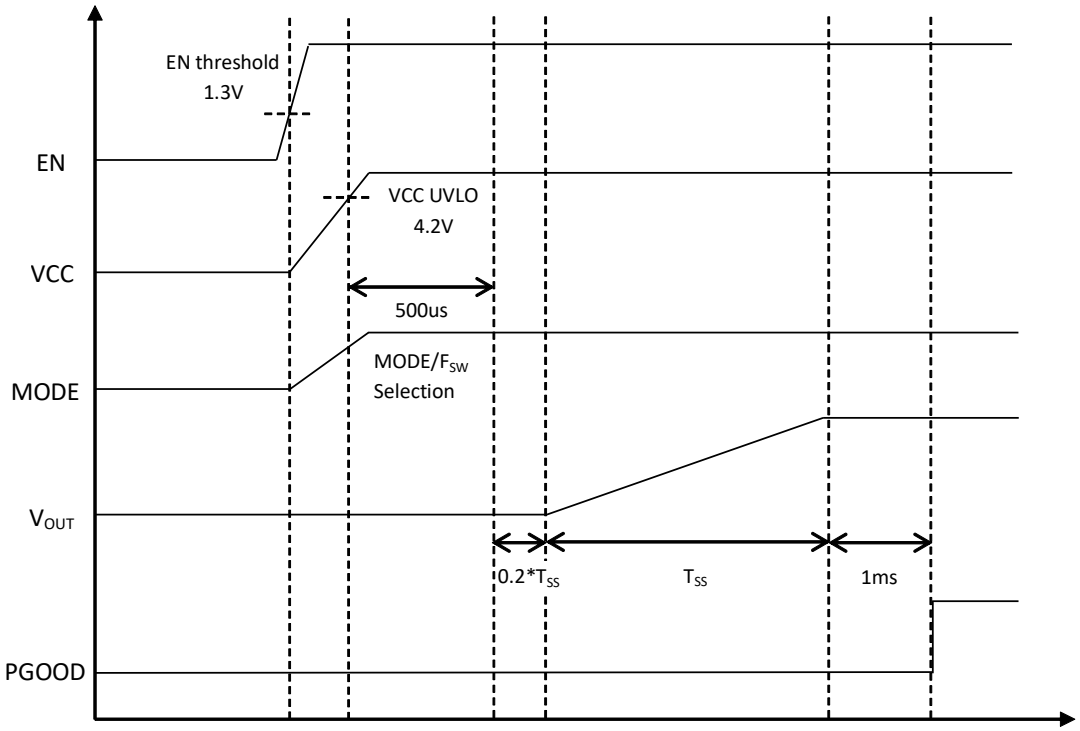


図 7-1. Power-Up Sequence

7.4.5 Standby Operation

The TPS51397A can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2 µA when in standby condition. EN pin is pulled low internally. When floating, the part is disabled by default.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The schematic in 図 8-1 shows a typical application for TPS51397A with 5-V output. This design converts an input voltage range of 5.5 V to 24 V down to 5 V with a maximum output current of 10 A.

8.2 Typical Application

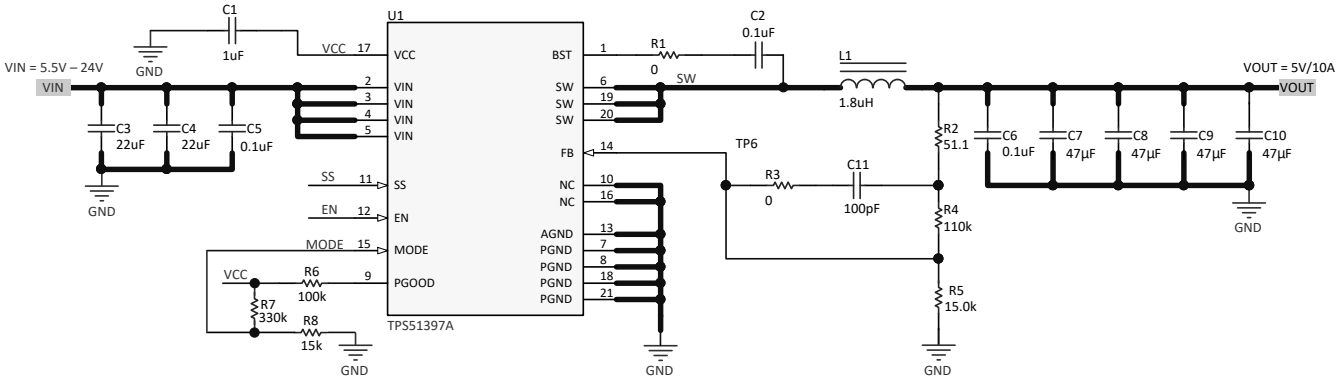


図 8-1. 5-V, 10-A Reference Design

8.2.1 Design Requirements

表 8-1 lists the design parameters for this example.

表 8-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Output voltage			5		V
I_{OUT}	Output current			10		A
ΔV_{OUT}	Transient response	1-A — 9-A load step, 2.5 A/µs		±5% x V_{OUT}		
V_{IN}	Input voltage		5.5	12	24	V
$V_{OUT(ripple)}$	Output voltage ripple	0-A — 10-A loading		2% x V_{OUT}		
F_{SW}	Switching frequency			500		kHz
	Light load operating mode			Eco-mode		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor, you can change the output voltage above 0.6 V. See 式 4.

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}}) \quad (4)$$

8.2.2.1.2 MODE Selection

The light load operation mode (Eco-mode or OOA) and switching frequency are set by a voltage divider from VCC to GND connected to the MODE pin. See 表 7-1 for possible MODE pin configurations. For this design example, the switching frequency is about 500 KHz, the light load operation mode is Eco-mode, and the output current is 10 A.

8.2.2.1.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See 表 8-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 式 5 and 式 6. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)}=\sqrt{\left(I^2_{OUT}+\frac{1}{12}\times\left(\frac{V_{OUT}\times\left(V_{IN(max)}-V_{OUT}\right)}{V_{IN(max)}\times L_{OUT}\times F_{SW}}\right)^2\right)} \quad (5)$$

$$I_{L(peak)}=I_{OUT}+\frac{I_{OUT(ripple)}}{2} \quad (6)$$

Under transient and short-circuit conditions, the inductor current can increase up to the current limit of the device, so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.4 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. In D-CAP3, the regulator reacts within one cycle to the change in the duty cycle, so good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 8-2. Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

表 8-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
0.6	10	0	500	0.33	66	330	-
			800	0.22	66	330	-
1.2	10	10	500	0.68	66	330	-
			800	0.47	66	330	-
2.5	15	47.5	500	1.2	66	330	-
			800	1.0	66	330	-
3.3	20	90	500	1.5	66	330	22-110
			800	1.2	66	330	22-110
5.0	15	110	500	1.8	66	330	22-110
			800	1.5	66	330	22-110

8.2.2.1.5 Input Capacitor Selection

The TPS51397A requires input decoupling capacitors on power supply input pin VIN, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in 式 7.

$$C_{IN(min)}=\frac{I_{OUT}\times V_{OUT}}{V_{INripple}\times V_{IN}\times F_{SW}} \quad (7)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of nominal 44 µF/35 V on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 式 8:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (8)$$

8.2.3 Application Curves

図 8-2 through 図 8-17 apply to the circuit of 図 8-1. V_{IN} = 12 V, T_A = 25°C, unless otherwise specified.

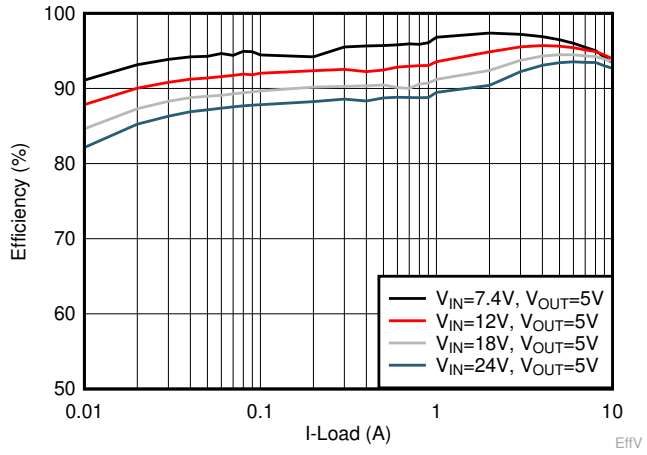


図 8-2. Efficiency Curve

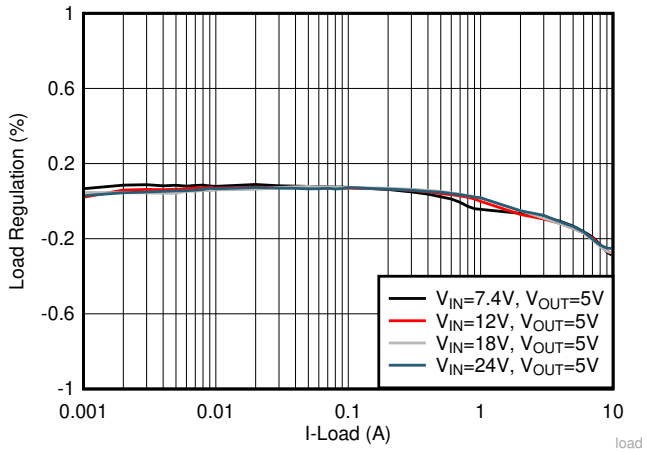


図 8-3. Load Regulation

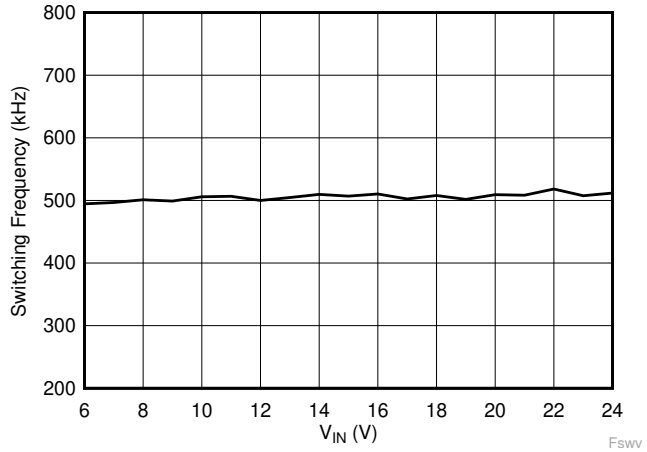


図 8-4. Switching Frequency vs Input Voltage, I_{OUT} = 5 A

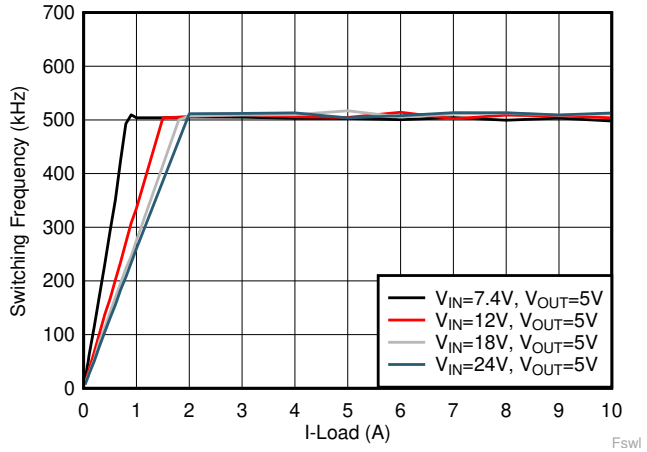


図 8-5. Switching Frequency vs Output Load

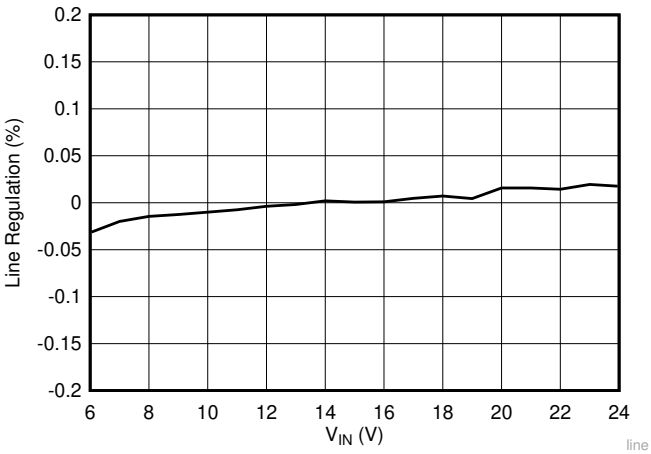


図 8-6. Line Regulation, I_{OUT} = 0.1 A

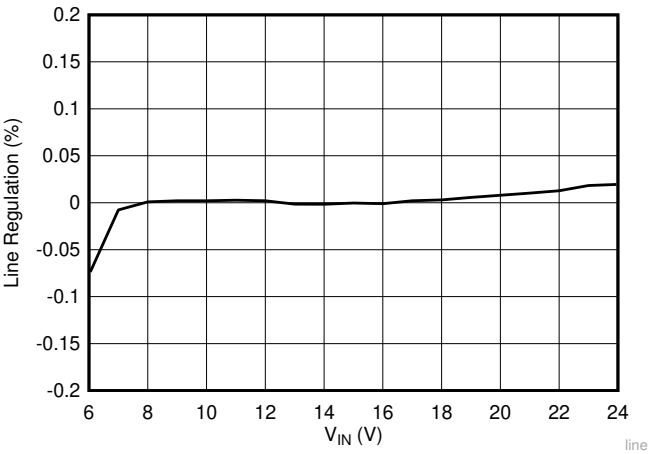


図 8-7. Line Regulation, I_{OUT} = 5 A

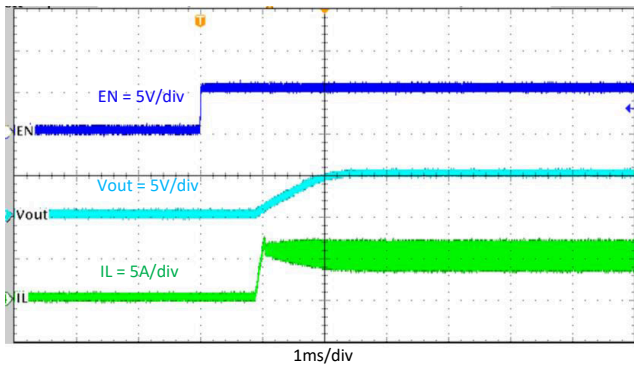


図 8-8. Start-Up Through EN, I_{OUT} = 5 A

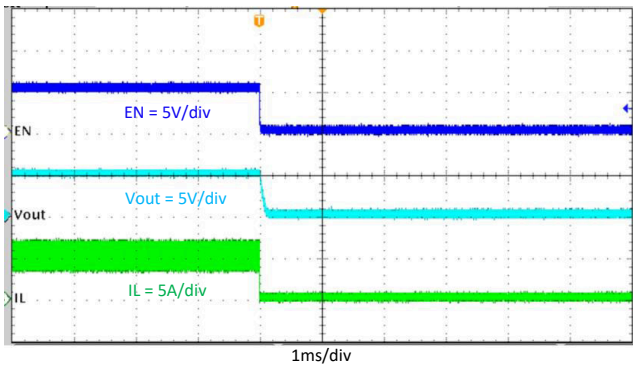


図 8-9. Shut-down Through EN, I_{OUT} = 5 A

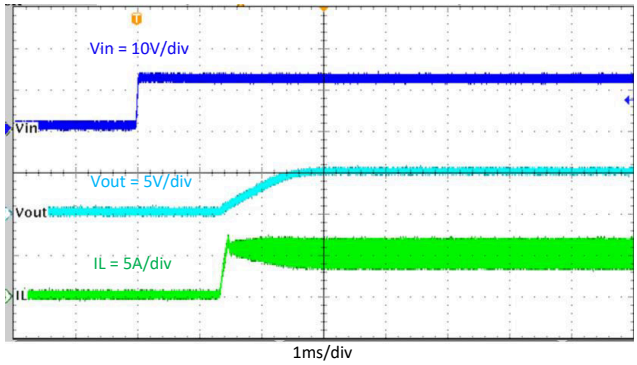


図 8-10. Start-up Relative to VIN Rising, I_{OUT} = 5 A

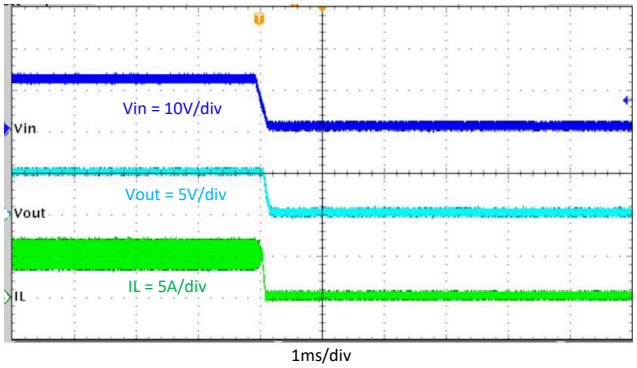


図 8-11. Shut Down Relative to VIN Falling, I_{OUT} = 5 A

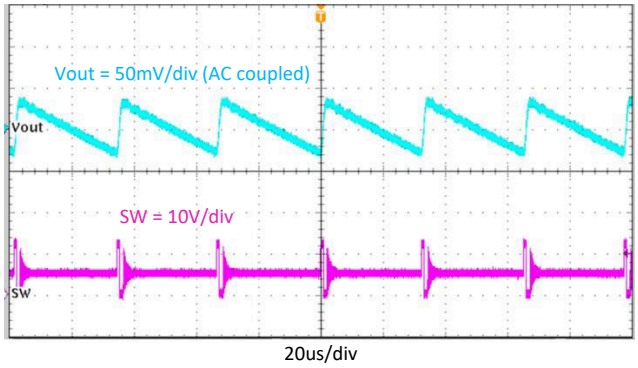


図 8-12. Output Voltage Ripple, I_{OUT} = 0.1 A

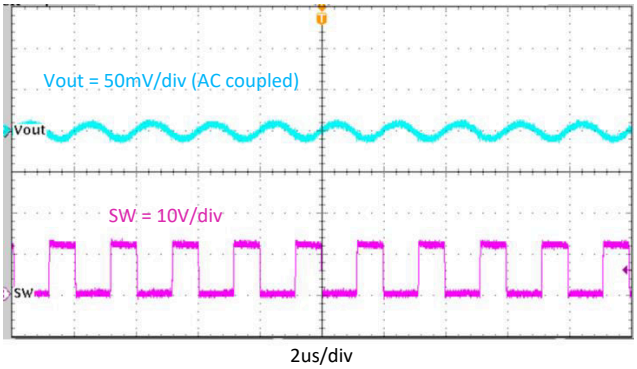


図 8-13. Output Voltage Ripple, I_{OUT} = 5 A

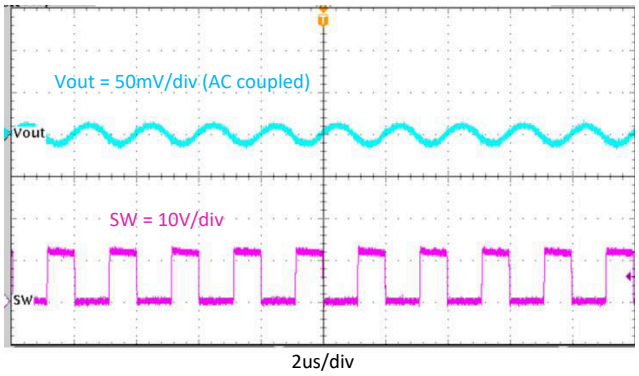


図 8-14. Output Voltage Ripple, I_{OUT} = 10 A

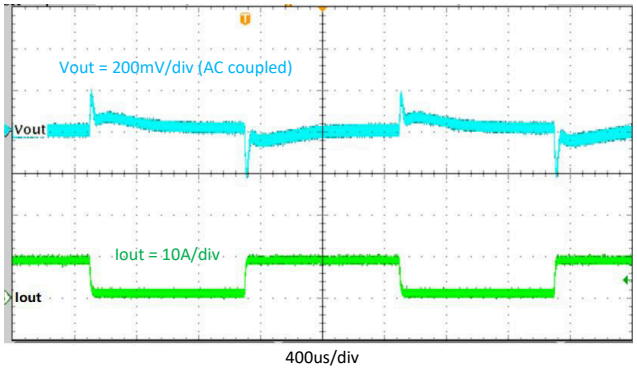


図 8-15. Transient Response, 1 A to 9 A, Slew Rate = 2.5 A/µs

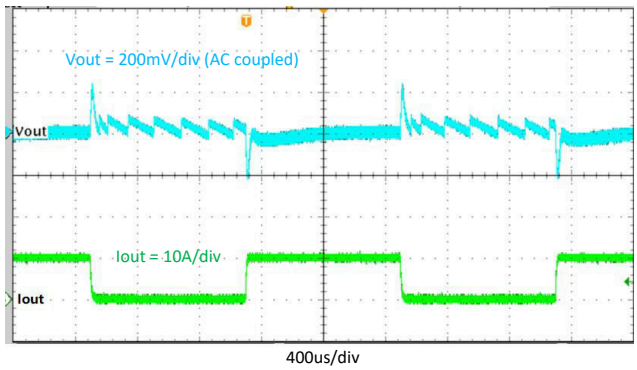


図 8-16. Transient Response, 0 A to 10 A, Slew Rate = 2.5 A/µs

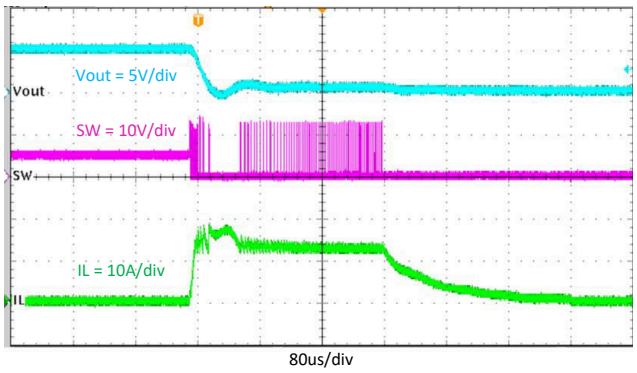


図 8-17. Normal Operation to Output Hard Short

9 Power Supply Recommendations

The TPS51397A is intended to be powered by a well-regulated DC voltage. The input voltage range is 4.5 V to 24 V. The TPS51397A is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far away from the TPS51397A circuit, some additional input bulk capacitance is recommended. Typical values are 100 µF to 470 µF.

10 Layout

10.1 Layout Guidelines

- A four-layer PCB is recommended for good thermal performance and with maximum ground plane. 3-inch × 2.75-inch, top and bottom layer PCB with 2-oz copper is used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductors and capacitors with IC at the same layer. SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the PGND connection of output capacitors and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane. >10-mil width trace is recommended to reduce line parasitic inductance.
- Feedback can be 10 mil and must be routed away from the switching node, BST node, or other high speed digital signal.
- VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance.

10.2 Layout Example

図 10-1 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in 図 8-1.

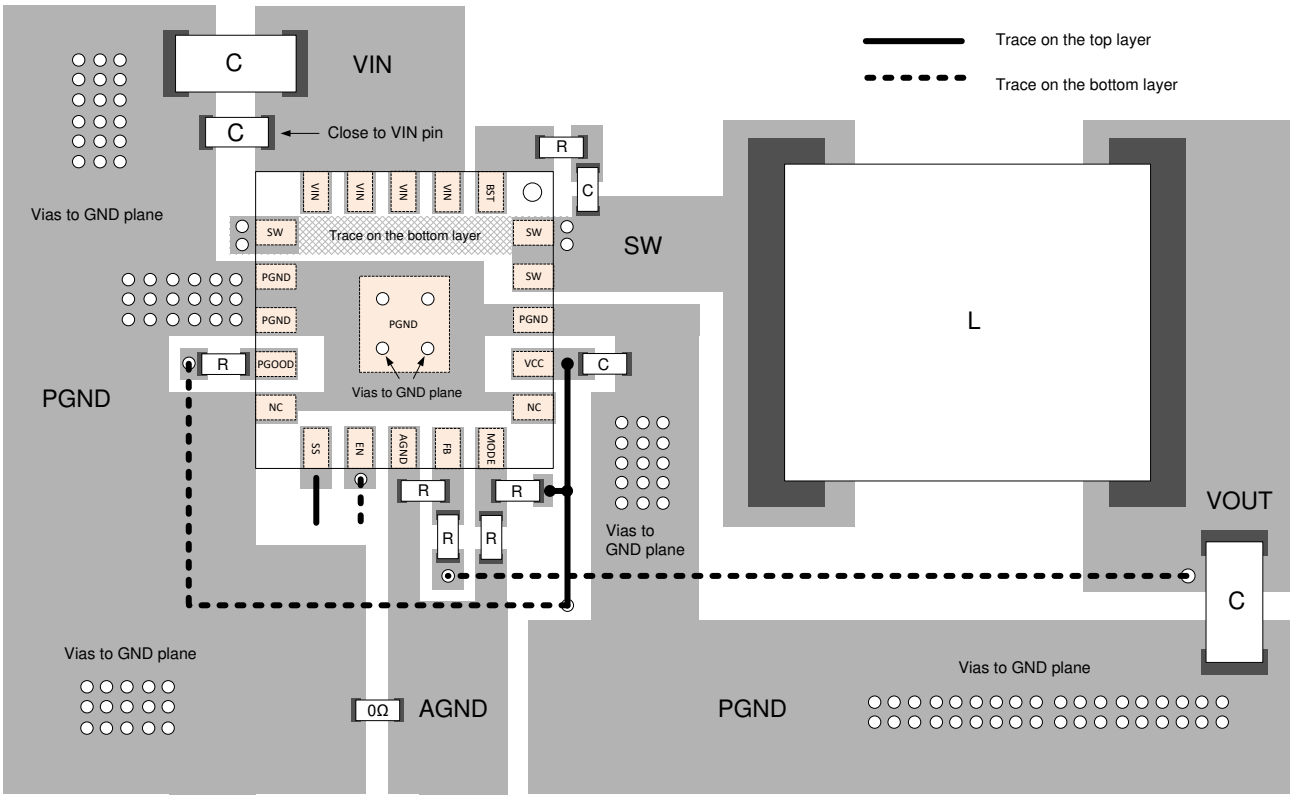


図 10-1. Top-Side Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

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11.5 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51397ARJER	Active	Production	VQFN-HR (RJE) | 20	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-2-260C-1 YEAR	-40 to 125	51397A
TPS51397ARJER.A	Active	Production	VQFN-HR (RJE) | 20	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	51397A
TPS51397ARJER.B	Active	Production	VQFN-HR (RJE) | 20	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	51397A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

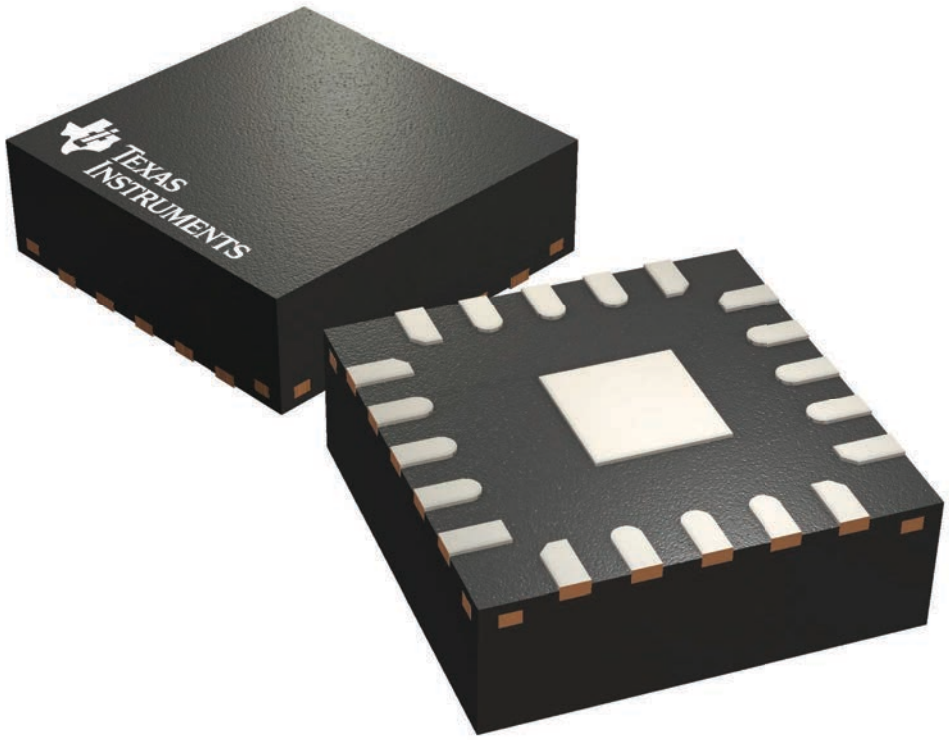
GENERIC PACKAGE VIEW

RJE 20

VQFN-HR - 1 mm max height

3 x 3, 0.45 mm pitch

QUAD FLATPACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

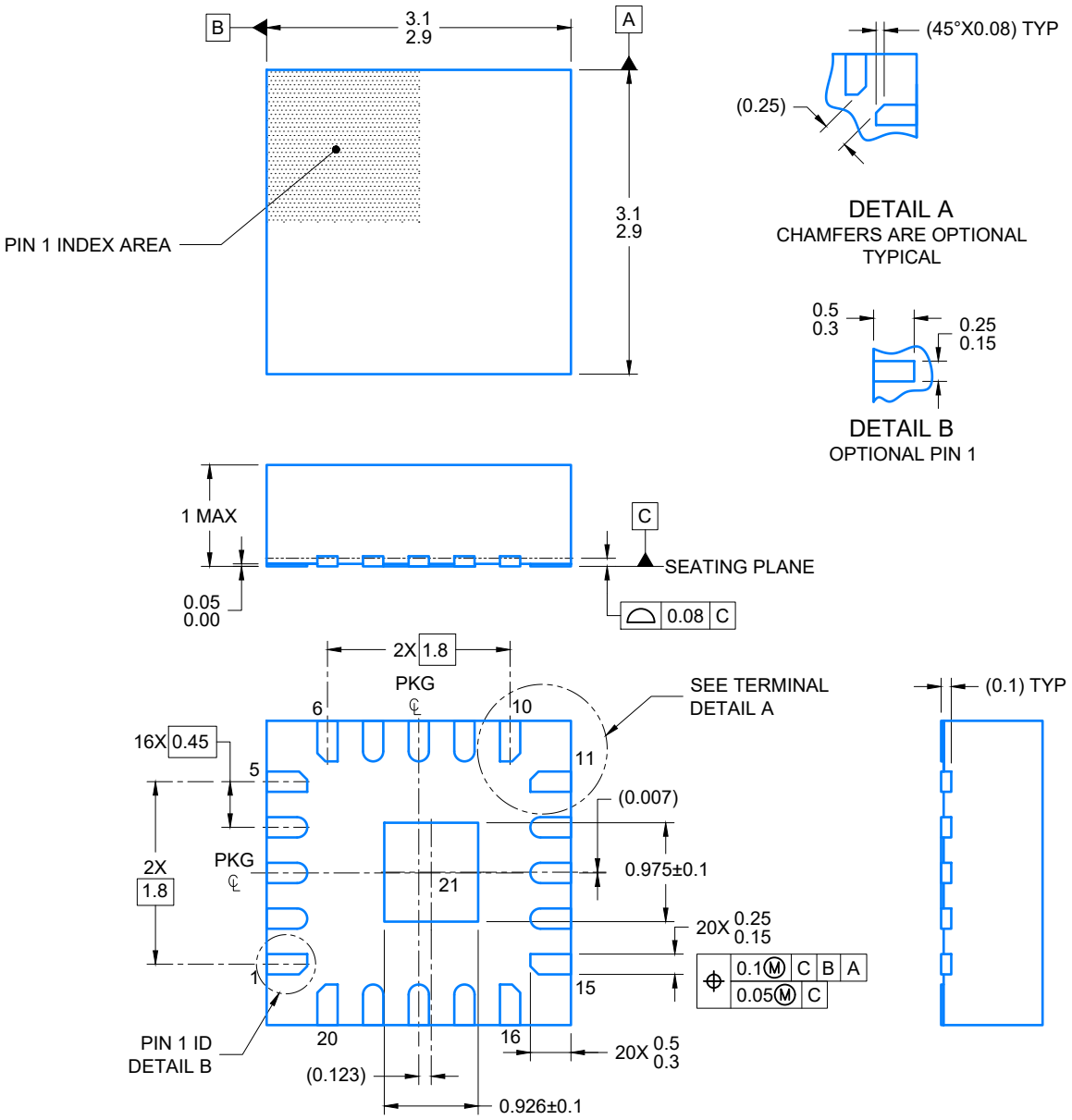
4224683/A

PACKAGE OUTLINE

RJE0020B

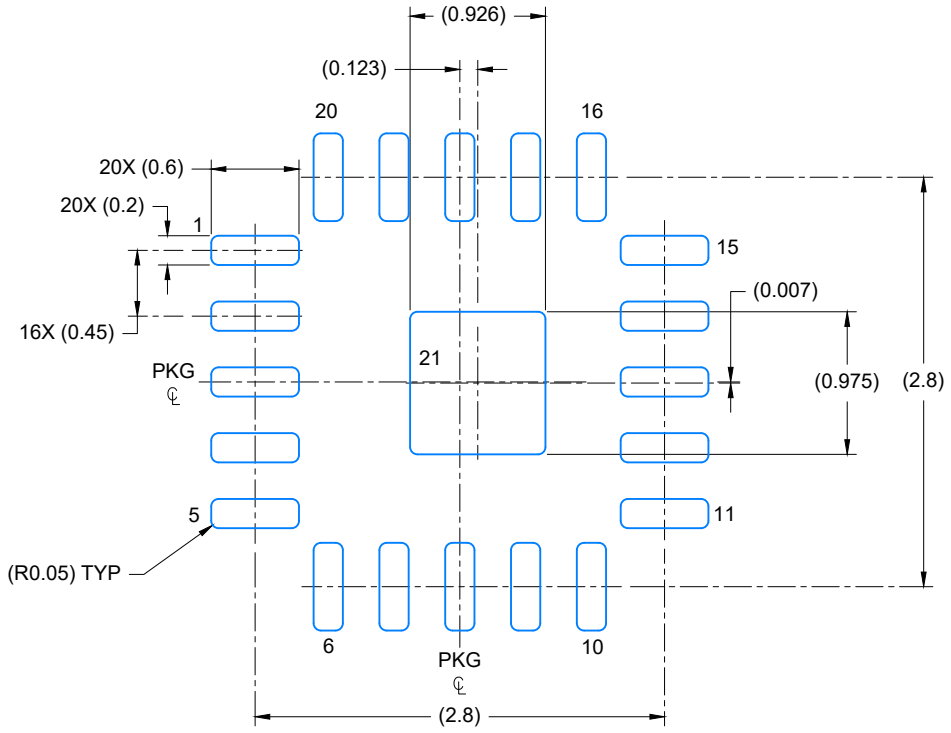
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

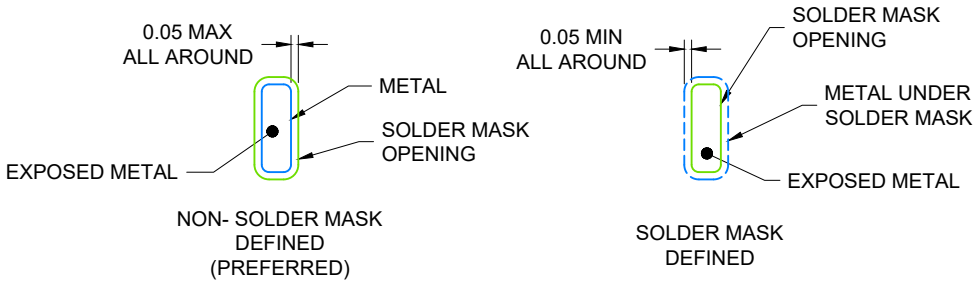


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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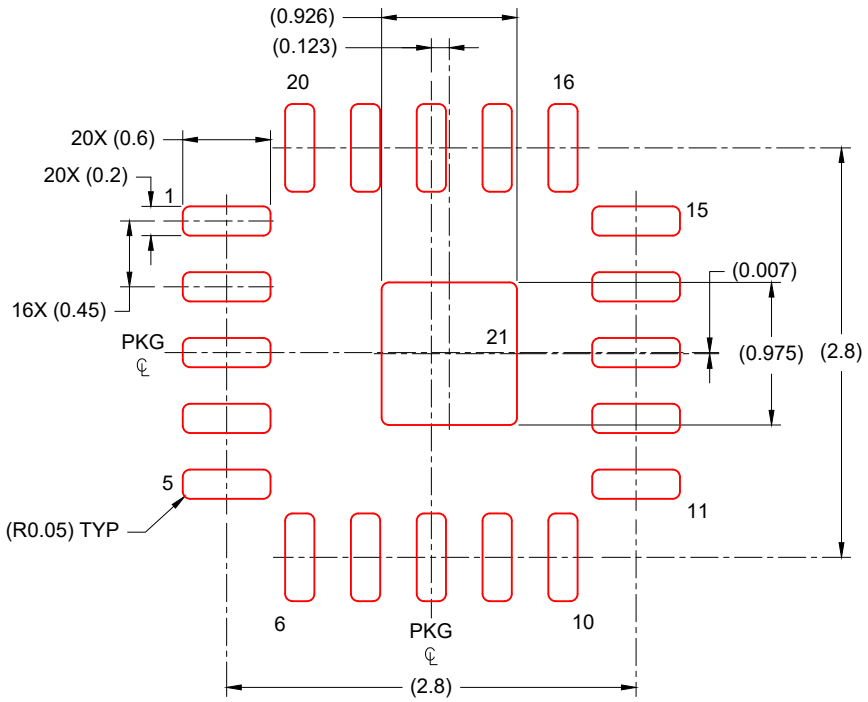
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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最終更新日：2025 年 10 月