TPS53681 デュアル・チャネル(6-Phase + 2-Phase) or (5-Phase + 3-Phase) D-CAP+™多相降圧コントローラ、NVMおよびPMBus™搭載

1 特長

- 変換入力電圧範囲：4.5V～17V
- 8ビットDAC、5mVまたは10mVの分解能を選択可能、出力電圧範囲：0.25V～1.52Vまたはデュアルチャネルで0.5～2.8125V
- 位相構成
  - 最大（6相+2相）または（5相+3相）
  - 最小（1相+1相）
- ドライバ不要の構成により効率的な高周波数のスイッチングを実現
- PMBusインターフェイスを介して設定可能なスルーレートによる動的な出力電圧遷移
- 閉ループ周波数制御による周波数選択：300kHz～1MHz
- プログラム可能な内部ループ補償
- 不揮発性メモリ(NVM)により設定可能なため外付け部品点数が少ない
- 位相ごとの電流較正およびレポート
- 設定可能な電流スレッショルドによる動的な位相シェディングで軽負荷時および重負荷時の効率を最適化
- 高速な位相追加によるアンダーシュート低減(USR)
- TI NexFET™電力段への完全対応により高密度ソリューションを実現
- 正確で変更可能な電圧ポジショニング
- 特許取得の AutoBalance™フェーズ・バランシング
- 位相単位で16レベルの電流制限を選択可能
- PMBus™電圧、電流、電力、温度、フォルト状態の遠隔測定に対応するシステム・インターフェイス
- 低静止電流
- 5mm×5mm、40ピン、QFN PowerPad™パッケージ

2 アプリケーション

- ネットワーク・プロセッサの電源(Broadcom®、Cavium®)
- データセンター、キャンパス、および支店のスイッチ
- コア/エッジ・ルータ
- 大電流のFPGA電源(Intel®、 Xilinx®)

3 概要

TPS53681はデュアルチャネル対応の、不揮発性メモリ(NVM)と PMBus™インターフェイスを内蔵した多相降圧コントローラで、TIのNexFET ™出力段に完全対応しています。また、D-CAP+™アーキテクチャなどの高度な制御機能とアンダーシュート低減(USR)により、高速な過渡応答、低出力容量、高効率を実現します。また、新しい位相インターリーブ方式と動的な位相シェディングにより、さまざまな負荷で効率が向上します。可変スルーレートによる高速な動的電圧遷移に対応する一方、PMBus通信インターフェイスをサポートしているため、電圧、電流、電力、温度、フォルト状態の遠隔測定レポートをシステムに送信できます。プログラム可能なパラメータは、いずれもPMBusインターフェイスを介して設定し、新しいデフォルト値としてNVMに保存できるため、外付け部品点数を最小限に抑えることができます。

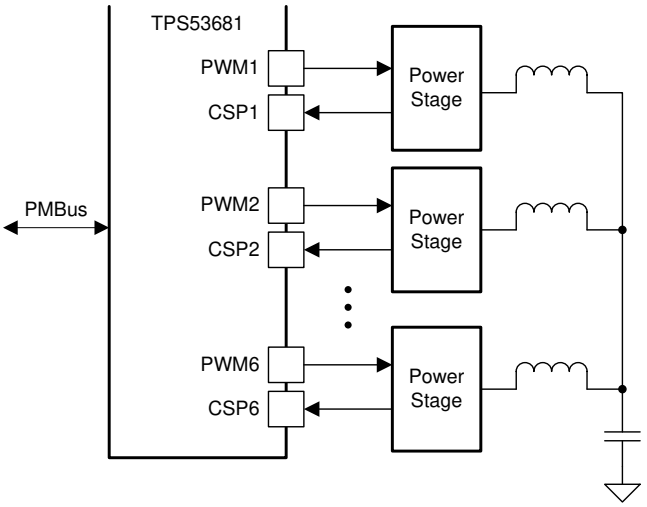
TPS53681は放熱特性に優れた40ピンQFNパッケージで供給され、–40°C～125°Cの温度範囲で仕様が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
TPS53681	QFN (40)	5mm×5mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

図 1. アプリケーション概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (November 2018) から Revision B に変更 **Page**

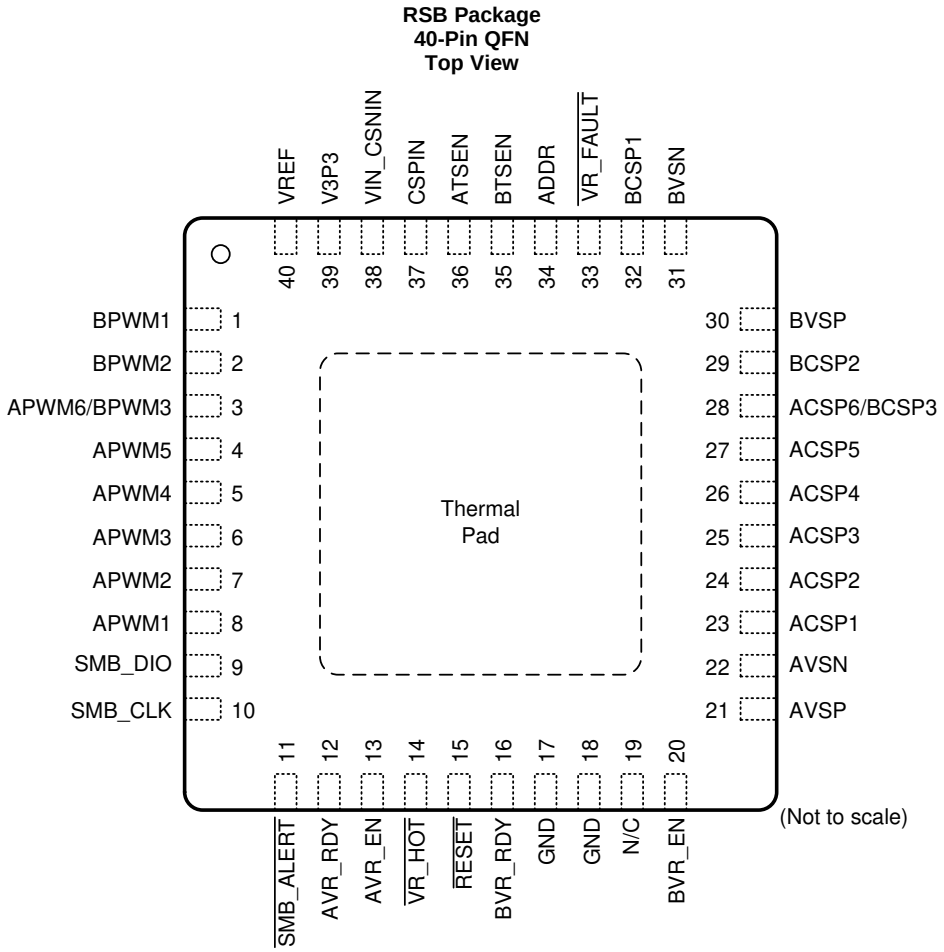
- Updated the device NVM default values in Supported Commands ... 45

2017年6月発行のものから更新 **Page**

- 「アプリケーション」項目を更新 ... 1
- 追加 (21h) VOUT_COMMAND register table in *Output Voltage Margin Testing* section ... 67

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5 Pin Configuration and Functions



Thermal pad acts as AGND.

NC = not connected

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ACSP1	23	I	Current sense input for the channel A. Connect to the IOUT pin of TI smart power stages. Tie the ACSP5, ACSP4, ACSP3, or ACSP2 pin to the V3P3 pin according to Table 1 to disable the corresponding phase.
ACSP2	24		
ACSP3	25		
ACSP4	26		
ACSP5	27		
ACSP6/BCSP3	28		Current sense inputs for channel A or channel B based on NVM option. Connect to the IOUT pin of smart power stages. Tie ACSP6/BCSP3 to the 3.3-V supply to disable corresponding phase.
ADDR	34	I	Voltage divider to VREF and GND. The voltage level sets the 7-bit PMBus address with an ADC. Address is latched at 3.3-V power up.
APWM1	8	O	PWM signal for phase 1 of channel A.
APWM2	7	O	PWM signal for phase 2 of channel A.
APWM3	6	O	PWM signal for phase 3 of channel A.
APWM4	5	O	PWM signal for phase 4 of channel A.
APWM5	4	O	PWM signal for phase 5 of channel A.

(1) G = ground, I = input, O = output, P = power input

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Pin Functions (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
APWM6/BPWM3	3	O	PWM signal for phase 6 of channel A, or phase 3 of channel B, based on the NVM option.
ATSEN	36	O	Connect to TAO pin of TI smart power stages of Channel A to sense the highest temperature of the power stages and to sense the built-in fault signal from power stages
AVR_EN	13	I	Active high enable input for channel A. Asserting the AVR_EN pin activates channel A. Re-cycling BVR_EN pin clears the faults of channel A.
AVR_RDY	12	O	Power good open-drain output signal of channel A. This open drain output requires an external pull-up resistor. The AVR_RDY pin is pulled low when a shutdown fault occurs.
AVSN	22	I	Negative input of the remote voltage sense of channel A.
AVSP	21	I	Positive input of the remote voltage sense of channel A.
BCSP1	32	I	Current sense input for channel B. Connect to the IOUT pins of TI smart power stages. If channel B is not used, then connect the BCSP1 pin to GND.
BCSP2	29	I	Current sense input for channel B. Connect to the IOUT pins of TI smart power stages. Tie the BCSP2 pin to the V3P3 pin according to Table 1 to disable the corresponding phase.
BPWM1	1	O	PWM signal for phase 1 of channel B
BPWM2	2	O	PWM signal for phase 2 of channel B
BTSEN	35	O	Connect to TAO pin of TI smart power stages of Channel B to sense the highest temperature of the power stages and to sense the built-in fault signal from power stages
BVR_EN	20	I	Active high enable input for channel B. Asserting the BVR_EN pin activates channel B. Re-cycling BVR_EN pin clears the faults of channel B.
BVR_RDY	16	O	Power good open-drain output signal of channel B. This open drain output requires an external pull-up resistor. BVR_RDY is pulled low when a shutdown fault occurs.
BVSN	31	I	Negative input of the remote voltage sense of channel B. If channel B is not used, connect BVSN to GND.
BVSP	30	I	Positive input of the remote voltage sense of channel B. If channel B is not used, connect BVSP to GND.
CSPIN	37	I	Input voltage from the positive terminal connecting to the input current sensing shunt. When input current sensing is not used, short CSPIN to VIN_CSNIN and connect to the converter input voltage (example: 12 V).
GND	17	G	Connect to GND
	18		
NC	19	–	No connection.
$\overline{\text{RESET}}$	15	I/O	Resets the output voltage to BOOT voltage
$\overline{\text{SMB_ALERT}}$	11	I/O	SMBus or I^2C bi-directional $\overline{\text{ALERT}}$ pin interface. (Open drain)
SMB_CLK	10	I	SMBus or I^2C serial clock interface. (Open drain)
SMB_DIO	9	I/O	SMBus or I^2C bi-directional serial data interface. (Open drain)
V3P3	39	P	3.3-V power input. Bypass to GND with a ceramic capacitor with a value greater than or equal to 1 µF. Used to power all digital logic circuits.
VIN_CSNIN	38	P	Input voltage sensing for on-time control and telemetry. Serves as the negative terminal connecting to the input current sensing shunt. When input current sensing is not used, short VIN_CSNIN to CSPIN and connect to the converter input voltage (example: 12 V).
$\overline{\text{VR_FAULT}}$	33	O	VR fault indicator. (Open-drain). The failures include the high-side FETs short, over-voltage, over-temperature, and the input over-current conditions. Use the fault signal on the platform to remove the power source by turning off the AC power supply. When the failure occurs, the $\overline{\text{VR_FAULT}}$ pin is LOW, and put the controller into latch-off mode. One NVM bit is used to select whether or not the faults from channel B asserts the $\overline{\text{VR_FAULT}}$. pin.
VREF	40	O	1.7-V LDO reference voltage. Bypass to GND with 1-µF ceramic capacitor. Connect the VREF pin to the REFIN pin of the TI smart power stages as the current sense common-mode voltage.
$\overline{\text{VR_HOT}}$	14	O	Active low external temperature indicator.
Thermal Pad		G	Analog ground pad. Connect to GND plan with vias.

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Table 1. Current Sense Inputs for Active Phases

Active Phase Channel		ACSP1	ACSP2	ACSP3	ACSP4	ACSP5	ACSP6	BSCP1	BSCP2
A	B								
1	0	AIOUT1	V3P3	n/a	n/a	n/a	n/a	GND	V3P3
2	1	AIOUT1	AIOUT2	V3P3	n/a	n/a	n/a	BIOUT1	V3P3
3	1	AIOUT1	AIOUT2	AIOUT3	V3P3	n/a	n/a	BIOUT1	V3P3
4	1	AIOUT1	AIOUT2	AIOUT3	AIOUT4	V3P3	n/a	BIOUT1	V3P3
5	1	AIOUT1	AIOUT2	AIOUT3	AIOUT4	AIOUT5	V3P3	BIOUT1	V3P3
6	0	AIOUT1	AIOUT2	AIOUT3	AIOUT4	AIOUT5	AIOUT6	GND	V3P3
6 (1)	1	AIOUT1	AIOUT2	AIOUT3	AIOUT4	AIOUT5	AIOUT6	BIOUT1	V3P3
6	2	AIOUT1	AIOUT2	AIOUT3	AIOUT4	AIOUT5	AIOUT6	BIOUT1	BIOUT2
5	2	AIOUT1	AIOUT2	AIOUT3	AIOUT4	AIOUT5	V3P3	BIOUT1	BIOUT2
5 (1)	3	AIOUT1	AIOUT2	AIOUT3	AIOUT4	AIOUT5	BIOUT3	BIOUT1	BIOUT2

(1) For *n*+1 or *n*+3 applications, the NVM setting must be changed. See also the *Phase Configuration for Channel B* section.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage (1) (2)	CSPIN, VIN_CSNIN	–0.3	19	V
	ACSP1, ACSP2, ACSP3, ACSP4, ACSP5, ACSP6/BCSP3, ADDR, ATSEN, AVR_EN, AVSP, BCSP1, BCSP2, BTSEN, BVR_EN, BVSP, $\overline{\text{RESET}}$, SMB_CLK, SMB_DIO, V3P3	–0.3	3.6	V
	AGND, AVSN, BVSN	–0.3	0.3	V
Output voltage (1) (2)	APWM1, APWM2, APWM3, APWM4, APWM5, APWM6/BPWM3, BPWM2, AVR_RDY, BPWM1, BVR_RDY, $\overline{\text{SMB_ALERT}}$, VREF, $\overline{\text{VR_FAULT}}$, $\overline{\text{VR_HOT}}$	–0.3	3.6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal GND unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Input voltage	CSPIN, VIN_CSNIN	4.5	12	17	V
	V3P3	2.97	3.3	3.5	
	ACSP1, ACSP2, ACSP3, ACSP4, ACSP5, ACSP6/BSCP3, ADDR, ATSEN, AVR_EN, AVSP, BCSP1, BCSP2, BTSEN, BVR_EN, BVSP, $\overline{\text{RESET}}$, SMB_CLK, SMB_DIO, V3P3	–0.1		3.5	
	AGND, AVSN, BVSN	–0.1		0.1	
Output voltage	VREF	–0.1		1.72	V
	APWM1, APWM2, APWM3, APWM4, APWM5, APWM6/BPWM3, BPWM2, AVR_RDY, BPWM1, BVR_RDY, $\overline{\text{SMB_ALERT}}$, VREF, $\overline{\text{VR_FAULT}}$, $\overline{\text{VR_HOT}}$	–0.1		3.5	
Ambient temperature, T_A		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		TPS53681 RSB (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Supply: Currents, UVLO, and Power-On Reset

V_{VIN_CSNIN} = 12.0 V, V_{V3P3} = 3.3 V, V_{AVSN} = GND, V_{BVSN} = GND, V_{AVSP} = V_{OUTA}, V_{BVSP} = V_{OUTB} (Unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply: Currents, UVLO, and Power-On Reset						
I_{V3P3}	V3P3 supply current	VDAC < VSP < VDAC + 100m V, ENABLE = 'HI '		13	18	mA
$I_{V3P3SBY}$	V3P3 standby current	ENABLE = 'LO '		9	13.5	mA
$V_{3NORMAL}$	V3P3 normal range	Normal operation	2.97		3.5	V
V_{3UVLOH}	V3P3 UVLO 'OK ' threshold	Ramp up	2.85		2.95	V
V_{3UVLOL}	V3P3 UVLO fault threshold	Ramp down	2.65		2.75	V
V_{12ON}	V12 UVLO 'OK ' threshold	VIN_ON = 0xF010	3.75	4	4.25	V
		VIN_ON = 0xF015	5	5.25	5.5	V
		VIN_ON = 0xF019	6	6.25	6.5	V
		VIN_ON = 0xF01D	7	7.25	7.5	V
		VIN_ON = 0xF021	8	8.25	8.5	V
		VIN_ON = 0xF025	9	9.25	9.5	V
		VIN_ON = 0xF029	10	10.25	10.5	V
		VIN_ON = 0xF02D	11	11.25	11.5	V
		VIN_ON = others		invalid		
V_{12UVF}	V12 UVLO fault threshold	VIN_UV_FAULT_LIMIT = 0xF011	4	4.25	4.48	V
		VIN_UV_FAULT_LIMIT = 0xF80B	5.25	5.5	5.78	V
		VIN_UV_FAULT_LIMIT = 0xF80D	6.25	6.5	6.78	V
		VIN_UV_FAULT_LIMIT = 0xF80F	7.25	7.5	7.78	V
		VIN_UV_FAULT_LIMIT = 0xF811	8.25	8.5	8.78	V
		VIN_UV_FAULT_LIMIT = 0xF813	9.25	9.5	9.78	V
		VIN_UV_FAULT_LIMIT = 0xF815	10.25	10.5	10.78	V
		VIN_UV_FAULT_LIMIT = 0xF817	11.25	11.5	11.8	V
		VIN_UV_FAULT_LIMIT = others		invalid		

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6.6 References: DAC and VREF

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIDSTP}	VID step size	10 mV DAC: Change VID0 HI to LO to HI		10		mV
		5 mV DAC: Change VID0 HI to LO to HI		5		mV
V_{DAC0}	VSP tolerance	10 mV DAC : 0.50 ≤ V_{VSP} ≤ 0.99 V, I_{CORE} = 0 A	–10		10	mV
V_{DAC1}	VSP tolerance	5 mV DAC: 0.25 ≤ V_{VSP} ≤ 0.795 V, I_{CORE} = 0 A	–8		8	mV
		10 mV DAC: 1.00 V ≤ V_{VSP} ≤ 1.49 V, I_{CORE} = 0 A				
V_{DAC2}	VSP tolerance	5 mV DAC: 0.8 ≤ V_{VSP} ≤ 0.995 V, I_{CORE} = 0 A	–5		5	mV
V_{DAC3}	VSP tolerance	5mV DAC: 1.00V ≤ VSP ≤ 1.52 V, I_{CORE} = 0 A	–0.5		0.5	%
		10 mV DAC: 1.50 V ≤ V_{VSP} ≤ 2.50 V, I_{CORE} = 0 A				
V_{VREF}	VREF output deeper sleep	2.97V ≤ V_{V3P3} ≤ 3.5 V, I_{VREF} = 0 A	1.692	1.7	1.708	V
$V_{VREFSRC}$	VREF output source	0 A ≤ I_{VREF} = 2 mA	–8			mV
$V_{VREFSNK}$	VREF output sink	–2 mA ≤ I_{VREF} = 0 A			8	mV
K_{RATIO}	Voltage divider ratio	VOUT_SCALE_LOOP = 0xe809, VOUT_SCALE_MONITOR = 0xe809		1.125		
		VOUT_SCALE_LOOP = 0xe808, VOUT_SCALE_MONITOR = 0xe808		1		
V_{OUT_TRIML}	V_{OUT} offset LSB	MFR_SPECIFIC_05 = 0x01	0	1.25	2.5	mV
V_{OUT_TRIMR}	V_{OUT} offset range	MFR_SPECIFIC_05 = 0x1F	37.5	38.75	40	mV
		MFR_SPECIFIC_05 = 0xA0	–43.25	–40	–37.75	
		MFR_SPECIFIC_05 = 0x5F	56.25	58.75	61.25	
		MFR_SPECIFIC_05 = 0xE0	–63	–60	–57	

6.7 Voltage Sense: AVSP and BVSP, AVSN and BVSN

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{AVSP}	AVSP input bias current	Not in Fault, Disable or UVLO; V_{VSP} = V_{VDAC} = 2.3 V, V_{VSN} = 0 V			75	µA
I_{AVSN}	AVSN input bias current	Not in Fault, Disable or UVLO; V_{VSP} = V_{VDAC} = 2.3 V, V_{VSN} = 0 V	–75			µA
I_{BVSP}	BVSP input bias current	Not in Fault, Disable or UVLO; V_{VSP} = V_{VDAC} = 1.0 V, V_{VSN} = 0 V			75	µA
I_{BVSN}	BVSN input bias current	Not in Fault, Disable or UVLO; V_{VSP} = V_{VDAC} = 1.0 V, V_{VSN} = 0 V	–75			µA

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6.8 Telemetry

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{READ_VOUT}	MFR_READ_VOUT Accuracy	5 mV DAC : 0.25 V ≤ V_{VSP} ≤ 1.52 V 10 mV DAC: 0.5 ≤ V_{VSP} ≤ 2.4 V	–12		12	mV
V_{READ_VIN}	READ_VIN Accuracy	4.50 V ≤ V_{IN} ≤ 17 V	–2.25%		2.25%	
I_{MON_ACC}	Digital current monitor accuracy, Rail A (READ_IOUT)	6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 22.8 A	–7.3%		7.3%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 45.6 A	–4.2%		4.2%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 68.4 A	–3.1%		3.1%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 91.2 A	–2.5%		2.5%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 114 A	–2.3%		2.3%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 136.8 A	–2%		2%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 228 A	–1.6%		1.6%	
		6-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 255 A	–1.5%		1.5%	
I_{MON_ACC}	Digital current monitor accuracy, Rail A (READ_IOUT)	5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 22.8 A	–6.4%		6.4%	
		5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 45.6 A	–3.7%		3.7%	
		5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 68.4 A	–2.9%		2.9%	
		5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 91.2 A	–2.3%		2.3%	
		5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 114 A	–2.1%		2.1%	
		5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 136.8 A	–1.9%		1.9%	
		5-phase, $I_{CC(max)}$ = 228 A, I_{OUT} = 228 A	–1.5%		1.5%	
I_{MON_ACC}	Digital current monitor accuracy, Rail A (READ_IOUT)	4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 20 A	–6.5%		6.5%	
		4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 40 A	–3.7%		3.7%	
		4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 60 A	–2.8%		2.8%	
		4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 80 A	–2.3%		2.3%	
		4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 100 A	–2.1%		2.1%	
		4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 120 A	–1.9%		1.9%	
		4-phase, $I_{CC(max)}$ = 200 A, I_{OUT} = 200 A	–1.5%		1.5%	
I_{MON_ACC}	Digital current monitor accuracy, Rail B (READ_IOUT)	3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 8.2 A	–11.4%		11.4%	
		3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 16.4 A	–6.1%		6.1%	
		3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 24.6 A	–4.6%		4.6%	
		3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 32.8 A	–3.4%		3.4%	
		3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 41 A	–3%		3%	
		3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 49.2 A	–2.8%		2.8%	
		3-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 82 A	–2%		2%	
I_{MON_ACC}	Digital current monitor accuracy, Rail B (READ_IOUT)	2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 8.2 A	–8.7%		8.7%	
		2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 16.4 A	–4.7%		4.7%	
		2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 24.6 A	–3.7%		3.7%	
		2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 32.8 A	–2.7%		2.7%	
		2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 41 A	–2.5%		2.5%	
		2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 49.2 A	–2.4%		2.4%	
		2-phase, $I_{CC(max)}$ = 82 A, I_{OUT} = 82 A	–1.8%		1.8%	
Temp	READ_TEMP1	0.28 V (–40°C) ≤ TSEN ≤ 1.8 V (150°C)	–2	0	2	°C

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6.9 Input Current Sensing

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	READ_IIN accuracy	$(V_{CSPIN} – V_{CSNIN})$ = 2.5 mV, I_{IN} = 5 A, R_{SENSE} = 0.5 mΩ	–10%		10%	
		$(V_{CSPIN} – V_{CSNIN})$ = 5 mV, I_{IN} = 10 A, R_{SENSE} = 0.5 mΩ	–6%		6%	
		$(V_{CSPIN} – V_{CSNIN})$ = 15 mV, I_{IN} = 30 A, R_{SENSE} = 0.5 mΩ	–3%		3%	

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6.10 Programmable Loadline Settings

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DCLL_{Channel\ A}$	DC loadline settings for Channel A	VOUT_DROOP = 0xD000		0		mΩ
		VOUT_DROOP = 0xD008	0.1125	0.125	0.1395	mΩ
		VOUT_DROOP = 0xD010	0.2412	0.25	0.2587	mΩ
		VOUT_DROOP = 0xD014	0.3031	0.3125	0.3218	mΩ
		VOUT_DROOP = 0xD018	0.3637	0.375	0.3872	mΩ
		VOUT_DROOP = 0xD01C	0.4265	0.4375	0.4484	mΩ
		VOUT_DROOP = 0xD020	0.4875	0.5	0.5125	mΩ
		VOUT_DROOP = 0xD024	0.5484	0.5625	0.5765	mΩ
		VOUT_DROOP = 0xD028	0.6093	0.625	0.6406	mΩ
		VOUT_DROOP = 0xD030	0.6855	0.7031	0.7207	mΩ
		VOUT_DROOP = 0xD033	0.7769	0.7969	0.8168	mΩ
		VOUT_DROOP = 0xD034	0.7921	0.8125	0.8328	mΩ
		VOUT_DROOP = 0xD035	0.8073	0.8281	0.8488	mΩ
		VOUT_DROOP = 0xD036	0.8227	0.8438	0.8648	mΩ
		VOUT_DROOP = 0xD037	0.8379	0.8594	0.8808	mΩ
		VOUT_DROOP = 0xD038	0.8531	0.875	0.8968	mΩ
		VOUT_DROOP = 0xD039	0.8683	0.8906	0.9128	mΩ
		VOUT_DROOP = 0xD03A	0.8836	0.9063	0.9289	mΩ
		VOUT_DROOP = 0xD03B	0.8988	0.9219	0.9449	mΩ
		VOUT_DROOP = 0xD03C	0.9140	0.9375	0.9609	mΩ
		VOUT_DROOP = 0xD03D	0.9292	0.9531	0.9769	mΩ
		VOUT_DROOP = 0xD03E	0.9445	0.9688	0.9930	mΩ
		VOUT_DROOP = 0xD03F	0.9597	0.9844	1.0090	mΩ
		VOUT_DROOP = 0xD040	0.975	1	1.025	mΩ
		VOUT_DROOP = 0xD041	0.9902	1.0156	1.0409	mΩ
		VOUT_DROOP = 0xD042	1.0055	1.0313	1.0570	mΩ
		VOUT_DROOP = 0xD043	1.0207	1.0469	1.0730	mΩ
		VOUT_DROOP = 0xD044	1.0359	1.0625	1.0890	mΩ
		VOUT_DROOP = 0xD048	1.0968	1.125	1.1531	mΩ
		VOUT_DROOP = 0xD050	1.2187	1.25	1.2812	mΩ
		VOUT_DROOP = 0xD058	1.3406	1.375	1.4093	mΩ
		VOUT_DROOP = 0xD060	1.4625	1.5	1.5375	mΩ
		VOUT_DROOP = 0xD068	1.5843	1.625	1.6656	mΩ
		VOUT_DROOP = 0xD070	1.7062	1.75	1.7937	mΩ
		VOUT_DROOP = 0xD078	1.8281	1.875	1.9218	mΩ
		VOUT_DROOP = 0xD07C	1.8890	1.9375	1.9859	mΩ
		VOUT_DROOP = 0xD080	1.95	2	2.05	mΩ
		VOUT_DROOP = 0xD084	2.0109	2.0625	2.1141	mΩ
		VOUT_DROOP = 0xD088	2.0718	2.125	2.1781	mΩ
		VOUT_DROOP = 0xD08C	2.1328	2.1875	2.2421	mΩ
		VOUT_DROOP = 0xD090	2.1937	2.25	2.3062	mΩ
		VOUT_DROOP = 0xD098	2.2698	2.328	2.3862	mΩ
		VOUT_DROOP = 0xD09B	2.3612	2.4218	2.4823	mΩ
		VOUT_DROOP = 0xD09C	2.3765	2.4375	2.4984	mΩ

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Programmable Loadline Settings (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DCLL_{Channel\ A}$	DC loadline settings for Channel A	VOUT_DROOP = 0xD09D	2.3917	2.4531	2.5144	mΩ
		VOUT_DROOP = 0xD09E	2.4069	2.4687	2.5304	mΩ
		VOUT_DROOP = 0xD09F	2.4221	2.4843	2.5464	mΩ
		VOUT_DROOP = 0xD0A0	2.4375	2.5	2.5625	mΩ
		VOUT_DROOP = 0xD0A1	2.4527	2.5156	2.5784	mΩ
		VOUT_DROOP = 0xD0A2	2.4679	2.5312	2.5944	mΩ
		VOUT_DROOP = 0xD0A3	2.4831	2.5468	2.6104	mΩ
		VOUT_DROOP = 0xD0A4	2.4984	2.5625	2.6265	mΩ
		VOUT_DROOP = 0xD0A5	2.5136	2.5781	2.6425	mΩ
		VOUT_DROOP = 0xD0A6	2.5288	2.5937	2.6585	mΩ
		VOUT_DROOP = 0xD0A7	2.5437	2.609	2.6742	mΩ
		VOUT_DROOP = 0xD0A8	2.5593	2.625	2.6906	mΩ
		VOUT_DROOP = 0xD0A9	2.5745	2.6406	2.7066	mΩ
		VOUT_DROOP = 0xD0AA	2.5897	2.6562	2.7226	mΩ
		VOUT_DROOP = 0xD0AB	2.6050	2.6718	2.7385	mΩ
		VOUT_DROOP = 0xD0AC	2.6203	2.6875	2.7546	mΩ
		VOUT_DROOP = 0xD0B0	2.6812	2.75	2.8187	mΩ
		VOUT_DROOP = 0xD0B8	2.8031	2.875	2.9468	mΩ
		VOUT_DROOP = 0xD0C0	2.925	3	3.075	mΩ
		VOUT_DROOP = 0xD0C8	3.0468	3.125	3.2031	mΩ
$DCLL_{Channel\ B}$	DC Loadline settings for Channel B	VOUT_DROOP = 0xD000		0		mΩ
		VOUT_DROOP = 0xD008	0.1125	0.125	0.1395	mΩ
		VOUT_DROOP = 0xD010	0.2355	0.25	0.2625	mΩ
		VOUT_DROOP = 0xD014	0.297	0.3125	0.3234	mΩ
		VOUT_DROOP = 0xD018	0.3637	0.375	0.395	mΩ
		VOUT_DROOP = 0xD01C	0.4244	0.4375	0.454	mΩ
		VOUT_DROOP = 0xD020	0.4875	0.5	0.517	mΩ
		VOUT_DROOP = 0xD024	0.5464	0.5625	0.5786	mΩ
		VOUT_DROOP = 0xD028	0.6093	0.625	0.648	mΩ
		VOUT_DROOP = 0xD030	0.6855	0.7031	0.7207	mΩ
		VOUT_DROOP = 0xD033	0.7769	0.7969	0.8168	mΩ
		VOUT_DROOP = 0xD034	0.7921	0.8125	0.8335	mΩ
		VOUT_DROOP = 0xD035	0.8073	0.8281	0.852	mΩ
		VOUT_DROOP = 0xD036	0.8227	0.8438	0.8648	mΩ
		VOUT_DROOP = 0xD037	0.8379	0.8594	0.8815	mΩ
		VOUT_DROOP = 0xD038	0.8531	0.875	0.8968	mΩ

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Programmable Loadline Settings (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACLL	AC Loadline settings for both Channel A and Channel B(1)	MFR_SPECIFIC_07 = 0x00		0		mΩ
		MFR_SPECIFIC_07 = 0x01	0.1125	0.125	0.1395	mΩ
		MFR_SPECIFIC_07 = 0x02	0.2412	0.25	0.2587	mΩ
		MFR_SPECIFIC_07 = 0x03	0.3031	0.3125	0.3218	mΩ
		MFR_SPECIFIC_07 = 0x04	0.3637	0.375	0.3862	mΩ
		MFR_SPECIFIC_07 = 0x05	0.4265	0.4375	0.4484	mΩ
		MFR_SPECIFIC_07 = 0x06	0.4875	0.5	0.5125	mΩ
		MFR_SPECIFIC_07 = 0x07	0.5484	0.5625	0.5765	mΩ
		MFR_SPECIFIC_07 = 0x08	0.6093	0.625	0.6406	mΩ
		MFR_SPECIFIC_07 = 0x09	0.7312	0.75	0.7687	mΩ
		MFR_SPECIFIC_07 = 0x0A	0.7769	0.7969	0.8168	mΩ
		MFR_SPECIFIC_07 = 0x0B	0.7921	0.8125	0.8328	mΩ
		MFR_SPECIFIC_07 = 0x0C	0.8073	0.8281	0.8488	mΩ
		MFR_SPECIFIC_07 = 0x0D	0.8227	0.8438	0.8648	mΩ
		MFR_SPECIFIC_07 = 0x0E	0.8379	0.8594	0.8808	mΩ
		MFR_SPECIFIC_07 = 0x0F	0.8531	0.875	0.8968	mΩ
		MFR_SPECIFIC_07 = 0x10	0.8683	0.8906	0.9128	mΩ
		MFR_SPECIFIC_07 = 0x11	0.8836	0.9063	0.9289	mΩ
		MFR_SPECIFIC_07 = 0x12	0.8988	0.9219	0.9449	mΩ
		MFR_SPECIFIC_07 = 0x13	0.9140	0.9375	0.9609	mΩ
		MFR_SPECIFIC_07 = 0x14	0.9292	0.9531	0.9769	mΩ
		MFR_SPECIFIC_07 = 0x15	0.9445	0.9688	0.9930	mΩ
		MFR_SPECIFIC_07 = 0x16	0.9597	0.9844	1.0090	mΩ
		MFR_SPECIFIC_07 = 0x17	0.975	1	1.025	mΩ
		MFR_SPECIFIC_07 = 0x18	0.9902	1.0156	1.0409	mΩ
		MFR_SPECIFIC_07 = 0x19	1.0055	1.0313	1.0570	mΩ
		MFR_SPECIFIC_07 = 0x1A	1.0207	1.0469	1.0730	mΩ
		MFR_SPECIFIC_07 = 0x1B	1.0359	1.0625	1.0890	mΩ
		MFR_SPECIFIC_07 = 0x1C	1.0968	1.125	1.1531	mΩ
		MFR_SPECIFIC_07 = 0x1D	1.2187	1.25	1.2812	mΩ
		MFR_SPECIFIC_07 = 0x1E	1.3406	1.375	1.4093	mΩ
		MFR_SPECIFIC_07 = 0x1F	1.4625	1.5	1.5375	mΩ
		MFR_SPECIFIC_07 = 0x20	1.5843	1.625	1.6656	mΩ
		MFR_SPECIFIC_07 = 0x21	1.7062	1.75	1.7937	mΩ
		MFR_SPECIFIC_07 = 0x22	1.8281	1.875	1.9218	mΩ
		MFR_SPECIFIC_07 = 0x23	1.8890	1.9375	1.9859	mΩ
		MFR_SPECIFIC_07 = 0x24	1.95	2	2.05	mΩ
		MFR_SPECIFIC_07 = 0x25	2.0109	2.0625	2.1140	mΩ
		MFR_SPECIFIC_07 = 0x26	2.0718	2.125	2.1781	mΩ
		MFR_SPECIFIC_07 = 0x27	2.1328	2.1875	2.2421	mΩ
		MFR_SPECIFIC_07 = 0x28	2.1937	2.25	2.3062	mΩ
		MFR_SPECIFIC_07 = 0x29	2.3156	2.375	2.4343	mΩ
		MFR_SPECIFIC_07 = 0x2A	2.3612	2.4218	2.4823	mΩ
		MFR_SPECIFIC_07 = 0x2B	2.3765	2.4375	2.4984	mΩ

(1) Specified by design. Not production tested.

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Programmable Loadline Settings (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACLL	AC Loadline settings for both Channel A and Channel B(1)	MFR_SPECIFIC_07 = 0x2C	2.3917	2.4531	2.5144	mΩ
		MFR_SPECIFIC_07 = 0x2D	2.4069	2.4687	2.5304	mΩ
		MFR_SPECIFIC_07 = 0x2E	2.4221	2.4843	2.5464	mΩ
		MFR_SPECIFIC_07 = 0x2F	2.4375	2.5	2.5625	mΩ
		MFR_SPECIFIC_07 = 0x30	2.4527	2.5156	2.5784	mΩ
		MFR_SPECIFIC_07 = 0x31	2.4679	2.5312	2.5944	mΩ
		MFR_SPECIFIC_07 = 0x32	2.4831	2.5468	2.6104	mΩ
		MFR_SPECIFIC_07 = 0x33	2.4984	2.5625	2.6265	mΩ
		MFR_SPECIFIC_07 = 0x34	2.5136	2.5781	2.6425	mΩ
		MFR_SPECIFIC_07 = 0x35	2.5288	2.5937	2.6585	mΩ
		MFR_SPECIFIC_07 = 0x36	2.5437	2.609	2.6742	mΩ
		MFR_SPECIFIC_07 = 0x37	2.5593	2.625	2.6906	mΩ
		MFR_SPECIFIC_07 = 0x38	2.5745	2.6406	2.7066	mΩ
		MFR_SPECIFIC_07 = 0x39	2.5897	2.6562	2.7226	mΩ
		MFR_SPECIFIC_07 = 0x3A	2.6050	2.6718	2.7385	mΩ
		MFR_SPECIFIC_07 = 0x3B	2.6203	2.6875	2.7546	mΩ
		MFR_SPECIFIC_07 = 0x3C	2.6812	2.75	2.8187	mΩ
		MFR_SPECIFIC_07 = 0x3D	2.8031	2.875	2.9468	mΩ
		MFR_SPECIFIC_07 = 0x3E	2.925	3	3.075	mΩ
		MFR_SPECIFIC_07 = 0x3F	3.0468	3.125	3.2031	mΩ
t_{INT}	Integration time constant(1)	MFR_SPEC_7<11:8> = 0000b		5		µs
		MFR_SPEC_7<11:8> = 0001b		10		µs
		MFR_SPEC_7<11:8> = 0010b		15		µs
		MFR_SPEC_7<11:8> = 0011b		20		µs
		MFR_SPEC_7<11:8> = 0100b		25		µs
		MFR_SPEC_7<11:8> = 0101b		30		µs
		MFR_SPEC_7<11:8> = 0110b		35		µs
		MFR_SPEC_7<11:8> = 0111b		40		µs
		MFR_SPEC_7<11:8> = 1000b		1		µs
		MFR_SPEC_7<11:8> = 1001b		2		µs
		MFR_SPEC_7<11:8> = 1010b		3		µs
		MFR_SPEC_7<11:8> = 1011b		4		µs
		MFR_SPEC_7<11:8> = 1100b		5		µs
		MFR_SPEC_7<11:8> = 1101b		6		µs
		MFR_SPEC_7<11:8> = 1110b		7		µs
		MFR_SPEC_7<11:8> = 1111b		8		µs

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6.11 Current Sense and Calibration

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ACSP1}	ACSP1 leakage current	V_{ACSP1} = 2.5 V	0		20	µA
I_{ACSP2}	ACSP2 leakage current	V_{ACSP2} = 2.5 V	0		20	µA
I_{ACSP3}	ACSP3 leakage current	V_{ACSP3} = 2.5 V	0		20	µA
I_{ACSP4}	ACSP4 leakage current	V_{ACSP4} = 2.5 V	0		20	µA
I_{ACSP5}	ACSP5 leakage current	V_{ACSP5} = 2.5 V	0		20	µA
I_{ACSP6}	ACSP6 leakage current	V_{ACSP6} = 2.5 V	0		20	µA
I_{BCSP1}	BCSP1 leakage current	V_{BCSP1} = 2.5 V	0		20	µA
I_{BCSP2}	BCSP2 leakage current	V_{BCSP2} = 2.5 V	0		20	µA
$I_{MON_CAL_OF1}$	Current monitor calibration offset LSB (per-phase)(1)	IOUT_CAL_OFFSET resolution (per-phase)		0.125		A
$I_{MON_CAL_OF2}$	Current monitor calibration offset range (per-phase)	IOUT_CAL_OFFSET = 0xE808 (per-phase)		1		A
		IOUT_CAL_OFFSET = 0xEFF9 (per-phase)		–0.875		A
$I_{MON_CAL_OF3}$	Current monitor calibration offset LSB (total)(1)	IOUT_CAL_OFFSET resolution (total)		0.25		A
$I_{MON_CAL_OF4}$	Current monitor calibration offset range (total)	IOUT_CAL_OFFSET = 0xE820 (total)		4		A
		IOUT_CAL_OFFSET = 0xEFE2 (total)		–3.75		A
$I_{MON_CAL_GA_LSB}$	Current monitor calibration gain LSB(1)	IOUT_CAL_GAIN resolution		0.3125%		
$I_{MON_CAL_GA_RNG}$	Current monitor calibration gain range	IOUT_CAL_GAIN = 0xD131		4.7656		mΩ
		IOUT_CAL_GAIN = 0xD150		5.25		mΩ

(1) Specified by design. Not production tested.

6.12 Logic Interface Pins: AVR_EN, AVR_RDY, BVR_EN, BVR_RDY, $\overline{\text{RESET}}$, $\overline{\text{VR_FAULT}}$, $\overline{\text{VR_HOT}}$

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{RPGDL}	Open-drain pulldown resistance	V_{AVR_RDY} = V_{BVR_RDY} = $V_{\overline{VR_FAULT}}$ = 0.45 V		36	50	Ω
I_{VRTTLK}	Open-drain leakage current	SDIO, $\overline{\text{VR_HOT}}$, AVR_RDY, BVR_RDY, $\overline{\text{VR_FAULT}}$, Hi Z Leakage, apply to 3.3-V supply in off state	–2	0.2	2	µA
V_{AENL}	Channel A ENABLE logic low				0.7	V
V_{AENH}	Channel A ENABLE logic high		0.8			V
V_{AENHYS}	Channel A ENABLE hysteresis		0.028	0.05	0.07	V
t_{AENDIG}	Channel A ENABLE deglitch(1)		0.2			µs
I_{AENH}	Channel A I/O 1.1-V leakage	V_{AVR_EN} = 1.1 V			25	µA
V_{BENL}	Channel B ENABLE logic low				0.7	V
V_{BENH}	Channel B ENABLE logic high		0.8			V
V_{BENHYS}	Channel B ENABLE hysteresis		0.028	0.05	0.07	V
t_{BENDIG}	Channel B ENABLE deglitch(1)		0.2			µs
$t_{AENVRRDYF}$	Channel A ENABLE low to AVR_RDY low	From AVR_EN low to AVR_RDY low			1.5	µs
I_{BENH}	Channel B I/O 1.1-V leakage	V_{BENH} = 1.1 V			25	µA
V_{RSTL}	$\overline{\text{RESET}}$ logic low				0.8	V
V_{RSTH}	$\overline{\text{RESET}}$ logic high(1)		1.09			V
$t_{RSTTDLY}$	$\overline{\text{RESET}}$ delay time			1		µs

(1) Specified by design. Not production tested.

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6.13 I/O Timing

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{STARTUPA}$	Channel A startup time(1)	V_{VBOOT} > 0 V, no faults, C_{REF} = 1 µF, TON_DELAY = 0xB1EC (PAGE 0)	0.38	0.48	0.58	ms
		TON_DELAY = 0xB396 (PAGE 0)	0.8	0.9	1	ms
		TON_DELAY = 0xBAD1 (PAGE 0)	1.308	1.408	1.508	ms
		TON_DELAY = 0xC26E (PAGE 0)	2.28	2.432	2.584	ms
		TON_DELAY = others		Invalid		
$t_{STARTUPB}$	Channel B startup time(2)	V_{VBOOT} > 0 V, no faults, C_{REF} = 1 µF, TON_DELAY = 0xB1EC (PAGE 1)	0.38	0.48	0.58	ms
		TON_DELAY = 0xB396 (PAGE 1)	0.8	0.9	1	ms
		TON_DELAY = 0xBAD1 (PAGE 1)	1.308	1.408	1.508	ms
		TON_DELAY = 0xC26E (PAGE 1)	2.28	2.432	2.584	ms
		TON_DELAY = others		Invalid		
t_{VCCVID}	VID change to VSP change (3)	ACK of SetVID_x command to start of voltage ramp			500	ns
$t_{VRTDGLT}$	$\overline{VR_HOT}$ update time	Temperature data update time		0.3	0.5	ms
t_{ON_BLANK}	Rising-edge blanking time (3)	MFR_SPEC_09<8:6> = 000b	53	72	92	ns
		MFR_SPEC_09<8:6> = 001b	58	78	98	ns
		MFR_SPEC_09<8:6> = 010b	66	86	108	ns
		MFR_SPEC_09<8:6> = 011b	70	92	114	ns
		MFR_SPEC_09<8:6> = 100b	78	100	125	ns
		MFR_SPEC_09<8:6> = 101b	82	108	132	ns
		MFR_SPEC_09<8:6> = 110b	88	114	139	ns
		MFR_SPEC_09<8:6> = 111b	91	120	145	ns

(1) Time from AVR_EN to output voltage ramp up to target voltage.
(2) Time from AVR_EN or BVR_EN to output voltage ramp up to target voltage.
(3) Specified by design. Not production tested.

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6.14 PMBus Address Setting

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{ADDR}	PMBus address bits (7-bit format)	V_{ADDR} ≤ 0.039 V		1011000 (B0h)		Bin
		V_{ADDR} = 0.073 V with ±15 mV tolerance		1011001 (B2h)		Bin
		V_{ADDR} = 0.122 V with ±15 mV tolerance		1011010 (B4h)		Bin
		V_{ADDR} = 0.171 V with ±15 mV tolerance		1011011 (B6h)		Bin
		V_{ADDR} = 0.219 V with ±15 mV tolerance		1011100 (B8h)		Bin
		V_{ADDR} = 0.268 V with ±15 mV tolerance		1011101 (BAh)		Bin
		V_{ADDR} = 0.317 V with ±15 mV tolerance		1011110 (BCh)		Bin
		V_{ADDR} = 0.366 V with ±15 mV tolerance		1011111 (BEh)		Bin
		V_{ADDR} = 0.415 V with ±15 mV tolerance		1100000 (C0h)		Bin
		V_{ADDR} = 0.464 V with ±15 mV tolerance		1100001 (C2h)		Bin
		V_{ADDR} = 0.513 V with ±15 mV tolerance		1100010 (C4h)		Bin
		V_{ADDR} = 0.562 V with ±15 mV tolerance		1100011 (C6h)		Bin
		V_{ADDR} = 0.610 V with ±15 mV tolerance		1100100 (C8h)		Bin
		V_{ADDR} = 0.660 V with ±15 mV tolerance		1100101 (CAh)		Bin
		V_{ADDR} = 0.708 V with ±15 mV tolerance		1100110 (CCh)		Bin
		V_{ADDR} = 0.757 V with ±15 mV tolerance		1100111 (CEh)		Bin
		V_{ADDR} = 0.806 V with ±15 mV tolerance		1101000 (D0h)		Bin
		V_{ADDR} = 0.854 V with ±15 mV tolerance		1101001 (D2h)		Bin
		V_{ADDR} = 0.903 V with ±15 mV tolerance		1101010 (D4h)		Bin
		V_{ADDR} = 0.952 V with ±15 mV tolerance		1101011 (D6h)		Bin
		V_{ADDR} = 1.000 V with ±15 mV tolerance		1101100 (D8h)		Bin
		V_{ADDR} = 1.050 V with ±15 mV tolerance		1101101 (DAh)		Bin
		V_{ADDR} = 1.098 V with ±15 mV tolerance		1101110 (DCh)		Bin
		V_{ADDR} = 1.147 V with ±15 mV tolerance		1101111 (DEh)		Bin
		V_{ADDR} = 1.196 V with ±15 mV tolerance		1110000 (E0h)		Bin
		V_{ADDR} = 1.245 V with ±15 mV tolerance		1110001 (E2h)		Bin
		V_{ADDR} = 1.294 V with ±15 mV tolerance		1110010 (E4h)		Bin
		V_{ADDR} = 1.343 V with ±15 mV tolerance		1110011 (E6h)		Bin
		V_{ADDR} = 1.392 V with ±15 mV tolerance		1110100 (E8h)		Bin
		V_{ADDR} = 1.440 V with ±15 mV tolerance		1110101 (EAh)		Bin
		V_{ADDR} = 1.489 V with ±15 mV tolerance		1110110 (ECh)		Bin
		V_{ADDR} = 1.540 V with ±15 mV tolerance		1110111 (EEh)		Bin

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6.15 Overcurrent Limit Thresholds

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCLAx}	Phase OCL levels for Channel A (ACSPx-VREF), valley current limit	MFR_SPEC_00<3:0>, (PAGE0) = 0000b	12.5	14.5	16.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0001b	16.5	18.5	20.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0010b	20.5	22.5	24.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0011b	24.5	26.5	28.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0100b	28.5	30.5	32.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0101b	32.5	34.5	36.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0110b	36.5	38.5	40.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0111b	40.5	42.5	44.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1000b	44.5	46.5	48.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1001b	48.5	50.5	52.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1010b	52.5	54.5	56.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1011b	56.5	58.5	60.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1100b	60.5	62.5	64.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1101b	64.5	66.5	68.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1110b	68.5	70.5	72.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1111b	72.5	74.5	76.5	A
I_{OCLBx}	Phase OCL levels for Channel B (BCSPx-VREF), valley current limit	MFR_SPEC_00<3:0>, (PAGE1) = 0000b	12	14	16	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0001b	16	18	20	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0010b	20	22	24	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0011b	24	26	28	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0100b	28	30	32	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0101b	32	34	36	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0110b	36	38	40	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0111b	40	42	44	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1000b	44	46	48	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1001b	48	50	52	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1010b	52	54	56	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1011b	56	58	60	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1100b	60	62	64	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1101b	64	66	68	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1110b	68	70	72	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1111b	72	74	76	A

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6.16 Switching Frequency

V_{IN} = 12 V, V_{AVSP} = 1.0 V, V_{BVSP} = 0.8 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	FREQUENCY_SWITCH = 0x012C	270	300	330	kHz
		FREQUENCY_SWITCH = 0x015E	315	350	385	kHz
		FREQUENCY_SWITCH = 0x0190	360	400	440	kHz
		FREQUENCY_SWITCH = 0x01C2	405	450	495	kHz
		FREQUENCY_SWITCH = 0x01F4	450	500	550	kHz
		FREQUENCY_SWITCH = 0x0226	500	550	600	kHz
		FREQUENCY_SWITCH = 0x0258	540	600	660	kHz
		FREQUENCY_SWITCH = 0x028A	585	650	715	kHz
		FREQUENCY_SWITCH = 0x02BC	630	700	770	kHz
		FREQUENCY_SWITCH = 0x02EE	675	750	825	kHz
		FREQUENCY_SWITCH = 0x0320	720	800	880	kHz
		FREQUENCY_SWITCH = 0x0352	765	850	935	kHz
		FREQUENCY_SWITCH = 0x0384	810	900	990	kHz
		FREQUENCY_SWITCH = 0x03B6	855	950	1045	kHz
		FREQUENCY_SWITCH = 0x03E8	900	1000	1100	kHz
		FREQUENCY_SWITCH = others		Invalid		kHz

6.17 Slew Rate Settings

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SL_{SET}	Slew rate setting	VOUT_TRANSITION_RATE = 0xE050	5	6	7	mV/µs
		VOUT_TRANSITION_RATE = 0xE0A0	10	12	14	mV/µs
		VOUT_TRANSITION_RATE = 0xE0F0	15	18		mV/µs
		VOUT_TRANSITION_RATE = 0xE140	20	24		mV/µs
		VOUT_TRANSITION_RATE = 0xE190	25	30		mV/µs
		VOUT_TRANSITION_RATE = 0xE1E0	30	36		mV/µs
		VOUT_TRANSITION_RATE = 0xE230	35	42		mV/µs
		VOUT_TRANSITION_RATE = 0xE280	40	48		mV/µs
		VOUT_TRANSITION_RATE = 0xE005	0.3125			mV/µs
		VOUT_TRANSITION_RATE = 0xE00A	0.625			mV/µs
		VOUT_TRANSITION_RATE = 0xE00F	0.9375			mV/µs
		VOUT_TRANSITION_RATE = 0xE014	1.25			mV/µs
		VOUT_TRANSITION_RATE = 0xE019	1.5625			mV/µs
		VOUT_TRANSITION_RATE = 0xE01E	1.875			mV/µs
		VOUT_TRANSITION_RATE = 0xE023	2.1875			mV/µs
		VOUT_TRANSITION_RATE = 0xE028	2.5			mV/µs
		VOUT_TRANSITION_RATE = others		Invalid data		mV/µs
SL_F	AVSP and BVSP slew rate SetVID_Fast			SL_{SET}		mV/µs
SL_{S1}	AVSP and BVSP slew rate slow			SL_{SET} / 4		mV/µs
				SL_{SET} / 2		mV/µs
SL_{SS}	AVSP and BVSP slew rate slew rate soft-start	MFR_SPEC_13<8> = 0b		SL_{SET} / 4		mV/µs
		MFR_SPEC_13<8> = 1b		SL_{SET} / 16		mV/µs

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6.18 Ramp Selections

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RAMP}	RAMP Setting	MFR_SPEC_14<2:0> = 000b	30	40	55	mV
		MFR_SPEC_14<2:0> = 001b	70	80	95	mV
		MFR_SPEC_14<2:0> = 010b	110	120	135	mV
		MFR_SPEC_14<2:0> = 011b	150	160	175	mV
		MFR_SPEC_14<2:0> = 100b	190	200	215	mV
		MFR_SPEC_14<2:0> = 101b	230	240	255	mV
		MFR_SPEC_14<2:0> = 110b	270	280	300	mV
		MFR_SPEC_14<2:0> = 111b	305	320	335	mV

6.19 Dynamic Integration and Undershoot Reduction

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DYN}	Dynamic integration voltage setting	MFR_SPEC_12<10:8> = 000b;	90	100	116	mV
		MFR_SPEC_12<10:8> = 001b;	135	150	175	mV
		MFR_SPEC_12<10:8> = 010b;	175	200	230	mV
		MFR_SPEC_12<10:8> = 011b;	225	250	285	mV
		MFR_SPEC_12<10:8> = 100b;	270	300	345	mV
		MFR_SPEC_12<10:8> = 101b;	315	350	400	mV
		MFR_SPEC_12<10:8> = 110b;	360	400	455	mV
		MFR_SPEC_12<10:8> = 111b;		OFF		mV
t_{DINT}	Dynamic integration time constant(1)	MFR_SPEC_12<7:4> = 0000b;		1		µs
		MFR_SPEC_12<7:4> = 0001b;		2		µs
		MFR_SPEC_12<7:4> = 0010b;		3		µs
		MFR_SPEC_12<7:4> = 0011b;		4		µs
		MFR_SPEC_12<7:4> = 0100b;		5		µs
		MFR_SPEC_12<7:4> = 0101b;		6		µs
		MFR_SPEC_12<7:4> = 0110b;		7		µs
		MFR_SPEC_12<7:4> = 0111b;		8		µs
		MFR_SPEC_12<7:4> = 1000b;		12		µs
		MFR_SPEC_12<7:4> = 1001b;		13		µs
		MFR_SPEC_12<7:4> = 1010b;		14		µs
		MFR_SPEC_12<7:4> = 1011b;		15		µs
		MFR_SPEC_12<7:4> = 1100b;		16		µs
		MFR_SPEC_12<7:4> = 1101b;		17		µs
		MFR_SPEC_12<7:4> = 1110b;		18		µs
		MFR_SPEC_12<7:4> = 1111b;		19		µs
V_{USR2}	USR level 2 voltage setting	MFR_SPEC_09<14:12> = 000b;	120	140	160	mV
		MFR_SPEC_09<14:12> = 001b;	155	180	205	mV
		MFR_SPEC_09<14:12> = 010b;	190	220	245	mV
		MFR_SPEC_09<14:12> = 011b;	230	260	290	mV
		MFR_SPEC_09<14:12> = 100b;	265	300	335	mV
		MFR_SPEC_09<14:12> = 101b;	300	340	375	mV
		MFR_SPEC_09<14:12> = 110b;	335	380	420	mV
		MFR_SPEC_09<14:12> = 111b;		OFF		mV

(1) Specified by design. Not production tested.

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Dynamic Integration and Undershoot Reduction (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{USR1}	USR level 1 voltage setting	MFR_SPEC_09<2:0> = 000b;	70	90	110	mV
		MFR_SPEC_09<2:0> = 001b;	100	120	140	mV
		MFR_SPEC_09<2:0> = 010b;	130	150	170	mV
		MFR_SPEC_09<2:0> = 011b;	160	180	205	mV
		MFR_SPEC_09<2:0> = 100b;	185	210	240	mV
		MFR_SPEC_09<2:0> = 101b;	215	240	270	mV
		MFR_SPEC_09<2:0> = 110b;	240	270	305	mV
		MFR_SPEC_09<2:0> = 111b;		OFF		mV
PH_{USR1}	Maximum phase added in USR level 1 (1)	MFR_SPEC_09<5> = 0b;		3		phases
		MFR_SPEC_09<5> = 1b;		4		phases
$V_{OUSRHYS}$	Dynamic integration/USR voltage hysteresis	MFR_SPEC_09<4:3> = 00b;	2	5	9	mV
		MFR_SPEC_09<4:3> = 01b;	5	10	15	mV
		MFR_SPEC_09<4:3> = 10b;	10	15	20	mV
		MFR_SPEC_09<4:3> = 11b;	15	20	25	mV

6.20 Boot Voltage and TMAX Settings

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX}	Maximum temperature setting	MFR_SPEC_12<2:0> = 000b		90		°C
		MFR_SPEC_12<2:0> = 001b		95		°C
		MFR_SPEC_12<2:0> = 010b		100		°C
		MFR_SPEC_12<2:0> = 011b		105		°C
		MFR_SPEC_12<2:0> = 100b		110		°C
		MFR_SPEC_12<2:0> = 101b		115		°C
		MFR_SPEC_12<2:0> = 110b		120		°C
		MFR_SPEC_12<2:0> = 111b		125		°C
V_{BOOT}	BOOT voltage setting (10-mV DAC)	MFR_SPEC_11<7:0> = 00h		0		V
		MFR_SPEC_11<7:0> = 74h		1.65		V
		MFR_SPEC_11<7:0> = 79h		1.7		V
		MFR_SPEC_11<7:0> = 7Eh		1.75		V
	BOOT voltage setting (5-mV DAC)	MFR_SPEC_11<7:0> = 00h		0		V
		MFR_SPEC_11<7:0> = 83h		0.9		V
		MFR_SPEC_11<7:0> = 97h		1		V
		MFR_SPEC_11<7:0> = BFh		1.2		V

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6.21 Protections: OVP and UVP

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RDYH5}	Tracking OVP	Measured at the VSP pin wrt VID code. Device latches OFF.	330		400	mV
V_{RDYH0}		Measured at the VSP pin wrt VID code. Device latches OFF.	140		200	mV
$t_{RDYDGLTO}$	VR_RDY deglitch time(1)				(2)2.5	µs
$t_{RDYDGLTU}$	VR_RDY deglitch time(1)	f_{SW} = 500 kHz		4		µs
V_{RDYL}	Undervoltage protection(3)	(V_{VSP} + V_{DROOP}) with respect to VID	370	400	430	mV
V_{OVPA}	Fixed overvoltage protection, Channel A(3)	V_{AVSP} > V_{OVP} for 1 µs, ENABLE = HI or LO, PWM to LO	2.75	2.8	2.86	V
V_{OVPB}	Fixed overvoltage protection, Channel B(3)	V_{BVSP} > V_{OVP} for 1 µs, ENABLE = HI or LO, PWM to LO	1.85	1.9	1.95	V

(1) Specified by design. Not production tested.
(2) Time from VSP out of +200 or +400 mV VDAC boundary to VR_RDY low.
(3) Can be programmed with different configurations.

6.22 Protections: ATSEN and BTSEN Pin Voltage Levels and Fault

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSEN	Thermal voltage definition	V_{TSEN} = 0.28 V	–42	–40	–38	°C
		V_{TSEN} = 0.8 V	23	25	27	°C
		V_{TSEN} = 1.2 V	73	75	77	°C
		V_{TSEN} = 1.4 V	98	100	102	°C
		V_{TSEN} = 1.6 V	123	125	127	°C
		V_{TSEN} = 1.8 V	148	150	152	°C
I_{TSEN}	TSEN leakage current		–3		3	µA

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6.23 PWM: I/O Voltage and Current

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PWML}	PWMx output low-level	I_{LOAD} = 0.5 mA		0.15	0.3	V
V_{PWMH}	PWMx output high-level	I_{LOAD} = –0.5 mA; V_{V3P3} = 2.97 V	2.8			V
$V_{PW-SKLK}$	PWMx tri-state	I_{LOAD} = ± 100 µA	1.6	1.7	1.8	V
t_{P-S_H-L}	PWMx H-L transition time (1)	C_{LOAD} = 10 pF, I_{LOAD} = ± 100 µ A, 10% to 90% both edges			10	ns
t_{P-S_TRI}	PWMx tri-state transition (1)	C_{LOAD} = 10 pF, I_{LOAD} = ± 100 µ A, 10% or 90% to tri-state, both edges			10	ns

(1) Specified by design. Not production tested.

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6.24 Dynamic Phase Add and Drop

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA1}$	Dynamic phase adding threshold, 1 to 2 Phases (Peak Current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	21	23	25	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	23	25	27	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	25	27	29	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	23	25	27	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	25	27	29	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	29	31	33	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	25	27	29	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	29	31	33	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	31	33	35	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	29	31	33	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	31	33	35	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	33	35	37	A

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Dynamic Phase Add and Drop (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS1}$	Dynamic phase shedding threshold, 2 to 1 phase (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	4	6	8	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	6	8	10	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	8	10	12	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	10	12	14	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	6	8	10	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	8	10	12	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	10	12	14	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	12	14	16	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	8	10	12	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	10	12	14	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	12	14	16	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	14	16	18	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	10	12	14	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	12	14	16	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	14	16	18	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	16	18	20	A

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Dynamic Phase Add and Drop (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA2}$	Dynamic phase adding threshold, 2 to 3 phases (Peak Current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	32.5	35	37.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	34.5	37	39.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	36.5	39	41.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	38.5	41	43.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	36.5	39	41.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	38.5	41	43.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	40.5	43	45.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	42.5	45	47.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	40.5	43	45.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	42.5	45	47.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	44.5	47	49.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	46.5	49	51.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	44.5	47	49.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	46.5	49	51.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	48.5	51	53.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	50.5	53	55.5	A

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS2}$	Dynamic phase shedding threshold, 3 to 2 phases (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	17.5	20	22.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	19.5	22	24.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	21.5	24	26.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	23.5	26	28.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	21.5	24	26.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	23.5	26	28.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	25.5	28	30.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	27.5	30	32.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	25.5	28	30.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	27.5	30	32.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	29.5	32	34.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	31.5	34	36.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	29.5	32	34.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	31.5	34	36.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	33.5	36	38.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	35.5	38	40.5	A

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Dynamic Phase Add and Drop (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA3}$	Dynamic phase adding threshold, 3 to 4 Phases (Peak Current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<8:7> = 00b); V_{RIPPLE} = 10 A (estimation)	44	47	50	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<8:7> = 01b); V_{RIPPLE} = 10 A (estimation)	46	49	52	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 10 A; (MFR_SPECIFIC_15<8:7> = 10b); V_{RIPPLE} = 10 A (estimation)	48	51	54	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 12 A; (MFR_SPECIFIC_15<8:7> = 11b); V_{RIPPLE} = 10 A (estimation)	50	53	56	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<8:7> = 00b); V_{RIPPLE} = 10 A (estimation)	50	53	56	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<8:7> = 01b); V_{RIPPLE} = 10 A (estimation)	52	55	58	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 10 A; (MFR_SPECIFIC_15<8:7> = 10b); V_{RIPPLE} = 10 A (estimation)	54	57	60	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 12 A; (MFR_SPECIFIC_15<8:7> = 11b); V_{RIPPLE} = 10 A (estimation)	56	59	62	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<8:7> = 00b); V_{RIPPLE} = 10 A (estimation)	56	59	62	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<8:7> = 01b); V_{RIPPLE} = 10 A (estimation)	58	61	64	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 10 A; (MFR_SPECIFIC_15<8:7> = 10b); V_{RIPPLE} = 10 A (estimation)	60	63	66	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 12 A; (MFR_SPECIFIC_15<8:7> = 11b); V_{RIPPLE} = 10 A (estimation)	62	65	68	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<8:7> = 00b); V_{RIPPLE} = 10 A (estimation)	62	65	68	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<8:7> = 01b); V_{RIPPLE} = 10 A (estimation)	64	67	70	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 10 A; (MFR_SPECIFIC_15<8:7> = 10b); V_{RIPPLE} = 10 A (estimation)	66	69	72	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 12 A; (MFR_SPECIFIC_15<8:7> = 11b); V_{RIPPLE} = 10 A (estimation)	68	71	74	A

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS3}$	Dynamic phase shedding threshold, 4 to 3 phases (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_14<11:10> = 00b)	31	34	37	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_14<11:10> = 01b)	33	36	39	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_14<11:10> = 10b)	35	38	41	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_14<11:10> = 11b)	37	40	43	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_14<11:10> = 00b)	37	40	43	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_14<11:10> = 01b)	39	42	45	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_14<11:10> = 10b)	41	44	47	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_14<11:10> = 11b)	43	46	49	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_14<11:10> = 00b)	43	46	49	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_14<11:10> = 01b)	45	48	51	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_14<11:10> = 10b)	47	50	53	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_14<11:10> = 11b)	49	52	55	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_14<11:10> = 00b)	49	52	55	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_14<11:10> = 01b)	51	54	57	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_14<11:10> = 10b)	53	56	59	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_14<11:10> = 11b)	55	58	61	A

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA4}$	Dynamic phase adding threshold, 4 to 5 Phases (Peak Current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<10:9> = 00b); V_{RIPPLE} = 8 A (estimation)	54.5	58	61.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<10:9> = 01b); V_{RIPPLE} = 8 A (estimation)	56.5	60	63.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 10 A; (MFR_SPECIFIC_15<10:9> = 10b); V_{RIPPLE} = 8 A (estimation)	58.5	62	65.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 12 A; (MFR_SPECIFIC_15<10:9> = 11b); V_{RIPPLE} = 8 A (estimation)	60.5	64	67.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<10:9> = 00b); V_{RIPPLE} = 8 A (estimation)	62.5	66	69.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<10:9> = 01b); V_{RIPPLE} = 8 A (estimation)	64.5	68	71.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 10 A; (MFR_SPECIFIC_15<10:9> = 10b); V_{RIPPLE} = 8 A (estimation)	66.5	70	73.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 12 A; (MFR_SPECIFIC_15<10:9> = 11b); V_{RIPPLE} = 8 A (estimation)	68.5	72	75.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<10:9> = 00b); V_{RIPPLE} = 8 A (estimation)	70.5	74	77.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<10:9> = 01b); V_{RIPPLE} = 8 A (estimation)	72.5	76	79.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 10 A; (MFR_SPECIFIC_15<10:9> = 10b); V_{RIPPLE} = 8 A (estimation)	74.5	78	81.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 12 A; (MFR_SPECIFIC_15<10:9> = 11b); V_{RIPPLE} = 8 A (estimation)	76.5	80	83.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<10:9> = 00b); V_{RIPPLE} = 8 A (estimation)	78.5	82	85.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<10:9> = 01b); V_{RIPPLE} = 8 A (estimation)	80.5	84	87.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 10 A; (MFR_SPECIFIC_15<10:9> = 10b); V_{RIPPLE} = 8 A (estimation)	82.5	86	89.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 12 A; (MFR_SPECIFIC_15<10:9> = 11b); V_{RIPPLE} = 8 A (estimation)	84.5	88	91.5	A

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS4}$	Dynamic phase shedding threshold, 5 to 4 phases (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_14<13:12> = 00b)	42.5	46	49.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_14<13:12> = 01b)	44.5	48	51.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_14<13:12> = 10b)	46.5	50	53.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_14<13:12> = 11b)	48.5	52	55.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_14<13:12> = 00b)	50.5	54	57.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_14<13:12> = 01b)	52.5	56	59.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_14<13:12> = 10b)	54.5	58	61.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_14<13:12> = 11b)	56.5	60	63.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_14<13:12> = 00b)	58.5	62	65.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_14<13:12> = 01b)	60.5	64	67.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_14<13:12> = 10b)	62.5	66	69.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_14<13:12> = 11b)	64.5	68	71.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_14<13:12> = 00b)	66.5	70	73.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_14<13:12> = 01b)	68.5	72	75.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_14<13:12> = 10b)	70.5	74	77.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_14<13:12> = 11b)	72.5	76	79.5	A

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Dynamic Phase Add and Drop (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA5}$	Dynamic phase adding threshold, 5 to 6 Phases (Peak Current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<12:11> = 00b); V_{RIPPLE} = 6 A (estimation)	65	69	73	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<12:11> = 01b); V_{RIPPLE} = 6 A (estimation)	67	71	75	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 10 A; (MFR_SPECIFIC_15<12:11> = 10b); V_{RIPPLE} = 6 A (estimation)	69	73	77	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 12 A; (MFR_SPECIFIC_15<12:11> = 11b); V_{RIPPLE} = 6 A (estimation)	71	75	79	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<12:11> = 00b); V_{RIPPLE} = 6 A (estimation)	75	79	83	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<12:11> = 01b); V_{RIPPLE} = 6 A (estimation)	77	81	85	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 10 A; (MFR_SPECIFIC_15<12:11> = 10b); V_{RIPPLE} = 6 A (estimation)	79	83	87	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 12 A; (MFR_SPECIFIC_15<12:11> = 11b); V_{RIPPLE} = 6 A (estimation)	81	85	89	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<12:11> = 00b); V_{RIPPLE} = 6 A (estimation)	85	89	93	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<12:11> = 01b); V_{RIPPLE} = 6 A (estimation)	87	91	95	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 10 A; (MFR_SPECIFIC_15<12:11> = 10b); V_{RIPPLE} = 6 A (estimation)	89	93	97	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 12 A; (MFR_SPECIFIC_15<12:11> = 11b); V_{RIPPLE} = 6 A (estimation)	91	95	99	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<12:11> = 00b); V_{RIPPLE} = 6 A (estimation)	95	99	103	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<12:11> = 01b); V_{RIPPLE} = 6 A (estimation)	97	101	105	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 10 A; (MFR_SPECIFIC_15<12:11> = 10b); V_{RIPPLE} = 6 A (estimation)	99	103	107	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 12 A; (MFR_SPECIFIC_15<12:11> = 11b); V_{RIPPLE} = 6 A (estimation)	101	105	109	A

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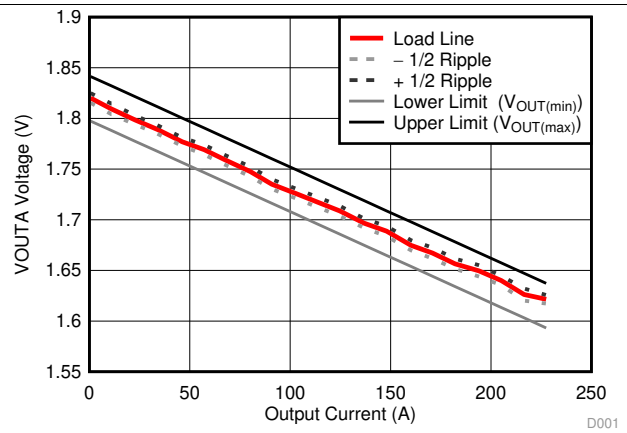
Dynamic Phase Add and Drop (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS5}$	Dynamic phase shedding threshold, 6 to 5 phases (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_14<15:14> = 00b)	54	58	62	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_14<15:14> = 01b)	56	60	64	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_14<15:14> = 10b)	58	62	66	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_14<15:14> = 11b)	60	64	68	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_14<15:14> = 00b)	64	68	72	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_14<15:14> = 01b)	66	70	74	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_14<15:14> = 10b)	68	72	76	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_14<15:14> = 11b)	70	74	78	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_14<15:14> = 00b)	74	78	82	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_14<15:14> = 01b)	76	80	84	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_14<15:14> = 10b)	78	82	86	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_14<15:14> = 11b)	80	84	88	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_14<15:14> = 00b)	84	88	92	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_14<15:14> = 01b)	86	90	94	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_14<15:14> = 10b)	88	92	96	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_14<15:14> = 11b)	90	94	98	A

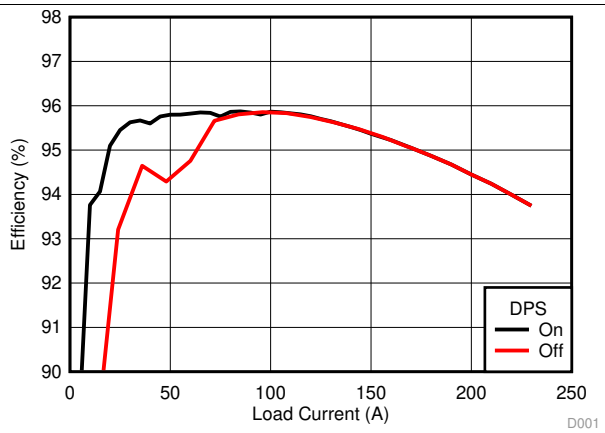
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6.25 Typical Characteristics



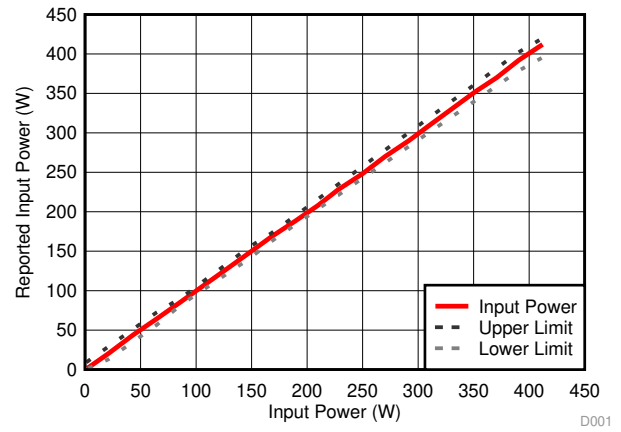
V_{VIN} = 12 V V_{OUT} = 1.82 V
Load Line = 0.9 mΩ

図 2. VOUTA Load Line



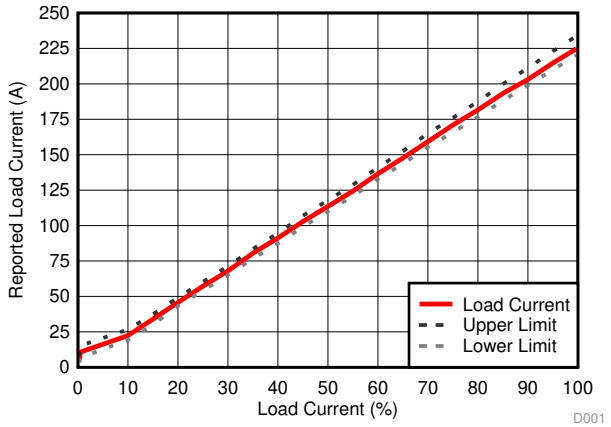
V_{VIN} = 12 V V_{OUT} = 1.8 V
Load Line = 0.9 mΩ f_{SW} = 600 kHz

図 3. Efficiency



V_{VIN} = 12 V V_{OUT} = 1.82 V
Load Line = 0.9 mΩ

図 4. VOUTA Reported Input Power by PMBus



V_{VIN} = 12 V V_{OUT} = 1.82 V
Load Line = 0.9 mΩ

図 5. VOUTA Reported Output Current by PMBus

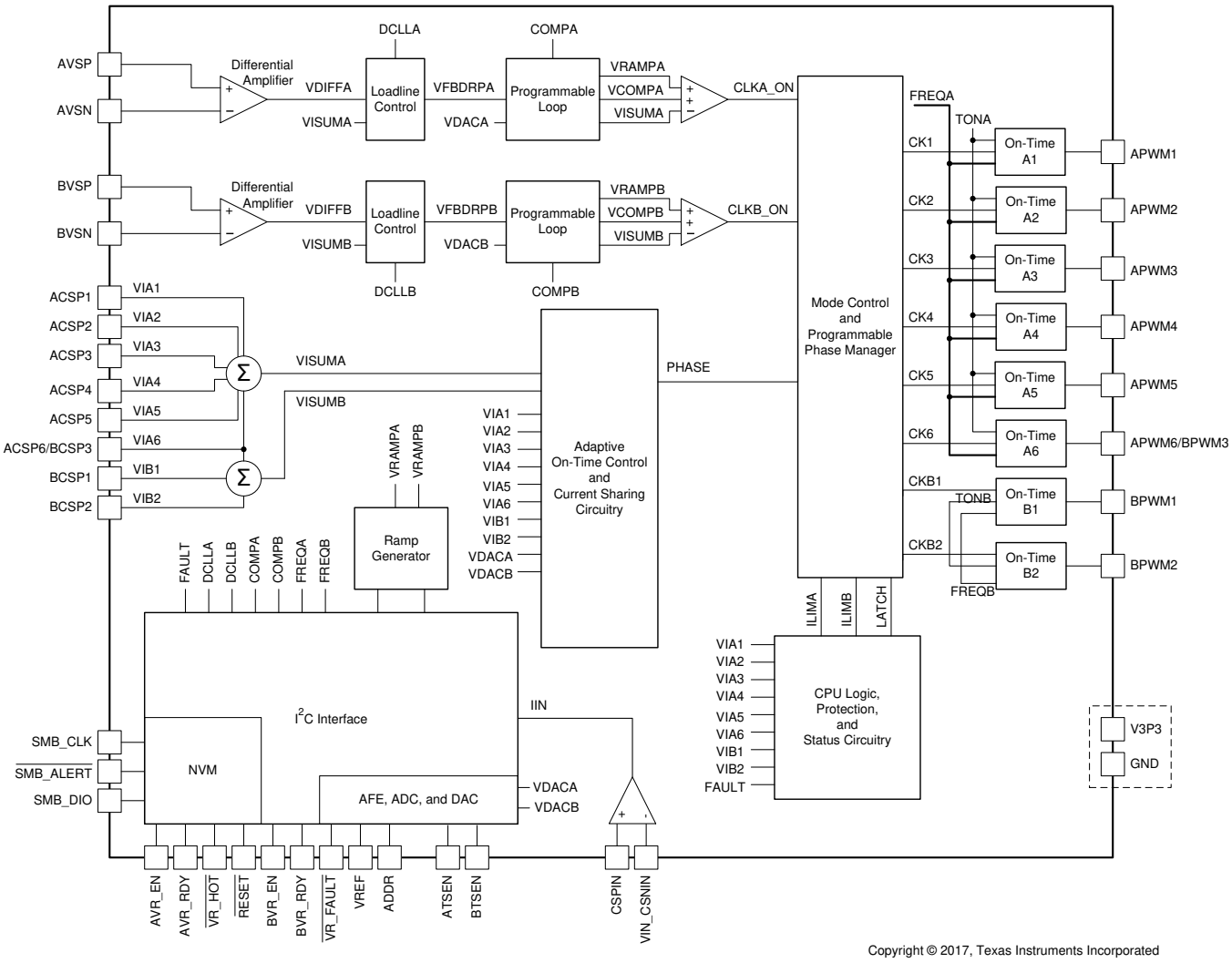
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7 Detailed Description

7.1 Overview

The TPS53681 is a multiphase step-down controller with dual channels, built-in non-volatile memory (NVM), and PMBus™ interface, and is fully compatible with TI NexFET ™ power stages. Advanced control features such as D-CAP+™ architecture with undershoot reduction (USR) provide transient response,

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Phase Interleaving and PWM Operation

As shown in the *Overview* section, in 8-phase continuous conduction mode, the device operates as described in 図 6.

Feature Description (continued)

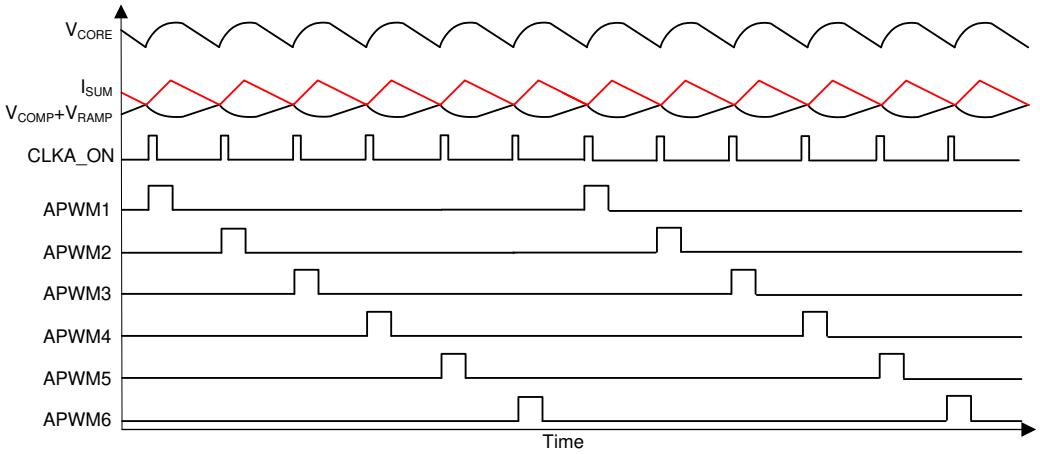


図 6. D-CAP+ Mode Basic Waveforms

Starting with the condition that the high-side FETs are off and the low-side FETs are on, the summed current feedback (V_{ISUM}) is higher than the summed error amplifier output (V_{COMP}) and the internal ramp signal (V_{RAMP}). I_{SUM} falls until it hits V_{COMP}+$V_{RAMP,}$ which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator. This generates the internal CLKA_ON signal. Each CLKA_ON signal corresponds to one switching ON pulse for one phase.

In case of single-phase operation, every CLKA_ON signal generates a switching pulse on the same phase. Also, V_{ISUM} corresponds to just a single-phase inductor current.

In case of multi-phase operation, the CLKA_ON signal gets distributed to each of the phases in a cycle. This approach of using the summed inductor current and cyclically distributing the ON pulses to each phase automatically gives the required interleaving of 360 / *n*, where *n* is the number of phases.

7.3.1.1 Setting the Load-Line (DROOP)

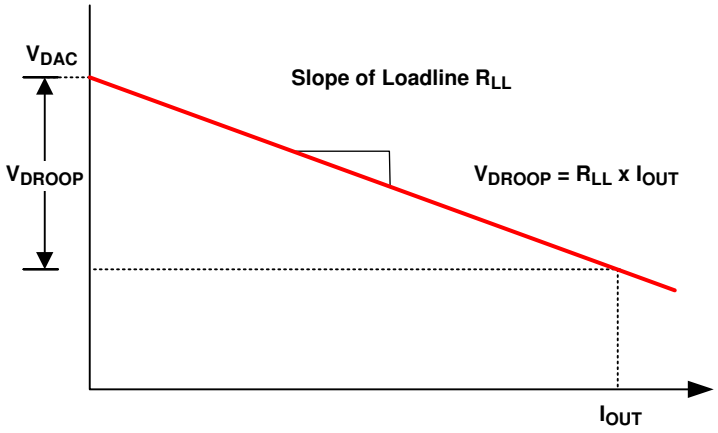


図 7. Load Line

The loadline can be set with VOUT_DROOP register via PMBus. The programmable range for channel A is between 0 mΩ and 3.125 mΩ with 64 options, and the range for channel B is between 0 mΩ and 0.875 mΩ with 16 options to fulfill the requirements for different applications.

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Feature Description (continued)

7.3.1.2 Load Transitions

When there is a sudden load increase, the output voltage immediately drops. The TPS53681 device reacts to this drop in a rising voltage on the COMP pin. This rise forces the PWM pulses to come in sooner and more frequently which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, the device reaches a steady-state operating condition and the PWM switching resumes the steady-state frequency.

When there is a sudden load release, the output voltage flies high. The TPS53681 device reacts to this rise in a falling voltage on the COMP pin. This drop forces the PWM pulses to be delayed until the inductor current reaches the new load current. At that point, the switching resumes and steady-state switching continues.

Please note in 図 8 and 図 9, the ripples on V_{OUT}, V_{RAMP}, and V_{COMP} voltages are not shown for simplicity.

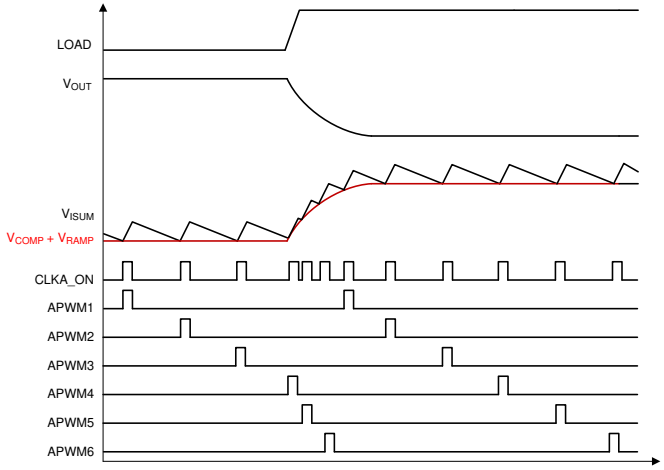


図 8. Load Insertion

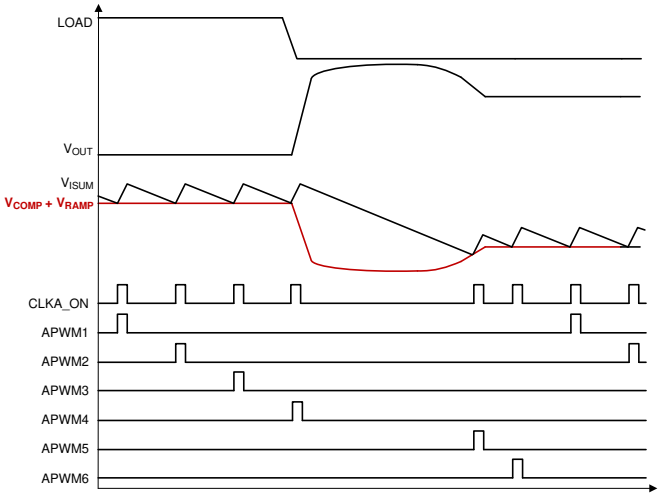


図 9. Load Release

The TPS53681 achieves fast load transient performance using the inherent variable switching frequency characteristics.図 8 illustrates the load insertion behavior that the PWM pulses can be generated with faster frequency than the steady-state frequency to provide more energy to improve the undershoot performance. 図 9 illustrates the load release behavior that PWM pulses can be gated to avoid charging extra energy to the load until the output voltage reaches the peak overshoot.

7.3.1.2.1 VID Table

The DAC voltage V_{DAC} can be changed via PMBus according to 表 2 . Set the VOUT_SCALE_LOOP command to 1.125 to achieve output voltages higher than 2.500. The controller will acknowledge all VID codes and ignore those which are unsupported per the table below.

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表 2. VID Table

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
00	0	0
01	0.25	0.50
02	0.255	0.51
03	0.26	0.52
04	0.265	0.53
05	0.27	0.54
06	0.275	0.55
07	0.28	0.56
08	0.285	0.57
09	0.29	0.58
0A	0.295	0.59
0B	0.30	0.60
0C	0.305	0.61
0D	0.31	0.62
0E	0.315	0.63
0F	0.32	0.64
10	0.325	0.65
11	0.33	0.66
12	0.335	0.67
13	0.34	0.68
14	0.345	0.69
15	0.35	0.70
16	0.355	0.71
17	0.36	0.72
18	0.365	0.73
19	0.37	0.74
1A	0.375	0.75
1B	0.38	0.76
1C	0.385	0.77
1D	0.39	0.78
1E	0.395	0.79
1F	0.40	0.80
20	0.405	0.81
21	0.41	0.82
22	0.415	0.83
23	0.42	0.84
24	0.425	0.85
25	0.43	0.86
26	0.435	0.87
27	0.44	0.88
28	0.445	0.89
29	0.45	0.90
2A	0.455	0.91
2B	0.46	0.92
2C	0.465	0.93
2D	0.47	0.94
2E	0.475	0.95

表 2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
2F	0.48	0.96
30	0.485	0.97
31	0.49	0.98
32	0.495	0.99
33	0.50	1.00
34	0.505	1.01
35	0.51	1.02
36	0.515	1.03
37	0.52	1.04
38	0.525	1.05
39	0.53	1.06
3A	0.535	1.07
3B	0.54	1.08
3C	0.545	1.09
3D	0.55	1.10
3E	0.555	1.11
3F	0.56	1.12
40	0.565	1.13
41	0.57	1.14
42	0.575	1.15
43	0.58	1.16
44	0.585	1.17
45	0.59	1.18
46	0.595	1.19
47	0.60	1.20
48	0.605	1.21
49	0.61	1.22
4A	0.615	1.23
4B	0.62	1.24
4C	0.625	1.25
4D	0.63	1.26
4E	0.635	1.27
4F	0.64	1.28
50	0.645	1.29
51	0.65	1.30
52	0.655	1.31
53	0.66	1.32
54	0.665	1.33
55	0.67	1.34
56	0.675	1.35
57	0.68	1.36
58	0.685	1.37
59	0.69	1.38
5A	0.695	1.39
5B	0.70	1.40
5C	0.705	1.41
5D	0.71	1.42

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表 2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
5E	0.715	1.43
5F	0.72	1.44
60	0.725	1.45
61	0.73	1.46
62	0.735	1.47
63	0.74	1.48
64	0.745	1.49
65	0.75	1.50
66	0.755	1.51
67	0.76	1.52
68	0.765	1.53
69	0.77	1.54
6A	0.775	1.55
6B	0.78	1.56
6C	0.785	1.57
6D	0.79	1.58
6E	0.795	1.59
6F	0.80	1.60
70	0.805	1.61
71	0.81	1.62
72	0.815	1.63
73	0.82	1.64
74	0.825	1.65
75	0.83	1.66
76	0.835	1.67
77	0.84	1.68
78	0.845	1.69
79	0.85	1.70
7A	0.855	1.71
7B	0.86	1.72
7C	0.865	1.73
7D	0.87	1.74
7E	0.875	1.75
7F	0.88	1.76
80	0.885	1.77
81	0.89	1.78
82	0.895	1.79
83	0.90	1.80
84	0.905	1.81
85	0.91	1.82
86	0.915	1.83
87	0.92	1.84
88	0.925	1.85
89	0.93	1.86
8A	0.935	1.87
8B	0.94	1.88
8C	0.945	1.89

表 2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
8D	0.95	1.90
8E	0.955	1.91
8F	0.96	1.92
90	0.965	1.93
91	0.97	1.94
92	0.975	1.95
93	0.98	1.96
94	0.985	1.97
95	0.99	1.98
96	0.995	1.99
97	1.00	2.00
98	1.005	2.01
99	1.01	2.02
9A	1.015	2.03
9B	1.02	2.04
9C	1.025	2.05
9D	1.03	2.06
9E	1.035	2.07
9F	1.04	2.08
A0	1.045	2.09
A1	1.05	2.10
A2	1.055	2.11
A3	1.06	2.12
A4	1.065	2.13
A5	1.07	2.14
A6	1.075	2.15
A7	1.08	2.16
A8	1.085	2.17
A9	1.09	2.18
AA	1.095	2.19
AB	1.10	2.20
AC	1.105	2.21
AD	1.11	2.22
AE	1.115	2.23
AF	1.12	2.24
B0	1.125	2.25
B1	1.13	2.26
B2	1.135	2.27
B3	1.14	2.28
B4	1.145	2.29
B5	1.15	2.30
B6	1.155	2.31
B7	1.16	2.32
B8	1.165	2.33
B9	1.17	2.34
BA	1.175	2.35
BB	1.18	2.36

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表 2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
BC	1.185	2.37
BD	1.19	2.38
BE	1.195	2.39
BF	1.20	2.40
C0	1.205	2.41
C1	1.21	2.42
C2	1.215	2.43
C3	1.22	2.44
C4	1.225	2.45
C5	1.23	2.46
C6	1.235	2.47
C7	1.24	2.48
C8	1.245	2.49
C9	1.25	2.50
CA	1.255	n/a
CB	1.26	n/a
CC	1.265	n/a
CD	1.27	n/a
CE	1.275	n/a
CF	1.28	n/a
D0	1.285	n/a
D1	1.29	n/a
D2	1.295	n/a
D3	1.30	n/a
D4	1.305	n/a
D5	1.31	n/a
D6	1.315	n/a
D7	1.32	n/a
D8	1.325	n/a
D9	1.33	n/a
DA	1.335	n/a
DB	1.34	n/a
DC	1.345	n/a
DD	1.35	n/a

表 2. VID Table (continued)

VID Hex VALUE	DAC STEP (5 mV)	DAC STEP (10 mV)
DE	1.355	n/a
DF	1.36	n/a
E0	1.365	n/a
E1	1.37	n/a
E2	1.375	n/a
E3	1.38	n/a
E4	1.385	n/a
E5	1.39	n/a
E6	1.395	n/a
E7	1.40	n/a
E8	1.405	n/a
E9	1.41	n/a
EA	1.415	n/a
EB	1.42	n/a
EC	1.425	n/a
ED	1.43	n/a
EE	1.435	n/a
EF	1.44	n/a
F0	1.445	n/a
F1	1.45	n/a
F2	1.455	n/a
F3	1.46	n/a
F4	1.465	n/a
F5	1.47	n/a
F6	1.475	n/a
F7	1.48	n/a
F8	1.485	n/a
F9	1.49	n/a
FA	1.495	n/a
FB	1.50	n/a
FC	1.505	n/a
FD	1.51	n/a
FE	1.515	n/a
FF	1.52	n/a

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7.3.1.3 Temperature and Fault Sensing

TI smart power stage senses the die temperature and sends out the temperature information as a voltage through the TAO pin. In a multi-phase application, the TAO pin of the TI smart power stages are connected together and then tied to the ATSEN and BTSEN pins of the TPS53681 device. In this case, the device reports the temperature of the hottest power stage. The reported temperature can be calculated as shown in 式 1.

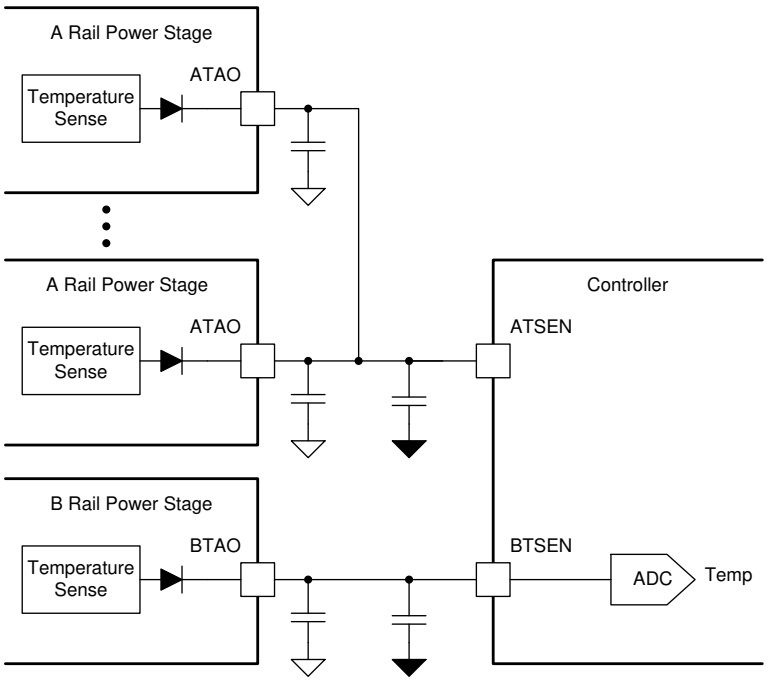
$$\text{TEMP} = \frac{(V_{TSEN} - 0.6)}{0.008} \quad (1)$$

where

- TEMP is the sensed temperature in °C
- V_{TSEN} is the voltage at ATSEN and BTSEN pins

TSEN signal is also used as an indicator for power stage fault. When an internal fault occurs in the TI smart power stage, the power stage pulls the xTAO pins high. If the TSEN voltage is higher than 2.5 V, the TPS53681 device senses the fault and turns off both the high-side and the low-side MOSFETS.

The TSEN signal is also used to indicate hand-shaking between the controller and the power stages. If the power stages are not powered, the TAO pin is pulled down to prevent switching, even if the controller is enabled.



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図 10. Temperature Sense

7.3.1.4 AutoBalance™ Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase as shown in 図 11. The PWM comparator (not shown) starts a pulse when the feedback voltage meets the reference. The V_{IN} voltage charges $C_{t(on)}$ through $R_{t(on)}$. The pulse terminates when the voltage at $C_{t(on)}$ matches the on-time reference, which normally equals the DAC voltage (V_{DAC}).

The circuit operates in the following fashion. First assume that the 1-µs averaged value from each phase current are equal. In this case, the PWM modulator terminates at V_{DAC}, and the normal pulse width is delivered to the system. If instead, I1 > I_{AVG}, then an offset is subtracted from V_{DAC}, and the pulse width for Phase 1 is shortened to reduce the phase current in Phase 1 for balancing. If I1 < I_{AVG}, then a longer pulse is generated to increase the phase current in Phase 1 to achieve current balancing.

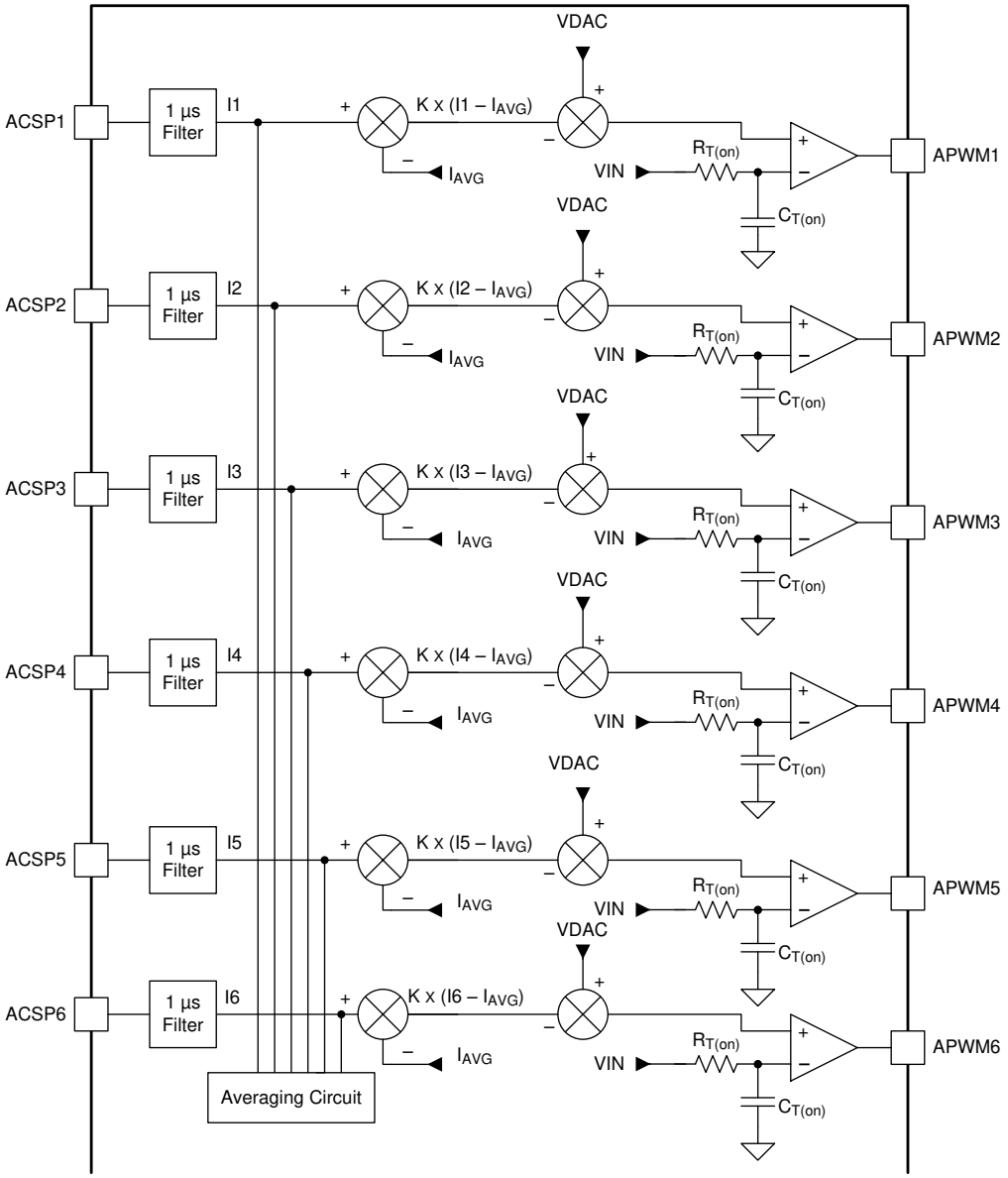


図 11. AutoBalance Current Sharing Circuit Detail

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7.3.1.5 Phase Configuration for Channel B

By default, the second rail of the TPS53681 is configured for two-phase operation. Two NVM bits, CHB_2PH and CHB_3PH control the number of phases available to channel B. The CHB_2PH bit is found in MFR_SPECIFIC_13 (bit 12), and the CHB_3PH bit is found in USER_DATA_11. See 表 3 below, which describes these bit settings, versus phase configuration for channel B. Refer to the accompanying *Technical Reference Manual* for a register map of MFR_SPECIFIC_13 and USER_DATA_11. Refer to Current Sense Inputs for Active Phases for information about pin configuration of CSP signals for various channel B phase configuration settings.

表 3. Channel B Phase Configuration

Channel B Phases	CHB_2PH MFR_SPECIFIC_13[PAGE0][12] USER_DATA_11[PAGE0][9]	CHB_3PH USER_DATA_11[PAGE0][9]
1	1b	0b
2	0b	0b
3	0b	1b

7.3.1.6 RESET Function

During adaptive voltage scaling (AVS) operation, the voltage may become falsely adjusted to be out of ASIC operating range. The RESET function returns the voltage to the VBOOT voltage. When the voltage is out of ASIC operating range, the ASIC issues a $\overline{\text{RESET}}$ signal to the TPS53681 device, as shown in 図 12. The device senses this signal and after a delay of greater than 1 µs, it sets an internal RESET_FAULT signal and sets VOUT_COMMAND to VBOOT. The device pulls the output voltage to the VBOOT level with the slew rate set by VOUT_TRANSITION_RATE command, as shown in 図 13.

When the $\overline{\text{RESET}}$ pin signal goes high, the internal RESET_FAULT signal goes low.

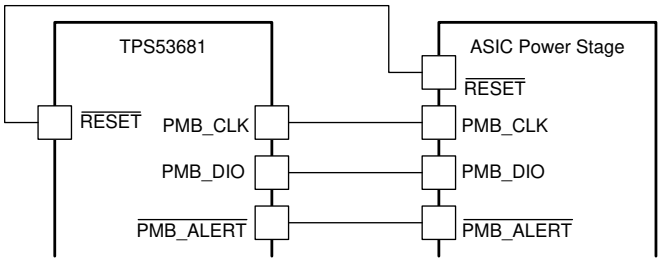


図 12. $\overline{\text{RESET}}$ Pin Connection

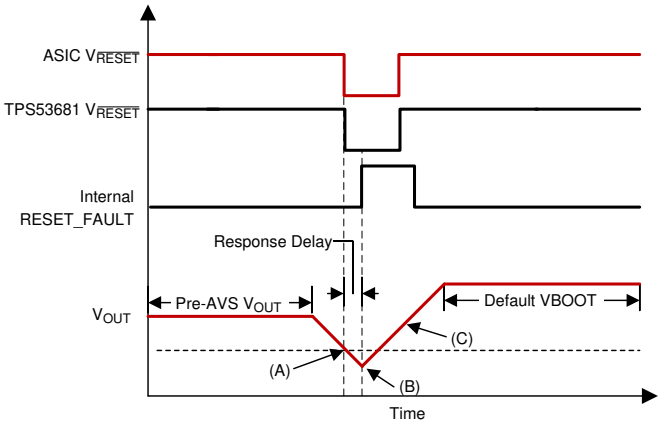


図 13. Reset Function

7.4 Device Functional Modes

7.5 Programming

7.5.1 PMBus Connections

The TPS53681 device can support either 100kHz class, 400 kHz class or 1 MHz class operation, with 1.8-V or 3.3-V logic levels. Connection for the PMBus interface should follow the DC specifications given in *Section 4.3 of the System Management Bus (SMBus) Specification V3.0* . The complete SMBus specification is available from the SMBus website, smbus.org.

7.5.2 PMBus Address Selection

The PMBus slave addresses for TPS53681 are selected with a resistor divider from VREF to ADDR.

Programming (continued)

The PMBus slave address is set by the voltage on the ADDR pin. Refer to Table 4. With the desired PMBus address, and R_{ADDRL} selected, calculate the R_{ADDRH} using Equation 2.

Note that TPS53681 uses 7 bit addressing, per the SMBus specification. Users communicating to the device using generic I^2C drivers should be aware that these 7 bits occupy the most significant bits of the first byte in each transaction, with the least significant bit being the data direction bit (0 for write operations, 1 for read operations). That is, for read transactions, the address byte is $A_6A_5A_4A_3A_2A_1A_01$ and for write operations the address byte is $A_6A_5A_4A_3A_2A_1A_00$. Refer to the SMBus specification for more information.

The general procedure for selecting these resistors is as follows:

1. Determine the desired PMBus slave addresses, per system requirements
2. Select an R_{ADDRL} value of 10 kΩ or 20 kΩ
3. Using the desired PMBus address, refer to Table 4 for the desired address pin voltage
4. Use Equation 2 to calculate R_{ADDRH}

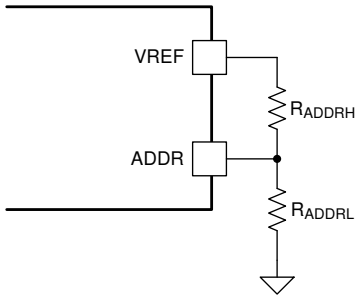


Figure 14. PMBus Address Selection

Contact your local Texas Instruments representative for a copy of the PMBus address setting design tool spreadsheet.

$$R_{ADDRH} = R_{ADDRL} \left(\frac{V_{REF}}{V_{ADDR}} - 1 \right) \quad (2)$$

Table 4. PMBus Slave Address Selection

V_{ADDR} (V)	PMBus Address (7 bit binary) $A_6A_5A_4A_3A_2A_1A_0$	PMBus Address (7-bit decimal)	I^2C Address Byte (Write Operation)	I^2C Address Byte (Read Operation)
≤ 0.039 V	1011000b	88d	B0h	B1h
0.073 V ± 15 mV	1011001b	89d	B2h	B3h
0.122 V ± 15 mV	1011010b	90d	B4h	B5h
0.171 V ± 15 mV	1011011b	91d	B6h	B7h
0.219 V ± 15 mV	1011100b	92d	B8h	B9h
0.268 V ± 15 mV	1011101b	93d	BAh	BBh
0.317 V ± 15 mV	1011110b	94d	BCh	BDh
0.366 V ± 15 mV	1011111b	95d	BEh	BFh
0.415 V ± 15 mV	1100000b	96d	C0h	C1h
0.464 V ± 15 mV	1100001b	97d	C2h	C3h
0.513 V ± 15 mV	1100010b	98d	C4h	C5h
0.562 V ± 15 mV	1100011b	99d	C6h	C7h
0.610 V ± 15 mV	1100100b	100d	C8h	C9h
0.660 V ± 15 mV	1100101b	101d	CAh	CBh
0.708 V ± 15 mV	1100110b	102d	CCh	CDh

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Table 4. PMBus Slave Address Selection (continued)

V_{ADDR} (V)	PMBus Address (7 bit binary) $A_6A_5A_4A_3A_2A_1A_0$	PMBus Address (7-bit decimal)	I^2C Address Byte (Write Operation)	I^2C Address Byte (Read Operation)
0.757 V ± 15 mV	1100111b	103d	CEh	CFh
0.806 V ± 15 mV	1101000b	104d	D0h	D1h
0.854 V ± 15 mV	1101001b	105d	D2h	D3h
0.903 V ± 15 mV	1101010b	106d	D4h	D5h
0.952 V ± 15 mV	1101011b	107d	D6h	D7h
1.000 V ± 15 mV	1101100b	108d	D8h	D9h
1.050 V ± 15 mV	1101101b	109d	DAh	DBh
1.098 V ± 15 mV	1101110b	110d	DCh	DDh
1.147 V ± 15 mV	1101111b	111d	DEh	DFh
1.196 V ± 15 mV	1110000b	112d	E0h	E1h
1.245 V ± 15 mV	1110001b	113d	E2h	E3h
1.294 V ± 15 mV	1110010b	114d	E4h	E5h
1.343 V ± 15 mV	1110011b	115d	E6h	E7h
1.392 V ± 15 mV	1110100b	116d	E8h	E9h
1.440 V ± 15 mV	1110101b	117d	EAh	EBh
1.489 V ± 15 mV	1110110b	118d	ECh	EDh
1.540 V ± 15 mV	1110111b	119d	EEh	EFh

7.5.3 Supported Commands

The table below summarizes the PMBus commands supported by the TPS53681. Only selected commands, which are most commonly used during device configuration and usage are reproduced in this document. For a full set of register maps for this device, refer to the accompanying *Technical Reference Manual*.

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CMD	Command Name	Description	R/W, NVM	Default Behavior	Default Value	
					Ch. A (PAGE 0)	Ch. B PAGE 1
00h	PAGE	Selects which channel subsequent PMBus commands address	RW	All commands address Channel A	N/A	
01h	OPERATION	Enable or disable each channel, enter or exit margin.	RW	Conversion disabled. Margin None.	00h	00h
02h	ON_OFF_CONFIG	Configure the combination of OPERATION, and enable pin required to enable power conversion for each channel.	RW, NVM	OPERATION command only.	1Bh	1Bh
03h	CLEAR_FAULT	Clears all fault status registers to 00h and releases PMB_ALERT	W	Write-only	N/A	
04h	PHASE	Selects which phase of the active channel subsequent PMBus commands address	RW	Commands address all phases.	FFh	FFh
10h	WRITE_PROTECT	Used to control writing to the volatile operating memory (PMBus and restore from NVM).	RW	Writes to all commands are allowed	00h	
11h	STORE_DEFAULT_ALL	Stores all current storable register settings into NVM as new defaults.	W	Write-only	N/A	
12h	RESTORE_DEFAULT_ALL	Restores all storable register settings from NVM.	W	Write-only	N/A	
19h	CAPABILITY	Provides a way for a host system to determine key PMBus capabilities of the device.	R	1 MHz, PEC, PMB_ALERT Supported	D0h	
1Bh	SMBALERT_MASK (STATUS_VOUT)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_IOUT)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_INPUT)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	LOW_VIN does not assert PMB_ALERT	08h	08h
1Bh	SMBALERT_MASK (STATUS_TEMPERATURE)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_CML)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_MFR_SPECIFIC)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
20h	VOUT_MODE	Read-only output mode indicator	R(1)	VID mode. 5 mV Step (Ch A), 5 mV Step (Ch B)	21h	21h
21h	VOUT_COMMAND	Output voltage target.	RW, NVM	0.500 V (Ch A) 0.500 V (Ch B)	0033h	0033h
24h	VOUT_MAX	Sets the maximum output voltage	RW, NVM	1.520 V (Ch A) 1.520 V (Ch B)	00FFh	00FFh
25h	VOUT_MARGIN_HIGH	Load the unit with the voltage to which the output is to be changed when OPERATION command is set to “Margin High”.	RW	0.000 V (CH A) 0.000 V (Ch B)	0000h	0000h
26h	VOUT_MARGIN_LOW	Load the unit with the voltage to which the output is to be changed when OPERATION command is set to “Margin Low”.	RW	0.000 V (CH A) 0.000 V (Ch B)	0000h	0000h
27h	VOUT_TRANSITION_RATE	Used to set slew rate settings for output voltage updates	RW, NVM	1.5625 mV/µs (Ch A) 1.5625 mV/µs (Ch B)	E019h	E019h

(1) NVM-backed bits in the MFR_SPECIFIC or USER_DATA commands affect the reset value of these commands. Refer to the individual register maps for more detail.

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CMD	Command Name	Description	R/W, NVM	Default Behavior	Default Value	
					Ch. A (PAGE 0)	Ch. B PAGE 1
28h	VOUT_DROOP	The VOUT_DROOP sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with Adaptive Voltage Positioning	RW, NVM	0.000 mΩ (Ch A) 0.000 mΩ (Ch B)	D000h	D000h
29h	VOUT_SCALE_LOOP	Used for scaling the VID code	RW, NVM	1.000 (Ch A) 1.000 (Ch B)	E808h	E808h
2Ah	VOUT_SCALE_MONITOR	Used for scaling output voltage telemetry	RW, NVM	1.000 (Ch A) 1.000 (Ch B)	E808h	E808h
2Bh	VOUT_MIN	Sets the minimum output voltage	RW, NVM	0.000 V (Ch A) 0.000 V (Ch B)	0000h	0000h
33h	FREQUENCY_SWITCH	Sets the switching frequency	RW, NVM	500 kHz (Ch A) 500 kHz (Ch B)	01F4h	01F4h
35h	VIN_ON	Sets value of input voltage at which the device should start power conversion.	RW, NVM	6.25 V	F019h	
38h	IOUT_CAL_GAIN	Sets the ratio of voltage at the current sense pins to the sensed current.	RW, NVM	5.000 mΩ (Ch A) 5.000 mΩ (Ch B)	D140h	D140h
39h	IOUT_CAL_OFFSET	Used to null offsets in the output current sensing circuit	RW, NVM	0.000 A (Ch A) 0.000 A (Ch B) (All Phases)	E800h	E800h
40h	VOUT_OV_FAULT_LIMIT	Sets the value of the sensed output voltage which triggers an output overvoltage fault	R	1.520 V (Ch A) 1.520 V (Ch B)	00FFh	00FFh
41h	VOUT_OV_FAULT_RESPONSE	Sets the converter response to an output overvoltage event	R	Shutdown, do not restart	80h	80h
44h	VOUT_UV_FAULT_LIMIT	Sets the value of the sensed output voltage which triggers an output undervoltage fault	R	0.000 V (Ch A) 0.000 V (Ch B)	0000h	0000h
45h	VOUT_UV_FAULT_RESPONSE	Sets the converter response to an output undervoltage event	RW, NVM	Shutdown, do not restart	80h	80h
46h	IOUT_OC_FAULT_LIMIT	Sets the output Over Current fault limit	RW, NVM(1)	39 A (Ch A) 39 A (Ch B)	0027h	0027h
47h	IOUT_OC_FAULT_RESPONSE	Define the over-current fault response.	RW, NVM	Shutdown, and Hiccup	FAh	FAh
4Ah	IOUT_OC_WARN_LIMIT	Sets the value of the output current that causes the over current detector to indicate an over current warning.	RW, NVM(1)	26 A (Ch A) 26 A (Ch B)	001Ah	001Ah
4Fh	OT_FAULT_LIMIT	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over temperature Fault.	RW, NVM(1)	135 °C (Ch A) 135 °C (Ch B)	0087h	0087h
50h	OT_FAULT_RESPONSE	Sets the converter response to an over temperature fault.	RW, NVM	Shutdown, do not restart	80h	80h
51h	OT_WARN_LIMIT	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over temperature warning.	RW	105 °C (Ch A) 105 °C (Ch B)	0069h	0069h
55h	VIN_OV_FAULT_LIMIT	Set the voltage, in volts, of the unit at which it should indicate a Vin Over-voltage Fault.	RW, NVM	14.000 V	000Eh	
56h	VIN_OV_FAULT_RESPONSE	Instructs the device on what action to take in response to an input overvoltage fault.	R	Continue Uninterrupted	00h	
59h	VIN_UV_FAULT_LIMIT	Sets the value of the input voltage that causes an Input Under voltage Fault	RW, NVM	5.500 V	F80Bh	
5Ah	VIN_UV_FAULT_RESPONSE	Sets the converter response to an input undervoltage event	R	Shutdown, do not restart	C0h	

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CMD	Command Name	Description	R/W, NVM	Default Behavior	Default Value	
					Ch. A (PAGE 0)	Ch. B PAGE 1
5Bh	IIN_OC_FAULT_LIMIT	Sets the value in amperes that causes the over current fault condition of the input current	RW, NVM	63.5 A	F87Fh	
5Ch	IIN_OC_FAULT_RESPONSE	Sets the converter response to input overcurrent events	R	Shutdown, do not restart	C0h	
5Dh	IIN_OC_WARN_LIMIT	Sets the value in amperes that causes the over current warning condition of the input current	RW, NVM	63.5 A	F87Fh	
60h	TON_DELAY	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.	RW, NVM	2.43 ms (Ch A) 2.43 ms (Ch B)	C26Eh	C26Eh
6Bh	PIN_OP_WARN_LIMIT	The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high	RW	450 W	08E1h	
78h	STATUS_BYTE	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
79h	STATUS_WORD	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Ah	STATUS_VOUT	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Bh	STATUS_IOUT	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Ch	STATUS_INPUT	PMBus read-only status and flag bits.	RW	Current Status	N/A	
7Dh	STATUS_TEMPERATURE	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Eh	STATUS_CML	PMBus read-only status and flag bits.	RW	Current Status	N/A	
80h	STATUS_MFR_SPECIFIC	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
88h	READ_VIN	Returns the input voltage in volts	R	Current Status	N/A	
89h	READ_IIN	Returns the input current in amperes	R	Current Status	N/A	
8Bh	READ_VOUT	Returns the output voltage in VID format	R	Current Status	N/A	N/A
8Ch	READ_IOUT	Returns the output current in amperes	R	Current Status	N/A	N/A
8Dh	READ_TEMPERATURE_1	Returns the highest power stage temperature in °C	R	Current Status	N/A	N/A
96h	READ_POUT	Returns the output power in Watts	R	Current Status	N/A	N/A
97h	READ_PIN	Returns the input power in Watts	R	Current Status	N/A	
98h	PMBUS_REVISION	Returns the version of the PMBus specification to which this device complies	R	PMBus 1.3 Part I, Part II	33h	
99h	MFR_ID	Loads the unit with bits that contain the manufacturer's ID	RW, NVM	Arbitrary NVM for user	0000h	
9Ah	MFR_MODEL	Loads the unit with bits that contain the manufacturer's model number	RW, NVM	Arbitrary NVM for user	0000h	
9Bh	MFR_REVISION	Loads the unit with bits that contain the manufacturer's model revision	RW, NVM	Arbitrary NVM for user	0400h	
9Dh	MFR_DATE	Loads the unit with bits that contain the manufacture date	RW, NVM	March 2017	1103h	
9Eh	MFR_SERIAL	NVM Checksum	R	NVM checksum	484D2979h	
ADh	IC_DEVICE_ID	Returns a number indicating the part number of the device	R	TPS53681	81h	
AEh	IC_DEVICE_REV	Returns a number indicating the device revision	R	Rev 1.0	00h	
B0h	USER_DATA_00	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B1h	USER_DATA_01	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	

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CMD	Command Name	Description	R/W, NVM	Default Behavior	Default Value	
					Ch. A (PAGE 0)	Ch. B PAGE 1
B2h	USER_DATA_02	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B3h	USER_DATA_03	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B4h	USER_DATA_04	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B5h	USER_DATA_05	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B6h	USER_DATA_06	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B7h	USER_DATA_07	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B8h	USER_DATA_08	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B9h	USER_DATA_09	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
BAh	USER_DATA_10	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
BBh	USER_DATA_11	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
BCh	USER_DATA_12	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
D0h	MFR_SPECIFIC_00	Configures per-phase overcurrent levels, current share thresholds, and other miscellaneous settings.	RW NVM	Misc. configuration, See register maps	0006h	3006h
D3h	MFR_SPECIFIC_03	Returns information regarding current imbalance warnings for each phase	R	Current status	N/A	N/A
D4h	MFR_SPECIFIC_04	Returns the output voltage for the active channel, in linear format	R	Current status	N/A	N/A
D5h	MFR_SPECIFIC_05	Used to trim the output voltage of the active channel, by applying an offset to the currently selected VID code.	RW NVM	0 mV offset (Ch A and Ch B)	00h	00h
D6h	MFR_SPECIFIC_06	Configures dynamic load line options for both channels, and selects Auto-DCM operation.	RW NVM	Misc. configuration, See register maps	0000h	0000h
D7h	MFR_SPECIFIC_07	Configures the internal loop compensation for both channels.	RW NVM	Misc. configuration, See to register maps	118Fh	118Fh
D8h	MFR_SPECIFIC_08	Used to identify catastrophic faults which occur first, and store this information to NVM	RW NVM	Current status	00h	00h
D9h	MFR_SPECIFIC_09	Used to configure non-linear transient performance enhancements such as undershoot reduction (USR)	RW NVM	Misc. configuration, See register maps	76C7h	06C7h
DAh	MFR_SPECIFIC_10	Used to configure input current sensing, and set the maximum output current	RW NVM	Misc. configuration, See register maps	C81Ah	001Ah
DBh	MFR_SPECIFIC_11	Boot-up VID code for each channel	RW NVM	VID 51d (Ch A) VID 51d (Ch B)	33h	33h
DCh	MFR_SPECIFIC_12	Used to configure input current sensing and other miscellaneous settings	RW NVM	Misc. configuration, See register maps	C704h	0700h
DDh	MFR_SPECIFIC_13	Used to configure output voltage slew rates, DAC stepsize, and other miscellaneous settings.	RW NVM	Misc. configuration, See register maps	8825h	0025h

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CMD	Command Name	Description	R/W, NVM	Default Behavior	Default Value	
					Ch. A (PAGE 0)	Ch. B PAGE 1
DEh	MFR_SPECIFIC_14	Used to configure dynamic phase shedding, and compensation ramp amplitude, and dynamic ramp amplitude during USR, and different power states	RW NVM	Misc. configuration, See register maps	0005h	0005h
DFh	MFR_SPECIFIC_15	Used to configure dynamic phase shedding.	RW NVM	Misc. configuration, See register maps	1FFAh	0000h
E4h	MFR_SPECIFIC_20	Used to set the maximum operational phase number, on-the-fly.	RW NVM	Misc. configuration, See register maps	Hardware Configured	
F0h	MFR_SPECIFIC_32	Used to set the input over-power warning	RW	450 W	00E1h	
FAh	MFR_SPECIFIC_42	NVM Security	RW NVM	NVM Security Key	0000h	

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7.5.4 Commonly Used PMBus Commands

The following sections describe the most commonly used PMBus commands and their usage in the configuration, operation and testing of TPS53681 power solutions:

- Voltage, Current, Power, and Temperature Readings
- Input Current Sense and Calibration
- Output Current Sense and Calibration
- Output Voltage Margin Testing
- Loop Compensation
- Converter Protection and Response
- Dynamic Phase Shedding
- NVM Programming
- NVM Security
- Black Box Fault Recording
- Board Identification and Inventory Tracking
- Status Reporting

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7.5.5 Voltage, Current, Power, and Temperature Readings

Using an internal ADC, the TPS53681 provides a full set of telemetry capabilities, allowing the user to read back critical information about the converter's input voltage, input current, input power, output voltage, output current, output power and temperature. The table below summarizes the available commands and their formats. Register maps for each command are included.

表 5. Telemetry Functions

Command	Description	Format	Units	Channel/Phase
READ_VIN	Input voltage telemetry	Linear	V	Shared, Channel A and B
READ_IIN	Input current telemetry	Linear	A	Shared, Channel A and B
READ_VOUT	Output voltage telemetry (VID format)	VID	VID Code	Per Channel
READ_IOUT	Output current telemetry	Linear	A	Per Channel and Per Phase
READ_TEMPERATURE_1	Power stage temperature telemetry	Linear	°C	Per Channel, Highest phase temperature only
READ_POUT	Output power telemetry	Linear	W	Per Channel
READ_PIN	Input power telemetry	Linear	W	Shared, Channel A and B
MFR_SPECIFIC_04	Output voltage telemetry (linear format)	Linear	V	Per Channel

7.5.5.1 (88h) READ_VIN

The READ_VIN command returns the input voltage in volts. The two data bytes are formatted in the Linear Data format. The refresh rate is 1200 µs. This command should be accessed through Read Word transactions, and is shared between channel A and channel B.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_VIN_EXP					READ_VIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 15. READ_VIN

表 6. READ_VIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_VIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_VIN_MAN	R	Current Status	Linear two's complement format mantissa.

7.5.5.2 (89h) READ_IIN

The READ_IIN command returns the input current in amperes. The refresh rate is 100 µs. The two data bytes are formatted in the Linear Data format. This command should be accessed through Read Word transactions, and is shared between channel A and channel B.

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15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_IIN_EXP					READ_IIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 16. READ_IIN

表 7. READ_IIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_IIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_IIN_MAN	R	Current Status	Linear two's complement format mantissa.

7.5.5.3 (8Bh) READ_VOUT

The READ_VOUT command returns the actual, measured output voltage. The two data bytes are formatted in the VID Data format, and the refresh rate is 1200 us. This command should be accessed through Read Word transactions. READ_VOUT is a paged register. In order to access READ_VOUT command for channel A, PAGE must be set to 00h. In order to access READ_VOUT register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VOUT_VID							

LEGEND: R/W = Read/Write; R = Read only

図 17. READ_VOUT

表 8. READ_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	READ_VOUT_VID	R	Current Status	Output voltage, VID format

7.5.5.4 (8Ch) READ_IOUT

The READ_IOUT command returns the output current in amperes. The update rate is 100us. READ_IOUT is a linear format command, and must be accessed through Read Word Transactions.

READ_IOUT is a paged register. In order to access READ_IOUT for channel A, PAGE must be set to 00h. In order to access the READ_IOUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. READ_IOUT is also a phased register. Depending on the configuration of the design, for channel A, PHASE must be set to 00h to access Phase 1, 01h to access Phase 2, etc... PHASE must be set to FFh to access all phases simultaneously. PHASE may also be set to 80h to readack the total phase current (sum of all active phase currents for the active channel) measurement, as described in Output Current Sense and Calibration. Note that READ_IOUT is only a phased command for Channel A (PAGE 0).

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15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_IOUT_EXP					READ_IOUT_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IOUT_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 18. READ_IOUT

表 9. READ_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_IOUT_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_IOUT_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction.

7.5.5.5 (8Dh) READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature in degree Celsius. The refresh rate is 1200 us.

READ_TEMPERATURE_1 is a linear format command. The READ_TEMPERATURE_1 command must be accessed through Read Word transactions.

READ_TEMPERATURE_1 is a paged register. In order to access READ_TEMPERATURE_1 command for channel A, PAGE must be set to 00h. In order to access READ_TEMPERATURE_1 register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_TEMP_EXP					READ_TEMP_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_TEMP_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 19. READ_TEMPERATURE_1

表 10. READ_TEMPERATURE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_TEMP_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_TEMP_MAN	R	Current Status	Linear two's complement format mantissa.

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Attempts to write to this command results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction

7.5.5.6 (96h) READ_POUT

The READ_POUT command returns the calculated output power, in watts for the active channel. The refresh rate is 1200 µs.

READ_POUT is a linear format command. The READ_POUT command must be accessed through Read Word transactions.

READ_POUT is a paged register. In order to access READ_POUT command for channel A, PAGE must be set to 00h. In order to access READ_POUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_POUT_EXP					READ_POUT_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_POUT_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 20. READ_POUT

表 11. READ_POUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_POUT_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_POUT_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction

7.5.5.7 (97h) READ_PIN

The READ_PIN command returns the calculated input power. The refresh rate is 1200 µs.

READ_PIN is a linear format command. The READ_PIN command must be accessed through Read Word transactions.

The READ_PIN command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_PIN_EXP					READ_PIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_PIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 21. READ_PIN

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表 12. READ_PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_PIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_PIN_MAN	R	Current Status	Linear two's complement format mantissa.

7.5.5.8 (D4h) MFR_SPECIFIC_04

The MFR_SPECIFIC_04 command is used to return the output voltage for the active channel, in the **linear** format (READ_VOUT uses VID format).

The MFR_SPECIFIC_04 command must be accessed through Read Word transactions. MFR_SPECIFIC_04 is a Linear format command.

MFR_SPECIFIC_04 is a paged register. In order to access MFR_SPECIFIC_04 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_04 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT_LIN_EXP					VOUT_LIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VOUT_LIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 22. MFR_SPECIFIC_04

表 13. MFR_SPECIFIC_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VOUT_LIN_EXP	R	Current Status	Linear format two's complement exponent.
10:0	VOUT_LIN_MAN	R	Current Status	Linear format two's complement mantissa.

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7.5.6 Input Current Sense and Calibration

The READ_IIN command reports the total input current to both channels. TPS53681 supports shunt or inductor DCR sensing. The section below describes how to calibrate the gain and offset of the sensed signal for accurate input current reporting. When input current sensing is not used, the CSPIN and VIN_CSNIN pins should be shorted together and connected to the power input voltage.

7.5.6.1 Measured Input Current Calibration

The TPS53681 reports input current via an integrated current sense interface on the CSPIN and VIN_CSNIN pins. A conceptual block diagram is shown in 図 23. This circuit must be calibrated to the value of the sense element, R_{SENSE} (e.g. shunt resistance or DCR), chosen. The values of A_{IIN}, IIN_MAX and IIN_OFS may be used to calibrate input current sensing. These settings are programmed using the MFR_SPECIFIC_10 and MFR_SPECIFIC_12 commands.

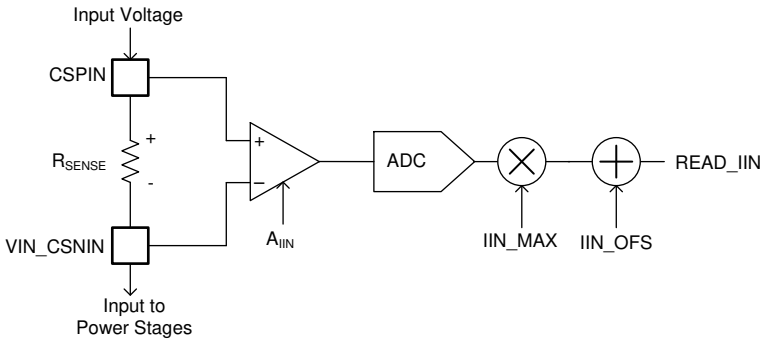


図 23. Measured Input Current Interface

The IIN_RGAIN bits in MFR_SPECIFIC_12, and the IIN_GAIN_CTRL bit in MFR_SPECIFIC_10 select A_{IIN}, the gain of the analog input current sense interface. Refer to 表 18 for a table of supported A_{IIN} values. Note that the analog gain setting also corresponds to maximum allowed signal level and measured input current according to 表 14.

表 14. A_{IIN}, Input Current Sense Analog Gain

IIN_GAIN_CTRL (MFR_SPECIFIC_10)	IIN_RGAIN (MFR_SPECIFIC_12)	Effective A_{IIN}	Maximum Supported (CSPIN–VIN_CSNIN) Voltage	Maximum Supported Input Current Measurement
0b	00b	0.15 mΩ	7.5 mV	50.0 A
0b	01b	0.25 mΩ	12.5 mV	50.0 A
0b	10b	0.3 mΩ	15.0 mV	50.0 A
0b	11b	0.5 mΩ	25.0 mV	50.0 A
1b	00b	1.2 mΩ	7.5 mV	6.25 A
1b	01b	2.0 mΩ	12.5 mV	6.25 A
1b	10b	2.4 mΩ	15.0 mV	6.25 A
1b	11b	4.0 mΩ	25.0 mV	6.25 A

The IIN_MAX bits in MFR_SPECIFIC_10 may also be used to digitally calibrate the gain of the input current reporting. Changing IIN_MAX allows the user to achieve fine gain calibration of the input current sense circuit, as well as support sense element resistor values other than those directly supported using A_{IIN}.

The nominal value of IIN_MAX is 50d. When the sense element resistance and A_{IIN} are equal, IIN_MAX should remain set to 50d. Changing IIN_MAX adjusts the current sense gain ratiometrically with respect to the nominal value of 50d. For example, changing IIN_MAX to 25d, reduces the effective gain by a factor of 2, and changing IIN_MAX to 10d, reduces the effective gain by a factor of 5. IIN_MAX has a maximum value of 64d. When using a sense element R_{SENSE} not equal to one of the supported A_{IIN} values, the IIN_MAX register must be adjusted according to 式 3 to achieve accurate gain calibration.

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$$IIN_MAX = 50d \times \frac{A_{IIN}}{R_{SENSE}} \quad (3)$$

The IIN_OFS bits in MFR_SPECIFIC_10 may also be used to apply an offset to the sensed current in amperes.

Example #1: 0.5 mΩ R_{SENSE}

With a 0.5 mΩ sense element value, for example, (V_{CSPIN} - V_{VIN_CSNIN}) = 10 mV corresponds to 20 A current. Select the analog interface gain, A_{IIN} =0.5 mΩ, since this selection is available in 表 18, and do not apply any scaling via IIN_MAX (set it to 50d).

1. Select the value of A_{IIN} that most closely matches the target sense resistance. In this case, A_{IIN} = 0.5 mΩ is available, which gives IIN_RGAIN = 11b, and IIN_GAIN_CTRL = 0b.
2. Set IIN_MAX = 50d × (0.5 mΩ / 0.5 mΩ) = 50d
3. Set IIN_OFS = 0 A to start with, and tune as needed based on measurements.

Example #2: 1.0 mΩ R_{SENSE}

With a 1.0 mΩ sense element value, for example, (V_{CSPIN} - V_{VIN_CSNIN}) = 10 mV corresponds to 10 A current. With the analog interface gain, A_{IIN} set to 0.5 mΩ, 10 mV would be interpreted as 20 A. Therefore apply IIN_MAX = 50*(0.5 mΩ / 1 mΩ) to reduce the effective gain by a factor of 2, so 10 mV is interpreted as 10 A.

1. Select the value of A_{IIN} that most closely matches the target sense resistance. In this case, 1.0 mΩ is not directly available. Select A_{IIN} = 0.5 mΩ , which gives IIN_RGAIN = 11b, and IIN_GAIN_CTRL = 0b.
2. Set IIN_MAX = 50d × (0.5 mΩ / 1.0 mΩ) = 25d
3. Set IIN_OFS = 0 A to start with, and tune as needed based on measurements.

7.5.6.2 (DAh) MFR_SPECIFIC_10

The MFR_SPECIFIC_10 command is used to configure input current sensing, and set the maximum output current. These values are used for input current and output current telemetry.

The MFR_SPECIFIC_10 command must be accessed through Write Word/Read Word transactions. MFR_SPECIFIC_10 is a paged register. In order to access MFR_SPECIFIC_10 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_10 register for channel B, PAGE must be set to 01h. Note that input current calibration is shared across both channels, but the configuration makes use of both PAGEs.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	R	RW	RW	RW
IIN_MAX (PAGE 0, bits 15:8) IIN_GAIN_CTRL (PAGE 1, bit 13) IIN_OFS (PAGE 1, bits 12:8)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOUT_MAX (PAGE 0, PAGE 1)							

LEGEND: R/W = Read/Write; R = Read only

図 24. MFR_SPECIFIC_10

表 15. MFR_SPECIFIC_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	IIN_MAX (PAGE 0)	RW	NVM	Maximum IIN setting. LSB = 0.25 A. Valid values range from 0 A to 63.75 A.
13	IIN_GAIN_CTRL (PAGE 1)	RW	NVM	Used to increase the effective IIN_RGAIN. See MFR_SPECIFIC_12 for more information.
12:8	IIN_OFS (PAGE 1)	RW	NVM	Input current sense offset calibration. See 表 16.
7:0	IOUT_MAX	RW	NVM	Sets the maximum output current for each channel (PAGE 0 for channel A, PAGE 1 for channel B). LSB = 1 A.

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表 16. Input Current Offset Calibration Settings

IIN_OFS (hex)	IIN Offset (A)
00h	0
01h	0.1
02h	0.2
03h	0.3
04h	0.4
05h	0.5
06h	0.6
07h	0.7
08h	0.8
09h	0.9
0Ah	1.0
0Bh	1.1
0Ch	1.2
0Dh	1.3
0Eh	1.4
0Fh	1.5
10h	-1.6
11h	-1.5
12h	-1.4
13h	-1.3
14h	-1.2
15h	-1.1
16h	-1.0
17h	-0.9
18h	-0.8
19h	-0.7
1Ah	-0.6
1Bh	-0.5
1Ch	-0.4
1Dh	-0.3
1Eh	-0.2
1Fh	-0.1

7.5.6.3 (DCh) MFR_SPECIFIC_12

The MFR_SPECIFIC_12 command is used to configure input current sensing.

The MFR_SPECIFIC_12 command must be accessed through Write Word/Read Word transactions. MFR_SPECIFIC_12 is a paged register, but all relevant configuration bits are associated with PAGE 0. PAGE should be set to 00h when accessing MFR_SPECIFIC_12.

15	14	13	12	11	10	9	8
RW	RW	R	RW	RW	RW	RW	RW
IIN_RGAIN		0	TI_INTERNAL				
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
TI_INTERNAL							

LEGEND: R/W = Read/Write; R = Read only

図 25. MFR_SPECIFIC_12

表 17. MFR_SPECIFIC_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	IIN_RGAIN (PAGE 0 only)	RW	NVM	Input shunt resistance value. Combined with IIN_RGAIN, IIN_OFS, IIN_MAX to calibrate measured input current sensing. Note that finer adjustments can be made using IIN_MAX.
12:0	TI_INTERNAL	RW	NVM	TI Internal bits. These bits are writeable, but should not be modified from their factory default setting.

表 18. A_{IIN}, Input Current Sense Analog Gain (1)

IIN_GAIN_CTRL (MFR_SPECIFIC_10)	IIN_RGAIN (MFR_SPECIFIC_12)	Effective A_{IIN}
0b	00b	0.15 mΩ
0b	01b	0.25 mΩ
0b	10b	0.3 mΩ
0b	11b	0.5 mΩ
1b	00b	1.2 mΩ
1b	01b	2.0 mΩ
1b	10b	2.4 mΩ
1b	11b	4.0 mΩ

(1) See Also 表 14

表 19. Maximum Temperature Settings

TMAX (binary)	Maximum Temperature (°C)
000b	90
001b	95
010b	100
011b	105
100b	110
101b	115
110b	120
111b	125

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7.5.7 Output Current Sense and Calibration

The READ_IOUT command may be used to read the individual phase currents, and the total channel current.

7.5.7.1 Reading Individual Phase Currents

Using the PAGE and PHASE commands, the TPS53681 can be configured to return output current information for each individual phase. The examples below demonstrate this process:

Example #1: Read back the output current of Channel A, First Phase

1. Select Channel A. Write PAGE to 00h
2. Select first phase. Write PHASE to 00h
3. Read READ_IOUT

Example #2: Read back the output current of Channel B, Second Phase

1. Select Channel B. Write PAGE to 01h
2. Select second phase. Write PHASE to 01h
3. Read READ_IOUT

7.5.7.1.1 Reading Total Current

When the PHASE command is set to 80h, the TPS53681 device is configured to return the total channel current (sum of individual phase currents) in response to the READ_IOUT command.

Example: Read the Total Output Current of Channel A

1. Select Channel A. Write PAGE to 00h
2. Select total current measurement. Write PHASE to 80h
3. Read READ_IOUT

7.5.7.1.2 Calibrating Current Measurements

The IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands are available to allow the user to fine-tune current measurements. Setting the PHASE command to 80h also allows the total current measurement to be calibrated in a similar manner. The TI power stage devices supply current information to the controller device, using the CSPx and CSNx pins, with a scale of 5 mV/A. The IOUT_CAL_GAIN command may be used to fine-tune the scaling inside the controller to account for any gain mismatch. Likewise, the IOUT_CAL_OFFSET command may be used to apply an offset to the controller current measurements, to null offset errors.

Example: Calibrating Total Output Current Measurement

1. Select Channel A. Write PAGE to 00h
2. Select the total current. Write PHASE to 80h
3. First read back READ_IOUT under two known output currents:
    1. For this example, apply a load of 60 A
    2. Read back READ_IOUT, record the value. For this example, consider that READ_IOUT gives 59.0 A.
    3. For this example, apply a load of 120 A
    4. Read back READ_IOUT, record the value. For this example, consider that READ_IOUT gives 119.6 A
4. Calculate the gain error:
    1. The current reading increased (119.6 A - 59.0 A) = 60.6 A for a 60 A current step
    2. Hence, the current reading gain is (60.6 A / 60 A) = 1.01.
    3. Ideally, the current reading gain is 1.00, so the readings show a +1% gain error.
5. Apply IOUT_CAL_GAIN to correct the gain error:
    1. The gain error is +1%, and the nominal current sense gain is 5 mΩ, so the current sense gain must be lowered by 1%.
    2. Hence, the IOUT_CAL_GAIN should be programmed to 5 mΩ × (1-1%) = 4.95 mΩ
    3. Referring to 表 21 the closest acceptable value is 4.953125 mΩ, or D13Dh.
    4. Write IOUT_CAL_GAIN to D13Dh.

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6. Determine the offset error at a given point:
   1. Apply a known load. In this example, 90 A.
   2. Read back READ_IOUT. For this example, consider that READ_IOUT gives 89 A.
   3. Hence, the offset error is (89 A - 90A) = -1A.
7. Apply IOUT_CAL_OFFSET to correct the gain error
   1. The offset error is -1 A, so an offset of +1 A must be applied.
   2. Refer to 表 24, the closest available value of IOUT_CAL_OFFSET is +1.0 A or E808h
   3. Write IOUT_CAL_OFFSET to E808h.
8. Issue STORE_DEFAULT_ALL to commit the calibration values to NVM.

7.5.7.2 (38h) IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the ratio of the voltage at the current sense pins to the sensed current, in mΩ.

IOUT_CAL_GAIN is a linear format command. The IOUT_CAL_GAIN command must be accessed through Read Word/Write Word transactions.

IOUT_CAL_GAIN is a paged register. In order to access IOUT_CAL_GAIN for channel A, PAGE must be set to 00h. In order to access the IOUT_CAL_GAIN register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. IOUT_CAL_GAIN is also a phased register. Depending on the configuration of the design, for channel A, PHASE must be set to 00h to access Phase 1, 01h to access Phase 2, etc... PHASE must be set to FFh to access all phases simultaneously. PHASE may also be set to 80h to apply IOUT_CAL_GAIN to the total phase current (sum of all active phases for the current channel) measurement, as described in Output Current Sense and Calibration.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOCG_EXP					IOCG_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOCG_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 26. IOUT_CAL_GAIN

表 20. IOUT_CAL_GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOCG_EXP	R	11010b	Linear two's complement exponent, –6. LSB = 0.015625 mΩ
10:0	IOCG_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

表 21. Acceptable Values of IOUT_CAL_GAIN

IOUT_CAL_GAIN (hex)	Current Sense Gain (mΩ)
D131h	4.765625
D132h	4.78125
D133h	4.796875
D134h	4.8125
D135h	4.828125
D136h	4.84375
D137h	4.859375
D138h	4.875
D139h	4.890625
D13Ah	4.90625

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表 21. Acceptable Values of IOUT_CAL_GAIN (continued)

IOUT_CAL_GAIN (hex)	Current Sense Gain (mΩ)
D13Bh	4.921875
D13Ch	4.9375
D13Dh	4.953125
D13Eh	4.96875
D13Fh	4.984375
D140h	5
D141h	5.015625
D142h	5.03125
D143h	5.046875
D144h	5.0625
D145h	5.078125
D146h	5.09375
D147h	5.109375
D148h	5.125
D149h	5.140625
D14Ah	5.15625
D14Bh	5.171875
D14Ch	5.1875
D14Dh	5.203125
D14Eh	5.21875
D14Fh	5.234375
D150h	5.25

Attempts to write any value other than those specified above results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction.

7.5.7.3 (39h) IOUT_CAL_OFFSET

The IOUT_CAL_OFFSET command is used to compensate for offset errors in the READ_IOUT command, in Amperes.

IOUT_CAL_OFFSET is a linear format command. The IOUT_CAL_OFFSET command must be accessed through Read Word/Write Word transactions

IOUT_CAL_OFFSET is a paged register. In order to access IOUT_CAL_OFFSET for channel A, PAGE must be set to 00h. In order to access the IOUT_CAL_OFFSET register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. IOUT_CAL_OFFSET is also a phased register. Depending on the configuration of the design, for channel A, PHASE must be set to 00h to access Phase 1, 01h to access Phase 2, etc... PHASE must be set to FFh to access all phases simultaneously. PHASE may also be set to 80h to apply IOUT_CAL_OFFSET to the total phase current (sum of all active phases for the current channel) measurement, as described in Output Current Sense and Calibration.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOCOS_EXP					IOCOS_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOCOS_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 27. IOUT_CAL_OFFSET

表 22. IOUT_CAL_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOCOS_EXP	R	11101b	Linear two's complement exponent, –3. LSB = 0.125 A
10:0	IOCOS_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below. Note that there is a different set of acceptable values for individual phases (e.g. PHASE = 00h - 05h, and FFh) vs. the total current telemetry function (e.g. PHASE = 80h). See Output Current Sense and Calibration for more information.

表 23. Acceptable Values of IOUT_CAL_OFFSET (Individual Phases, PHASE ≠ 80h)

IOUT_CAL_OFFSET (hex)	Current Sense Offset (A)
E800h	0.00
E801h	0.125
E802h	0.25
E803h	0.375
E804h	0.5
E805h	0.625
E806h	0.75
E807h	0.875
E808h	1.0
EFF9h	-0.875
EFFAh	-0.75
EFFBh	-0.625
EFFCh	-0.5
EFFDh	-0.375
EFFEh	-0.25
EFFFh	-0.125

表 24. Acceptable Values of IOUT_CAL_OFFSET (Total Current, PHASE = 80h)

IOUT_CAL_OFFSET (hex)	Current Sense Offset (A)
E800h	0.00
E802h	0.25
E804h	0.5
E806h	0.75
E808h	1.0
E80Ah	1.25
E80Ch	1.5
E80Eh	1.75
E810h	2.0
E812h	2.25
E814h	2.5
E816h	2.75
E818h	3.0
E81Ah	3.25
E81Ch	3.5
E81Eh	3.75
E820h	4.0

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表 24. Acceptable Values of IOUT_CAL_OFFSET (Total Current, PHASE = 80h) (continued)

IOUT_CAL_OFFSET (hex)	Current Sense Offset (A)
EFE2h	-3.75
EFE4h	-3.5
EFE6h	-3.25
EFE8h	-3.0
EFEAh	-2.75
EFECh	-2.5
EFEEh	-2.25
EFF0h	-2.0
EFF2h	-1.75
EFF4h	-1.5
EFF6h	-1.25
EFF8h	-1.0
EFFAh	-0.75
EFFCh	-0.5
EFFEh	-0.25

Attempts to write any value other than those specified above results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction.

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7.5.8 Output Voltage Margin Testing

The TPS53681 provides several commands to enable voltage margin testing.

The upper two MARGIN bits in the OPERATION command can be used to toggle the active channel between three states:

1. **Margin None (MARGIN = 0000b).** The output voltage target is equal to VOUT_COMMAND.
2. **Margin Low (MARGIN = 01xxb).** The output voltage target is equal to VOUT_MARGIN_LOW.
3. **Margin High (MARGIN = 10xxb).** The output voltage target is equal to VOUT_MARGIN_HIGH.

In order to use OPERATION, the active channel must be configured for to respect the OPERATION command, via ON_OFF_CONFIG. Output voltage transitions will occur at the slew rate defined by VOUT_TRANSITION_RATE.

The lower two MARGIN bits in the OPERATION command select overvoltage/undervoltage fault handling during margin testing:

1. **Ignore Faults (MARGIN = xx01b) .** Overvoltage/Undervoltage faults will not trigger during margin tests.
2. **Act on Faults (MARGIN = xx10b).** Overvoltage/Undervoltage faults will trigger during margin tests.

Example: Output Voltage Margin Testing (Ignore Faults)

1. Write to the PAGE command to select the desired channel (E.g. PAGE = 00h for channel A).
2. Write VOUT_COMMAND to the desired VID code during Margin None operation.
3. Write VOUT_MARGIN_LOW to the desired VID code during Margin Low operation.
4. Write VOUT_MARGIN_HIGH to the desired VID code during Margin High operation.
5. Set the CMD bit in ON_OFF_CONFIG to 1b to ensure the device is configured to respect the OPERATION command.
6. Margin None. Write OPERATION to 80h.
7. Margin Low. Write OPERATION to 94h.
8. Margin High. Write OPERATION to A4h.

7.5.8.1 (01h) OPERATION

The OPERATION command is used to turn the device output on or off in conjunction with the input from the AVR_EN pin for channel A, and BEN pin for channel B, according to the configuration of the ON_OFF_CONFIG command. It is also used to set the output voltage to the upper or lower MARGIN levels.

OPERATION is a paged register. In order to access OPERATION command for channel A, PAGE must be set to 00h. In order to access OPERATION register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The OPERATION command must be accessed through Read Byte/Write Byte transactions.

7	6	5	4	3	2	1	0
RW	R	RW	RW	RW	RW	RW	RW
ON	0	MARGIN				0	0

LEGEND: R/W = Read/Write; R = Read only

図 28. OPERATION

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表 25. OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ON	RW	0b	Enable/disable power conversion for the currently selected channel(s) according to the PAGE command, when the ON_OFF_CONFIG command is configured to require input from the ON bit for output control. Note that there may be several other requirements that must be satisfied before the currently selected channel(s) can begin converting power (e.g. input voltages above UVLO thresholds, AVR_EN/BEN pins high if required by ON_OFF_CONFIG, etc...) 0b: Disable power conversion 1b: Enable power conversion
5:2	MARGIN	RW	0000b	Set the output voltage to either the value selected by the VOUT_MARGIN_HIGH or MARGIN_LOW commands, for the currently selected channel(s), according to the PAGE command. 0000b: Margin Off. Output voltage is set to the value of VOUT_COMMAND 0101b: Margin Low (Ignore Fault). Output voltage is set to the value of VOUT_MARGIN_LOW. 0110b: Margin Low (Act on Fault). Output voltage is set to the value of VOUT_MARGIN_LOW. 1001b: Margin High (Ignore Fault). Output voltage is set to the value of VOUT_MARGIN_HIGH 1010b: Margin High (Act on Fault). Output voltage is set to the value of VOUT_MARGIN_HIGH.
1:0	0	RW	00b	These bits are writeable but should always be set to 00b.

Note that the VOUT_MAX_WARN bit in STATUS_VOUT can be caused by a margin operation, if "Act on Fault" is selected, and the VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW value loaded by the margin operation exceeds the value of VOUT_COMMAND.

7.5.8.2 (21h) VOUT_COMMAND

VOUT_COMMAND is used to set the output voltage of the active PAGE.

VOUT_COMMAND is a VID format command. VOUT_COMMAND command must be accessed through Read Word/Write Word transactions.

VOUT_COMMAND is a paged register. In order to access VOUT_COMMAND for channel A, PAGE must be set to 00h. In order to access the VOUT_COMMAND register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_CMD_VID							

LEGEND: R/W = Read/Write; R = Read only

図 29. VOUT_COMMAND

表 26. VOUT_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_CMD_VID	RW	NVM	Used to set the commanded VOUT. Cannot be set to a level above the value set by VOUT_MAX.

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7.5.8.3 (26h) VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

VOUT_MARGIN_LOW is a VID format command. The VOUT_MARGIN_LOW command must be accessed through Read Word/Write Word transactions.

VOUT_MARGIN_LOW is a paged register. In order to access VOUT_MARGIN_LOW for channel A, PAGE must be set to 00h. In order to access the VOUT_MARGIN_LOW register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGL_VID							

LEGEND: R/W = Read/Write; R = Read only

図 30. VOUT_MARGIN_LOW

表 27. VOUT_MARGIN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MARGL_VID	RW	00h	Used to set the output voltage to be loaded when the active PAGE is set to Margin Low, in VID format.

7.5.8.4 (25h) VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

VOUT_MARGIN_HIGH is a VID format command. The VOUT_MARGIN_HIGH command must be accessed through Read Word/Write Word transactions.

VOUT_MARGIN_HIGH is a paged register. In order to access VOUT_MARGIN_HIGH for channel A, PAGE must be set to 00h. In order to access the VOUT_MARGIN_HIGH register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGH_VID							

LEGEND: R/W = Read/Write; R = Read only

図 31. VOUT_MARGIN_HIGH

表 28. VOUT_MARGIN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MARGH_VID	RW	00h	Used to set the output voltage to be loaded when the active PAGE is set to Margin High, in VID format.

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7.5.9 Loop Compensation

The TPS53681 provides several options for tuning the output voltage feedback and response to transients. These may be configured by programming the MFR_SPECIFIC_07, VOUT_DROOP, and MFR_SPECIFIC_14. Several such parameters may be configured through these commands:

- **DC Load Line** - Selects the DC shift in output voltage corresponding to increased output current. The DC load line affects both the final value the output voltage settles to, as well as the settling time. Use the VOUT_DROOP command to select the DC load line.
- **Integration Time Constant** - In order to maintain DC accuracy, the control loop includes an integration stage. Use MFR_SPECIFIC_07 to select the integration time constant.
- **Integration Path Gain** - The gain of the integration and AC paths may be selected independently. The AC and DC gains both affect the small-signal bandwidth of the converter. Use MFR_SPECIFIC_07 to select the integration path gain.
- **AC Load Line** - Selects the AC response to output voltage error. The AC load line affects the settling and response time following a load transient event. Use the MFR_SPECIFIC_07 command to select the AC load line.
- **AC Path Gain** - The gain of the integration and AC paths may be selected independently. The AC and DC gains both affect the small-signal bandwidth of the converter. Use MFR_SPECIFIC_07 to select the AC path gain.
- **Ramp Amplitude** - Smaller ramp settings result in faster response, but may also lead to increased frequency jitter. Likewise, large ramp settings result in lower frequency jitter, but may be slightly slower to respond to changing conditions. The ramp setting also affects the small-signal bandwidth of the converter. Use MFR_SPECIFIC_14 to select the ramp heigh setting.

7.5.9.1 (D7h) MFR_SPECIFIC_07

The MFR_SPECIFIC_07 command is used to configure the internal loop compensation for both channels. The MFR_SPECIFIC_07 command must be accessed through Write Word/Read Word transactions.

MFR_SPECIFIC_07 is a paged register. In order to access MFR_SPECIFIC_07 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_07 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	RW	RW	RW	RW	RW	RW
0	0	INT_GAIN		INT_TC			
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
AC_GAIN		ACLL					

LEGEND: R/W = Read/Write; R = Read only

図 32. MFR_SPECIFIC_07

表 29. MFR_SPECIFIC_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Not used	R	0	Not used and set to 0.
13:12	INT_GAIN	RW	NVM	Integration path gain. See 表 30.
11:8	INT_TC	RW	NVM	Integration time constant. See 表 31.
7:6	AC_GAIN	RW	NVM	AC path gain. See 表 32.
5:0	ACLL	RW	NVM	AC Load Line. See 表 33.

表 30. Integration path gain settings

INT_GAIN (binary)	Integration path gain (V/V)
00b	2 × AC_GAIN
01b	1 × AC_GAIN
10b	0.66 × AC_GAIN

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表 30. Integration path gain settings (continued)

INT_GAIN (binary)	Integration path gain (V/V)
11b	0.5 × AC_GAIN

表 31. Integration time constant settings

INT_TC (binary)	Time constant (µs)
0000b	5
0001b	10
0010b	15
0011b	20
0100b	25
0101b	30
0110b	35
0111b	40
1000b	1
1001b	2
1010b	3
1011b	4
1100b	5
1101b	6
1110b	7
1111b	8

表 32. AC path gain settings

AC_GAIN (binary)	AC path gain (V/V)
00b	1
01b	1.5
10b	2
11b	0.5

表 33. AC Load line settings

Bin	ACLL (hex)	AC Load line (mΩ)
0	00h	0.0000
1	01h	0.1250
2	02h	0.2500
3	03h	0.3125
4	04h	0.3750
5	05h	0.4375
6	06h	0.5000
7	07h	0.5625
8	08h	0.6250
9	09h	0.7500
10	0Ah	0.7969
11	0Bh	0.8125
12	0Ch	0.8281
13	0Dh	0.8438
14	0Eh	0.8594
15	0Fh	0.8750
16	10h	0.8906

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表 33. AC Load line settings (continued)

Bin	ACLL (hex)	AC Load line (mΩ)
17	11h	0.9063
18	12h	0.9219
19	13h	0.9375
20	14h	0.9531
21	15h	0.9688
22	16h	0.9844
23	17h	1.000
24	18h	1.0156
25	19h	1.0313
26	1Ah	1.0469
27	1Bh	1.0625
28	1Ch	1.1250
29	1Dh	1.2500
30	1Eh	1.3750
31	1Fh	1.5000
32	20h	1.6250
33	21h	1.7500
34	22h	1.8750
35	23h	1.9375
36	24h	2.000
37	25h	2.0625
38	26h	2.1250
39	27h	2.1875
40	28h	2.2500
41	29h	2.375
42	2Ah	2.4218
43	2Bh	2.4375
44	2Ch	2.4531
45	2Dh	2.4687
46	2Eh	2.4843
47	2Fh	2.5000
48	30h	2.5156
49	31h	2.5312
50	32h	2.5468
51	33h	2.5625
52	34h	2.5781
53	35h	2.5937
54	36h	2.609
55	37h	2.625
56	38h	2.6406
57	39h	2.6562
58	3Ah	2.6718
59	3Bh	2.6875
60	3Ch	2.750
61	3Dh	2.875
62	3Eh	3.000
63	3Fh	3.125

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7.5.9.2 (28h) VOUT_DROOP

The VOUT_DROOP command sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning. This is also referred to as the DC Load Line (DCLL).

VOUT_DROOP is a linear format command. The VOUT_DROOP command must be accessed through Read Word/Write Word transactions.

VOUT_DROOP is a paged register. In order to access VOUT_DROOP for channel A, PAGE must be set to 00h. In order to access the VOUT_DROOP register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VDROOP_EXP					VDROOP_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VDROOP_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 33. VOUT_DROOP

表 34. VOUT_DROOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VDROOP_EXP	R	11010b	Linear two's complement fixed exponent, –6. LSB = 0.015625 mΩ
10:0	VDROOP_MAN	RW	NVM	Linear two's complement mantissa. See table of acceptable values below, note that Channel A and Channel B support different acceptable values of VOUT_DROOP.

The table below summarizes the acceptable values of VOUT_DROOP for channel A and channel B. Attempts to write any value other than those specified below will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

表 35. Acceptable VOUT_DROOP Values

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
0	D000h	Yes	Yes	0
1	D008h	Yes	Yes	0.125
2	D010h	Yes	Yes	0.25
3	D014h	Yes	Yes	0.3125
4	D018h	Yes	Yes	0.375
5	D01Ch	Yes	Yes	0.4375
6	D020h	Yes	Yes	0.5
7	D024h	Yes	Yes	0.5625
8	D028h	Yes	Yes	0.625
9	D030h	Yes	Yes	0.7031
10	D033h	Yes	Yes	0.7969
11	D034h	Yes	Yes	0.8125
12	D035h	Yes	Yes	0.8281
13	D036h	Yes	Yes	0.8438
14	D037h	Yes	Yes	0.8594
15	D038h	Yes	Yes	0.875
16	D039h	Yes	No	0.8906

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表 35. Acceptable VOUT_DROOP Values (continued)

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
17	D03Ah	Yes	No	0.9063
18	D03Bh	Yes	No	0.9219
19	D03Ch	Yes	No	0.9375
20	D03Dh	Yes	No	0.9531
21	D03Eh	Yes	No	0.9688
22	D03Fh	Yes	No	0.9844
23	D040h	Yes	No	1
24	D041h	Yes	No	1.0156
25	D042h	Yes	No	1.0313
26	D043h	Yes	No	1.0469
27	D044h	Yes	No	1.0625
28	D048h	Yes	No	1.125
29	D050h	Yes	No	1.25
30	D058h	Yes	No	1.375
31	D060h	Yes	No	1.5
32	D068h	Yes	No	1.625
33	D070h	Yes	No	1.75
34	D078h	Yes	No	1.875
35	D07Ch	Yes	No	1.9375
36	D080h	Yes	No	2
37	D084h	Yes	No	2.0625
38	D088h	Yes	No	2.125
39	D08Ch	Yes	No	2.1875
40	D090h	Yes	No	2.25
41	D098h	Yes	No	2.328
42	D09Bh	Yes	No	2.4218
43	D09Ch	Yes	No	2.4375
44	D09Dh	Yes	No	2.4531
45	D09Eh	Yes	No	2.4687
46	D09Fh	Yes	No	2.4843
47	D0A0h	Yes	No	2.5
48	D0A1h	Yes	No	2.5156
49	D0A2h	Yes	No	2.5312
50	D0A3h	Yes	No	2.5468
51	D0A4h	Yes	No	2.5625
52	D0A5h	Yes	No	2.5781
53	D0A6h	Yes	No	2.5937
54	D0A7h	Yes	No	2.609
55	D0A8h	Yes	No	2.625
56	D0A9h	Yes	No	2.6406
57	D0AAh	Yes	No	2.6562
58	D0ABh	Yes	No	2.6718
59	D0ACh	Yes	No	2.6875
60	D0B0h	Yes	No	2.75
61	D0B8h	Yes	No	2.875
62	D0C0h	Yes	No	3
63	D0C8h	Yes	No	3.125

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7.5.10 Converter Protection and Response

The TPS53681 supports a variety of power supply protection features. The table below summarizes these protection features, and their related PMBus registers. See the following sections for more details.

Table 36. TPS53681 Protection and Response

	Threshold		Response	
	Command Name	**Default Value**	**Command Name**	**Default Value**
Output Voltage				
Over-Voltage Protection	VOUT_OV_FAULT_LIMIT	1.520 V (Ch A) 1.520 V (Ch B)	VOUT_OV_FAULT_RESPONSE	Shutdown, do not restart
Maximum Allowed Output Voltage	VOUT_MAX	1.520 V (Ch A) 1.520 V (Ch B)	Refer to Register Description	
Under-Voltage Protection	VOUT_UV_FAULT_LIMIT	0.000 V (Ch A) 0.000 V (Ch B)	VOUT_UV_FAULT_RESPONSE	Shutdown, do not restart
Minimum Allowed Output Voltage	VOUT_MIN	0.000 V (Ch A) 0.000 V (Ch B)	Refer to Register Description	
Output Current				
Over-Current Protection	IOUT_OC_FAULT_LIMIT MFR_SPECIFIC_10	39 A (Ch A) 39 A (Ch B)	IOUT_OC_FAULT_RESPONSE	Shutdown, do not restart
Over-Current Warning	IOUT_OC_WARN_LIMIT	26 A (Ch A) 26 A (Ch B)	N/A. Warning Only.	
Input Voltage				
Turn-On Threshold	VIN_ON	6.25 V	N/A	
Over-Voltage Protection	VIN_OV_FAULT_LIMIT	14.00 V	VIN_OV_FAULT_RESPONSE	Continue Uninterrupted
Under-Voltage Protection	VIN_UV_FAULT_LIMIT	5.50 V	VIN_UV_FAULT_RESPONSE	Shutdown, do not restart
Input Current				
Over-Current Protection	IIN_OC_FAULT_LIMIT	63.5 A	IIN_OC_FAULT_RESPONSE	Shutdown, do not restart
Over-Current Warning	IIN_OC_WARN_LIMIT	63.5 A	N/A. Warning Only	
Temperature				
Over-Temperature Protection	OT_FAULT_LIMIT	135 °C (Ch A) 135 °C (Ch B)	OT_FAULT_RESPONSE	Shutdown, do not restart
Over-Temperature Warning	OT_WARN_LIMIT	105 °C (Ch A) 105 °C (Ch B)	N/A. Warning Only.	

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7.5.11 Output Overvoltage Protection and Response

The output overvoltage thresholds track the configured maximum output voltage, VOUT_MAX, with a fixed offset, and may be read back in VID format via the read-only VOUT_OV_FAULT_LIMIT command. The converter response to an overvoltage fault is configured by the read-only VOUT_OV_FAULT_RESPONSE command.

7.5.11.1 (40h) VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT is used to read back the value of the output voltage measured at the sense or output pins that causes an output overvoltage fault in VID format. VOUT_OV_FAULT_LIMIT is a VID format command, and must be accessed through Read Word/Write Word transactions. VOUT_OV_FAULT_LIMIT is a paged register. In order to access VOUT_OV_FAULT_LIMIT for channel A, PAGE must be set to 00h. In order to access the VOUT_OV_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_OVF_VID							

LEGEND: R/W = Read/Write; R = Read only

図 34. VOUT_OV_FAULT_LIMIT

表 37. VOUT_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_OVF_VID	R	See below.	Read-only overvoltage fault limit, in VID format.

When the 5-mV DAC mode VID table is selected via MFR_SPECIFIC_13, the VOUT_OV_FAULT_LIMIT register will be set to FFh. When the 10-mV DAC mode VID table is enabled, the VOUT_OV_FAULT_LIMIT is determined according to the value of VOUT_MAX, with a fixed offset applied.

7.5.11.2 (41h) VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE instructs the device on what action to take in response to an output overvoltage fault. The VOUT_OV_FAULT_RESPONSE command must be accessed through Read Byte transactions. The VOUT_OV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-voltage fault, the controller is latched off, and the following actions are taken:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_OV_FAULT bit in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_OV_RESP							

LEGEND: R/W = Read/Write; R = Read only

図 35. VOUT_OV_FAULT_RESPONSE

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表 38. VOUT_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_OV_RESP	R	80h	80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

7.5.12 Maximum Allowed Output Voltage Setting

The VOUT_MAX command sets an upper limit on the output voltage that the unit may be commanded to, regardless of an other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level.

7.5.12.1 (24h) VOUT_MAX

The VOUT_MAX command sets an upper limit on the output voltage that the unit may be commanded to, regardless of an other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. VOUT_MAX is a VID format command, and must be accessed through Read Word/Write Word transactions. VOUT_MAX is a paged register. In order to access VOUT_MAX for channel A, PAGE must be set to 00h. In order to access the VOUT_COMMAND register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The device detects that an attempt has been made to program the output to a voltage greater than the value set by the VOUT_MAX command. Attempts to program the output voltage greater than VOUT_MAX can include VOUT_COMMAND attempts, and margin events where the VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW values exceed the value of VOUT_MAX. These events will be treated as warning conditions and not as fault conditions. If an attempt is made to program the output voltage higher than the limit set by the VOUT_MAX command, the device will respond as follows:

- The commanded output voltage will be clamped to VOUT_MAX,
- The OTHER bit will be set in the STATUS_BYTE,
- The VOUT bit will be set in the STATUS_WORD,
- The VOUT_MIN_MAX warning bit will be set in the STATUS_VOUT register, and
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

This register should be programmed by the user depending upon the maximum output voltage the converter can support.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MAX_VID							

LEGEND: R/W = Read/Write; R = Read only

図 36. VOUT_MAX

表 39. VOUT_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MAX_VID	RW	NVM	Used to set the maximum VOUT of the device in VID format.

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7.5.13 Output Undervoltage Protection and Response

The output undervoltage protection threshold is configured based on commanded output voltage, VOUT_COMMAND, including the shift due to the DC load line, and a fixed offset. The undervoltage threshold may be read back in VID format via the read-only VOUT_UV_FAULT_LIMIT command. The converter response to an undervoltage fault is configured by the read-only VOUT_UV_FAULT_RESPONSE command.

7.5.13.1 (44h) VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT is used to read back the value of the output voltage measured at the sense or output pins that causes an output undervoltage fault in VID format. VOUT_UV_FAULT_LIMIT is a VID format command, and must be accessed through Read Word transactions. VOUT_UV_FAULT_LIMIT is a paged register. In order to access VOUT_UV_FAULT_LIMIT for channel A, PAGE must be set to 00h. In order to access the VOUT_UV_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_UVF_VID							

LEGEND: R/W = Read/Write; R = Read only

図 37. VOUT_UV_FAULT_LIMIT

表 40. VOUT_UV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_UVF_VID	R	See below.	Read-only undervoltage fault limit, in VID format.

7.5.13.2 (45h) VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault.

Upon triggering the undervoltage fault, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_UV_FAULT bit in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The VOUT_UV_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions.

The VOUT_UV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VO_UV_RESP							

LEGEND: R/W = Read/Write; R = Read only

図 38. VOUT_UV_FAULT_RESPONSE

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表 41. VOUT_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_UV_RESP	RW	NVM	00h: Ignore. The controller will set the appropriate status bits, and alert the host, but continue converting power. BAh: Shutdown and restart. The controller will shutdown the channel on which the fault occurred, and attempt to restart 20ms later. This will occur continuously until the condition causing the fault has disappeared, or the controller has been disabled. 80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

7.5.14 Minimum Allowed Output Voltage Setting

The VOUT_MIN command sets a lower bound on the output voltage to which the unit can be commanded, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under voltage protection.

7.5.14.1 (2Bh) VOUT_MIN

The VOUT_ MIN command sets a lower bound on the output voltage to which the unit can be commanded, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under voltage protection. VOUT_MIN is a VID format command, and must be accessed through Read Word/Write Word transactions. VOUT_MIN is a paged register. In order to access VOUT_MIN for channel A, PAGE must be set to 00h. In order to access the VOUT_MIN register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

If an attempt is made to program the output voltage lower than the limit set by this command, the device will respond as follows:

- The commanded output voltage will be clamped to VOUT_MIN
- The OTHER bit will be set in the STATUS_BYTE
- The VOUT bit will be set in the STATUS_WORD
- The VOUT_MIN_MAX Warning bit will be set in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MIN_VID							

LEGEND: R/W = Read/Write; R = Read only

図 39. VOUT_MIN

表 42. VOUT_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MIN_VID	RW	NVM	Used to set a lower bound for output voltage programming for the active PAGE, is set to in VID format.

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7.5.15 Output Overcurrent Protection and Response

Overcurrent thresholds are configured using the IOUT_OC_FAULT_LIMIT. When the overcurrent fault threshold is reached, the converter will respond according to the settings in IOUT_OC_FAULT_RESPONSE. The IOUT_OC_WARN_LIMIT may also be used to configure an information-only overcurrent warning, which triggers prior to an overcurrent fault. Note, that the MFR_SPECIFIC_00 command, not listed below, also contains settings for per-phase overcurrent limits. Refer to the device *Technical Reference Manual* for more information.

7.5.15.1 (46h) IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the total output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. The command has two data bytes and the data format is Linear as shown in the table below. The units are amperes. IOUT_OC_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. IOUT_OC_FAULT_LIMIT is a paged register. In order to access IOUT_OC_FAULT_LIMIT command for channel A, PAGE must be set to 00h. In order to access IOUT_OC_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOOCF_EXP					IOOCF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCF_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 40. IOUT_OC_FAULT_LIMIT

表 43. IOUT_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOOCF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1.0 A
10:0	IOOCF_MAN	RW	See below.	Linear two's complement mantissa

At power-on, or after a RESTORE_DEFAULT_ALL operation, the IOUT_OC_FAULT_LIMIT command will be loaded with the value of IOUT_MAX × 1.50. The IOUT_MAX bits for each channel are stored in MFR_SPECIFIC_10 (PAGE 0 for channel A, PAGE 1 for channel B). IOUT_OC_FAULT_LIMIT may be changed during operation, but returns to this value on reset.

7.5.15.2 (4Ah) IOUT_OC_WARN_LIMIT

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition. IOUT_OC_WARN_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. IOUT_OC_WARN_LIMIT is a paged register. In order to access IOUT_OC_WARN_LIMIT command for channel A, PAGE must be set to 00h. In order to access IOUT_OC_WARN_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

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IOUT_OC_WARN_LIMIT maximum default value is 255A. In case, Application maximum load current is greater than 255A, IOUT_OC_WARN_LIMIT needs to change as max load current value each time after power-on or RESTORE_DEFAULT_ALL operation.

Upon triggering the overcurrent warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT Over current Warning bit in the STATUS_IOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not

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set)

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOOCW_EXP					IOOCW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCW_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 41. IOUT_OC_WARN_LIMIT

表 44. IOUT_OC_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOOCW_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1.0 A
10:0	IOOCW_MAN	RW	See below.	Linear two's complement mantissa.

At power-on, or after a RESTORE_DEFAULT_ALL operation, the IOUT_OC_WARN_LIMIT command will be loaded with the value of IOUT_MAX. The IOUT_MAX bits for each channel are stored in MFR_SPECIFIC_10 (PAGE 0 for channel A, PAGE 1 for channel B). IOUT_OC_WARN_LIMIT may be changed during operation, but will return to this value on reset.

7.5.15.3 (47h) IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to an output over-current fault. The IOUT_OC_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions. The IOUT_OC_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-current fault, the controller is latched off, and the following actions are taken:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IO_OC_RESP							

LEGEND: R/W = Read/Write; R = Read only

図 42. IOUT_OC_FAULT_RESPONSE

表 45. IOUT_OC_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IO_OC_RESP	RW	NVM	C0h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device. FAh: Shutdown and restart. The controller will shutdown the channel on which the fault occurred, and attempt to restart 20ms later. This will occur continuously until the condition causing the fault has disappeared, or the controller has been disabled.

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7.5.16 Input Under-Voltage Lockout (UVLO)

The TPS53681 may not start converting power, until the power stage input voltage reaches the level specified by VIN_ON.

7.5.16.1 (35h) VIN_ON

The VIN_ON command sets the value of the input voltage, in Volts, at which the unit should start power conversion. This command has two data bytes encoded in linear data format, and must be accessed through Read Word/Write Word transactions. The VIN_ON command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command. The supported range for VIN_ON is from 4.0 V volts to 11.25 Volts.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VINON_EXP					VINON_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VINON_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 43. VIN_ON

表 46. VIN_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VINON_EXP	R	11110b	Linear two's complement exponent, –2. LSB = 0.25 V
10:0	VINON_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

表 47. Acceptable Values of VIN_ON

VIN_ON (hex)	Turn-On Voltage (V)
F010h	4.0
F015h	5.25
F019h	6.25
F01Dh	7.25
F021h	8.25
F025h	9.25
F029h	10.25
F02Dh	11.25

7.5.17 Input Over-Voltage Protection and Response

The TPS53681 provides protection from input transients via the VIN_OV_FAULT_LIMIT and VIN_OV_FAULT_RESPONSE commands.

7.5.17.1 (55h) VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an input overvoltage fault. VIN_OV_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. The VIN_OV_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VIN_OVF_EXP					VIN_OVF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN_OVF_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 44. VIN_OV_FAULT_LIMIT

表 48. VIN_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VIN_OVF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 V
10:0	VIN_OVF_MAN	RW	NVM	Linear two's complement mantissa. Valid values of the mantissa range from 0d to 31d.

7.5.17.2 (56h) VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The VIN_OV_FAULT_RESPONSE command must be accessed through Read Byte transactions. The VIN_OV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

In response to the VIN_OV_LIMIT being exceeded, the device will:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN_OV_FAULT bit in the STATUS_INPUT register
- Notify the host (assert the PMB_ALERT signal, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VI_OVF_RESP							

LEGEND: R/W = Read/Write; R = Read only

図 45. VIN_OV_FAULT_RESPONSE

表 49. VIN_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VI_OVF_RESP	R	00h	00h: Ignore. The controller will set the appropriate status bits, and alert the host, but continue converting power.

7.5.18 Input Undervoltage Protection and Response

The TPS53681 provides protection from input transients via the VIN_UV_FAULT_LIMIT and VIN_UV_FAULT_RESPONSE commands.

7.5.18.1 (59h) VIN_UV_FAULT_LIMIT

The VIN_UV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Under voltage Fault. This fault is masked until the input exceeds the value set by the VIN_ON command for the first time, and the unit has been enabled. VIN_UV_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. The VIN_UV_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN_UVF_EXP					VIN_UVF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN_UVF_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 46. VIN_UV_FAULT_LIMIT

表 50. VIN_UV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VIN_UVF_EXP	RW	NVM	Linear two's complement exponent. See the table of acceptable values below.
10:0	VIN_UVF_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

表 51. Acceptable Values of VIN_UV_FAULT_LIMIT

VIN_UV_FAULT_LIMIT (hex)	VIN UVF Limit (V)
F011h	4.25
F80Bh	5.5
F80Dh	6.5
F80Fh	7.5
F811h	8.5
F813h	9.5
F815h	10.5
F817h	11.5

7.5.18.2 (5Ah) VIN_UV_FAULT_RESPONSE

The VIN_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The VIN_UV_FAULT_RESPONSE command must be accessed through Read Byte transactions. The VIN_UV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

In response to the VIN_UV_LIMIT being exceeded, the device will:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Set the VIN_UV_FAULT bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VI_UVF_RESP							

LEGEND: R/W = Read/Write; R = Read only

図 47. VIN_UV_FAULT_RESPONSE

表 52. VIN_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VI_UVF_RESP	R	C0h	C0h: Shutdown and restart when the fault condition is no longer present.

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7.5.19 Input Overcurrent Protection and Response

Input overcurrent protection is configured via the IIN_OC_FAULT_LIMIT, IIN_OC_WARN_LIMIT and IIN_OC_FAULT_RESPONSE commands.

7.5.19.1 (5Bh) IIN_OC_FAULT_LIMIT

The IIN_OC_FAULT_LIMIT command sets the value of the input current, in amperes, that causes the input over current fault condition. IIN_OC_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. The IIN_OC_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IIN_OCF_EXP					IIN_OCF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IIN_OCF_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 48. IIN_OC_FAULT_LIMIT

表 53. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IIN_OCF_EXP	R	11111b	Linear two's complement format exponent, –1. LSB = 0.5 A.
10:0	IIN_OCF_MAN	RW	See below.	Linear two's complement format mantissa. Acceptable values range from 0d (0 A) to 127d (63.5 A).

During operation, the IIN_OC_FAULT_LIMIT may be changed to any valid value, as specified above. The IIN_OC_FAULT_LIMIT command has only limited NVM backup. The table below summarizes the values that IIN_OC_FAULT_LIMIT may be restored to following a reset, or RESTORE_DEFAULT_ALL operation.

表 54. IIN_OC_FAULT_LIMIT reset values

Hex Value	IIN_OC_FAULT_LIMIT during NVM store operation	IIN_OC_FAULT_LIMIT following Reset/Restore Operation
F810h	8 A	8 A
F820h	16 A	16 A
F830h	24 A	24 A
F840h	32 A	32 A
F850h	40 A	40 A
F860h	48 A	48 A
F870h	56 A	56 A
F87Fh	63.5 A	63.5 A
Any other valid data	Any other valid data	63.5 A

7.5.19.2 (5Dh) IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes the input overcurrent warning condition. The IIN_OC_WARN_LIMIT command must be accessed through Read Word/Write Word transactions. The IIN_OC_WARN_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-current warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN Over-current Warning bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

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15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IIN_OCW_EXP					IIN_OCW_MAN		
7	6	5	4	3	2	1	0
R	RW	RW	RW	RW	RW	RW	RW
IIN_OCW_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 49. IIN_OC_WARN_LIMIT

表 55. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IIN_OCW_EXP	R	11111b	Linear two's complement format exponent, –1. LSB = 0.5 A.
10:0	IIN_OCW_MAN	RW	See below.	Linear two's complement format mantissa. Acceptable values range from 0d (0 A) to 127d (63.5 A).

During operation, the IIN_OC_FAULT_LIMIT may be changed to any valid value, as specified above. The IIN_OC_FAULT_LIMIT command has only limited NVM backup. The table below summarizes the values that IIN_OC_FAULT_LIMIT may be restored to following a reset, or RESTORE_DEFAULT_ALL operation.

表 56. IIN_OC_WARN_LIMIT reset values

Hex Value	IIN_OC_WARN_LIMIT during NVM store operation	IIN_OC_WARN_LIMIT following Reset/Restore Operation
F810h	8 A	8 A
F820h	16 A	16 A
F830h	24 A	24 A
F840h	32 A	32 A
F850h	40 A	40 A
F860h	48 A	48 A
F870h	56 A	56 A
F87Fh	63.5 A	63.5 A
Any other valid data	Any other valid data	63.5 A

7.5.19.3 (5Ch) IIN_OC_FAULT_RESPONSE

The IIN_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an input over-current fault. IIN_OC_FAULT_RESPONSE command must be accessed through Read Byte transactions. The IIN_OC_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the input over-current fault, the controller is latched off, and the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN_OC_FAULT bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT and VR_FAULT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IIN_OC_RESP							

LEGEND: R/W = Read/Write; R = Read only

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図 50. IIN_OC_FAULT_RESPONSE

表 57. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IIN_OC_RESP	R	C0h	C0h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

7.5.20 Over-Temperature Protection and Response

Overtemperature protection is configured via the OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE commands.

7.5.20.1 (4Fh) OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an overtemperature fault condition when the sensed temperature from the external sensor exceeds this limit. The default value is selected inMFR_SPECIFIC_13, using the OTF_DFLT bit. Refer to the device *Technical Reference Manual* for more information. OT_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. OT_FAULT_LIMIT is a paged register. In order to access OT_FAULT_LIMIT command for channel A, PAGE must be set to 00h. In order to access OT_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
OTF_EXP					OTF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 51. OT_FAULT_LIMIT

表 58. OT_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	OTF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 ºC
10:0	OTF_MAN	RW	NVM	Linear two's complement mantissa. The default OT_FAULT_LIMIT is set by the OTF_DFLT bit in MFR_SPECIFIC_13.

7.5.20.2 (51h) OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over-temperature Warning event. OT_WARN_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. OT_WARN_LIMIT is a paged register. In order to access OT_WARN_LIMIT command for channel A, PAGE must be set to 00h. In order to access OT_WARN_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

In response to the OT_WARN_LIMIT being exceeded, the device will:

- Set the TEMPERATURE bit in the STATUS_BYTE
- Set the Over-temperature Warning bit in the STATUS_TEMPERATURE register
- Notify the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

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15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
OTW_EXP					OTW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTW_MAN							

LEGEND: R/W = Read/Write; R = Read only

図 52. OT_WARN_LIMIT

表 59. OT_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	OTF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 ºC
10:0	OTF_MAN	RW	105d	Linear two's complement mantissa. Default = 105 ºC

7.5.20.3 (50h) OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE instructs the device on what action to take in response to an output over-temperature fault. The OT_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions. The OT_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-temperature fault, the controller is latched off, and the following actions are taken:

- Set the TEMPERATURE bit in the STATUS_BYTE
- Set the OT_FAULT bit in the STATUS_TEMPERATURE register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF_RESP							

LEGEND: R/W = Read/Write; R = Read only

図 53. OT_FAULT_RESPONSE

表 60. OT_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OTF_RESP	RW	NVM	80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device. C0h: Shutdown and restart when the fault condition is no longer present.

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7.5.21 Dynamic Phase Shedding (DPS)

The dynamic phase shedding (DPS) feature allows the TPS53681 to dynamically select the number of operational phases for each channel, based on the total output current. This increases the total converter efficiency by reducing unnecessary switching losses when the output current is low enough to be supported by a fewer number of phases, than are available in hardware. The MFR_SPECIFIC_14 and MFR_SPECIFIC_15 commands may be used to configure dynamic phase shedding behavior and thresholds.

The DPS_EN bit in MFR_SPECIFIC_14 may be used to enable or disable dynamic phase shedding. Un-setting (writing to 0b) this bit forces each channel to use the maximum number of available phases, regardless of the output current.

The phase add/drop thresholds, at which phases are added or dropped are configured based on the peak efficiency point per phase. For a given switching frequency/duty cycle, the efficiency of an individual power stage has a "peak" point, at which switching losses become less significant and conduction losses begin to dominate. For a multiphase converter, the optimum efficiency is achieved when all of the power stages operate as close as possible to their peak efficiency point. For example, consider a 4-phase design, with power stages that have a peak efficiency point of 12 A per phase. When the total output current is 25 A, if all four phases were active, each phase would be supplying 6.25 A, and hence would be operating far away from their peak efficiency point. With only two phases active, however, each phase supplies 12.5A, meaning that each power stage is operating close to its peak efficiency point, therefore the total converter efficiency is higher overall.

In order to maintain regulation during severe load transient events, phases may be added immediately whenever the total peak current reaches phase addition thresholds. To prevent chattering, phases are dropped when the total average current falls below phase drop thresholds, after a delay of 85 µs typically. Phases are always added/dropped, in numerical order. For example, phase 3 is added after phase 2, and dropped after phase 4.

The DPS_COURSE_TH bits in MFR_SPECIFIC_15 select the peak efficiency point per phase. Refer to the power stage datasheet to determine the peak efficiency point per phase.

Phase adding thresholds are configured based on the peak efficiency point per phase. Each phase transition has a configurable threshold of 6 A to 12 A above the peak efficiency point. For example, the threshold at which the converter transitions from 2 phases to 3 phases is determined by the DPS_2TO3_FINE_ADD bits in MFR_SPECIFIC_15. When 8 A is selected, the total peak current which causes the third phase to be added is 2 × $I_{EFF(PEAK)}$ + 8 A. See the register descriptions below for more detailed information.

Likewise, phase drop thresholds are configured based on the peak efficiency point per phase. Each phase transition has a configurable threshold of 2A below to 4 A above the peak efficiency point. For example, the threshold at which the converter transitions from 3 phases to 2 phases is determined by the DPS_3TO2_FINE_DROP bits in MFR_SPECIFIC_14. When 0 A is selected, the total average current which causes the third phase to be dropped is 2 × $I_{EFF(PEAK)}$. See the register descriptions below for more detailed information.

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7.5.21.1 (DEh) MFR_SPECIFIC_14

The MFR_SPECIFIC_14 command is used to configure dynamic phase shedding, and compensation ramp amplitude, and dynamic ramp amplitude during USR, and different power states. The MFR_SPECIFIC_14 command must be accessed through Write Word/Read Word transactions.

MFR_SPECIFIC_14 is a paged register. In order to access MFR_SPECIFIC_14 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_14 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
DPS_6TO5_FINE_DROP (PAGE 0 only)		DPS_5TO4_FINE_DROP (PAGE 0 only)		DPS_4TO3_FINE_DROP (PAGE 0 only)		DPS_3TO2_FINE_DROP	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
DPS_EN	DYN_RAMP_USR		DYN_RAMP_2 PH	DYN_RAMP_1 PH	RAMP		

LEGEND: R/W = Read/Write; R = Read only

図 54. MFR_SPECIFIC_14

表 61. MFR_SPECIFIC_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DPS_6TO5_FINE_DROP (PAGE 0 only)	RW	NVM	Dynamic phase drop threshold, fine adjustment, 6 phases to 5 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 5 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 5 × $I_{EFF(PEAK)}$ 10b: Threshold = 5 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 5 × $I_{EFF(PEAK)}$ + 4 A
13:12	DPS_5TO4_FINE_DROP (PAGE 0 only)	RW	NVM	Dynamic phase drop threshold, fine adjustment, 5 phases to 4 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 4 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 4 × $I_{EFF(PEAK)}$ 10b: Threshold = 4 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 4 × $I_{EFF(PEAK)}$ + 4 A
11:10	DPS_4TO3_FINE_DROP (PAGE 0 only)	RW	NVM	Dynamic phase drop threshold, fine adjustment, 4 phases to 3 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 3 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 3 × $I_{EFF(PEAK)}$ 10b: Threshold = 3 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 3 × $I_{EFF(PEAK)}$ + 4 A
9:8	DPS_3TO2_FINE_DROP	RW	NVM	Dynamic phase drop threshold, fine adjustment, 3 phases to 2 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 2 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 2 × $I_{EFF(PEAK)}$ 10b: Threshold = 2 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 2 × $I_{EFF(PEAK)}$ + 4 A

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表 61. MFR_SPECIFIC_14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	DPS_EN	RW	NVM	Enable or Disable Dynamic Phase Shedding 0b: Disable dynamic phase shedding 1b: Enable dynamic phase shedding
6:5	DYN_RAMP_USR	RW	NVM	Dynamic ramp amplitude setting during USR operation. Only applies to USR Level 1. 00b: Equal to the settings in the RAMP bits 01b: 40 mV 10b: 80 mV 11b: 120 mV
4	DYN_RAMP_2PH	RW	NVM	Dynamic ramp amplitude setting during 2 phase operation. 0b: Equal to the settings in the RAMP bits 1b: 120 mV
3	DYN_RAMP_1PH	RW	NVM	Dynamic ramp amplitude setting during 1 phase operation. 0b: Equal to the settings in the RAMP bits 1b: 80 mV
2:0	RAMP	RW	NVM	Ramp amplitude settings. See 表 62.

表 62. Ramp Amplitude Settings

RAMP (binary)	Ramp Amplitude Setting (mV)
000b	40
001b	80
010b	120
011b	160
100b	200
101b	240
110b	280
111b	320

7.5.21.2 (DFh) MFR_SPECIFIC_15

The MFR_SPECIFIC_15 command is used to configure dynamic phase shedding. The MFR_SPECIFIC_15 command must be accessed through Write Word/Read Word transactions.

MFR_SPECIFIC_15 is a paged register. In order to access MFR_SPECIFIC_15 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_15 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
DPS_DCM	DPS_2TO1_FINE_DROP		DPS_5TO6_FINE_ADD (PAGE 0 only)		DPS_4TO5_FINE_ADD (PAGE 0 only)		DPS_3TO4_FINE_ADD (PAGE 0 only)
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
DPS_3TO4_FINE_ADD (PAGE 0 only)	DPS_2TO3_FINE_ADD		DPS_1TO2_FINE_ADD		2TO1_PH_EN	DPS_COURSE_TH	

LEGEND: R/W = Read/Write; R = Read only

図 55. MFR_SPECIFIC_15

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表 63. MFR_SPECIFIC_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DPS_DCM	RW	NVM	Enable DCM mode during 1 phase operation, when higher order phases are dropped due to dynamic phase shedding. 0b: Disable DCM operation during 1 phase operation 1b: Enable DCM operation during 1 phase operation
14:13	DPS_2TO1_FINE_DROP	RW	NVM	Dynamic phase drop threshold, fine adjustment, 2 phases to 1phase. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below. 00b: Threshold = 1× $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 1 × $I_{EFF(PEAK)}$ 10b: Threshold = 1 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 1 × $I_{EFF(PEAK)}$ + 4 A
12:11	DPS_5TO6_FINE_ADD (PAGE 0 only)	RW	NVM	Dynamic phase add threshold, fine adjustment, 5 phases to 6 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below. 00b: Threshold = 5 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 5 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 5 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 5 × $I_{EFF(PEAK)}$ + 12 A
10:9	DPS_4TO5_FINE_ADD (PAGE 0 only)	RW	NVM	Dynamic phase add threshold, fine adjustment, 4 phases to 5 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 4 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 4 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 4 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 4 × $I_{EFF(PEAK)}$ + 12 A
8:7	DPS_3TO4_FINE_ADD (PAGE 0 only)	RW	NVM	Dynamic phase add threshold, fine adjustment, 3 phases to 4 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 3 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 3 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 3 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 3 × $I_{EFF(PEAK)}$ + 12 A
6:5	DPS_2TO3_FINE_ADD	RW	NVM	Dynamic phase add threshold, fine adjustment, 2 phases to 3 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 2 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 2 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 2 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 2 × $I_{EFF(PEAK)}$ + 12 A

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表 63. MFR_SPECIFIC_15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	DPS_1TO2_FINE_ADD	RW	NVM	Dynamic phase add threshold, fine adjustment, 1 phase to 2 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 1 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 1 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 1 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 1 × $I_{EFF(PEAK)}$ + 12 A
3	2TO1_PH_EN	RW	NVM	Enable phase dropping from 2 phases to 1 phase operation. 0b: Disable phase shedding to 1 phase 1b: Enable phase shedding to 1 phase
2:0	DPS_COURSE_TH	RW	NVM	Sets the peak efficiency point per phase. This is used to determine phase add/drop thresholds. 00b: $I_{EFF(PEAK)}$ = 12 A 01b: $I_{EFF(PEAK)}$ = 14 A 10b: $I_{EFF(PEAK)}$ = 16 A 11b: $I_{EFF(PEAK)}$ = 18 A

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7.5.22 NVM Programming

The USER_DATA_00 - USER_DATA_12 commands are provided to streamline NVM programming. These 6-byte block commands are mapped internally to all of the user-configurable parameters the TPS53681 supports. The MFR_SERIAL command also provides a checksum, to streamline verification of desired programming values.

The generalized procedure for programming the TPS53681 is summarized below.

Configure User-Programmable Parameters

1. First, configure all of the user-accessible parameters via the standard PMBus, and Manufacturer Specific commands. TI provides the Fusion Digital Power Designer graphical interface software to streamline this step. The user can also refer to the *Technical Reference Manual* for a full set of register maps for these commands.
2. Once the device is configured as desired, issue the STORE_DEFAULT_ALL command to commit these values to NVM, and update the checksum value. Wait approximately 100 ms after issuing STORE_DEFAULT_ALL before communicating with the device again.
3. Write PAGE to 00h
4. Read-back and Record the value of IC_DEVICE_ID and IC_DEVICE_REV commands
5. Read-back and Record the value of the USER_DATA_00 through USER_DATA_12 commands
6. Read-back and Record the value of the MFR_SERIAL command
7. Read-back and Record the value of VOUT_MAX
8. Write PAGE to 01h
9. Read-back and Record the value of VOUT_MAX

Program and Verify NVM (repeat for each device)

1. Power the device by supplying +3.3V to the V3P3 pin. Power conversion should be disabled for NVM programming.
2. Read-back and verify that IC_DEVICE_ID and IC_DEVICE_REV values match those recorded previously. This ensures that user-parameters being programmed correspond to the same device/revision as previously configured.
3. Write PAGE to 00h.
4. Write the USER_DATA_00 through USER_DATA_12 commands, with the values recorded previously.
5. Write VOUT_MAX (Page 0) with the value recorded previously.
6. Write PAGE to 01h
7. Write VOUT_MAX (Page 1) with the value recorded previously.
8. Issue STORE_DEFAULT_ALL. Wait appx 100 ms after issuing STORE_DEFAULT_ALL before communicating with the device again.
9. Read-back the MFR_SERIAL command, and compare the value to that recorded previously. If the new MFR_SERIAL matches the value recorded previously, NVM programming was successful.

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7.5.23 NVM Security

The MFR_SPECIFIC_42 command can be optionally used to set a password for NVM programming. To prevent a hacker from simply sending the password command with all possible passwords, the TPS53681 goes into a special extra-secure state when an incorrect password is received. In this state, all passwords are rejected, even the valid one. The device must be power cycled to clear this state so that another password attempt may be made. When NVM security is enabled, the TPS53681 will not accept writes to any command other than PAGE and PHASE, which are necessary for reading certain parameters.

Enabling NVM Security

1. Set the NVM password. Write MFR_SPECIFIC_42 to a value other than FFFFh.
2. Issue STORE_DEFAULT_ALL
3. Wait 100ms for the NVM store to complete
4. Power cycle V3P3. NVM Security will be enabled at the next power-up.

Disabling NVM Security

To disable NVM security, use the following procedure:

1. Write the password to MFR_SPECIFIC_42 to disable NVM security. Once the correct password has been given, NVM security will be disabled, and the device will once again accept write transactions to configuration registers.

NVM security will be re-enabled at the next power-on, unless MFR_SPECIFIC_42 is set to FFFFh (NVM Security Disabled), and an NVM store operation (issue STORE_DEFAULT_ALL and wait 100 ms) is performed.

Determining Whether NVM Security is Active

Reads to the MFR_SPECIFIC_42 command returns one of three values:

- 0000h = NVM Security is Disabled
- 0001h = NVM Security is Enabled
- 0002h = MFR_SPECIFIC_42 is locked due to incorrect password entry

7.5.23.1 (FAh) MFR_SPECIFIC_42

MFR_SPECIFIC_42 is used for NVM Security. The MFR_SPECIFIC_42 command must be accessed through Read Word/Write Word transactions.

MFR_SPECIFIC_42 is a shared register. Write transactions to this register will apply to both channels, and read transactions to this register returns the same data regardless of the current PAGE.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
NVM_SECURITY_KEY							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
NVM_SECURITY_KEY							

LEGEND: R/W = Read/Write; R = Read only

図 56. MFR_SPECIFIC_42

表 64. MFR_SPECIFIC_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_SECURITY_KEY	RW	NVM	16 bit code for NVM security key.

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7.5.24 Black Box Recording

The TPS53681 provides a "black box" feature to aid in system-level debugging. According to the PMBus specification, status bits are latched whenever the condition causing them occurs, regardless of whether or not other status bits are already set. This, however, makes it difficult for the system designer to understand which fault condition occurred first, in the case that one fault condition causes others to trigger. The MFR_SPECIFIC_08 command provides a "snapshot" of the first faults to occur chronologically, for each channel, which may be stored to NVM, for future debugging. Only the most catastrophic fault conditions are logged, such as the over-voltage fault, over-current fault, and power stage failure. The black box command may also be reset, or cleared by writing 00h to the register, and storing to NVM if the NVM value must also be cleared.

Resetting the Black Box Record

Resetting the record allows the user to determine which faults occur first, *after* the register is cleared. To clear the record, write 00h to MFR_SPECIFIC_08, and issue STORE_DEFAULT_ALL.

Triggering Black Box Recording

Black box recording is always active, whether or not the TPS53681 is converting power. Note however many of the critical faults summarized in MFR_SPECIFIC_08 are only possible to trigger during power conversion. Whenever any of the following catastrophic faults occur, the MFR_SPECIFIC_08 register will be updated according to the register description below, but only if the black box record has been cleared since the last catastrophic faults occurred. Faults logged include:

- Overvoltage Fault (Device was Converting Power)
- Overvoltage Fault (Device was not Converting Power)
- Input Overcurrent Fault
- Output Overcurrent Fault
- Power Stage Fault
- Input Over-Power Fault

Retrieving the Black Box Record

Reading the MFR_SPECIFIC_08 returns the current value of the Black Box record. If the register reads 00h, no catastrophic faults have occurred since the record was last cleared. If any value other than 00h is stored in the register, then de-code the value according to the register description below. In order to read-back the black box record following a power-down, the STORE_DEFAULT_ALL command must be issued, to store the contents of the black box record to NVM.

7.5.24.1 (D8h) MFR_SPECIFIC_08

The MFR_SPECIFIC_08 command is used to identify catastrophic faults which occur first, and store this information to NVM. The MFR_SPECIFIC_08 command must be accessed through Write Byte/Read Byte transactions. MFR_SPECIFIC_08 is a shared register. Transactions to this register do not require specific PAGE settings. However, note that channels A and B have independent bit fields within the command.

7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
0	0	CF_CHB			CF_CHA		

LEGEND: R/W = Read/Write; R = Read only

図 57. MFR_SPECIFIC_08

表 65. MFR_SPECIFIC_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Not used	R	0	Not used and set to 0.
5:3	CF_CHB	RW	NVM	Catastrophic fault record for channel B.
2:0	CF_CHA	RW	NVM	Catastrophic fault record for channel A.

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Whenever a catastrophic fault occurs, the first event detected will trigger the MFR_SPECIFIC_08 command to update according to the tables below. This recording happens independently for channel A and channel B. If the PMBus host issues a STORE_DEFAULT_ALL, this information will be committed to NVM, and may be retrieved at a later time. In order to clear the record for either channel, the PMBus host must write the corresponding bits (CF_CHA for channel A, CF_CHB for channel B) to 000b, and issue STORE_DEFAULT_ALL.

Attempts to write any non-zero value to this command will be treated as invalid data - data will be ignored, the appropriate flags in STATUS_CML, and STATUS_WORD, will be set, and the PMB_ALERT pin will be asserted to notify the host of the invalid transaction.

表 66. Catastrophic Fault Recording Interpretation

CF_CHA / CF_CHB (binary)	Interpretation
000b	No fault occurred
001b	OVF occurred, power conversion was disabled
010b	OVF occurred, power conversion was enabled
011b	IIN Overcurrent fault occurred
100b	IOUT Overcurrent fault occurred
101b	Overtemperature fault occurred
110b	Power stage fault occurred
111b	Input overpower warning occurred

7.5.25 Board Identification and Inventory Tracking

The TPS53681 provides several bytes of arbitrarily programmable NVM-backed memory to allow for inventory management and board identification. By default, these values reflect information about the date/revision of the TPS53681 device being used itself. However, they may be re-programmed by the user, at the board level during manufacturing. This provides a convenient and easy to use method of tracking boards, revisions and manufacturing dates. The following commands are provided for this purpose:

- MFR_ID - 16 bits of NVM for end-users to track the PCB/power supply supplier name
- MFR_MODEL - 16 bits of NVM for tracking the manufacturer model number
- MFR_REVISION - 16 bits of NVM for tracking PCB/power supply revision code
- MFR_DATE - 16 bits of NVM for tracking PCB manufacturing date code

7.5.25.1 (9Ah) MFR_MODEL

The MFR_MODEL command is used to either set or read the manufacturer's model number.

The MFR_MODEL command must be accessed through Block Write/Block Read transactions.

The MFR_MODEL command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_MODEL							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_MODEL							

LEGEND: R/W = Read/Write; R = Read only

図 58. MFR_MODEL

表 67. MFR_MODEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_MODEL	RW	NVM	Arbitrary 16 bits with NVM backup for Model number identification

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7.5.25.2 (9Bh) MFR_REVISION

The MFR_REVISION command is used to either set or read the manufacturer's revision number

The MFR_REVISION command must be accessed through Block Write/Block Read transactions.

The MFR_REVISION command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_REV							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_REV							

LEGEND: R/W = Read/Write; R = Read only

図 59. MFR_REVISION

表 68. MFR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_REV	RW	NVM	Arbitrary 16 bits with NVM backup for revision number identification

7.5.25.3 (9Dh) MFR_DATE

The MFR_DATE command is used to either set or read the manufacturing date.

The MFR_DATE command must be accessed through Block Write/Block Read transactions.

The MFR_DATE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
MFR_DATE							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_DATE							

LEGEND: R/W = Read/Write; R = Read only

図 60. MFR_DATE

表 69. MFR_DATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_DATE	RW	NVM	Arbitrary 16 bits with NVM backup for manufacture date identification

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7.5.26 Status Reporting

The TPS53681 provides several registers containing status information. The flags in these registers are latched whenever their corresponding condition occurs, and are not cleared until either the CLEAR_FAULTS command is issued, or the host writes a value of 1b to that bit location. Register maps for the all of the supported status registers are shown in the following sections.

7.5.26.1 (78h) STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, such as over-voltage, overcurrent, over-temperature, etc.

The STATUS_BYTE command must be accessed through Read Byte transactions. STATUS_BYTE is a paged register. In order to access STATUS_BYTE command for channel A, PAGE must be set to 00h. In order to access STATUS_BYTE register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
0	R	R	R	R	R	R	R
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER

図 61. STATUS_BYTE

表 70. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0	Not supported and always set to 0.
6	OFF	R	Current Status	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	Current Status	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	Current Status	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	Current Status	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	Current Status	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	Current Status	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	Current Status	Other Fault (None of the Above) This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. However, the bits in the STATUS_BYTE are summary bits only and reflect the status of corresponding bits in STATUS_VOUT, STATUS_IOUT, etc... To clear these bits individually, the user must clear them by writing to the corresponding STATUS_X register. For example: the output overcurrent fault sets the IOUT_OC bit in STATUS_BYTE, and the IOUT_OC_FLT bit in STATUS_IOUT. Writing a 1 to the IOUT_OC_FLT bit in STATUS_IOUT clears the fault in both STATUS_BYTE and STATUS_IOUT. Writes to STATUS_BYTE itself will be treated as invalid transactions.

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7.5.26.2 (79h) STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of critical faults, such as over-voltage, overcurrent, over-temperature, etc..

The STATUS_WORD command must be accessed through Read Word transactions. STATUS_WORD is a paged register. In order to access STATUS_WORD command for channel A, PAGE must be set to 00h. In order to access STATUS_WORD register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT	IOUT	INPUT	MFR	PGOOD	FANS	OTHER	UNKNOWN
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER

図 62. STATUS_WORD

表 71. STATUS_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VOUT	R	Current Status	Output Voltage Fault/Warning. Refer to STATUS_VOUT for more information. 0: Latched flag indicating no VOUT fault or warning has occurred. 1: Latched flag indicating a VOUT fault or warning has occurred.
14	IOUT	R	Current Status	Output Current Fault/Warning. Refer to STATUS_IOUT for more information. 0: Latched flag indicating no IOUT fault or warning has occurred. 1: Latched flag indicating an IOUT fault or warning has occurred.
13	INPUT	R	Current Status	Input Voltage/Current Fault/Warning. Refer to STATUS_INPUT for more information. 0: Latched flag indicating no VIN or IIN fault or warning has occurred. 1: Latched flag indicating a VIN or IIN fault or warning has occurred.
12	MFR	R	Current Status	MFR_SPECIFIC Fault. Refer to STATUS_MFR for more information. 0: Latched flag indicating no MFR_SPECIFIC fault has occurred. 1: Latched flag indicating a MFR_SPECIFIC fault has occurred.
11	PGOOD	R	Current Status	Power Good Status. Note: Per the PMBus specification, the PGOOD bit is not latched, always reflecting the current status of the AVR_RDY/BVR_RDY pin. 0: Raw status indicating AVR_RDY/BVR_RDY pin is at logic high. 1: Raw status indicating AVR_RDY/BVR_RDY pin is at logic low.
10	FANS	R	0	Not supported and always set to 0.
9	OTHER	R	0	Not supported and always set to 0.
8	UNKNOWN	R	0	Not supported and always set to 0.
7	BUSY	R	0	Not supported and always set to 0.
6	OFF	R	Current Status	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	Current Status	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	Current Status	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.

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表 71. STATUS_WORD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	VIN_UV	R	Current Status	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	Current Status	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	Current Status	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	Current Status	Other Fault (None of the Above) This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. However, the bits in the STATUS_WORD are summary bits only and reflect the status of corresponding bits in STATUS_VOUT, STATUS_IOUT, etc... To clear these bits individually, the user must clear them by writing to the corresponding STATUS_X register. For example: the output overcurrent fault sets the IOUT_OC bit in STATUS_WORD, and the IOUT_OC_FLT bit in STATUS_IOUT. Writing a 1 to the IOUT_OC_FLT bit in STATUS_IOUT clears the fault in both STATUS_WORD and STATUS_IOUT. Writes to STATUS_WORD will be treated as invalid transactions.

7.5.26.3 (7Ah) STATUS_VOUT

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.

The STATUS_VOUT command must be accessed through Read Byte/Write Byte transactions. STATUS_VOUT is a paged register. In order to access STATUS_VOUT command for channel A, PAGE must be set to 00h. In order to access STATUS_VOUT register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	0	0	RW	RW	0	0	0
VOUT_OVF	VOUT_OVW	VOUT_UVW	VOUT_UVF	VOUT_MIN_MAX	TON_MAX	TOFF_MAX	VOUT_TRACK

図 63. STATUS_VOUT

表 72. STATUS_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VOUT_OVF	RW	Current Status	Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred.
6	VOUT_OVW	R	0	Not supported and always set to 0.
5	VOUT_UVW	R	0	Not supported and always set to 0.
4	VOUT_UVF	RW	Current Status	Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred.

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表 72. STATUS_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	VOUT_MIN_MAX	RW	Current Status	Output Voltage Max/Min Exceeded Warning 0: Latched flag indicating no VOUT_MAX/VOUT_MIN warning has occurred. 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX/VOUT_MIN command.
2	TON_MAX	R	0	Not supported and always set to 0.
1	TOFF_MAX	R	0	Not supported and always set to 0.
0	VOUT_TRACK	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.26.4 (7Bh) STATUS_IOUT

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.

The STATUS_IOUT command must be accessed through Read Byte/Write Byte transactions. STATUS_IOUT is a paged register. In order to access STATUS_IOUT command for channel A, PAGE must be set to 00h. In order to access STATUS_IOUT register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	0	RW	0	RW	0	0	0
IOUT_OCF	IOUT_OCUVF	IOUT_OCW	IOUT_UCF	CUR_SHAREF	POW_LIMIT	POUT_OPF	POUT_OPW

図 64. STATUS_IOUT

表 73. STATUS_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IOUT_OCF	RW	Current Status	Output Over-Current Fault 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating a IOUT OC fault has occurred .
6	IOUT_OCUVF	R	0	Not supported and always set to 0.
5	IOUT_OCW	RW	Current Status	0: Latched flag indicating no IOUT OC warning has occurred 1: Latched flag indicating a IOUT OC warning has occurred
4	IOUT_UCF	R	0	Not supported and always set to 0.
3	CUR_SHAREF	RW	Current Status	0: Latched flag indicating no current sharing fault has occurred 1: Latched flag indicating a current sharing fault has occurred
2	POW_LIMIT	R	0	Not supported and always set to 0.
1	POUT_OPF	R	0	Not supported and always set to 0.
0	POUT_OPW	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.26.5 (7Ch) STATUS_INPUT

The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.

The STATUS_INPUT command must be accessed through Read Byte/Write Byte transactions. The STATUS_INPUT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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7	6	5	4	3	2	1	0
RW	0	0	RW	RW	RW	RW	RW
VIN_OVF	VIN_OVW	VIN_UVW	VIN_UVF	LOW_VIN	IIN_OCF	IIN_OCW	PIN_OPW

図 65. STATUS_INPUT Register

表 74. STATUS_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVF	R	Current Status	Input Over-Voltage Fault 0: Latched flag indicating no VIN OV fault has occurred. 1: Latched flag indicating a VIN OV fault has occurred.
6	VIN_OVW	R	0	Not supported and always set to 0.
5	VIN_UVW	R	0	Not supported and always set to 0.
4	VIN_UVF	R	Current Status	Input Under-Voltage Fault 0: Latched flag indicating no VIN UV fault has occurred. 1: Latched flag indicating a VIN UV fault has occurred.
3	LOW_VIN	R	Current Status	Unit Off for insufficient input voltage 0: Latched flag indicating no LOW_VIN fault has occurred. 1: Latched flag indicating a LOW_VIN fault has occurred
2	IIN_OCF	R	Current Status	Input Over-Current Fault 0: Latched flag indicating no IIN OC fault has occurred. 1: Latched flag indicating a IIN OC fault has occurred.
1	IIN_OCW	R	Current Status	Input Over-Current Warning 0: Latched flag indicating no IIN OC warning has occurred. 1: Latched flag indicating a IIN OC warning has occurred.
0	PIN_OPW	R	Current Status	Input Over-Power Warning 0: Latched flag indicating no input over-power warning has occurred. 1: Latched flag indicating a input over-power warning has occurred.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.26.6 (7Dh) STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter's temperature related faults.

The STATUS_TEMPERATURE command must be accessed through Read Byte/Write Byte transactions. STATUS_TEMPERATURE is a paged register. In order to access STATUS_TEMPERATURE command for channel A, PAGE must be set to 00h. In order to access STATUS_TEMPERATURE register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	RW	0	0	0	0	0	0
OTF	OTW	UTW	UTF	Reserved			

図 66. STATUS_TEMPERATURE Register

表 75. STATUS_TEMPERATURE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTF	RW	Current Status	Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	RW	Current Status	Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.

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表 75. STATUS_TEMPERATURE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	UTW	R	0	Not supported and always set to 0.
4	UTF	R	0	Not supported and always set to 0.
3-0	Reserved	R	0000	Always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.26.7 (7Eh) STATUS_CML

The STATUS_CML command returns one byte with contents regarding communication, logic, or memory conditions.

The STATUS_CML command must be accessed through Read Byte/Write Byte transactions. The STATUS_CML command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	0	0	RW	0
IV_CMD	IV_DATA	PEC_FAIL	MEM	PRO_FAULT	Reserved	COM_FAIL	CML_OTHER

図 67. STATUS_CML Register

表 76. STATUS_CML Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IV_CMD	RW	Current Status	Invalid or Unsupported Command Received 0: Latched flag indicating no invalid or unsupported command has been received. 1: Latched flag indicating an invalid or unsupported command has been received.
6	IV_DATA	RW	Current Status	Invalid or Unsupported Data Received 0: Latched flag indicating no invalid or unsupported data has been received. 1: Latched flag indicating an invalid or unsupported data has been received.
5	PEC_FAIL	RW	Current Status	Packet Error Check Failed 0: Latched flag indicating no packet error check has failed 1: Latched flag indicating a packet error check has failed
4	Reserved	R	0	Always set to 0.
3	MEM	RW	Current Status	Memory/NVM Error 0: Latched flag indicating no memory error has occurred 1: Latched flag indicating a memory error has occurred
2	Reserved	R	0	Always set to 0.
1	COM_FAIL	RW	Current Status	Other Communication Faults 0: Latched flag indicating no communication fault other than the ones listed in this table has occurred. 1: Latched flag indicating a communication fault other than the ones listed in this table has occurred.
0	CML_OTHER	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

7.5.26.8 (80h) STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns one byte containing manufacturer-defined faults or warnings.

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The STATUS_MFR_SPECIFIC command must be accessed through Read Byte/Write Byte transactions. STATUS_MFR_SPECIFIC is a paged register. In order to access STATUS_MFR_SPECIFIC command for channel A, PAGE must be set to 00h. In order to access STATUS_MFR_SPECIFIC register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

図 68. STATUS_MFR_SPECIFIC Register

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	0	0	RW
FLT_PS	VSNS_OPEN	MAX_PH_WARN	TSNS_LOW	RST_VID (Page 0)	Reserved		PHFLT

表 77. STATUS_MFR_SPECIFIC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MFR_FAULT_PS	RW	Current Status	Power Stage Fault 0b: Latched flag indicating no fault from TI power stage has occurred. 1b: Latched flag indicating a fault from TI power stage has occurred.
6	VSNS_OPEN	RW	Current Status	VSNS pin open 0b: Latched flag indicating VSNS pin was not open at power-up. 1b: Latched flag indicating VSNS pin was open at power-up.
5	MAX_PH_WARN	RW	Current Status	Maximum Phase Warning If the selected operational phase number is larger than the maximum available phase number specified by the hardware, then MAX_PH_WARN is set, and the operational phase number is changed to the maximum available phase number. 0b: Latched flag indicating no maximum phase warning has occurred. 1b: Latched flag indicating a maximum phase warning has occurred.
4	TSNS_LOW	RW	Current Status	0b: Latched flag indicating that TSEN < 150 mV before soft-start. 1b: Latched flag indicating that TSEN ≥ 150 mV before soft-start.
3	RST_VID (Page 0)	RW	Current Status	RST_VID (Page 0 only) 0b: A VID reset operation has NOT occurred 1b: A VID reset operation has occurred
2:1	Reserved	R	00b	Always set to 0.
0	PHFLT	RW	Current Status	Phase current share fault. The PHFLT bit is set if any phase has current imbalance warnings occurring repetitively for 7 detection cycles (~500 µs continuously). Phases with current imbalance warnings may be read back via MFR_SPECIFIC_03. 0b: No repetitive current share fault has occurred 1b: Repetitive current share fault has occurred

Per the description in the PMBus 1.3 specification, part II, TPS53681 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

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8 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53681 device has a very simple design procedure. All programmable parameters can be configured by PMBus and stored in NVM as the new default values to minimize external component count. This design describes a typical 6-phase, 0.9-V, 300-A application and 2-phase 0.8-V, 90-A application.

8.2 Typical Application

8.2.1 6-phase, 0.9-V, 300-A Application and 2-phase 0.8-V, 90-A Application

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8.2.1.1 Schematic

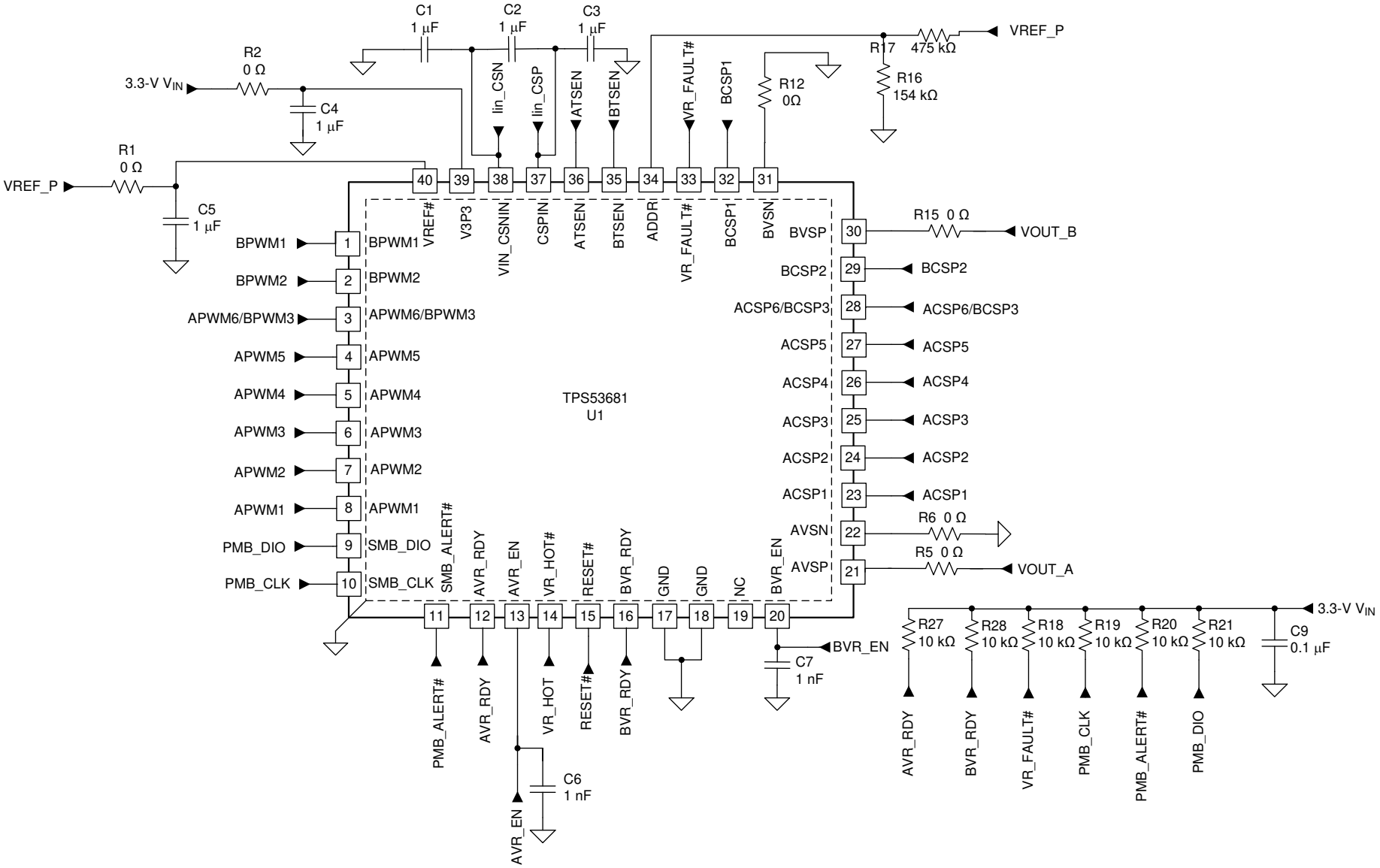


Figure 69. 6-Phase + 2-Phase Application

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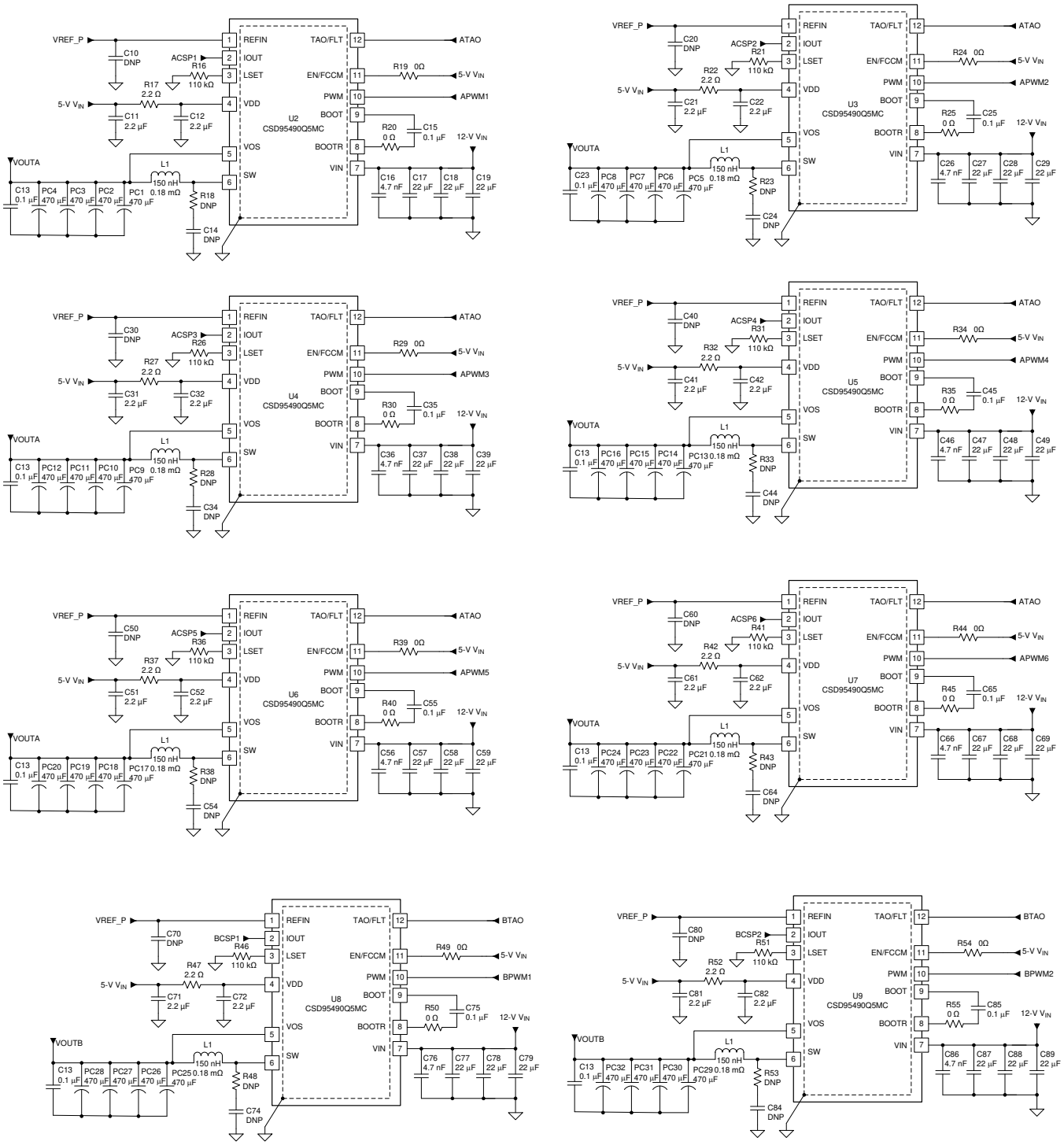


Figure 70. Power Stage

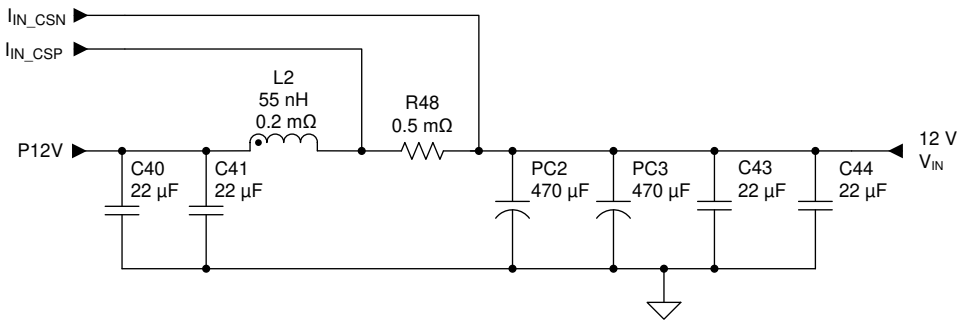


Figure 71. 12-V Input Filter

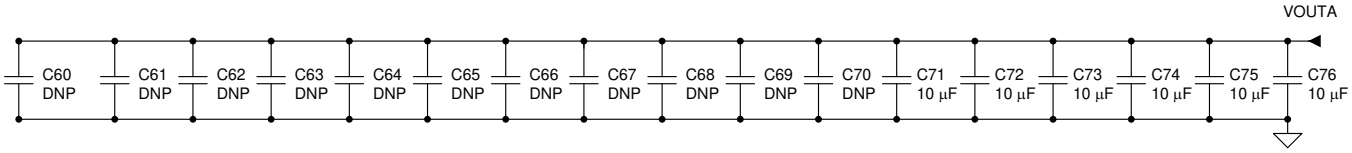


Figure 72. VOUTA Filter for a 6-Phase Application

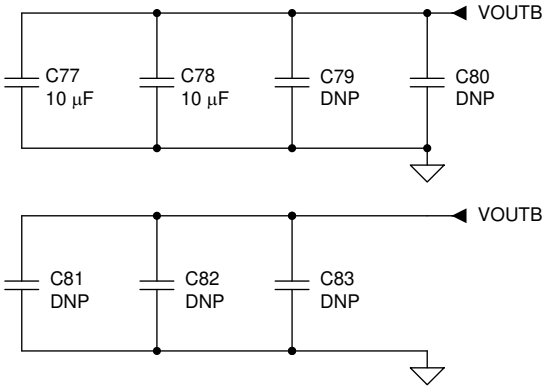


Figure 73. VOUTB Filter for a 2-Phase Application

8.2.1.2 Design Requirements

Table 78. Target Application Specifications

	VOUTA	VOUTB
Number of phases	6	2
Input voltage range	10.8 V – 13.2 V	
Output voltage	0.9 V	0.8 V
I_{OUT}	300 A	90 A
$I_{DYN(max)}$	150 A	45 A
Load-line	0 mΩ	0 mΩ
Fast slew rate (min)	10 mV/µs	
Boot voltage, V_{BOOT}	0.9 V	0.8 V
Maximum temperature, T_{MAX}	90°C	
PMBus Address	1100000 (C0h)	
Switching frequeny (f_{SW})	500 kHz	

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8.2.1.3 Detailed Design Procedure

The following steps illustrate how to configure and fine-tune via PMBus and stored in NVM as the new default setting.

8.2.1.3.1 Choose Inductor

Smaller inductance values yield better transient performance, but also have a higher ripple and lower efficiency. Higher inductance values have the opposite characteristics. It is common practice to limit the ripple current to between 30% and 45% of the maximum per-phase current. In this design example, 30% of the maximum per-phase current is used.

$$I_{P-P} = \frac{I_{OUT}}{n} \times 30\% = \frac{300\ A}{6} \times 0.3 = 15\ A \quad (4)$$

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{I_{P-P}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{13.2\ V - 0.9\ V}{15\ A} \times \frac{0.9\ V}{13.2\ V} \times \frac{1}{500\ kHz} = 0.112\ \mu H \quad (5)$$

A standard inductor value of 150 nH with 0.18 mΩ DCR is chosen. With the same design procedure, the inductor value for the Rail B (V_{OUTB}) of 150 nH is chosen.

8.2.1.3.2 Select the Per-Phase Valley Current Limit

Equation 6 shows the calculation of the per-phase, valley current limit based on the maximum processor current, the operating phase number and the per-phase current ripple I_{P-P}.

$$I_{OCL} = \left(k \times \frac{I_{OUT}}{n}\right) - \left(\frac{I_{P-P}}{2}\right) = 150\% \times \frac{300\ A}{6} - \left(\frac{15\ A}{2}\right) = 67.5A \quad (6)$$

where

- k is the maximum operating margin
- I_{OUT} is the maximum processor current
- I_{P-P} is the ripple current
- n is the number of phases

The factor k of 150% is used to avoid reaching current limits during transients. For this design, a 70-A valley current limit is selected in PMBus GUI.

$$I_{SAT} = I_{OCL} + I_{P-P} = 70\ A + 15\ A = 85A \quad (7)$$

Equation 7 indicates that the maximum saturation current for the inductor needs to be higher than 85 A. Using the same design procedure, the valley current limit for Channel B is selected to be 80 A.

8.2.1.3.3 Set the Maximum Temperature Level (T_{MAX})

For this design, T_{MAX} is selected as 90°C. The temperature is sensed by the ATSEN and BTSEN pins through its connection to the xTAO pins of each phase of the CSD95490Q5MC. The controller reports the highest temperature sensed by power stages of Rail A and Rail B.

8.2.1.3.4 Set USR Thresholds to Improve Load Transient Performance

There are two levels of undershoot reduction protection (USR) (USR1/USR2) selection. USR1 enables up to 3 or 4 phases and USR2 enables up to the maximum number of phases. The initial setting of the USR threshold is to start with USR1 and USR2 as OFF, and then to meet the load insertion transient requirement by lowering the threshold to enable pulse-overlap during the load transients.

For this design, VOUTA USR1 is selected as 240 mV and USR2 is selected as 300 mV. VOUTB USR1 and USR2 are selected as OFF.

8.2.1.4 Inductor DCR and Shunt Current Sensing Design for Input Power

This section describes designing the thermal compensation network. The NTC thermistor is used to compensate thermal variations in the resistance of the inductor winding. The winding is usually copper. And as such has a resistance coefficient of 3900 PPM/°C. Alternatively, the NTC thermistor characteristic is very non-linear and requires two or three resistors to linearize them over the range of interest. Figure 74 shows a typical DCR circuit.

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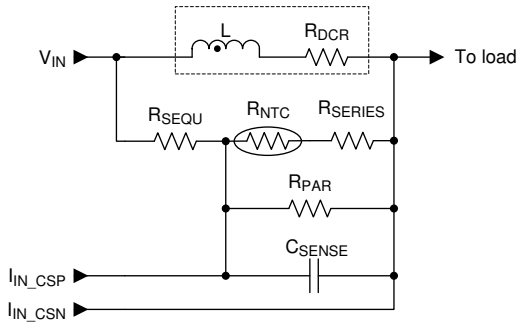


Figure 74. Typical DCR Current Sensing Circuit

Equation 8 calculates the voltage across the C_{SENSE} capacitor when it exactly equals the voltage across R_{DCR}.

$$C_{SENSE} \times R_{EQ} = \frac{L}{R_{DCR}} \quad (8)$$

where

- R_{EQ} is the series/parallel combination of R_{SEQU}, R_{NTC}, R_{SERIES} and R_{PAR}

$$R_{EQ} = \frac{R_{P_N} \times R_{SEQU}}{R_{P_N} + R_{SEQU}} \quad (9)$$

$$R_{P_N} = \frac{R_{PAR} \times (R_{NTC} + R_{SERIES})}{R_{PAR} + R_{NTC} + R_{SERIES}} \quad (10)$$

Ensure that C_{SENSE} is a capacitor type which is stable over temperature, use X7R or better dielectric (C0G preferred). Because calculating these values by hand can be time-consuming, TI offers a spreadsheet using the Excel Solver function available to provide calculation assistance. Contact your local TI representative to get a copy of the spreadsheet.

This example uses a simple design process to enable input shunt sensing, so no DCR network is needed. Insert a 0.5-mΩ shunt resistor in series between the input inductor and the input bulk capacitors.

8.2.1.4.1 Compensation Design

Figure 75 shows the compensation block diagram of the DCAP+ architecture.

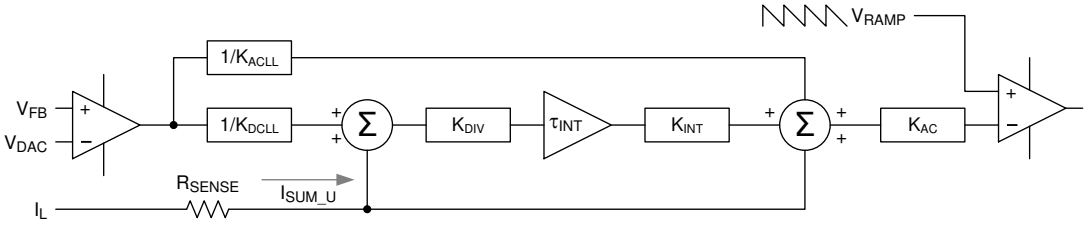


Figure 75. DCAP+ Compensation Block Diagram

- R_{SENSE}: typical 5 mΩ which is gain from power stage
- K_{DCLL}: DC load line which is adjustable from 0 mΩ to 3.125 mΩ
- K_{ACLL}: AC load line which is adjustable from 0.5 mΩ to 3.125 mΩ
- K_{DIV}: not be adjustable. Changing DCLL, this parameter changes automatically
- τ_{INT}: Integrator time constant which is adjustable from 01 µs to 08 µs (scale = 1 µs) and from 10 µs to 40 µs (scale = 5 µs)
- K_{INT}: Integrator time gain which can be adjustable from 0.5×, 0.66×, 1×, 2×
- K_{AC}: AC gain which is adjustable from 0.5×, 1×, 1.5×, 2×

For this design, Table 79 lists the default values that are preset into the PMBus GUI.

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Table 79. PMBus GUI Default Values

	VOUTA	VOUTB
AC_gain	2×	
AC_LL	0.5 mΩ	
INT_Time	01 µs	10 µs
INTGAIN	2×	

8.2.1.4.2 Set PMBus Addresses

To communicate with other system controllers with the PMBus interfaces, use the values of R16 and R17 resistors to set the PMBus address.

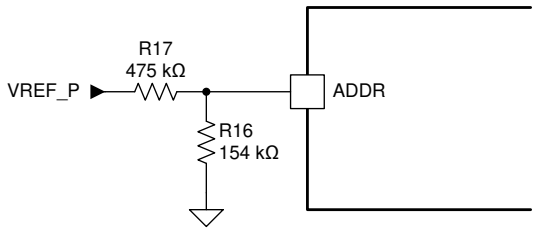


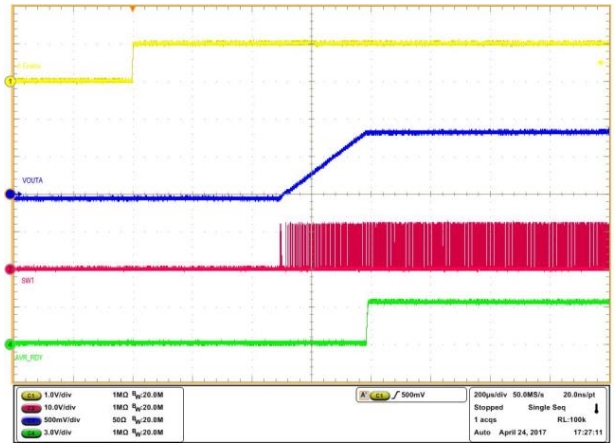
Figure 76. PMBus Address Setting

Contact your local Texas Instruments representative for a copy of PMBus address setting design tool spreadsheet.

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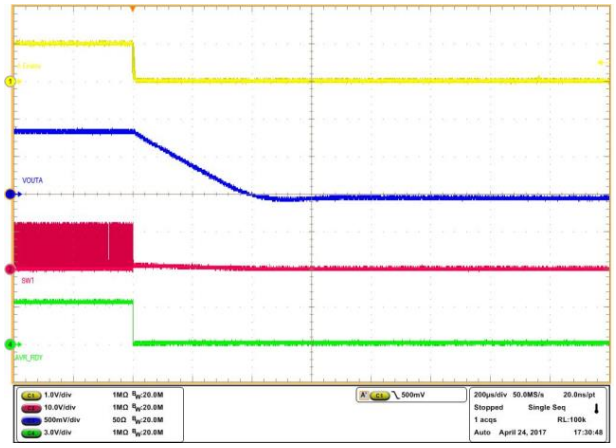
8.2.1.5 Application Performance Plots

For this design, choose 500 kHz for the switching frequency. The frequency is an approximate frequency and is expected to vary based on load and input voltage.



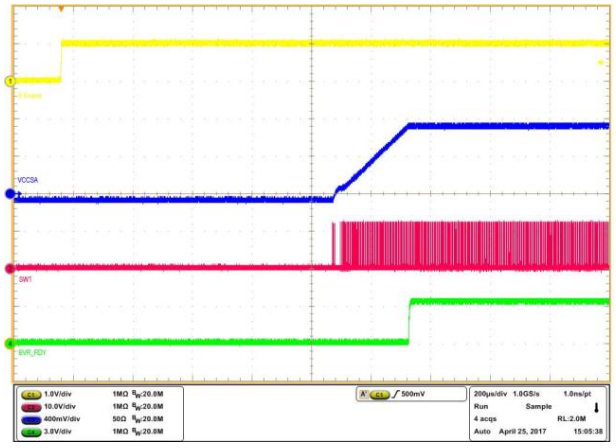
V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUTA} = 10 A

Figure 77. VOUT_A Enable Start-up



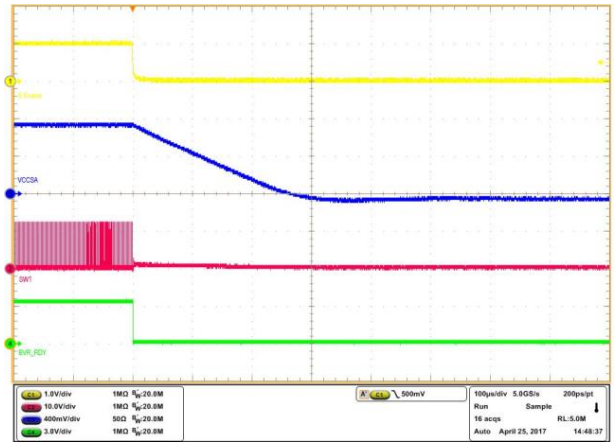
V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUTA} = 10 A

Figure 78. VOUT_A Enable Shut-down



V_{VIN} = 12 V V_{VOUT_B} = 0.8 V
I_{OUTB} = 10 A

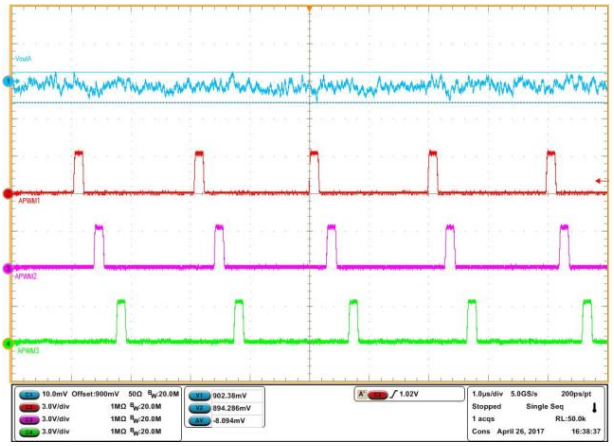
Figure 79. VOUT_B Enable Start-up



V_{VIN} = 12 V V_{VOUT_B} = 0.8 V
I_{OUTB} = 10 A

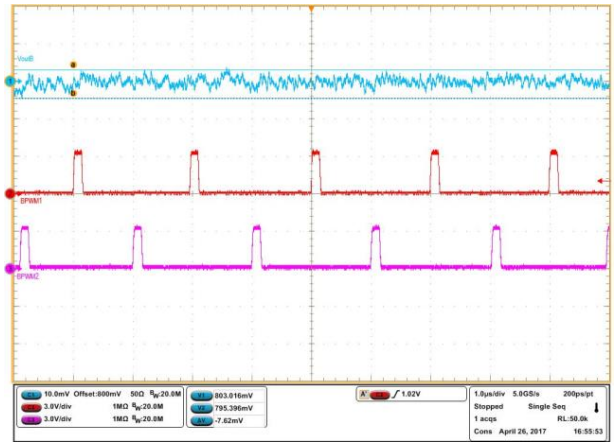
Figure 80. VOUT_B Enable Shut-down

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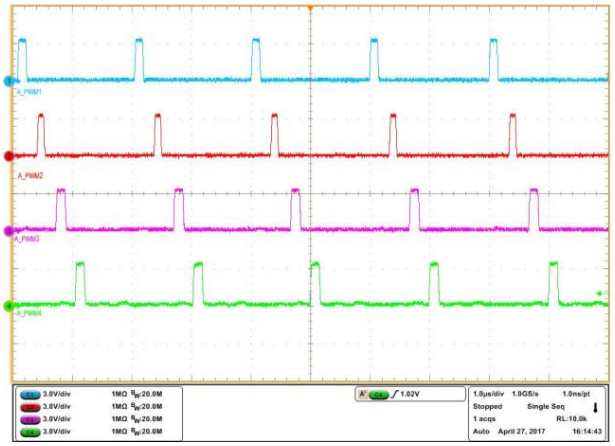
V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUTA} = 30 A

Figure 81. Output Voltage (VOUTA) Ripple



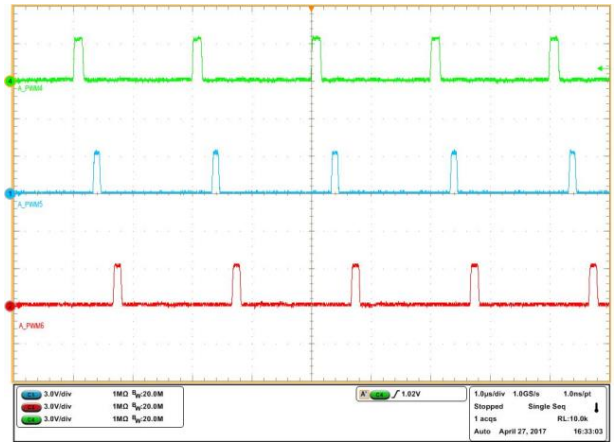
V_{VIN} = 12 V V_{VOUT_B} = 0.8 V
I_{OUT_B} = 30 A

Figure 82. Output Voltage (VOUTB) Ripple



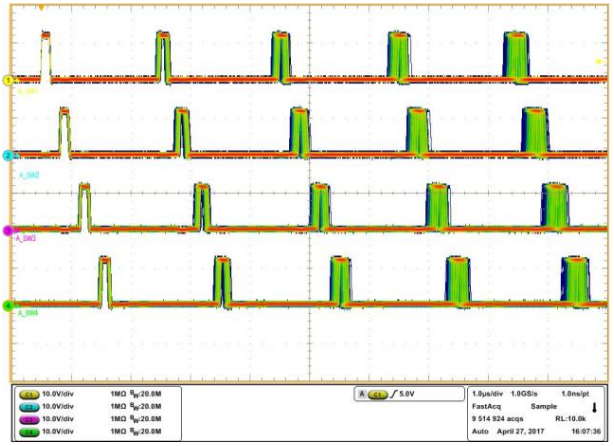
V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUT_A} = 10 A

Figure 83. VOUTA PWM Interleaving (Phases 1-4)



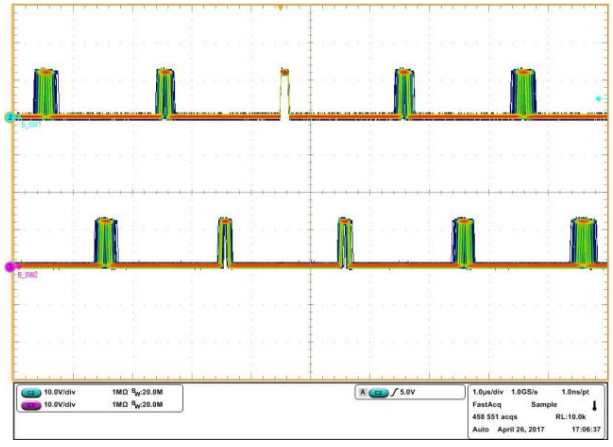
V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUT_A} = 10 A

Figure 84. VOUTA PWM Interleaving (Phases 4-6)



V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUT_A} = 10 A

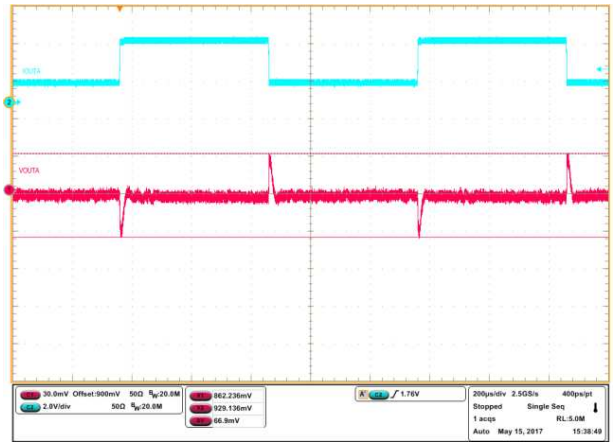
Figure 85. VOUTA PWM Jitter



V_{VIN} = 12 V V_{VOUT_B} = 0.8 V
I_{OUT_B} = 10 A

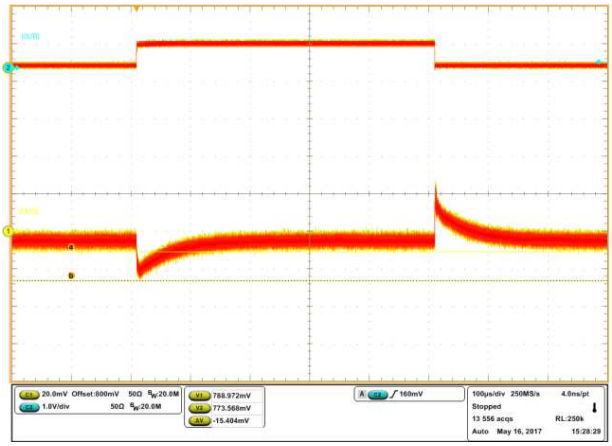
Figure 86. VOUTB PWM Jitter

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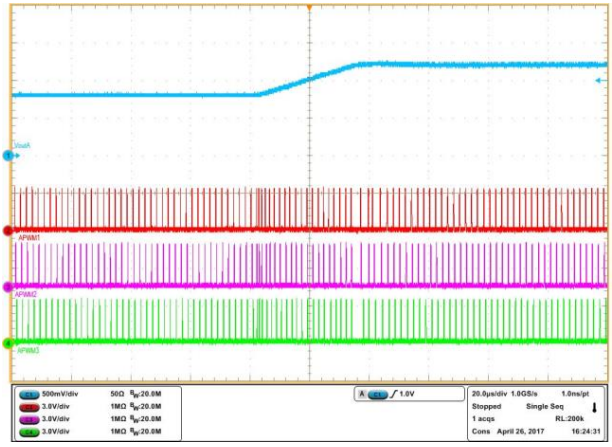
V_{VIN} = 12 V V_{VOUT_A} = 0.9 V
I_{OUT_A} from 150 A to 300 A
Slew rate = 100 A/µs

Figure 87. VOUTA Transient Response



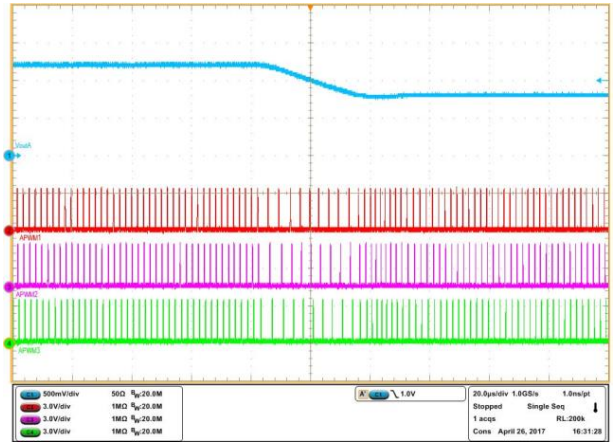
V_{VIN} = 12 V V_{VOUT_B} = 0.8 V
I_{OUT_B} from 1 A to 41 A
Slew rate = 100 A/µs

Figure 88. VOUTB Transient Response



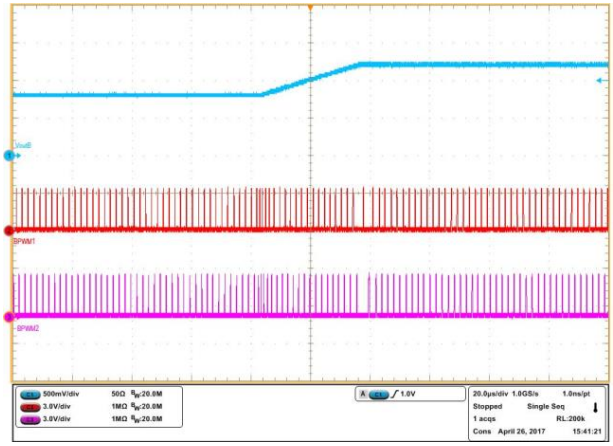
V_{VIN} = 12 V I_{VOUT_A} = 30 A
V_{OUT_A} VID step from 0.8 V to 1.2 V

Figure 89. VOUTA VID-up Change



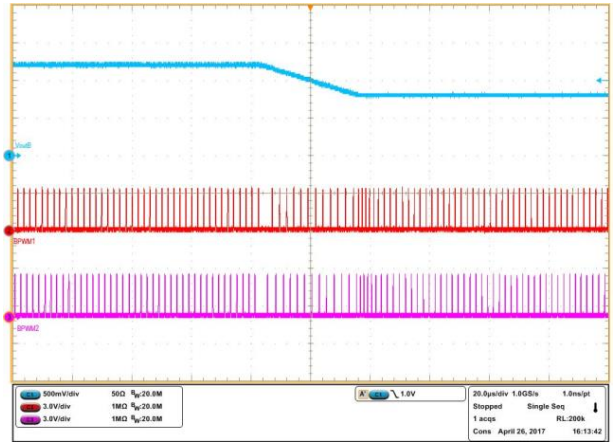
V_{VIN} = 12 V I_{VOUT_A} = 30 A
V_{OUT_A} VID step from 1.2 V to 0.8 V

Figure 90. VOUTA VID-down Change



V_{VIN} = 12 V I_{VOUT_B} = 30 A
V_{OUT_B} VID step from 0.8 V to 1.2 V

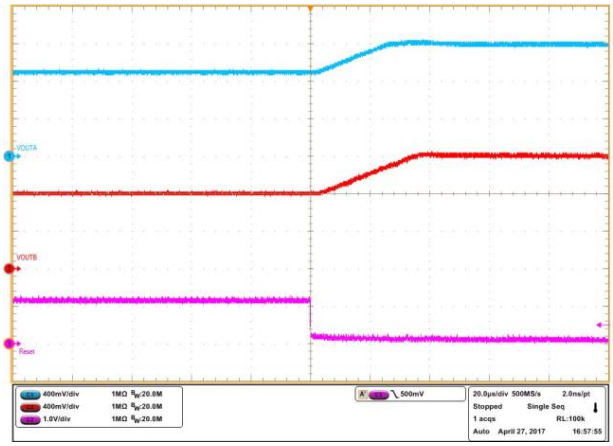
Figure 91. VOUTB VID-up Change



V_{VIN} = 1.2 V I_{VOUT_B} = 30 A
V_{OUT_B} VID step from 1.2 V to 0.8 V

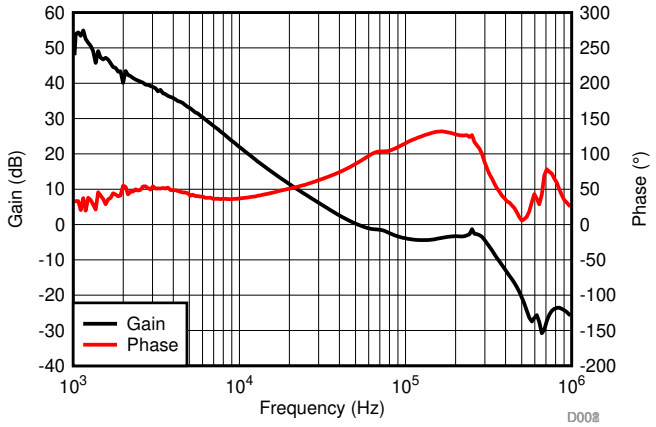
Figure 92. VOUTB VID-down Change

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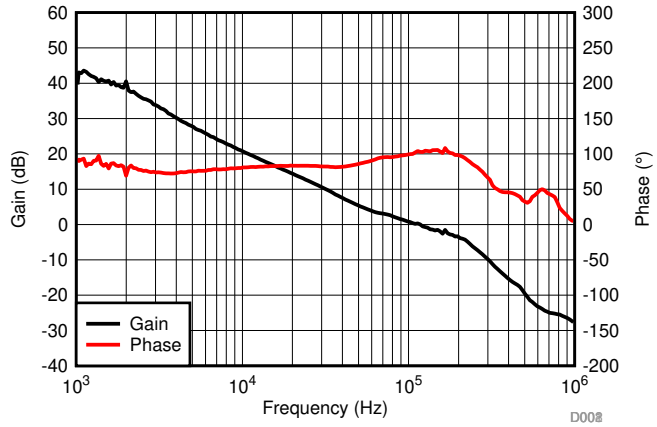
V_{VIN} = 12 V
V_{OUT_A} change from 0.9 V to 1.2 V
V_{OUT_B} change from 0.8 V to 1.2 V

Figure 93. RESET Function



V_{VIN} = 12 V
V_{VOUT_A} = 900 mV
I_{OUT_A} = 100 A

Figure 94. Bode Plot



V_{VIN} = 12 V
V_{VOUT_B} = 800 mV
I_{OUT_B} = 30 A

Figure 95. Bode Plot

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9 Power Supply Recommendations

The TPS53681 device operates from 3.3-V supply at the V3P3 pin (pin 39) and the 12-V supply from the VIN_CSNIN pin (pin 38). TI recommends the following power-up and power-down sequence in order for the controller to monitor the complete power-up and power-down procedure, fault protection and fault recording. The device provides pre-start up overvoltage protection when the controller and the power stage are enabled before the 12-V input is applied.

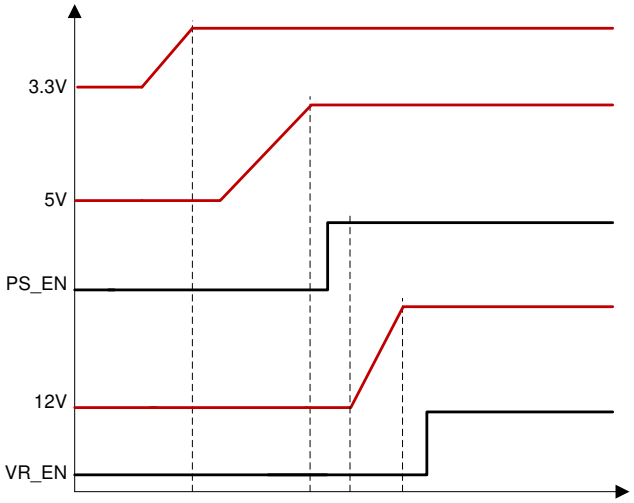


図 96. StartUp Waveforms

The recommended power-up sequence is:

1. 3.3 V
2. 5 V
3. PS_EN
4. 12 V
5. VR_EN

The recommended power-down sequence is:

1. VR_EN
2. 12 V
3. PS_EN
4. 5 V
5. 3.3 V

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10 Layout

10.1 Layout Guidelines

Contact your local TI representative to get a copy of the schematic and PCB layout guide.

10.1.1 Device Guidelines

The TPS53681 device makes it easy to separate noisy driver interface lines from sensitive interface lines. Because the power stage is external to the device, all gate-drive and switch-node traces must be local to the inductor and power stages.

The device does not require special care in the layout of power chain components, because independent isolated current feedback is provided. Route the phases as symmetrically as possible. Current feedback from each phase must be free of noise and have equal amounts of effective current sense resistance.

MOST IMPORTANT LAYOUT SUGGESTION

Separate noisy driver interface lines from sensitive analog and PMBus interface lines.

10.1.2 Power Stage Guidelines

- Use the recommended land pattern including the via pattern for the power stage footprint.
- The input voltage bypass capacitors require a minimum of two vias per pad (for both VIN and GND).
- Place additional GND vias along the sides of the device as space allows.
- For multi-phase systems, ensure that the GND pour connects all phases.
- The VOS pin feedback point begins at the inner edge of the inductor output voltage pad.
- Place the VDD and PVDD bypass capacitors directly next to pins on the top layer of the board.

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10.2 Layout Examples

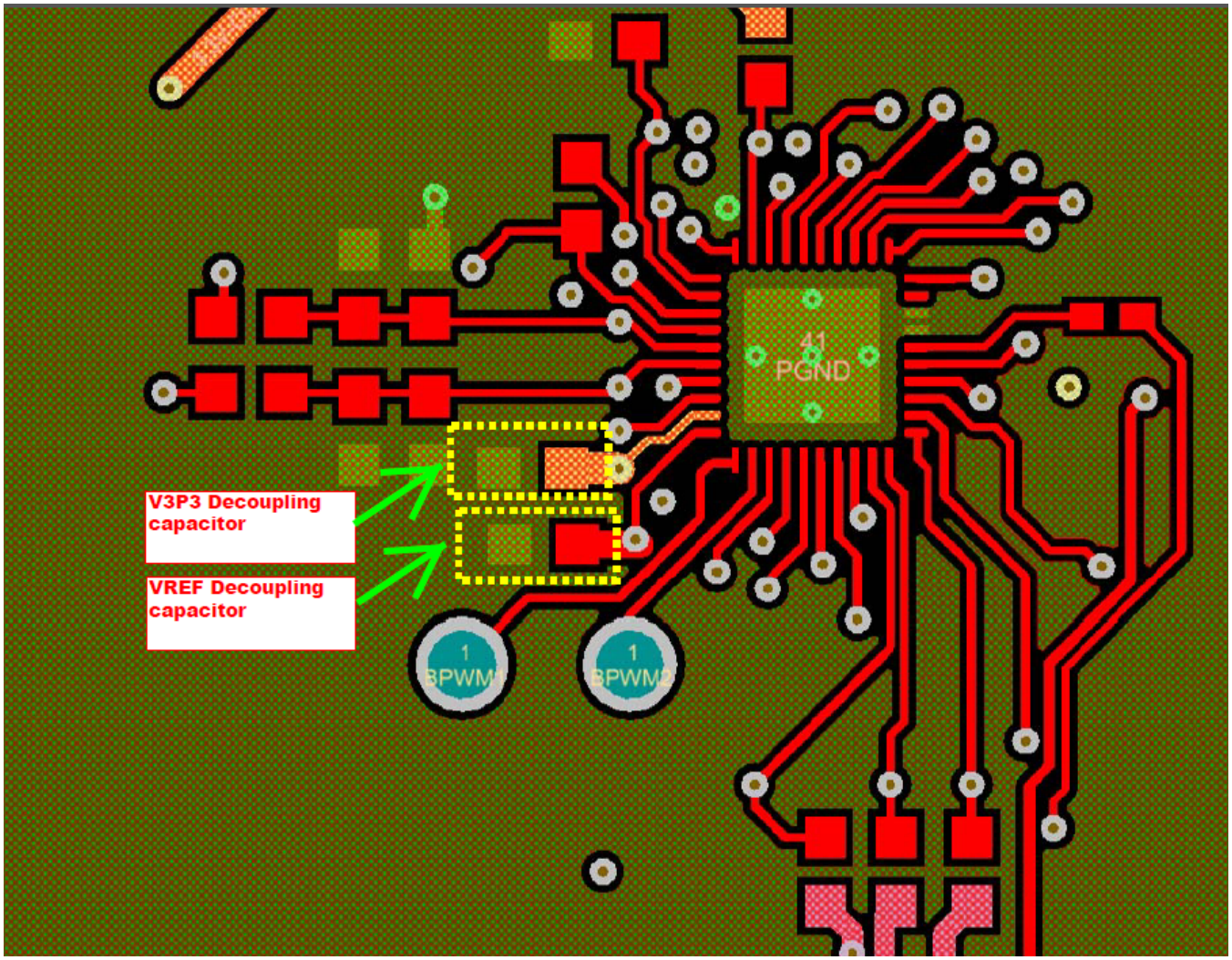


図 97. Controller Layout Example

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Layout Examples (continued)

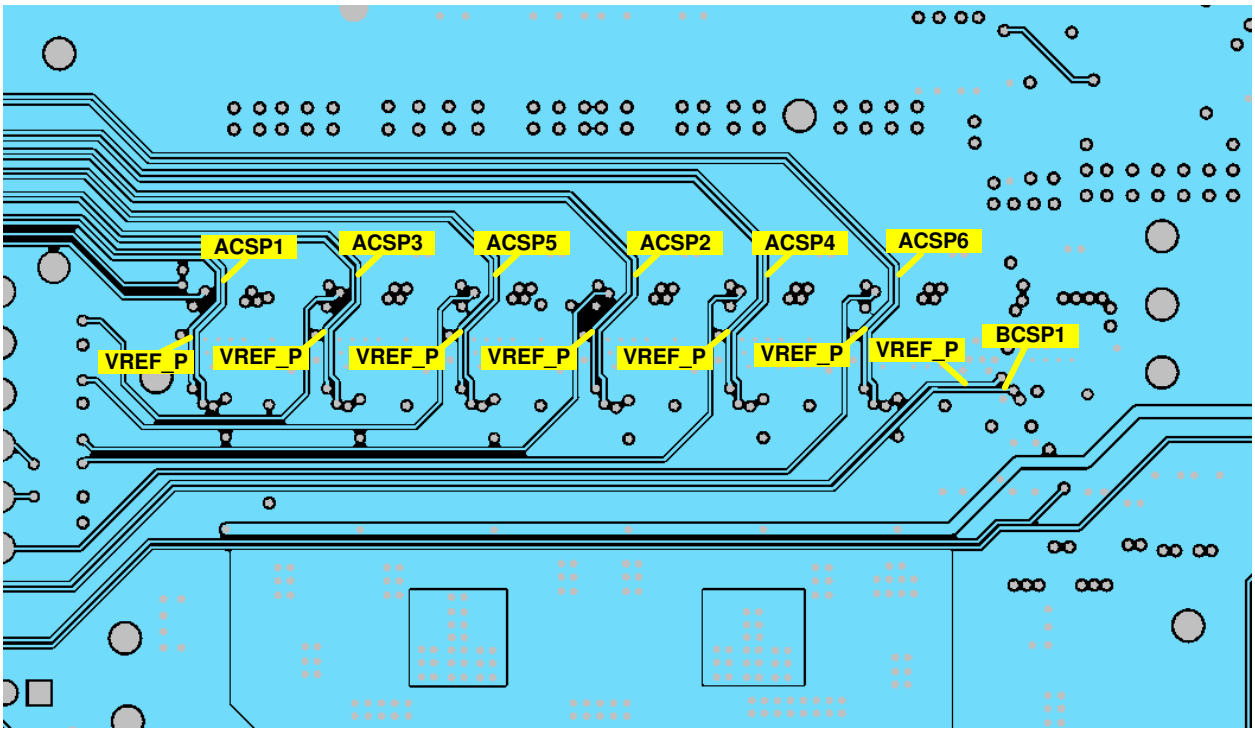


図 98. Power Stage Current Sense Differential Pairs Layout Example

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53681RSBR	Active	Production	WQFN (RSB) | 40	3000 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	TPS 53681
TPS53681RSBR.A	Active	Production	WQFN (RSB) | 40	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	TPS 53681
TPS53681RSBT	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS 53681
TPS53681RSBT.A	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS 53681

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

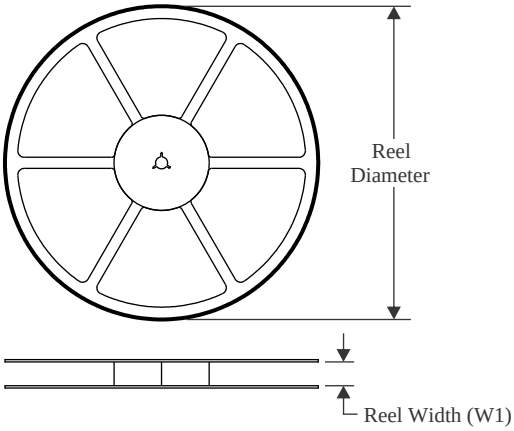
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

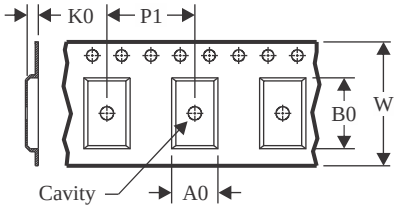
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

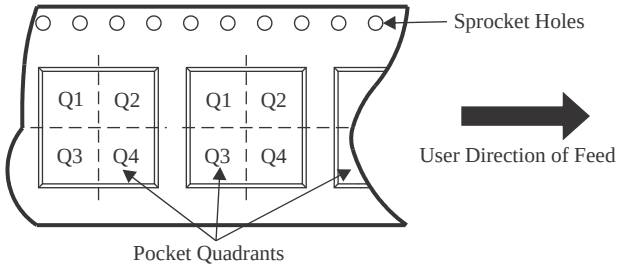


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

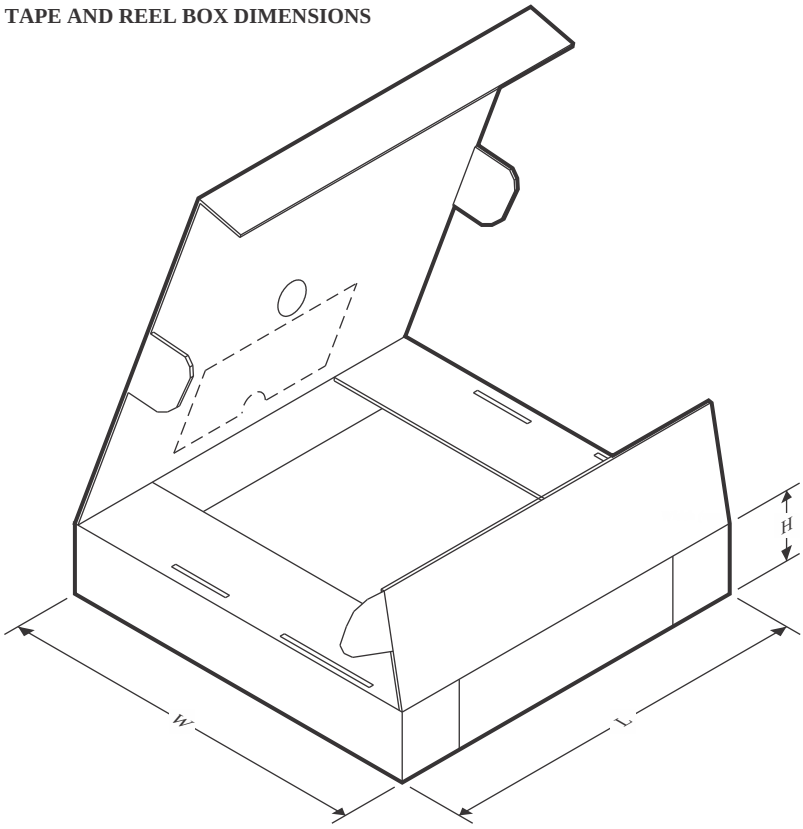
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53681RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

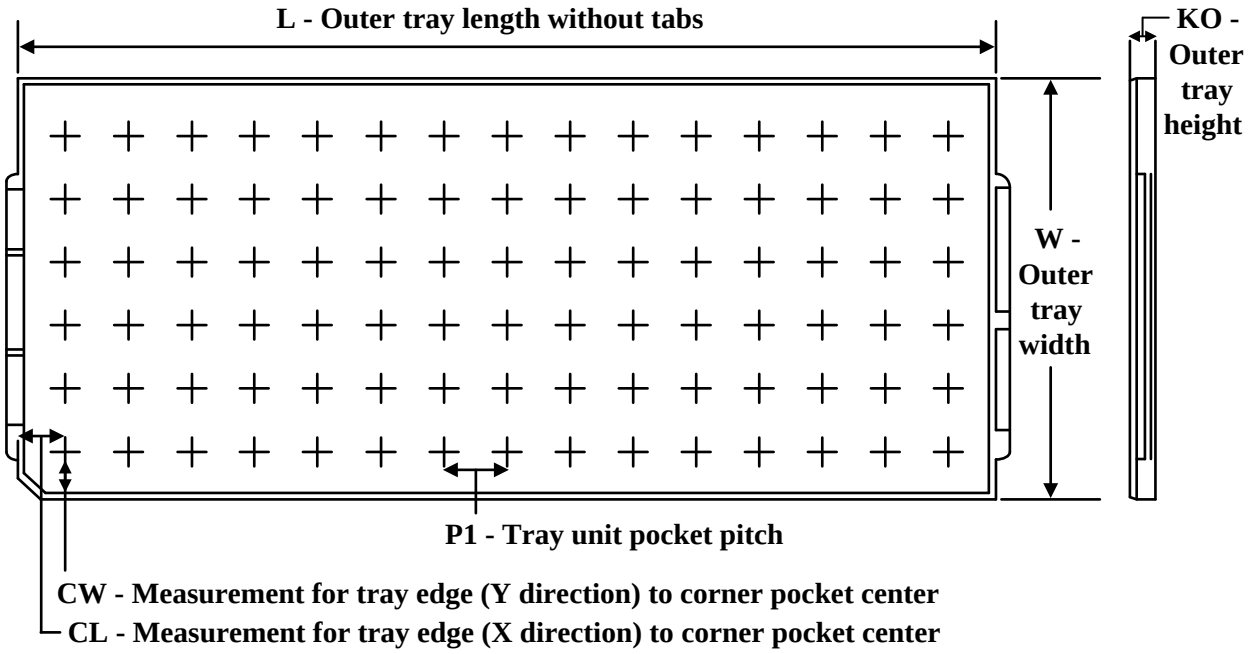
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53681RSBR	WQFN	RSB	40	3000	346.0	346.0	33.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPS53681RSBR	RSB	WQFN	40	3000	35 X 14	150	322.6	135.9	7620	8.8	7.9	8.15
TPS53681RSBR.A	RSB	WQFN	40	3000	35 X 14	150	322.6	135.9	7620	8.8	7.9	8.15
TPS53681RSBT	RSB	WQFN	40	250	35 X 14	150	322.6	135.9	7620	8.8	7.9	8.15
TPS53681RSBT.A	RSB	WQFN	40	250	35 X 14	150	322.6	135.9	7620	8.8	7.9	8.15

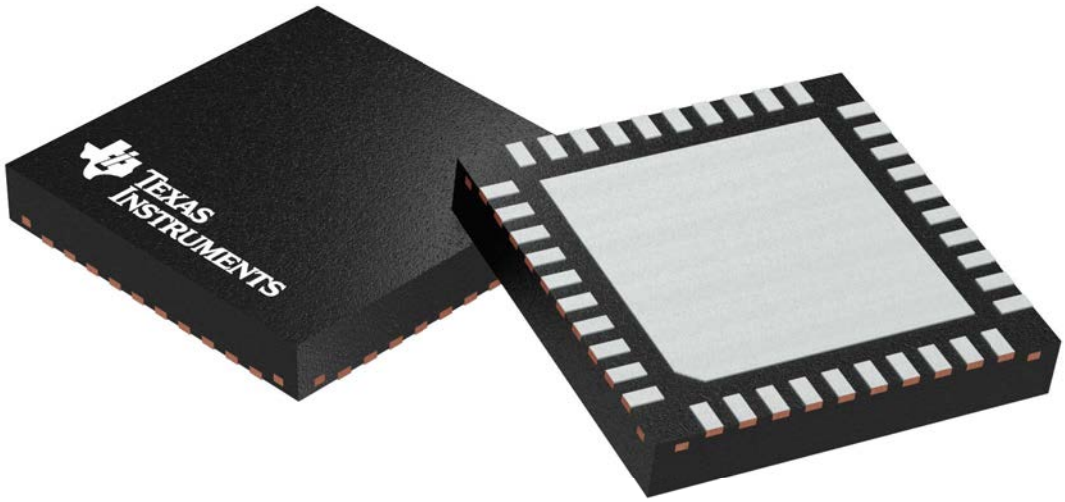
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



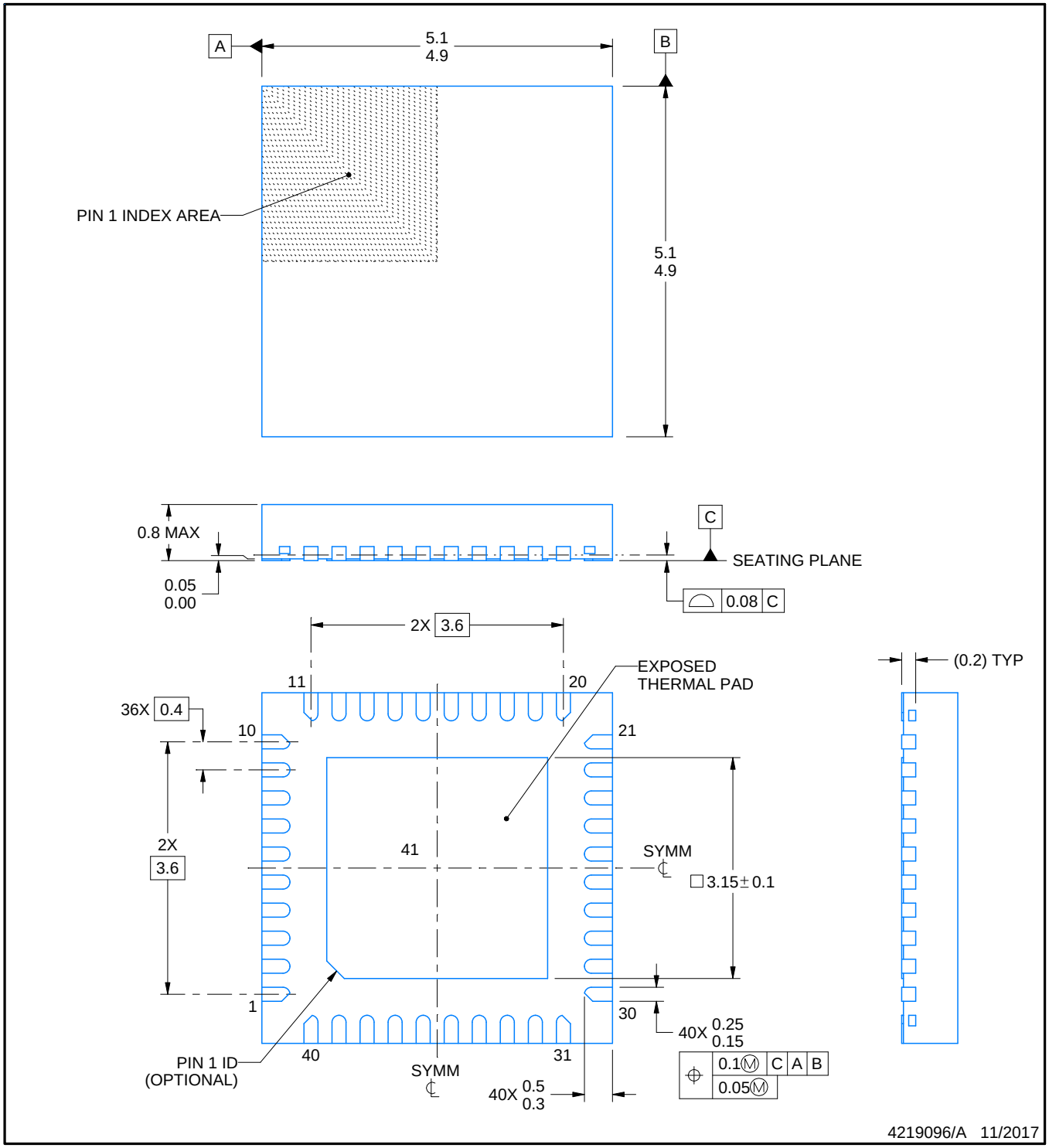
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RSB0040E

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

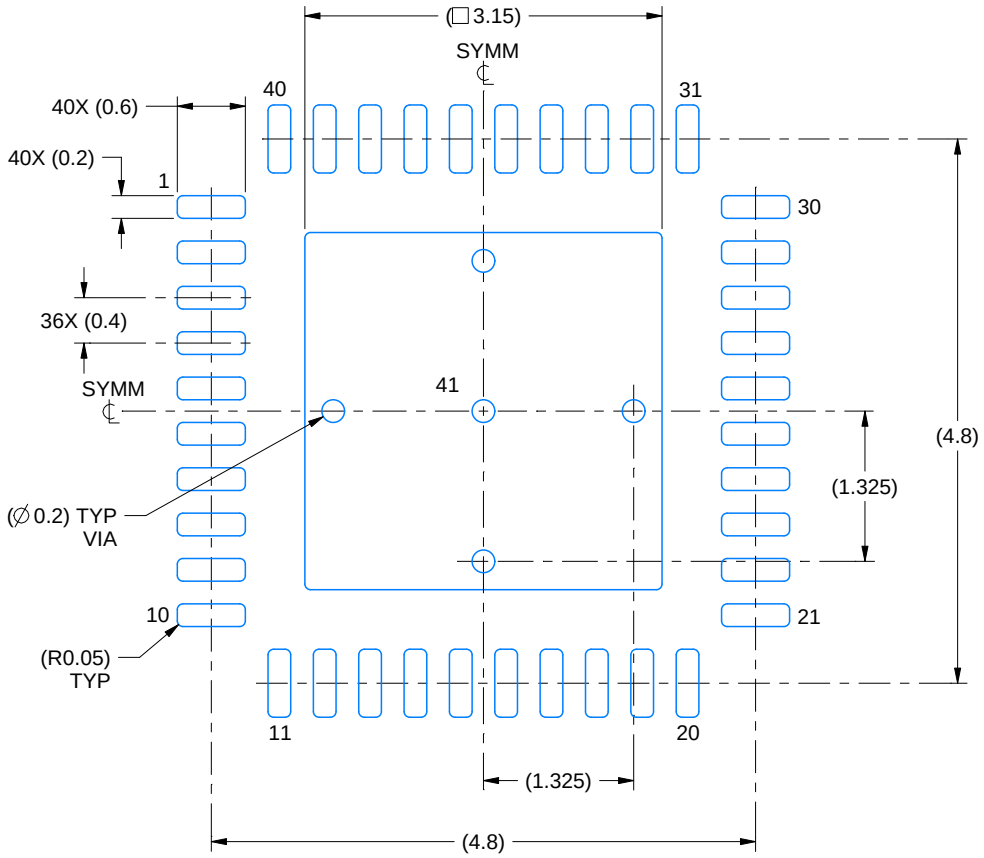
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

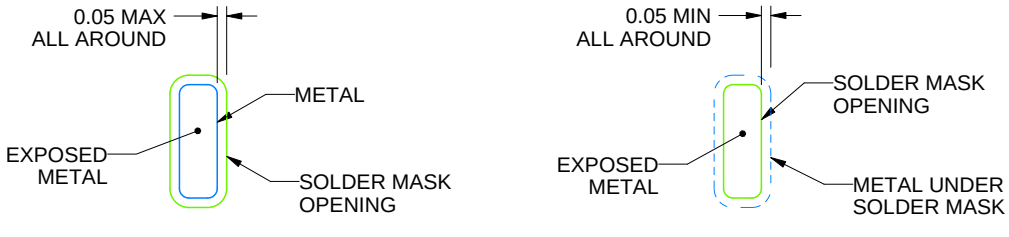
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

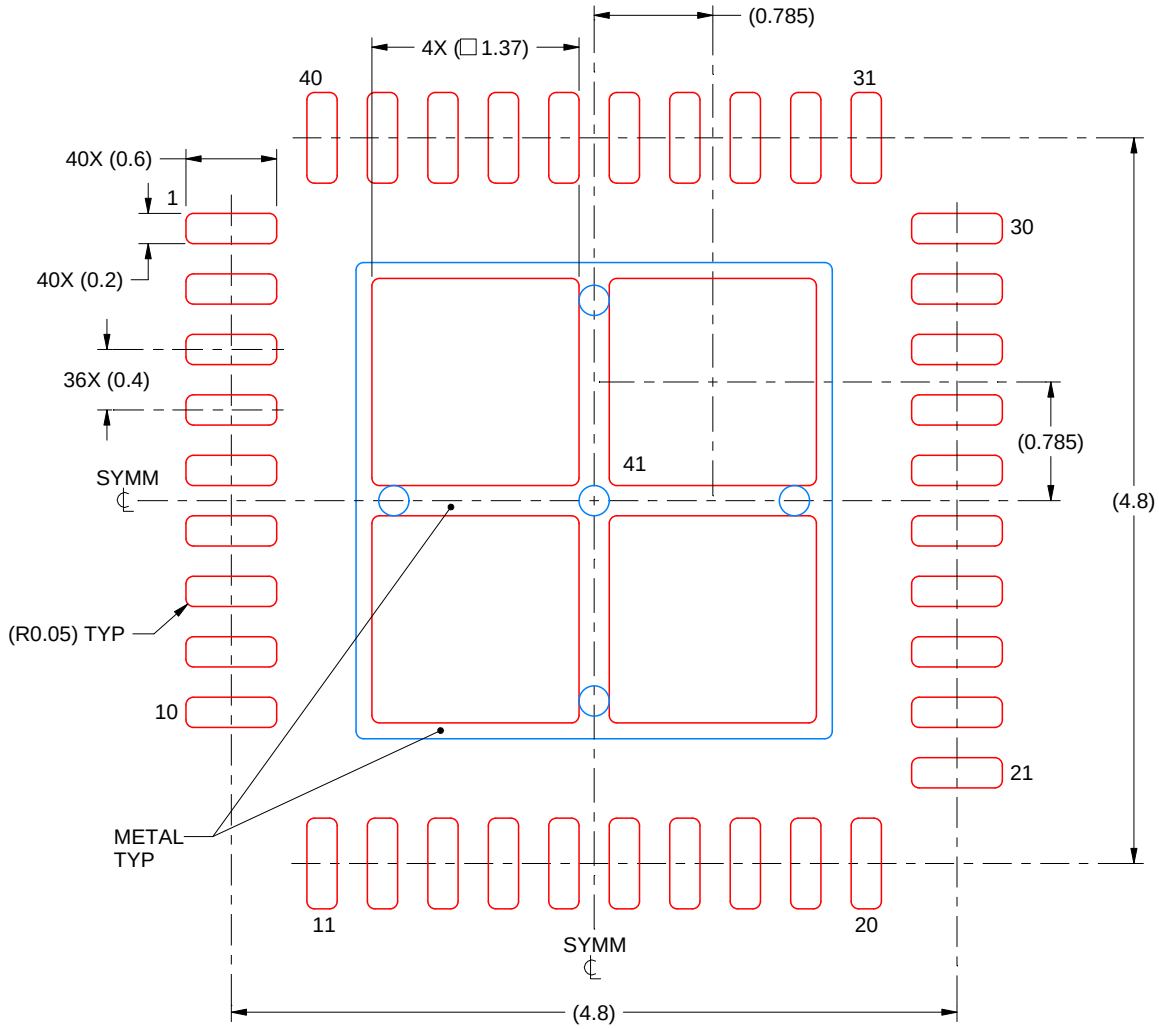
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219096/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219096/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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