TEXAS INSTRUMENTS
TPS54335A, TPS54335-1A, TPS54336A
JAJSC29D – NOVEMBER 2014 – REVISED FEBRUARY 2016

TPS5433xA 4.5V～28V入力、3A出力、同期整流降圧型DC/DCコンバータ

1 特長

- 同期整流128mΩおよび84mΩ MOSFETによる3Aの連続出力電流
- TPS54335A: 内部的な2msのソフトスタート、50kHz～1.5MHzの可変周波数
- TPS54336A: 可変ソフトスタート、340kHz固定周波数
- シャットダウン時に2μAの低静止電流
- 0.8V、±0.8%精度の基準電圧
- 電流モード制御
- プリバイアスされた出力への単調起動
- パルス・スキップによる軽負荷効率の向上
- ヒカップ・モード過電流保護
- サーマル・シャットダウン(TSD)および過電圧遷移保護
- 8ピンSO PowerPAD™および10ピンVSONパッケージ

2 アプリケーション

- デジタルTV (DVT)、セットトップ・ボックス(STB、DVD/Blu-rayプレイヤー)、LCDディスプレイ、CPE (ケーブルモデム、Wi-Fiルーター)、DLPプロジェクター、スマート・メーターなどの消費者向けアプリケーション
- バッテリ充電器
- 工業用および車載オーディオ用の電源
- 5V、12V、24Vの分散電力バス電源

3 概要

TPS5433xAファミリのデバイスは、入力電圧範囲が4.5V～28Vの同期コンバータです。このデバイスにはローサイド・スイッチングFETが搭載されており、外付けのダイオードが必要ないため、部品数を減らすことができます。

内蔵の128mΩおよび84mΩのMOSFET、低いI_Q、軽負荷時のパルス・スキップにより最大の効率を実現しています。イネーブル・ピンにより、シャットダウン時消費電流を2μAまで低減できます。この降圧型(バック)コンバータは、温度に対して1.5%と安定した、十分にレギュレートされている基準電圧により、さまざまな負荷に対して正確なレギュレーションを実現します。

ハイサイドMOSFETでのサイクル単位の電流制限により、TPS5433xAファミリのデバイスは過負荷の状況で保護されて、ローサイドのソース電流制限により電流暴走が防止され、強化されています。ローサイドのシンク電流制限により、ローサイドMOSFETがオフになることで、過剰な逆電流が防止されます。あらかじめ設定された時間を超えて過電流の状態が続いた場合、ヒカップ・モード保護が作動します。サーマル・シャットダウンにより、ダイの温度がスレッショルドを超えるとデバイスがディスエーブルされ、設定済みの過熱ヒカップ時間が経過するとイネーブルに戻ります。

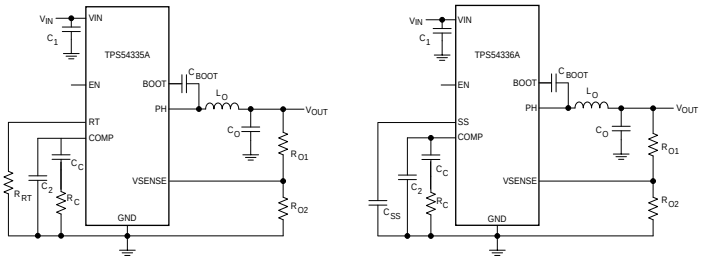
製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS54335A	SO PowerPAD (8)	4.89mm×3.90mm
TPS54336A	VSON (10)	3.00mm×3.00mm
TPS54335-1A	VSON (10)(2)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) TPS54335-1A用のDRCパッケージは、ピンとヒートパッドとの間の隙間を広げるため、ヒートパッドが狭くなっています。*Differences Between the Two DRC Packages*セクションを参照してください。

概略回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

Revision C (March 2015) から **Revision D** に変更 **Page**

- データシートのタイトルからSWIFT™を削除 ... 1

Revision B (August 2015) から **Revision C** に変更 **Page**

- TPS54335-1Aデバイスをデータシートへ 追加 ... 1

Revision A (December 2014) から **Revision B** に変更 **Page**

- 「*関連リンク*」セクションを追加し、データシートから*選択的公開*声明を 削除 ... 1
- Changed the *Device Functional Modes* section ... 21
- Changed the *Power Supply Recommendations* section ... 38

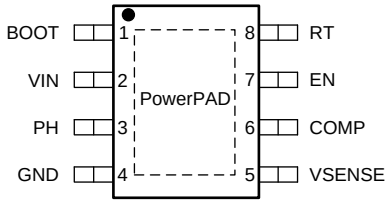
2014年11月 発行のものから更新 **Page**

- デバイスの状態を*製品プレビュー*から*量産データ*へ 変更 ... 1

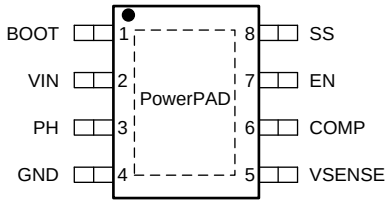
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5 Pin Configuration and Functions

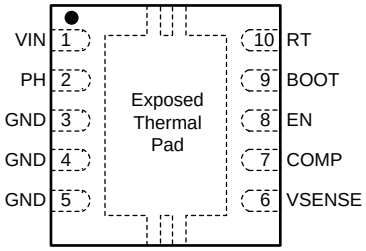
DDA Package
8-Pin SO PowerPAD
TPS54335A Top View



DDA Package
8-Pin SO PowerPAD
TPS54336A Top View



DRC Package
10-Pin VSON With Exposed Thermal Pad
TPS54335A and TPS54335-1A Top View



DRC Package
10-Pin VSON With Exposed Thermal Pad
TPS54336A Top View

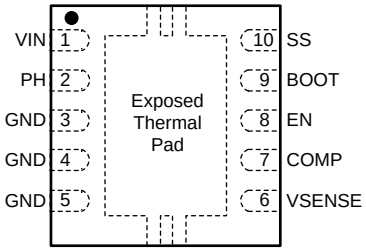


Table 1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SO PowerPAD	VSON		
BOOT	1	9	O	A bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	6	7	O	This pin is the error-amplifier output and the input to the output switch-current comparator. Connect frequency compensation components to this pin.
EN	7	8	I	This pin is the enable pin. Float the EN pin to enable.
GND	4	3	—	Ground
GND	4	4	—	Ground
GND	4	5	—	Ground
PH	3	2	O	The PH pin is the source of the internal high-side power MOSFET.
RT (TPS54335A and TPS54335-1A)	8	10	O	Connect the RT pin to an external timing resistor to adjust the switching frequency of the device.
SS (TPS54336A)	8	10	O	The SS pin is the soft-start and tracking pin. An external capacitor connected to this pin sets the internal voltage-reference rise time. The voltage on this pin overrides the internal reference.
VIN	2	1	—	This pin is the 4.5- to 28-V input supply voltage.
VSENSE	5	6	I	This pin is the inverting node of the transconductance (gm) error amplifier.
PowerPAD (SO only)			—	For proper operation, connect the GND pin to the exposed thermal pad. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.
Thermal pad (VSON only)			—	

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	30	V
	EN	–0.3	6	V
	BOOT	–0.3	(V_{PH} + 7.5)	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	RT	–0.3	3	V
	SS	–0.3	3	V
Output voltage	BOOT-PH	0	7.5	V
	PH	–1	30	V
	PH, 10-ns transient	–3.5	30	V
V_{DIFF} (GND to exposed thermal pad)		–0.2	0.2	V
Source current	EN	100	100	µA
	RT	100	100	µA
	PH		Current-limit	A
Sink current	PH		Current-limit	A
	COMP	200	200	µA
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under the *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{SS}	Supply input voltage	4.5	28	V
V_{OUT}	Output voltage	0.8	24	V
I_{OUT}	Output current	0	3	A
T_J	Operating junction temperature(1)	–40	150	°C

(1) The device must operate within 150°C to ensure continuous function and operation of the device.

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6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPS5433xA	TPS5433xA and TPS54335-1A	TPS54335-2A	UNIT
		DDA (SO PowerPAD)	DRC (VSON)	DRC (VSON)	
		8 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.1	43.9	43.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.9	55.4	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	18.9	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8	0.7	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	19.1	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	5.3	5.3	°C/W

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that will not degrade the parametric or functional specifications of the device for the life of the product containing it. T_J = –40°C to 150°C, V_{IN} = 4.5 to 28 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND UVLO (VIN PIN)					
Operating input voltage		4.5		28	V
Input UVLO threshold	Rising V_{IN}		4	4.5	V
Input UVLO hysteresis			180	400	mV
VIN-shutdown supply current	V_{EN} = 0 V		2	10	µA
VIN-operating non-switching supply current	V_{VSENSE} = 810 mV		310	800	µA
ENABLE (EN PIN)					
Enable threshold	Rising		1.21	1.28	V
Enable threshold	Falling	1.1	1.17		V
Input current	V_{EN} = 1.1 V		1.15		µA
Hysteresis current	V_{EN} = 1.3 V		3.3		µA
VOLTAGE REFERENCE					
Reference	T_J =25°C	0.7936	0.8	0.8064	V
		0.788	0.8	0.812	
MOSFET					
High-side switch resistance(1)	$V_{(BOOT-PH)}$ = 3 V		160	280	mΩ
	$V_{(BOOT-PH)}$ = 6 V		128	230	mΩ
Low-side switch resistance(1)	V_{IN} = 12 V		84	170	mΩ
ERROR AMPLIFIER					
Error-amplifier transconductance (gm)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		1300		µmhos
Error-amplifier source and sink	V_{COMP} = 1 V, 100-mV overdrive		100		µA
Start switching peak current threshold			0.5		A
COMP to I_{SWITCH} gm			8		A/V
CURRENT-LIMIT					
High-side switch current-limit threshold		4	4.9	6.5	A
Low-side switch sourcing current-limit		3.5	4.7	6.1	A
Low-side switch sinking current-limit			0		A

(1) Measured at pins

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Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that will not degrade the parametric or functional specifications of the device for the life of the product containing it. T_J = –40°C to 150°C, V_{IN} = 4.5 to 28 V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown		160	175		°C
Thermal shutdown hysteresis			10		°C
BOOT PIN					
BOOT-PH UVLO			2.1	3	V
SOFT START					
Soft-start charge current, TPS54336A			2.3		µA

6.6 Timing Requirements

	MIN	TYP	MAX	UNIT
CURRENT-LIMIT				
Hiccup wait time		512		Cycles
Hiccup time before restart		16384		Cycles
THERMAL SHUTDOWN				
Thermal shutdown hiccup time		32768		Cycles
SOFT START				
Internal soft-start time, TPS54335A and TPS54335-1A		2		ms

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PH PIN					
Minimum on time	Measured at 90% to 90% of VIN, I_{PH} = 2 A		94	145	ns
Minimum off time	$V_{(BOOT-PH)}$ ≥ 3 V		0%		
SWITCHING FREQUENCY					
Switching frequency range, TPS54335A and TPS54335-1A		50		1500	kHz
	$R_{(RT)}$ = 100 kΩ	384	480	576	kHz
	$R_{(RT)}$ = 1000 kΩ, –40°C to 105°C	40	50	60	kHz
	$R_{(RT)}$ = 30 kΩ	1200	1500	1800	kHz
Internal switching frequency, TPS54336A		272	340	408	kHz

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6.8 Typical Characteristics

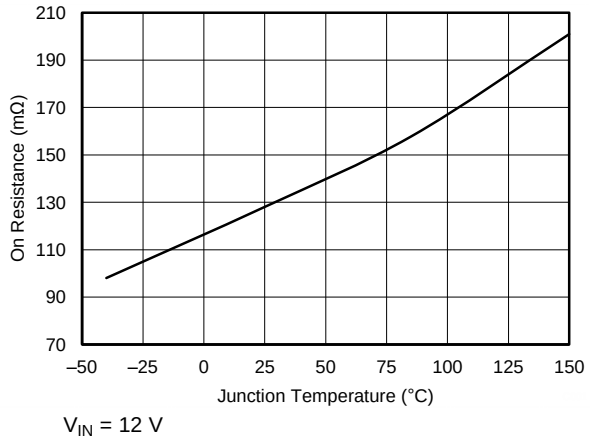


Figure 1. High-Side MOSFET on Resistance vs Junction Temperature

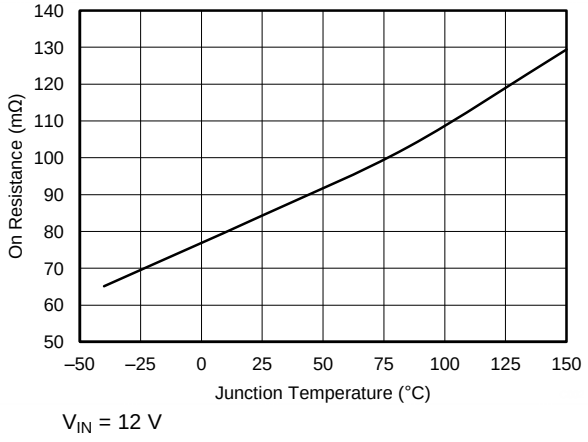


Figure 2. Low-Side MOSFET on Resistance vs Junction Temperature

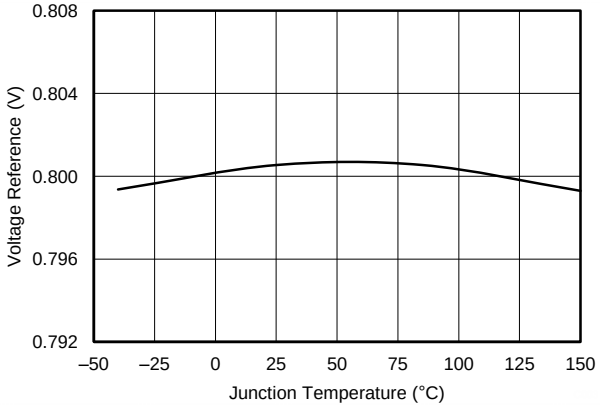


Figure 3. Voltage Reference vs Junction Temperature

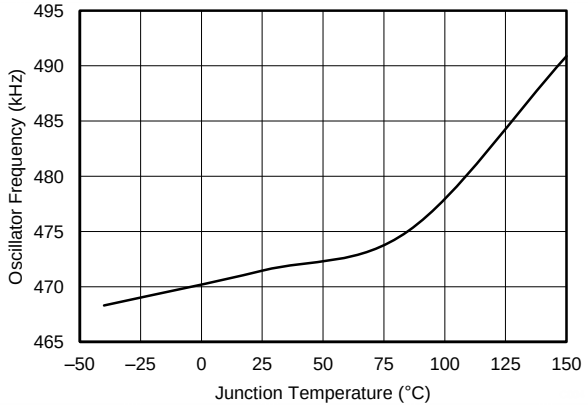


Figure 4. Oscillator Frequency vs Junction Temperature

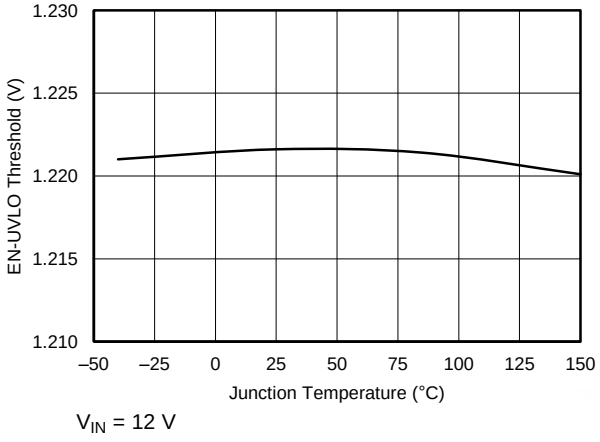


Figure 5. UVLO Threshold vs Junction Temperature

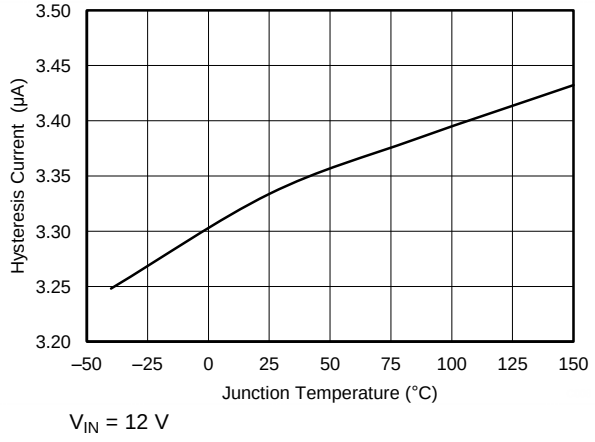


Figure 6. Hysteresis Current vs Junction Temperature

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Typical Characteristics (continued)

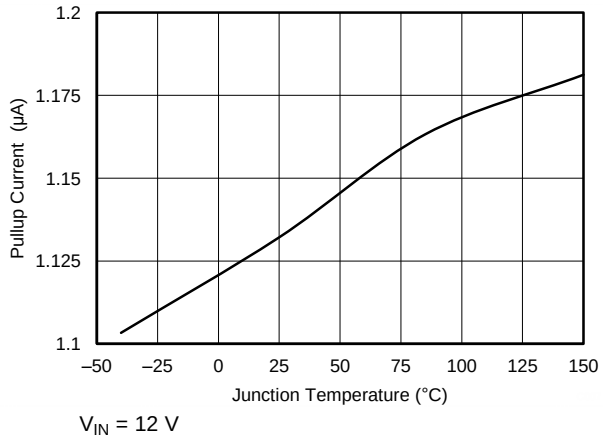


Figure 7. Pullup Current vs Junction Temperature

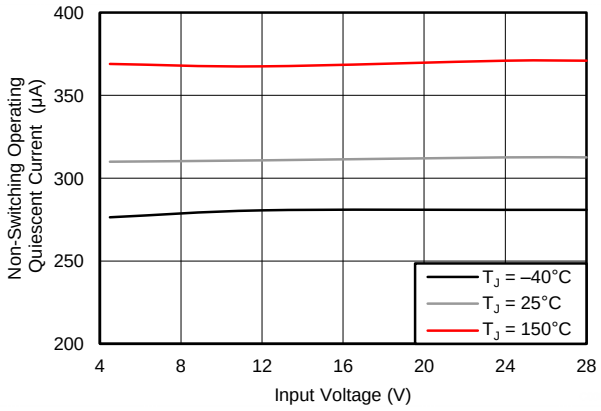


Figure 8. Non-Switching Operating Quiescent Current vs Input Voltage

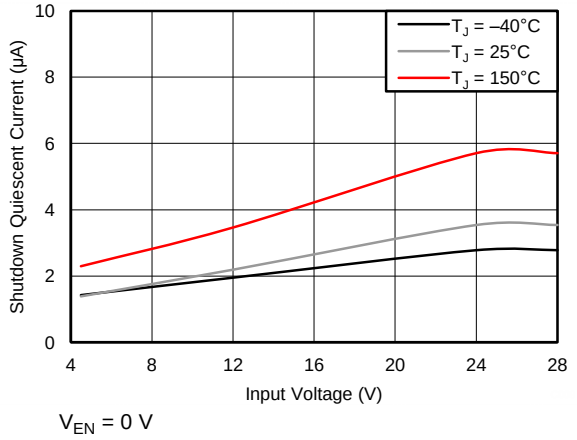


Figure 9. Shutdown Quiescent Current vs Input Voltage

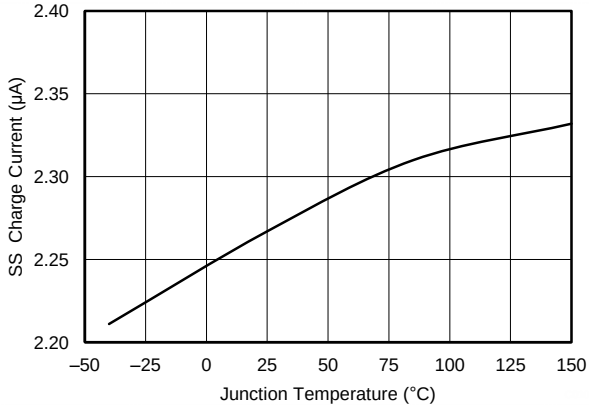


Figure 10. SS Charge Current vs Junction Temperature

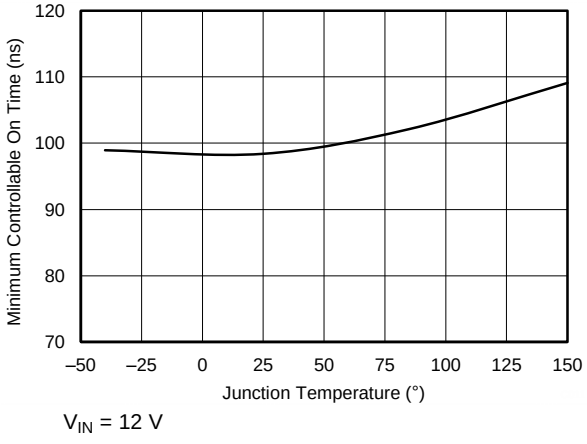


Figure 11. Minimum Controllable On Time vs Junction Temperature

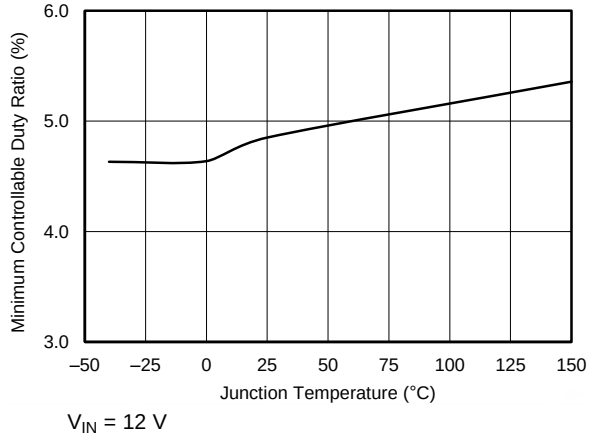


Figure 12. Minimum Controllable Duty Ratio vs Junction Temperature

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Typical Characteristics (continued)

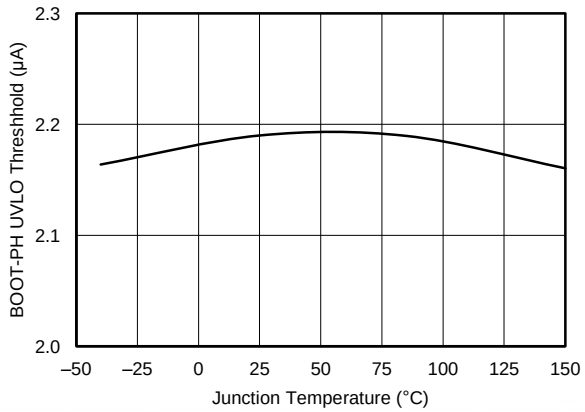


Figure 13. BOOT-PH UVLO Threshold vs Junction Temperature

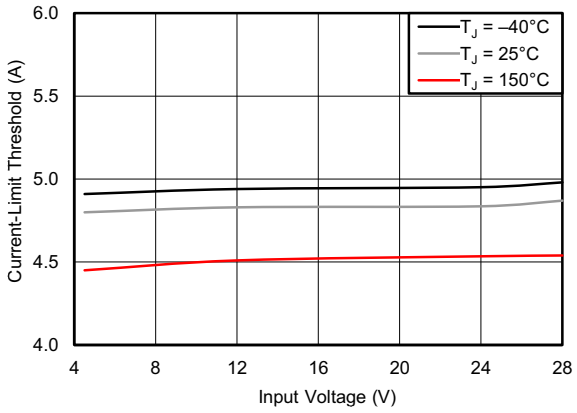


Figure 14. Current Limit Threshold vs Input Voltage

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7 Detailed Description

7.1 Overview

The device is a 28-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current-mode control which reduces output capacitance and simplifies external frequency-compensation design.

The device has been designed for safe monotonic startup into pre-biased loads. The device has a typical default startup voltage of 4 V. The EN pin has an internal pullup-current source that can provide a default condition when the EN pin is floating for the device to operate. The total operating current for the device is 310 μA (typical) when not switching and under no load. When the device is disabled, the supply current is less than 5 μA.

The integrated 128-mΩ and 84-mΩ MOSFETs allow for high-efficiency power-supply designs with continuous output currents up to 3 A.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. The output voltage can be stepped down to as low as the 0.8-V reference voltage.

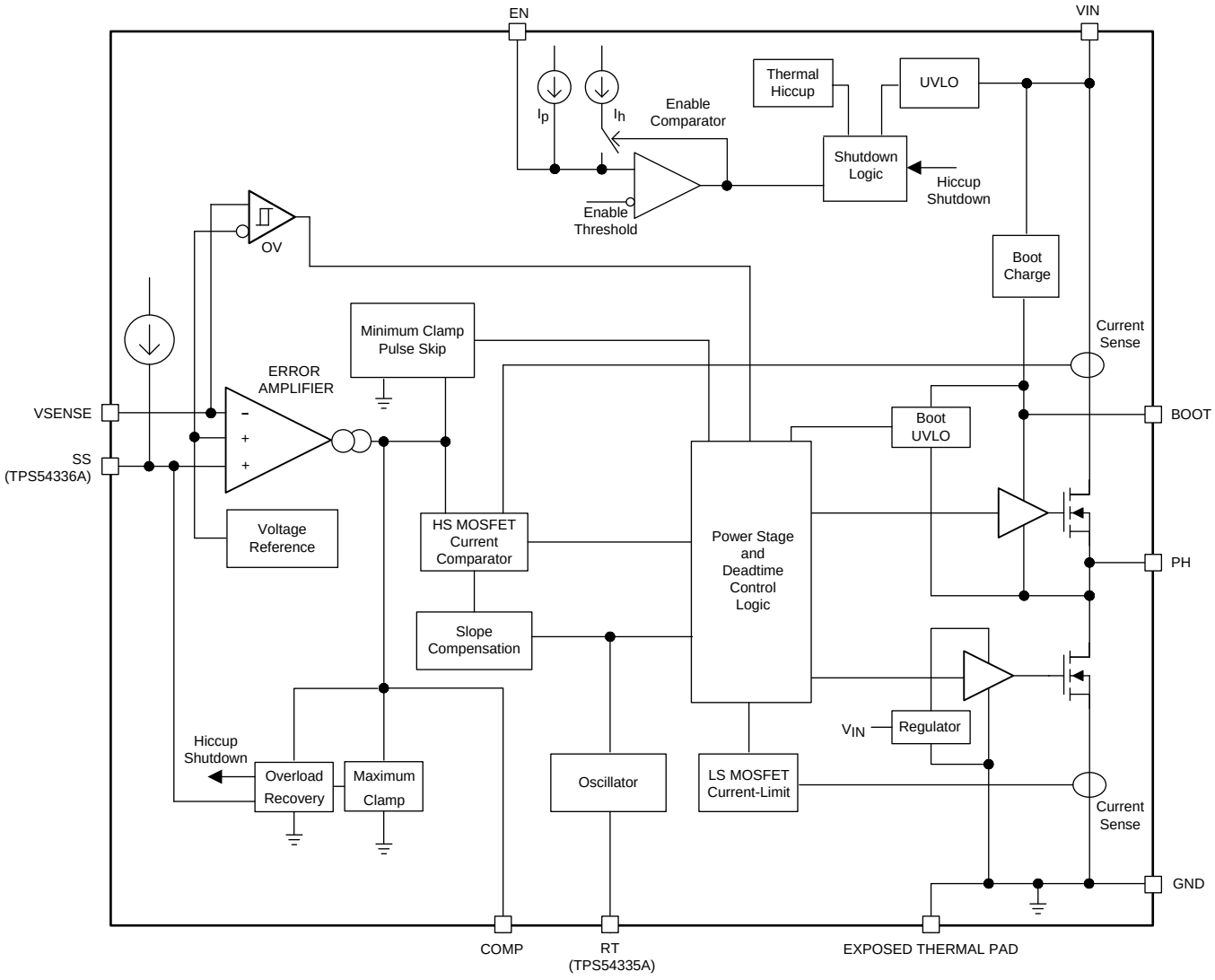
The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. When the regulated output voltage is greater than 106% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The TPS54335A device has a wide switching frequency of 50 kHz to 1500 kHz which allows for efficiency and size optimization when selecting the output filter components. The internal 2-ms soft-start time is implemented to minimize inrush currents.

The TPS54336A device has a fixed 340-kHz switching frequency. The device adjusts the soft-start time with the SS pin.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

7.3.2 Light-Load Operation

The device monitors the peak switch current of the high-side MOSFET. When the peak switch current is lower than 0.5 A (typical), the device stops switching to boost the efficiency until the peak switch current again rises higher than 0.5 A (typical).

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Feature Description (continued)

7.3.3 Voltage Reference

The voltage-reference system produces a precise ±1.5% voltage-reference over temperature by scaling the output of a temperature-stable bandgap circuit.

7.3.4 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. Using divider resistors with 1% tolerance or better is recommended. Begin with a value of 10 kΩ for the upper resistor divider, R1, and use Equation 1 to calculate the value of R2. Consider using larger value resistors to improve efficiency at light loads. If the values are too high then the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (1)$$

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Feature Description (continued)

7.3.5 Enabling and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (I_Q) state.

The EN pin has an internal pullup-current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 180 mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 15. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a small pullup-current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. Use Equation 2, and Equation 3 to calculate the values of R1 and R2 for a specified UVLO threshold.

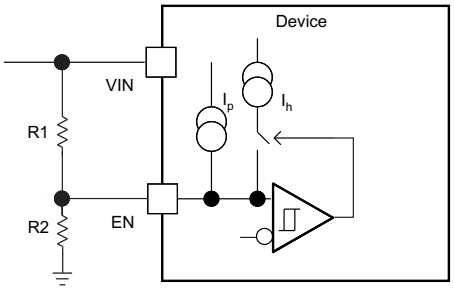


Figure 15. Adjustable VIN Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h}$$

where

- I_P = 1.15 µA
- I_H = 3.3 µA
- $V_{ENfalling}$ = 1.17 V
- $V_{ENrising}$ = 1.21 V

(2)

$$R2 = \frac{R1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R1(I_p + I_h)}$$

where

- I_P = 1.15 µA
- I_H = 3.3 µA
- $V_{ENfalling}$ = 1.17 V
- $V_{ENrising}$ = 1.21 V

(3)

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Feature Description (continued)

7.3.6 Error Amplifier

The device has a transconductance amplifier as the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 1300 μA/V (typical). The frequency compensation components are placed between the COMP pin and ground.

7.3.7 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents subharmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.8 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage (TPS54335A), or SS pin voltage (TPS54336A) is higher than VSENSE pin voltage.

7.3.9 Bootstrap Voltage (BOOT)

The device has an integrated boot regulator. The boot regulator requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than the VIN voltage and when the BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage. When the voltage between BOOT and PH pins drops below the BOOT-PH UVLO threshold, which is 2.1 V (typical), the high-side MOSFET turns off and the low-side MOSFET turns on, allowing the boot capacitor to recharge.

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Feature Description (continued)

7.3.10 Adjustable Switching Frequency (TPS54335A Only)

To determine the RT resistance, R_{RT}, for a given switching frequency, use or the curve in . To reduce the solution size, set the switching frequency as high as possible, but consider the tradeoffs of the supply efficiency and minimum controllable on time.

$$R_{RT}\ (k\Omega) = 55300 \times f_{SW}{}^{-1.025}(kHz) \quad (4)$$

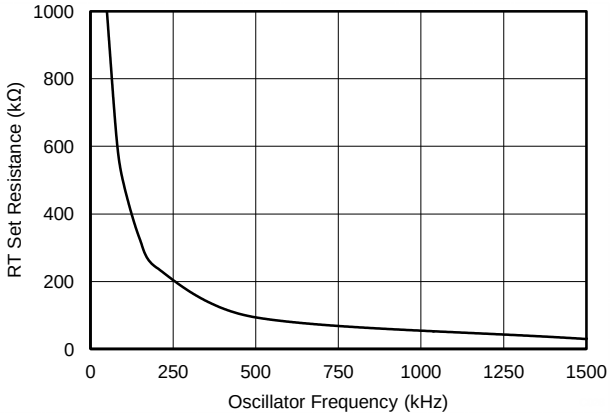


Figure 16. RT Set Resistor vs Switching Frequency

7.3.11 Soft-Start (TPS54336A Only)

The TPS54336A device uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS pin to ground implements a soft-start time. The device has an internal pullup current source of 2.3 μA that charges the external soft-start capacitor. Use to calculate the soft time (t_{SS}, 10% to 90%) and soft capacitor (C_{SS}).

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)}$$

where

- V_{REF} is the voltage reference (0.8 V)
- I_{SS} is the soft-start charge current (2.3 μA) (5)

When the input UVLO is triggered, the device stops switching and enters low-current operation when either the EN pin is pulled below 1.21 V or a thermal-shutdown event occurs. At the subsequent power-up, when the shutdown condition is removed, the device does not begin switching until it has discharged the SS pin to ground ensuring proper soft-start behavior.

7.3.12 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage-protection (OVP) circuit to minimize output voltage overshoot. For example, when the power-supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. When the condition is removed, the regulator output rises and the error-amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power-supply output voltage can respond faster than the error amplifier which leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off which prevents current from flowing to the output and minimizes output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

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Feature Description (continued)

7.3.13 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

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Feature Description (continued)

7.3.13.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the COMP pin voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.

7.3.13.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing current-limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current-limit is exceeded the low-side MOSFET turns off immediately for the remainder of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.14 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. When the junction temperature drops below 165°C typically, the internal thermal-hiccup timer begins to count. The device reinitiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.

7.3.15 Small-Signal Model for Loop Response

Figure 17 shows an equivalent model for the device control loop which can be modeled in a circuit-simulation program to check frequency and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 µA/V. The error amplifier can be modeled using an ideal voltage-controlled current source. The resistor, R_{oea} (3.07 MΩ), and capacitor, C_{oea} (20.7 pF), model the open-loop gain and frequency response of the error amplifier. The 1-mV AC-voltage source between the nodes ***a*** and ***b*** effectively breaks the control loop for the frequency response measurements. Plotting ***ac***-***c*** and ***c***-***b*** show the small-signal responses of the power stage and frequency compensation respectively. Plotting ***a***-***b*** shows the small-signal response of the overall loop. The dynamic loop response can be checked by replacing the load resistance, R_L, with a current source with the appropriate load-step amplitude and step rate in a time-domain analysis.

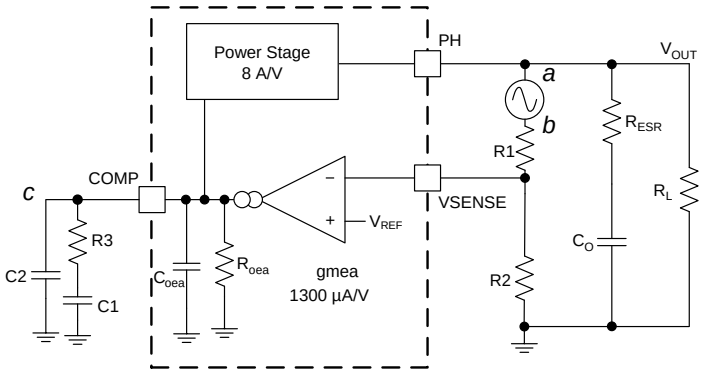


Figure 17. Small-Signal Model For Loop Response

Feature Description (continued)

7.3.16 Simple Small-Signal Model for Peak Current-Mode Control

Figure 18 is a simple small-signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage-controlled current-source (duty-cycle modulator) supplying current to the output capacitor and load resistor. The control-to-output transfer function is shown in Equation 6 and consists of a DC gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in the COMP pin voltage (node ***c*** in Figure 17) is the power-stage transconductance (gm_{ps}) which is 8 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance, R_L, with resistive loads as shown in Equation 7. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 8). The combined effect is highlighted by the dashed line in Figure 19. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes designing the frequency compensation easier.

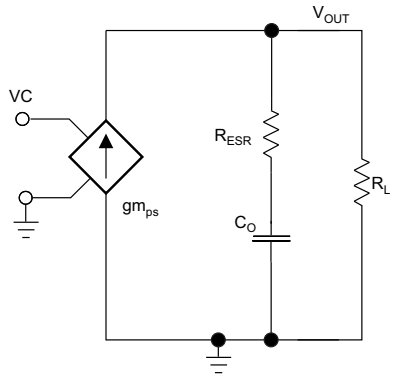


Figure 18. Simplified Small-Signal Model for Peak Current-Mode Control

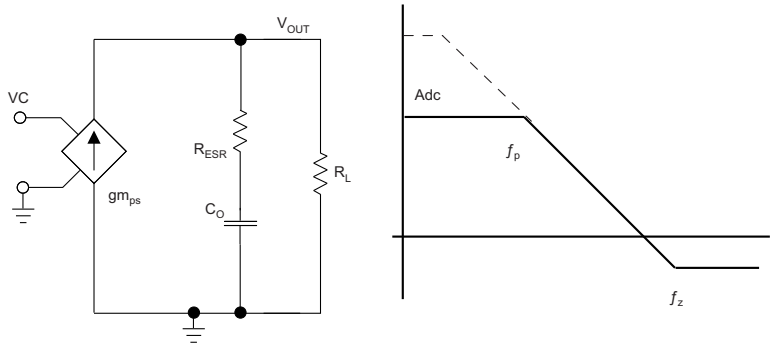


Figure 19. Simplified Frequency Response for Peak Current-Mode Control

$$\frac{V_{OUT}}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_z}\right)}{\left(1 + \frac{s}{2\pi \times f_p}\right)} \quad (6)$$

$$Adc = gm_{ps} \times R_L$$

where

- gm_{ps} is the power stage gain (8 A/V)
- R_L is the load resistance

(7)

$$f_p = \frac{1}{C_O \times R_L \times 2\pi}$$

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Feature Description (continued)

where

- C_O is the output capacitance (8)

$$f_z = \frac{1}{C_O \times R_{ESR} \times 2\pi}$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor (9)

7.3.17 Small-Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 20. In Type 2A, one additional high frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The following design guidelines are provided for advanced users who prefer to compensate using the general method. The following equations only apply to designs whose ESR zero is above the bandwidth of the control loop which is usually true with ceramic output capacitors.

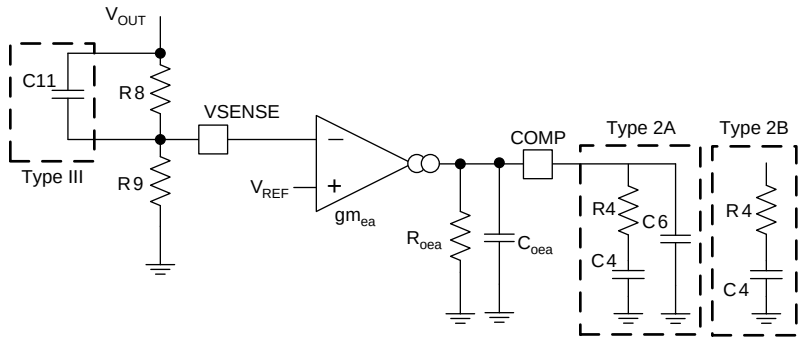


Figure 20. Types of Frequency Compensation

Feature Description (continued)

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, f_c. A good starting value for f_c is 1/10th of the switching frequency, f_{SW}.
2. Use Equation 10 to calculate the value of R4.

$$R4 = \frac{2\pi \times f_c \times V_{OUT} \times C_O}{gm_{ea} \times V_{REF} \times gm_{ps}} \quad (10)$$

   where
   - gm_{ea} is the GM amplifier gain (1300 μA/V)
   - gm_{ps} is the power stage gain (8 A/V)
   - V_{REF} is the reference voltage (0.8 V)

3. Place a compensation zero at the dominant pole and use Equation 11 to calculate the value of f_p.

$$\left(f_p = \frac{1}{C_O \times R_L \times 2\pi} \right) \quad (11)$$

4. Use Equation 12 to calculate the value of C4.

$$C4 = \frac{R_L \times C_O}{R4} \quad (12)$$

5. The use of C6 is optional. C6 can be used to cancel the zero from the ESR (equivalent series resistance) of the output capacitor C_O. If used, use Equation 13 to calculate the value of C6.

$$C6 = \frac{R_{ESR} \times C_O}{R4} \quad (13)$$

6. Type III compensation can be implemented with the addition of one capacitor, C11. The use of C11 allows for slightly higher loop bandwidths and higher phase margins. If used, use Equation 14 to calculate the value of C11.

$$C11 = \frac{1}{(2 \times \pi \times R8 \times f_C)} \quad (14)$$

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7.4 Device Functional Modes

7.4.1 Operation With V_I < 4.5 V (minimum V_I)

The device is designed to operate with input voltages above 4.5 V. The typical VIN UVLO threshold is 4V and if VIN falls below this threshold the device stops switching. If the EN pin voltage is above EN threshold the device becomes active when the VIN pin passes the UVLO threshold. .

7.4.2 Operation With EN Control

The enable threshold is 1.2-V typical. If the EN pin voltage is below this threshold the device does not switch even though the Vin is above the UVLO threshold. The IC quiescent current is reduced in this state. Once the EN is above the threshold with VIN above UVLO threshold the device is active again and the soft-start sequence is initiated.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS5433xA family of devices are step-down DC-DC converters. The devices are typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. Use the following design procedure to select component values for each device. Alternately, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.1.1 Supplementary Guidance

The device must operate within 150°C to ensure continuous function and operation of the device.

8.1.2 Differences Between the Two DRC Packages

The TPS54335A and TPS54335-1A devices are packaged in the same 3-mm × 3-mm SON package family which is designated as DRC (see the *メカニカル、パッケージ、および注文情報* section for all package options). However, these two DRC packages are not exactly the same.

The difference between these two DRC packages is the clearance between the pins and heat pad. Figure 21 shows a side-by-side picture of these two packages. In some applications, controlling the amount of solder paste during the assembly process of an application board is difficult. The risk of a pin-to-heat pad short (solder bridge) is possible in such an assembly process. The TPS54335-1A device is intended to support this type of application by having wider clearance.

NOTE

This heat-pad shape is the only difference between the TPS54335A and TPS54335-1A devices. The electrical functions and performances of both devices are the same. The thermal resistance and parameter values between these two packages are almost the same with negligible differences.

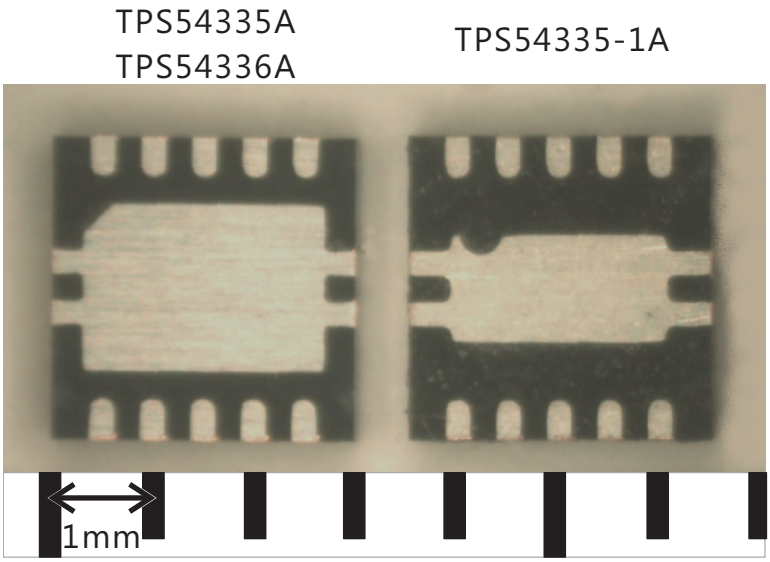


Figure 21. Difference Between the Two DRC Packages

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8.2 Typical Applications

TPS5433xA and TPS54335-1A typical application.

The application designs for the TPS54335A, TPS54335-1A, and TPS54336A devices are identical. The design for the TPS54336A device has small difference which is described in the section.

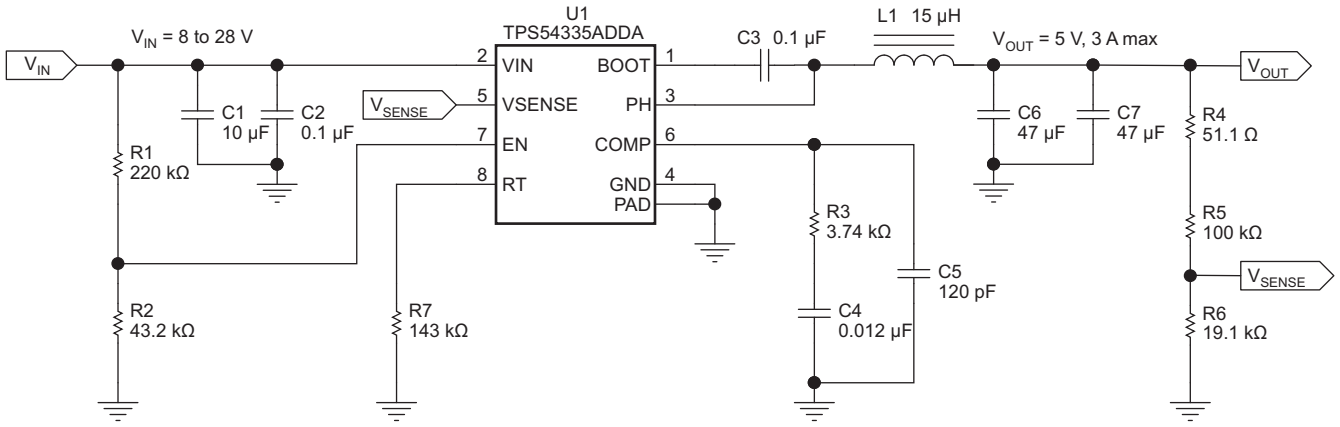


Figure 22. Typical Application Schematic, TPS54335A and TPS54335-1A

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 to 28 V
Output voltage	5 V
Transient response, 1.5-A load step	ΔV_O = ±5 %
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating Frequency	340 kHz

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8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54335A and TPS54336A devices. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process using the TPS54335A device.

For this design example, use the input parameters listed in Table 2.

8.2.2.1 Switching Frequency

The switching frequency of the TPS54335A device is set at 340 kHz to match the internally set frequency of the TPS54336A device for this design. Use to calculate the required value for R7. The calculated value is 140.6 kΩ. Use the next higher standard value of 143 kΩ for R7.

8.2.2.2 Output Voltage Set Point

The output voltage of the TPS54335A device is externally adjustable using a resistor divider network. In the application circuit of , this divider network is comprised of R5 and R6. Use Equation 15 and Equation 16 to calculate the relationship of the output voltage to the resistor divider.

$$R6 = \frac{R5 \times V_{ref}}{V_{OUT} - V_{ref}} \tag{15}$$

$$V_{OUT} = V_{ref} \times \left[\frac{R5}{R6} + 1\right] \tag{16}$$

Select a value of R5 to be approximately 100 kΩ. Slightly increasing or decreasing R5 can result in closer output-voltage matching when using standard value resistors. In this design, R5 = 100 kΩ and R6 = 19.1 kΩ which results in a 4.988-V output voltage. The 51.1-Ω resistor, R4, is provided as a convenient location to break the control loop for stability testing.

8.2.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) set point can be adjusted using the external-voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS54335A device. R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the minimum input voltage is 8 V, so the start-voltage threshold is set to 7.15 V with 1-V hysteresis. Use Equation 2 and Equation 3 to calculate the values for the upper and lower resistor values of R1 and R2.

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8.2.2.4 Input Capacitors

The TPS54335A device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 μF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however a 10-μF capacitor has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54335A circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design, a 10-μF, X7R dielectric capacitor rated for 35 V is used for the input decoupling capacitor. The ESR is approximately 2 mΩ, and the current rating is 3 A. Additionally, a small 0.1-μF capacitor is included for high frequency filtering.

Use Equation 17 to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (17)$$

where

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum load current
- ESR_{MAX} is the maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use Equation 18 to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{O(MAX)}}{2} \quad (18)$$

In this case, the input ripple voltage is 227 mV and the RMS ripple current is 1.5 A.

NOTE

The actual input-voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

The *Design Requirements* section shows the actual input voltage ripple for this circuit which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is $V_{IN(MAX)} + \Delta V_{IN} / 2$. The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 3 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

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8.2.2.5 Output Filter Components

Two components must be selected for the output filter, the output inductor (L_O) and C_O. Because the TPS54335A device is an externally compensated device, a wide range of filter component types and values can be supported.

8.2.2.5.1 Inductor Selection

Use Equation 19 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (19)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as K_{IND} = 0.3 can be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3. The minimum inductor value is calculated as 13.4 µH. For this design, a close standard value of 15 µH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 20 to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \right)^2} \quad (20)$$

Use Equation 21 to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times f_{SW}} \quad (21)$$

For this design, the RMS inductor current is 3.002 A and the peak inductor current is 3.503 A. The selected inductor is a Coilcraft 15 µH, XAL6060-153MEB. This inductor has a saturation current rating of 5.8 A and an RMS current rating of 6 A which meets the requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple. In general, for the TPS54335A device, use inductors with values in the range of 0.68 µH to 100 µH.

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8.2.2.5.2 Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use Equation 22 to calculate the minimum required output capacitance.

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$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency of the regulator
- ΔV_{OUT} is the allowable change in the output voltage (22)

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT}, for a load step of 1.5 A. For this example, ΔI_{OUT} = 1.5 A and ΔV_{OUT} = 0.05 × 5 = 0.25 V. Using these values results in a minimum capacitance of 35.3 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 23 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 23 yields 12.3 µF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}}$$

where

- f_{SW} is the switching frequency
- $V_{OUTripple}$ is the maximum allowable output voltage ripple
- I_{ripple} is the inductor ripple current (23)

Use Equation 24 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 24 indicates the ESR should be less than 29.8 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 29.8 mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}} \tag{24}$$

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 47-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 25 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 25 yields 116.2 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times N_C} \right) \tag{25}$$

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8.2.2.6 Compensation Components

Several possible methods exist to design closed loop compensation for DC-DC converters. For the ideal current-mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and begins to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees which is one decade above the modulator pole frequency. Use Equation 26 to calculate the simple modulator pole (f_{p_mod}).

$$f_{p_mod} = \frac{I_{OUT}\,max}{2\pi \times V_{OUT} \times C_{OUT}} \tag{26}$$

For the TPS54335A device, most circuits have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics deviate from the ideal approximations. The phase loss of the power stage will now approach –180 degrees, making compensation more difficult. The power stage transfer function can be solved but it requires a tedious calculation. Use the PSpice model to accurately model the power-stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct measurement of the power stage characteristics can be used which is the technique used in this design procedure. For this design, the calculated values are as follows:

L1 = 15 µH

C6 and C7 = 47 µF

ESR = 3 mΩ

Figure 23 shows the power stage characteristics.

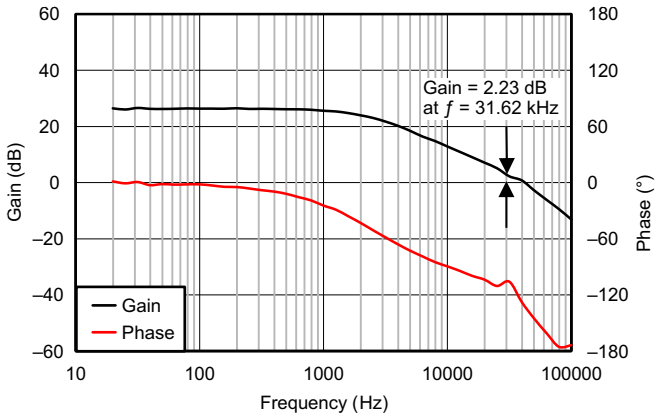


Figure 23. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 31.62 kHz (an actual measured data point exists for that frequency). From the power stage gain and phase plots, the gain at 31.62 kHz is 2.23 dB and the phase is about -106 degrees. For 60 degrees of phase margin, additional phase boost from a feed-forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. Use Equation 27 to calculate the required value of R3.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{ea}} \times \frac{V_{OUT}}{V_{REF}} \quad (27)$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 31.62 kHz. Use Equation 28 to calculate the required value for C4.

$$C4 = \frac{1}{2 \times \pi \times R3 \times \frac{f_{CO}}{10}} \quad (28)$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 31.62 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. Use Equation 29 to calculate the value of C5.

$$C5 = \frac{1}{2 \times \pi \times R3 \times 10 \times f_{CO}} \quad (29)$$

For this design the calculated values for the compensation components are as follows:

R3 = 3.74 kΩ
C4 = 0.012 µF
C5 = 120 pF

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8.2.2.7 Bootstrap Capacitor

Every TPS54335A design requires a bootstrap capacitor, C3. The bootstrap capacitor value must 0.1 μF. The bootstrap capacitor is located between the PH and BOOT pins. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.8 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode operations. These formulas should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse-skipping Eco-mode™.

The device power dissipation includes:

1. Conduction loss:

$$P_{CON} = I_{OUT}^2 \times r_{DS(on)} \times V_{OUT} / V_{IN}$$

where

- I_{OUT} is the output current (A)
- $r_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
- V_{OUT} is the output voltage (V)
- V_{IN} is the input voltage (V)

(30)

2. Switching loss:

$$E = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{SW}$$

where

- f_{SW} is the switching frequency (Hz)

(31)

3. Gate charge loss:

$$P_G = 22.8 \times 10^{-9} \times f_{SW}$$

(32)

4. Quiescent current loss:

$$P_Q = 0.11 \times 10^{-3} \times V_{IN}$$

(33)

Therefore:

$$P_{tot} = P_{CON} + E + P_G + P_Q$$

where

- P_{tot} is the total device power dissipation (W)

(34)

For given T_A :

$$T_J = T_A + R_{th} \times P_{tot}$$

where

- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- R_{th} is the thermal resistance of the package (°C/W)

(35)

For given $T_J$max = 150°C:

$$T_A\text{max} = T_J\text{max} - R_{th} \times P_{tot}$$

where

- $T_A$max is the maximum ambient temperature (°C)
- $T_J$max is the maximum junction temperature (°C)

(36)

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8.2.3 Application Curves

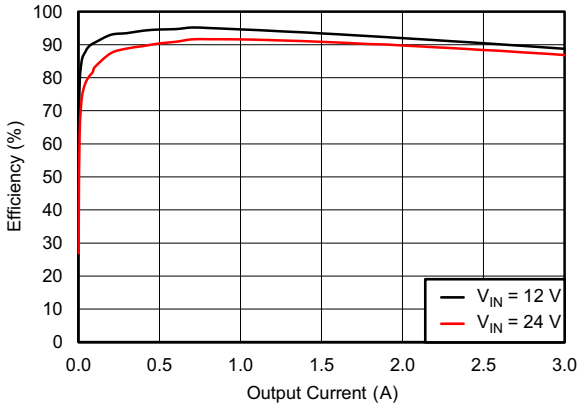


Figure 24. TPS54335A Efficiency

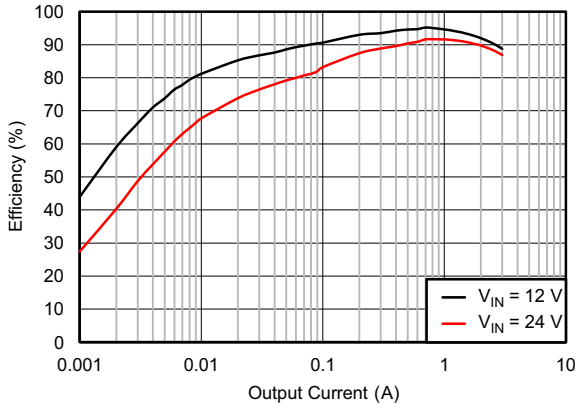


Figure 25. TPS54335A Low-Current Efficiency

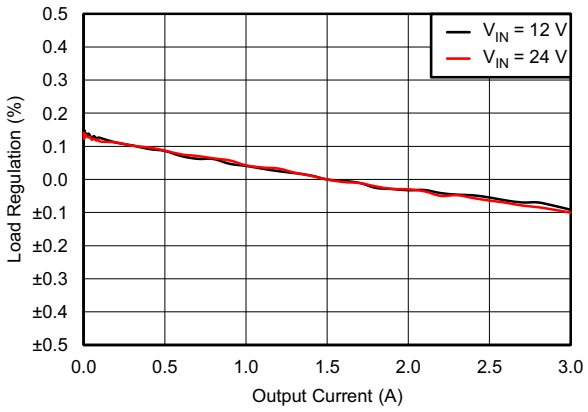


Figure 26. TPS54335A Load Regulation

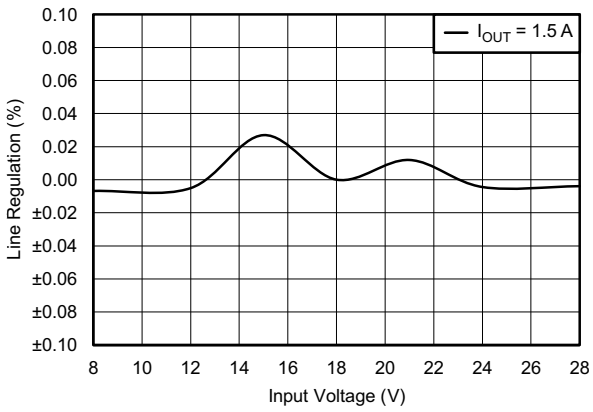


Figure 27. TPS54335A Line Regulation

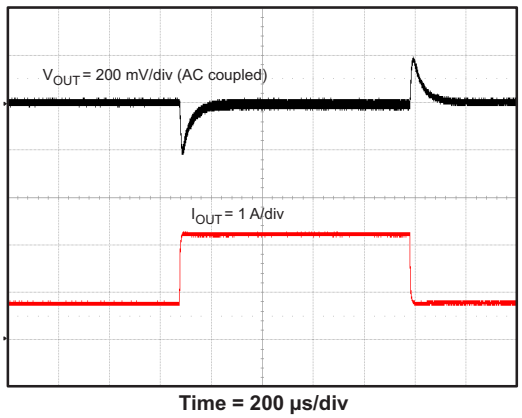


Figure 28. TPS54335A Transient Response

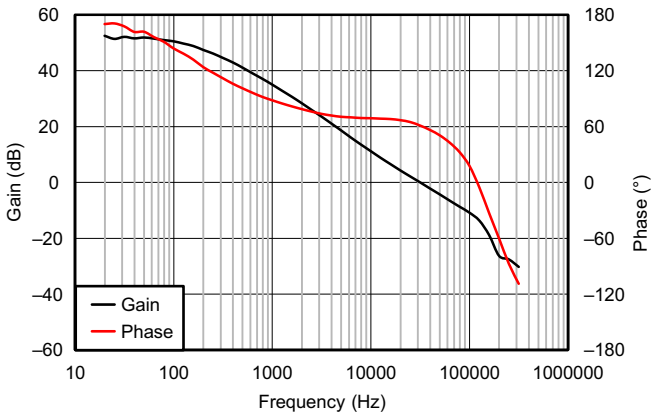


Figure 29. TPS54335A Loop Response

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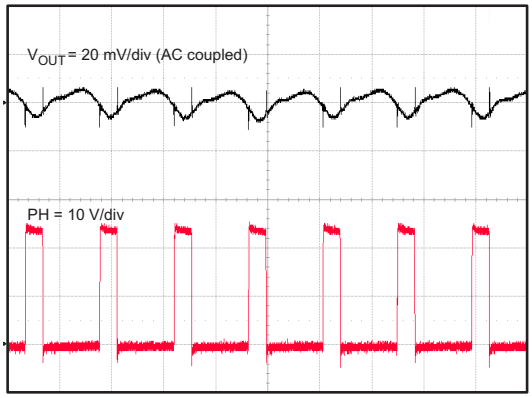


Figure 30. TPS54335A Full-Load Output Ripple

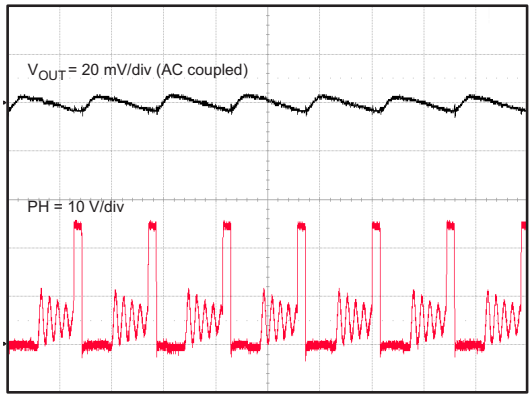


Figure 31. TPS54335A 100-mA Output Ripple

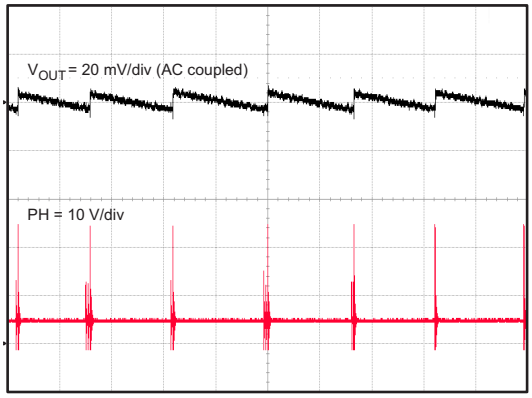


Figure 32. TPS54335A No-Load Output Ripple

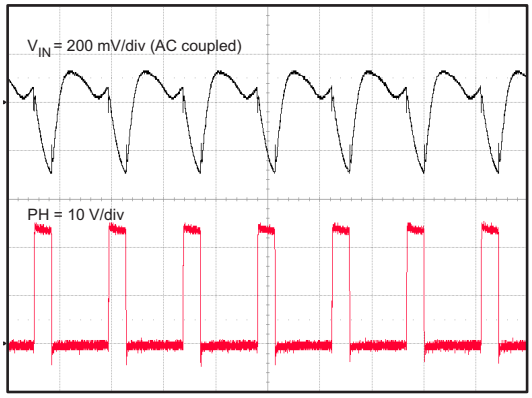


Figure 33. TPS54335A Full-Load Input Ripple

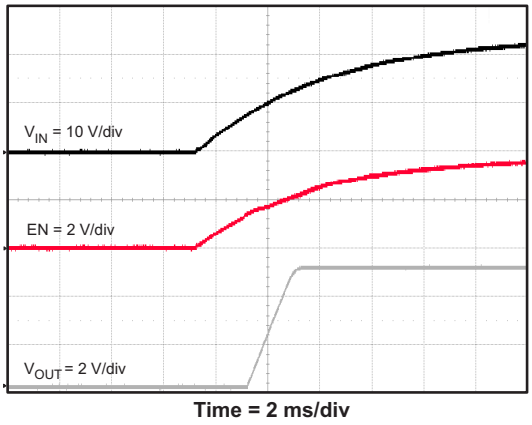


Figure 34. TPS54335A Startup Relative To VIN

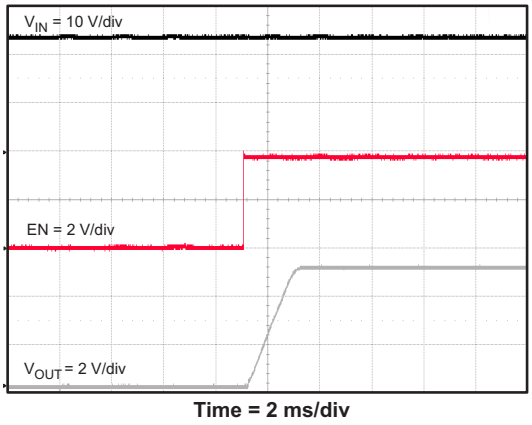


Figure 35. TPS54335A Startup Relative To Enable

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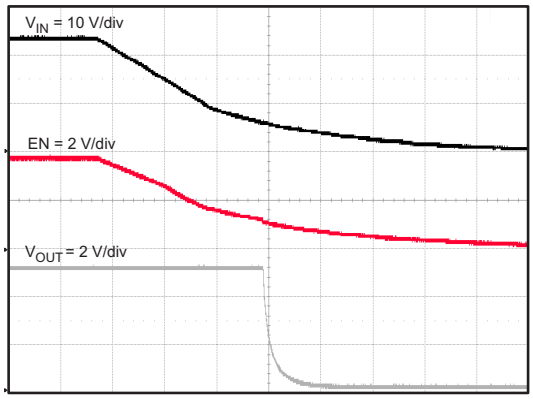


Figure 36. TPS54335A Shutdown Relative To VIN

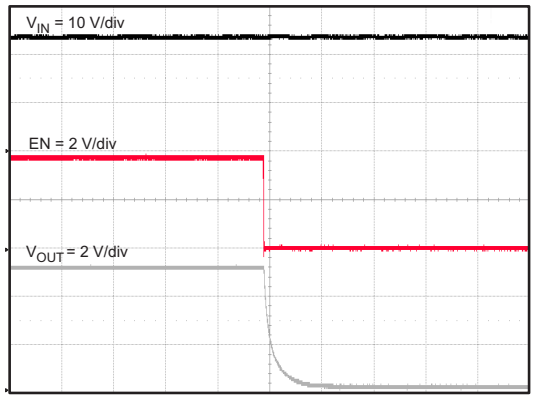


Figure 37. TPS54335A Shutdown Relative To EN

8.2.4 TPS54336A Typical Application

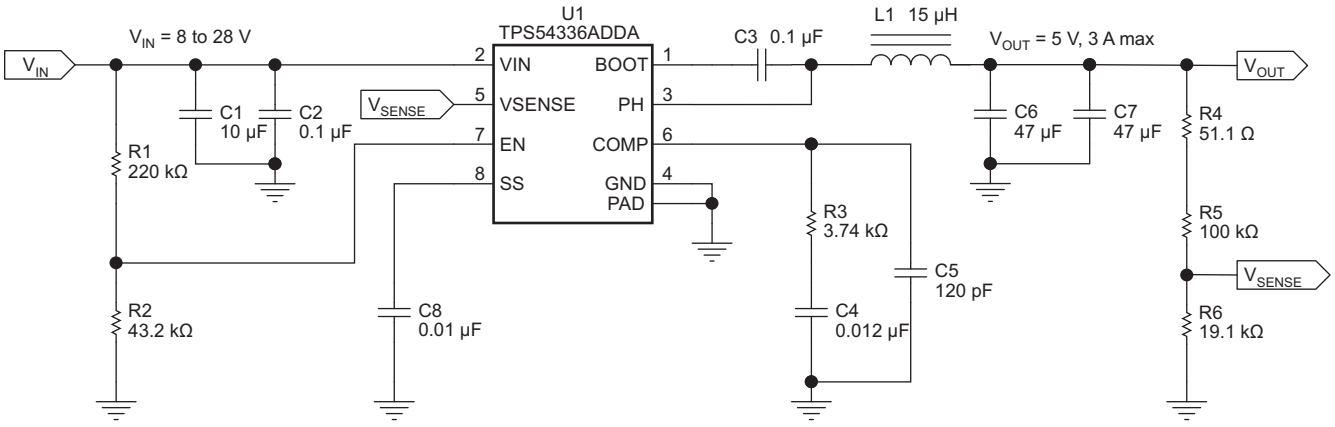


Figure 38. Typical Application Schematic, TPS54336A

8.2.4.1 Design Requirements

For this design example, use the parameters listed in .

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 to 28 V
Output voltage	5 V
Transient response, 1.5-A load step	ΔV_{OUT} = ±5 %
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Soft-start time	3.5 ms

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8.2.4.2 Detailed Design Procedure

8.2.4.2.1 TPS54336A Design

The design procedure for the TPS54336A device is identical to the TPS54335A device, except that the TPS54336A device uses a soft-start circuit rather than an externally set switching frequency at pin 8. The switching frequency is internally set for 340 kHz.

8.2.4.2.2 Soft-Start Capacitor

The soft-start capacitor determines the minimum amount of time required for the output voltage to reach the nominal programmed value during power up. This feature is useful if a load requires a controlled-voltage slew rate. This feature is also used if the output capacitance is very large and requires large amounts of current to quickly charge the capacitor to the output voltage level. The large currents required to charge the capacitor can cause the TPS54336A device to reach the current-limit. Excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. Use to calculate the value of the soft-start capacitor. For the example circuit, the soft-start time is not too critical because the output capacitor value is 2 × 47 µF which does not require much current to charge to 5 V. The example circuit has the soft-start time set to an arbitrary value of 3.5 ms which requires a 10-nF capacitor. For the TPS54336A device, the calculated values are as follows:

I_{SS} = 2.3 µA
V_{REF} = 0.8 V

8.2.4.3 Application Curves

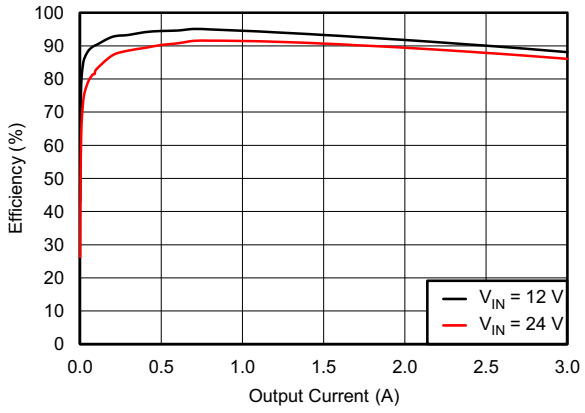


Figure 39. TPS54336A Efficiency

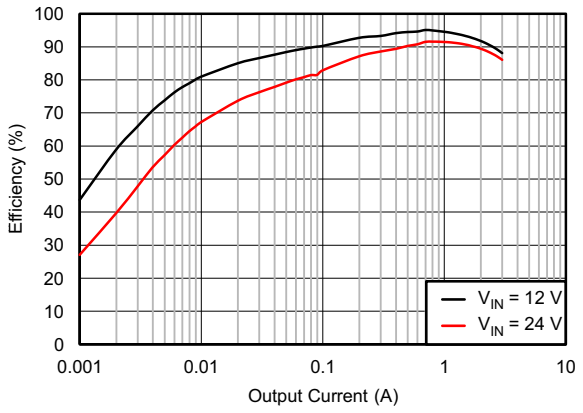


Figure 40. TPS54336A Low-Current Efficiency

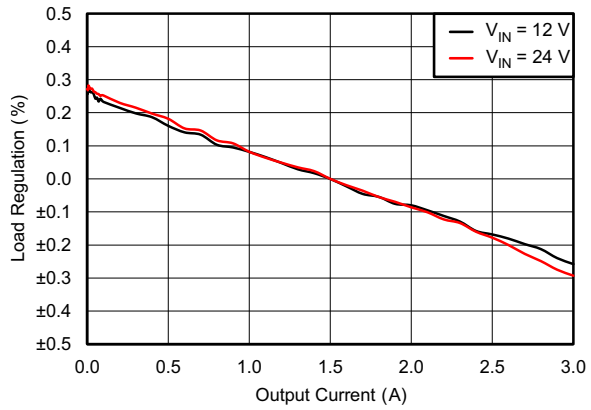


Figure 41. TPS54336A DDA Load Regulation

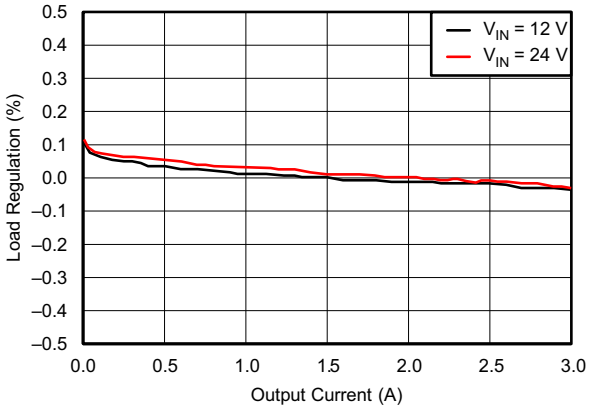


Figure 42. TPS54336A DRC Load Regulation

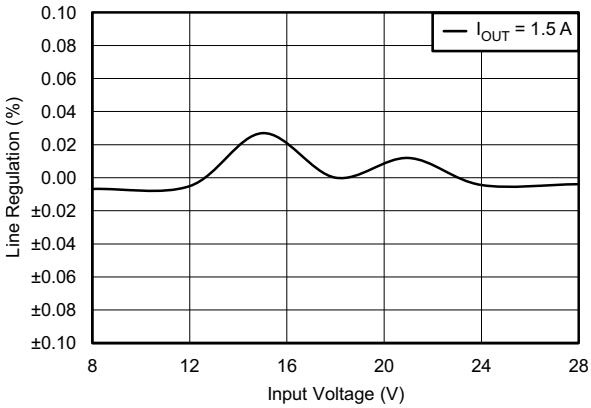
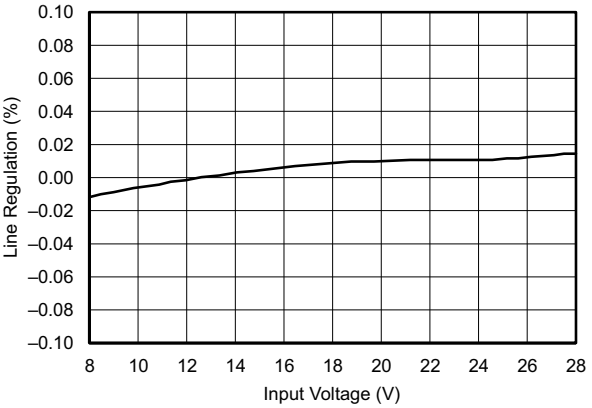
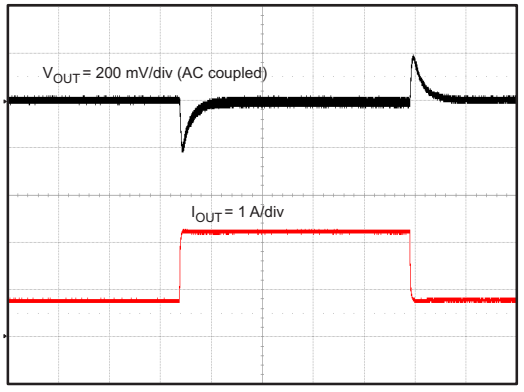


Figure 43. TPS54336A DDA Line Regulation



I_{OUT} = 1.5 A

Figure 44. TPS54336A DRC Line Regulation



Time = 200 µs/div

0.75- to 2.25-A load step Slew rate = 500 mA/µs

Figure 45. TPS54336A Transient Response

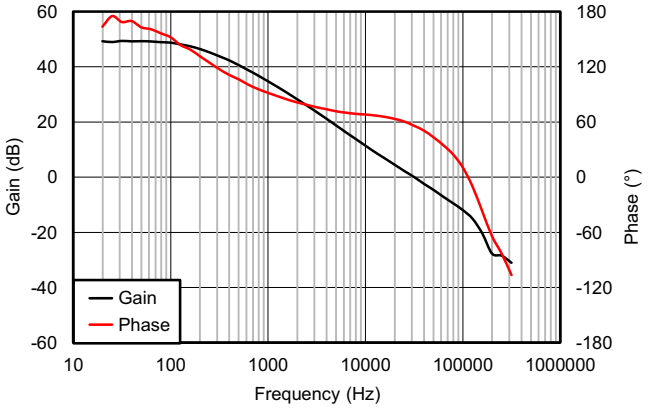


Figure 46. TPS54336A Loop Response

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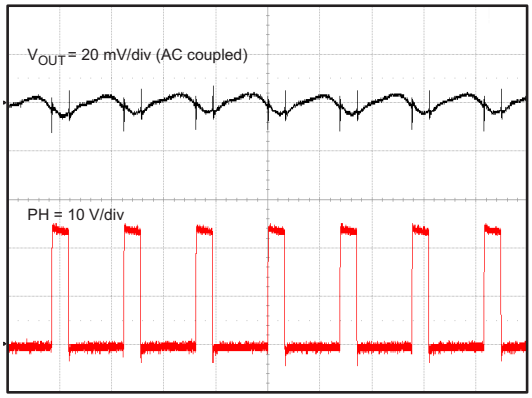


Figure 47. TPS54336A Full-Load Output Ripple

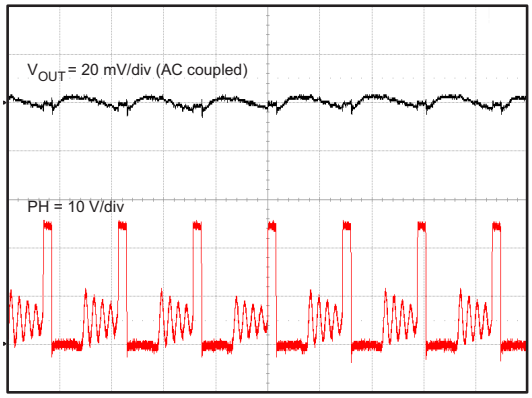


Figure 48. TPS54336A 100-mA Output Ripple

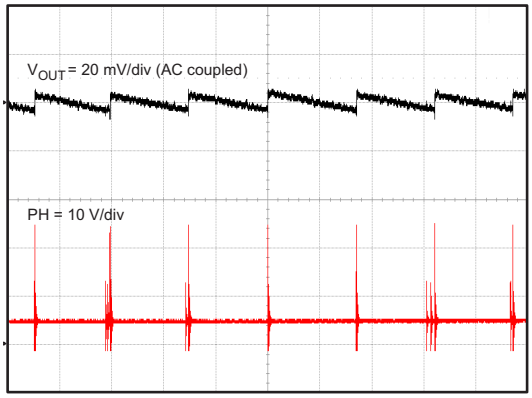


Figure 49. TPS54336A No-Load Output Ripple

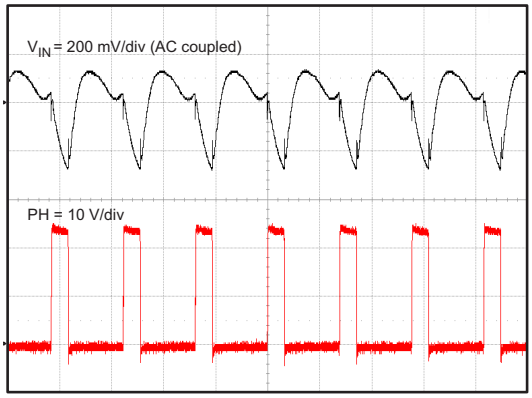


Figure 50. TPS54336A Full- Load Input Ripple

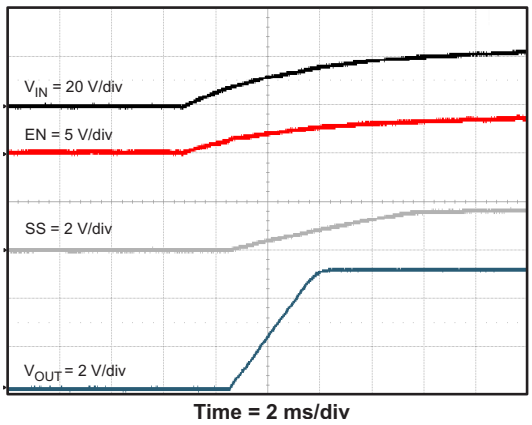


Figure 51. TPS54336A Startup Relative to VIN

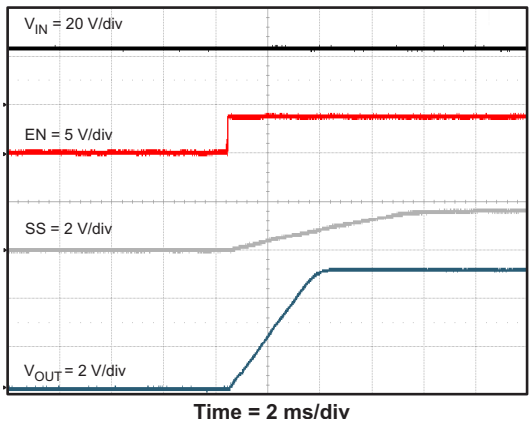


Figure 52. TPS54336A Startup Relative to Enable

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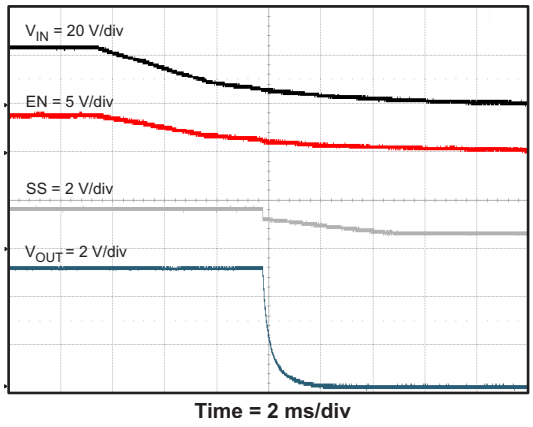


Figure 53. TPS54336A Shutdown Relative to VIN

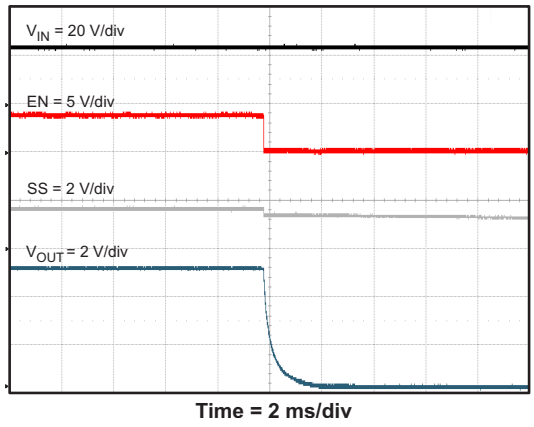


Figure 54. TPA54336A Shutdown Relative to EN

9 Power Supply Recommendations

The devices are designed to operate from an input supply ranging from 4.5 V to 28 V. The input supply should be well regulated. If the input supply is located more than a few inches from the converter an additional bulk capacitance typically 100 µF may be required in addition to the ceramic bypass capacitors.

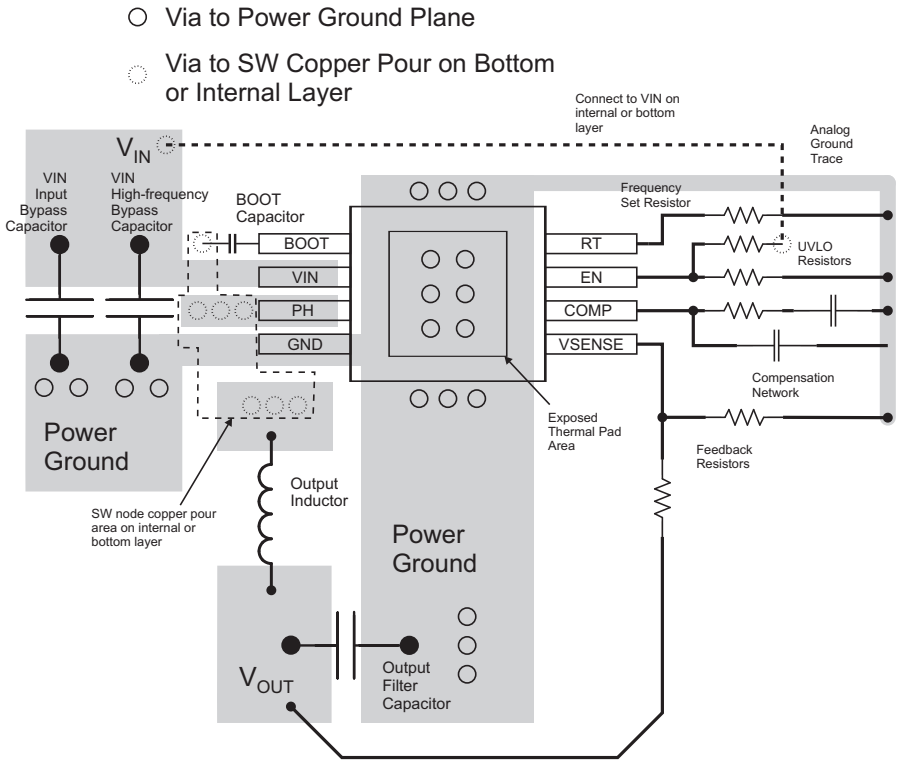
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10 Layout

10.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10-μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. See Figure 55 for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. To facilitate close placement of the input bypass capacitors, the PH pin should be routed to a small copper area directly adjacent to the pin. Use vias to route the PH signal to the bottom side or an inner layer. If necessary, allow the top-side copper area to extend slightly under the body of the closest input bypass capacitor. Make the copper trace on the bottom or internal layer short and wide as practical to reduce EMI issues. Connect the trace with vias back to the top side to connect with the output inductor as shown after the GND pin. In the same way use a bottom or internal layer trace to route the PH signal across the VIN pin to connect to the boot capacitor as shown. Make the circulating loop from the PH pin to the output inductor and output capacitors and then back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper . For operation at a full rated load, the ground area near the IC must provide adequate heat dissipating area. Connect the exposed thermal pad to the bottom or internal layer ground plane using vias as shown. Additional vias may be used adjacent to the IC to tie top-side copper to the internal or bottom layer copper. The additional external components can be placed approximately as shown. Use a separate ground trace to connect the feedback, compensation, UVLO, and RT (SS for TPS54336A) returns. Connect this ground trace to the main power ground at a single point to minimize circulating currents. Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

10.2 Layout Example



Note: Pin 8 for the TPS54336A device is SS. Connect an SS capacitor instead of an RT resistor from pin 8 to GND.

Figure 55. TPS54335ADDA Board Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

WEBENCH回路設計と選択シミュレーション・サービスについては、www.ti.com/WEBENCHを参照してください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下をを参照してください：

『電流モード降圧型コンバータ用のタイプIII補償回路の設計』(SLVA352)

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS54335A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS54335-1A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS54336A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商標

PowerPAD, Eco-mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54335-1ADRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543351
TPS54335-1ADRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543351
TPS54335-1ADRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543351
TPS54335-1ADRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543351
TPS54335-1ADRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543351
TPS54335-1ADRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	543351
TPS54335ADDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADDARG4.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54335A
TPS54335ADRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54335A
TPS54335ADRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54335A
TPS54336ADDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	54336A
TPS54336ADDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54336A
TPS54336ADDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	54336A
TPS54336ADDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54336A
TPS54336ADDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54336A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54336ADDARG4.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54336A
TPS54336ADRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54336A
TPS54336ADRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54336A
TPS54336ADRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54336A
TPS54336ADRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54336A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

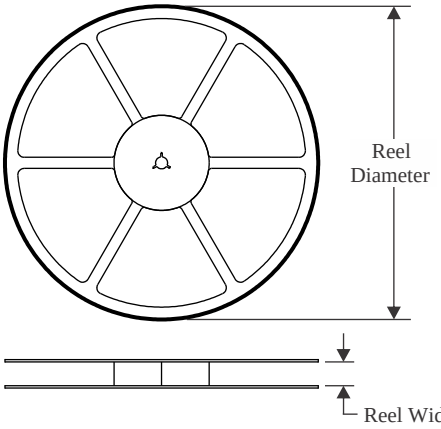
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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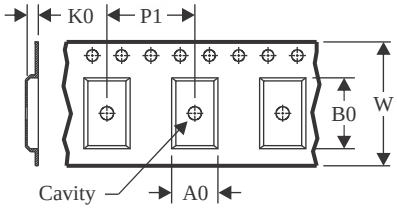
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

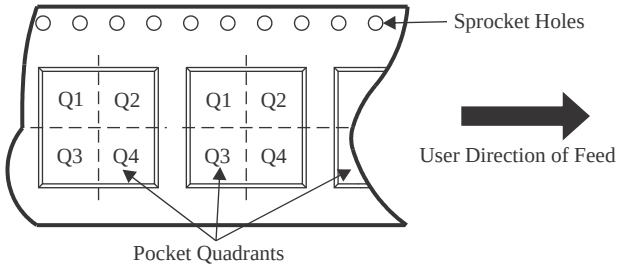


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

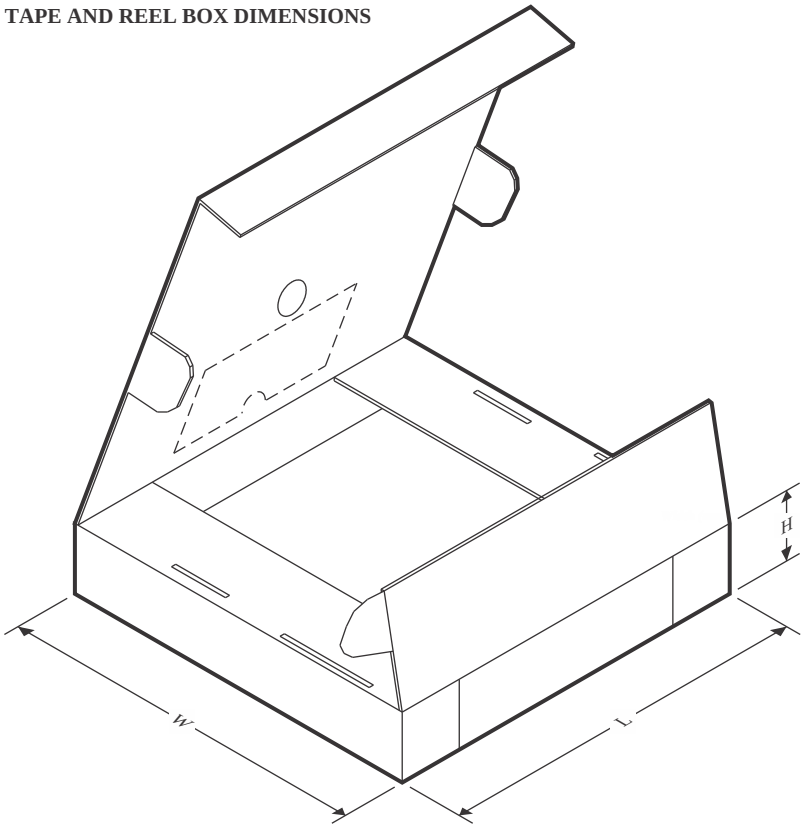
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54335-1ADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54335-1ADRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54335-1ADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54335ADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54335ADRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54335ADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54336ADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54336ADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

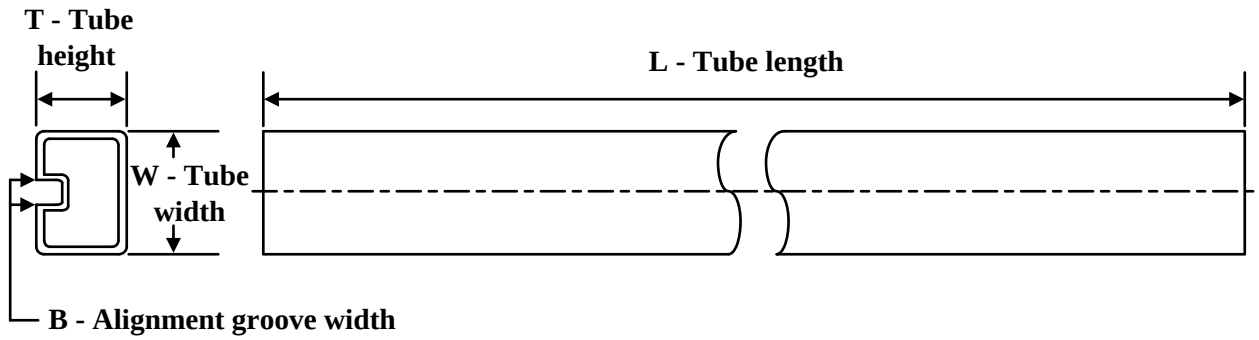
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54335-1ADRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS54335-1ADRCRG4	VSON	DRC	10	3000	346.0	346.0	33.0
TPS54335-1ADRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS54335ADRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS54335ADRCRG4	VSON	DRC	10	3000	346.0	346.0	33.0
TPS54335ADRCT	VSON	DRC	10	250	182.0	182.0	20.0
TPS54336ADRCR	VSON	DRC	10	3000	335.0	335.0	25.0
TPS54336ADRCT	VSON	DRC	10	250	182.0	182.0	20.0

TUBE

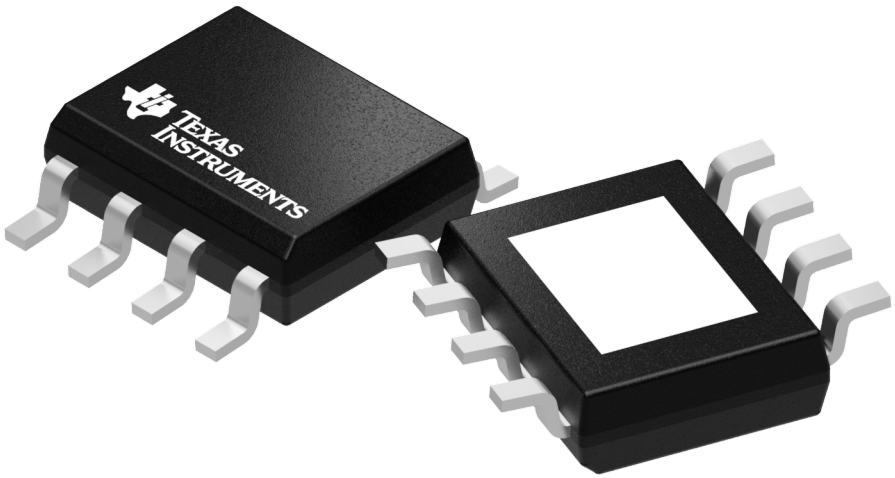


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54335ADDA.A	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54335ADDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54336ADDA	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54336ADDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54336ADDA.A	DDA	HSOIC	8	75	507	8	3940	4.32
TPS54336ADDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25

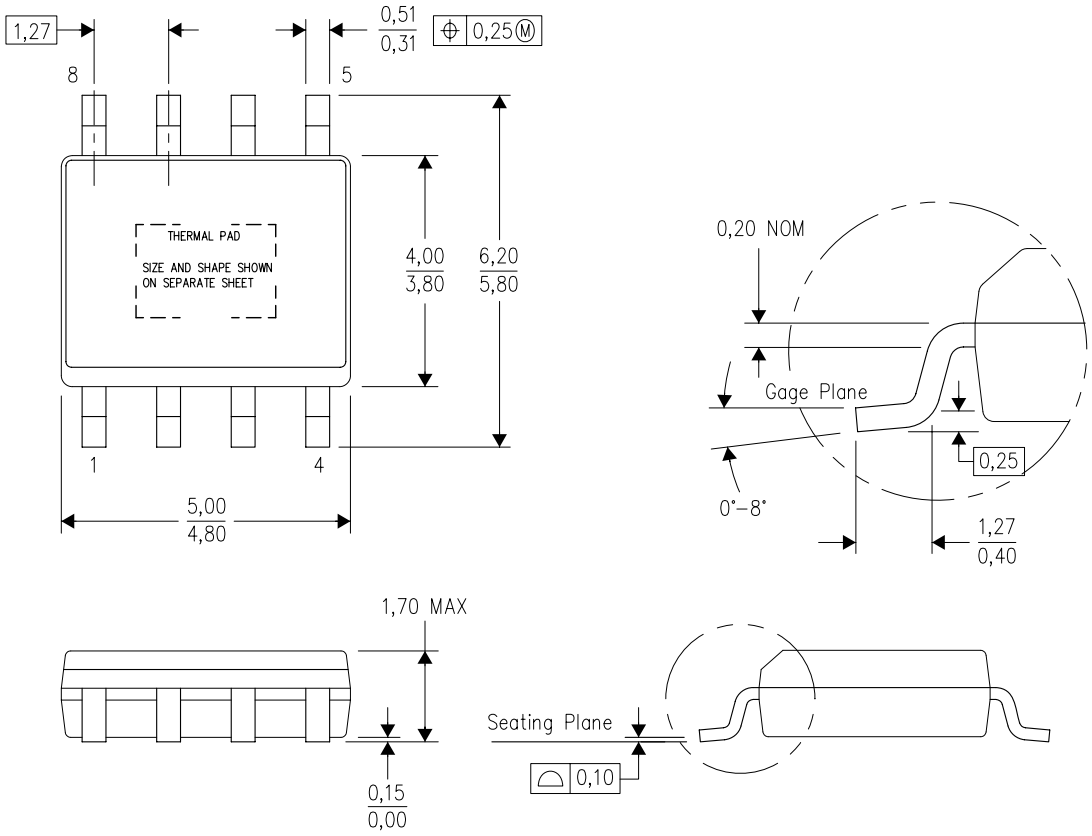
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

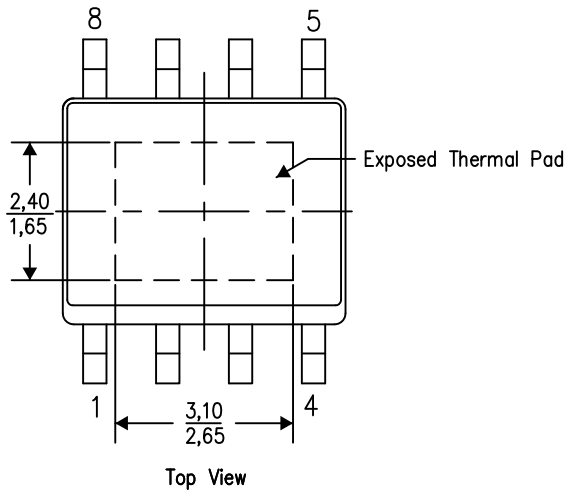
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



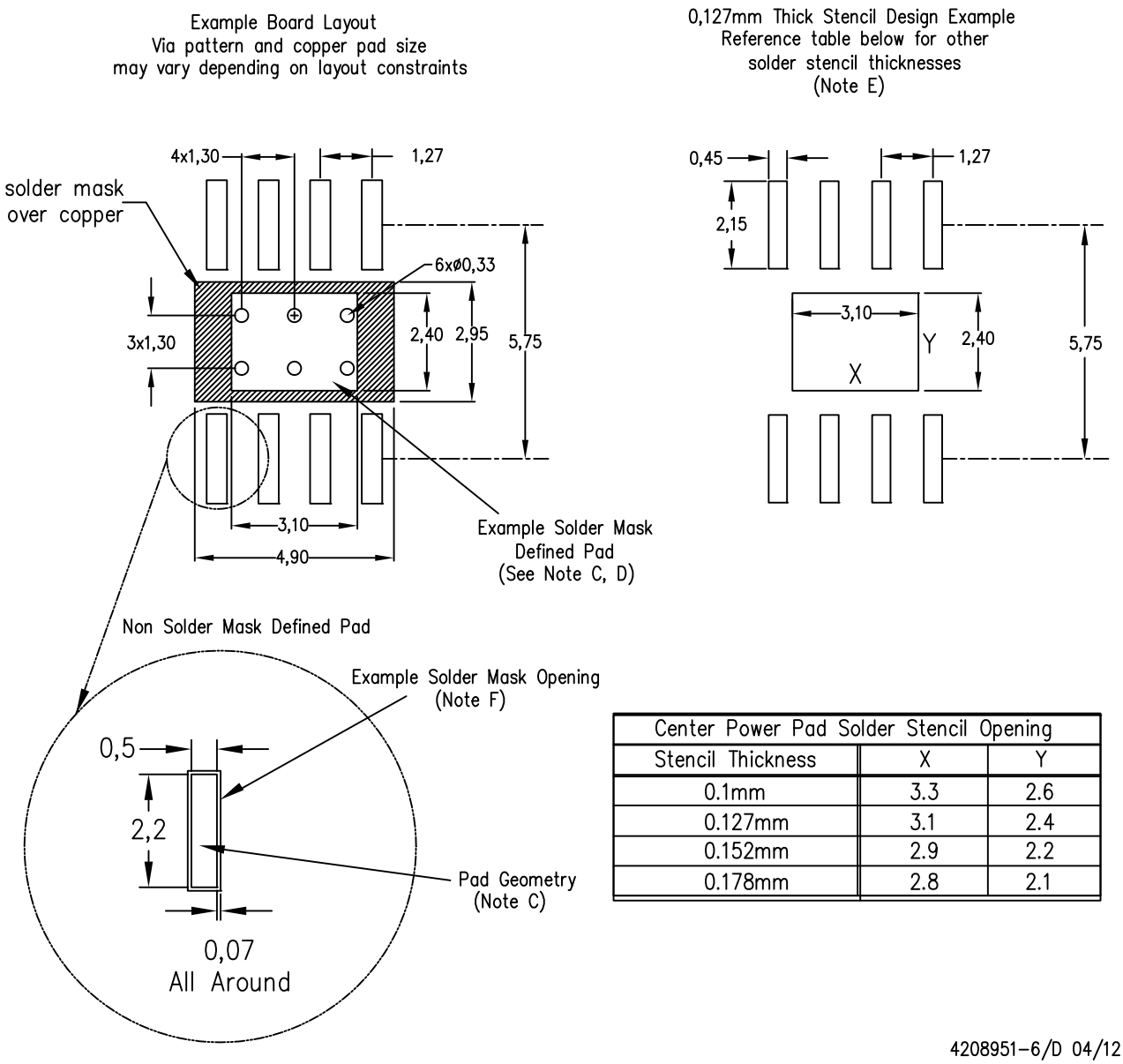
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

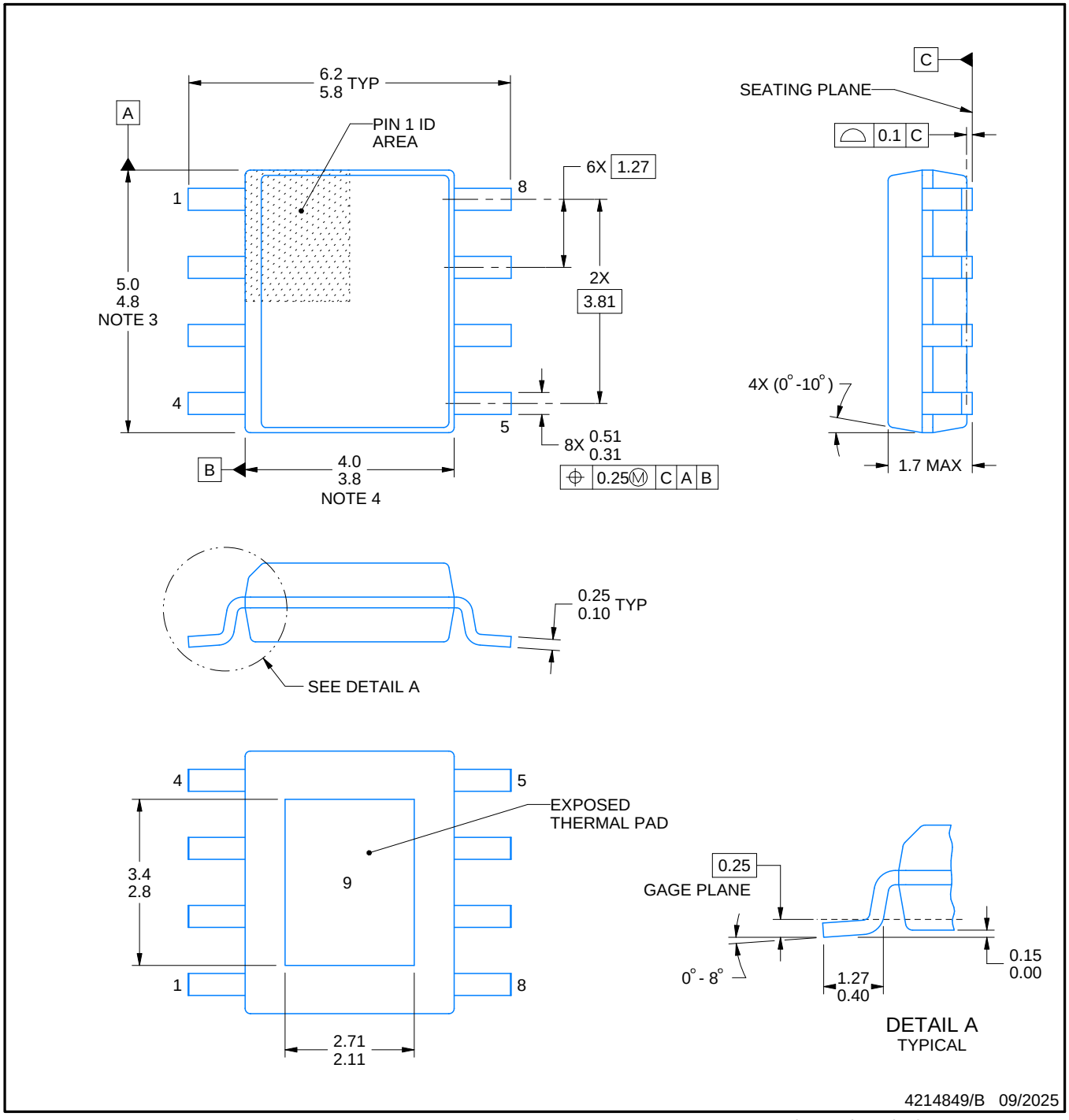
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

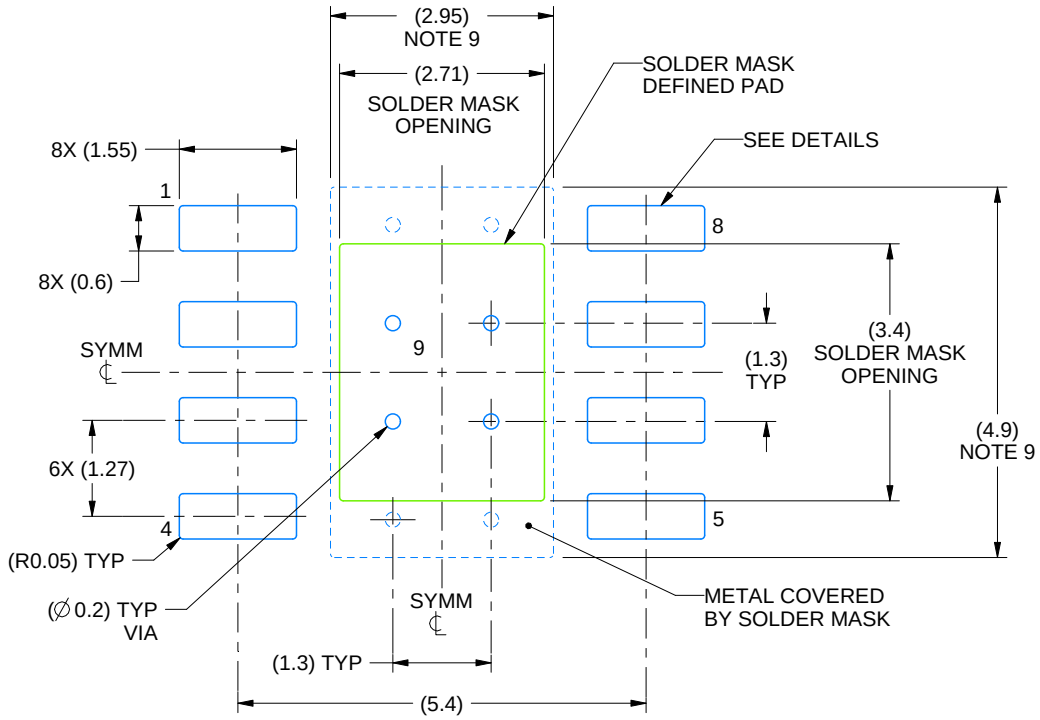
PLASTIC SMALL OUTLINE



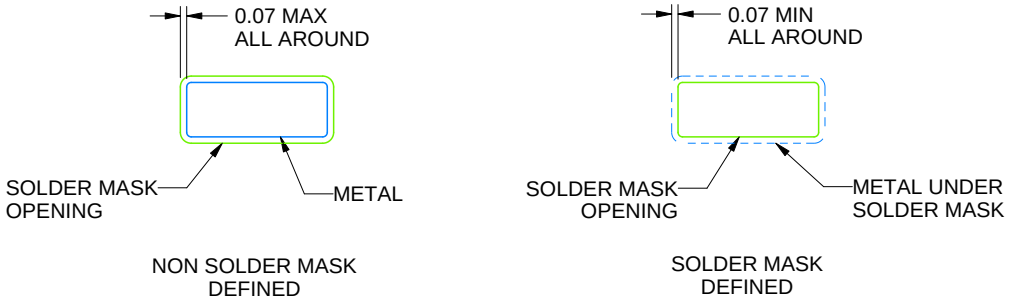
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

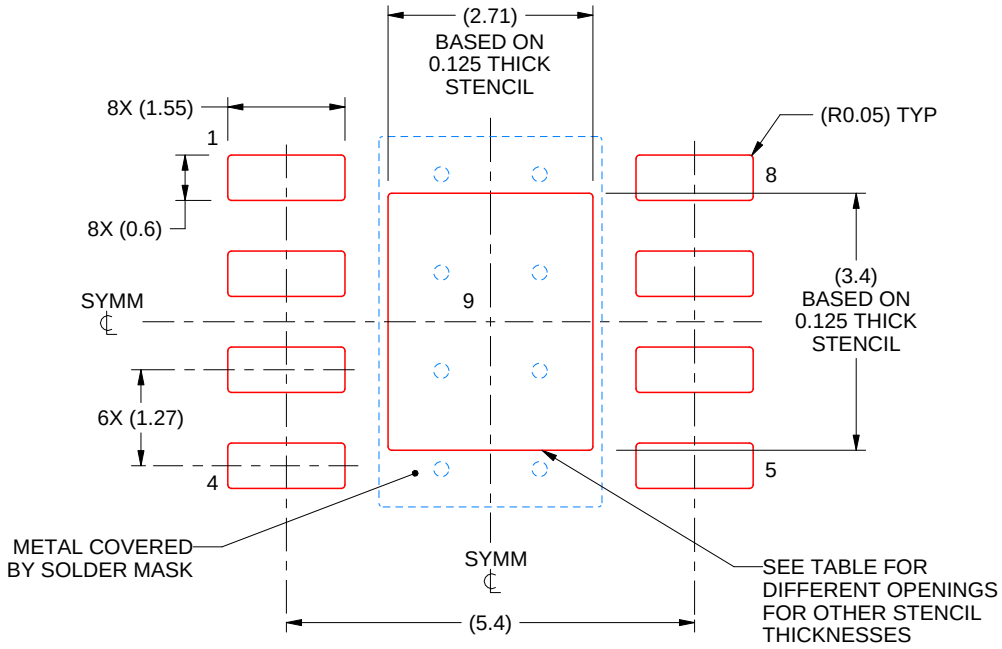
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

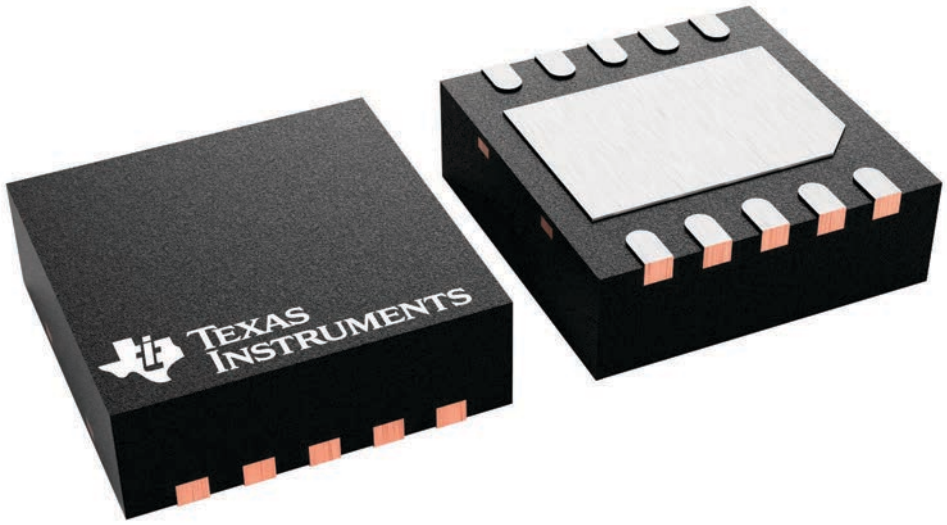
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



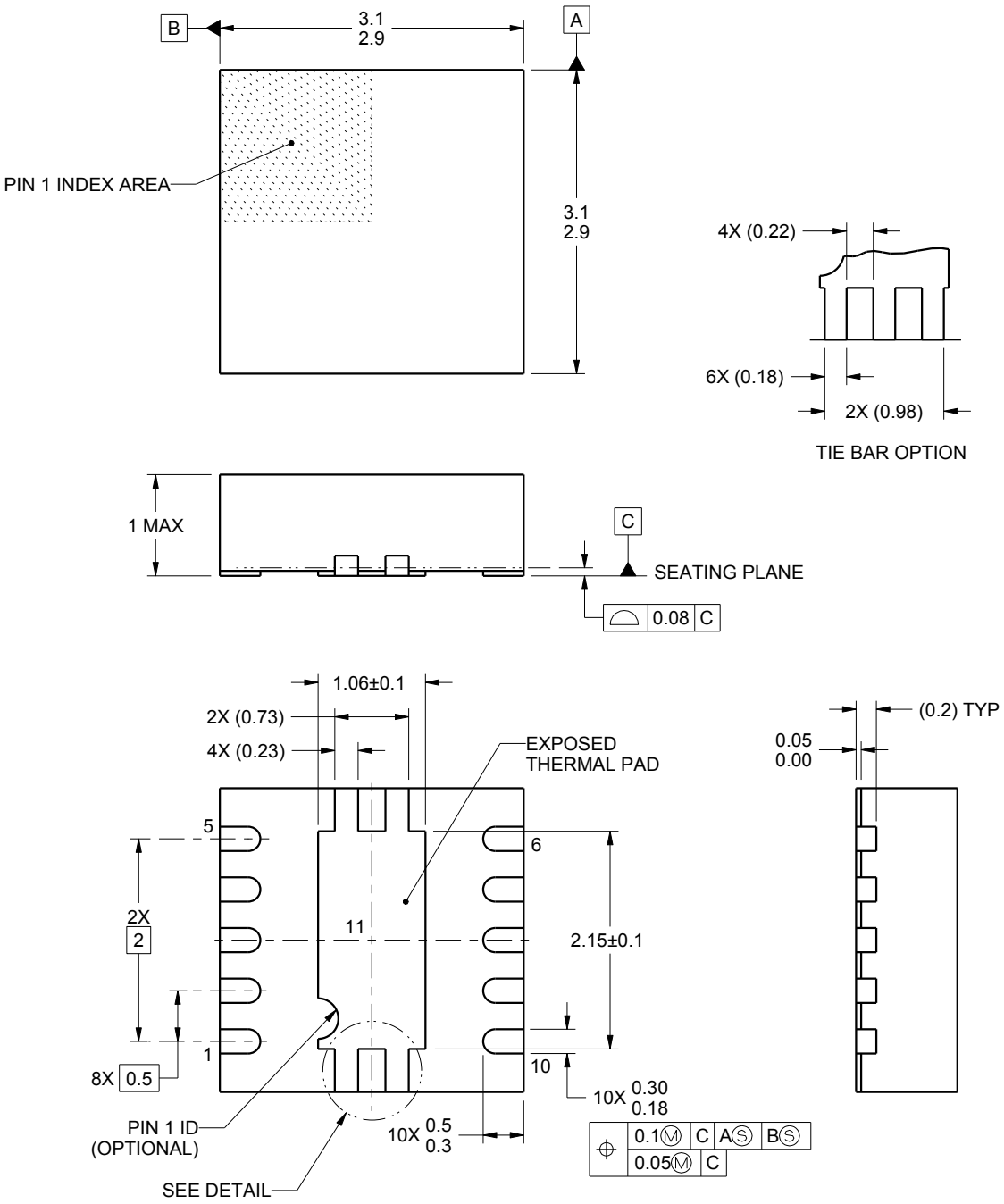
4226193/A

PACKAGE OUTLINE

DRC0010M

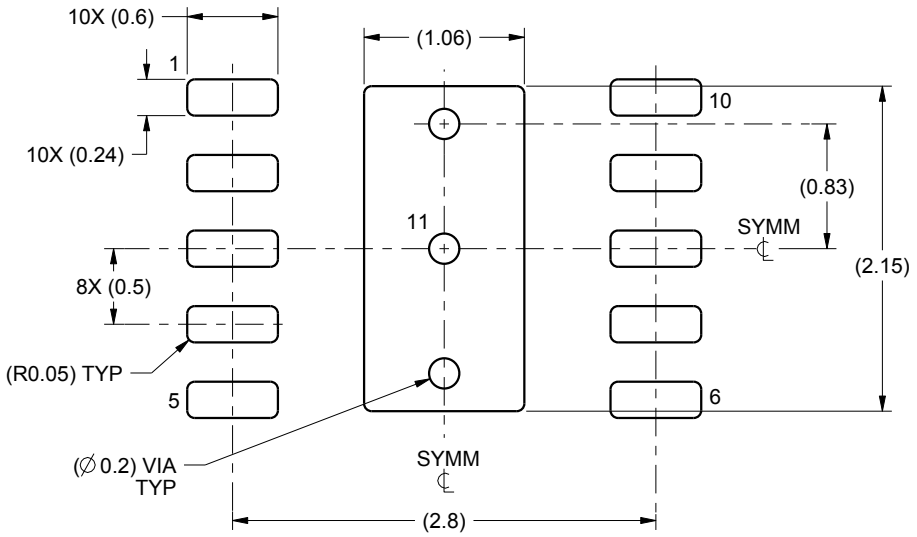
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

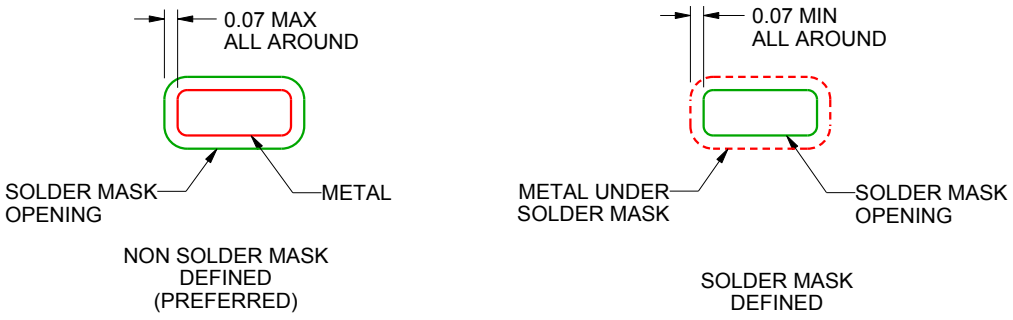


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

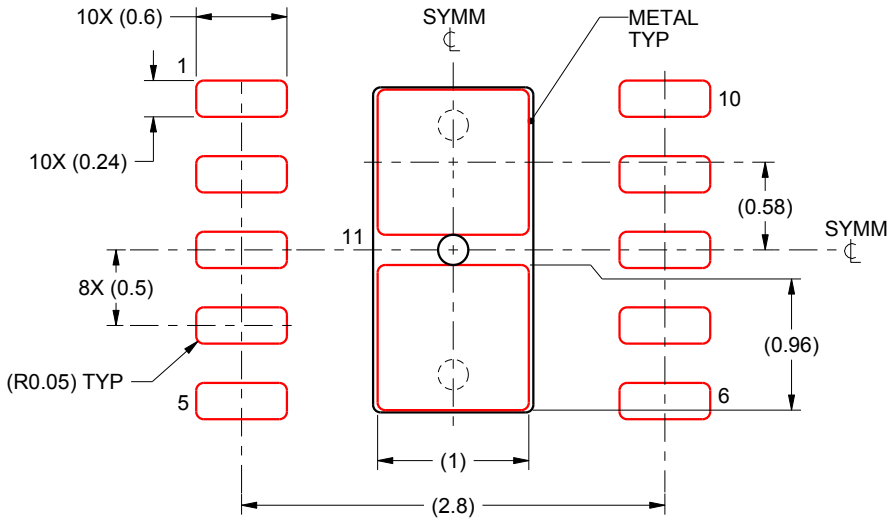


SOLDER MASK DETAILS

4222672/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222672/A 02/2016

NOTES: (continued)

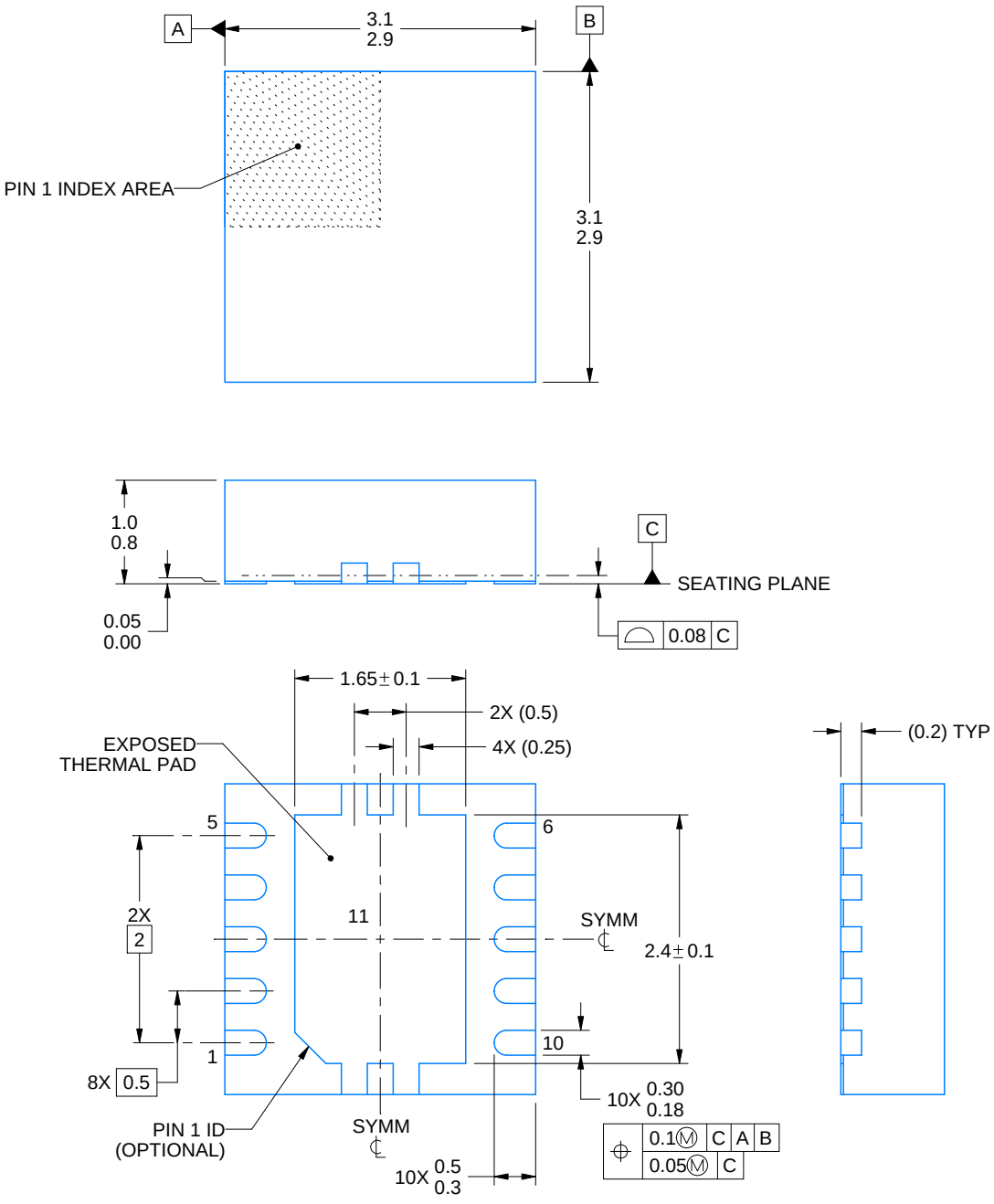
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRC0010J

PACKAGE OUTLINE

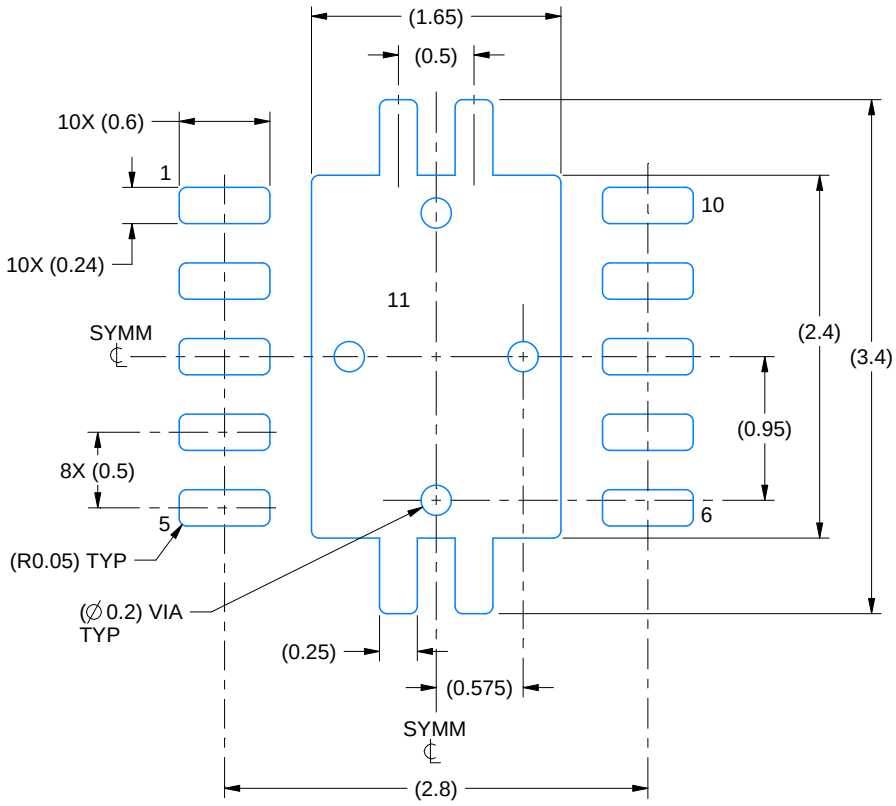
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

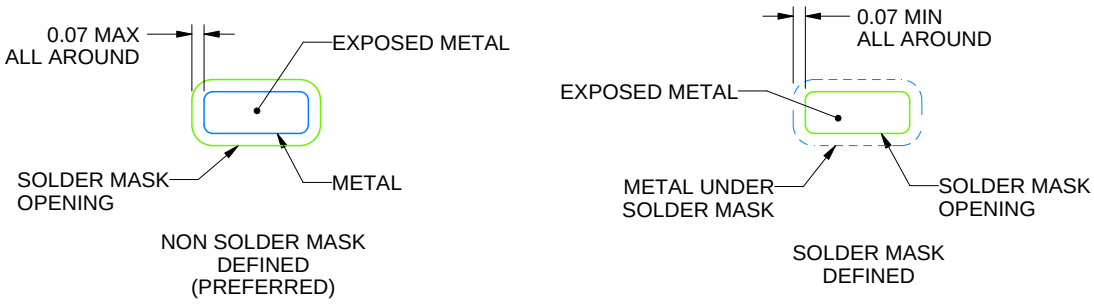


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

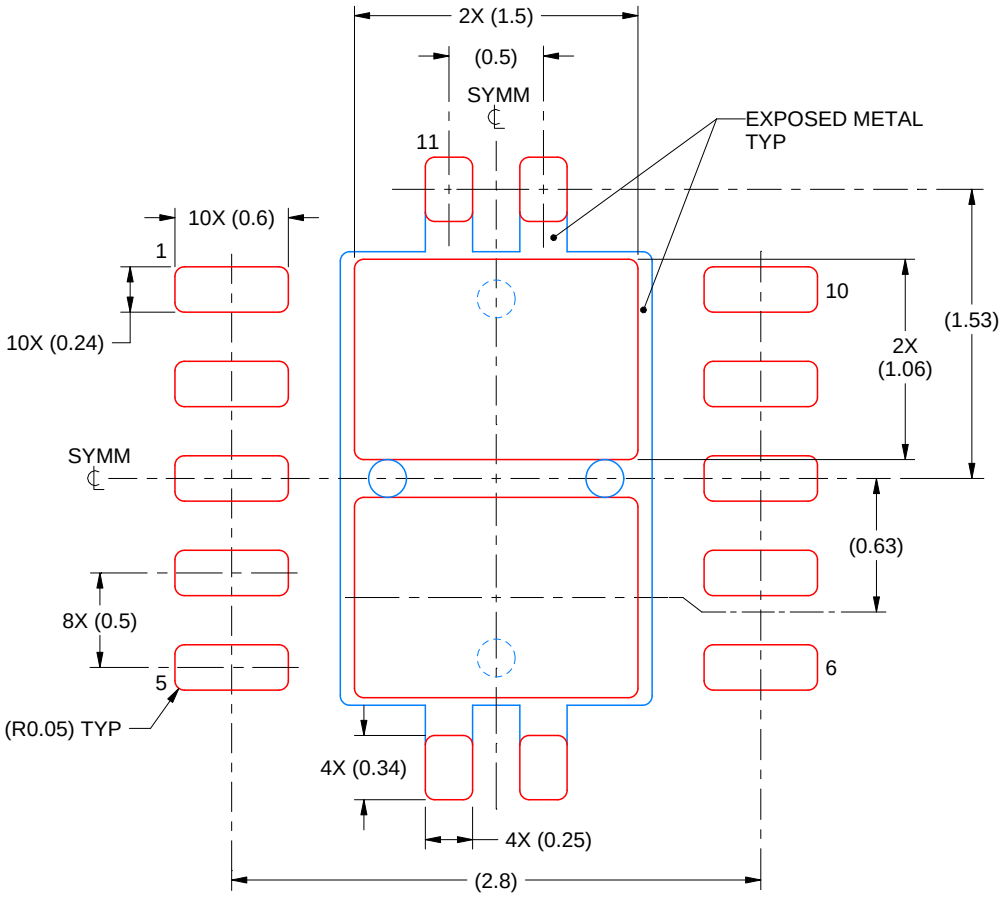
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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