TEXAS INSTRUMENTS
TPS544C26
JAJSP58 – SEPTEMBER 2022

TPS544C26 4V～16V 入力、35A で SVID および I²C インターフェイス付きの同期整流降圧コンバータ

ADVANCE INFORMATION

1 特長

- SVID レール用のシングルチップ電源
- Intel® VR13 SVID に準拠
- I²C インターフェイスと NVM による構成、遠隔測定 (V/I/T)、フォルト報告
- DDR5 メモリ RAPL の入力電力監視
- 4.0mΩ および 1.0mΩ の MOSFET を内蔵し、35A の連続電流動作に対応
- 入力電圧:4V～16V (絶対最大定格 18V)
- 外部 5V バイアスをサポートすることで効率が向上し、最小 2.7V の入力電圧で動作
- 出力電圧を 0.25V～3.04V の範囲でプログラム可能
- 出力電圧のスルーレートをプログラム可能:1.25mV/µs～10mV/µs
- 高精度の電圧リファレンスと差動リモート検出による高精度の出力
  - 0℃～85℃の接合部で ±0.5% の Vout 許容誤差
  - -40℃～125℃の接合部で ±1% の Vout 許容誤差
- 高速過渡応答の D-CAP+™ 制御トポロジ
- すべての出力コンデンサでセラミック・コンデンサの使用をサポート
- ドループも含めて内部ループ補償をプログラム可能
- サイクル単位のバレー電流制限を選択可能
- DCM または FCCM 動作で、動作周波数を 0.6MHz～1.2MHz の範囲で選択可能
- プリバイアスされた出力への安全なスタートアップ
- ソフトスタート時間を 1ms～16ms の範囲でプログラム可能
- ソフトストップ時間を 0.5ms～4ms の範囲でプログラム可能
- オープン・ドレインのパワー・グッド出力 (VRRDY) と致命的な障害のインジケータ (CAT_FAULT#)
- 過電流、過電圧、低電圧、過熱保護機能をプログラム可能
- 5mm × 6mm、ピン・ピッチ 0.5mm の 37 ピン WQFN-FCRLF パッケージ

2 アプリケーション

- サーバーおよびクラウド・コンピューティング POL
- ハードウェア・アクセラレータ
- ネットワーク・インターフェイス・カード

3 概要

TPS544C26 デバイスは高度に統合された降圧コンバータで、D-CAP+ 制御トポロジによって高速過渡応答を実現しています。すべてのプログラム可能なパラメータは、I²C インターフェイスを介して設定し、新しいデフォルト値として NVM に保存できるため、外付け部品点数を最小限に抑えることができます。これらの機能により、このデバイスはスペースに制約のあるアプリケーションに最適です。

TPS544C26 デバイスは、Intel のサーバーおよび SoC プラットフォームの低電流から中電流の SVID レール用に設計されています。SVID と I²C インターフェイス機能が搭載された TPS544C26 デバイスは、単相 CPU 電源レール用に構成できます。

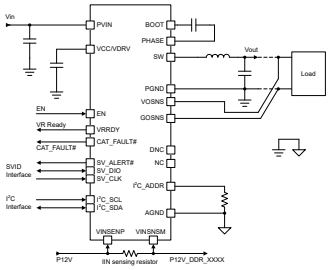
デバイスには、過電流、過電圧、低電圧、過熱保護機能が搭載されています。TPS544C26 デバイスには、出力電圧、出力電流、IC 温度などの遠隔測定機能がすべて搭載されています。さらに、TPS544C26 デバイスには、外付けのセンシング抵抗による入力電力の監視機能が搭載されています。

TPS544C26 は鉛フリー・デバイスで、適用除外なしで RoHS に準拠しています。

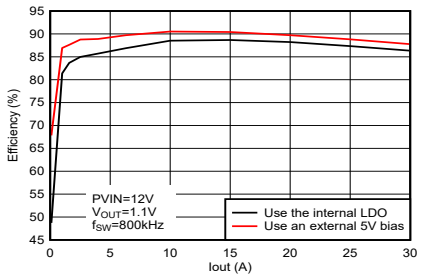
パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS544C26	RXX (WQFN-FCRLF、37)	5.00mm × 6.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



効率代表値

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2022	*	Advance Information release

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5 Pin Configuration and Functions

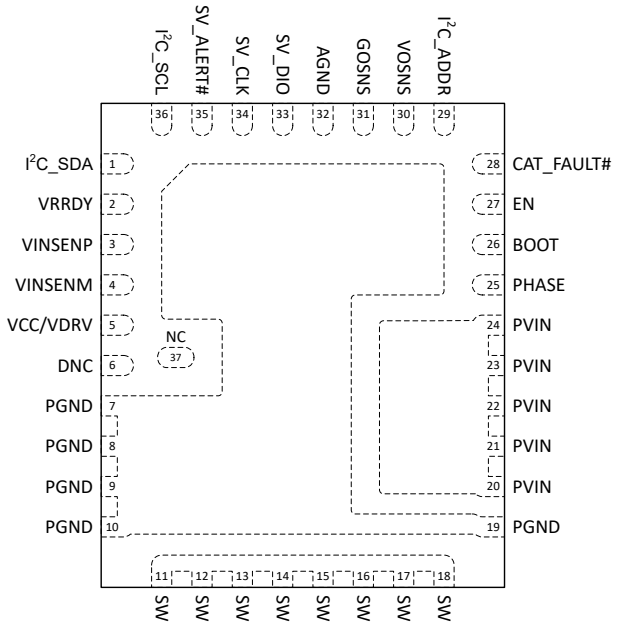


図 5-1. RXX 37-pin WQFN-FCRLF Package (Top View)

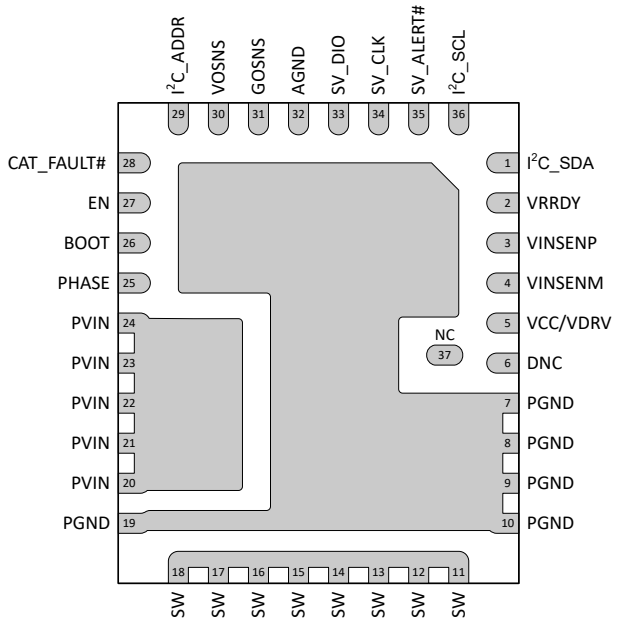


図 5-2. RXX 37-pin WQFN-FCRLF Package (Bottom View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	32	G	Ground pin, reference point for internal control circuitry.
BOOT	26	P	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to PHASE pin. A high temperature (X7R) 0.1 µF or greater value ceramic capacitor is recommended.
CAT_FAULT#	28	O	Catastrophic Fault indicator, open-drain. The CAT_FAULT# indicator asserts low when any catastrophic fault event (over-voltage, under-voltage and over-temperature) happens. During nominal operation, the CAT_FAULT# indicator holds high.
DNC	6	—	Do Not Connect (DNC) pin. This pin is the output of internal circuitry and must be floating. Pin 6 and pin 37 can be shorted together but NO any other PCB connection is allowed on pin 6.
EN	27	I	Enable pin, an active-high input pin that, when asserted high, causes the converter to begin its soft-start sequence for its output voltage rail. When de-asserted low, the converter must de-assert VRRDY and begin the shutdown sequence of the output voltage rail and continue to completion.
GOSNS	31	I	Negative input of the differential remote sense circuit, connect to the ground sense point on the load side.
I2C_ADDR	29	I	The I2C address of the device is set by tying an external resistor between this pin and AGND.
I2C_SCL	36	I	I2C serial clock pin, open drain.
I2C_SDA	1	I/O	I2C bi-directional serial data pin, open drain.
NC	37	—	Not connected. This pin is floating internally. Pin 37 and pin 6 can be shorted together.
PGND	7–10, 19	G	Power ground for the internal power stage.
PHASE	25	—	Return for high-side MOSFET driver. Shorted to SW internally. Connect the bootstrap capacitor from BOOT pin to this pin.
PVIN	20–24	P	Power input for both the power stage. PVIN is the input of the internal VCC LDO as well.

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表 5-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
SV_ALERT#	35	O	SVID active low ALERT# signal, open drain. This output is asserted to indicate the status of the converter has changed.
SV_CLK	34	I	SVID clock pin, open drain.
SV_DIO	33	I/O	SVID bi-directional data pin, open drain.
SW	11–18	O	Output switching terminal of the power converter. Connect these pins to the output inductor.
VCC/VDRV	5	P	Internal VCC LDO output and also the input for gate driver circuit. An external 5-V bias can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal control circuitry and the gate driver. A 2.2 µF (or 4.7 µF), at least 6.3 V rating ceramic capacitor is required to be placed from VCC/VDRV pin to PGND pins to decouple the noise generated by driver circuitry. Check layout guidelines for more details.
VINSENM	4	I	Negative input for the input power telemetry. Connect to the negative side of the input power sense resistor. Input voltage is also sensed at this pin. To minimize the impact from switching noise, a ceramic decoupling capacitor with at least 100 pF capacitance is required from this pin to PGND. Check layout guidelines for more details.
VINSENP	3	I	Positive input for the input power telemetry. Connect to the positive side of the input power sense resistor. To minimize the impact from switching noise, a ceramic decoupling capacitor with at least 100-pF capacitance is required from this pin to PGND. Check layout guidelines for more details.
VOSNS	30	I	Positive input of the differential remote sense circuit, connect to the Vout sense point on the load side.
VRRDY	2	O	Voltage regulator “Ready” output signal. The VRRDY indicator is asserted when the controller is ready to accept SVID commands after the EN is asserted. VRRDYalso de-asserts low when a shutdown fault occurs. This open-drain output requires an external pullup resistor.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	PVIN	–0.3	18	V
Pin voltage	PVIN – SW, DC	–0.3	18	V
Pin voltage	PVIN – SW, transient < 10 ns	–1.5	26	V
Pin voltage	SW – PGND, DC	–0.3	18	V
Pin voltage	SW, transient < 10 ns	–3.0	21.5	V
Pin voltage	BOOT – PGND	–0.3	23.5	V
Pin voltage	BOOT – SW	–0.3	5.5	V
Pin voltage	VCC/VDRV	–0.3	5.5	V
Pin voltage	PHASE	–0.3	18	V
Pin voltage	VINSENP, VINSENM	–0.3	20	V
Pin voltage	EN, VOSNS, SM_ADDR, VRRDY, CAT_FAULT#	–0.3	5.5	V
Pin voltage	SV_CLK, SV_DIO, SV_ALERT#, SM_CLK, SM_DIO	–0.3	5.5	V
Pin voltage	GOSNS – AGND	–0.3	0.3	V
Pin voltage	DNC, NC	–0.3	1.9	V
Sink current	VRRDY	0	10	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{OUT}	Output voltage range (programmed through SVID interface)		0.5		3.04	V
V_{IN}	Input voltage	PVIN when VCC/VDRV is powered by the internal LDO	4.0		16	V
		PVIN when VCC/VDRV is powered by a valid external bias	2.7		16	V
V_{BIAS}	Input voltage	VCC/VDRV external bias	4.75		5.3	V
I_{OUT}	Output current range				35	A
	Pin voltage	VINSENP, VINSENM	8		16	V
	Pin voltage	EN, VRRDY, CAT_FAULT#	–0.1		5.3	V
	Pin voltage	SV_CLK, SV_DIO, SV_ALERT#	–0.1		1.5	V
	Pin voltage	SM_CLK, SM_DIO	–0.1		5.3	V
I_{VRRDY}	VRRDY input current capability				10	mA
T_J	Operating junction temperature		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		DEVICE		UNIT
		RXX (QFN, JEDEC)	RXX (QFN, TI EVM)	
		37 PINS	37 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.0	15.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.4	Not applicable(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	Not applicable(2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	Not applicable(2)	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal test or simulation setup is not applicable to a TI EVM layout.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
	PVIN operating input range		4		18	V
$I_{Q(PVIN)}$	PVIN quiescent current	Non-switching, PVIN = 12 V, V_{EN} = 0 V, no bias on VCC/VDRV pin		7.5	9	mA
I_{VCC}	VCC/VDRV external bias current	5 V external bias on VCC/VDRV pin, regular switching. T_J = 25°C, PVIN = 12 V, V_{OUT} = 1.1 V, V_{EN} = 2 V, f_{SW} = 1 MHz		30		mA
$I_{Q(VCC)}$	VCC/VDRV quiescent current	5V external bias on VCC/VDRV pin, non-switching. PVIN = 12V, V_{EN} = 2 V, V_{FB} = V_{REF} + 50 mV		5		mA
UVLO						
$PVIN_{OV}$	PVIN overvoltage rising threshold	PVIN rising, VIN_OV_FAULT_LIMIT register (55h) = 0b		16.5		V
$PVIN_{OV}$	PVIN overvoltage rising threshold	PVIN rising, VIN_OV_FAULT_LIMIT register (55h) = 1b		18.5		V
$PVIN_{OV}$	PVIN overvoltage falling threshold	PVIN falling. PVIN_OVF status bit, once it is set, cannot be cleared unless PVIN falls below the PVIN overvoltage falling threshold		13.5		V
VIN_ON	PVIN turn-on voltage	PVIN rising, VIN_ON register (35h) = 00b		10		V
VIN_ON	PVIN turn-on voltage	PVIN rising, VIN_ON register (35h) = 01b		9		V
VIN_ON	PVIN turn-on voltage	PVIN rising, VIN_ON register (35h) = 10b		8		V
VIN_ON	PVIN turn-on voltage	PVIN rising, VIN_ON register (35h) = 11b. Ignore VIN_ON setting, and use VCC UVLO rising threshold to enable the device.		Disabled		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 000b		reserved		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 000b		4.2		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 001b		9.5		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 010b		8.5		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 011b		7.5		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 100b		6.5		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 101b		5.5		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 110b		4.2		V
VIN_OFF	PVIN turn-off voltage	PVIN falling, VIN_OFF register (36h) = 111b. Ignore VIN_OFF setting, and use VCC UVLO falling threshold to disable the device.		Disabled		V
$PVIN_{UVLO(R)}$	PVIN UVLO rising threshold	PVIN rising, 5V external bias on VCC/VDRV pin	2.0	2.55	3.0	V

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PVIN_{UVLO(F)}$	PVIN UVLO falling threshold	PVIN falling, 5V external bias on VCC/ VDRV pin	1.8	2.3	2.8	V
$PVIN_{UVLO(H)}$	PVIN UVLO hysteresis			0.25		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.14	1.19	1.24	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.94	0.98	1.02	V
$V_{EN(H)}$	EN voltage hysteresis			0.21		V
$t_{EN(DIG)}$	EN Deglitch Time		0.2			µs
	EN internal pulldown resistor	EN to AGND	87	103	119	kΩ
INTERNAL VCC LDO						
$t_{delay(uvlo_I2C)}$	Delay from VCC UVLO to I^2C ready to communicate	VCC/VDRV >= 3 V		TBD		ms
	Internal VCC LDO output voltage	PVIN= 4 V, $I_{VCC(load)}$ = 5 mA	3.925	3.97	4.0	V
	Internal VCC LDO output voltage	PVIN= 5 V to 16 V, $I_{VCC(load)}$ = 5 mA	4.28	4.44	4.55	V
	VCC UVLO rising threshold	VCC rising	3.69	3.75	3.81	V
	VCC UVLO falling threshold	VCC falling	3.49	3.55	3.61	V
	VCC UVLO hysteresis			0.2		V
	VCC LDO dropout voltage	PVIN – V_{VCC}, PVIN = 4 V, $I_{VCC(load)}$ = 45 mA	90	144	226	mV
	VCC LDO short-circuit current limit	PVIN = 5 V	150	200		mA
VOUT VOLTAGE						
	Output Voltage controlled through SVID interface	Output voltage range by SetVID & SetWP commands	0.5		3.04	V
	Output Voltage controlled through SVID interface	Output voltage resolution by SetVID & SetWP commands		5		mV
	Output Voltage controlled through SVID interface	SVID fast slew rate, register (AFh) DVS_CFG = 010b	2.5	2.78	3.06	mV/µs
	Output Voltage controlled through SVID interface	SVID fast slew rate, register (AFh) DVS_CFG = 100b	5	5.5	6.1	mV/µs
	Output Voltage controlled through SVID interface	SVID fast slew rate, register (AFh) DVS_CFG = 110b	10	11.1	12.2	mV/µs
	Output Voltage controlled through SVID interface	SVID OFFSET range	–127		127	Step
	Output Voltage controlled through SVID interface	SVID OFFSET resolution		1		Step
	Output Voltage controlled through I^2C interface	Output voltage range by register (A6h) VOUT_CMD	0.5		3.04	V
	Output Voltage controlled through I^2C interface	Output voltage resolution by register (A6h) VOUT_CMD		5		mV
	Output Voltage controlled through I^2C interface	Output voltage transition slew rate by register (A6h) VOUT_CMD, register (AFh) DVS_CFG = 010b	0.625			mV/µs
	Output Voltage controlled through I^2C interface	Output voltage transition slew rate by register (A6h) VOUT_CMD, register (AFh) DVS_CFG = 100b	1.25			mV/µs
	Output Voltage controlled through I^2C interface	Output voltage transition slew rate by register (A6h) VOUT_CMD, register (AFh) DVS_CFG = 110b	2.5			mV/µs
	Output Voltage controlled through I^2C interface	I^2C offset (register (A8h) VID_OFFSET) range, 5mV VID step	–63		63	mV
	Output Voltage controlled through I^2C interface	I^2C offset (register (A8h) VID_OFFSET) resolution, 5mV VID step		0.5		mV
	Output Voltage controlled through I^2C interface	I^2C offset (register (A8h) VID_OFFSET) range, 10mV VID step	–127		127	mV
	Output Voltage controlled through I^2C interface	I^2C offset (register (A8h) VID_OFFSET) resolution, 10mV VID step		1.0		mV

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT(ACC)}$	Output voltage accuracy	T_J = 0°C to 85°C, V_{OUT} = 0.75 V, V_{VOSNS}–V_{GOSNS}	0.744	0.75	0.756	V
$V_{OUT(ACC)}$	Output voltage accuracy	T_J = 0°C to 85°C, V_{OUT} = 1.1 V, V_{VOSNS}–V_{GOSNS}	1.0945	1.1	1.1055	V
$V_{OUT(ACC)}$	Output voltage accuracy	T_J = 0°C to 85°C, V_{OUT} = 1.8 V, V_{VOSNS}–V_{GOSNS}	1.791	1.8	1.809	V
$V_{OUT(ACC)}$	Output voltage accuracy	T_J = –40°C to 125°C, V_{OUT} = 0.75 V, V_{VOSNS}–V_{GOSNS}	0.7425	0.75	0.7575	V
$V_{OUT(ACC)}$	Output voltage accuracy	T_J = –40°C to 125°C, V_{OUT} = 1.1 V, V_{VOSNS}–V_{GOSNS}	1.089	1.1	1.111	V
$V_{OUT(ACC)}$	Output voltage accuracy	T_J = –40°C to 125°C, V_{OUT} = 1.8 V, V_{VOSNS}–V_{GOSNS}	1.782	1.8	1.818	V
I_{VOS}	VOSNS input current	V_{VOSNS} = 1.8 V		111	130	µA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, FREQUENCY_SWITCH register (33h) = 00b	540	600	660	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, FREQUENCY_SWITCH register (33h) = 01b	720	800	880	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, FREQUENCY_SWITCH register (33h) = 10b	900	1000	1100	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	T_J = –40°C to 125°C, PVIN = 12 V, V_{OUT} = 1.1 V, no load, FREQUENCY_SWITCH register (33h) = 11b	1080	1200	1320	kHz
STARTUP						
$t_{ON(DLY)}$	Power on sequence delay	V_{VCC} = 4.5 V, register (60h) TON_DELAY = 00b		0.5	0.55	ms
$t_{ON(DLY)}$	Power on sequence delay	V_{VCC} = 4.5 V, register (60h) TON_DELAY = 01b		1.0	1.1	ms
$t_{ON(DLY)}$	Power on sequence delay	V_{VCC} = 4.5 V, register (60h) TON_DELAY = 10b		1.5	1.65	ms
$t_{ON(DLY)}$	Power on sequence delay	V_{VCC} = 4.5 V, register (60h) TON_DELAY = 11b		2.0	2.2	ms
$t_{OFF(DLY)}$	Power off sequence delay	V_{VCC} = 4.5 V, register (64h) TOFF_DELAY = 00b		0	0.05	ms
$t_{OFF(DLY)}$	Power off sequence delay	V_{VCC} = 4.5 V, register (64h) TOFF_DELAY = 01b		1.0	1.1	ms
$t_{OFF(DLY)}$	Power off sequence delay	V_{VCC} = 4.5 V, register (64h) TOFF_DELAY = 10b		1.5	1.65	ms
$t_{OFF(DLY)}$	Power off sequence delay	V_{VCC} = 4.5 V, register (64h) TOFF_DELAY = 11b		2.0	2.2	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, register (61h) TON_RISE = 000b		1.0	1.1	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, register (61h) TON_RISE = 001b		2.0	2.2	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, register (61h) TON_RISE = 010b		4.0	4.4	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, register (61h) TON_RISE = 011b		8.0	8.8	ms
$t_{ON(Rise)}$	Soft-start time	V_{VCC} = 4.5 V, register (61h) TON_RISE = 1xxb		16.0	17.6	ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 00b, Vboot = 1.1V, PROTOCOL ID = 07h, 5mV VID step	2.00	2.2	2.44	V/ms

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 01b, Vboot = 1.1V, PROTOCOL ID = 07h, 5mV VID step	1.00	1.1	1.22	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 10b, Vboot = 1.1V, PROTOCOL ID = 07h, 5mV VID step	0.50	0.55	0.61	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 11b, Vboot = 1.1V, PROTOCOL ID = 07h, 5mV VID step	0.25	0.275	0.31	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 00b, Vboot = 1.8V, PROTOCOL ID = 04h, 10mV VID step	3.27	3.6	4.00	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 01b, Vboot = 1.8V, PROTOCOL ID = 04h, 10mV VID step	1.64	1.8	2.00	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 10b, Vboot = 1.8V, PROTOCOL ID = 04h, 10mV VID step	0.82	0.9	1.00	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by SVID	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 11b, Vboot = 1.8V, PROTOCOL ID = 04h, 10mV VID step	0.41	0.45	0.50	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 00b, PROTOCOL ID = 07h, 5mV VID step	2.00	2.2	2.44	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 01b, PROTOCOL ID = 07h, 5mV VID step	1.00	1.1	1.22	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 10b, PROTOCOL ID = 07h, 5mV VID step	0.50	0.55	0.61	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 11b, PROTOCOL ID = 07h, 5mV VID step	0.25	0.275	0.31	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 00b, PROTOCOL ID = 04h, 10mV VID step	3.27	3.6	4.00	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 01b, PROTOCOL ID = 04h, 10mV VID step	1.64	1.8	2.00	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 10b, PROTOCOL ID = 04h, 10mV VID step	0.82	0.9	1.00	V/ms
$t_{OFF(Fall)}$	Soft-stop slew rate, V_{OUT} controlled by I^2C	V_{VCC} = 4.5 V, register (65h) TOFF_FALL = 11b, PROTOCOL ID = 04h, 10mV VID step	0.41	0.45	0.50	V/ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, $V_{BOOT-SW}$ = 4.5 V		4		mΩ
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, $V_{BOOT-SW}$ = 5.0 V		3.91		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, V_{VCC} = 4.5 V		1		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, PVIN = 12 V, V_{VCC} = 5 V		0.98		mΩ
$t_{ON(min)}$	Minimum ON pulse width	V_{VCC} = 4.5 V			50	ns
$t_{OFF(min)}$	Minimum OFF pulse width	V_{VCC} = 4.5 V, I_O=1.5A, V_{OUT} = $V_{OUT(set)}$ – 20 mV, SW falling edge to rising edge			180	ns
BOOT CIRCUIT						
$I_{BOOT(LKG)}$	BOOT leakage current	V_{EN} = 2 V, $V_{BOOT-SW}$ = 5 V			150	µA
$V_{BOOT-SW(UV_F)}$	BOOT-SW UVLO falling threshold		2.60	2.76		V
OVERCURRENT PROTECTION						
$I_{LS(OC)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0000b	8.5	10	11.5	A
$I_{LS(OC)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0001b	10.2	12	13.8	A
$I_{LS(OC)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0010b	13.5	15	16.5	A
$I_{LS(OC)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0011b	17.1	19	20.9	A

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LS(OC)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0100b	18	20	22	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0101b	22.5	25	27.5	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0110b	23.4	26	28.6	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 0111b	27	30	33	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 1000b	29.7	33	36.3	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 1001b	31.5	35	38.5	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 1010b	35.1	39	42.9	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 1011b	36	40	44	A
$I_{LS(OCL)}$	Low-side valley overcurrent limit (TPS544C26)	Valley current limit on LS FET, IOUT_OC_FAULT_LIMIT (46h) = 11xxb	36	40	44	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 000b	8.5	10	11.5	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 001b	13.5	15	16.5	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 010b	18	20	22	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 011b	22.5	25	27.5	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 100b	27	30	33	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 101b	31.5	35	38.5	A
$I_{LS(OCW)}$	Low-side valley overcurrent warning (TPS544C26)	Valley current limit on LS FET, IOUT_OC_WARN_LIMIT (4Ah) = 11xb	36	40	44	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 00b, I_{CCMAX} ≥ 15A	–18	–20	–22	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 00b, I_{CCMAX} ≤ 10 A	–8.5	–10	–11.5	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 01b, I_{CCMAX} ≥ 15A	–13.5	–15	–16.5	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 01b, I_{CCMAX} ≤ 10 A	–6.37	–7.5	–8.63	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 10b, I_{CCMAX} ≥ 15A	–10.2	–12	–13.8	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 10b, I_{CCMAX} ≤ 10 A	–5.1	–6	–6.9	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 11b, I_{CCMAX} ≥ 15A	–8.5	–10	–11.5	A
$I_{LS(NOC)}$	Low-side negative overcurrent limit	Sinking current limit on LS FET, IOUT_NOC_LIMIT (B4h) = 11b, I_{CCMAX} ≤ 10 A	–4.25	–5	–5.75	A
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 00b, enter DCM		1200		mA

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 00b, exit DCM		1500		mA
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 01b, enter DCM		900		mA
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 01b, exit DCM		1200		mA
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 10b, enter DCM		0		mA
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 10b, exit DCM		300		mA
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 11b, enter DCM		–300		mA
I_{ZC}	Zero-cross detection current threshold	V_{IN} = 12 V, V_{VCC} = 4.5 V, SEL_ZC = 11b, exit DCM		0		mA
	Response delay before entering Hiccup	UV RESPONSE_DELAY = 00b		2		µs
	Response delay before entering Hiccup	UV RESPONSE_DELAY = 01b		16		µs
	Response delay before entering Hiccup	UV RESPONSE_DELAY = 10b		64		µs
	Response delay before entering Hiccup	UV RESPONSE_DELAY = 11b		256		µs
	Hiccup sleep time before a restart			56		ms
OUTPUT OVP AND UVP						
V_{OVP}	Vout tracking overvoltage protection (OVP) threshold, offset above Vout	(VOSNS – GOSNS) rising. (40h) VOUT_OV_FAULT_LIMIT = 00b	80	100	120	mV
V_{OVP}	Vout tracking overvoltage protection (OVP) threshold, offset above Vout	(VOSNS – GOSNS) rising. (40h) VOUT_OV_FAULT_LIMIT = 01b	120	150	180	mV
V_{OVP}	Vout tracking overvoltage protection (OVP) threshold, offset above Vout	(VOSNS – GOSNS) rising. (40h) VOUT_OV_FAULT_LIMIT = 10b	160	200	240	mV
V_{OVP}	Vout tracking overvoltage protection (OVP) threshold, offset above Vout	(VOSNS – GOSNS) rising. (40h) VOUT_OV_FAULT_LIMIT = 11b	240	300	360	mV
	Vout tracking OVP de-glitch time			2		µs
V_{FixOV}	Vout fixed OVP threshold, 5mV step	(VOSNS – GOSNS) rising. (CFh) FAULT_CTRL2, SEL_FIX_OVF = 0b, and (CCh) PROTOCOL_ID_SVID, PROTOCOL_ID<7:6> = 01b or 10b (5mV step)	1.425	1.5	1.575	V
V_{FixOV}	Vout fixed OVP threshold, 5mV step	(VOSNS – GOSNS) rising. (CFh) FAULT_CTRL2, SEL_FIX_OVF = 1b, and (CCh) PROTOCOL_ID_SVID, PROTOCOL_ID<7:6> = 01b or 10b (5mV step)	1.71	1.8	1.89	V
V_{FixOV}	Vout fixed OVP threshold, 10mV step	(VOSNS – GOSNS) rising. (CFh) FAULT_CTRL2, SEL_FIX_OVF = 0b, and (CCh) PROTOCOL_ID_SVID, PROTOCOL_ID<7:6> = 00b or 11b (10mV step)	2.33	2.4	2.47	V
V_{FixOV}	Vout fixed OVP threshold, 10mV step	(VOSNS – GOSNS) rising. (CFh) FAULT_CTRL2, SEL_FIX_OVF = 1b, and (CCh) PROTOCOL_ID_SVID, PROTOCOL_ID<7:6> = 00b or 11b (10mV step)	2.93	3.0	3.07	V
	Vout fixed OVP de-glitch time			2		µs
V_{UVP}	Vout tracking undervoltage protection (UVP) threshold, offset below Vout	(VOSNS – GOSNS) falling. (44h) VOUT_UV_FAULT_LIMIT = 00b	–120	–150	–180	mV
V_{UVP}	Vout tracking undervoltage protection (UVP) threshold, offset below Vout	(VOSNS – GOSNS) falling. (44h) VOUT_UV_FAULT_LIMIT = 01b	–160	–200	–240	mV
V_{UVP}	Vout tracking undervoltage protection (UVP) threshold, offset below Vout	(VOSNS – GOSNS) falling. (44h) VOUT_UV_FAULT_LIMIT = 10b	–160	–200	–240	mV
V_{UVP}	Vout tracking undervoltage protection (UVP) threshold, offset below Vout	(VOSNS – GOSNS) falling. (44h) VOUT_UV_FAULT_LIMIT = 11b	–240	–300	–360	mV

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Vout tracking UVP response delay time	(45h) VOUT_UV_FAULT_RESPONSE, RESPONSE_DELAY<1:0> = 00b. From UV detection to tri-state of the power FETs		2	4	µs
	Vout tracking UVP response delay time	(45h) VOUT_UV_FAULT_RESPONSE, RESPONSE_DELAY<1:0> = 01b. From UV detection to tri-state of the power FETs	14.4	16	17.6	µs
	Vout tracking UVP response delay time	(45h) VOUT_UV_FAULT_RESPONSE, RESPONSE_DELAY<1:0> = 10b. From UV detection to tri-state of the power FETs	57.6	64	70.4	µs
	Vout tracking UVP response delay time	(45h) VOUT_UV_FAULT_RESPONSE, RESPONSE_DELAY<1:0> = 11b. From UV detection to tri-state of the power FETs	230.4	256	281.6	µs
VR READY AND CATASTROPHIC FAULT						
$V_{OL(VRRDY)}$	VRRDY pin output low-level voltage	I_{VRRDY} = 10 mA, V_{IN} = 12 V, V_{VCC} = 4.5 V			300	mV
$I_{LKG(VRRDY)}$	VRRDY pin Leakage current when open drain output is high	R_{pullup} = 10 kΩ, V_{VRRDY} = 5 V			5	µA
	Min VCC for valid VRRDY pin output	PVIN = 0 V, V_{EN} = 0 V, R_{pullup} = 10 kΩ, V_{VRRDY} ≤ 0.3 V			1.2	V
	CAT_FAULT# pin output low-level voltage	R_{pullup} = 4.99 kΩ, V_{pullup} = 3.3 V		210	300	mV
	CAT_FAULT# pin Leakage current when open drain output is high	R_{pullup} = 4.99 kΩ, V_{pullup} = 3.3 V			5	µA
OUTPUT DISCHARGE						
	Output discharge on VOSNS pin	V_{IN} = 12 V, V_{VCC} = Internal LDO, V_{VOSNS} = 0.5 V, EN=0V		40		Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Junction temperature rising	153	166		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			30		°C
MEASUREMENT SYSTEM (I2C)						
$M_{IOUT(rng)}$	Output current measurement range	(C0h) ICC_MAX = 40 A	0		40	A
$M_{IOUT(acc)}$	Output current measurement accuracy	(C0h) ICC_MAX = 40 A, 0 ≤ I_{OUT} ≤ 4 A, –40°C ≤ T_J ≤ 125°C	–0.625		0.625	A
$M_{IOUT(acc)}$	Output current measurement accuracy	(C0h) ICC_MAX = 40 A, I_{OUT} = 12 A, –40°C ≤ T_J ≤ 125°C	–8%		8%	
$M_{IOUT(acc)}$	Output current measurement accuracy	(C0h) ICC_MAX = 40 A, 24 A ≤ I_{OUT} < 40 A, –40°C ≤ T_J ≤ 125°C	–6%		6%	
$M_{IOUT(lsb)}$	Output current measurement bit resolution	(C0h) ICC_MAX = 40 A		0.1563		A
$M_{VOUT(rng)}$	Output voltage measurement range		0		3.04	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy	0.75 V ≤ VOUT ≤ 1.5 V, PROTOCOL ID = 07h, 5mV VID step	–19		19	mV
$M_{VOUT(acc)}$	Output voltage measurement accuracy	1.5 V < VOUT ≤ 3.0 V, PROTOCOL ID = 04h, 10mV VID step	–37.5		37.5	mV
$M_{VOUT(lsb)}$	Output voltage measurement bit resolution	PROTOCOL ID = 07h, 5mV VID step		6.25		mV
$M_{VOUT(lsb)}$	Output voltage measurement bit resolution	PROTOCOL ID = 04h, 10mV VID step		12.5		mV
$M_{PIN(rng)}$	Input power measurement range	(6Bh) PIN_OP_WARN_LIMIT = 000b (360 W)	0		360	W
$M_{PIN(acc)}$	Input power measurement accuracy datapoint	Room Temp, 12V, 15A, 180W		180		W
$M_{PIN(acc)}$	Input power measurement accuracy datapoint	Room Temp, 12V, 25A, 300W		300		W
$M_{PIN(acc)}$	Input power measurement accuracy		%		%	
$M_{PIN(lsb)}$	Input power measurement bit resolution					W
$M_{VIN(rng)}$	Input voltage measurement range	VINSNSM – AGND	8		16	V
$M_{VIN(acc)}$	Input voltage measurement accuracy datapoint	VINSNSM – AGND. T_J = 0°C to 85°C		8		V

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$M_{VIN(acc)}$	Input voltage measurement accuracy datapoint	VINSNSM – AGND. T_J = 0°C to 85°C		12		V
$M_{VIN(acc)}$	Input voltage measurement accuracy datapoint	VINSNSM – AGND. T_J = 0°C to 85°C		16		V
$M_{VIN(acc)}$	Input voltage measurement accuracy	8 V≤ VINSNSM ≤ 16 V	%		%	
$M_{VIN(lsb)}$	Input voltage measurement bit resolution	VINSNSM – AGND				V
$M_{IIN(rng)}$	Input current measurement range	(B3h) PIN_SENSE_RES = 100b (1.0 mΩ), 101b (0.5 mΩ)	0		32	A
$M_{IIN(acc)}$	Input current measurement accuracy datapoint	Room temp, PIN_SENSE_RES set accordingly		15		A
$M_{IIN(acc)}$	Input current measurement accuracy datapoint	Room temp, PIN_SENSE_RES set accordingly		25		A
$M_{IIN(acc)}$	Input current measurement accuracy		%		%	
$M_{IIN(lsb)}$	Input current measurement bit resolution					A
$M_{TSNS(rng)}$	Internal temperature sense range		–40		125	°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy datapoint			-40		°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy datapoint			0		°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy datapoint			25		°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy datapoint			85		°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy datapoint			125		°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy	–40°C ≤ T_J ≤ 125°C	%		%	
$M_{TSNS(lsb)}$	Internal temperature sense bit resolution					°C
SVID Timing and Physical Characteristics						
C_{PAD_SVID}	SVID pin pad capacitance(1)		0		4	pF
C_{PIN_SVID}	SVID pin capacitance(1)		0		5	pF
V_{MAX_SVID}	VDS max open drain buffer to accommodate ringing on bus		–1		3.3	V
V_{IL_SVID}	SV_CLK, SV_DIO input low voltage		0.45	0.5	0.55	V
V_{IH_SVID}	SV_CLK, SV_DIO input high voltage		0.54	0.59	0.64	V
V_{HYS_SVID}	SV_CLK, SV_DIO input voltage hysteresis		0.05			V
R_{RSVIDL}	Open Drain Pulldown resistance	SV_DIO, SV_ALERT# pins pulldown resistance	4	8	13	Ω
I_{LKG_SVID}	Input leakage current	Pullup source = 5.5 V, off state			20	µA
D_{CLK_SVID}	SVID clock duty ratios (Period and duty cycle are measured with respect to 0.5 x VccIO)		0.4		0.6	
$t_{CO_VR_SVID}$	VR Clock to Data delay without board parasitic				12	ns
$t_{SU_VR_SVID}$	Setup time of data at VR side				7	ns
$t_{H_VR_SVID}$	Hold time of data at VR side				14	ns
$t_{CO_CPU_SVID}$	CPU Clock to Data delay	Measured at bump	–3.6		0.65	ns
$t_{SU_CPU_SVID}$	Setup time of data at CPU side			1		ns
$t_{H_CPU_SVID}$	Hold time of data at CPU side			3		ns
SR_{F_DATA}	Falling slew rate of SV_DIO(1)	SV_DIO from 0.735V to 0.315V, Rpu=64.9Ω	1.2		4	V/ns
SR_{R_DATA}	Rising slew rate of SV_DIO(1)	SV_DIO from 0.315V to 0.735V, Rpu=64.9Ω	1.1		3.6	V/ns
SR_{F_ALERT}	Falling slew rate of SV_ALERT#(1)	SV_ALERT# from 0.735V to 0.315V, Rpu=75Ω	1.25		4.2	V/ns

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; -40°C, 0°C, 25°C, 85°C, 125°C. PVIN = 4 V to 16 V, V_{VCC} = 4.5 V to 5.0 V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12 V and V_{VCC} = 4.5 V.

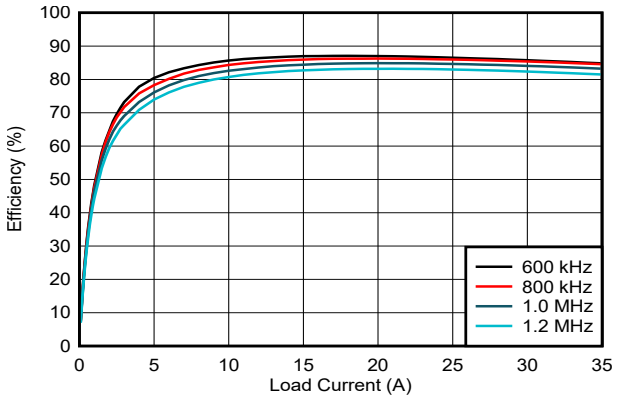
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR_{R_ALERT}	Rising slew rate of SV_ALERT#(1)	SV_ALERT# from 0.315V to 0.735V, Rpu=75Ω	1.15		3.3	V/ns
$FREQ_{SVID}$	Max SVID Clock frequency Support		43			MHz
I²C Timing and Physical Characteristics						
$FREQ_{I2C}$	I²C operating frequency range		50		1000	kHz
V_{IH_I2C}	SM_CLK, SM_DIO High-level input voltage		0.535	0.585	0.635	V
V_{IL_I2C}	SM_CLK, SM_DIO Low-level input voltage		0.465	0.515	0.565	V
V_{HYS_I2C}	SM_CLK, SM_DIO Input voltage hysteresis		0.05			V
N_{WRNVM}	Number of NVM writeable cycles (1)	–40°C ≤ T_J ≤ 125°C	1000			Cycles
C_{BUS_I2C}	I²C bus capacitance on each bus line(1)		0		400	pF
C_{PIN_I2C}	I²C pin capacitance(1)		0		10	pF
t_{H_STA}	Hold time for a (repeated) START condition		0.26			µs
t_{LOW}	Low period of SM_CLK		0.5			µs
t_{HIGH}	High period of SM_CLK		0.26			µs
t_{SU_STA}	Setup time for a repeated START condition		0.26			µs
t_{H_I2C}	I²C DATA hold time		0			µs
t_{SU_I2C}	I2C DATA setup time		50			ns
t_{R_I2C}	SM_CLK and SM_DIO rise time(1)	100 kHz class			1000	ns
		400 kHz class			300	ns
		1000 kHz class			120	ns
t_{F_I2C}	SM_CLK and SM_DIO fall time(1)	100 kHz class			1000	ns
		400 kHz class			300	ns
		1000 kHz class			120	ns
t_{SU_STO}	Setup time for a STOP condition		0.26			µs
t_{BUF}	Bus free time between a STOP and START condition		0.5			µs

(1) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purpose of TI's product warranty.

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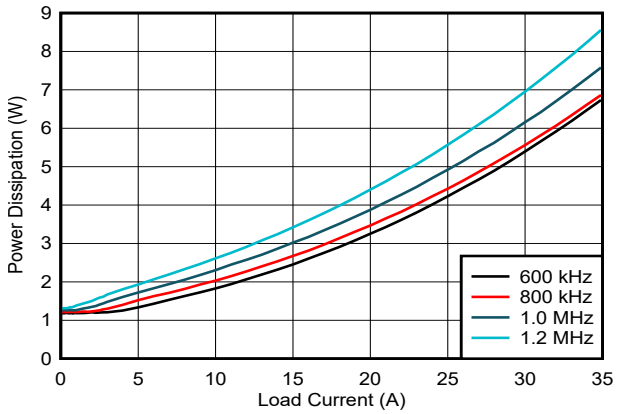
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6.6 Typical Characteristics



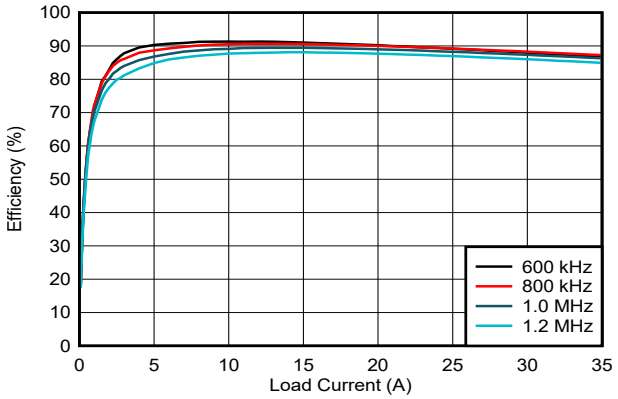
PVIN = 12 V VCC = Internal LDO V_{OUT} = 1.1 V
MODE = FCCM

図 6-1. Efficiency vs Output Current



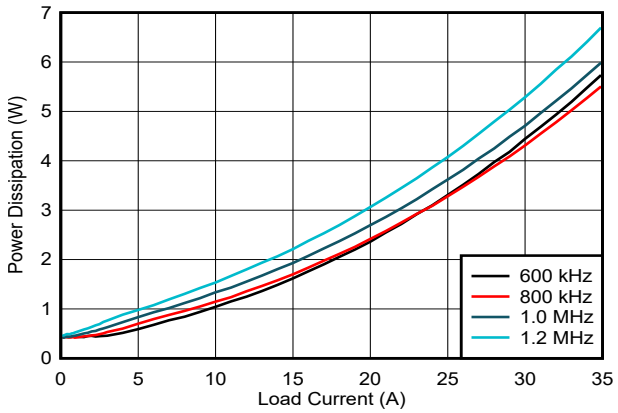
PVIN = 12 V VCC = Internal LDO V_{OUT} = 1.1 V
MODE = FCCM

図 6-2. Power Dissipation vs Output Current



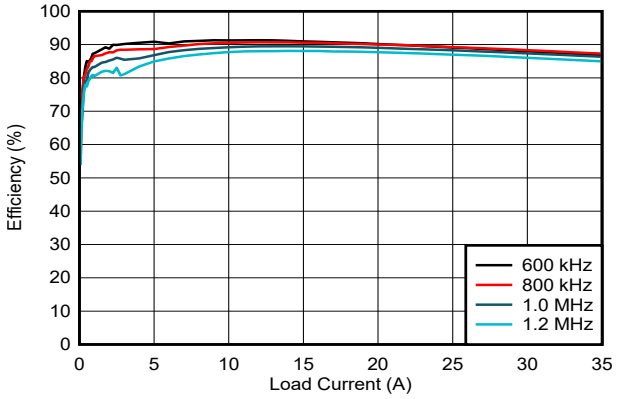
PVIN = 12 V VCC = External 5-V Bias V_{OUT} = 1.1 V
MODE = FCCM

図 6-3. Efficiency vs Output Current



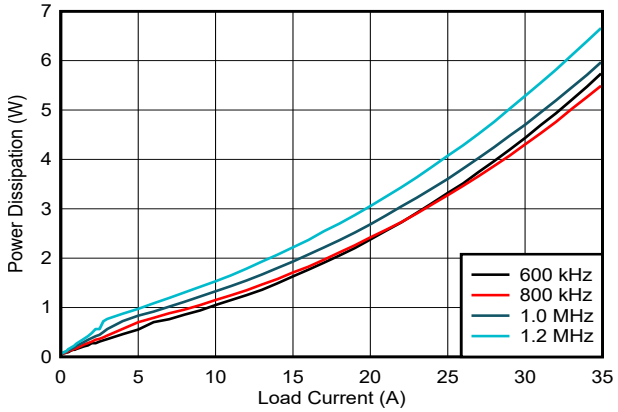
PVIN = 12 V VCC = External 5-V Bias V_{OUT} = 1.1 V
MODE = FCCM

図 6-4. Power Dissipation vs Output Current



PVIN = 12 V VCC = External 5-V Bias V_{OUT} = 1.1 V
MODE = DCM

図 6-5. Efficiency vs Output Current



PVIN = 12 V VCC = External 5-V Bias V_{OUT} = 1.1 V
MODE = DCM

図 6-6. Power Dissipation vs Output Current

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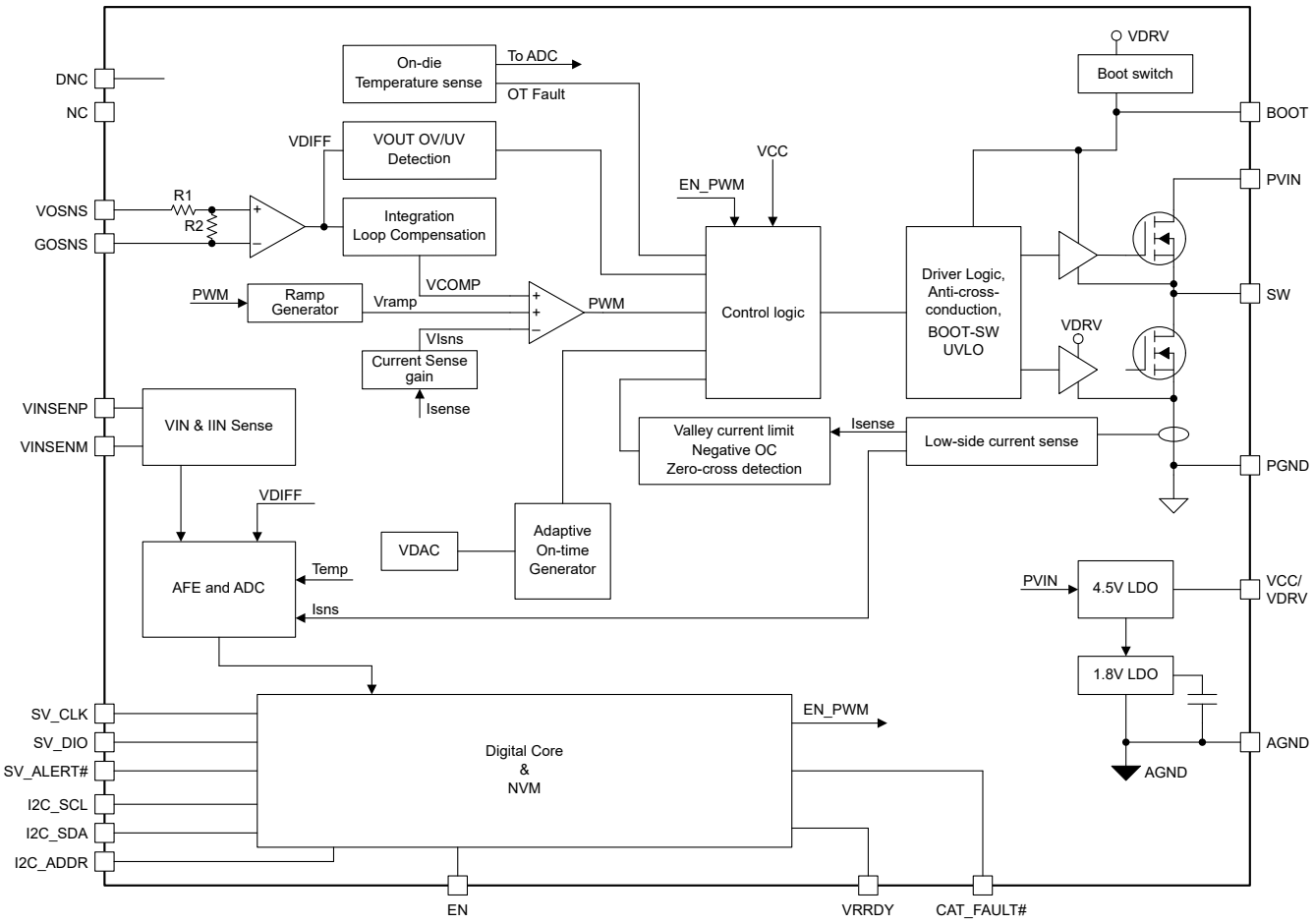
7 Detailed Description

7.1 Overview

The TPS544C26 device is highly integrated buck converter with D-CAP+ control topology for fast transient response and reduced output capacitance. All programmable parameters can be configured by the I2C interface and stored in NVM as the new default values to minimize the external component count. These features make the device well-suited for space-constrained applications. The TPS544C26 device is designed for low-to-mid current SVID rails in Intel's server and SoC CPUs. The TPS544C26 device with SVID and I2C interface feature can be configured for single phase CPU power rail.

Over-current, Over-voltage, and Under-voltage, Overtemperature protections are provided internally in the device. The TPS544C26 device offers a full set of telemetry features, including output voltage, output current, IC temperature, and input power monitoring through an external sensing resistor. TPS544C26 is a lead-free device and is RoHS compliant without exemption.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal VCC LDO and Using an External Bias on VCC/VDRV Pin

TPS544C26 device has an internal 4.5-V LDO featuring input from PVIN and output to VCC/VDRV pin. When the PVIN voltage rises, the internal LDO is enabled automatically and starts regulating LDO output voltage on the VCC/VDRV pin. The VCC voltage provides the bias voltage for the internal analog circuitry in controller side and the VDRV voltage provides the supply voltage for the power stage side.

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A 2.2-µF or 4.7-µF, at least 6.3-V rating ceramic capacitor must be closely placed from VCC/VDRV pin to PGND pin to decouple the noise generated by driver circuitry. Referring this decoupling capacitor to AGND introduces extra noise to the analog circuitry in controller, which likely causes more noise on digital interface pins.

An external bias ranging 4.75-V to 5.30-V can be connect to VCC/VDRV pin and power the IC. This enhances the efficiency of the solution because the VCC and VDRV power supply current now runs off this external bias instead of the internal linear regulator.

A VCC UVLO circuit monitors the VCC/VDRV pin voltage and disables the switching when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC/VDRV voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VDRV and VCC pin are shown below:

- Connect the external bias to VCC/VDRV pin.
- When the external bias is applied on the VCC/VDRV pin earlier than PVIN rail, the internal LDO is be always forced off and the internal analog circuits have a stable power supply rail at their power enable.
- (Not recommended) When the external bias is applied on the VCC/VDRV pin late (for example, after PVIN rail ramp-up), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC/VDRV pin. Understand that an external discharge path on the VCC/VDRV pin, which can pull a current higher than the current limit of the internal LDO, can potentially turn off VCC LDO thereby shutting off the converter output.
- A good power-up sequence is: the external 5-V bias is applied first, then the 12 V bus is applied on PVIN, and then EN signal goes high.

7.3.2 Input Undervoltage Lockout (UVLO)

The TPS544C26 device provides four independent UVLO functions for the broadest range of flexibility in start-up control. While only the fixed VCC UVLO is required to enable I^2C connectivity as well as PIN/IOUT/VOUT/TEMPERATURE monitoring, all four UVLO functions must be met before switching can be enabled.

7.3.2.1 Fixed VCC UVLO

The TPS544C26 device has an internally fixed UVLO of 3.2 V (typical) on VCC to enable the digital core and initiate power-on reset, including pin strap detection. The off-threshold on VCC is 3.1 V (typical). Once VCC level rises above 3.2 V (typical) and stays above 3.1 V (typical), the I^2C communication is enabled.

7.3.2.2 Fixed VDRV UVLO

The TPS544C26 device has an internally fixed UVLO of 3.6 V (typical) on VDRV to enable drivers for power FETs and output voltage conversion. The off-threshold on VDRV is 3.4 V (typical).

7.3.2.3 Programmable PVIN UVLO

Two I2C commands (*(35h) VIN_ON* and *(36h) VIN_OFF*) allow the user to set PVIN voltage turn-on and turn-off thresholds independently.

The highest register data value on each command (*VIN_ON = 11b* or *VIN_OFF = 111b*) utilizes multiple UVLO circuitries (VCC, VDRV and PVIN UVLO) to enable or disable the power conversion. When *VIN_ON = 11b* is selected, both PVIN > 2.55 V and VCC > 3.8 V conditions have to be satisfied to enable the power conversion. When *VIN_OFF = 111b* is selected, either PVIN ≤ 2.3 V or VDRV ≤ 3.4 V disables the power conversion. This particular configuration together with an external 5 V bias on VCC/VDRV pin allows power conversion under low PVIN condition down to 2.7 V, as long as the external bias maintains at 5 V level to satify both the VCC rising threshold (3.8 V typical) and the VDRV falling threshold (3.4 V typical).

表 7-1. PVIN_ON Thresholds

PVIN_ON[1:0]	PVIN_ON Threshold (V)
00	10
01	9
10	8
11	ON threshold by both PVIN and VCC conditions. See (35h) VIN_ON

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表 7-2. PVIN_OFF Thresholds

PVIN_OFF[2:0]	PVIN_OFF Threshold (V)
000	4.2
001	9.5
010	8.5
011	7.5
100	6.5
101	5.5
110	4.2
111	ON threshold by both PVIN and VDRV conditions. See (36h) VIN_OFF

注

If *VIN_OFF* is programmed higher than *VIN_ON*, the TPS544C26 device rapidly switches between enabled and disabled while PVIN remains below *VIN_OFF*. Please set (35h) VIN_ON threshold always greater than (36h) VIN_OFF threshold.

7.3.2.4 Enable

The TPS544C26 device offers precise enable, disable threshold on EN pin. The power stage switching is held off until EN pin voltage rises above the logic high threshold (typically 1.2 V). The power stage switching is turned off after EN pin voltage drops below the logic low threshold (typically 1 V).

EN pin has an internal filter to avoid unexpected ON or OFF due to short glitches. The deglitch time is set to 0.2 µs.

The recommended operating condition for EN pin is up to 5.3 V and the absolute maximum rating is 5.5 V. DO NOT connect the EN pin to PVIN pin directly.

The TPS544C26 device remains disabled state when EN pin floats. EN pin is internally pulled down to AGND through a 121-kΩ resistor.

7.3.3 Differential Remote Sense and Internal Feedback Divider

The TPS544C26 includes a fully integrated, internal, precision feedback divider and remote sense. Using both the selectable feedback divider and precision adjustable reference, output voltages up to 3.04 V can be obtained. The feedback divider can be programmed to divider ratios of 1:2 or 1:4 using the *PROTOCOL_ID* in register (C2h) PROTOCOL_ID_SVID.

The recommended operating VOUT range is dependent upon the feedback divider ratio configured by *PROTOCOL_ID* as follows:

表 7-3. VOUT Step and Recommended VOUT Range

VOUT_CTRL	VOUT Control Method	VOUT Step	Internal FB Divider Ratio	Recommended VOUT Range (V)
00b	SVID only	5 mV (PROTOCOL_ID = 01b or 10b)	1:2	0.25 to 1.52
01b	SVID + I^2C			
10b or 11b	I^2C only			
00b	SVID only	10 mV (PROTOCOL_ID = 00b or 11b)	1:4	0.5 to 3.04
01b	SVID + I^2C			
10b or 11b	I^2C only			

Setting VOUT lower than the recommended range can negatively affect VOUT regulation accuracy. Setting VOUT above the recommended range is not achievable due to internal hardware limitation.

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注

Do not to use extra external divider to set VOUT higher than the recommended range. Using external divider leads to higher switching frequency than the desired value set in register (33h) FREQUENCY_SWITCH. The switching frequency shift varies depending on the delta between internal VOUT setting and the actual VOUT setting determined by the external divider. The more delta on internal vs external VOUT, the higher switching frequency shift.

The TPS544C26 device offers true differential remote sense function which is implemented between VOSNS pin and GOSNS pin. The output of the differential remote sense amplifier is internally fed into the control loop and doesn't come out to a package pin.

Differential remote sense function compensates a potential voltage drop on the PCB traces thus helps maintain VOUT accuracy under steady state operation and load transient event. Connecting the VOSNS pin and GOSNS pin to the remote location allows sensing the output voltage at a remote location. The connections from VOSNS pin and GOSNS pin to the remote location must be a pair of PCB traces with at least 12 mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher. The ground connection of the remote sensing signal must be connected to GOSNS pin. The VOUT connection of the remote sensing signal must be connected to VOSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW node, or high frequency clock lines. It is recommended to shield the pair of remote sensing lines with ground planes above and below.

The recommended GOSNS operating range (refer to AGND pin) is −100 mV to +100 mV. In case of local sense (no remote sensing), short GOSNS pin to AGND.

7.3.4 Set the Output Voltage and VID Table

The TPS544C26 device offers VOUT adjustment through either SVID interface (for example, VID related SVID commands) or I2C interface (for example, (A6h) VOUT_CMD register). To allow flexibility and also avoid conflict, the device utilizes VOUT_CTRL[1:0] bits in register (A0h) SYS_CFG_USER1 to select which interface or method controls the VOUT level during the soft-start and nominal operation target. 表 7-4 describes more details.

The VOUT_CTRL value is latched after the power conversion is enabled (EN=high). While the device is enabled, a write to VOUT_CTRL bits are acknowledged but the VOUT control method does not change until an EN toggle happens.

表 7-4. VOUT Control Method

VOUT_CTRL	VOUT Control Method	Start-up		Nominal Operation		Maximum VOUT Limit	Further Restrictions
		VOUT	VOUT Offset	VOUT	VOUT Offset		
00b	SVID only	Set by Vboot in I²C register (C2h) PROTOCOL_ID_SVID	Set by SVID register (33h) OFFSET. This offset is always zero before EN=high	Set by SVID commands (such as SetVID, SetWP)	Set by SVID register (33h) OFFSET	SVID register 09h-0Ah VIDoMAX	I²C register (A6h) VOUT_CMD is always ignored (ACK response for a write but does nothing). I²C register (A8h) I2C_OFFSET is de-activated (NACK response for a write)
01b	SVID + I²C	Set by Vboot in I²C register (C2h) PROTOCOL_ID_SVID	Set by I²C register (A8h) I²C_OFFSET	Set by SVID commands (such as SetVID, SetWP)	Set by I²C register (A8h) I²C_OFFSET. A new I²C_OFFSET value does not take effect immediately. Instead, the new value takes effect on the next start-up	SVID register 09h-0Ah VIDoMAX	I²C register (A6h) VOUT_CMD is always ignored (ACK response for a write but does nothing). SVID register (33h) OFFSET is ignored (ACK response for a write but does nothing)

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表 7-4. VOUT Control Method (continued)

VOUT_CTRL	VOUT Control Method	Start-up		Nominal Operation		Maximum VOUT Limit	Further Restrictions
		VOUT	VOUT Offset	VOUT	VOUT Offset		
10b or 11b	I²C only	Set by I²C register (A6h) VOUT_CMD	Set by I²C register (A8h) I²C_OFFSET	Set by I²C register (A6h) VOUT_CMD. A new VOUT_CMD value takes effect immediately.	Set by I²C register (A8h) I²C_OFFSET. A new I²C_OFFSET value takes effect immediately.	17E in hex	SVID SetVID/SetWP command and SVID register (33h) OFFSET are always ignored (ACK response for a write but does nothing)

With VOUT_CTRL[1:0] = 00b or 01b (VOUT controlled by SVID), the initial output voltage can be set by the *Vboot* during initial power up, with the range from 0.75 V to 1.8 V (see 表 7-5). Vboot value can be adjusted through a write into the Vboot filed in I²C register (C2h) PROTOCOL_ID_SVID. Upon the acknowledge of the I²C write, the new Vboot value is automatically copied into SVID (26h) Vboot register. With a successful I²C (15h) STORE_USER_ALL command, this new value is saved into NVM. During next power-on sequence, TPS544C26 loads the saved Vboot value from NVM into both I²C Vboot field and SVID (26h) Vboot register. Once the soft-start ramp finishes, the output voltage can be changed by sending SetVID or SetWP command to the device, or sending a new SVID OFFSET value to the device.

With VOUT_CTRL[1:0] = 10b or 11b (VOUT controlled by I²C), the initial output voltage can be set by the register *(A6h) VOUT_CMD* during initial power up. The available VOUT_CMD range is 0.25 V to 1.52 V for PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV), and 0.50 V to 3.04 V for PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV). Once the soft-start ramp finishes, the output voltage can be changed by sending new value to I²C register (A6h) VOUT_CMD, or sending a new (A8h) I²C_OFFSET value to the device. Upon the acknowledge of a I²C write into I²C register (A6h) VOUT_CMD or (A8h) I²C_OFFSET, the new value takes effect immediately. With a successful I²C (15h) STORE_USER_ALL command, this new value is saved into NVM. During next power-on sequence, TPS544C26 loads the saved value from NVM and use that value for the soft-start.

表 7-5. Vboot Settings

Vboot in (C2h) PROTOCOL_ID_SVID	VID code[1] (Hex)	Vboot (V)	PROTOCOL_ID in (C2h) PROTOCOL_ID_SVID
0000b	00h	0	Must set PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)
0001b	65h	0.75	
0010b	6Fh	0.80	
0011b	79h	0.85	
0100b	83h	0.90	
0101b	8Dh	0.95	
0110b	97h	1.00	
0111b	A1h	1.05	
1000b	ABh	1.10	
1001b	AFh	1.20	
1010b	C9h	1.25	
1011b	DDh	1.35	
1100b	FBh	1.50	
1101b	6Fh	1.60	Must set PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)
1110b	79h	1.70	
1111b	83h	1.80	

1. VID code is not directly visiable to customer but shows up in I2C register (A7h) VID_SETTING and SVID register (31h) VID_SETTING.

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TPS544C26 always follows below VID table when setting output voltage, no matter through SVID interface or I²C interface. When setting output voltage, aligning the VOUT value with PROTOCOL_ID (5 mV or 10 mV) accordantly is important. An incorrect selection on the VOUT and PROTOCOL_ID value can result in a NACK response for the write into (C2h) PROTOCOL_ID_SVID register. For example, a configuration of Vboot = 1.8 V and PROTOCOL_ID = 01b (VOUT step 5 mV) results in a NACK response. Another example with VOUT_CTRL[1:0] = 10b or 11b (VOUT controlled by I²C), setting VOUT_CMD to 2.5 V requires PROTOCOL_ID = 00b or 11b (VOUT step 10 mV) and thus requires Vboot to be one of the 3 options of 1.6 V, 1.7 V and 1.8 V. Even the Vboot value does not affect VOUT level for VOUT_CTRL[1:0] = 10b or 11b selection, a suitable Vboot value is needed to pass the error check on Vboot and PROTOCOL_ID fields.

表 7-6. VID Table for Output Voltage

VID code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step	VID Code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step	VID Code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step	VID Code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step
00	0.000	0.00	40	0.565	1.13	80	0.885	1.77	C0	1.205	2.41
01	0.250	0.50	41	0.570	1.14	81	0.890	1.78	C1	1.210	2.42
02	0.255	0.51	42	0.575	1.15	82	0.895	1.79	C2	1.215	2.43
03	0.260	0.52	43	0.580	1.16	83	0.900	1.80	C3	1.220	2.44
04	0.265	0.53	44	0.585	1.17	84	0.905	1.81	C4	1.225	2.45
05	0.270	0.54	45	0.590	1.18	85	0.910	1.82	C5	1.230	2.46
06	0.275	0.55	46	0.595	1.19	86	0.915	1.83	C6	1.235	2.47
07	0.280	0.56	47	0.600	1.20	87	0.920	1.84	C7	1.240	2.48
08	0.285	0.57	48	0.605	1.21	88	0.925	1.85	C8	1.245	2.49
09	0.290	0.58	49	0.610	1.22	89	0.930	1.86	C9	1.250	2.50
0A	0.295	0.59	4A	0.615	1.23	8A	0.935	1.87	CA	1.255	2.51
0B	0.300	0.60	4B	0.620	1.24	8B	0.940	1.88	CB	1.260	2.52
0C	0.305	0.61	4C	0.625	1.25	8C	0.945	1.89	CC	1.265	2.53
0D	0.310	0.62	4D	0.630	1.26	8D	0.950	1.90	CD	1.270	2.54
0E	0.315	0.63	4E	0.635	1.27	8E	0.955	1.91	CE	1.275	2.55
0F	0.320	0.64	4F	0.640	1.28	8F	0.960	1.92	CF	1.280	2.56
10	0.325	0.65	50	0.645	1.29	90	0.965	1.93	D0	1.285	2.57
11	0.330	0.66	51	0.650	1.30	91	0.970	1.94	D1	1.290	2.58
12	0.335	0.67	52	0.655	1.31	92	0.975	1.95	D2	1.295	2.59
13	0.340	0.68	53	0.660	1.32	93	0.980	1.96	D3	1.300	2.60
14	0.345	0.69	54	0.665	1.33	94	0.985	1.97	D4	1.305	2.61
15	0.350	0.70	55	0.670	1.34	95	0.990	1.98	D5	1.310	2.62
16	0.355	0.71	56	0.675	1.35	96	0.995	1.99	D6	1.315	2.63
17	0.360	0.72	57	0.680	1.36	97	1.000	2.00	D7	1.320	2.64
18	0.365	0.73	58	0.685	1.37	98	1.005	2.01	D8	1.325	2.65
19	0.370	0.74	59	0.690	1.38	99	1.010	2.02	D9	1.330	2.66
1A	0.375	0.75	5A	0.695	1.39	9A	1.015	2.03	DA	1.335	2.67
1B	0.380	0.76	5B	0.700	1.40	9B	1.020	2.04	DB	1.340	2.68
1C	0.385	0.77	5C	0.705	1.41	9C	1.025	2.05	DC	1.345	2.69
1D	0.390	0.78	5D	0.710	1.42	9D	1.030	2.06	DD	1.350	2.70
1E	0.395	0.79	5E	0.715	1.43	9E	1.035	2.07	DE	1.355	2.71
1F	0.400	0.80	5F	0.720	1.44	9F	1.040	2.08	DF	1.360	2.72
20	0.405	0.81	60	0.725	1.45	A0	1.045	2.09	E0	1.365	2.73
21	0.410	0.82	61	0.730	1.46	A1	1.050	2.10	E1	1.370	2.74
22	0.415	0.83	62	0.735	1.47	A2	1.055	2.11	E2	1.375	2.75

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表 7-6. VID Table for Output Voltage (continued)

VID code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step	VID Code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step	VID Code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step	VID Code (Hex)	VOUT (V) 5-mV Step	VOUT (V) 10-mV Step
23	0.420	0.84	63	0.740	1.48	A3	1.060	2.12	E3	1.380	2.76
24	0.425	0.85	64	0.745	1.49	A4	1.065	2.13	E4	1.385	2.77
25	0.430	0.86	65	0.750	1.50	A5	1.070	2.14	E5	1.390	2.78
26	0.435	0.87	66	0.755	1.51	A6	1.075	2.15	E6	1.395	2.79
27	0.440	0.88	67	0.760	1.52	A7	1.080	2.16	E7	1.400	2.80
28	0.445	0.89	68	0.765	1.53	A8	1.085	2.17	E8	1.405	2.81
29	0.450	0.90	69	0.770	1.54	A9	1.090	2.18	E9	1.410	2.82
2A	0.455	0.91	6A	0.775	1.55	AA	1.095	2.19	EA	1.415	2.83
2B	0.460	0.92	6B	0.780	1.56	AB	1.100	2.20	EB	1.420	2.84
2C	0.465	0.93	6C	0.785	1.57	AC	1.105	2.21	EC	1.425	2.85
2D	0.470	0.94	6D	0.790	1.58	AD	1.110	2.22	ED	1.430	2.86
2E	0.475	0.95	6E	0.795	1.59	AE	1.115	2.23	EE	1.435	2.87
2F	0.480	0.96	6F	0.800	1.60	AF	1.120	2.24	EF	1.440	2.88
30	0.485	0.97	70	0.805	1.61	B0	1.125	2.25	F0	1.445	2.89
31	0.490	0.98	71	0.810	1.62	B1	1.130	2.26	F1	1.450	2.90
32	0.495	0.99	72	0.815	1.63	B2	1.135	2.27	F2	1.455	2.91
33	0.500	1.00	73	0.820	1.64	B3	1.140	2.28	F3	1.460	2.92
34	0.505	1.01	74	0.825	1.65	B4	1.145	2.29	F4	1.465	2.93
35	0.510	1.02	75	0.830	1.66	B5	1.150	2.30	F5	1.470	2.94
36	0.515	1.03	76	0.835	1.67	B6	1.155	2.31	F6	1.475	2.95
37	0.520	1.04	77	0.840	1.68	B7	1.160	2.32	F7	1.480	2.96
38	0.525	1.05	78	0.845	1.69	B8	1.165	2.33	F8	1.485	2.97
39	0.530	1.06	79	0.850	1.70	B9	1.170	2.34	F9	1.490	2.98
3A	0.535	1.07	7A	0.855	1.71	BA	1.175	2.35	FA	1.495	2.99
3B	0.540	1.08	7B	0.860	1.72	BB	1.180	2.36	FB	1.500	3.00
3C	0.545	1.09	7C	0.865	1.73	BC	1.185	2.37	FC	1.505	3.01
3D	0.550	1.10	7D	0.870	1.74	BD	1.190	2.38	FD	1.510	3.02
3E	0.555	1.11	7E	0.875	1.75	BE	1.195	2.39	FE	1.515	3.03
3F	0.560	1.12	7F	0.880	1.76	BF	1.200	2.40	FF	1.520	3.04

7.3.5 Startup and Shutdown

Startup

The startup sequence includes three sequential periods. During the first period, the device does initialization which includes building up internal LDOs and references, register value initialization, pin strap detection, enabling digital interface, and so forth. The initialization, which is not gated by EN pin voltage, starts as long as VCC/VDRV pin voltage is above the VCC UVLO rising threshold (3.2-V typical). The length of this period is about 200 µs for TPS544C26 device. The I^2C communication including both read and write operations is allowed after finishing the initialization.

Once the EN pin voltage crosses above EN high threshold (typically 1.2 V) the device moves to the second period, power-on delay. The power-on delay is programmable in TPS544C26 through register (60h) TON_DELAY with minimum 0.5 ms delay and maximum 2 ms delay.

The V_{OUT} soft-start is the third period. A soft-start ramp, which is an internal signal, starts when the chosen power-on delay finishes. The soft-start time can be selected in register (61h) TON_RISE with options of 1 ms, 2

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ms, 4 ms, 8 ms, and 16 ms. When starting up without pre-bias on the output, the VOUT ramps up from 0 V to either the selected Vboot value or the programmabled VOUT_CMD value (depending on the VOUT_CTRL setting) to avoid the inrush current by the output capacitor charging, and also minimize VOUT overshoot. The VOUT ramping up slew rate is determined by VOUT step (set by PROTOCOL_ID in register (C2h) PROTOCOL_ID_SVID, Vboot and TON_RISE values, and the actual soft-start time can vary from the selected TON_RISE value. 表 7-7 shows more details.

For the startup with a pre-biased output the device limits current from being discharged from the prebiased output voltage by preventing the low-side FET from forcing the SW node low until after the first PWM pulse turns on the high-side FET. Once the increasing reference voltage exceeds the feedback voltage which is internally divided down from (VOSNS−GOSNS) level, the high-side SW pulses start. This enables a smooth startup with a pre-biased output.

Once VOUT reaches the regulation value and VRRDY delay expires, the converter asserts VRRDY pin and becomes ready for SVID commands. The VRRDY delay can be programmed in (A0h) SYS_CFG_USER1 register and the default value is set to 0 ms to meet SVID communication requirement.

表 7-7. Soft-start Slew Rate and the Actual Soft-start Time

VOUT_CTRL	VOUT Control Method	VOUT Step	Soft-start Slew Rate (V/ms)	Actual Soft-start Time (ms)
00b	SVID only	5 mV or 10 mV	Vboot / TON_RISE	TON_RISE
01b	SVID + I²C	5 mV or 10 mV	Vboot / TON_RISE	(1 + I²C_OFFSET / Vboot) × TON_RISE
10b or 11b	I²C only	5 mV	1.1 V / TON_RISE	(VOUT_CMD + I²C_OFFSET) / 1.1 V × TON_RISE
10b or 11b	I²C only	10 mV	1.8 V / TON_RISE	(VOUT_CMD + I²C_OFFSET) / 1.1 V × TON_RISE

Shutdown

The TPS544C26 device also offers programmable soft-stop feature through I2C register (65h) TOFF_FALL with 0.5 ms, 1 ms, 2 ms, and 4 ms options. The soft-stop feature force a controlled decrease of the output voltage from regulation to 200 mV. Once Vout is discharged to 200 mV level the power stage stops switching and goes to tri-state. There can be negative inductor current forced during the TOFF_FALL time to discharge the output voltage. This feature can be enabled or disabled through I2C. Configuring EN_SOFT_STOP bit in register (A0h) SYS_CFG_USER1 to value “0” disables the soft-stop feature and automatically sets TOFF_DELAY to 0 ms.

In the case of Soft-stop is enabled, after a stop condition is received and the selected TOFF_DELAY delay expires, the TPS544C26 device enters the soft-stop operation during which the control loop actively controls the discharge slew rate of the output voltage. The power stage continues switching while the internal reference ramps down linearly. The discharge slew rate during this phase is determined by the selected boot up voltage (not the current output voltage) and the selected TOFF_FALL time. Once Vout is discharged to 200 mV level the power stage stops switching and goes to tri-state. The Vout discharge continues but the discharge slew rate is controlled by the load current. With this discharge operation, the TPS544C26 device controls the soft-stop slew rate rather the total soft-stop time, thus the total VOUT discharge time (a.k.a soft-stop time) can vary from the register (65h) TOFF_FALL value. Another word, The TOFF_FALL time is utilized to set the internal reference DAC ramp-down time from the regulation level to 0 mV. For example, under heavy load condition, the total soft-stop time from VOUT regulation level to zero volt is likely shorter than the programmed TOFF_FALL value. Under light load, the total soft-stop time likely becomes longer than the programmed TOFF_FALL value. Table Soft-stop Slew Rate and the Actual Soft-stop Time shows more details.

In the case of soft-stop feature is disabled through the *EN_SOFT_STOP* bit in (A0h) SYS_CFG_USER1 register, both high-side and low-side FET drivers are turned off immediately at the time when a stop condition is received (as programmed by the (02h) ON_OFF_CONFIG command), and the output voltage discharge slew rate is controlled by the external load.

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表 7-8. Soft-stop Slew Rate and the Actual Soft-stop Time

VOUT_CTRL	VOUT Control Method	VOUT Step	Soft-stop Slew Rate (V/ms)	Actual Soft-stop Time (ms)
00b	SVID only	5 mV or 10 mV	Vboot / TOFF_FALL	(Current VOUT − 0.2 V) / Vboot × TOFF_FALL + t_{DELAY} (1)
01b	SVID + I^2C	5 mV or 10 mV	Vboot / TOFF_FALL	(Current VOUT − 0.2 V) / Vboot × TOFF_FALL + t_{DELAY} (1)
10b or 11b	I^2C only	5 mV	1.1 V / TOFF_FALL	(Current VOUT − 0.2 V) / 1.1 V × TOFF_FALL + t_{DELAY} (1)
10b or 11b	I^2C only	10 mV	1.8 V / TOFF_FALL	(Current VOUT − 0.2 V) / 1.8 V × TOFF_FALL + t_{DELAY} (1)

(1) Power stage switching ends at VOUT = 200 mV. t_{DELAY} is determined by output capacitance and the load current.

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7.3.6 Dynamic Voltage Slew Rate

TPS544C26 device offers (AFh) DVS_CFG register to set SetVID-Fast slew rate during dynamic voltage scaling.

SetVID command sets the new target voltage. During the output voltage transition, due to the quick charge or discharge to output capacitors, the power stage sees extra inrush current. This inrush current plus load current can trigger overcurrent protection when there is no sufficient room from OCL or NOC setting. For example, the positive inductor current during VOUT step-up transition goes higher than nominal operation. If the LS valley OCL threshold is set relatively low and doesn't allow the extra inrush current, the inductor current is potentially limited by the cycle-by-cycle overcurrent limit feature, thus the actual step-up slew rate is lower than the desired value. Similar situation can happen to VOUT step-down transition with no load condition. The negative inductor current during VOUT step-down transition goes more negative than nominal operation. However, the inductor current is not allowed to go more negative than the Negative OC threshold. Thus, triggering NOC operation during VOUT step-down transition results that the actual step-down slew rate is lower than the desired value.

7.3.7 Adaptive Voltage Positioning (Droop) and DC Load Line (DCLL)

TPS544C26 device supports adaptive voltage positioning (AVP) through DC Load Line (DCLL) setting in the (ADh) COMP3 register. Use a non-zero DC load line reduces output voltage set-point as a function of the load current, with a controlled slope. This feature is optional and the DCLL setting usually matches what the processor suggests. If a processor doesn't utilize Droop, setting DCLL to 0 mΩ is recommended to avoid violating the VOUT tolerance band spec of the processor.

The DC load line provides two main benefits:

- Reducing the output voltage set-point, reduces the power consumption of the system, when the load current is high.
- Adaptive voltage positioning increases the allowable undershoot and overshoot during load transient events. Below figure compares example output voltage specifications for systems with zero load line and non-zero load line. The nominal setting for the output voltage is chosen to be higher, to allow the entire transient window as margin for transient overshoot and undershoot.

7.3.8 Loop Compensation

The TPS544C26 device provides several options for tuning the output voltage feedback and response to transients. Register (A9h) COMP1_MAIN, (AAh) COMP2_MAIN and (ADh) COMP3 configure the control loop compensation through these fields:

- DC Load Line: Selects the DC shift in output voltage corresponding to increased output current. See (ADh) COMP3 for available options.
- AC Gain: The gain of the integration and AC paths can be selected independently. The AC and integration gains both affect the small-signal bandwidth of the converter. The higher AC Gain, the faster the control loop responds to an output voltage error or a change on the current sense signal. Too high AC Gain results in less noise immunity (a.k.a higher jitter). See (A9h) COMP1_MAIN for available options.

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- AC Load Line (ACLL): Selects the AC response to an output voltage error. Lower ACLL configuration directly improves the load transient performance (less V_{OUT} deviation). However, the control loop becomes noise sensitive too low ACLL configuration. The ACLL also affects the settling and response time following a load transient event. See (A9h) COMP1_MAIN for available options.
- Integration Gain: To maintain a good VOUT regulation over load, the control loop includes an integration stage. Integration Gain selects the gain of the integration stage which affects the loop response to an output voltage error. Given the integration time constant is several times of switching cycle time, the Integration Gain affects the loop gain in middle frequency range. The gain of the integration and AC paths can be selected independently. The integration and AC gains both affect the small-signal bandwidth of the converter. See (AAh) COMP2_MAIN for available options.
- Integration Time Constant: The Integration Time Constant affects the settling and response time following an output voltage error. See (AAh) COMP2_MAIN for available options.
- Ramp Amplitude: A ramp based on PVIN/V_{OUT}/f_{SW} information is generated inside the IC to improve jitter performance. Smaller ramp settings result in faster response to load transient event, but also lead to increased off-time jitter. Likewise, large ramp settings result in lower frequency jitter, but becomes slightly slower to respond to an output voltage deviation. The ramp setting also affects the small-signal bandwidth of the converter. See (AAh) COMP2_MAIN for available options.

7.3.9 Set Switching Frequency

TPS544C26 device provides programmable operation mode including the forced CCM operation for tight output voltage ripple and auto-skipping Eco-mode for high light-load efficiency. The TPS544C26 device allows users to select the switching frequency through (33h) FREQUENCY_SWITCH register and operation mode through FCCM bit in (A0h) SYS_CFG_USER1. The available switching frequency options are 600 kHz, 800 kHz, 1 MHz and 1.2 MHz.

The FCCM bit is set during initial power-on and latched after the power conversion is enabled (EN=high). While the device is enabled, a write to FCCM bit ia acknowledged but the operation mode does not change until an EN toggle happens.

表 7-9. Switching Frequency Options

(33h) FREQUENCY_SWITCH (Hex)	f_{SW} (kHz)
00	600
01	800
02	1000
03	1200

7.3.10 Switching Node (SW)

The SW pins connect to the switching node of the power conversion stage. The SW pins act as the return path for the high-side gate driver. During nominal operation, the voltage swing on SW normally traverses from below ground to above the input voltage. Parasitic inductance in the PVIN to PGND loop (including the component from the PCB layout and also the component inside the package) and the output capacitance (COSS) of both power FETs form a resonant circuit that can produce high frequency (> 100 MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. TPS544C26 high-side gate driver is fine tuned to minimize the peak ringing amplitude so that a RC snubber on SW node is usually not needed. However, it is highly recommended for the user to measure the voltage stress across either the high-side or low-side FET and ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit listed in the Absolute Maximum Ratings table.

7.3.11 Overcurrent Limit and Low-side Current Sense

For a synchronous buck converter, the inductor current increases at a linear rate determined by the input voltage, the output voltage, and the output inductor value during the high-side MOSFET on-time (ON time). During the low-side MOSFET on-time (OFF time), this inductor current decreases linearly per slew rate determined by the output voltage and the output inductor value. The inductor during the OFF time, even with a negative slew rate, usually flows from the device SW node to the load the device which is said to be sourcing

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current and the output current is declared to be positive. This section describes the overcurrent limit feature based on the positive low-side current. The next section describes the overcurrent limit feature based on the negative low-side current.

The positive overcurrent limit (OCL) feature in the TPS544C26 device is implemented to clamp low-side *valley current* on a cycle-by-cycle basis. The inductor current is monitored during the OFF time by sensing the current flowing through the low-side MOSFET. When the sensed low-side MOSFET current remains above the selected OCL threshold, the low-side MOSFET stays ON until the sensed current level becomes lower than the selected OCL threshold. This operation extends the OFF time and pushes the next ON time (where the high-side MOSFET turns on) out. As a result, the OCL bit in (7Bh) STATUS_IOUT is set, also the average output current sourced by the device is reduced. As long as the load pulls a heavy load where the sensed low-side *valley current* exceeds the selected OCL threshold, the device continuously operates in this clamping mode which extends the current OFF time and pushes the next ON time out. The device does not implement a fault response circuit directly tied to the overcurrent limit circuit, instead, the VOUT Tracking UVF function is utilized to shuts the device down under an overcurrent fault. During an overcurrent event, the current sunk by the load (I_{OUT}) exceeds the current sourced by the device to the output capacitors, thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the selected undervoltage fault threshold, the VOUT Tracking UVF comparator detects and shuts down the device after the UVF Response Delay (programmable in (45h) VOUT_UV_FAULT_RESPONSE register). The device then responds to the Tracking UVF trigger per bit[3] *RESTART* selection in (45h) VOUT_UV_FAULT_RESPONSE register. With the *RESTART* bit unset (value "0"), the device latches OFF both high-side and low-side drivers. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *RESTART* bit set (value "1"), the device enters hiccup mode and re-starts automatically after a hiccup sleep time of 56 ms, without limitation on the number of restart attempts. In other words, the response to an overcurrent fault is set by the programmed UVF response.

If an OCL condition happens during a soft-start ramp the device still operates with the cycle-by-cycle current limit based on the sensed low-side valley current. This operation can limit the energy charged into the output capacitors thus the output voltage likely ramps up slower than the desired soft-start slew rate. During the soft-start, the VOUT Tracking UVF comparator is disabled thus the device does not respond to a UVF event. Upon the completion of the soft-start, the VOUT Tracking UVF comparator is enabled, then the device starts responding to the UVF event.

The OCL feature in the device is implemented by detecting the low-side valley current through analog circuitries and has no relationship with the integrated Analog-to-Digital converter (ADC). The telemetry analog-front-end gets an input from the low-side current sense circuit and average low-side MOSFET current from the start to the end of each low-side MOSFET on time. By this method, the telemetry sub-system reports the load current (IOUT) which is the average value of the inductor current but not peak or valley values.

7.3.12 Negative Overcurrent Limit

The TPS544C26 device is a synchronous Buck converter, thus the current can flow from the device to the load or from the load into the device through SW node. When current is flowing from the device SW node to the load the device is said to be sourcing current and the output current declared to be positive. When current is flowing into the device SW node from the load, the device is said to be sinking current and the current is declared to be negative.

The device offers a programmable, cycle-by-cycle negative overcurrent (NOC) limit through (B4h) IOUT_NOC_LIMIT register. The available NOC thresholds which scale with ICC_MAX setting (see ICC_MAX) are shown in 表 7-10. Similar with the positive overcurrent limit, the inductor current is monitored during the low-side MOSFET ON period. To prevent too large negative current and a damage of low-side MOSFET, the device turns off the low-side MOSFET after the detected on the low-side MOSFET exceeds the selected NOC limit. And then the high-side FET is turned on for an on-time determined by PVIN, SEL_NOC_TON bit (see (ADh) COMP3) and f_{SW} setting).

The NOC operation usually happens after an overvoltage event but can also happen during VOUT step-down transition with fast slew rate.

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表 7-10. Negative Overcurrent Limits

SEL_NOC[1:0]	Negative Overcurrent Limits (A)	
	ICC_MAX ≥ 15 A	ICC_MAX ≤ 10 A
00	−20	−10
01	−15	−7.5
10	−12	−6
11	−10	−5

7.3.13 Zero-Crossing Detection

TPS544C26 device implements an internal circuit for the zero inductor-current detection during skip-mode operation. The fixed Z-C detection threshold is set to a slightly positive value such as 300 mA to compensate the delay time of the Z-C detection circuit and avoid too-late detection. Depending on the inductor value, frequency, VIN and Vout conditions, this can result diode conduction for a short period.

7.3.14 Input Overvoltage Protection

The TPS544C26 device actively monitors the PVIN input voltage. When the PVIN voltage level is above the over-voltage threshold, TPS544C26 device stops switching and pulls VRRDY signal low. Two options are provided for PVIN OV rising threshold in (55h) VIN_OV_FAULT_LIMIT register while the PVIN OV falling threshold is always 13.5V.

Once the PVIN over-voltage fault is triggered, the device latches off until EN pin is toggled or PVIN is reset.

7.3.15 Output Overvoltage and Undervoltage Protection

The TPS544C26 device monitors the output voltage (VOSNS − GOSNS) to provide overvoltage (OV) and undervoltage (UV) protection. The Tracking OVF and Tracking UVF thresholds both track to the VOUT setting (commanded by either SVID SetVID command or I^2C (A6h) VOUT_CMD) but can be selected independently.

VOUT Tracking UVF

The 表 7-11 shows the available tracking UVF thresholds. When the output voltage (VOSNS − GOSNS) drops below the VOUT setting by the value configured in (44h) VOUT_UV_FAULT_LIMIT register, the tracking UVF comparator detects and an internal UVF Response Delay counter selected in (45h) VOUT_UV_FAULT_RESPONSE register begins. At the same time, the UVF bit in (7Ah) STATUS_VOUT register is set. When the UVF Response Delay expires, the device responds to the UV fault per bit[3] *RESTART* selection in (45h) VOUT_UV_FAULT_RESPONSE register. With the *RESTART* bit unset (value "0"), the device latches OFF both high-side and low-side drivers. The latch is cleared with a reset of VCC or by re-toggling the EN pin. With the *RESTART* bit set (value "1"), the device enters hiccup mode and re-starts automatically after a hiccup sleep time of 56 ms, without limitation on the number of restart attempts.

The tracking UVF function is enabled only after the soft-start period completes.

During the UVF Response Delay, if the output voltage (VOSNS − GOSNS) rises above the UVF threshold, thus not qualified for a UVF event, the UVF response delay timer resets to zero. When the VOUT drops below the UVF threshold again, the UVF response delay timer re-starts from zero.

The TPS544C26 device also offers tracking UV Warning (UVW) function. The 表 7-12 shows the available tracking UVW thresholds. When the output voltage (VOSNS − GOSNS) drops lower than the VOUT setting by the value configured in (43h) VOUT_UV_WARN_LIMIT register, the tracking UVW comparator detects and the UVW bit in (7Ah) STATUS_VOUT register is set. There is no purpose delay for UVW event.

表 7-11. VOUT Tracking UV Fault Thresholds

SEL_UVF[1:0]	VOUT Tracking UVF Threshold (mV)
00	−150
01	−200

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表 7-11. VOUT Tracking UV Fault Thresholds (continued)

SEL_UVF[1:0]	VOUT Tracking UVF Threshold (mV)
10	−200
11	−300

表 7-12. VOUT Tracking UV Warning Thresholds

SEL_UVW[1:0]	VOUT Tracking UVW Threshold (mV)
00	−100
01	−150
10	−200
11	−300

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VOUT Tracking OVF

The 表 7-13 shows the available tracking OVF thresholds. When the output voltage (VOSNS − GOSNS) rises higher than the VOUT setting by the value configured in (40h) VOUT_OV_FAULT_LIMIT register, the tracking OVF comparator detects and the device responds to the OV fault immediately per bit[3] *RESTART* selection in (41h) VOUT_OV_FAULT_RESPONSE register. At the same time, the OVF bit in (7Ah) STATUS_VOUT register is set. With the *RESTART* bit unset (value "0"), the device latches OFF the high-side MOSFET driver and turns on the low-side MOSFET. The low-side MOSFET is kept ON until the sensed low-side negative current reaches the selected negative overcurrent (NOC) limit (see (B4h) IOUT_NOC_LIMIT register). Upon reaching the NOC limit, the low-side MOSFET is turned off, and the high-side MOSFET is turned on, for an on-time determined by PVIN, SEL_NOC_TON bit (see (ADh) COMP3) and f_{SW} setting. After the high-side MOSFET turns off the low-side MOSFET turns on again and the negative current on low-side MOSFET is monitored to compare with the selected NOC limit. The device operates in this cycle until the output voltage is fully discharged. Then the device has high-side MOSFET latched OFF and low-side MOSFET latched ON. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *RESTART* bit set (value "1"), the device still discharge output voltage by the NOC operation. However, the device activates hiccup mode and re-starts automatically after a hiccup sleep time of 56 ms, without limitation on the number of restart attempts. The hiccup sleep time counter starts right after the OVF trigger.

The tracking OVF function is enabled only after the soft-start period completes.

The TPS544C26 device also offers tracking OV Warning (OVW) function. The 表 7-14 shows the available tracking OVW thresholds. When the output voltage (VOSNS − GOSNS) rises higher than the VOUT setting by the value configured in (42h) VOUT_OV_WARN_LIMIT register, the tracking OVW comparator detects and the OVW bit in (7Ah) STATUS_VOUT register is set. There is no purpose delay for OVW event.

表 7-13. VOUT Tracking OV Fault Thresholds

SEL_OVF[1:0]	VOUT Tracking OVF Threshold (mV)
00	+100
01	+150
10	+200
11	+300

表 7-14. VOUT Tracking OV Warning Thresholds

SEL_OVW[1:0]	VOUT Tracking OVW Threshold (mV)
00	+100
01	+150
10	+200

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表 7-14. VOUT Tracking OV Warning Thresholds (continued)

SEL_OVW[1:0]	VOUT Tracking OVW Threshold (mV)
11	+300

VOUT Fixed OVF

In parallel with VOUT tracking OVF the TPS544C26 device offers Fixed OVF feature. The Fixed OVF comparator implments a constant reference which is configured in (B4h) IOUT_NOC_LIMIT register and the reference level does not track with the VOUT setting. The Fixed OVF comparator is activated to monitor the output voltage (VOSNS − GOSNS) all the time including power conversion off period (EN = low) and soft-start period. Once the VOUT Fixed OVF is triggered, the OVF bit in (7Ah) STATUS_VOUT register is set, and the device enters NOC operation immediately no matter the power conversion is enabled or not. The device operates in NOC operation to fully discharge the output voltage. Then the device has high-side MOSFET latched OFF and low-side MOSFET latched ON. The latch is cleared with a reset of VCC or by toggling the EN pin. A Fixed OVF event always leads to latch-off response and the selected OVF response in (41h) VOUT_OV_FAULT_RESPONSE register does not affect the response for a Fixed OVF event.

Given the Fixed OVF comparator is always activated the device provides alternate protection to high-side MOSFET damage cases. When the high-side MOSFET is damaged and short PVIN to the SW node, the output voltage (VOSNS − GOSNS) rises quickly. The TPS544C26 device can detect this kind of event and turn on low-side MOSFET to discharge the excess energy, thus protecting the load from damage.

In a case that the commanded VOUT is higher than the Fixed OVF threshold, the device triggers Fixed OV fault and enters the NOC operation immediately. If this scenario happens before soft-start, the device never initiate the soft-start ramp and enters latch-off directly. To avoid this situation, the Fixed OVF feature can be disabled through the bit[2] *EN_FIX_OVF* in (B4h) IOUT_NOC_LIMIT register.

表 7-15. VOUT Fixed OV Fault Thresholds

PROTOCOL_ID in (C2h) PROTOCOL_ID_SVID	SEL_FIX_OVF[1] in (B4h) IOUT_NOC_LIMIT	VOUT Fixed OVF Threshold (V)
PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)	0	1.5
PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)	1	1.8
PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)	0	2.4
PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)	1	3.0

7.3.16 Overtemperature Protection

To have full coverage for a potential overtemperature event, the TPS544C26 device implements three overtemperature protection circuitries - two on the Controller die and one on the Power Stage (PS) die.

Programmable OTP by Monitoring the Controller Die Temperature

The on-die temperature sense circuit senses the controller die temperature. The sensed signal is fed into an internal ADC and converted to the Controller die temperature which is reported as (8Dh) READ_TEMPERATURE_1 through the Telemetry sub-system. This feature utilizes a digital comparator that compares the output of the IC TEMPERATURE telemetry to the fault threshold selected in (4Fh) OT_FAULT_LIMIT register. The device stops the SW switching when the sensed IC temperature goes beyond the selected threshold. The device response to a Programmable OTP event is described in (50h) OT_FAULT_RESPONSE.

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Analog OTP by Monitoring the Controller Die Temperature

The sensed temperature signal is fed into an analog OTP circuit on the Controller die as well. An analog comparator is utilized to compare the output of the Controller die temperature sensing circuit to a fixed threshold (rising 166 °C typical). The device stops the SW switching when the sensed IC temperature goes beyond the fixed threshold. The device response to an Analog OTP event is always the same as the Programmable OTP.

Given the fixed threshold (166 °C typical) for the Analog OTP is higher than the highest setting (150 °C typical) in Programmable OTP, the Analog OTP is unlikely to trigger during the nominal operation.

Analog OTP by Monitoring the Power Stage Die Temperature

A temperature sensing circuit is implemented in the Power Stage (PS) die. This sensed is fed into an analog OTP circuit on the PS die. An analog comparator is utilized to compare the output of the PS die temperature sensing circuit to a fixed threshold (rising 166 °C typical). The device stops the SW switching when the sensed IC temperature goes beyond the fixed threshold. Once the PS die temperature falls 30 °C below the rising threshold, the device automatically restarts with an initiated soft-start. This Analog OTP is a non-latch protection.

7.3.17 VR Ready

The TPS544C26 device offers VRRDY output that asserts high when the converter output is within the target. The VRRDY output stays low when the switching is disabled either by EN pin or through I2C (01h) OPERATION command. The VRRDY function is activated after the soft-start ramp is completed. The VRRDY output is an open-drain output and must be pulled up externally through a pull-up resistor (usually 10 kΩ). The recommended VRRDY pull-up resistor value is 1 kΩ to 100 kΩ.

7.3.18 Catastrophic Fault Alert: CAT_FAULT#

The device has CAT_FAULT# output on pin 28 which alerts the system to potentially catastrophic power supply faults. The CAT_FAULT# output is an open-drain output and must be pulled up externally through a pullup resistor. The recommended CAT_FAULT# pull-up resistor value is 3.3 kΩ to 10 kΩ while pulling up to 3.3 V voltage source through a 4.99 kΩ resistor is commonly used. The CAT_FAULT# function is activated after VCC/VDRV pin voltage rises above VCC UVLO rising threshold (3.2V typical) regardless of by EN pin logic level.

Fault conditions which assert the CAT_FAULT# pin include:

- Over-voltage fault detected by fixed VOUT OVP
- Over-voltage fault detected by tracking VOUT OVP
- Under-voltage fault detected by tracking VOUT UVP, including the an UV fault caused by overcurrent event
- Over-temperature fault (based on the threshold set through I2C in (4Fh) OT_FAULT_LIMIT register)
- Powerstage OT or VDRV_UV faults (Either fault asserts PS_FLT status bit in (80h) STATUS_MFR register)

Once asserted low by a fault event CAT_FAULT# pin latches low until a reset of PVIN or an EN toggle.

7.3.19 Telemetry

The telemetry sub-system in the controller core supports the following measurements:

- Input voltage (direct measurement)
- Input current (direct measurement)
- Output voltage (direct measurement)
- Output current (direct measurement)
- Controller die temperature (direct measurement)
- Input Power (Calculation, the product of the input voltage and the input current)

The ADC output is a single conversion of each measurement without rolling window averaging for fast refresh rate of these key system parameter. All above parameters are measured sequentially while the Input current and Output current are measured more often than the others. This sequence design allows each IIN or IOUT telemetry value to be updated within 95 µs, while each of the rest of telemetry value to be updated within 190 µs.

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Input Power Telemetry (VIN/IIN/PIN)

The input voltage sense telemetry senses the voltage level on pin 4 VINSENM. The device offers internal divider to minimize the external component count and save solution size. The VIN reporting range is limited from 8 V to 16 V to improve the reporting resolution. For any VIN value less than 8 V, the VIN reports 8 V. For any VIN value higher than 16 V, the VIN reports 16 V. For example, the READ_VIN reports 8 V for a VIN = 6 V condition. The VIN conversion equation is:

$$\text{VIN} = \text{READ_VIN} \times 0.03125 + 8 \quad (1)$$

Where

- VIN is the voltage level seen on pin 4 VINSENM
- READ_VIN is the I^{2}C (88h) READ_VIN register value in decimal

The input current sense telemetry senses the differntial voltage level across pin 3 VINSENP and pin 4 VINSENM. A high accuracy sensing resistor in series with the input bus is commonly used for this feature. Together with the setting in (B3h) PIN_SENSE_RES register, the ADC converts the sensed differential voltage to input current in amp. The device offers internal gain stage to minimize the external component count and save solution size. Given the sensed differential voltage is in millivolts range and to avoid impact from the switching noise on the input bus, a ceramic bypass capacitor is required on each pin (pin 3 VINSENP and pin 4 VINSENM) referring to PGND and the recommended value is at least 100 pF with X7R temperature characterisitic. The IIN conversion equation is:

$$\text{IIN} = \text{READ_IIN} \times \frac{\text{IIN_MAX}}{256} \quad (2)$$

Where

- IIN is the input current level flowing through the choosen IIN sensing resistor
- READ_IIN is the I^{2}C (89h) READ_IIN register value in decimal
- IIN_MAX is a maximum input current value selected in I^{2}C (B3h) PIN_SENSE_RES register

The input power reported in (97h) READ_PIN register is a simple calculation, which is the product of the measured raw input voltage and the measured raw input current. The calculation does not use the register value in (88h) READ_VIN and (89h) READ_IIN. The PIN conversion equation is:

$$\text{PIN} = \text{READ_PIN} \times \frac{\text{PIN_MAX}}{255} \quad (3)$$

Where

- PIN is the calculated input power value
- READ_PIN is the I^{2}C (97h) READ_PIN register value in decimal
- PIN_MAX is a maximum input power value selected in I^{2}C (6Bh) PIN_OP_WARN_LIMIT register

When input power feature is not used, follow below connection for pin 3 VINSENP and pin 4 VINSENM so that the device can report the input voltage level on PVIN node:

1. Short pin 3 VINSENP to pin 4 VINSENM,
2. Place a 0.1 µF ceramic bypass capacitor on pin 4 VINSENM referring to AGND,
3. Connect pin 4 VINSENM to PVIN node of TPS544C26 device.

VOUT and IOUT Telemetry

The output voltage sense telemetry senses the differential voltage across VOSNS to GOSNS pin. The conversion equation for VOUT is related with VOUT step (5 mV or 10 mV) which is defined by *PROTOCOL_ID* bits in I^{2}C (C2h) PROTOCOL_ID_SVID register.

The VOUT conversion equation for 5 mV step is:

$$\text{VOUT} = \text{READ_VOUT} \times 0.00625 + 0.125 \quad (4)$$

The VOUT conversion equation for 10 mV step is:

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$$VOUT = READ_VOUT \times 0.0125 + 0.250 \quad (5)$$

Where

- VOUT is the sensed output voltage (VOSNS−GOSNS)
- READ_VOUT is the I²C (8Bh) READ_VOUT register value in decimal

The output current sense telemetry senses the average of low-side FET current from the start to the end of each low-side FET on time which provides the average inductor current. To achieve high accuracy and wide report range, the device automatically sets the current sense gain based on ICC_MAX setting in (C0h) ICC_MAX register. When the ICC_MAX is equal or greater than 15 A, the current sense gain is set to a smaller value to achieve wide report range. When the ICC_MAX is equal or less than 10 A, the current sense circuit uses a higher gain to get a significant amplitude and achieve good accuracy. The change of gain setting does not affect the positive overcurrent limit (OCL) threshold but affect the negative overcurrent (NOC) threshold. The IOUT conversion equation is:

$$IOUT = READ_IOUT \times \frac{ICC_MAX}{255} \quad (6)$$

Where

- IOUT is the DC output current flowing from the output capacitors to the load
- READ_IOUT is the I²C (8Ch) READ_IOUT register value in decimal
- ICC_MAX is a full-scale value selected in I²C (C0h) ICC_MAX register

IC Temperature Telemetry

The die temperature sense telemetry senses the controller die temperature. The power stage die implementes its own over-temperature protection and power stage die temperature is not reported through temetry sub-system. The IC Temperature conversion equation is:

$$TEMP = READ_TEMPERATURE_1 - 40 \quad (7)$$

Where

- TEMP is the controller die temperature
- READ_TEMPERATURE_1 is the I²C (8Dh) READ_TEMPERATURE_1 register value in decimal

7.3.20 I²C Interface General Description

The TPS544C26 device offers both I²C interface and SVID interface for programming and telemetry report. The device supports a group of I²C registers which is listed in . The device also supports a subset of the SVID registers listed in .

For I²C interface, the TPS544C26 device supports minimum 50 kHz and maximum 1 MHz operating frequency range, with the support of the Standard-mode, Fast-mode, and Fast-mode Plus bus timing requirements.

The high threshold of I²C SCL and SDA pin is 0.585 V typical, and the low threshold of I2C SCL and SDA pin is 0.515 V typical.

The TPS544C26 device contains nonvolatile memory that is used to store user-accessible configurations. The settings programmed into the device are not automatically saved into this nonvolatile memory. The (15h) STORE_USER_ALL command must be used to commit the current I²C settings to nonvolatile memory as device defaults. For example, after importing a group of settings from a user specific configuration file the (15h) STORE_USER_ALL command must be used to save the settings into the nonvolatile memory. The settings that are capable of being stored in nonvolatile memory are noted in their detailed descriptions.

注

Per I²C Standard, the packet error checking (PEC) feature is not supported by TPS544C26. A command with PEC can result in unexpected communication error.

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7.3.20.1 Setting the I²C Address

The TPS544C26 device offers selectable 7-bit I²C address either through a resistor from the I²C_ADDR pin (pin 29) to AGND, or programmable by writing an 7-bit address value into the (A2h) I²C_ADDR register.

As the default configuration, a resistor from the I²C_ADDR pin (pin 29) to AGND sets the pre-configured 7-bit I²C address (0x70 to 0x7F) in the memory map. Up to 16 different addresses can be set, allowing 16 devices with unique addresses in a single system. TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C

As an alternative method, the I²C address of a TPS544C26 device can be programmed by writing an address value into (A2h) I2C_ADDR register. This register supports the full range from 00h to 7Fh (7-bit, '0000000' to '1111111'). And, an override bit has to be set to '1' so that TPS544C26 device ignores the pin 29 detection and straightly go to (A2h) I²C_ADDR register for I²C address. This method allows much more flexibility on the address selections. This override bit locates in (A0h) SYS_CFG_USER1 register bit[0].

For the programmed address to take effect, below actions have to be taken:

1. Write the desired I²C address value to bit[6:0] in the (A2h) I2C_ADDR register.
2. Set the OVRD_I2C_ADDR bit in the (A0h) SYS_CFG_USER1 register.
3. Store the new values to EEPROM by writing "1" to bit[0] in (15h) STORE_USER_ALL register. The whole store process takes 150 ms to finish.
4. Wait sufficient time for the store action to finish. Power cycle the device. During the power-on, the address programmed to the (A2h) I2C_ADDR register takes effect.

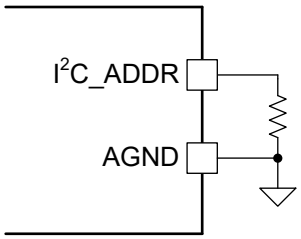


図 7-1. I2C Address Pin-strapping

表 7-16. I2C_ADDR pin resistor selected values

R_{ADDR} (kΩ)	(A2h) I²C_ADDR (Bin)	(A2h) I²C_ADDR (Hex)
SHORT	1110000	70
5.62	1110001	71
9.53	1110010	72
14	1110011	73
21	1110100	74
30.1	1110101	75
36.5	1110110	76
43.2	1110111	77
51.1	1111000	78
61.9	1111001	79
75	1111010	7A
88.7	1111011	7B
105	1111100	7C
127	1111101	7D
150	1111110	7E
FLOAT	1111111	7F

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For example, using 9.53 kΩ selects 1110010b (72h) as the 7-bit I²C address. Then the 8-bit I²C address is 11100100b (E4h), which is the 7-bit address followed by the write bit 0b.

表 7-17. I²C 8-bit Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	0	1	0	0
7 bits set by address pin resistor							Write bit

7.3.20.2 I²C Write Protection

The TPS544C26 device offers write protection feature through (B1h) REG_LOCK register. After power-on, the user accessible registers with write access are by default under "write protected" state, meaning the response to a write is NACK. The device always acknowledges a read command and responds the data byte accordantly. Only after writing the correct passcodes (multiple writes in the right order) into this REG_LOCK register, the user accessible registers are "unlocked" and the device acknowledges the next write commands. (B1h) REG_LOCK shows more details.

7.3.20.3 I²C Registers With Special Handling

In most cases the effect of an I²C write to a register is immediate: Once the write is performed, the value becomes available for use in the system. There are a few exceptions with special handling for preserving the integrity of the system.

Prevent write when the SW switching is enabled

A write to the following list of registers is prevented and the system response is to NACK writes to these registers when the SW switching is enabled. For example, before importing the user specific configuration, disabling the SW switching is required to successfully import a new value to these registers.

- (16h) RESTORE_USER_ALL
- (60h) TON_DELAY
- (61h) TON_RISE
- (64h) TOFF_DELAY
- (65h) TOFF_FALL
- (BDh) EXT_CAPABILITY_VIDOMAX_H
- (BEh) VIDO_MAX_L

When ON_OFF_CONFIG is set to *Always On*, the values from the NVM restore for these registers will be NACKed and will never become effective. Even the NVM restore during power-on initialization is affected by this kind of configuration.

Register update waits until the SW switching is disabled

When a write to one of these registers is accepted (ACKed), one or more bit-fields in this register are allowed to take effect immediately only if the SW switching is disabled. If the SW switching is enabled, the previous value for those bit-fields continues to be used by the system, and the new value for those bit-fields is kept ready inside the IC but only become effective the next time when the SW switching is disabled. A readback attempt will be accepted (ACKed) and return the most recent ACKed value.

- (A0h) SYS_CFG_USER1 register, FCCM bit
- (A0h) SYS_CFG_USER1 register, VOUT_CTRL field
- (A0h) SYS_CFG_USER1 register, EN_SOFT_STOP bit
- (A0h) SYS_CFG_USER1 register, VRRDY_DELAY field
- (A1h) SVID_ADDR
- (C2h) PROTOCOL_ID_SVID register, ALL_CALL_SEL field
- (A8h) I²C_OFFSET, but only when VOUT_CTRL field is set to “01b”

When ON_OFF_CONFIG is set to *Always On*, the values from the NVM restore can be kept in the staging area and never become effective. Even the NVM restore during power-on initialization is affected by this kind of configuration.

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Register update waits for a power cycling or a manual restore

When a write to one of these register is accepted (ACKed), one or more bit-fields in the register are not allowed to take effect at all. The new value takes effect only if the value is stored into NVM first and then retrieved from NVM after the device is powered on.

- (A0h) SYS_CFG_USER1 register, OVRD_SVID_ADDR bit
- (A0h) SYS_CFG_USER1 register, OVRD_I2C_ADDR bit
- (A2h) I²C_ADDR register, I²C_ADDR filed

The sequence of events, for the contents of those fields to take effect is as follows:

1. The user writes the desired value to the register,
2. The user executes an NVM store command ((15h) STORE_USER_ALL),
3. The part is power-cycled.

7.4 Device Functional Modes

7.4.1 Forced Continuous-Conduction Mode

When the operation mode is set to FCCM, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

When FCCM is selected, the TPS544C26 device operates at CCM during the whole soft-start period as well as the nominal operation.

7.4.2 Auto-Skip Eco-mode™ Light Load Operation

When the operation mode is set to DCM, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation IOUT(LL) (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in below equation.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (8)$$

Where

- f_{SW} is the switching frequency

TI recommends sing low ESR capacitors (such as ceramic capacitor) for skip-mode.

7.5 Programming

7.5.1 Supported I²C Registers

The Supported I²C and Default Values Table lists the implemented registers and also the default for the bit behavior and register values.

表 7-18. Supported I²C and Default Values

Register address	Register Name	R/W	NVM	Default Value (Hex)	Default Behavior
01h	OPERATION	R/W	NO	00h	OPERATION OFF

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表 7-18. Supported I²C and Default Values (continued)

Register address	Register Name	R/W	NVM	Default Value (Hex)	Default Behavior
02h	ON_OFF_CONFIG	R/W	YES	40h	Turn ON/OFF by EN pin only
03h	CLEAR_FAULTS	W	NO	N/A	Clear all faults
15h	STORE_USER_ALL	W	NO	N/A	Stores all current storable register settings into NVM
16h	RESTORE_USER_ALL	W	NO	N/A	Restores all storable register settings from NVM
33h	FREQUENCY_SWITCH	R/W	YES	01h	Switching frequency is set to 800 kHz
35h	VIN_ON	R/W	YES	03h	ON threshold is determined by both PVIN and VCC conditions. Both PVIN > 2.55 V and VCC > 3.8 V conditions have to be satisfied to enable the power conversion.
36h	VIN_OFF	R/W	YES	07h	OFF threshold is determined by both PVIN and VCC conditions. Either PVIN ≤ 2.3 V or VDRV ≤ 3.4 V disables the power conversion.
40h	VOUT_OV_FAULT_LIMIT	R/W	YES	02h	VOUT Tracking OV Fault threshold = +200 mV
41h	VOUT_OV_FAULT_RESPONSE	R/W	YES	00h	Latch-off after a fault
42h	VOUT_OV_WARN_LIMIT	R/W	YES	01h	VOUT Tracking OV Warning threshold = +150 mV
43h	VOUT_UV_WARN_LIMIT	R/W	YES	01h	VOUT Tracking UV Warning threshold = −150 mV
44h	VOUT_UV_FAULT_LIMIT	R/W	YES	02h	VOUT Tracking UV Fault threshold = −200 mV
45h	VOUT_UV_FAULT_RESPONSE	R/W	YES	02h	Latch-off after a fault, and the response delay before disabling the power conversion is 64 µs
46h	IOUT_OC_FAULT_LIMIT	R/W	YES	09h	Low-side valley current limiting threshold = 35 A
4Fh	OT_FAULT_LIMIT	R/W	YES	07h	Programmable OT Fault threshold = 150 °C
50h	OT_FAULT_RESPONSE	R/W	YES	00h	Latch-off after a fault
51h	OT_WARN_LIMIT	R/W	YES	06h	Programmable OT Warning threshold = 125 °C
55h	VIN_OV_FAULT_LIMIT	R/W	YES	01h	PVIN OV Fault threshold = 18.5 V
60h	TON_DELAY	R/W	YES	00h	0.5 ms delay when a start condition is received (as programmed by the ON_OFF_CONFIG register) until the output voltage starts to rise
61h	TON_RISE	R/W	YES	00h	1 ms from when the output starts to rise until the output voltage has entered the regulation band
64h	TOFF_DELAY	R/W	YES	00h	0 ms from when a stop condition is received (as programmed by the ON_OFF_CONFIG register) until the unit starts the soft-stop operation
65h	TOFF_FALL	R/W	YES	00h	0.5 ms from the end of the turn-off delay time until the internal reference DAC is commanded to 0 mV
6Bh	PIN_OP_WARN_LIMIT	R/W	YES	03h	Maximum PIN (input power) threshold = 360 W
7Ah	STATUS_VOUT	R/W	NO	N/A	Current status
7Bh	STATUS_IOUT	R/W	NO	N/A	Current status
7Ch	STATUS_INPUT	R/W	NO	N/A	Current status
7Dh	STATUS_TEMPERATURE	R/W	NO	N/A	Current status
80h	STATUS_MFR_SPECIFIC	R/W	NO	N/A	Current status
88h	READ_VIN	R	NO	N/A	Measured input voltage on pin 4 VINSENM
89h	READ_IIN	R	NO	N/A	Measured input current over the external sensing resistor
8Bh	READ_VOUT	R	NO	N/A	Measured output voltage
8Ch	READ_IOUT	R	NO	N/A	Measured output current
8Dh	READ_TEMPERATURE_1	R	NO	N/A	Measured Controller die temperature
97h	READ_PIN	R	NO	N/A	Calculated input power, the product of the measured input voltage and input current
A0h	SYS_CFG_USER1	R/W	YES	10h	Operation mode under light load condition is DCM VOUT is controlled by SVID bus only Soft-stop feature is enabled VR Ready delay = 0 ms I²C address is set by pin 29 pin strap detection

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表 7-18. Supported I²C and Default Values (continued)

Register address	Register Name	R/W	NVM	Default Value (Hex)	Default Behavior
A2h	I²C_ADDR	R/W	YES	N/A	Bit[7] = 0b, reserved for TI usage I²C address saved in NVM is 77h. However, after initial power-on, the effective I²C address shown in this field is determined by the resistor on pin 29
A3h	SVID_ADDR	R/W	YES	00h	Device address for SVID communication is set to 00h
A4h	IMON_CAL	R/W	YES	78h	IMON gain calibration = 0% IMON offset calibration = 0 A
A5h	IIN_CAL	R/W	YES	78h	IIN gain calibration = 0% IIN offset calibration = 0 A
A6h	VOUT_CMD	R/W	YES	ABh	Default VOUT setting saved in VOUT_CMD is 1.1V. The VOUT_CMD does not control VOUT unless VOUT_CTRL = 10b or 11b
A7h	VID_SETTING	R	NO	N/A	After initial power-on, this register shows a value reflecting the last commanded VOUT either from SVID bus or I²C bus
A8h	I²C_OFFSET	R/W	YES	00h	I²C OFFSET = 0 mV
A9h	COMP1_MAIN	R/W	YES	4Ah	AC Gain = 2 AC Load Line = 7
AAh	COMP2_MAIN	R/W	YES	19h	Integration gain = 2 Integration time constant = 4.25 µs Ramp Amplitude = 60 mV
ABh	COMP1_ALT	R/W	YES	23h	This register is not activated in the TPS544C26 device and affects nothing.
ACh	COMP2_ALT	R/W	YES	A2h	This register is not activated in the TPS544C26 device and affects nothing.
ADh	COMP3	R/W	YES	02h	Bit[7] = 0b, reserverd for TI usage Force DCM during soft-start enable/disable bit = disabled On-time during NOC (Negative OC) operation = longer t_{ON_NOC} L_{OUT} (output inductor value) for current sensing circuit = 100 nH DC Load Line = 0.75 mΩ
AFh	DVS_CFG	R/W	YES	06h	Dynamic voltage change fast slew rate configuration = 10 mV/µs
B0h	DVID_OFFSET	R/W	YES	00h	DVID Up positive DAC offset = 0 mV DVID Down positive DAC offset = 0 mV
B1h	REG_LOCK	W	YES	N/A	The user-accessible registers (not including B1h) are “write protected” and by default. User can still read back from registers
B3h	PIN_SENSE_RES	R/W	YES	05h	Input power sense resistor is 0.5 mΩ. This also sets the Maximum IIN to 40 A with IIN_LSB = 0.15625 A
B4h	IOUT_NOC_LIMIT	R/W	YES	05h	VOUT Fixed OV Fault threshold = 1.5 V VOUT Fixed OV Fault enable/disable bit = enabled Negative OC limit = −15 A when ICC_MAX ≥ 15 A or −7.5 A when ICC_MAX < 10 A
B5h	USER_DATA_01	R/W	YES	00h	Bit[7:4]: For user to store manufacturer specific information
B6h	USER_DATA_02	R/W	YES	00h	Bit[7:5]: For user to store manufacturer specific information
BAh	STATUS1_SVID	R/W	YES	N/A	A direct copy of the bits of SVID STATUS_1 register
BBh	STATUS2_SVID	R/W	YES	N/A	A direct copy of the bits of SVID STATUS_2 register
BCh	CAPABILITY	R	NO	FBh	A direct copy of the bits of SVID CAPABILITY register
BDh	EXT_CAPABILITY_VIDOMAX_H	R/W	YES	04h	A direct copy of the bits of SVID VIDOMAX_H_CAPA register

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表 7-18. Supported I²C and Default Values (continued)

Register address	Register Name	R/W	NVM	Default Value (Hex)	Default Behavior
BEh	VIDOMAX_L	R/W	YES	B6h	9-bit VIDoMAX = 1.155 V
C0h	ICC_MAX	R/W	YES	05h	ICC_MAX = 30 A
C1h	TEMP_MAX	R/W	YES	06h	TEMP_MAX = 125 °C while controls SVID "ThermAlert" bit
C2h	PROTOCOL_ID_SVID	R/W	YES	63h	PROTOCOL_ID_SVID = 07h (VR13, VOUT step 5 mV) Vboot = 1.1 V Respond to SVID All-call address both 0Eh and 0Fh
C6h	VENDOR_ID	R	NO	22h	SVID VENDOR_ID = 22h. This vendor ID is assigned to Texas Instruments by Intel, to identify the VR vendor.
C8h	PRODUCT_ID	R	NO	13h	TPS544C26 Product ID = 13h
C9h	PRODUCT_REV_ID	R	NO	02h	TPS544C26 current device revision = PG2.1

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7.5.2 Support of Intel SVID Interface

The TPS544C26 device supports Intel SVID interface (VR13 Mode). Details are described in this section.

The SVID address for a TPS544C26 device can be programmabled in (A3h) SVID_ADDR register, allowing address value from 00h to 0Dh.

The TPS544C26 device supports VR13 Mode SVID registers and also VIDoMAX register. The table below summarizes the SVID register initialization performed by TPS544C26 at each power-on. Any writeable register can be changed by the SVID host after initialization. Refer to the Intel documentation for more detailed description of the individual register functionality.

表 7-19. SVID Register Support (VR13 Mode)

Register Address	Register Name	R/W	Source or Behavior
00h	VENDOR_ID	R	22h
01h	PROD_ID	R	Per I²C register (C8h) PRODUCT_ID
02h	PROD_REV	R	Per I²C register (C9h) PROD_REV_ID
05h	PROTOCOL_ID	R	Per I²C register (C2h) PROTOCOL_ID_SVID[7:6]
06h	CAPABILITY	R	FBh
09h	VIDOMAX_H_CAPA	R	Per I²C register (BDh) EXT_CAPABILITY_VIDOMAX_H[7:0]
0Ah	VIDOMAX_L	R	Per I²C register (BEh) VIDO_MAX_L[7:0]
0Bh	VIN_FULLSCALE_H	R	06h
0Ch	VIN_FULLSCALE_L	R	40h
0Dh	VOUT_FULLSCALE_H	R	0Ch
0Eh	VOUT_FULLSCALE_L	R	80h
0Fh	ALLCALL_ACT	R/W	Per I²C register (C2h) PROTOCOL_ID_SVID[1:0]
10h	STATUS1	R	Current status
11h	STATUS2	R	Current status
12h	TEMPERATURE	R	Current status
15h	IOUT_H	R	Current status
16h	VOUT_H	R	Current status
17h	VR_TEMP	R	Current status
19h	IIN_H	R	Current status
1Ah	VIN_H	R	Current status
1Bh	PIN_H	R	Current status
1Ch	STATUS2_LASTREAD	R	Current status
20h	ICC_IN_MAX	R	FFh
21h	ICC_MAX	R	Per I²C register (C0h) ICC_MAX[2:0]
22h	TEMP_MAX	R	Per I²C register (C1h) TEMP_MAX[2:0]
24h	SR_FAST	R	Per I²C register (AFh) DVS_CFG[2:0]
25h	SR_SLOW	R	Programmed by SVID register (2Ah) SLOW_SR_SEL_HC
26h	VBOOT	R	Per I²C register (C2h) PROTOCOL_ID_SVID[5:2]
2Ah	SLOW_SR_SEL_HC	R/W	02h
2Bh	PS4_EXIT_LAT	R	85h
2Eh	PIN_MAX	R	Per I²C register (6Bh) PIN_OP_WARN_LIMIT
30h	VID_MAX	R/W	FFh
31h	VID_SETTING	R	Current status
32h	PWR_STATE	R	00h
33h	OFFSET	R/W	00h
34h	MULTI_VR_CONFIG	R/W	01h
3Ah	WP0	R/W	00h
3Bh	WP1	R/W	00h
3Ch	WP2	R/W	00h
3Dh	WP3	R/W	00h

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表 7-19. SVID Register Support (VR13 Mode) (continued)

Register Address	Register Name	R/W	Source or Behavior
56h	DIGOUT_STATUS	R	Current status

The table below summarizes the SVID commands supported by TPS544C26.Refer to the Intel documentation for more detailed description of the individual command functionality.

表 7-20. Supported SVID Command

Command Code	Command	Supported by TPS544C26
01h	SetVID_Fast	Yes
02h	SetVID_Slow	Yes
03h	SetVID_Decay	Yes
04h	SetPS	Yes
05h	SetRegAddr	Yes
06h	SetRegData	Yes
07h	GetReg	Yes
09h	SetWP	Yes

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7.6 Register Maps

7.6.1 (01h) OPERATION

CMD Address	01h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	No
Updates:	On-the-fly

The OPERATION command is used to enable or disable power conversion.

Return to Supported I2C and Default Values.

図 7-2. (01h) OPERATION Register Map

7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R
ON_OFF	Reserved						

LEGEND: R/W = Read/Write; R = Read only

表 7-21. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	ON_OFF	R/W	0b	Enable/disable power conversion. Note that there can be several other requirements that must be satisfied before the power conversion can begin (for example, input voltages above UVLO thresholds). 0b: Disable power conversion. 1b: Enable power conversion.
6:0	Reserved	R	0000000b	Not used and always set to 0.

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7.6.2 (02h) ON_OFF_CONFIG

Register Address	02h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The ON_OFF_CONFIG command configures the combination of enable pin input and serial bus commands needed to enable/disable power conversion. This includes how the unit responds when power is applied to PVIN.

Return to Supported I2C and Default Values.

図 7-3. (02h) ON_OFF_CONFIG Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R	R	R	R	R
ON_OFF_CONFIG			Reserved				

LEGEND: R/W = Read/Write; R = Read only

表 7-22. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:5	ON_OFF_CONFIG	R/W	NVM	These bits determine the on-off mechanism as follow: 000b: Power conversion is always ON 001b: Turn power conversion ON/OFF by I2C Operation Command only 010b: Turn power conversion ON/OFF by EN pin only 011b: The power conversion is not turned ON until commanded by the EN pin and OPERATION command. The power conversion can be turned OFF either commanded by the EN pin or OPERATION command 100b to 111b: Reserved. The device always acknowledges a write with this value but does not change the operation state.
4:0	Reserved	R	00000b	Not used and always set to 0.

Attempts to write ON_OFF_CONFIG to any value other than those explicitly listed above will be considered invalid/unsupported data and cause the TPS544C26 to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

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7.6.3 (03h) CLEAR_FAULTS

CMD Address	03h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	On-the-fly

CLEAR_FAULTS is a command used to clear any fault bits that have been set. CLEAR_FAULTS is a write-only command with no data. Writing a "1" into bit[0] of this command clears all bits in all status registers. The bit clears itself after the write.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately set again.

Return to Supported I²C and Default Values.

図 7-4. (03h) CLEAR_FAULTS Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Reserved							CLEAR_FAULTS

LEGEND: R/W = Read/Write; R = Read only

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7.6.4 (15h) STORE_USER_ALL

CMD Address	15h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The STORE_USER_ALL command instructs the TPS544C26 device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store Memory. Any items in Operating Memory that do not have matching locations in the User Store Memory are ignored. Writing a "1" into bit[0] of this command executes the store operation. The bit clears itself after the write.

User must wait for at least 150 msec from executing this command before power can be turned off to make sure a successful write to NVM is executed. NVM store operation is not recommended while the output is enabled, although the user is not explicitly prevented from doing so, as interruption can result in a corrupted NVM. I^2C commands issued during this time will be ignored. Following issuance of NVM store operations, TI recommends disabling regulation and waiting a minimum of 125 ms before continuing.

Return to Supported I^2C and Default Values.

図 7-5. (15h) STORE_USER_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Reserved							STORE

LEGEND: R/W = Read/Write; R = Read only

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7.6.5 (16h) RESTORE_USER_ALL

CMD Address	16h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	Conversion Disable: on-the-fly. Conversion Enable: hardware update blocked

The RESTORE_USER_ALL command instructs the the TPS544C26 device to copy the entire contents of the non-volatile User Store Memory to the matching locations in the Operating Memory. Any items in Operating Memory that do not have matching locations in the User Store Memory are ignored (for example the STATUS registers). This operation overwrite any value set through a pin detection after the last power-cycle, such as the I²C address set through the I²C_ADDR pin.

Writing a "1" into bit[0] of this command executes the restore operation. When acknowledged, the I²C serial interface is disabled while the restore takes place and all frames will be NACKed during that time. The bit clears itself after the write.

注

Using the RESTORE_USER_ALL command while the SW switching is enabled is not allowed, meaning a NACK response is provided by the device. RESTORE_USER_ALL command can be executed after the SW switching is disabled.

Return to Supported I²C and Default Values.

図 7-6. (16h) RESTORE_USER_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Reserved							RESTORE

LEGEND: R/W = Read/Write; R = Read only

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7.6.6 (33h) FREQUENCY_SWITCH

CMD Address	33h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

FREQUENCY_SWITCH sets the switching frequency of the active device.

Return to Supported I2C and Default Values.

図 7-7. (33h) FREQUENCY_SWITCH Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						SEL_FSW	

LEGEND: R/W = Read/Write; R = Read only

表 7-23. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	SEL_FSW	R/W	NVM	00b: switching frequency is set to 0.6 MHz 01b: switching frequency is set to 0.8 MHz 10b: switching frequency is set to 1.0 MHz 11b: switching frequency is set to 1.2 MHz

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7.6.7 (35h) VIN_ON

CMD Address	35h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VIN_ON command sets the value of the PVIN input voltage, in Volts, at which the unit starts power conversion.

Return to Supported I²C and Default Values.

図 7-8. (35h) VIN_ON Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						PVIN_ON	

LEGEND: R/W = Read/Write; R = Read only

表 7-24. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	PVIN_ON	R/W	NVM	00b: ON threshold is PVIN = 10 V. 01b: ON threshold is PVIN = 9 V 10b: ON threshold is PVIN = 8 V 11b: ON threshold is determined by both PVIN and VCC conditions. When this option is selected, both PVIN > 2.55 V and VCC > 3.8 V conditions have to be satisfied to enable the power conversion.

Note that the PVIN_UVF condition in (7Ch) STATUS_INPUT register is masked until the sensed input voltage exceeds the VIN_ON threshold for the first time following a power-on reset. The EN pin toggles and NVM store or restore operations do not reset this masking.

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7.6.8 (36h) VIN_OFF

CMD Address	36h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VIN_OFF command sets the value of the PVIN input voltage, in Volts, at which the unit must stop power conversion. If the power conversion enable conditions as defined by (02h) ON_OFF_CONFIG are met and PVIN is less than the selected VIN_OFF threshold, the power conversion turns off and the PVIN_UVF bit in (7Ch) STATUS_INPUT is set.

Return to Supported I²C and Default Values.

図 7-9. (36h) VIN_OFF Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					PVIN_OFF		

LEGEND: R/W = Read/Write; R = Read only

表 7-25. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	PVIN_OFF	R/W	NVM	000b: OFF threshold is PVIN = 4.2 V 001b: OFF threshold is PVIN = 9.5 V 010b: OFF threshold is PVIN = 8.5 V 011b: OFF threshold is PVIN = 7.5 V 100b: OFF threshold is PVIN = 6.5 V 101b: OFF threshold is PVIN = 5.5 V 110b: OFF threshold is PVIN = 4.2 V 111b: OFF threshold is determined by both PVIN and VDRV conditions. When this option is selected, either PVIN ≤ 2.3 V or VDRV ≤ 3.4 V disables the power conversion.

While it is possible to set (36h) VIN_OFF threshold greater than (35h) VIN_ON threshold, it is not advisable and can produce rapid enabling and disabling of conversion and undesirable operation. Please set (35h) VIN_ON threshold always greater than (36h) VIN_OFF threshold.

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7.6.9 (40h) VOUT_OV_FAULT_LIMIT

CMD Address	40h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output overvoltage fault. SEL_OVF bits set an overvoltage fault threshold relative to the current VOUT setting that is commanded by either SVID SetVID command or I^{2}C (A6h) VOUT_CMD. The VOUT Tracking OVF function is activated after the soft-start ramp completes.

Following an overvoltage fault condition, the device responds according to (41h) VOUT_OV_FAULT_RESP. Due to the lack of an I^{2}C alert pin, the TPS544C26 device does not have a way to notify the host.

Return to Supported I^{2}C and Default Values.

図 7-10. (40h) VOUT_OV_FAULT_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						SEL_OVF	

LEGEND: R/W = Read/Write; R = Read only

表 7-26. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	SEL_OVF	R/W	NVM	Sets the overvoltage fault threshold. 00b: VOUT Tracking OVF threshold = +100 mV 01b: VOUT Tracking OVF threshold = +150 mV 10b: VOUT Tracking OVF threshold = +200 mV 11b: VOUT Tracking OVF threshold = +300 mV

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7.6.10 (41h) VOUT_OV_FAULT_RESPONSE

CMD Address	41h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. Upon triggering the tracking overvoltage fault (a.k.a VOUT Tracking OVF), the TPS544C26 device responds according to the *RESTART* bit in this register, and the following actions are taken:

- Set the OVF bit in the (7Ah) STATUS_VOUT register.
- Enter continuous Negative Overcurrent (NOC) operation immediately, and the delay from the VOUT Tracking OVF detection circuit is minimized (less than 1 µs).
- Due to the lack of an I^2C alert pin, the TPS544C26 device does not have a way to notify the host.

The selected Tracking OVF response in this VOUT_OV_FAULT_RESP register does not affect the response for a Fixed OVF event.

Return to Supported I^2C and Default Values.

図 7-11. (41h) VOUT_OV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R	R	R
Reserved				RESTART	Reserved		

LEGEND: R/W = Read/Write; R = Read only

表 7-27. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3	RESTART	R/W	NVM	VOUT Tracking OVF response selection 0b: Latch-off after the fault. A VCC power cycle or EN toggle can restart the power conversion. 1b: Automatically restart after a delay of 56 ms, without limitation on the number of restart attempts.
2:0	Reserved	R	000b	Not used and always set to 0.

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7.6.11 (42h) VOUT_OV_WARN_LIMIT

CMD Address	42h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output voltage high warning. This value is typically less than the output overvoltage fault threshold. The SEL_OVW bits set an overvoltage warning threshold relative to the current VOUT setting that is commanded by either SVID SetVID command or I²C (A6h) VOUT_CMD.

When the sensed output voltage exceeds the VOUT Tracking OVW threshold, the OVW bit in the (7Ah) STATUS_VOUT register is set. Due to the lack of an I²C alert pin, the TPS544C26 device does not have a way to notify the host.

Return to Supported I²C and Default Values.

図 7-12. (42h) VOUT_OV_WARN_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						SEL_OVW	

LEGEND: R/W = Read/Write; R = Read only

表 7-28. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	SEL_OVW	R/W	NVM	Sets the overvoltage warning threshold. 00b: VOUT Tracking OVW threshold = +100 mV 01b: VOUT Tracking OVW threshold = +150 mV 10b: VOUT Tracking OVW threshold = +200 mV 11b: VOUT Tracking OVW threshold = +300 mV

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7.6.12 (43h) VOUT_UV_WARN_LIMIT

CMD Address	43h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output voltage low warning. This value is typically less negative than the output undervoltage fault threshold. The SEL_UVW bits set an undervoltage warning threshold relative to the current VOUT setting that is commanded by either SVID SetVID command or I²C (A6h) VOUT_CMD.

When the sensed output voltage falls below the VOUT Tracking UVW threshold, the UVW bit in the (7Ah) STATUS_VOUT register is set. Due to the lack of an I²C alert pin, the TPS544C26 device does not have a way to notify the host.

Return to Supported I²C and Default Values.

図 7-13. (43h) VOUT_UV_WARN_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						SEL_UVW	

LEGEND: R/W = Read/Write; R = Read only

表 7-29. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	SEL_UVW	R/W	NVM	Sets the undervoltage warning threshold. 00b: VOUT Tracking UVW threshold = −100 mV 01b: VOUT Tracking UVW threshold = −150 mV 10b: VOUT Tracking UVW threshold = −200 mV 11b: VOUT Tracking UVW threshold = −300 mV

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7.6.13 (44h) VOUT_UV_FAULT_LIMIT

CMD Address	44h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output undervoltage fault. The SEL_UVF bits set an undervoltage fault threshold relative to the current VOUT setting that is commanded by either SVID SetVID command or I^{2}C (A6h) VOUT_CMD. The VOUT Tracking UVF function is activated after the soft-start ramp completes.

When the undervoltage fault condition is triggered, the device responds according to (45h) VOUT_UV_FAULT_RESPONSE. Due to the lack of an I^{2}C alert pin, the TPS544C26 device does not have a way to notify the host.

Return to Supported I^{2}C and Default Values.

図 7-14. (44h) VOUT_UV_FAULT_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						SEL_UVF	

LEGEND: R/W = Read/Write; R = Read only

表 7-30. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	SEL_UVF	R/W	NVM	Sets the undervoltage fault threshold. 00b: VOUT Tracking UVF threshold = −150 mV 01b: VOUT Tracking UVF threshold = −200 mV 10b: VOUT Tracking UVF threshold = −200 mV 11b: VOUT Tracking UVF threshold = −300 mV

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7.6.14 (45h) VOUT_UV_FAULT_RESPONSE

CMD Address	45h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. Upon triggering the tracking undervoltage fault (a.k.a VOUT Tracking UVF), the TPS544C26 device responds according to the *RESTART* bit in this register, and the following actions are taken:

- Set the UVF bit in the (7Ah) STATUS_VOUT register.
- Start the UVF Response Delay selected in this register. During the UVF Response Delay, if the output voltage (VOSNS − GOSNS) rises above the UVF threshold, thus not qualified for a UVF event, the UVF response delay timer resets to zero. When the VOUT drops below the UVF threshold again, the UVF response delay timer re-starts from zero.
- Due to the lack of an I^2C alert pin, the TPS544C26 device does not have a way to notify the host.

Return to Supported I^2C and Default Values.

図 7-15. (45h) VOUT_UV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R	R/W	R/W
Reserved				RESTART	Reserved	RESPONSE_DELAY	

LEGEND: R/W = Read/Write; R = Read only

表 7-31. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3	RESTART	R/W	NVM	VOUT Tracking UVF response selection 0b: Latch-off after the fault. A VCC power cycle or EN toggle can restart the power conversion. 1b: Automatically restart after a delay of 56 ms, without limitation on the number of restart attempts.
2	Reserved	R	0b	Not used and always set to 0.
1:0	RESPONSE_DELAY	R/W	NVM	VOUT Tracking UVF Response Delay selection 00b: UVF Response Delay = 2 µs 00b: UVF Response Delay = 16 µs 00b: UVF Response Delay = 64 µs 00b: UVF Response Delay = 256 µs

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7.6.15 (46h) IOUT_OC_FAULT_LIMIT

CMD Address	46h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM or Pin Detection
Updates:	On-the-fly

The IOUT_OC_FAULT_LIMIT command sets the value of the output current that causes the overcurrent detector to indicate an overcurrent fault condition. The thresholds selected here are compared to the sensed low-side valley current. See Overcurrent Limit and Low-side Current Sense for more details.

Return to Supported I2C and Default Values.

図 7-16. (46h) IOUT_OC_FAULT_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

表 7-32. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3:0	SEL_OCL	R/W	NVM	These bits select the I_{OUT} valley current limiting threshold.

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7.6.16 (4Fh) OT_FAULT_LIMIT

CMD Address	4Fh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The OT_FAULT_LIMIT command sets the temperature of the unit, at which, it indicates an overtemperature fault condition. The unit of this command is degrees Celsius. This feature utilizes a digital comparator that compares the output of the IC TEMPERATURE telemetry to the fault threshold selected in this register.

The device response to an overtemperature event is described in (50h) OT_FAULT_RESPONSE.

Return to Supported I²C and Default Values.

図 7-17. (4Fh) OT_FAULT_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					SEL_OTF		

LEGEND: R/W = Read/Write; R = Read only

表 7-33. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	SEL_OTF	R/W	NVM	These bits select the OT fault threshold which is compared with the output of the IC TEMP telemetry. 000b: OTF threshold = 115 °C 001b: OTF threshold = 120 °C 010b: OTF threshold = 125 °C 011b: OTF threshold = 130 °C 100b: OTF threshold = 135 °C 101b: OTF threshold = 140 °C 110b: OTF threshold = 145 °C 111b: OTF threshold = 150 °C

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7.6.17 (50h) OT_FAULT_RESPONSE

CMD Address	50h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The (50) OT_FAULT_RESPONSE command instructs the device on what action to take in response to an overtemperature fault. Upon triggering the overtemperature fault, the device responds per the *RESTART* bit in this register, and sets the *OTF_PROG* bit in the (7Dh) STATUS_TEMPERATURE register. Due to the lack of an I^{2}C alert pin, the device does not have a way to notify the host.

Return to Supported I^{2}C and Default Values.

図 7-18. (50h) OT_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R	R	R
Reserved				RESTART	Reserved		

LEGEND: R/W = Read/Write; R = Read only

表 7-34. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3	RESTART	R/W	NVM	This bit selects the response to a programmable OT fault condition 0b: Latch-off after the fault. A VCC power cycle or EN toggle can restart the power conversion. 1b: Automatically restart after a delay of 56 ms, without limitation on the number of restart attempts.
2:0	Reserved	R	000b	Not used and always set to 0.

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7.6.18 (51h) OT_WARN_LIMIT

CMD Address	51h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The OT_WARN_LIMIT command sets the temperature of the unit, at which, it indicates an overtemperature warning alarm. The unit of this command is degrees Celsius. This feature utilizes a digital comparator that compares the output of the IC TEMPERATURE telemetry to the warning threshold selected in this register.

Upon triggering the overtemperature fault, the device sets the *OTW_PROG* bit in the (7Dh) STATUS_TEMPERATURE register. Due to the lack of an I²C alert pin, the TPS544C26 device does not have a way to notify the host.

Return to Supported I²C and Default Values.

図 7-19. (51h) OT_WARN_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					SEL_OTW		

LEGEND: R/W = Read/Write; R = Read only

表 7-35. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	SEL_OTW	R/W	NVM	These bits select the OT warning threshold which is compared with the output of the IC TEMP telemetry. 000b: OTW threshold = 85 °C 001b: OTW threshold = 95 °C 010b: OTW threshold = 100 °C 011b: OTW threshold = 105 °C 100b: OTW threshold = 110 °C 101b: OTW threshold = 115 °C 110b: OTW threshold = 125 °C 111b: OTW threshold = 135 °C

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7.6.19 (55h) VIN_OV_FAULT_LIMIT

CMD Address	55h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VIN_OV_FAULT_LIMIT command sets the PVIN voltage, in volts, when a VIN_OV_FAULT is declared. The response to a detected VIN_OV_FAULT is latch-off always. (55h) VIN_OV_FAULT_LIMIT is typically used to stop switching in the event of excessive input voltage, which can result in over-stress damage to the power FETs due to ringing on the SW node. Upon triggering the PVIN overvoltage fault, the device sets the PVIN_OVF bit in the (7C) STATUS_INPUT register.

Due to the lack of an I^2C alert pin, the device does not have a way to notify the host.

Return to Supported I^2C and Default Values.

図 7-20. (55h) VIN_OV_FAULT_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R/W
							PVIN_OVF

LEGEND: R/W = Read/Write; R = Read only

表 7-36. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:1	Reserved	R	0000000b	Not used and always set to 0.
0	PVIN_OVF	R/W	NVM	This bit selects the PVIN_OVF rising threshold. The falling threshold is always 13.5 V. 0b: PVIN_OVF rising threshold = 16.5 V 1b: PVIN_OVF rising threshold = 18.5 V

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7.6.20 (60h) TON_DELAY

CMD Address	60h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received (as programmed by the (02h) ON_OFF_CONFIG command) until the output voltage starts to rise.

Return to Supported I2C and Default Values.

図 7-21. (60h) TON_DELAY Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						TON_DELAY	

LEGEND: R/W = Read/Write; R = Read only

表 7-37. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	TON_DELAY	R/W	NVM	These bits select the turn-on delay options before enabling the SW switching. 00b: TON_DELAY time = 0.5 ms 01b: TON_DELAY time = 1 ms 10b: TON_DELAY time = 1.5 ms 11b: TON_DELAY time = 2 ms

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7.6.21 (61h) TON_RISE

CMD Address	61h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM or Pin Detection
Updates:	On-the-fly

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band, which effectively sets the slew rate of the reference DAC during the soft-start period. Note that the soft-start time is equal to TON_RISE selection only when the output voltage is controlled by SVID bus. The soft-start time varies from the TON_RISE selection when I^{2}C_OFFSET is involved or (A6h) VOUT_CMD is used for boot up. See section Startup and 表 7-7 for more details.

Return to Supported I^{2}C and Default Values.

図 7-22. (61h) TON_RISE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					TON_RISE		

LEGEND: R/W = Read/Write; R = Read only

表 7-38. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	TON_RISE	R/W	NVM	These bits select the soft-start time options. 000b: TON_RISE time = 1 ms 001b: TON_RISE time = 2 ms 010b: TON_RISE time = 4 ms 011b: TON_RISE time = 8 ms 100b to 111b: TON_RISE time = 16 ms

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7.6.22 (64h) TOFF_DELAY

CMD Address	64h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the (02h) ON_OFF_CONFIG command) until the device starts the soft-stop operation. When the soft-stop feature is disabled through the *EN_SOFT_STOP* bit in (A0h) SYS_CFG_USER1 register, the TOFF_DELAY time is automatically set to 0 ms, thus the device stops switching (tri-state power FETs) immediately when a stop condition is received.

Return to Supported I²C and Default Values.

図 7-23. (64h) TOFF_DELAY Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						TOFF_DELAY	

LEGEND: R/W = Read/Write; R = Read only

表 7-39. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	TOFF_DELAY	R/W	NVM	These bits select the turn-off delay options before starting soft-stop operation. When soft-stop feature is disabled the TOFF_DELAY is automatically set to 0 ms. 00b: TOFF_DELAY time = 0 ms 01b: TOFF_DELAY time = 1 ms 10b: TOFF_DELAY time = 1.5 ms 11b: TOFF_DELAY time = 2 ms

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7.6.23 (65h) TOFF_FALL

CMD Address	65h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the reference DAC is commanded to 0 mV. This command is used with the TPS544C26 device whose output can sink enough current to cause the output voltage to decrease at a controlled rate, which effectively sets the slew rate of the reference DAC during the soft-off period. The VOUT fall time is actually not equal to TOFF_FALL value since the device stops SW switching once the output voltage is discharged to 200 mV, and the fall time is more for setting the reference DAC slew rate. See Shutdown and 表 7-8 for more details.

Return to Supported I2C and Default Values.

図 7-24. (65h) TOFF_FALL Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R/W	R/W
Reserved						TOFF_FALL	

LEGEND: R/W = Read/Write; R = Read only

表 7-40. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:2	Reserved	R	000000b	Not used and always set to 0.
1:0	TOFF_FALL	R/W	NVM	These bits select the soft-stop time option before disabling the SW switching and tri-state the power FETs. 00b: TOFF_FALL time = 0.5 ms 01b: TOFF_FALL time = 1 ms 10b: TOFF_FALL time = 2 ms 11b: TOFF_FALL time = 4 ms

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7.6.24 (6Bh) PIN_OP_WARN_LIMIT

CMD Address	6Bh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high. The PIN_MAX value which is the maximum input power threshold is always the same as PIN_OP_WARN_LIMIT value. This feature utilizes a digital comparator that compares the output of the PIN telemetry to the fault threshold selected in this register.

In response to the PIN_OP_WARN_LIMIT being exceeded, the device sets the PIN_OPW bit in the (7Ch) STATUS_INPUT register.

Return to Supported I²C and Default Values.

図 7-25. (6Bh) PIN_OP_WARN_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					PIN_OPW		

LEGEND: R/W = Read/Write; R = Read only

表 7-41. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	PIN_OPW	R/W	NVM	These bits select the PIN_OPW and PIN_MAX thresholds. 000b: PIN_OPW = PIN_MAX = 510 W 001b: PIN_OPW = PIN_MAX = 480 W 010b: PIN_OPW = PIN_MAX = 420 W 011b: PIN_OPW = PIN_MAX = 360 W 100b: PIN_OPW = PIN_MAX = 300 W 101b: PIN_OPW = PIN_MAX = 240 W 110b: PIN_OPW = PIN_MAX = 180 W 111b: PIN_OPW = PIN_MAX = 120 W

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7.6.25 (7Ah) STATUS_VOUT

CMD Address	7Ah
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Updates:	On-the-fly

The STATUS_VOUT command returns one data byte with contents as follows. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing a "1" to the (7Ah) STATUS_VOUT register in their position. If a fault condition is still present when the corresponding bit is cleared, the fault bit is immediately set again.

Return to Supported I2C and Default Values.

図 7-26. (7Ah) STATUS_VOUT Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R	R	R	R
VOUT_OVF	VOUT_OVW	VOUT_UVW	VOUT_UVF	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

表 7-42. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	VOUT_ OVF	R/W	0b	0b: Latched flag indicating a VOUT OV fault has *not* occurred. 1b: Latched flag indicating either a VOUT Fixed OV fault or a VOUT Tracking OV fault has occurred.
6	VOUT_ OVW	R/W	0b	0b: Latched flag indicating a VOUT Tracking OV warn has *not* occurred. 1b: Latched flag indicating a VOUT Tracking OV warn has occurred.
5	VOUT_ UVW	R/W	0b	0b: Latched flag indicating a VOUT Tracking UV warn has *not* occurred. 1b: Latched flag indicating a VOUT Tracking UV warn has occurred.
4	VOUT_ UVF	R/W	0b	0b: Latched flag indicating a VOUT Tracking UV fault has *not* occurred. 1b: Latched flag indicating a VOUT Tracking UV fault has occurred.
3:0	Not supported	R	0000b	Not supported and always set to 0.

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7.6.26 (7Bh) STATUS_IOUT

CMD Address	7Bh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Updates:	On-the-fly

The STATUS_IOUT command returns one data byte with contents as follows. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing a "1" to the (7Bh) STATUS_IOUT register in their position. If a fault condition is still present when the corresponding bit is cleared, the fault bit is immediately set again.

Return to Supported I2C and Default Values.

図 7-27. (7Bh) STATUS_IOUT Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R	R	R	R	R	R
IOUT_OCL	IOUT_OCUV	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

表 7-43. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IOUT_ OCL	R	0b	0b: Latched flag indicating low-side valley OC limit has *not* occurred. 1b: Latched flag indicating low-side valley OC limit has occurred.
6	IOUT_OCUV	R/W	0b	0b: Latched flag indicating both low-side valley OC limit and VOUT Tracking UV fault have *not* occurred. 1b: Latched flag indicating both low-side valley OC limit and VOUT Tracking UV fault have occurred.
5:0	Not supported	R	000000b	Not supported and always set to 0.

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7.6.27 (7Ch) STATUS_INPUT

CMD Address	7Ch
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Updates:	On-the-fly

The STATUS_INPUT command returns one data byte with contents as follows. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing a "1" to the (7Ch) STATUS_INPUT register in their position. If a fault condition is still present when the corresponding bit is cleared, the fault bit is immediately set again.

Return to Supported I2C and Default Values.

図 7-28. (7Ch) STATUS_INPUT Register Map

7	6	5	4	3	2	1	0
R/W	R	R	R/W	R	R	R	R/W
PVIN_OVF	0	0	PVIN_UVF	0	0	0	PIN_OPW

LEGEND: R/W = Read/Write; R = Read only

表 7-44. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	PVIN_OVF	R/W	0b	0b: Latched flag indicating a PVIN OV fault has *not* occurred. 1b: Latched flag indicating a PVIN OV fault has occurred.
6:5	Not supported	R	00b	Not supported and always set to 0.
4	PVIN_UVF	R/W	0b	0b: Latched flag indicating a PVIN UV fault has *not* occurred. 1b: Latched flag indicating a PVIN UV fault has occurred.
3:1	Not supported	R	000b	Not supported and always set to 0.
0	PIN_ OPW	R/W	0b	0b: Latched flag indicating a PIN OP event has *not* occurred. 1b: Latched flag indicating a PIN OP event has occurred.

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7.6.28 (7Dh) STATUS_TEMPERATURE

CMD Address	7Dh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Updates:	On-the-fly

The STATUS_TEMPERATURE command returns one data byte with contents as follows. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing a "1" to the (7Dh) STATUS_TEMPERATURE register in their position. If a fault condition is still present when the corresponding bit is cleared, the fault bit is immediately set again.

Return to Supported I2C and Default Values.

図 7-29. (7Dh) STATUS_TEMPERATURE Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R	R	R	R	R	R
OTF_PROG	OTW_PROG	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only

表 7-45. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	OTF_PROG	R/W	0b	0b: Latched flag indicating an OT fault has *not* occurred. 1b: Latched flag indicating an OT fault has occurred on the Controller die. Note: A digital comparator on the Controller die is utilized to compare the output of the IC TEMP telemetry to the fault threshold selected in (4Fh) OT_FAULT_LIMIT register. This bit has no relationship with the overtemperature detection implemented on the Power Stage (PS) die.
6	OTW_PROG	R/W	0b	0b: Latched flag indicating an OT warn has *not* occurred. 1b: Latched flag indicating an OT warn has occurred on the Controller die. Note: A digital comparator on the Controller die is utilized to compare the output of the IC TEMP telemetry to the warning threshold selected in (51h) OT_WARN_LIMIT register. This bit has no relationship with the overtemperature detection implemented on the Power Stage (PS) die.
5:0	Not supported	R	000000b	Not supported and always set to 0.

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7.6.29 (80h) STATUS_MFR_SPECIFIC

CMD Address	80h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Updates:	On-the-fly

The STATUS_MFR_SPECIFIC command returns one data byte with contents as follows. All supported bits, except *DCM* bit, can be cleared either by CLEAR_FAULTS, or individually by writing a "1" to the (80h) STATUS_MFR_SPECIFIC register in their position. If a fault condition is still present when the corresponding bit is cleared, the fault bit is immediately set again.

Bit[7] DCM is a LIVE bit updated by the analog detection circuit, which continuously monitors the output of the zero-cross comparator. During CCM operation, this bit shows a value of "0". Once the device enters DCM operation this bit is set showing a value of "1".

Return to Supported I²C and Default Values.

図 7-30. (80h) STATUS_MFR_SPECIFIC Register Map

7	6	5	4	3	2	1	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DCM	OTF_ANALOG	PS_FAULT	PS_COMM_WRN	RESTORE_ERR	NOC	PS_OTF_ANALOG	VDRV_UVF

LEGEND: R/W = Read/Write; R = Read only

表 7-46. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	DCM	R/W	0b	A LIVE bit updated by the analog detection circuit, which continuously monitors the output of the zero-cross comparator. 0b: Un-latched flag indicating the the device is under CCM operation. 1b: Un-latched flag indicating the the device is under DCM operation.
6	OTF_ANALOG	R/W	0b	0b: Latched flag indicating an OT fault has *not* occurred. 1b: Latched flag indicating an OT fault has occurred on the Controller die. Note: An analog comparator on the Controller die is utilized to compare the output of the IC temperature sensing circuit to a fixed threshold (166 °C typical). This bit has no relationship with the overtemperature detection implemented on the Power Stage (PS) die.
5	PS_FAULT	R/W	0b	0b: Latched flag indicating *no* fault has occurred on Power Stage (PS) die. 1b: Latched flag indicating at least one fault has occurred on the PS die.
4	PS_COMM_WRN	R/W	0b	0b: Latched flag indicating *no* error has occurred for the communications between the Controller and PS die. 1b: Latched flag indicating a communications error has occurred between the Controller and PS die. Note: A VCC reset (power cycle) is recommended when this bit is set.
3	RESTORE_ERR	R/W	0b:	0b: Latched flag indicating *no* error has occurred during the initial restore from NVM operation (copy the entire contents of the non-volatile User Store Memory to the matching locations in the Operating Memory). 1b: Latched flag indicating an error has occurred during the initial restore from NVM operation. Note: The restore operation mentioned here refers to the one-time restore operation during the initial power-on. This bit doesn't validate the RESTORE_USER_ALL operation. A VCC reset (power cycle) is recommended when this bit is set.

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表 7-46. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
2	NOC	R/W	0b	0b: Latched flag indicating *no* NOC operation has occurred. 1b: Latched flag indicating at least one cycle of NOC operation has occurred.
1	PS_OTF_ANALOG	R/W	0b	0b: Un-latched flag indicating an OT fault has *not* occurred. 1b: Un-latched flag indicating an OT fault has occurred on the Power Stage (PS) die. Note: An analog comparator on the Power Stage die is utilized to compare the output of the IC temperature sensing circuit to a fixed threshold (166 °C typical). This bit has no relationship with the overtemperature detection implemented on the Controller die.
0	VDRV_UVF	R/W	0b	0b: Latched flag indicating a VDRV UV fault has *not* occurred. 1b: Latched flag indicating a VDRV UV fault has occurred.

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7.6.30 (88h) READ_VIN

CMD Address	88h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Update Rate:	190 µs
Supported Range:	8 V – 16 V

The READ_VIN command returns input voltage in Volts. See Telemetry for more details.

Return to Supported I2C and Default Values.

図 7-31. (88h) READ_VIN Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VIN							

LEGEND: R/W = Read/Write; R = Read only

表 7-47. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	READ_VIN_	R	Input voltage	Input voltage (on pin 4 VINSENM) reading. See Telemetry for more details.

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7.6.31 (89h) READ_IIN

CMD Address	89h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Update Rate:	95 µs
Supported Range:	0 A to 40 A (if PIN_SENSE_RES = 05h)

The READ_IIN command returns the measured input current in Amperes. See Telemetry for more details.

Return to Supported I2C and Default Values.

図 7-32. (89h) READ_IIN Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IIN							

LEGEND: R/W = Read/Write; R = Read only

表 7-48. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	READ_IIN	R	Current Status	Input current (over the external sensing resistor) reading. See Telemetry for more details.

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7.6.32 (8Bh) READ_VOUT

CMD Address	8Bh
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Update Rate:	190 µs
Supported Range	VOUT 5 mV step: up to 1.6 V VOUT 10 mV step: up to 3.2 V

The READ_VOUT command returns the actual, measured output voltage (VOSNS−GOSNS) in Volts. See Telemetry for more details.

Return to Supported I2C and Default Values.

図 7-33. (8Bh) READ_VOUT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VOUT							

LEGEND: R/W = Read/Write; R = Read only

表 7-49. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	READ_VOUT	R	Current Status	Output voltage reading. See Telemetry for more details.

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7.6.33 (8Ch) READ_IOUT

CMD Address	8Ch
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Update Rate:	95 µs
Supported Range:	0 A to 40 A (if ICC_MAX = 40 A)

The READ_IOUT command returns the measured output current in Amperes. See Telemetry for more details.

Return to Supported I2C and Default Values.

図 7-34. (8Ch) READ_IOUT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IOUT							

LEGEND: R/W = Read/Write; R = Read only

表 7-50. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	READ_IOUT	R	Current Status	Output current reading. See Telemetry for more details.

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7.6.34 (8Dh) READ_TEMPERATURE_1

CMD Address	8Dh
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Update Rate:	190 µs
Supported Range:	–40°C to 150°C

The READ_TEMPERATURE_1 command returns the Controller die temperature in degrees Celsius. See Telemetry for more details.

Return to Supported I2C and Default Values.

図 7-35. (8Dh) READ_TEMPERATURE_1 Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_TEMPERATURE_1							

LEGEND: R/W = Read/Write; R = Read only

表 7-51. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	READ_TEMPERATURE_1	R	Current Status	Controller die temperture reading. See Telemetry for more details.

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7.6.35 (97h) READ_PIN

CMD Address	97h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Update Rate:	95 µs
Supported Range:	0 W to 510 W (if PIN_OPW = 510 W)

The READ_PIN command returns the measured input power, in watts. See Telemetry for more details.

Return to Supported I2C and Default Values.

図 7-36. (97h) READ_PIN Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_PIN							

LEGEND: R/W = Read/Write; R = Read only

表 7-52. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	READ_PIN	R	Current Status	Input power reading. See Telemetry for more details.

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7.6.36 (A0h) SYS_CFG_USER1

Register Address	A0h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly. Note that many of the fields in this register either require the output to be disabled to take effect or require (15h) STORE_USER_ALL then VCC reset.

The SYS_CFG_USER1 command contains miscellaneous bits for the device configuration.

Return to Supported I²C and Default Values.

図 7-37. (A0h) SYS_CFG_USER1 Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FCCM	VOUT_CTRL		EN_SOFT_STOP	VRRDY_DELAY		OVRD_SVID_ADDR	OVRD_I2C_ADDR

LEGEND: R/W = Read/Write; R = Read only

表 7-53. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	FCCM(1)	R/W	NVM	0b: Discontinuous conduction mode (DCM) operation at light loads. 1b: Forced continuous conduction mode (FCCM) operation at light loads.
6:5	VOUT_CTRL(1)	R/W	NVM	00b: Output voltage and offset are programmed through the SVID interface. Writes to I²C register (A6h) VOUT_CMD are always accepted but do not change the output voltage. Writes to (A8h) I²C_OFFST are always NACKed. 01b: Output voltage is programmed through the SVID interface and offset is programmed through the I²C interface (A8h) I²C_OFFST. Writes to SVID (33h) OFFSET register are always accepted but do not change the output voltage. 10b: Output voltage and offset are controlled via I²C register (A6h) VOUT_CMD and (A8h) I2C_OFFST, respectively. Writes to SVID (33h) OFFSET register or SetVID commands are always accepted but do not change the output voltage. 11b: Same as 10b.
4	EN_SOFT_STOP(1)	R/W	NVM	0b: The SW switching is turned off immediately (ignores TOFF_FALL (soft-stop) and TOFF_DELAY is automatically set to 0 ms). 1b: The SW switching is turned off after going through TOFF_DELAY and TOFF_FALL (soft-stop).
3:2	VRRDY_DELAY(1)	R/W	NVM	Program the rising edge delay time from soft start complete to VRRDY pin going high: 00b: 0 ms 01b: 0.5 ms 10b: 1.0 ms 11b: 2.0 ms
1	OVRD_SVID_ADDR(2)	R/W	NVM	This bit is reserved for future usage.
0	OVRD_I2C_ADDR(2)	R/W	NVM	0b: I²C address is determined by pin-strapping on the I²C_ADDR pin. 1b: I²C address is determined by NVM backup.

(1) Writes are always accepted and the data is updated; however, in order for this bit to take effect, the device's swtiching must be disabled, including the (02h) ON_OFF_CONFIG register cannot be set to "Always on" behavior.

(2) Writes are always accepted and the data is updated; however, in order for this bit to take effect, send a (15h) STORE_USER_ALL to store the new value to NVM then reset the VCC.

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7.6.37 (A2h) I²C_ADDR

Register Address	A2h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	Update the I²C_ADDR value, set the OVRD_I2C_ADDR bit, セクション 7.6.4 then VCC reset are all required for the device to respond to a new I²C address.

The I²C_ADDR command reads the I²C device address when the address is determined by pin-strapping. When the *OVRD_I2C_ADDR* bit is set the device address is set by the value written into this register. Update the I²C_ADDR value, set the OVRD_I2C_ADDR bit, execute (15h) STORE_USER_ALL then VCC reset are all required for the device to respond to a new I²C address

Return to Supported I²C and Default Values.

図 7-38. (A2h) I²C_ADDR Register Map

7	6	5	4	3	2	1	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reserved	I²C_ADDR						

LEGEND: R/W = Read/Write; R = Read only

表 7-54. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	Reserved	R	0b	Reserved for TI usage.
6:0	I²C_ADDR	R/W	NVM	These bits set the I²C address. By default, the address is set through the resistor on the I²C_ADDR pin as described in Setting the I²C Address. The I²C address can be changed through these bits together using the OVRD_I2C_ADDR bit. The OVRD_I2C_ADDR bit must be set to "1", stored to NVM and the VCC resets before the TPS544C26 will respond to the programmed new address.

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7.6.38 (A3h) SVID_ADDR

CMD Address	A3h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The SVID_ADDR command sets the SVID address for the device.

Return to Supported I2C and Default Values.

図 7-39. (A3h) SVID_ADDR Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W
Reserved				SVID_ADDR			

LEGEND: R/W = Read/Write; R = Read only

表 7-55. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3:0	SVID_ADDR	R/W	NVM	0000b: SVID address = 00h 0001b: SVID address = 01h 0010b: SVID address = 02h 0011b: SVID address = 03h 0100b: SVID address = 04h 0101b: SVID address = 05h 0110b: SVID address = 06h 0111b: SVID address = 07h 1000b: SVID address = 08h 1001b: SVID address = 09h 1010b: SVID address = 0Ah 1011b: SVID address = 0Bh 1100b: SVID address = 0Ch 1101b: SVID address = 0Dh 1110b: Reserved 1111b: Reserved

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7.6.39 (A4h) IMON_CAL

CMD Address	A4h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IMON_CAL command contains 2 fields (Gain and Offset) for READ_IOUT (IMON) calibration.

Return to Supported I2C and Default Values.

図 7-40. (A4h) IMON_CAL Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IMON_GAIN_CAL				IMON_OFS_CAL			

LEGEND: R/W = Read/Write; R = Read only

表 7-56. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	IMON_GAIN_CAL	R/W	NVM	These bits contains the READ_IOUT (IMON) gain calibration. This field gives flexibility to change the gain of nominal reporting by −3.5% to +4%. 0000b: IMON Gain Adjustment = −3.5% 0001b: IMON Gain Adjustment = −3.0% 0010b: IMON Gain Adjustment = −2.5% 0011b: IMON Gain Adjustment = −2.0% 0100b: IMON Gain Adjustment = −1.5% 0101b: IMON Gain Adjustment = −1.0% 0110b: IMON Gain Adjustment = −0.5% 0111b: IMON Gain Adjustment = −0% 1000b: IMON Gain Adjustment = +0.5% 1001b: IMON Gain Adjustment = +1.0% 1010b: IMON Gain Adjustment = +1.5% 1011b: IMON Gain Adjustment = +2.0% 1100b: IMON Gain Adjustment = +2.5% 1101b: IMON Gain Adjustment = +3.0% 1110b: IMON Gain Adjustment = +3.5% 1111b: IMON Gain Adjustment = +4.0%

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表 7-56. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
3:0	IMON_OFS_CAL	R/W	NVM	These bits contains the READ_IOUT (IMON) offset calibration. This field gives flexibility to change the nominal reporting by −2.0 A to 1.75 A. However, special attention is needed when setting the offset adjustment to a negative value. The calculation from the combination of ADC conversion and calibration register input is not clamped at zero. When the calculated value of (ADC conversion result + calibration offset value) goes negative, the final reporting value rolls over to a large positive value (decreased from the maximum limit). For example, for a case of real I_{OUT} = 0.5 A, IMON offset adjutment = −1.0 A, ICC_MAX = 30 A, the final reporting value is not clamped at 0 A, instread, the reporting value shows +29.5 A. TI suggests using the calibration offset in a way that the calculated value from (ADC conversion result + calibration offset value) never goes negative, especially at minimum load case. 0000b - 0111b: Negative offset adjustment but NOT recommended to use if the minimum load (IOUT) is 0 A. Contact TI for details in case of negative offset adjustment needed. 1000b: IMON Offset Adjustment = 0 A 1001b: IMON Offset Adjustment = +0.25 A 1010b: IMON Offset Adjustment = +0.50 A 1011b: IMON Offset Adjustment = +0.75 A 1100b: IMON Offset Adjustment = +1.00 A 1101b: IMON Offset Adjustment = +1.25 A 1110b: IMON Offset Adjustment = +1.50 A 1111b: IMON Offset Adjustment = +1.75 A

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7.6.40 (A5h) IIN_CAL

CMD Address	A5h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IIN_CAL command contains 2 fields (Gain and Offset) for READ_IIN calibration.

Return to Supported I2C and Default Values.

図 7-41. (A5h) IIN_CAL Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IIN_GAIN_CAL				IIN_OFS_CAL			

LEGEND: R/W = Read/Write; R = Read only

表 7-57. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	IIN_GAIN_CAL	R/W	NVM	These bits contains the READ_IIN gain calibration. This field gives flexibility to change the gain of nominal reporting by −3.5% to +4%. 0000b: IIN Gain Adjustment = −3.5% 0001b: IIN Gain Adjustment = −3.0% 0010b: IIN Gain Adjustment = −2.5% 0011b: IIN Gain Adjustment = −2.0% 0100b: IIN Gain Adjustment = −1.5% 0101b: IIN Gain Adjustment = −1.0% 0110b: IIN Gain Adjustment = −0.5% 0111b: IIN Gain Adjustment = −0% 1000b: IIN Gain Adjustment = +0.5% 1001b: IIN Gain Adjustment = +1.0% 1010b: IIN Gain Adjustment = +1.5% 1011b: IIN Gain Adjustment = +2.0% 1100b: IIN Gain Adjustment = +2.5% 1101b: IIN Gain Adjustment = +3.0% 1110b: IIN Gain Adjustment = +3.5% 1111b: IIN Gain Adjustment = +4.0%

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表 7-57. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
3:0	IIN_OFS_CAL	R/W	NVM	These bits contains the READ_IIN offset calibration. This field gives flexibility to change the nominal reporting by −2.0 A to 1.75 A. However, special attention is needed when setting the offset adjustment to a negative value. The calculation from the combination of ADC conversion and calibration register input is not clamped at zero. When the calculated value of (ADC conversion result + calibration offset value) goes negative, the final reporting value rolls over to a large positive value (decreased from the maximum limit). For example, for a case of real I_{IN} = 0.5 A, IIN offset adjutment = −1.0 A, IIN_MAX = 32 A, the final reporting value is not clamped at 0 A, instread, the reporting value shows +31.5 A. TI suggests using the calibration offset in a way that the calculated value from (ADC conversion result + calibration offset value) never goes negative, especially at minimum IIN case. 0000b - 0111b: Negative offset adjustment but NOT recommended to use if the minimum IIN is 0 A. Contact TI for details in case of negative offset adjustment needed. 1000b: IIN Offset Adjustment = 0 A 1001b: IIN Offset Adjustment = +0.25 A 1010b: IIN Offset Adjustment = +0.50 A 1011b: IIN Offset Adjustment = +0.75 A 1100b: IIN Offset Adjustment = +1.00 A 1101b: IIN Offset Adjustment = +1.25 A 1110b: IIN Offset Adjustment = +1.50 A 1111b: IIN Offset Adjustment = +1.75 A

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7.6.41 (A6h) VOUT_CMD

Register Address	A6h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	VID, either 5 mV/LSB or 10 mV/LSB
NVM Back-up:	EEPROM
Updates:	On-the-fly

If the *VOUT_CTRL* bits in (A0h) SYS_CFG_USER1 are set to 10b, VOUT_CMD causes the device to set its output voltage to the commanded value. Output voltage changes due to VOUT_CMD occur at ¼ of the fast slew rate which is selected in (AFh) DVS_CFG register.

The VOUT step (LSB) is either 5 mV/LSB or 10 mV/LSB which is determined by *PROCOTOL_ID* bits in (C2h) PROTOCOL_ID_SVID register.

The device will NACK writes to VOUT_CMD during soft-start and soft-stop. The device will ACK writes to VOUT_COMMAND after soft-start has completed. After soft-start has completed, writes to VOUT_CMD are also allowed even if the output voltage is still transitioning to a previously programmed VOUT_CMD. The output voltage will immediately begin transitioning to the newly programmed VOUT_CMD at the ¼ of the fast slew rate which is selected in (AFh) DVS_CFG register. The device does not wait for the prior transition to completed.

Return to Supported I²C and Default Values.

図 7-42. (A6h) VOUT_CMD Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VOUT_CMD							

LEGEND: R/W = Read/Write; R = Read only

表 7-58. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	VOUT_CMD	R/W	NVM	Sets the output voltage target via the I²C interface. See 表 7-6 for the available values.

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7.6.42 (A7h) VID_SETTING

CMD Address	A7h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	VID, either 5 mV/LSB or 10 mV/LSB
NVM Backup:	No
Update Rate:	190 µs
Supported Range:	8 V – 16 V

The VID_SETTING command returns the last commanded VOUT level either from I^{2}C or from SVID including Vboot. The reading in this register is “in sync” with the SVID (31h) VID_SETTING register. This register does not include any OFFSET contributions from either SVID or I^{2}C space.

Return to Supported I^{2}C and Default Values.

図 7-43. (A7h) VID_SETTING Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VID_SETTING							

LEGEND: R/W = Read/Write; R = Read only

表 7-59. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	VID_SETTING	R	Last commanded VOUT	These bits tells the last commanded VOUT (VID format).

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7.6.43 (A8h) I²C_OFFSET

Register Address	A8h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	DIRECT
NVM Back-up:	EEPROM
Updates:	on-the-fly

The I²C_OFFSET is used to apply a fixed offset voltage to the output voltage command value. Output voltage changes due to I²C_OFFSET occur at ¼ of the fast slew rate which is selected in (AFh) DVS_CFG register..

The usage of I²C_OFFSET depends on the value of *VOUT_CTRL* in (A0h) SYS_CFG_USER1 register. See 表 7-4 for more details.

When the *PROTOCOL_ID* bits in (C2h) PROTOCOL_ID_SVID is 01b or 10b (VOUT step = 5 mV), the I²C_OFFSET adds offset to the output voltage with the 0.5 mV/LSB. With a signed implementation, the offset can be programmed in a range of −64 mV to +63 mV.

When the *PROTOCOL_ID* bits in (C2h) PROTOCOL_ID_SVID is 00b or 11b (VOUT step = 10 mV), the I²C_OFFSET adds offset to the output voltage with the 1.0 mV/LSB. With a signed implementation, the offset can be programmed in a range of −128 mV to +127 mV.

Return to Supported I²C and Default Values.

図 7-44. (A8h) I²C_OFFSET Register Map

7	6	5	4	3	2	1	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
I²C_OFFSET							

LEGEND: R/W = Read/Write; R = Read only

表 7-60. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	I²C_OFFSET	R/W	NVM	Output voltage offset with Direct format. VOUT step = 5 mV configuration: I²C OFFSET is 0.5 mV/LSB, with a range of −64 mV to +63 mV. VOUT step = 10 mV configuration: I²C OFFSET is 1.0 mV/LSB, with a range of −128 mV to +127 mV.

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7.6.44 (A9h) COMP1_MAIN

CMD Address	A9h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The COMP1_MAIN command contains 2 fields (AC Gain and AC Load Line) for the control loop compensation. See Loop Compensation for more details.

The AC_GAIN bits select the gain of the AC paths including the output voltage error and the load current step.

The AC Load Line (ACLL) bits set the AC response to an output voltage error.

Return to Supported I2C and Default Values.

図 7-45. (A9h) COMP1_MAIN Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AC_GAIN				ACLL			

LEGEND: R/W = Read/Write; R = Read only

表 7-61. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	AC_GAIN	R/W	NVM	These bits determine the AC gain setting. 0000b: AC Gain = 0.3 0001b: AC Gain = 0.5 0010b: AC Gain = 1.0 0011b: AC Gain = 1.5 0100b: AC Gain = 2.0 0101b: AC Gain = 2.5 0110b: AC Gain = 3.0 0111b: AC Gain = 3.5 1000b: AC Gain = 4.0 1001b: AC Gain = 5.0 1010b: AC Gain = 6.0 1011b: AC Gain = 7.0 1100b to 1111b: Reserved. Do not set AC Gain to these values.

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表 7-61. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
3:0	ACLL	R/W	NVM	These bits determine the AC Load Line (ACLL) setting. 0000b: ACLL = 0.5 0001b: ACLL = 1.0 0010b: ACLL = 1.5 0011b: ACLL = 2.0 0100b: ACLL = 2.5 0101b: ACLL = 3.0 0110b: ACLL = 3.5 0111b: ACLL = 4.0 1000b: ACLL = 5.0 1001b: ACLL = 6.0 1010b: ACLL = 7.0 1011b: ACLL = 9.0 1100b: ACLL = 10.0 1101b: ACLL = 12.0 1110b: ACLL = 13.0 1111b: ACLL = 15.0

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7.6.45 (AAh) COMP2_MAIN

CMD Address	AAh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This COMP2_MAIN command contains 3 fields for configuring the internal integration circuit and the ramp generation circuit. See Loop Compensation for more details.

The INT_GAIN bits select the gain of the integration stage.

The INT_TIME bits set the time constant of the integration stage which affects the settling and response time following an output voltage error.

The RAMP bits select the amplitude of the internal-generated ramp.

Return to Supported I²C and Default Values.

図 7-46. (AAh) COMP2_MAIN Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
INT_GAIN		INT_TIME			RAMP		

LEGEND: R/W = Read/Write; R = Read only

表 7-62. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:6	INT_GAIN	R/W	NVM	These bits selects the gain of the integration stage. 00b: integration stage gain = 2 01b: integration stage gain = 1.5 10b: integration stage gain = 1 11b: integration stage gain = 0.5
5:3	INT_TIME	R/W	NVM	These bits set the time constant of the integration stage which affects the settling and response time following an output voltage error. 000b: integration time constant = 0.25 µs 001b: integration time constant = 1.0 µs 010b: integration time constant = 3.0 µs 011b: integration time constant = 4.5 µs 100b: integration time constant = 6.25 µs 101b: integration time constant = 8.0 µs 110b: integration time constant = 10.0 µs 111b: integration time constant = 20.0 µs
2:0	RAMP	R/W	NVM	These bits select the amplitude of the internal-generated ramp. 000b: ramp amplitude = 40 mV 001b: ramp amplitude = 60 mV 010b: ramp amplitude = 80 mV 011b: ramp amplitude = 100 mV 100b: ramp amplitude = 120 mV 101b: ramp amplitude = 160 mV 110b: ramp amplitude = 200 mV 111b: ramp amplitude = 240 mV

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7.6.46 (ABh) COMP1_ALT

CMD Address	ABh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The COMP1_ALT command contains 2 *alternate* fields (AC Gain and AC Load Line) for the control loop compensation. This register is not activated in the TPS544C26 device and affects nothing.

Return to Supported I²C and Default Values.

図 7-47. (ABh) COMP1_ALT Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AC_GAIN_ALT				ACLL_ALT			

LEGEND: R/W = Read/Write; R = Read only

表 7-63. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	AC_GAIN_ALT	R/W	NVM	These bits determine the *alternate* AC gain setting. 0000b: *alternate* AC Gain = 0.3 0001b: *alternate* AC Gain = 0.5 0010b: *alternate* AC Gain = 1.0 0011b: *alternate* AC Gain = 1.5 0100b: *alternate* AC Gain = 2.0 0101b: *alternate* AC Gain = 2.5 0110b: *alternate* AC Gain = 3.0 0111b: *alternate* AC Gain = 3.5 1000b: *alternate* AC Gain = 4.0 1001b: *alternate* AC Gain = 5.0 1010b: *alternate* AC Gain = 6.0 1011b: *alternate* AC Gain = 7.0 1100b to 1111b: Reserved. Do not set AC Gain to these values.
3:0	ACLL_ALT	R/W	NVM	These bits determine the *alternate* AC Load Line (ACLL) setting. 0000b: *alternate* ACLL = 0.5 0001b: *alternate* ACLL = 1.0 0010b: *alternate* ACLL = 1.5 0011b: *alternate* ACLL = 2.0 0100b: *alternate* ACLL = 2.5 0101b: *alternate* ACLL = 3.0 0110b: *alternate* ACLL = 3.5 0111b: *alternate* ACLL = 4.0 1000b: *alternate* ACLL = 5.0 1001b: *alternate* ACLL = 6.0 1010b: *alternate* ACLL = 7.0 1011b: *alternate* ACLL = 9.0 1100b: *alternate* ACLL = 10.0 1101b: *alternate* ACLL = 12.0 1110b: *alternate* ACLL = 13.0 1111b: *alternate* ACLL = 15.0

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7.6.47 (ACh) COMP2_ALT

CMD Address	ACh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This COMP2_ALT command contains 3 *alternate* fields for configuring the internal integration circuit and the ramp generation circuit. This register is not activated in the TPS544C26 device and affects nothing.

Return to Supported I²C and Default Values.

図 7-48. (ACh) COMP2_ALT Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
INT_GAIN_ALT		INT_TIME_ALT			RAMP_ALT		

LEGEND: R/W = Read/Write; R = Read only

表 7-64. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:6	INT_GAIN_ALT	R/W	NVM	These bits selects the gain of the integration stage. 00b: *alternate* integration stage gain = 2 01b: *alternate* integration stage gain = 1.5 10b: *alternate* integration stage gain = 1 11b: *alternate* integration stage gain = 0.5
5:3	INT_TIME_ALT	R/W	NVM	These bits set the time constant of the integration stage which affects the settling and response time following an output voltage error. 000b: *alternate* integration time constant = 0.25 µs 001b: *alternate* integration time constant = 1.0 µs 010b: *alternate* integration time constant = 3.0 µs 011b: *alternate* integration time constant = 4.5 µs 100b: *alternate* integration time constant = 6.25 µs 101b: *alternate* integration time constant = 8.0 µs 110b: *alternate* integration time constant = 10.0 µs 111b: *alternate* integration time constant = 20.0 µs
2:0	RAMP_ALT	R/W	NVM	These bits select the amplitude of the internal-generated ramp. 000b: *alternate* ramp amplitude = 40 mV 001b: *alternate* ramp amplitude = 60 mV 010b: *alternate* ramp amplitude = 80 mV 011b: *alternate* ramp amplitude = 100 mV 100b: *alternate* ramp amplitude = 120 mV 101b: *alternate* ramp amplitude = 160 mV 110b: *alternate* ramp amplitude = 200 mV 111b: *alternate* ramp amplitude = 240 mV

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7.6.48 (ADh) COMP3

CMD Address	ADh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The COMP3 command contains 4 fields for configuring the control loop.

The EN_SS_DCM bit sets the operation mode during the soft-start ramp. With value "1" on this bit, the device is forced to under DCM operation during the soft-start ramp. This bit doesn't control the operation mode after the soft-start ramp completes.

The SEL_NOC_TON bit selects the on-time reference for a NOC operation and thus determines the high-side FET conduction time during a NOC operation period. The on-time option selected here can help to avoid two undesired behaviors:

- For relatively low VOUT applications (such as VOUT = 1.1 V) using longer t_{ON_NOC} helps to prevent negative current run-away behavior. A NOC run-away behavior occurs when the inductor current moves more negatively during low-side FET conduction time than the movement during high-side conduction time. A NOC run-away behavior can lead to excessive stress on low-side FET and raise the concern of FET reliability.
- For applications with an extra large inductor current ripple (≥ 10 A) and the NOC threshold is set to a less negative value (for example NOC threshold = −7.5 A), the average current during the NOC operation is likely not that negative. This leads to insufficient discharge on VOUT and thus the load is stressed under the overvoltage condition for a longer period. To build sufficient negative current during the NOC operation, select the shorter t_{ON_NOC} to reduce the positive inductor current movement during the high-side on-time. A design example of this kind of case is VCCFA_EHV rail which can have the following configuration: PVIN = 12 V, VOUT = 1.8 V, f_{SW} = 1 MHz, L_{OUT} = 150 nH, ICC_MAX = 10 A, and NOC threshold = −7.5 A. To have sufficient discharge on VOUT, the design can either select the shorter t_{ON_NOC} or set ICC_MAX to 15 A so that the NOC threshold is more negative (such as −15 A).

These SEL_LO_CS bits select the L_{OUT} (output inductor value) for the current sensing circuit. The TPS544C26 IC utilizes the output inductor value entered here to build an accurate output from the current sense circuit. Please choose a value closest to the inductor that is used in a BOM. For any inductor value higher than 400 nH, set SEL_LO_CS to 11b. Selecting a value that is significantly different from the real inductor (for example, 400 nH used but 100 nH selected) can lead to an inaccurate current sense output which can cause unexpected control loop behavior and also an inaccurate READ_IOUT telemetry report.

The DCLL bits determine the DC load line setting. Select a DCLL value per the requirement from the processor or the load, otherwise, the load regulation can be out of expectation.

Return to Supported I²C and Default Values.

図 7-49. (ADh) COMP3 Register Map

7	6	5	4	3	2	1	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reserved	EN_SS_DCM	SEL_NOC_TON	SEL_LO_CS		DCLL		

LEGEND: R/W = Read/Write; R = Read only

表 7-65. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	Reserved	R	0b	Not used and always set to 0.

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表 7-65. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
6	EN_SS_DCM	R/W	NVM	0b: the operation during the soft-start ramp follows the configuration set by the *FCCM* bit in (A0h) SYS_CFG_USER1 register. 1b: Forced DCM operation during the soft-start ramp
5	SEL_NOC_TON	R/W	NVM	Select the on-time for NOC operation. See for more details
4:3	SEL_LO_CS	R/W	NVM	These bits select the L_{OUT} (output inductor value) for the current sensing circuit. 00b: L_{OUT} = 100 nH 01b: L_{OUT} = 200 nH 10b: L_{OUT} = 300 nH 11b: L_{OUT} = 400 nH
2:0	DCLL	R/W	NVM	These bits determine the DCLL setting. 000b: DCLL = 0 mΩ (VOUT maintains the regulation regardless of the load current) 001b: DCLL = 0.5 mΩ 010b: DCLL = 0.75 mΩ 011b: DCLL = 1.0 mΩ 100b: DCLL = 1.5 mΩ 101b: DCLL = 2.9 mΩ 110b: DCLL = 3.2 mΩ 111b: DCLL = 4.05 mΩ

表 7-66. High-side On Time During a NOC Operation

PROTOCOL_ID in (C2h) PROTOCOL_ID_SVID	SEL_NOC_TON	Option	t_{ON_NOC} (ns)
PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)	1	Shorter t_{ON_NOC}	Use: $t_{ON_NOC} = \frac{0.6\ V}{PVIN \times f_{SW}}$ (9)
	0	Longer t_{ON_NOC}	Use: $t_{ON_NOC} = \frac{1.6\ V}{PVIN \times f_{SW}}$ (10)
PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)	1	Shorter t_{ON_NOC}	Use: $t_{ON_NOC} = \frac{1.2\ V}{PVIN \times f_{SW}}$ (11)
	0	Longer t_{ON_NOC}	Use: $t_{ON_NOC} = \frac{3.2\ V}{PVIN \times f_{SW}}$ (12)

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7.6.49 (AFh) DVS_CFG

Register Address	AFh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	on-the-fly

The DVS_CFG sets the fast slew rate at which any output voltage changes per SVID SetVID-Fast command. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off. The unit is mV/µs.

Return to Supported I2C and Default Values.

図 7-50. (AFh) DVS_CFG Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					DVS_CFG		

LEGEND: R/W = Read/Write; R = Read only

表 7-67. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	DVS_CFG	R/W	NVM	These bits select the Dynamic Voltage Scale (DVS) fast slew rate. Upon acknowledging a new value written into this register, the new slew rate value is loaded into SVID (24h) SR_FAST register immediately. See below table for details.

表 7-68. Dynamic Voltage Scale Fast Slew Rate Options

DVS_CFG	DVS Fast Slew Rate (mV/µs)	
	PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)	PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)
000	1.34	2.67
001	1.43	2.86
010	2.50	5.00
011	2.67	5.34
100	5.00	10.00
101	5.56	11.12
110	10.00	20.00
111	12.50	25.00

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7.6.50 (B0h) DVID_OFFSET

CMD Address	B0h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The DVID_OFFSET command contains 2 fields for configuring the DAC offset during a DVID transition. This Vout-referred offset is added only during a DVID transition (for example per SetVID or SetWP command). DVID_OFS_UP is used to compensate for delays in the feedback compensation network and reach the target value faster for DVID up scenario, and DVID_OFS_DOWN is implemented to prevent the output from ringing below the target for DVID down scenario. Note that:

- The offsets are used only when the selected DVID slew rate is Fast or Slow.
- The offsets are not used when the selected DVID slew rate is Decay nor for (A6h) VOUT_CMD changes via I^2C.
- The offsets are not used during soft-start nor during soft-stop period.

Return to Supported I^2C and Default Values.

図 7-51. (B0h) DVID_OFFSET Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W
Reserved				DVID_OFS_DOWN		DVID_OFS_UP	

LEGEND: R/W = Read/Write; R = Read only

表 7-69. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3:2	DVID_OFS_DOWN	R/W	NVM	This positive offset is effectively a threshold: When the new VID target is lower than the current VOUT, the DAC starts counting down from its current value using the selected slew rate, and continues until the DAC reaches VID target + DVID_OFS_DOWN. At that point, the VOUT transition slew rate changes to ¼ of the selected slew rate until the actual VID target is reached. 00b: DVID_OFS_DOWN = 0 mV 01b: DVID_OFS_DOWN = 5 mV 10b: DVID_OFS_DOWN = 10 mV 11b: DVID_OFS_DOWN = 20 mV
1:0	DVID_OFS_UP	R/W	NVM	This positive DAC offset is to be added when the new VID target is higher than the current VOUT. DVID_OFS_UP is added immediately to the current DAC count as the first step toward the new target, and as soon as the DAC count reaches the VID target, the DAC stops the ramp, and DVID_OFS_UP is no longer applied. 00b: DVID_OFS_UP = 0 mV 01b: DVID_OFS_UP = 5 mV 10b: DVID_OFS_UP = 10 mV 11b: DVID_OFS_UP = 20 mV

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7.6.51 (B1h) REG_LOCK

CMD Address	B1h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No
Updates:	On-the-fly

The REG_LOCK command controls writing to the TPS544C26 device. The intent of this command is to provide protection against accidental changes. This command does NOT provide protection against deliberate or malicious changes to a configuration or operation of the device.

After power-on, the user accessible registers with write access are by default under "write protected" state, meaning the response to a write is NACK. The device always acknowledges a read command and responds the data byte accordantly. Only after writing the correct passcodes (multiple writes in the right order) into this REG_LOCK register, the user accessible registers are "unlocked" and the device acknowledges the next write commands. For a device under "unlock" state, the writable registers turn to "write protected" state again if one more write is sent to (B1h) REG_LOCK register, no matter with the correct passcode or wrong one. The user has to go through the complete passcode write combination to unlock the write protection again.

For a device under "unlock" state, VCC power cycling resets the device and the user accessible registers with write access are now under "write protected" state. A RESTORE_USER_ALL command does not change the state.

The expected response for a write into this REG_LOCK register is always NACK, no matter with a correct passcode or a wrong value. For security considerations, the passcodes are not listed in this datasheet. Please contact TI for more details.

All user accessible registers with write access are protected by this mechanism except below ones:

- (03h) CLEAR_FAULTS
- (7Ah) STATUS_VOUT
- (7Bh) STATUS_IOUT
- (7Ch) STATUS_INPUT
- (7Dh) STATUS_TEMPERATURE
- (80h) STATUS_MFR
- (A2h) I2C_ADDR, bit[7] - this bit is reserved for TI usage and always under write protection
- (B1h) REG_LOCK

Return to Supported I2C and Default Values.

図 7-52. (B1h) REG_LOCK Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
Passcode							

LEGEND: R/W = Read/Write; R = Read only

表 7-70. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	Passcode	W	00000000b	Write the passcodes to unlock the write protection.

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7.6.52 (B3h) PIN_SENSE_RES

CMD Address	B3h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The PIN_SENSE_RES command selects the external input current/power sense resistor value and related configurations. The supported sensing resistor value ranges from 0.25 mΩ to 4 mΩ.

Return to Supported I2C and Default Values.

図 7-53. (B3h) PIN_SENSE_RES Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					PIN_SENSE_RES		

LEGEND: R/W = Read/Write; R = Read only

表 7-71. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	PIN_SENSE_RES	R/W	NVM	These bits select the external sensing resistor used for input current/power measurement. See below table for more details.

表 7-72. Input Current/Power Sense Resistor Value and IIN_MAX

PIN_SENSE_RES	RSENSE used in a BOM (mΩ)	Internal Gain (V/V)	IIN_MAX (A)	IIN LSB (A)
000	4	12.5	16	0.0625
001	3	12.5	21.3	0.0833
010	2	25	16	0.0625
011	1	20	40	0.15625
100	1	25	32	0.125
101	0.5	40	40	0.15625
110	0.5	50	32	0.125
111	0.25	50	64	0.250

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7.6.53 (B4h) IOUT_NOC_LIMIT

CMD Address	B4h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The IOUT_NOC_LIMIT command contains 3 fields for configuring the VOUT Fixed OVF and Neagive Overcurrent (NOC) limit selection.

The SEL_FIX_OVF bit sets the value of the output voltage measured at the (VOSNS − GOSNS) pins that causes an output overvoltage fault. The Fixed OVF function sets a constant overvoltage threshold that has no relationship to the current VOUT setting. The VOUT Fixed OVF is active as soon as the TPS544C26 device completes its power-on reset, even if the output conversion is disabled.

Following a Fixed OVF condition, the device always latches OFF high-side MOSFET and latches ON low-side MOSFET. The response setting in (41h) VOUT_OV_FAULT_RESP register does not affect the response for a Fixed OVF condition.

The VOUT Fixed OVF feature can be disabled through the *EN_FIX_OVF* bit.

The NOC threshold which scales with ICC_MAX setting (see (C0h) ICC_MAX) is selected by SEL_NOC field.

Return to Supported I²C and Default Values.

図 7-54. (B4h) IOUT_NOC_LIMIT Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W
Reserved				SEL_FIX_OVF	EN_FIX_OVF	SEL_NOC	

LEGEND: R/W = Read/Write; R = Read only

表 7-73. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	Reserved	R	0000b	Not used and always set to 0.
3	SEL_FIX_OVF	R/W	NVM	Select the VOUT Fixed OVF thresholds. See details on 表 7-74.
2	EN_FIX_OVF	R/W	NVM	0b: Enable the VOUT Fixed OVF 1b: Disable the VOUT Fixed OVF
1:0	SEL_NOC	R/W	NVM	Select the Negative Overcurrent limits which scale with ICC_MAX setting. See details on 表 7-75.

表 7-74. VOUT Fixed OV Fault Thresholds

PROTOCOL_ID in (C2h) PROTOCOL_ID_SVID	SEL_FIX_OVF[1] in (B4h) IOUT_NOC_LIMIT	VOUT Fixed OVF threshold (V)
PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)	0	1.5
PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)	1	1.8
PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)	0	2.4
PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)	1	3.0

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表 7-75. Negative Overcurrent Limits

SEL_NOC[1:0]	Negative Overcurrent Limits (A)	
	ICC_MAX ≥ 15 A	ICC_MAX ≤ 10 A
00	−20	−10
01	−15	−7.5
10	−12	−6
11	−10	−5

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7.6.54 (B5h) USER_DATA_01

CMD Address	B5h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The USER_DATA_01 command provides memory for users to store manufacturer specific information. User chooses the format and data value.

Return to Supported I²C and Default Values.

図 7-55. (B5h) USER_DATA_01 Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R	R	R	R
USER_DATA_01				Reserved			

LEGEND: R/W = Read/Write; R = Read only

表 7-76. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	USER_DATA_01	R	NVM	User to store manufacturer specific information
3:0	Reserved	R	0000b	Not used and always set to 0.

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7.6.55 (B6h) USER_DATA_02

CMD Address	B6h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The USER_DATA_02 command provides memory for users to store manufacturer specific information. User chooses the format and data value.

Return to Supported I²C and Default Values.

図 7-56. (B6h) USER_DATA_02 Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R	R	R	R	R
USER_DATA_02			Reserved				

LEGEND: R/W = Read/Write; R = Read only

表 7-77. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:5	USER_DATA_02	R/W	NVM	User to store manufacturer specific information
4:0	Reserved	R	00000b	Not used and always set to 0.

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7.6.56 (BAh) STATUS1_SVID

CMD Address	BAh
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)

The STATUS1_SVID command contains direct copies of the bits of SVID (10h) STATUS_1 register. When a bit in the SVID (10h) STATUS_1 register is cleared via the SVID bus, the corresponding bit in I^2C (BAh) STATUS1_SVID register also get cleared. There is no separate clear mechanism for the bits in BAh register via the I^2C bus.

Return to Supported I^2C and Default Values.

図 7-57. (BAh) STATUS1_SVID Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_STATUS2	Reserved			VID_DAC_High	IccMaxAlert	ThermAlert	VR_Settled

LEGEND: R/W = Read/Write; R = Read only

表 7-78. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	READ_STATUS2	R	Current status	Defined by Intel. Refer to Intel document for details.
6:4	Reserved	R	000b	Not supported and always set to 0.
3	VID_DAC_High	R	Current status	Defined by Intel. Refer to Intel document for details.
2	IccMaxAlert	R	Current status	Defined by Intel. Refer to Intel document for details.
1	ThermAlert	R	Current status	Defined by Intel. Refer to Intel document for details.
0	VR_Settled	R	Current status	Defined by Intel. Refer to Intel document for details.

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7.6.57 (BBh) STATUS2_SVID

CMD Address	BBh
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)

The STATUS2_SVID command contains direct copies of the bits of SVID (11h) STATUS_2 register. When a bit in the SVID (11h) STATUS_2 register is cleared via the SVID bus, the corresponding bit in I^2C (BBh) STATUS2_SVID register also get cleared. There is no separate clear mechanism for the bits in BBh register via the I^2C bus.

Return to Supported I^2C and Default Values.

図 7-58. (BBh) STATUS2_SVID Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
Reserved					SVID_OCL_LATCH	SVID_frame_err	SVID_parity_err

LEGEND: R/W = Read/Write; R = Read only

表 7-79. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not supported and always set to 0.
2	SVID_OCL_LATCH	R	Current status	Defined by Intel. Refer to Intel document for details.
1	SVID_frame_err	R	Current status	Defined by Intel. Refer to Intel document for details.
0	SVID_parity_err	R	Current status	Defined by Intel. Refer to Intel document for details.

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7.6.58 (BCh) CAPABILITY

CMD Address	BCh
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)

The CAPABILITY command contains direct copies of the bits of SVID (06h) CAPABILITY register, which indicates telemetry capabilities of the part. This register is read-only.

Return to Supported I2C and Default Values.

図 7-59. (BCh) CAPABILITY Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IOUT	TEMP	PIN	VIN	IIN	POUT	VOUT	VR13+

LEGEND: R/W = Read/Write; R = Read only

表 7-80. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IOUT	R	1b	1b: IOUT telemetry is supported
6	TEMP	R	1b	1b: TEMP telemetry is supported
5	PIN	R	1b	1b: PIN telemetry is supported
4	VIN	R	1b	1b: VIN telemetry is supported
3	IIN	R	1b	1b: IIN telemetry is supported
2	POUT	R	0b	0b: POUT telemetry is NOT supported
1	VOUT	R	1b	1b: VOUT telemetry is supported
0	VR13+	R	1b	1b: The output current telemetry is supported in the VR13+ format

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7.6.59 (BDh) EXT_CAPABILITY_VIDOMAX_H

CMD Address	BDh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	Bit[7:1]: No Bit[0]: Yes
Updates:	Bit[0] only: On-the-fly when the power conversion is disabled. A write is not allowed (NACK response) when the power conversion is enabled.

The EXT_CAPABILITY_VIDOMAX_H command contains direct copies of the bits of SVID (09h) VIDOMAX_H_CAPA register except bit[0]. The lowest bit (bit[0]) is MSB of 9-bit VIDo_MAX value and the user can read and write into this bit. See more details in (BEh) VIDO_MAX_L register. The rest 7 bits in this register indicates the extended capabilities of the part. These 7 bits are read-only.

Return to Supported I2C and Default Values.

図 7-60. (BDh) EXT_CAPABILITY_VIDOMAX_H Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R/W
PsysWarn	IMON_CAL	DFDS	DFDV	HI_PRES	IccInMax	Reserved	VIDo_MAX[8]

LEGEND: R/W = Read/Write; R = Read only

表 7-81. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	PsysWarn	R	0b	0b: PsysWarn is NOT supported
6	IMON_CAL	R	0b	0b: SVID IMON_CAL is NOT supported
5	DFDS	R	0b	0b: DFDS function is NOT supported
4	DFDV	R	0b	0b: DFDV function is NOT supported
3	HI_PRES	R	0b	0b: HI_PRES telemetry is NOT supported
2	IccInMax	R	0b	1b: IccInMax is supported for IIN telemetry
1	Reserved	R	0b	Not used and always set to 0.
0	VIDo_MAX[8]	R/W	NVM	MSB of 9-bit VIDo_MAX value. See more details in (BEh) VIDO_MAX_L register.

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7.6.60 (BEh) VIDOMAX_L

Register Address	BEh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly when the power conversion is disabled. A write is not allowed (NACK response) when the power conversion is enabled.

The VIDOMAX_L command together with the bit[0] in (BDh) EXT_CAPABILITY_VIDOMAX_H forms a 9-bit register to set the maximum value of (VID+Offset) allowed via SVID. Setting the 9-bit VIDo_MAX register to 17E (hex) value reaches the maximum possible (VID+Offset) value with 8-bit register for each (VID unsigned, offset signed).

Exceeding VIDo_MAX with (VID + offset) causes a REJ (Reject) response for individual rail SVID requests and a NACK response for all-call SVID requests.

When a write to this register is attempted, the VIDOMAX_L value combined with VIDo_MAX[8] value (bit[0] in (BDh) EXT_CAPABILITY_VIDOMAX_H register) must satisfy a range check:

- If the combined value is not greater than 0, the write is NACKed.
- If the combined value is greater than 0, then the write is ACKed.

Further, VIDo_MAX bit in (BDh) EXT_CAPABILITY_VIDOMAX_H register does not take effect when updated. It only takes effect when the VIDOMAX_L register is written with a value (can be the same value as the current one) and also the combined value satisfies the range check. When attempting to write a new VIDo_MAX value, it is recommended to write in the following order: write into the (BDh) EXT_CAPABILITY_VIDOMAX_H register first, and then write into the VIDOMAX_L register. To illustrate, a few examples are listed below:

- Example #1: Firstly, a value is written into (BDh) EXT_CAPABILITY_VIDOMAX_H register and is acknowledged. Secondly, another write command is sent to (BEh) VIDOMAX_L register and this write is acknowledged too.
  - Result: The 9-bit VIDo_MAX register is updated and takes effect.
- Example #2: A value is written into (BEh) VIDOMAX_L register and is acknowledged. No write command is sent to (BDh) EXT_CAPABILITY_VIDOMAX_H register.
  - Result: The 9-bit VIDo_MAX register is updated in the lower 8-bit (in (BEh) VIDOMAX_L register) and the new value takes effect.
- Example #3: Firstly, a value is written into (BEh) VIDOMAX_L register and is acknowledged. Secondly, another write command is sent to (BDh) EXT_CAPABILITY_VIDOMAX_H register to update VIDo_MAX bit with a new value and this write is acknowledged too.
  - Result: The 9-bit VIDo_MAX register is updated but the VIDo_MAX bit in (BDh) EXT_CAPABILITY_VIDOMAX_H register does not take effect.

Note: (BDh) EXT_CAPABILITY_VIDOMAX_H and (BEh) VIDOMAX_L registers acknowledges a write only when the power conversion is disabled. A write is not allowed (NACK response) when the power conversion is enabled.

Return to Supported I²C and Default Values.

図 7-61. (A6h) VOUT_CMD Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VIDOMAX_L							

LEGEND: R/W = Read/Write; R = Read only

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表 7-82. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	VIDOMAX_L	R/W	NVM	These bits sets the lower 8-bit value for the 9-bit VIDoMAX register.

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7.6.61 (C0h) ICC_MAX

CMD Address	C0h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The ICC_MAX command sets the effective maximum output current that the device reports through the IOUT telemetry sub-system. ICC_MAX setting is not a fault threshold. Upon acknowledging a new value written into this register, the new ICC_MAX value is loaded into SVID (21h) ICC_MAX register immediately.

Return to Supported I2C and Default Values.

図 7-62. (C0h) ICC_MAX Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					ICC_MAX		

LEGEND: R/W = Read/Write; R = Read only

表 7-83. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	ICC_MAX	R/W	NVM	These bits configures the ICC_MAX setting. 000b: ICC_MAX = 6 A (not recommended) 001b: ICC_MAX = 10 A (not recommended) 010b: ICC_MAX = 15 A (recommend using 15 A setting for a design with maximum load less than 10 A) 011b: ICC_MAX = 20 A 100b: ICC_MAX = 25 A 101b: ICC_MAX = 30 A 110b: ICC_MAX = 35 A 111b: ICC_MAX = 40 A Note: ICC_MAX = 6 A or 10 A option is not recommended to use. Instread, using the 15 A option for a design with 10A or less load is recommended.

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7.6.62 (C1h) TEMP_MAX

CMD Address	C1h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The TEMP_MAX command provides a default value for SVID (22h) TEMP_MAX register. The TEMP_MAX setting is not a fault threshold. Upon acknowledging a new value written into this register, the new TEMP_MAX value is loaded into SVID (22h) TEMP_MAX register immediately.

Return to Supported I2C and Default Values.

図 7-63. (C1h) TEMP_MAX Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R/W	R/W	R/W
Reserved					TEMP_MAX		

LEGEND: R/W = Read/Write; R = Read only

表 7-84. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:3	Reserved	R	00000b	Not used and always set to 0.
2:0	TEMP_MAX	R/W	NVM	These bits configures the TEMP_MAX setting. 000b: TEMP_MAX = 95 °C 001b: TEMP_MAX = 100 °C 010b: TEMP_MAX = 105 °C 011b: TEMP_MAX = 110 °C 100b: TEMP_MAX = 115 °C 101b: TEMP_MAX = 120 °C 110b: TEMP_MAX = 125 °C 111b: TEMP_MAX = 130 °C

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7.6.63 (C2h) PROTOCOL_ID_SVID

CMD Address	C2h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	Vboot: on-the-fly. PROTOCOL_ID and ALL_CALL_SEL: field value update will wait until the power conversion is disabled.

This PROTOCOL_ID_SVID command contains 3 fields for configuring the SVID Protocol ID, Vboot (boot up voltage), and All-call address selection.

The PROTOCOL_ID bits set the Protocol ID for SVID communication. The setting also programs an internal precision resistor divider thus determines the VOUT scaling (mV/LSB) of the device.

The Vboot bits program the initial output voltage at start-up when the output voltage is controlled by SVID interface (e.g. VOUT_CTRL = 00b or 01b).

The ALL_CALL_SEL bits set the All-call address for SVID communication.

Return to Supported I2C and Default Values.

図 7-64. (C2h) PROTOCOL_ID_SVID Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PROTOCOL_ID		Vboot				ALL_CALL_SEL	

LEGEND: R/W = Read/Write; R = Read only

表 7-85. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:6	PROTOCOL_ID	R/W	NVM	These bits set the Protocol ID for SVID communication. The setting also programs an internal precision resistor divider thus determines the VOUT scaling (mV/LSB) of the device. 00b: SVID PROTOCOL ID = 04h (VR13, 10 mV). And VOUT_CMD step = 10 mV/LSB 01b: SVID PROTOCOL ID = 07h (VR13, 5 mV). And VOUT_CMD step = 5 mV/LSB 10b: SVID PROTOCOL ID = 09h (VR14, 5 mV). And VOUT_CMD step = 5 mV/LSB 11b: SVID PROTOCOL ID = 0Ah (VR14, 10 mV). And VOUT_CMD step = 10 mV/LSB The function selected in this field is loaded into SVID register (05h) PROTOCOL_ID as well. In order for this field to take effect, the power conversion must be disabled. *Note: The TPS544C26 device is VR13 compliant and no support to VR14.*
5:2	Vboot	R/W	NVM	These bits program the initial output voltage at start-up. See 表 7-86 for the available settings. The Vboot and Protocol ID selections have to align based on the listed options on 表 7-86 no matter the VOUT adjustment is controlled by SVID interface or I2C interface. Otherwise, an error check will NACK the write attempt. For example, a write attempt with C2h = 011111xxb (Vboot = 1.8 V and Protocol ID = 5 mV) will be NACKed, while a write attempt with C2h = 011000xxb (Vboot = 1.1V and Protocol ID = 5mV) will be ACKed. The function selected in this field is loaded into SVID register (26h) VBOOT as well, in VID format.

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表 7-85. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
1:0	ALL_CALL_SEL	R/W	NVM	These bits set the All-call address for SVID communication. 00b: Not support All-call address, will reject both 0Eh and 0Fh address 01b: Respond to All-call address 0Fh only 10b: Respond to All-call address 0Eh only 11b: Respond to All-call address both 0Eh and 0Fh The function selected in this field is loaded into SVID register (0Fh) ALLCALL_ACT as well. In order for this field to take effect, the power conversion must be disabled.

表 7-86. Vboot settings

Vboot	VID code(1) (Hex)	Vboot (V)	PROTOCOL_ID
0000b	00h	0	Must set PROTOCOL_ID = 01b or 10b (VOUT step = 5 mV)
0001b	65h	0.75	
0010b	6Fh	0.80	
0011b	79h	0.85	
0100b	83h	0.90	
0101b	8Dh	0.95	
0110b	97h	1.00	
0111b	A1h	1.05	
1000b	ABh	1.10	
1001b	AFh	1.20	
1010b	C9h	1.25	
1011b	DDh	1.35	
1100b	FBh	1.50	
1101b	6Fh	1.60	Must set PROTOCOL_ID = 00b or 11b (VOUT step = 10 mV)
1110b	79h	1.70	
1111b	83h	1.80	

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7.6.64 (C6h) VENDOR_ID

CMD Address	C6h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)

The VENDOR_ID command reads an unique identity of the IC vendor. This vendor ID value is assigned to Texas Instruments by Intel. The Vendor ID value is loaded into SVID (00h) VENDOR_ID register during the initial power-on.

Return to Supported I2C and Default Values.

図 7-65. (C6h) VENDOR_ID Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VENDOR_ID							

LEGEND: R/W = Read/Write; R = Read only

表 7-87. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	VENDOR_ID	R	00100010b	A Vendor ID to identify the IC vendor.

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7.6.65 (C8h) PRODUCT_ID

CMD Address	C8h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)

The PRODUCT_ID command reads an unique identity of the IC. This unique product ID is chosen by Texas Instruments for TPS544C26 device. The product ID value is loaded into SVID (01h) PRODUCT_ID register during the initial power-on.

Return to Supported I2C and Default Values.

図 7-66. (C8h) PRODUCT_ID Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PRODUCT_ID							

LEGEND: R/W = Read/Write; R = Read only

表 7-88. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	PRODUCT_ID	R	00010011b	A product ID to identify the TPS544C26 device.

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7.6.66 (C9h) PRODUCT_REV_ID

CMD Address	C9h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)

The PRODUCT_REV_ID command reads the IC's revision. This product revision ID is assigned by Texas Instruments and this value is loaded into SVID (02h) PRODUCT_REV register during the initial power-on.

Return to Supported I2C and Default Values.

図 7-67. (C9h) PRODUCT_REV_ID Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PRODUCT_REV_ID							

LEGEND: R/W = Read/Write; R = Read only

表 7-89. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	PRODUCT_REV_ID	R	00000010b	These bits read the TPS544C26 device's revision. 00000010b: PG2.1 production unit (current revision) 00000001b: PG2.0 engineering samples (previous revision) 00000000b: PG1.0 engineering samples (previous revision)

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8 Application and Implementation

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8.1 Application Information

The TPS544C26 device is a highly-integrated, synchronous, step-down DC/DC converter. The TPS544C26 has a simple design procedure where programmable parameters can be configured by I^{2}C and stored to nonvolatile memory (NVM) to minimize external component count.

8.2 Typical Application

8.2.1 Application

This design describes a 1.1-V, 35-A application for a VCCD_HV rail in an Intel Server platform.

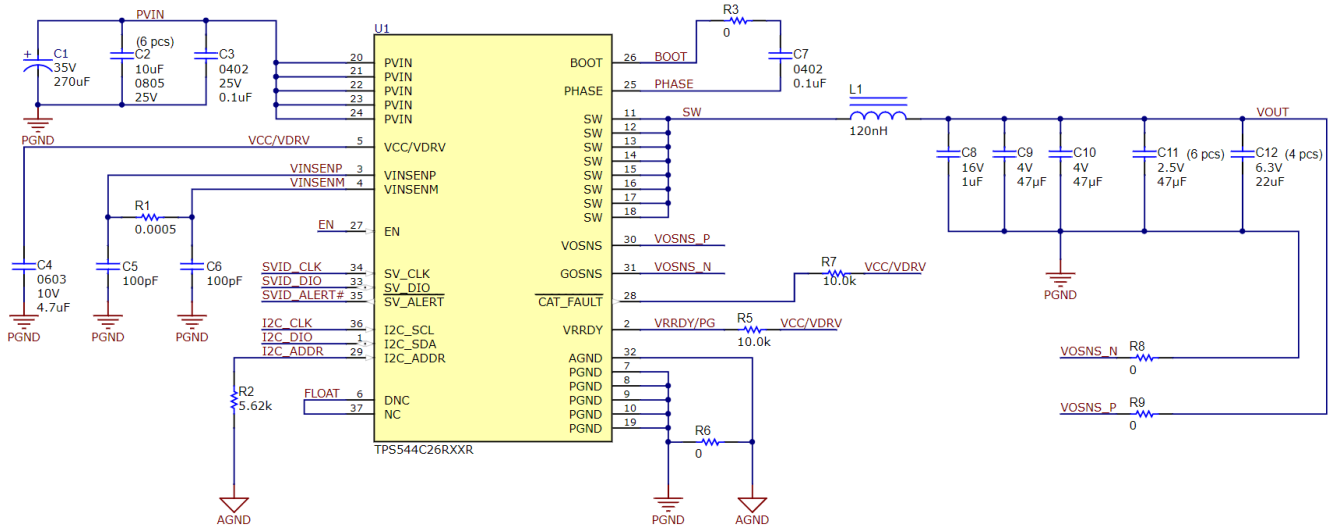


図 8-1. VCCD_HV 1.1 V Output Application

8.2.2 Design Requirements

This design uses the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input Voltage	10.8 V – 13.2 V
Output Voltage	1.1 V
Output Current	35 A
Switching Frequency	800 kHz
I^{2}C Address	71h
SVID Address	00h

8.2.3 Detailed Design Procedure

This design example leverages the requirements for the VCCD_HV rail in an Intel Server platform. The default settings for this device are optimal for this application. The following steps illustrate how to select key components.

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8.2.3.1 Inductor Selection

The inductor must be selected such that the transient performance and ripple requirements are balanced for a particular design. In general, a smaller inductance increases loop bandwidth leading to better transient response at the expense of higher current and voltage ripple. In this example, a 120-nH, 0.228-mΩ inductor is used.

8.2.3.2 Input Capacitor Selection

Input capacitors must be selected to provide reduction in input voltage ripple and high-frequency bypassing, which in return will reduce switching stress on the power stage MOSFETs internal to the device. In this example, a 0.1-µF, 25-V, 0402 must be placed as close as possible to pin 20 of the device on the same layer as the IC on the PCB. In addition, 6x 10-µF ceramic capacitors are used and a 270-µF bulk capacitor is used on the input.

8.2.3.3 Output Capacitor Selection

To meet the output voltage ripple and load transient requirements in the Intel specification, use a 1-µF and 2 x 47-µF ceramic capacitors local to the output of the inductor. Additionally, use 6 x 47-µF on the top-side of the CPU socket cavity combined with 4 x 22-µF capacitors on the bottom-side of the CPU socket cavity.

8.2.3.4 VCC/VRDV Bypass Capacitor

Use a minimum of 2.2-µF to 4.7-µF, 10-V rated capacitor for bypassing of the VCC/VDRV pin. This bypass capcitor must refer to PGND to minimize the length of high-frequency driving current path.

8.2.3.5 BOOT Capacitor Selection

Use a minimum of a 0.1-µF capacitor connected from Phase (pin 25) to Boot (pin 26). An optional serires boot resistor of 0-Ω or 2.2-Ω can be added.

8.2.3.6 RSENSE Selection

In this application, a 0.5-Ω resistor is selected to sense the input current (IIN) on a 12 V bus for DDR5 DIMMs. The sensed input current and the sensed input voltage on pin 4 VINSENM are used to calculate the total input power. The input power information can be read through telemetry registers and used for power management.

8.2.3.7 VINSENP and VINSENN Capacitor Selection

Use a 100-pF ceramic capacitor referenced to PGND on both the VINSENP (pin 3) and VINSENN (pin 4). The decoupling capacitors minimizes the impact from switching noise on the 12 bus and thus help the device to achieve high accuracy on IIN reporting.

8.2.3.8 VRRDY Pullup Resistor Selection

The VRRDY output is an open-drain output and must be pulled up externally through a pullup resistor. Place a pull-up resistor, within a 1-kΩ to 100-kΩ range, at the VRRDY pin (pin 2). In this example, VRRDY is pulled up to VCC/VDRV with a 10-kΩ resitor.

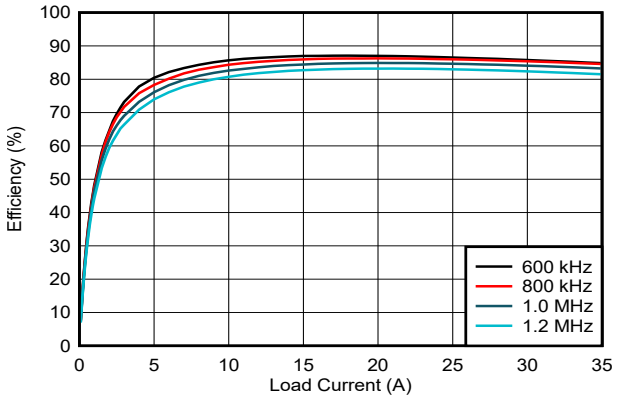
8.2.3.9 I^2C Address Resistor Selection

Refer to 表 7-16 for the list of I^2C addresses selectable by an external resistor. A resistor between the I^2C_ADDR (pin 29) and AGND sets the preconfigured I^2C address in the memory map. In this application, the 5.62-kΩ resistor selects an I^2C address of 71h.

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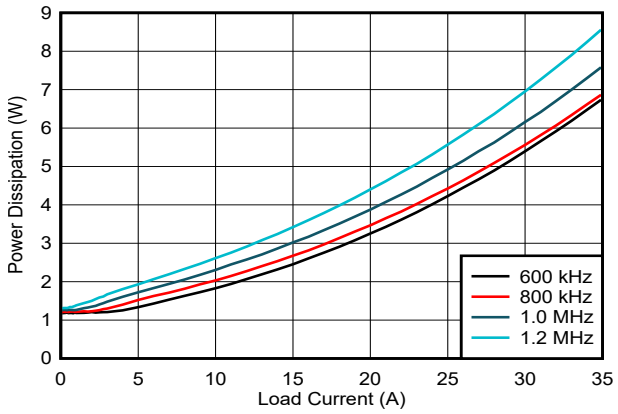
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8.2.4 Application Curves



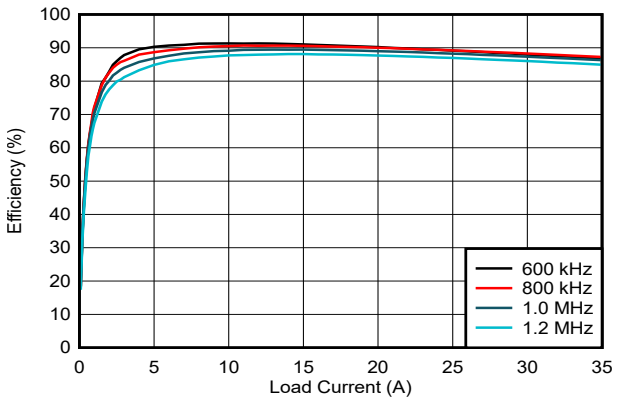
PVIN = 12 V V_{OUT} = 1.1 V

図 8-2. Efficiency, FCCM, Internal LDO



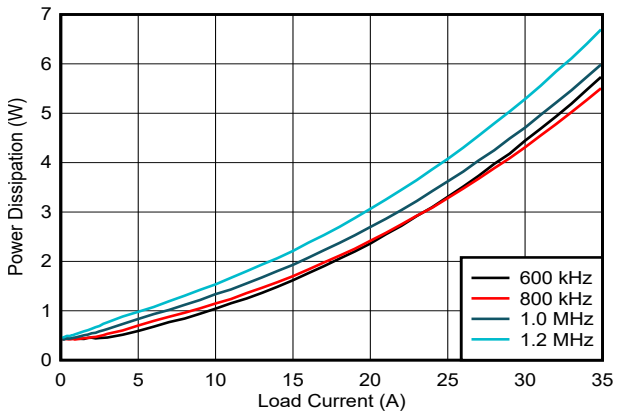
PVIN = 12 V V_{OUT} = 1.1 V

図 8-3. Power Dissipation, FCCM, Internal LDO



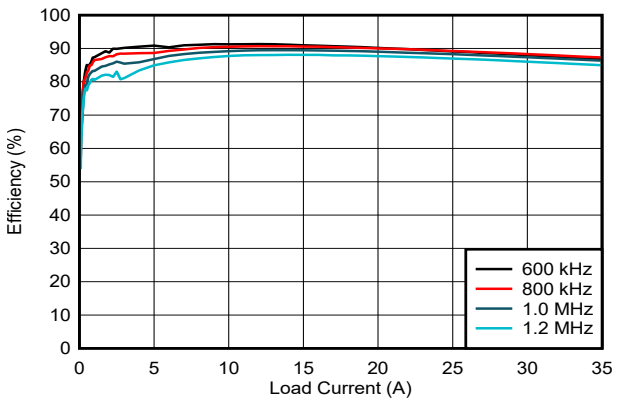
PVIN = 12 V V_{OUT} = 1.1 V

図 8-4. Efficiency, FCCM, External 5-V Bias



PVIN = 12 V V_{OUT} = 1.1 V

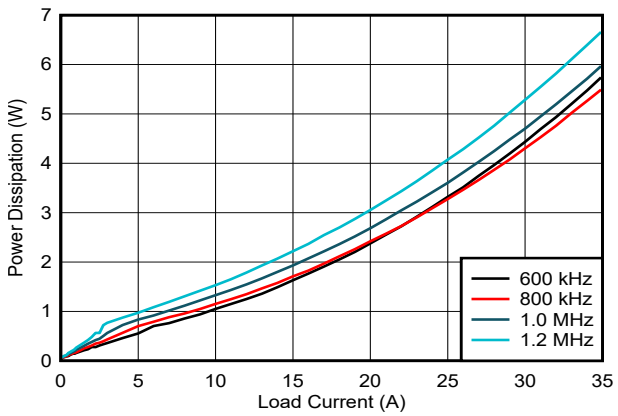
図 8-5. Power Dissipation, FCCM, External 5-V Bias



注

PVIN = 12 V V_{OUT} = 1.1 V

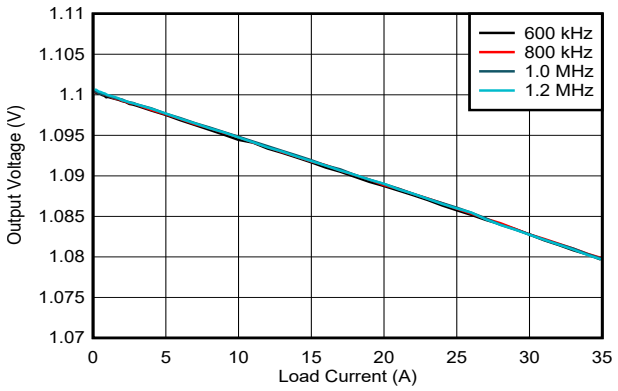
図 8-6. Efficiency, DCM, External 5-V Bias



PVIN = 12 V V_{OUT} = 1.1 V

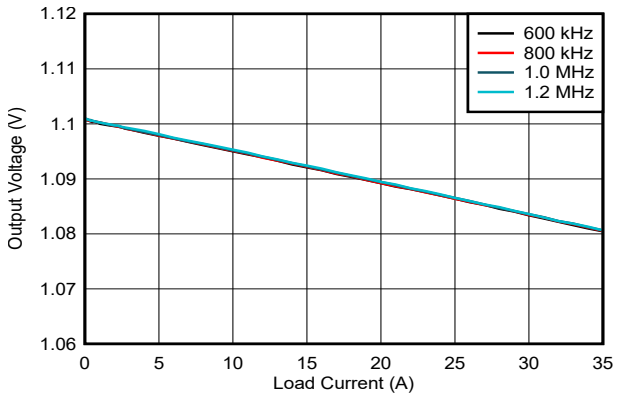
図 8-7. Power Dissipation, DCM, External 5-V Bias

ADVANCE INFORMATION



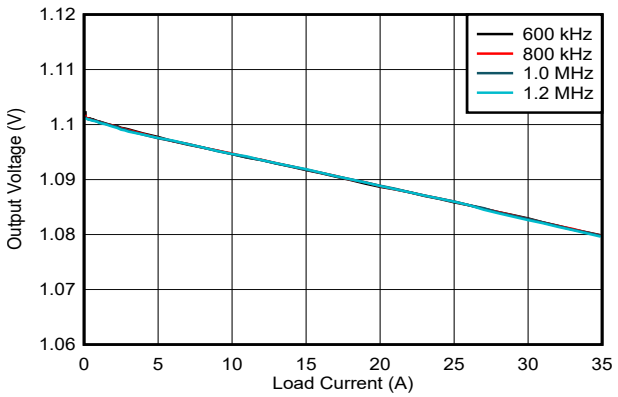
PVIN = 12 V
DC Load Line (DCLL) = 0.75 mΩ

図 8-8. Load Regulation, FCCM, Internal LDO



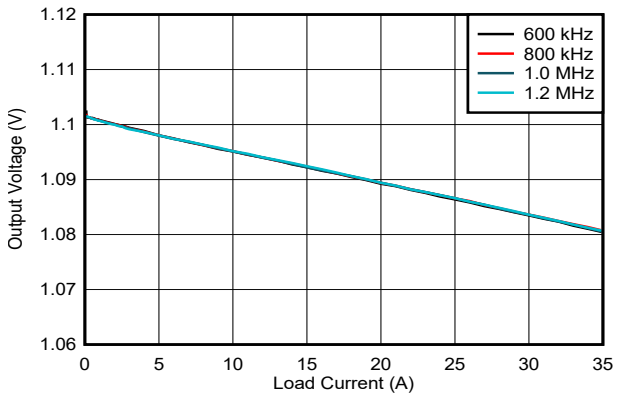
PVIN = 12 V
DC Load Line (DCLL) = 0.75 mΩ

図 8-9. Load Regulation, FCCM, External 5-V Bias



PVIN = 12 V
DC Load Line (DCLL) = 0.75 mΩ

図 8-10. Load Regulation, DCM, Internal VCC LDO



PVIN = 12 V
DC Load Line (DCLL) = 0.75 mΩ

図 8-11. Load Regulation, DCM, External 5-V Bias

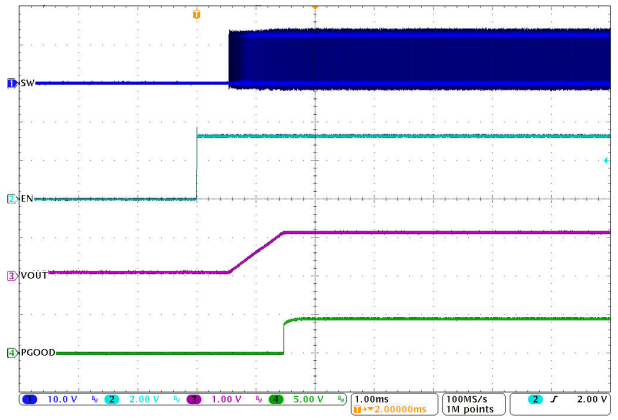


図 8-12. ENABLE Start-Up Waveform

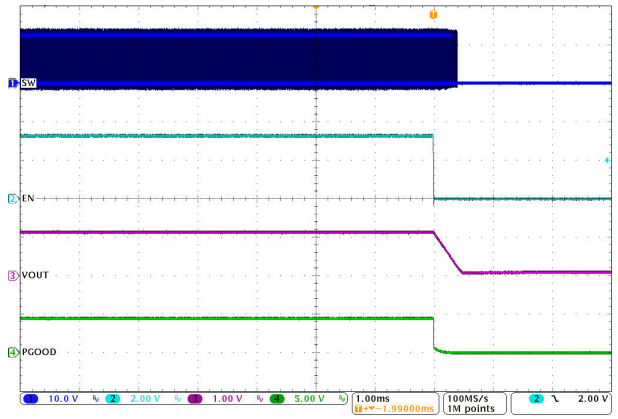


図 8-13. ENABLE Shutdown Waveform

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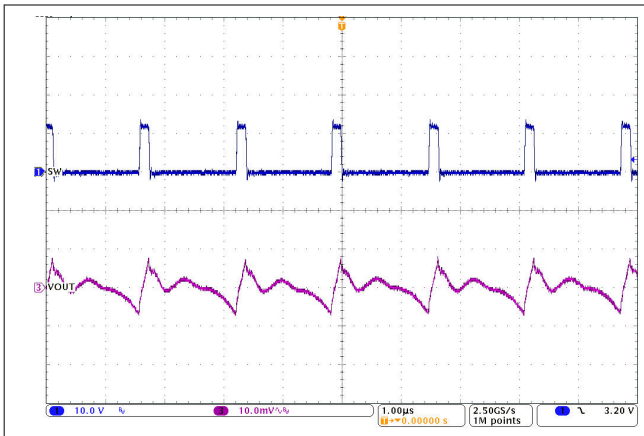


図 8-14. Output Voltage Ripple, 600 kHz FCCM, 35-A Load

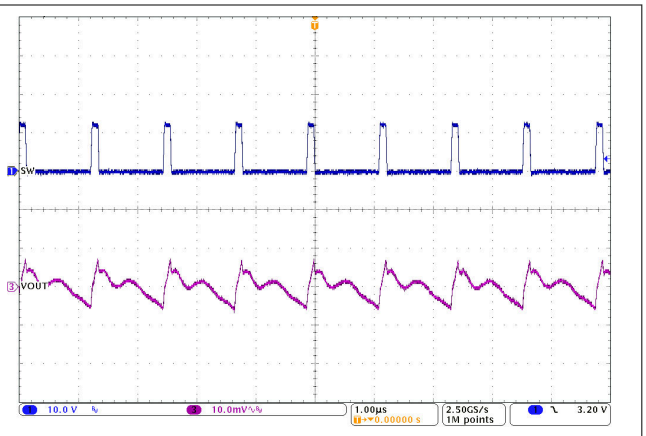


図 8-15. Output Voltage Ripple, 800 kHz FCCM, 35-A Load

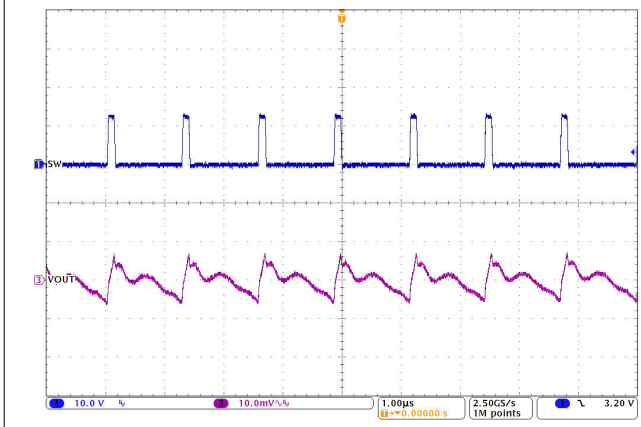


図 8-16. Output Voltage Ripple, FCCM, No load

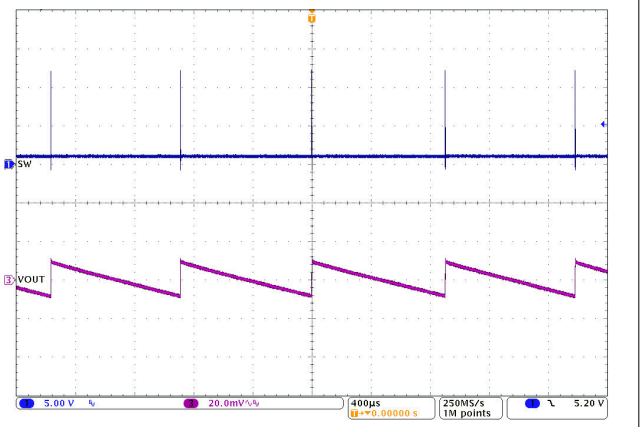


図 8-17. Output Voltage Ripple, DCM, No load

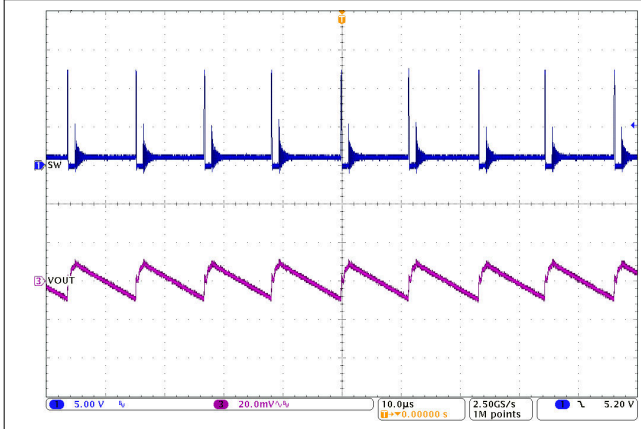


図 8-18. Output Voltage Ripple, DCM, 500-mA Load

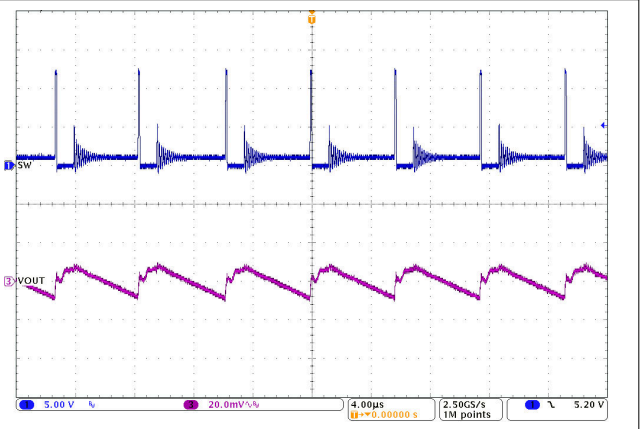


図 8-19. Output Voltage Ripple, DCM, 1-A Load

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The device is designed to operate from a wide input voltage supply range between 2.7 V and 16 V when the VCC/VDRV pin is powered by an external bias ranging from 4.75 V to 5.3 V. Both input supplies (PVIN and VCC bias) must be well regulated. Proper bypassing of input supplies (PVIN and VCC/VDRV) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *Layout Guidelines*.

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ADVANCE INFORMATION

8.4 Layout

8.4.1 Layout Guidelines

Layout is critical for good power-supply design. Layout example shows the recommended PCB-layout configuration. A list of PCB layout considerations using the device is listed as follows:

- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- PVIN-to-PGND decoupling capacitors are important for FET robustness. Besides the large volume 0603 or 0805 ceramic capacitors, TI highly recommends a 0.1-µF 0402 ceramic capacitor with 25 V / X7R rating on PVIN pin 20 (top layer) to bypass any high frequency current in PVIN to PGND loop. The 25-V rating is recommended but can be lowered to 16-V rating for an application with tightly regulated 12-V input bus.
- When one or more PVIN-to-PGND decoupling capacitors are placed on bottom layer, extra impedance is introduced to bypass IC PVIN node to IC PGND node. Placing at least 3 times PVIN vias on PVIN pad (formed by pin 20 to pin 24) and at least 9 times PGND vias on the thermal pad (underneath of the IC) is important to minimize the extra impedance for the bottom layer bypass capacitors.
- Except the PGND vias underneath the thermal pad, at least 4 PGND vias are required to be placed as close as possible to the PGND pin 7 to pin 10. At least 2 PGND vias are required to be placed as close as possible to the PGND pin 19. Thisaction minimizes PGND bounces and also lowers thermal resistance.
- Place the VCC/VDRV-to-PGND decoupling capacitor as close as possible to the device. TI recommends a2.2-µF/6.3-V/X7R/0603 or 4.7-µF/6.3-V/X6S/0603 ceramic capacitor. The voltage rating of this bypass capacitor must be at least 6.3 V but no more than 10 V to lower ESR and ESL. The recommended capacitor size is 0603 to minimize the capacitance drop due to DC bias effect. Ensure the VCC/VDRV to PGND decoupling loop is the smallest and ensure the routing trace is wide enough to lower impedance.
- For remote sensing, the connections from the VOSNS/GOSNS pins to the remote location must be a pair of PCB traces with at least 12 mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher. The ground connection of the remote sensing signal must be connected to GOSNS pin. The VOUT connection of the remote sensing signal must be connected to the VOSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. And TI recommends to shield the pair of remote sensing lines with ground planes above and below.
- For single-end sensing, connect the VOSNS pin to a high-frequency local bypass capacitor of 0.1 µF or higher, and short GOSNS to AGND with shortest trace.
- To minimize the impact from switching noise and achieve high accuracy on the input power monitoring feature, a PGND referenced bypass capacitor is required for each of VINSENP and VINSENM pins, with at least 100-pF volume and at least 25-V rating. These bypass capacitors must be placed close to VINSENP or VINSENM pin accordingly.
- In a case that the input power feature is not used, follow below connection for pin 3 VINSENP and pin 4 VINSENM so that the device can report the input voltage level on PVIN node:
  1. Short pin 3 VINSENP to pin 4 VINSENM,
  2. Place a 0.1 µF ceramic bypass capacitor on pin 4 VINSENM referring to AGND,
  3. Connect pin 4 VINSENM to PVIN node of TPS544C26 device.
- The AGND pin 32 must be connected to a solid PGND plane. TI recommends to place two AGND vias close to pin 32 to route AGND from top layer to bottom layer, and then connect the AGND trace to the PGND vias (underneath IC) through either a net-tie or a 0 Ω resistor on the bottom layer.
- Connecting a resistor from pin 29 (I^2C_ADDR) to AGND sets I^2C address. It is required not to have any capacitor on pin 29. A capacitor on pin 29 likely leads to a wrong detection result for I^2C address.
- Pin 6 (DNC) is a Do-Not-Connect pin. Pin 6 can be shorted to pin 37, which is an NC pin (No internal Connection). Do not connect pin 6 to any other net including ground.

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8.4.2 Layout Example

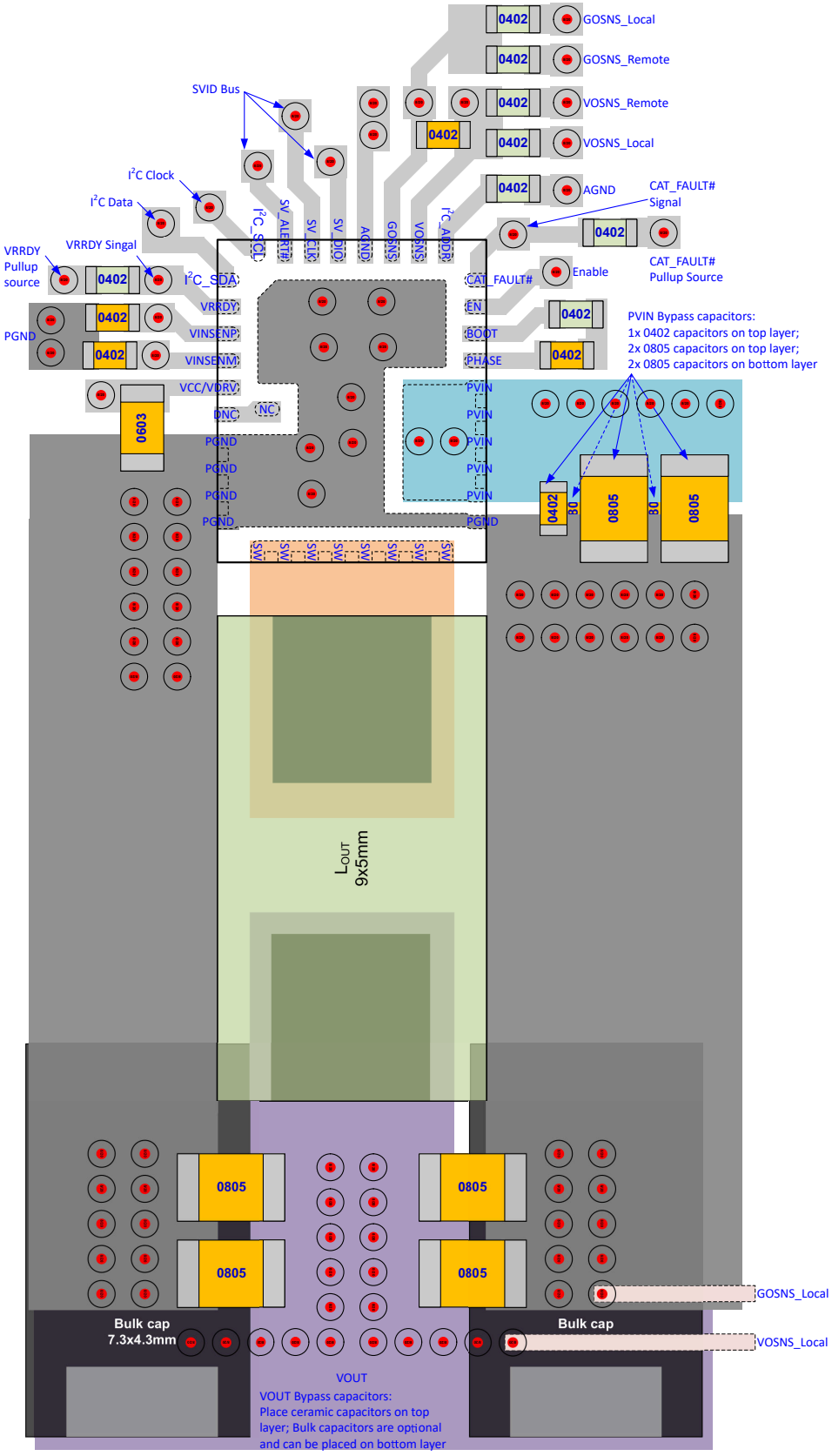


図 8-20. Layout Recommendation

ADVANCE INFORMATION

8.4.2.1 Thermal Performance on TPS544C26EVM

Below are thermal results captured on the TPS544C26EVM with PVIN = 12 V, V_{OUT} = 1.1 V conditions.

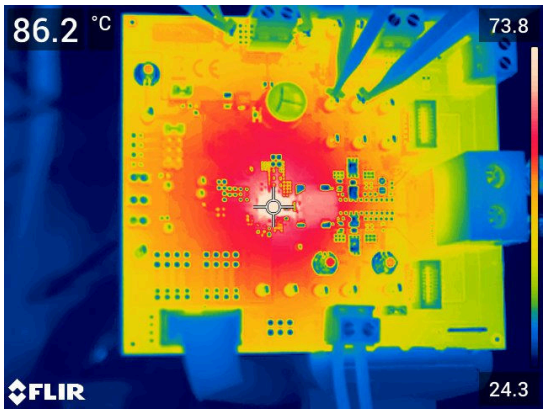


図 8-21. Thermal Characteristics, 600 kHz FCCM, Internal LDO, 35 A Load

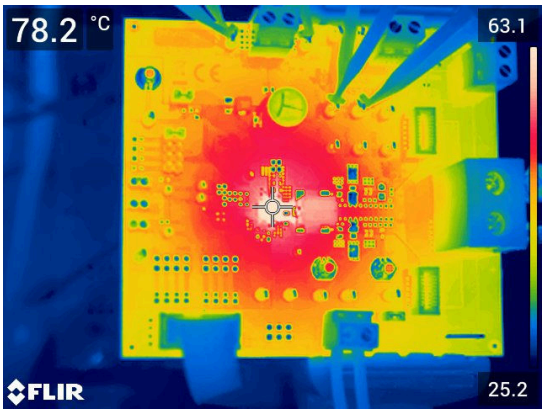


図 8-22. Thermal Characteristics, 600 kHz FCCM, External 5-V Bias, 35-A Load

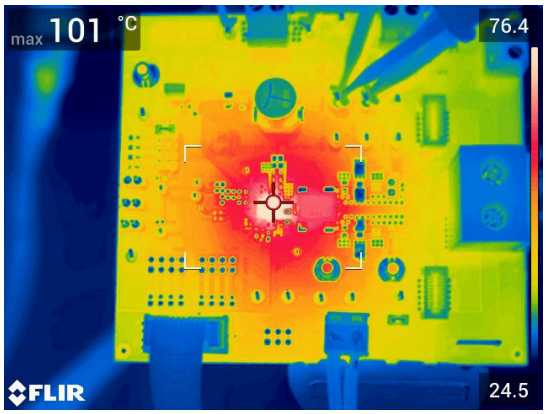


図 8-23. Thermal Characteristics, 800 kHz FCCM, Internal LDO, 35-A Load

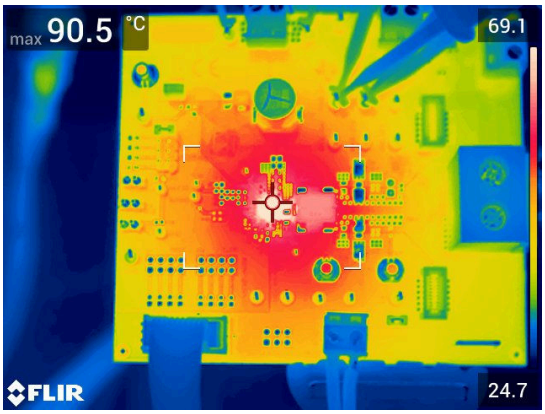


図 8-24. Thermal Characteristics, 800 kHz FCCM, External 5-V Bias, 35-A Load

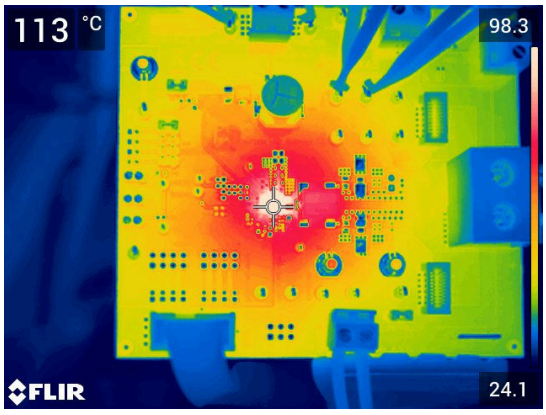


図 8-25. Thermal Characteristics, 1.2-MHz FCCM, Internal LDO, 35-A Load

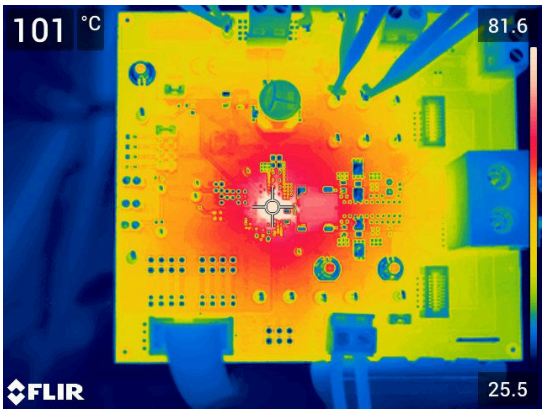


図 8-26. Thermal Characteristics, 1.2-MHz FCCM, External 5-V Bias, 35-A Load

ADVANCE INFORMATION

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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Intel® is a registered trademark of Intel.
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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

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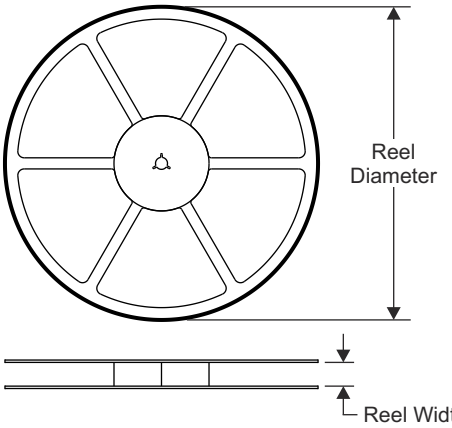
ADVANCE INFORMATION

10 Mechanical, Packaging, and Orderable Information

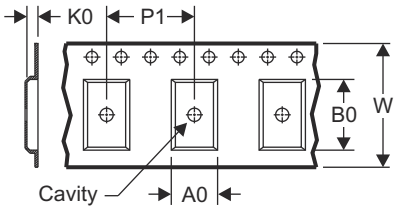
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

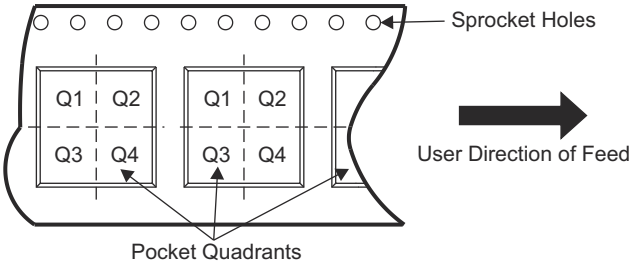


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

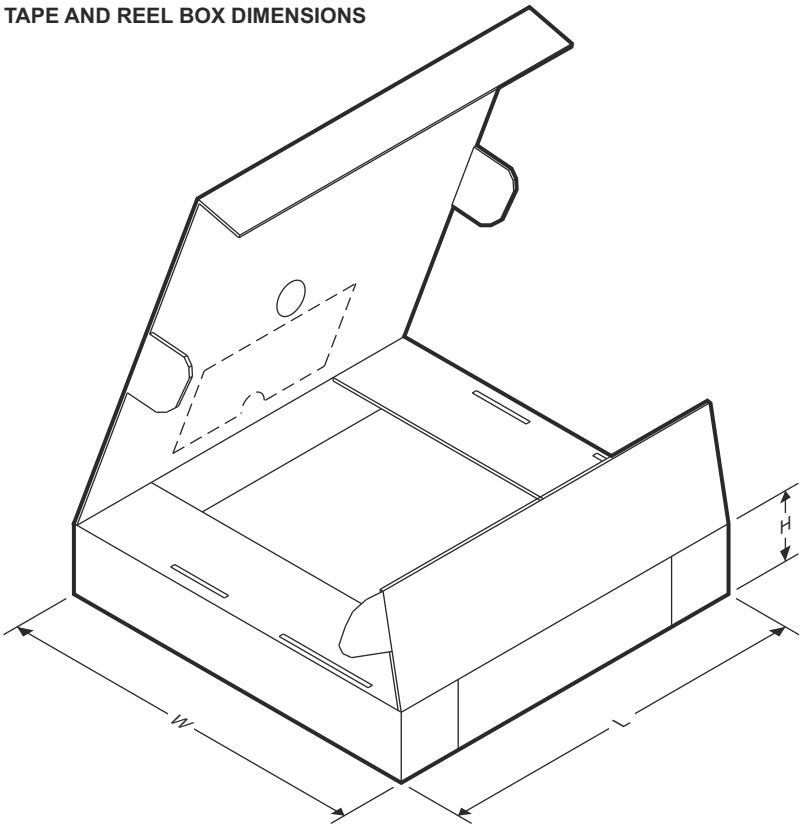
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS544C26RXXR	WQFN-FCRLF	RXX	37	3000	330.0	12.0	5.25	6.3	1.0	8.0	12.0	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS544C26RXXR	WQFN-FCRLF	RXX	37	3000	355.0	338.0	35.0

ADVANCE INFORMATION

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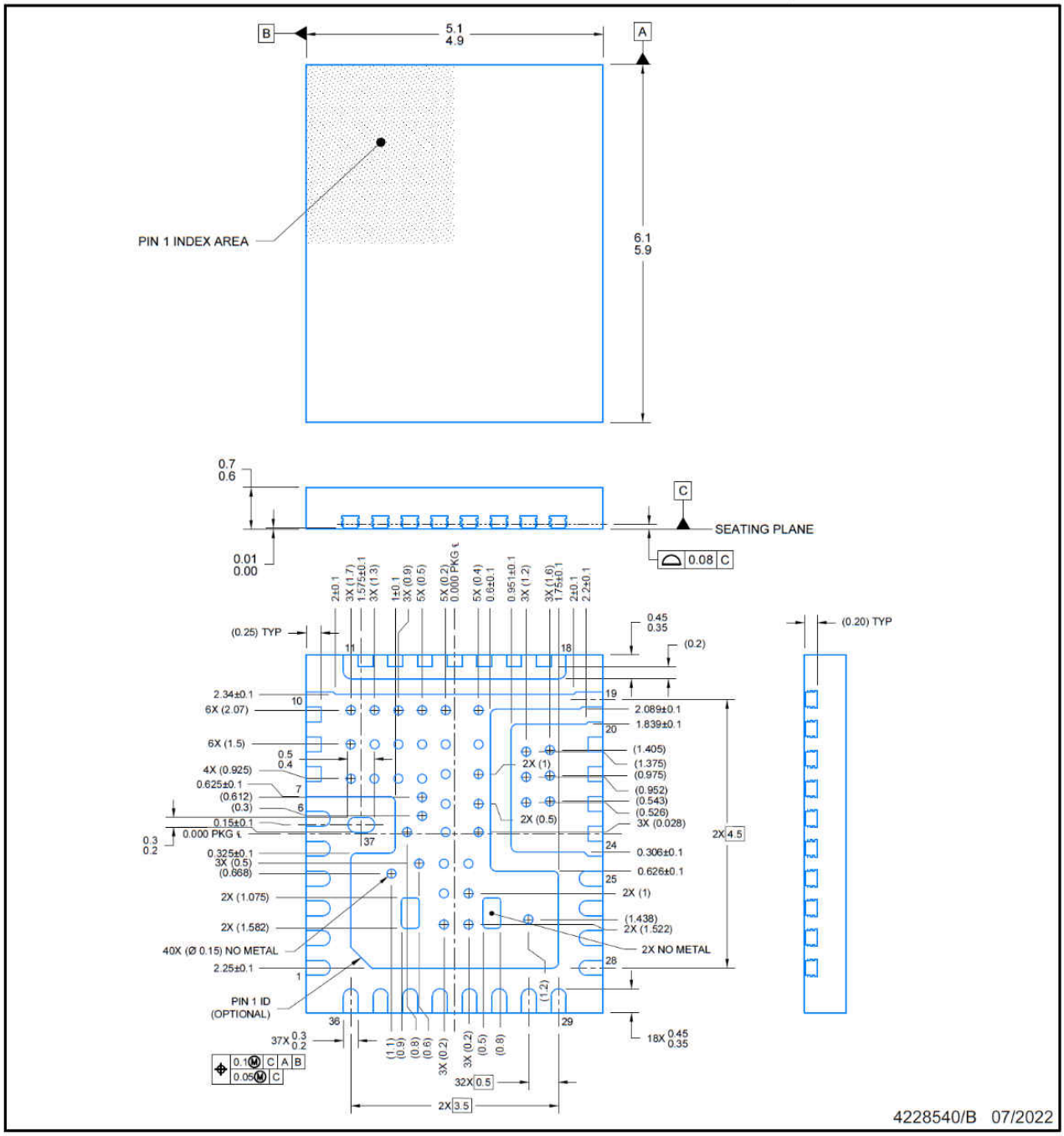
ADVANCE INFORMATION

PACKAGE OUTLINE

RXX0037B

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

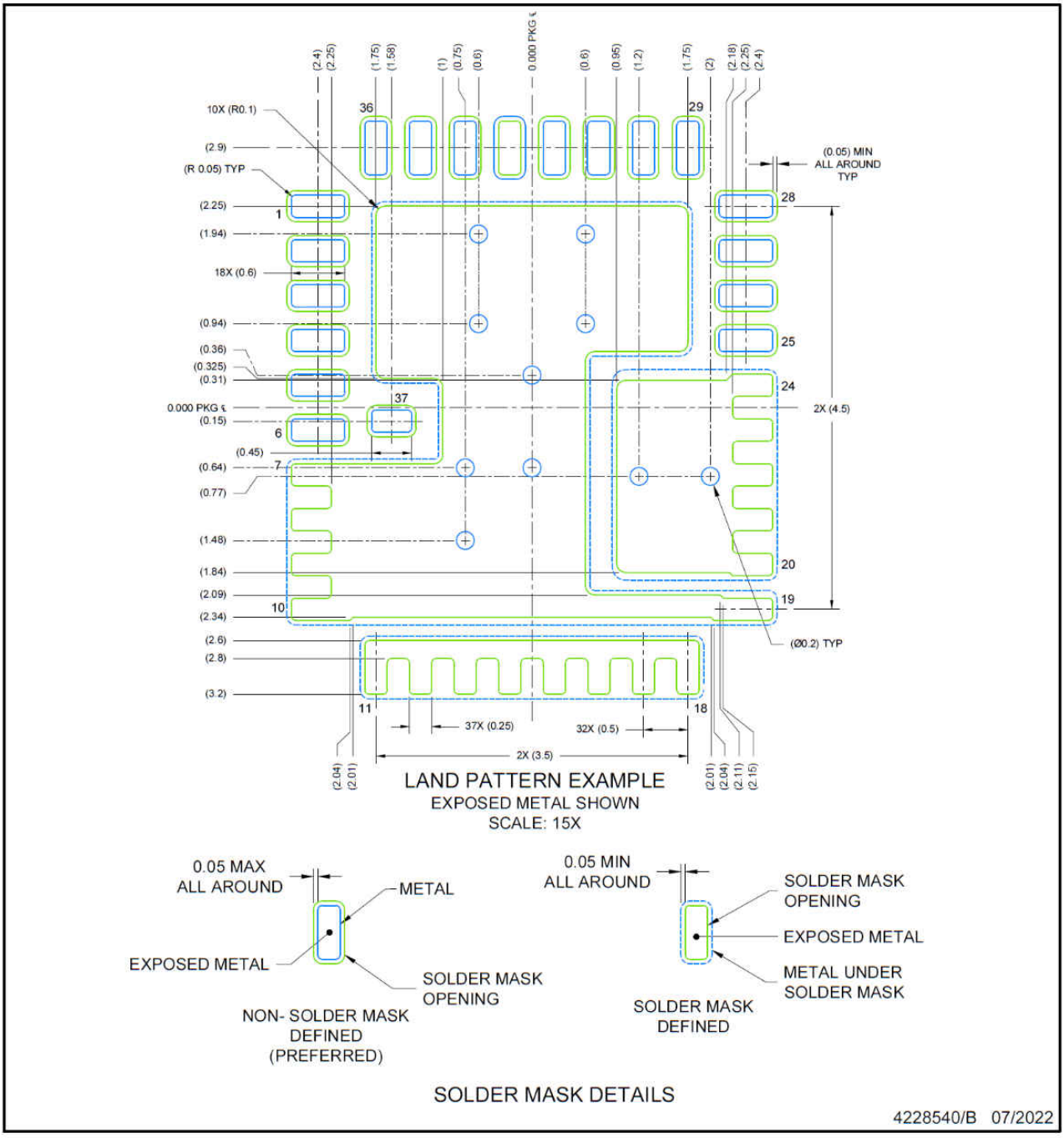
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EXAMPLE BOARD LAYOUT

RXX0037B

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

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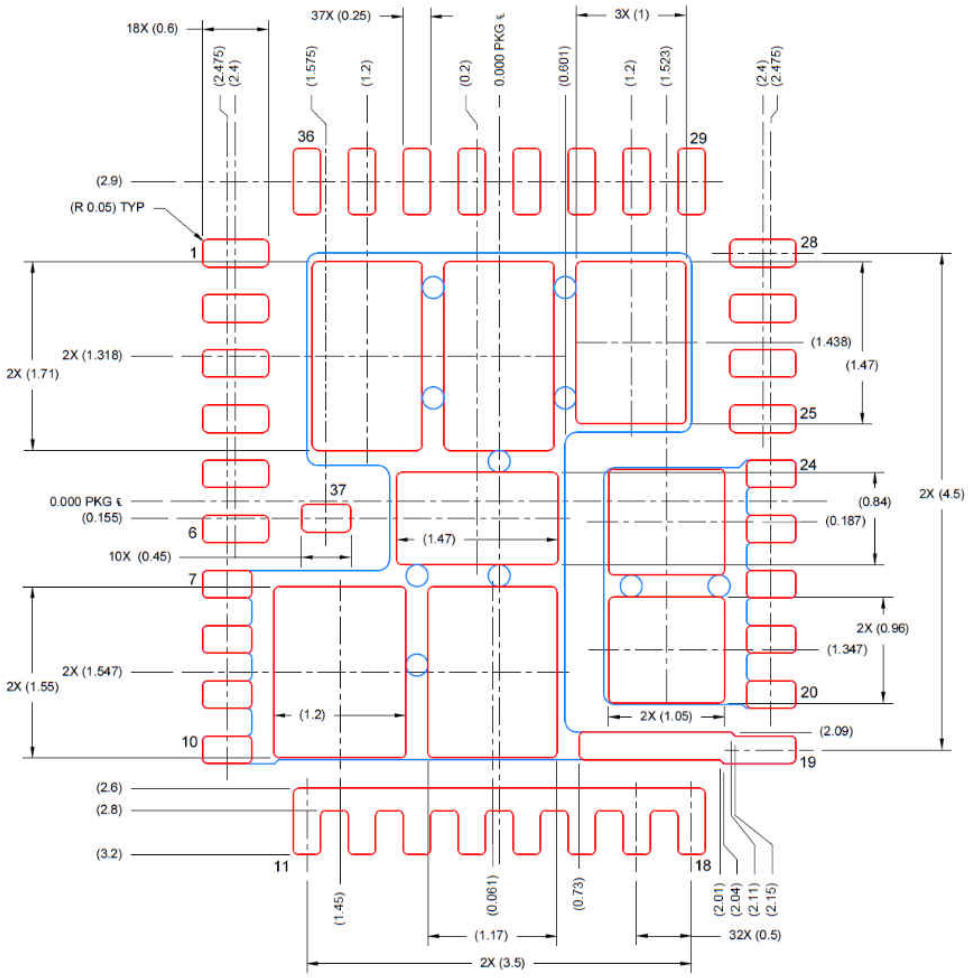
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RXX0037B

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE BY AREA UNDER PACKAGE :
THERMAL PAD CONNECTED TO PINS 7-10 &19: 80%
THERMAL PAD CONNECTED TO PINS 20-24: 86%
SCALE: 15X

4228540/B 07/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS544C26RXXR	Active	Production	WQFN-FCRLF (RXX) | 37	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	544C26
TPS544C26RXXR.A	Active	Production	WQFN-FCRLF (RXX) | 37	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	544C26

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

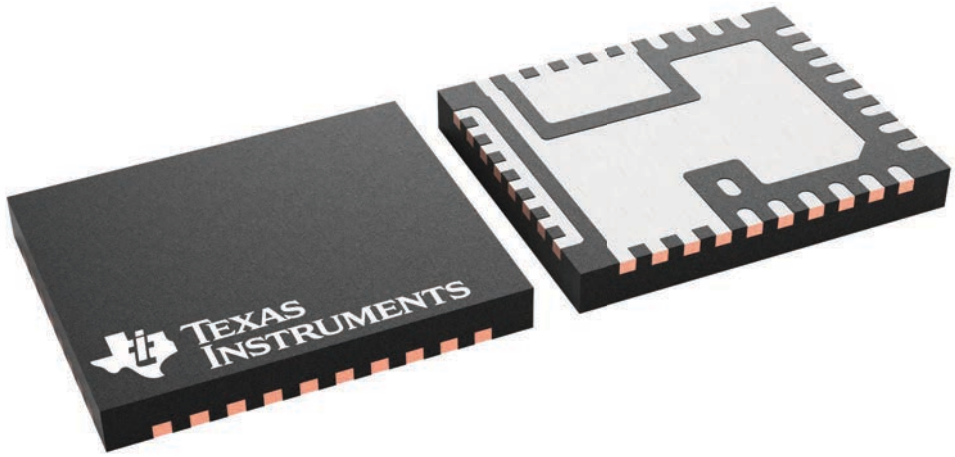
RXX 37

VQFN-FCRLF - 1.05 mm max height

5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



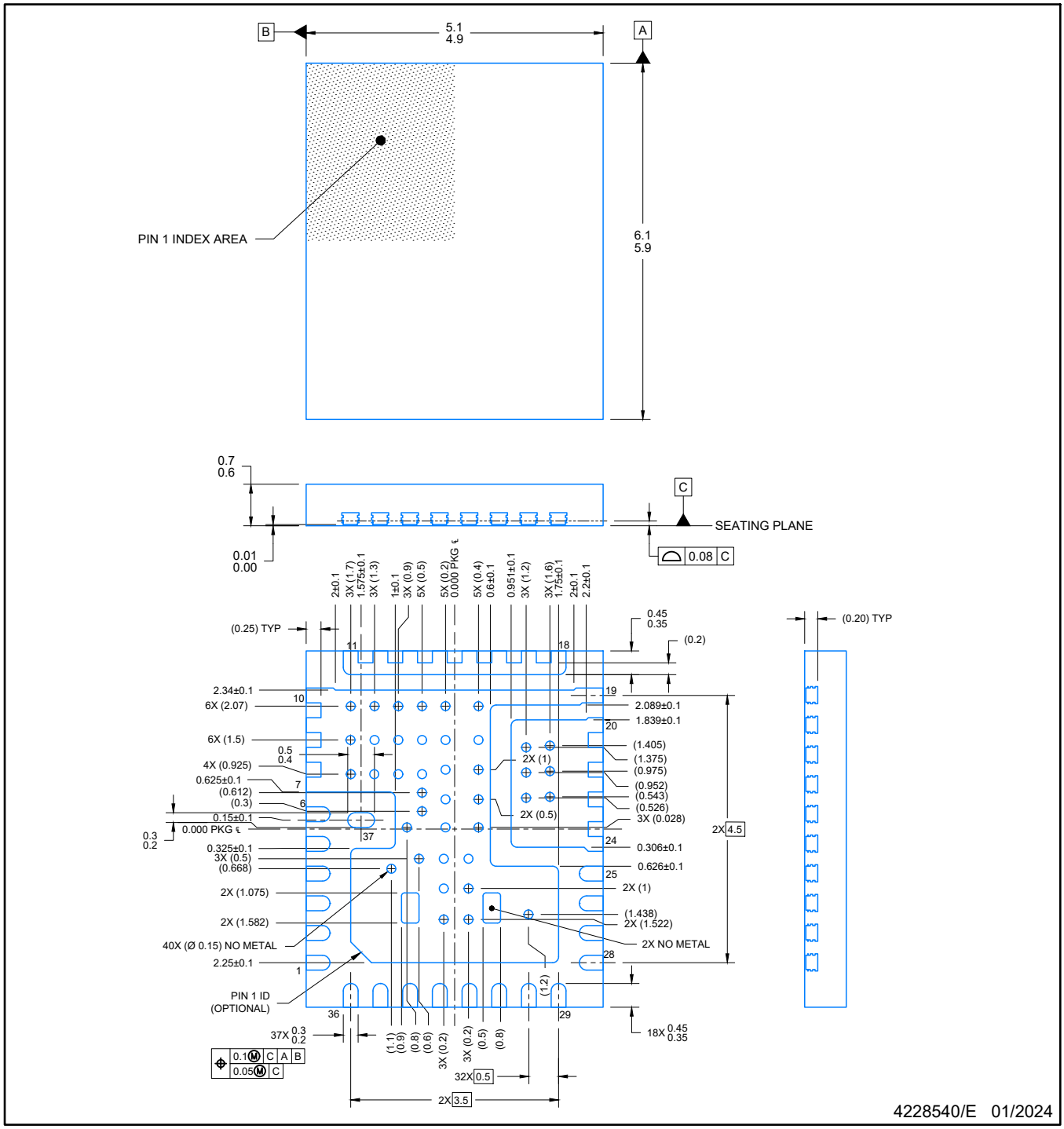
4228557/A

PACKAGE OUTLINE

RXX0037B

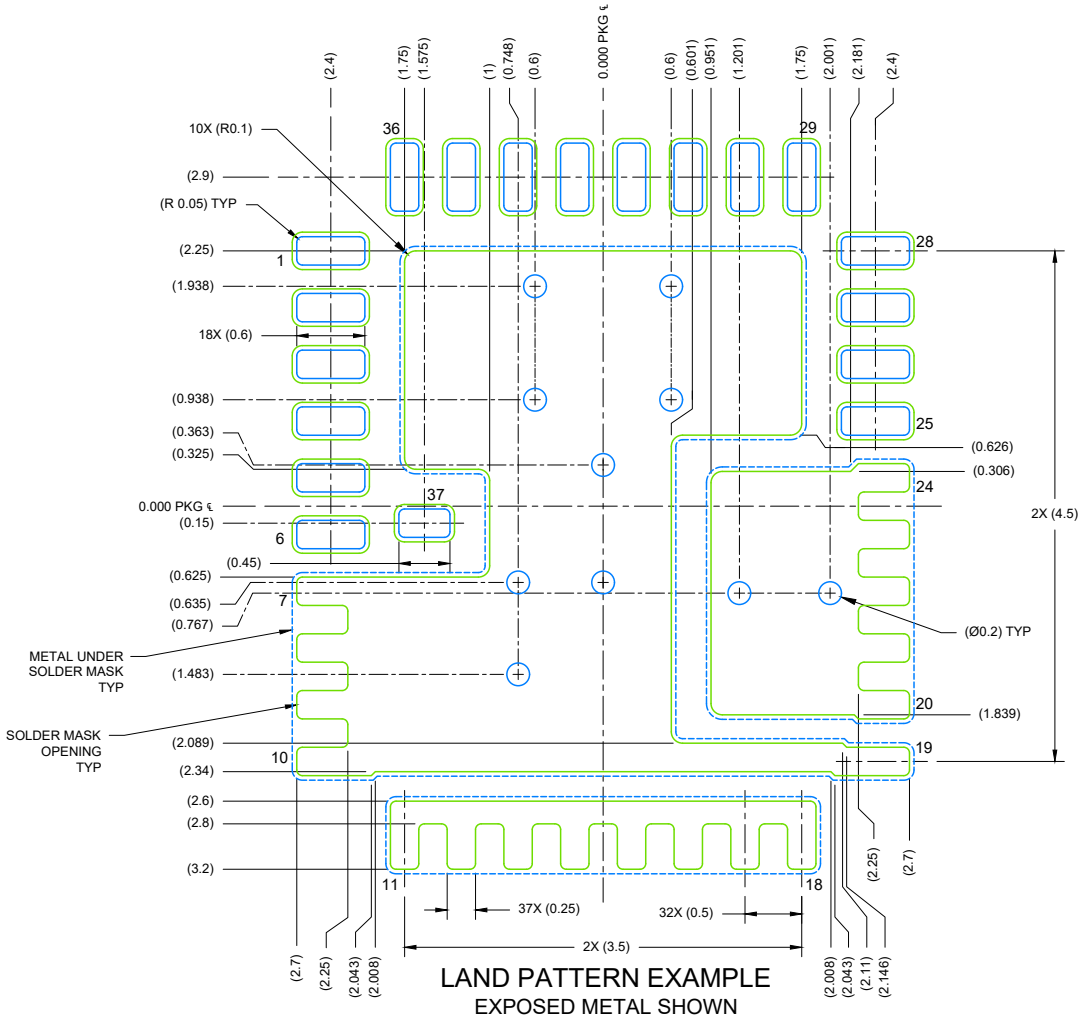
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

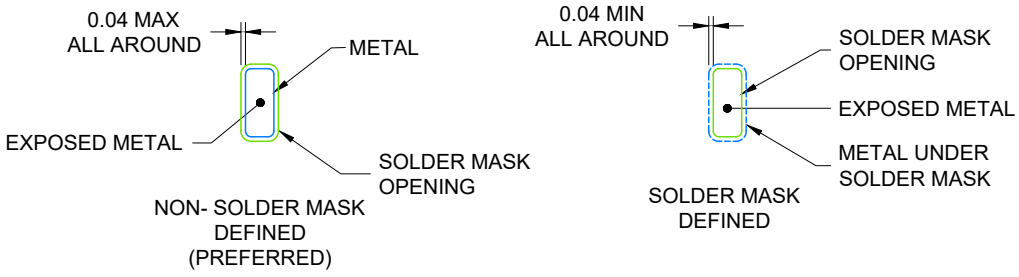
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 15X

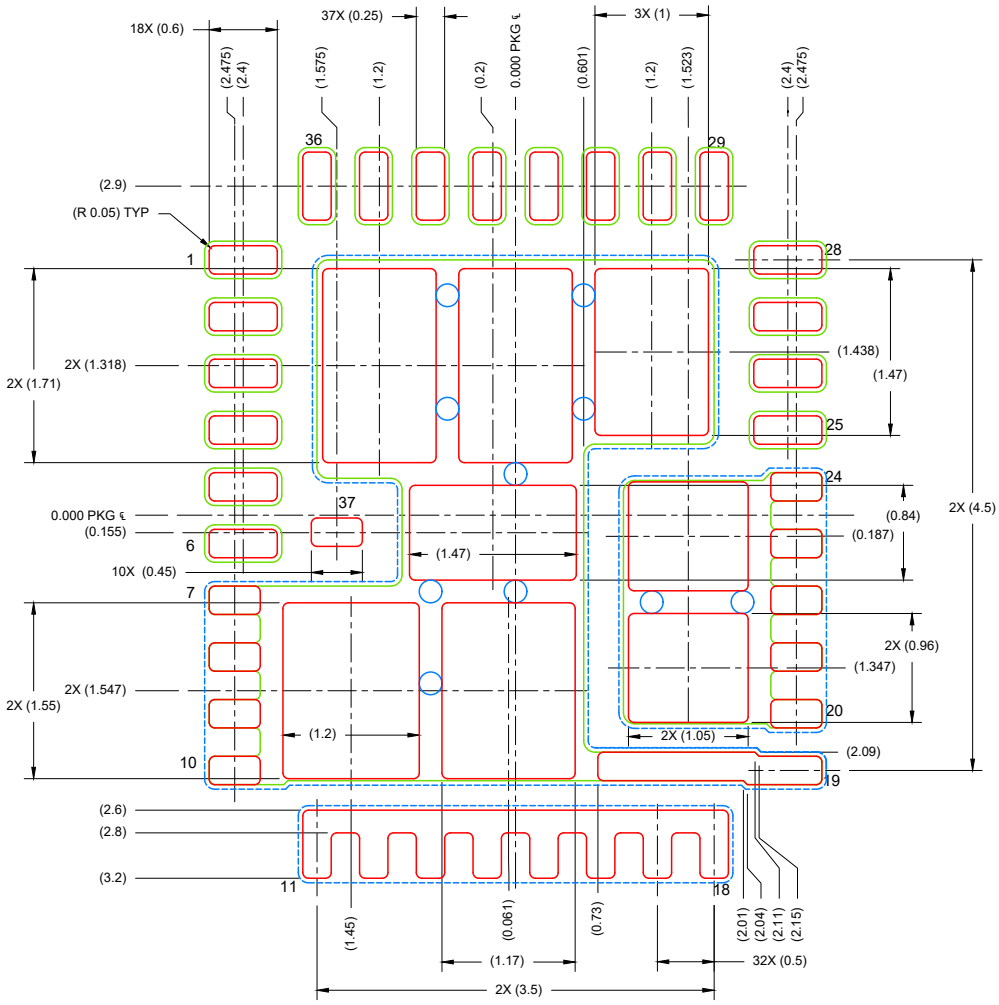


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Recommended board layout is designed for 2oz copper for high current applications.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE BY AREA UNDER PACKAGE :
THERMAL PAD CONNECTED TO PINS 7-10 &19: 80%
THERMAL PAD CONNECTED TO PINS 20-24: 86%
SCALE: 15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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