# TPS54527 4.5V～18V入力、5A、同期整流降圧型コンバータ

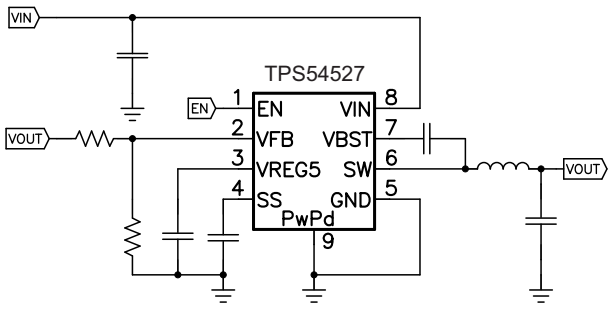
## 1 特長

- D-CAP2™モードにより高速な過渡応答が可能
- 低出力リップル、セラミック出力コンデンサを使用可能
- 広い入力電圧範囲: 4.5V～18V
- 出力電圧範囲: 0.76V～6V
- 低デューティ・サイクルのアプリケーションに対して最適化された高効率の内蔵FET: 65mΩ (ハイサイド)および36mΩ (ローサイド)
- 高効率、シャットダウン時10μA未満
- 高い初期バンドギャップ・リファレンス精度
- 調整可能なソフト・スタート
- プリバイアス付きのソフト・スタート
- 650kHzのスイッチング周波数
- サイクル単位の過電流制限

## 2 アプリケーション

- 幅広い範囲の低電圧システム用アプリケーション
  - デジタル・テレビ用電源
  - 高精細 Blu-ray Disc™プレーヤー
  - ネットワーク・ホーム・ターミナル
  - デジタル・セットトップ・ボックス(STB)

### 概略回路図




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## 3 概要

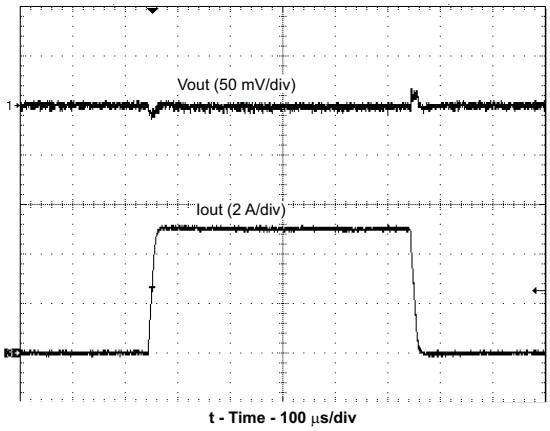
TPS54527は、適応型オン時間D-CAP2モードに対応した同期整流降圧型コンバータです。システム設計者がTPS54527を採用することで、各種の最終機器の電源バス・レギュレータに対して、コスト効果が高く、部品数の少ない、低スタンバイ電流のソリューションを実現できます。TPS54527の主制御ループではD-CAP2モード制御を使用し、外部補償部品なしで高速な過渡応答が得られます。また、TPS54527には、POSCAPやSP-CAPなどの低ESR (等価直列抵抗)出力コンデンサだけでなく、超低ESRのセラミック・コンデンサにも対応できる、独自の回路が採用されています。このデバイスは、4.5V～18Vの入力電圧で動作します。出力電圧は、0.76Vから6Vの範囲でプログラムできます。このデバイスは、ソフトスタート時間も調整可能です。TPS54527は8ピンのDDAパッケージで利用でき、-40℃～85℃の温度範囲で動作するよう設計されています。

### 製品情報(1)

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| TPS54527 | SO PowerPAD (8) | 4.89mm×3.90mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

### 負荷過渡応答




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision C (May 2012) から Revision D に変更** **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- データシートの末尾にあるPOAを参照し、「*注文情報*」表を 削除 ... 1

**Revision B (January 2012) から Revision C に変更** **Page**

- Changed $t_{OFF(MIN)}$ From: 310 ns To: 330 ns ... 5

**Revision A (November 2011) から Revision B に変更** **Page**

- Changed equation 1 denominator from 2 to 6 ... 8

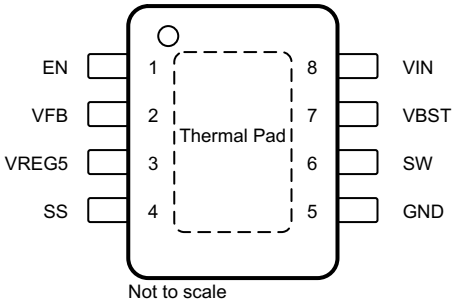
**2011年7月発行のものから更新** **Page**

- Changed pinout drawing to correct pins 5, 6, 7, 8 location ... 3


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# 5 Pin Configuration and Functions

**DDA Package**
**8-Pin SO PowerPAD**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 1 | I | Enable input control. EN is active high and must be pulled up to enable the device. |
| VFB | 2 | I | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| VREG5 | 3 | O | 5.5-V power supply output. A capacitor (typically 1 µF) must be connected to GND. VREG5 is not active when EN is low. |
| SS | 4 | I | Soft-start control. An external capacitor must be connected to GND. |
| GND | 5 | — | Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point. |
| SW | 6 | O | Switch node connection between high-side NFET and low-side NFET. |
| VBST | 7 | O | Supply input for the high-side FET gate drive circuit. Connect 0.1-µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST. |
| VIN | 8 | I | Input voltage supply pin. |
| Thermal Pad | Back side | — | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN, EN | –0.3 | 20 | V |
| | VBST | –0.3 | 26 | |
| | VBST (10-ns transient) | –0.3 | 28 | |
| | VBST (vs SW) | –0.3 | 6.5 | |
| | VFB, SS | –0.3 | 6.5 | |
| | SW | –2 | 20 | |
| | SW (10-ns transient) | –3 | 22 | |
| Output voltage | VREG5 | –0.3 | 6.5 | V |
| | GND | –0.3 | 0.3 | |
| Voltage from GND to thermal pad, $V_{diff}$ | | –0.2 | 0.2 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage | | 4.5 | 18 | V |
| | Input voltage | VBST | –0.1 | 24 | V |
| | | VBST (10 ns transient) | –0.1 | 27 | |
| | | VBST(vs SW) | –0.1 | 5.7 | |
| | | SS | –0.1 | 5.7 | |
| | | EN | –0.1 | 18 | |
| | | VFB | –0.1 | 5.5 | |
| | | SW | –1.8 | 18 | |
| | | SW (10 ns transient) | –3 | 21 | |
| | | GND | –0.1 | 0.1 | |
| $V_{OUT}$ | Output voltage | VREG5 | –0.1 | 5.7 | V |
| $I_{OUT}$ | Output current | $I_{VREG5}$ | 0 | 5 | mA |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | 150 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TPS54527 DDA (SO PowerPAD) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 43.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 49.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 25.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 25.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 5.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 6.5 Electrical Characteristics

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{VIN}$ | Operating non-switching supply current | VIN current, $T_A$ = 25°C, EN = 5 V, $V_{FB}$ = 0.8 V | | 900 | 1400 | µA |
| $I_{VINSDN}$ | Shutdown supply current | VIN current, $T_A$ = 25°C, EN = 0 V | | 3.6 | 10 | µA |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN high-level input voltage | EN | 1.6 | | | V |
| $V_{ENL}$ | EN low-level input voltage | EN | | | 0.6 | V |
| **VFB VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | |
| $V_{FBTH}$ | VFB threshold voltage | $T_A$ = 25°C, $V_{OUT}$ = 1.05 V, continuous mode | 757 | 765 | 773 | mV |
| | | $T_A$ = –40°C to 85°C , $V_{OUT}$ = 1.05 V, continuous mode (1) | 751 | 765 | 779 | mV |
| $I_{VFB}$ | VFB input current | $V_{FB}$ = 0.8 V, $T_A$ = 25°C | | 0 | ±0.15 | µA |
| **VREG5 OUTPUT** | | | | | | |
| $V_{REG5}$ | VREG5 output voltage | $T_A$ = 25°C, 6 V < $V_{IN}$ < 18 V, 0 < $I_{VREG5}$ < 5 mA | 5.2 | 5.5 | 5.7 | V |
| $V_{LN5}$ | Line regulation | 6 V < $V_{IN}$ < 18 V, $I_{VREG5}$ = 5 mA | | | 25 | mV |
| $V_{LD5}$ | Load regulation | 0 mA < $I_{VREG5}$ < 5 mA | | | 100 | mV |
| $I_{VREG5}$ | Output current | $V_{IN}$ = 6 V, $V_{REG5}$ = 4 V, $T_A$ = 25°C | | 60 | | mA |
| **MOSFET** | | | | | | |
| $R_{DS(ON)H}$ | High side switch resistance | $T_A$ = 25°C, $V_{BST}$ – SW = 5.5 V | | 65 | | mΩ |
| $R_{DS(ON)L}$ | Low side switch resistance | $T_A$ = 25°C | | 36 | | mΩ |
| **CURRENT LIMIT** | | | | | | |
| $I_{ocl}$ | Current limit | L out = 1.5 µH (1) | 5.6 | 6.4 | 7.9 | A |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature (1) | | 165 | | °C |
| | | Hysteresis (1) | | 35 | | |
| **SOFT START** | | | | | | |
| $I_{SSC}$ | SS charge current | $V_{SS}$ = 1 V | 4.2 | 6 | 7.8 | µA |
| $I_{SSD}$ | SS discharge current | $V_{SS}$ = 0.5 V | 0.1 | 0.2 | | mA |
| **UVLO** | | | | | | |
| UVLO | UVLO threshold | Wake up VREG5 voltage | 3.45 | 3.75 | 4.05 | V |
| | | Hysteresis VREG5 voltage | 0.19 | 0.32 | 0.45 | |

(1) Not production tested.

## 6.6 Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ON-TIME TIMER CONTROL** | | | | | | |
| $t_{ON}$ | ON time | $V_{IN}$ = 12 V, $V_{OUT}$ = 1.05 V | | 150 | | ns |
| $t_{OFF(MIN)}$ | Minimum OFF time | $T_A$ = 25°C, $V_{FB}$ = 0.7 V | | 260 | 330 | ns |

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## 6.7 Typical Characteristics

$V_{IN}$ = 12 V, $T_A$ = 25°C (unles otherwise noted)

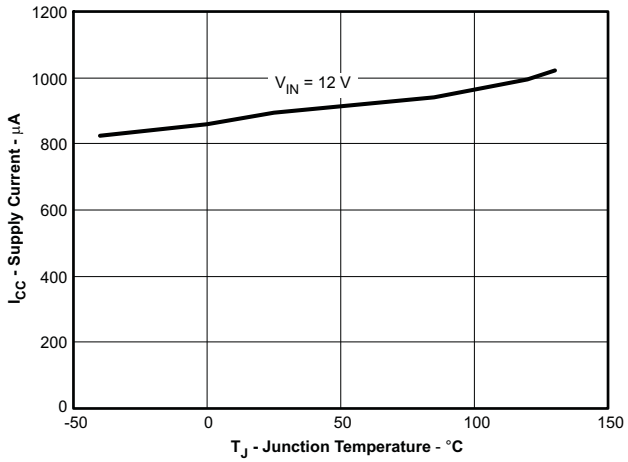



**Figure 1. VIN Current vs Junction Temperature**

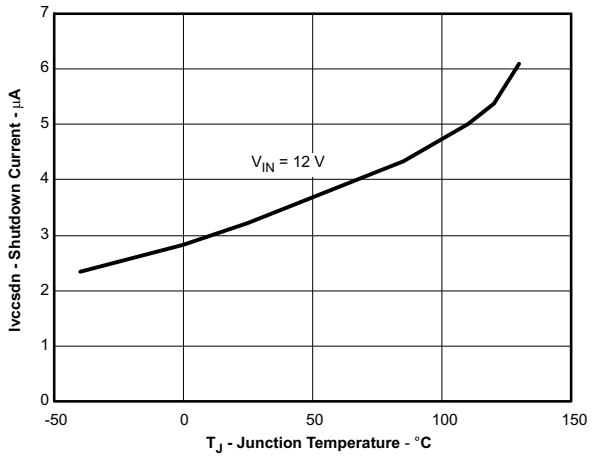



**Figure 2. VIN Shutdown Current vs Junction Temperature**

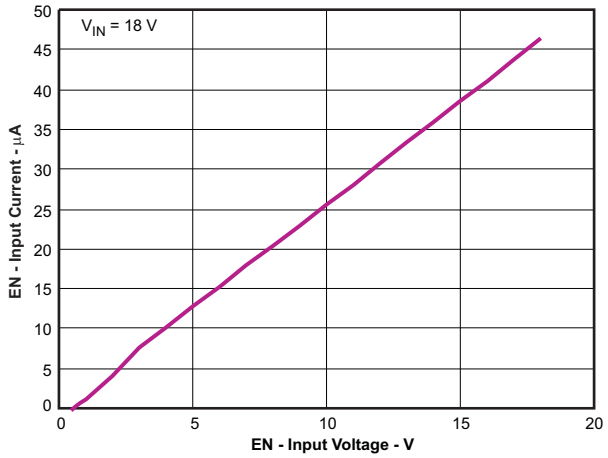



**Figure 3. EN Current vs EN Voltage**

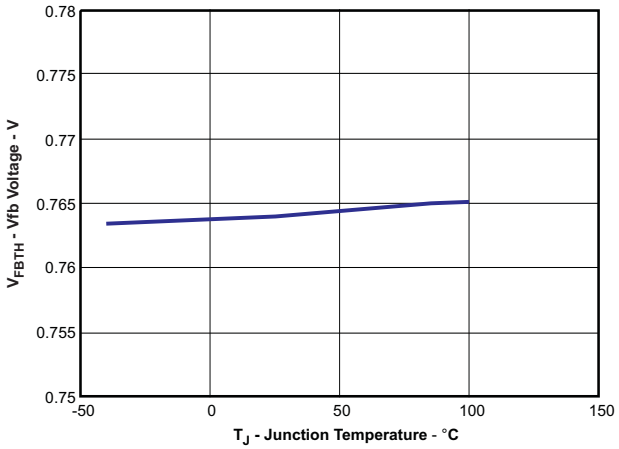



**Figure 4. VFB Voltage vs Junction Temperature**

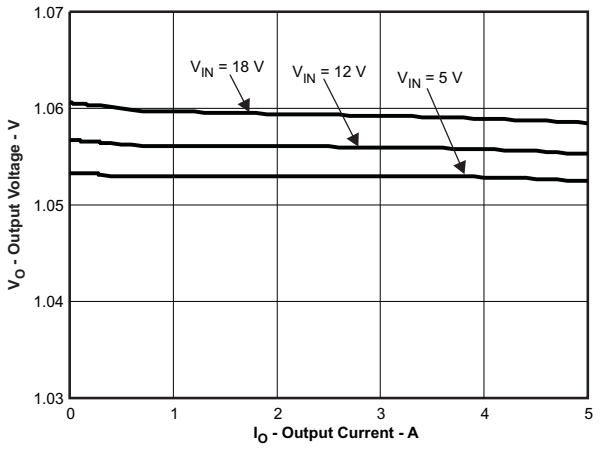



**Figure 5. 1.05-V Output Voltage vs Output Current**

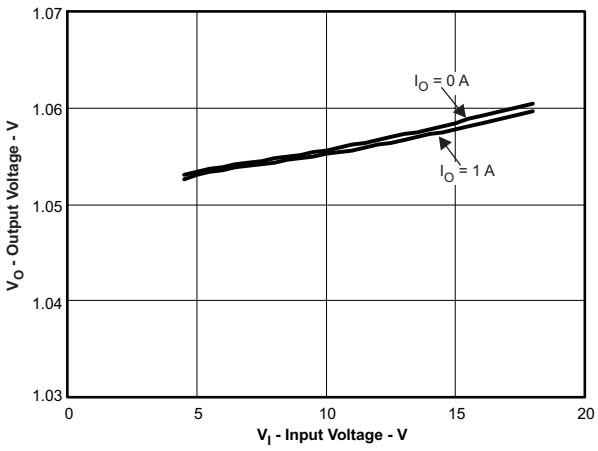



**Figure 6. 1.05-V Output Voltage vs Input Voltage**


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## Typical Characteristics (continued)

$V_{IN}$ = 12 V, $T_A$ = 25°C (unles otherwise noted)

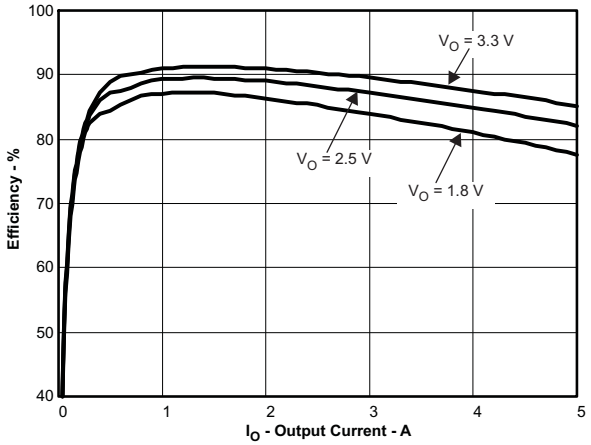



**Figure 7. Efficiency vs Output Current**

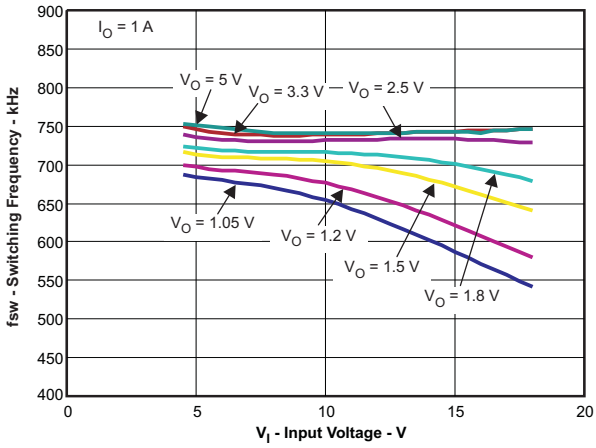



**Figure 8. Switching Frequency vs Input Voltage**

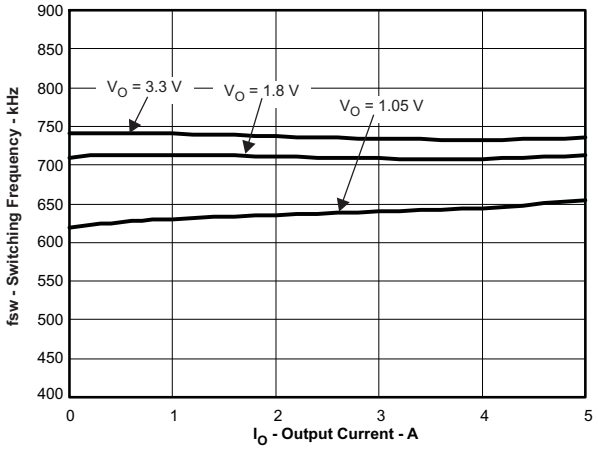



**Figure 9. Switching Frequency vs Output Current**

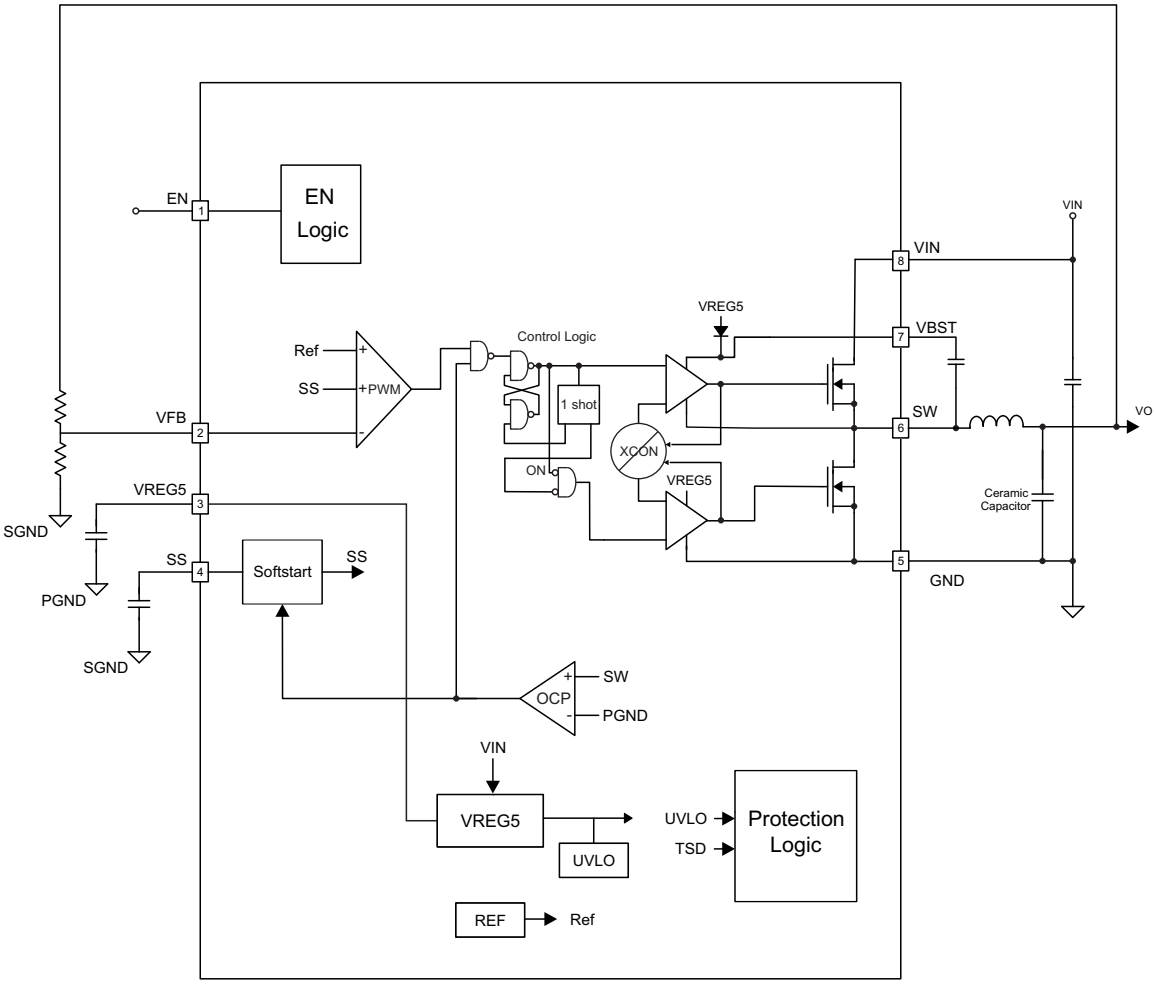
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# 7 Detailed Description

## 7.1 Overview

The TPS54527 is a 5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## 7.2 Functional Block Diagram




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## 7.3 Feature Description

### 7.3.1 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 6-µA.

$$t_{SS}(ms) = \frac{C6(nF) \times V_{FB} \times 1.1}{I_{SS}(\mu A)} = \frac{C6(nF) \times 0.765 \times 1.1}{6} \quad (1)$$


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## Feature Description (continued)

The TPS54527 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage $V_{FB}$), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by 1 – D, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the output voltage ($V_{OUT}$) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### 7.3.2 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current ($I_{OUT}$). The TPS54527 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the over-current threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

### 7.3.3 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54527 is shut off. This protection is non-latching.

### 7.3.4 Thermal Shutdown

TPS54527 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 PWM Operation

The main control loop of the TPS54527 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

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## Device Functional Modes (continued)

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage ($V_{IN}$) and the output voltage ($V_{OUT}$) to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

### 7.4.2 PWM Frequency and Adaptive On-Time Control

TPS54527 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54527 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is $V_{OUT}$ / $V_{IN}$, the frequency is constant.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS54327 is designed to provide up to a 2-A output current from an input voltage source ranging from 4.5 V to 18 V. The output voltage is configuarable from 0.7 V to 6 V.

## 8.2 Typical Application

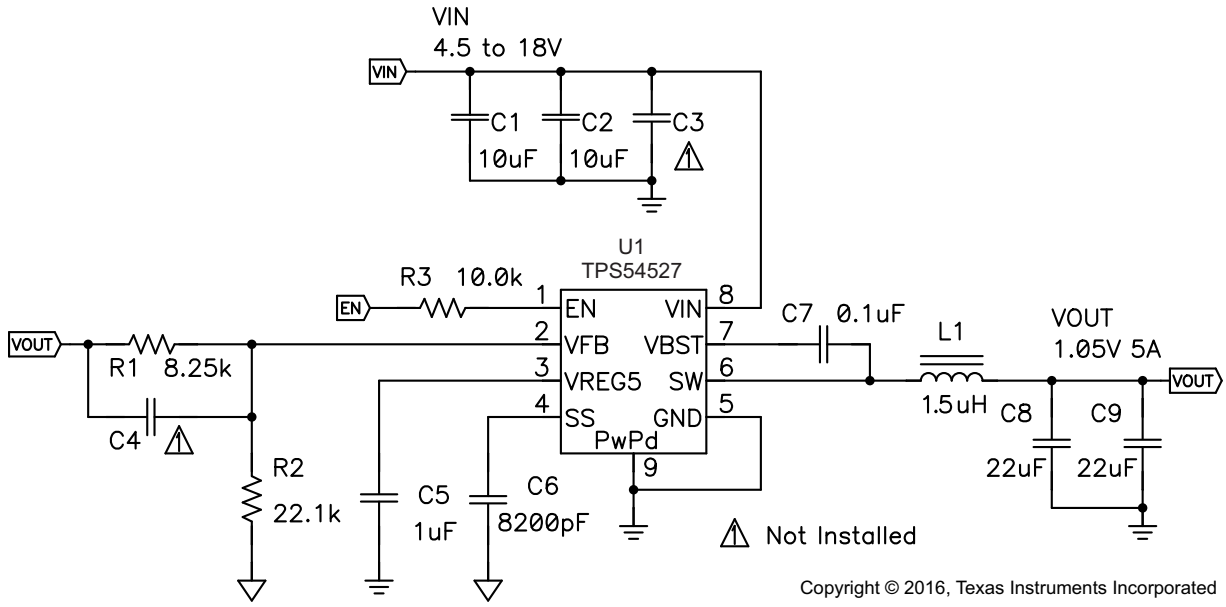



**Figure 10. Shows the schematic diagram for this design example.**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

**Table 1. Design Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 4.5 V to 18 V |
| Output voltage | 1.05 V |
| Output current | 5 A |
| Output voltage ripple | 20 mV |
| Input voltage ripple | 100 mV |

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using a 1% tolerance or better divider resistors. Start by using Equation 2 to calculate $V_{OUT}$.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current is more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

#### 8.2.2.2 Output Filter Selection

The output filter used with the TPS54527 is an LC circuit. This LC filter has a double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54527. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. TI recommends the values in Table 2 to meet this requirement.

**Table 2. Recommended Component Values**

| OUTPUT VOLTAGE (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF)(1) | L1 (µH) | C8 + C9 (µF) |
|---|---|---|---|---|---|
| 1 | 6.81 | 22.1 | — | 1 to 1.5 | 22 to 68 |
| 1.05 | 8.25 | 22.1 | — | 1 to 1.5 | 22 to 68 |
| 1.2 | 12.7 | 22.1 | — | 1 to 1.5 | 22 to 68 |
| 1.5 | 21.5 | 22.1 | — | 1.5 | 22 to 68 |
| 1.8 | 30.1 | 22.1 | 5 to 22 | 1.5 | 22 to 68 |
| 2.5 | 49.9 | 22.1 | 5 to 22 | 2.2 | 22 to 68 |
| 3.3 | 73.2 | 22.1 | 5 to 22 | 2.2 | 22 to 68 |
| 5 | 124 | 22.1 | 5 to 22 | 3.3 | 22 to 68 |

(1) Optional

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for $f_{SW}$.

Use 650 kHz for $f_{SW}$. Chose an inductor that is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{IPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{Ipeak} = I_O + \frac{I_{Ipp}}{2} \quad (5)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{IPP}^2} \quad (6)$$


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For this design example, the calculated peak current is 5.51 A and the calculated RMS current is 5.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54527 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.29 A and each output capacitor is rated for 4 A.

#### 8.2.2.3 Input Capacitor Selection

The TPS54527 requires an input decoupling capacitor and a bulk capacitor is required depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must to be greater than the maximum input voltage.

#### 8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST and SW pins for proper operation. TI recommends using a ceramic capacitor.

#### 8.2.2.5 VREG5 Capacitor Selection

A 1-µF. ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. TI recommends using a ceramic capacitor.

### 8.2.3 Application Curves

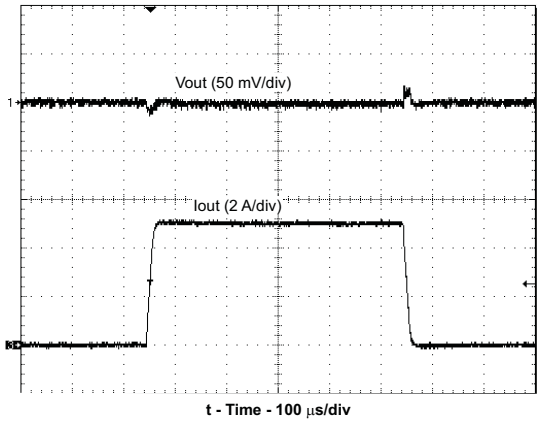



**Figure 11. 1.05-V, 50-mA to 2-A Load Transient Response**

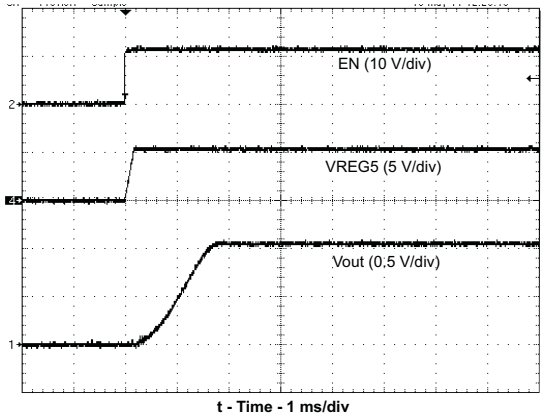
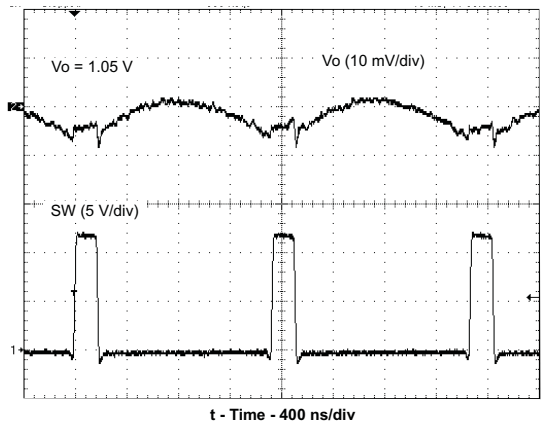
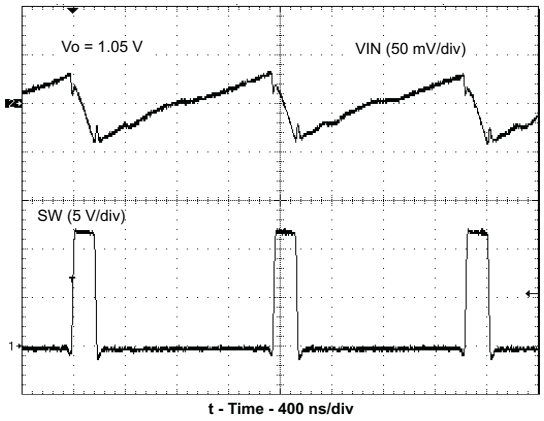



**Figure 12. Start-Up Wave Form**




$I_{OUT}$ = 2 A

**Figure 13. Voltage Ripple at Output**




$I_{OUT}$ = 2 A

**Figure 14. Voltage Ripple at Input**

## 9 Power Supply Recommendations

The input voltage range is from 4.5 V to 18 V. The input power supply and the input capacitors must be placed as close to the device as possible to minimize the impedance of the power-supply line.

## 10 Layout

### 10.1 Layout Guidelines

1. The TPS54527 can supply large load currents up to 5 A, so heat dissipation may be a concern. The top side area adjacent to the TPS54527 must be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC must a dedicated ground area. It must be directly connected to the thermal pad of the device using vias as shown. The ground area must be as large as practical. Additional internal layers can be dedicated as ground planes and connected to the vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor must be placed near the device, and connected PGND.
11. Output capacitor must be connected to a broad pattern of the PGND.
12. Voltage feedback loop must be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin must be tied to SGND.
14. Providing sufficient via is required for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND must be as broad as possible.
16. VIN capacitor must be placed as near as possible to the device.


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## 10.2 Layout Example

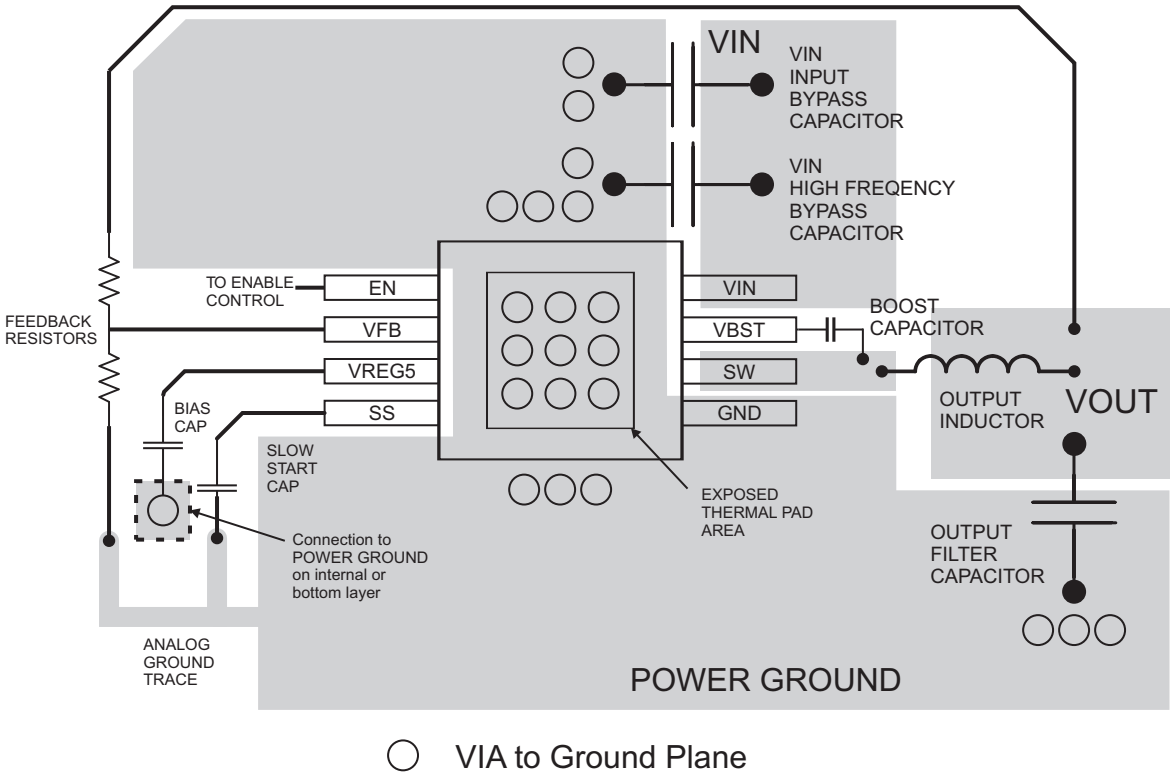



**Figure 15. PCB Layout**

## 10.3 Thermal Consideration

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heat sink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see *PowerPAD Thermally Enhanced Package* and *PowerPAD Made Easy*.

The exposed thermal pad dimensions for this package are shown in Figure 16.

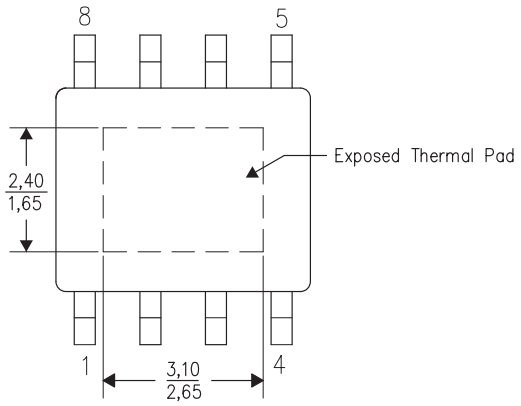



**Figure 16. Thermal Pad Dimensions (Top View)**

# 11 デバイスおよびドキュメントのサポート

## 11.1 ドキュメントのサポート

### 11.1.1 関連資料

関連資料については、以下を参照してください。

- *『放熱特性の優れたPowerPADパッケージ』*(SLMA002)
- *『PowerPADの簡単な使用法』*(SLMA004)

## 11.2 ドキュメントの更新通知を受け取る方法

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## 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS54527DDA | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| BULK | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 54527 |
| TPS54527DDA.A | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| BULK | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54527 |
| TPS54527DDA.B | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| BULK | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54527 |
| TPS54527DDAR | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 54527 |
| TPS54527DDAR.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54527 |
| TPS54527DDAR.B | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54527 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

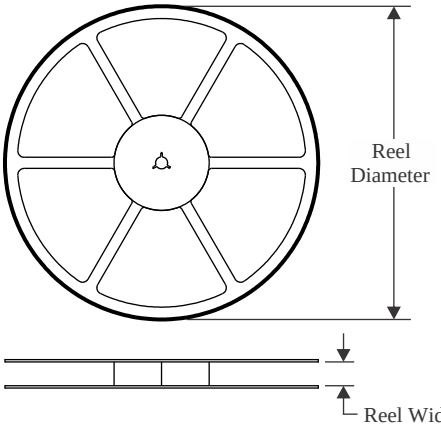
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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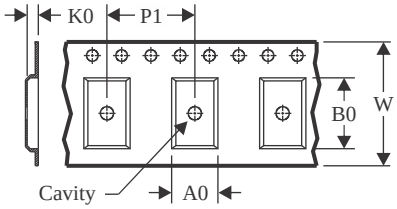
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

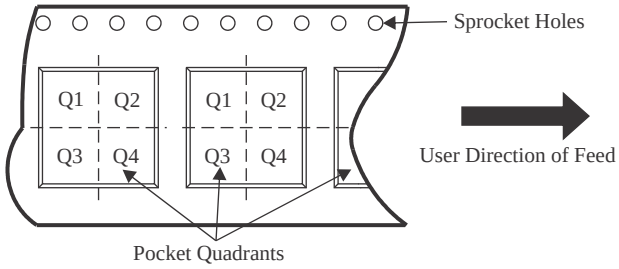



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

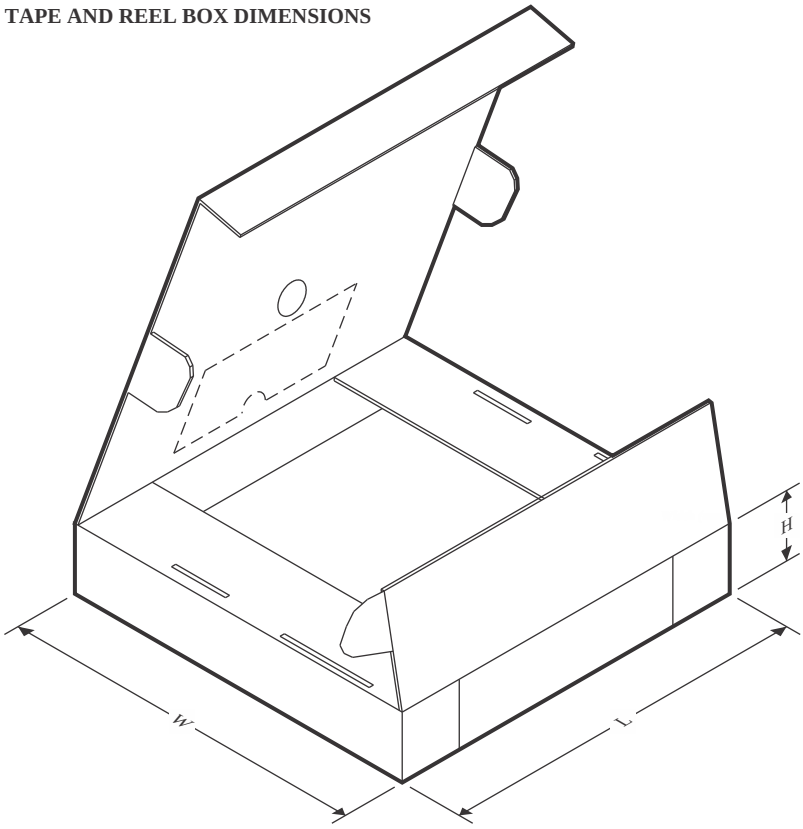
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54527DDAR | SO PowerPAD | DDA | 8 | 2500 | 330.0 | 12.8 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

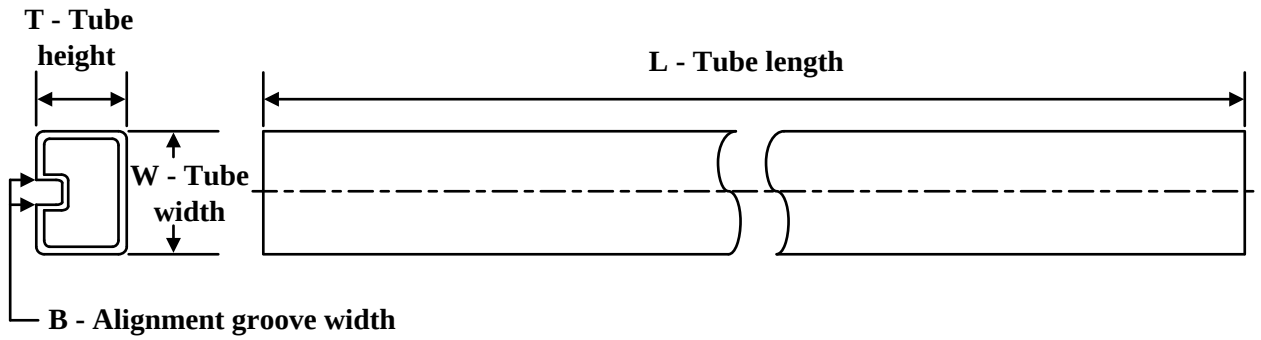
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54527DDAR | SO PowerPAD | DDA | 8 | 2500 | 366.0 | 364.0 | 50.0 |

## TUBE

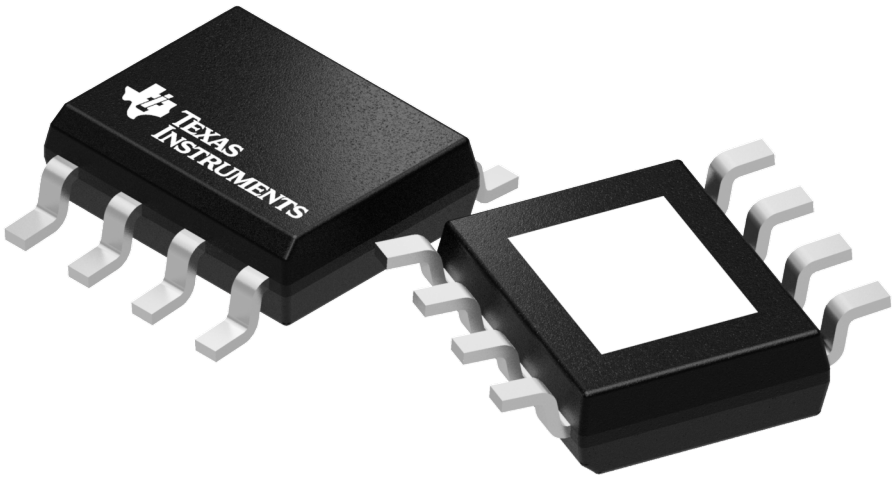



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS54527DDA | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |
| TPS54527DDA.A | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |
| TPS54527DDA.B | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |

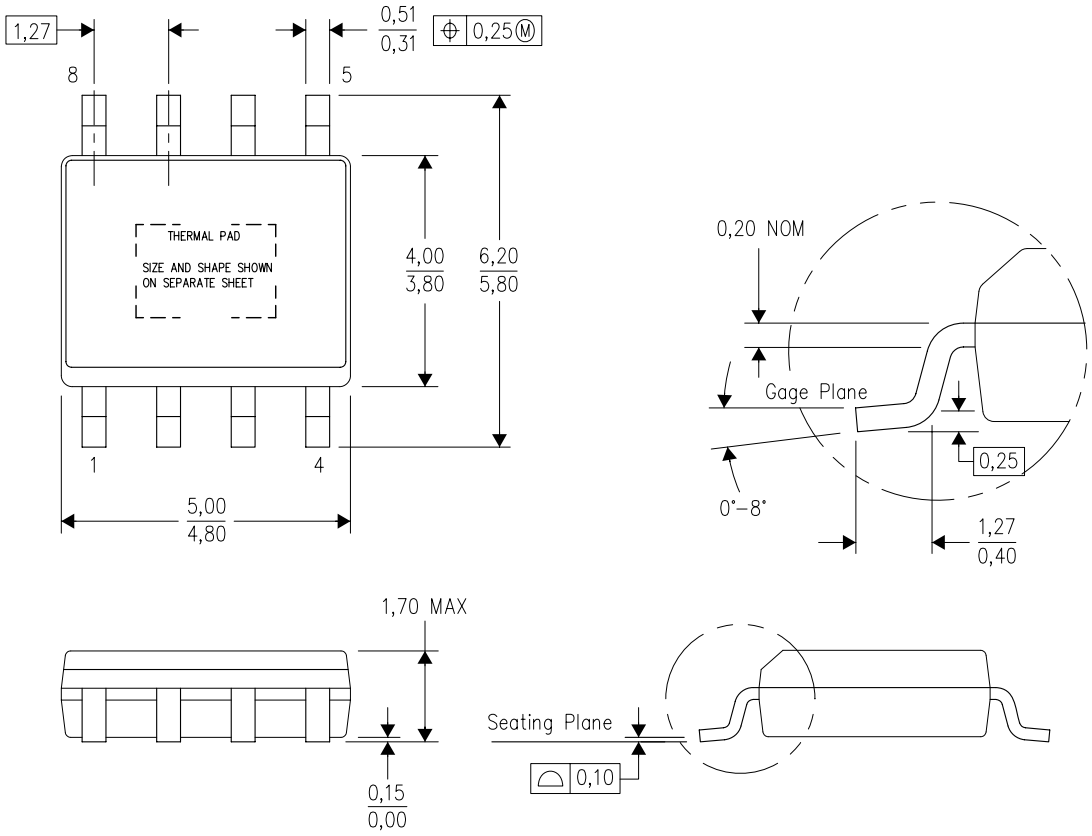
# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

**PowerPAD is a trademark of Texas Instruments.**

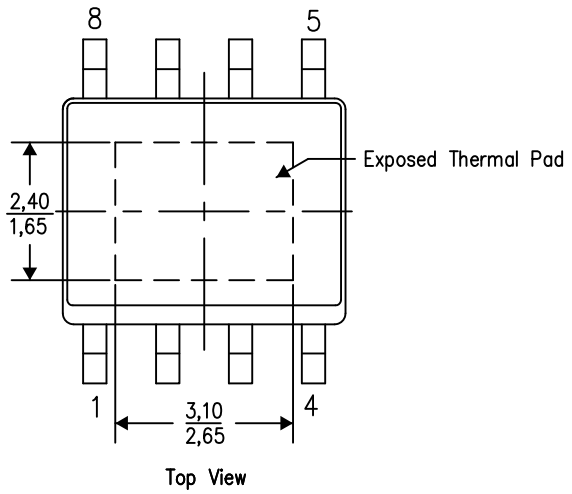
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



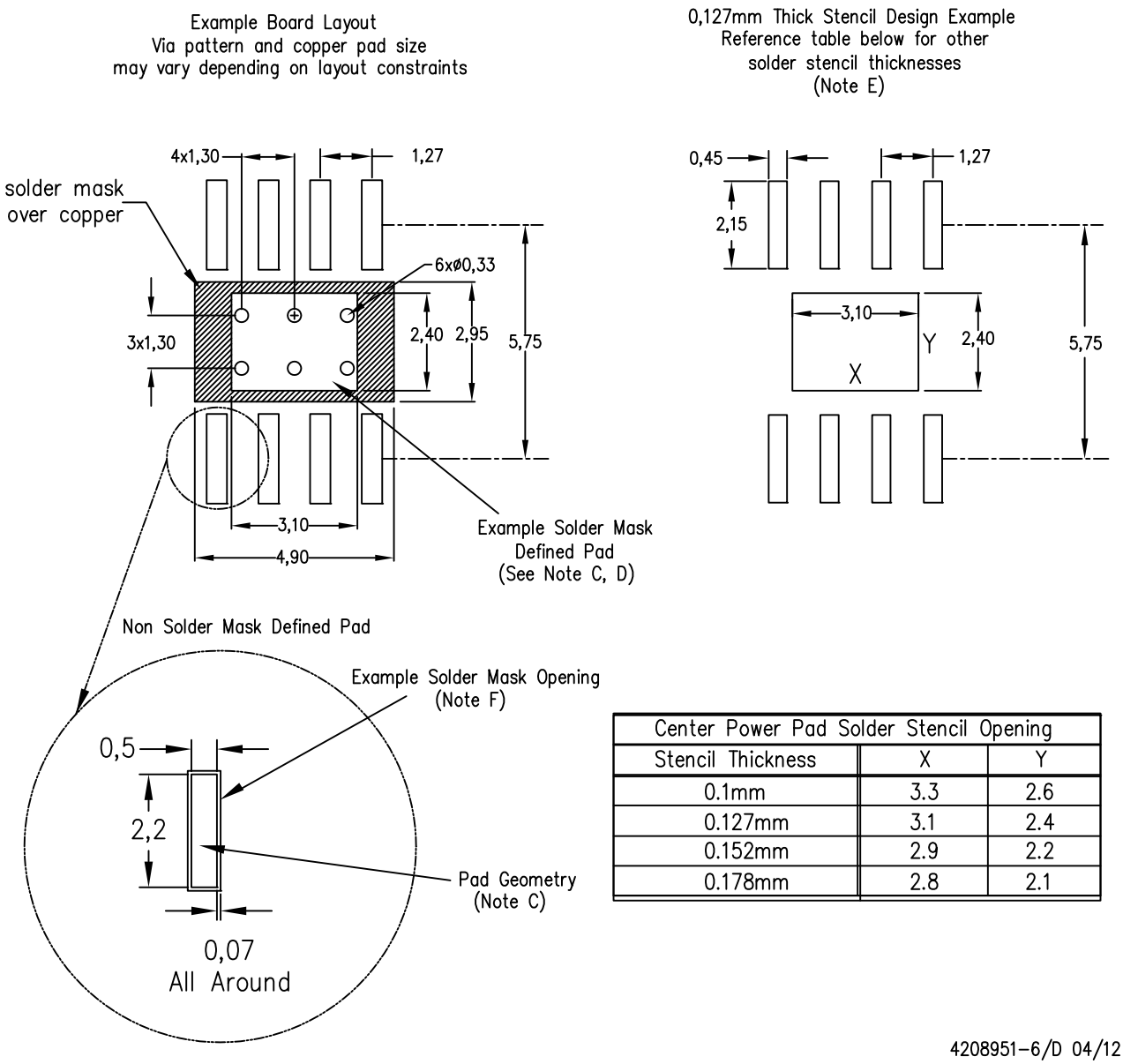

Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.3 | 2.6 |
| 0.127mm | 3.1 | 2.4 |
| 0.152mm | 2.9 | 2.2 |
| 0.178mm | 2.8 | 2.1 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

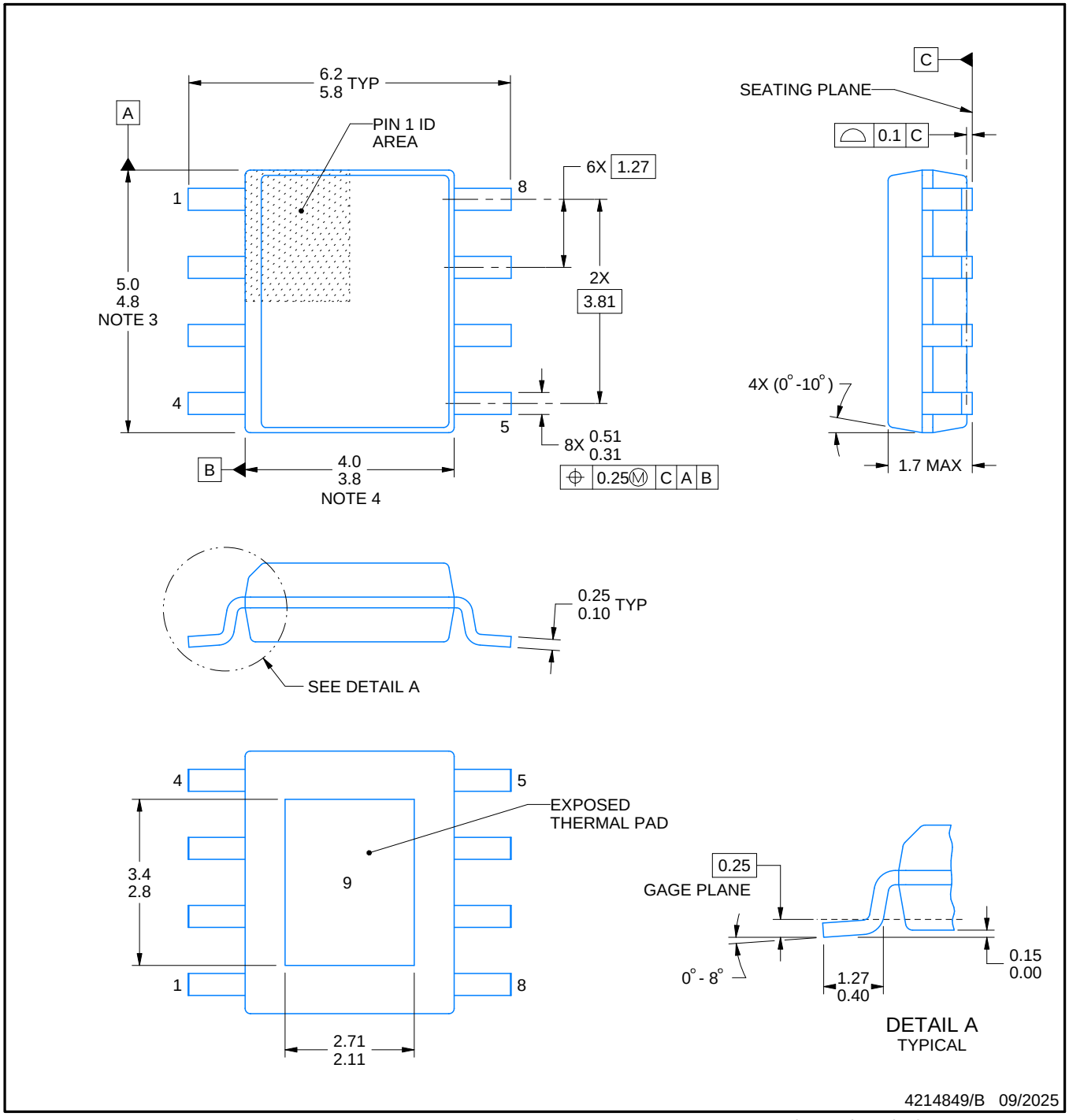
PowerPAD is a trademark of Texas Instruments.

# PACKAGE OUTLINE

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

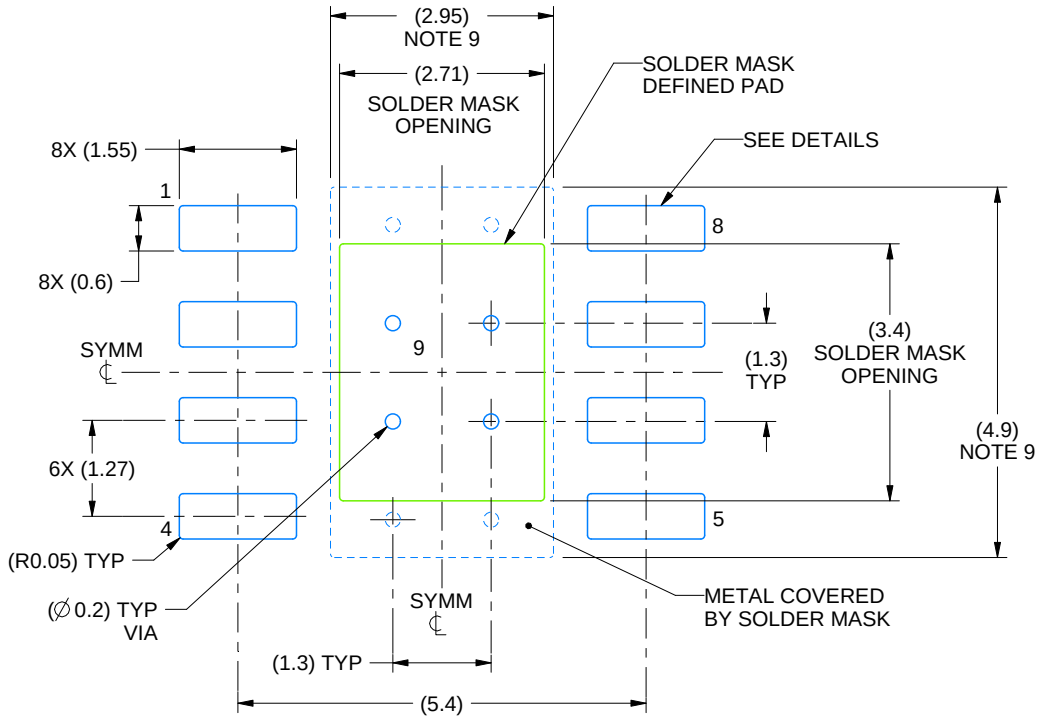
PLASTIC SMALL OUTLINE



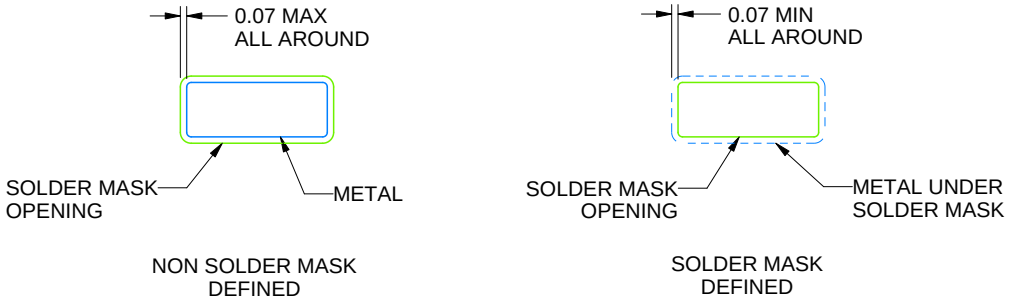

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

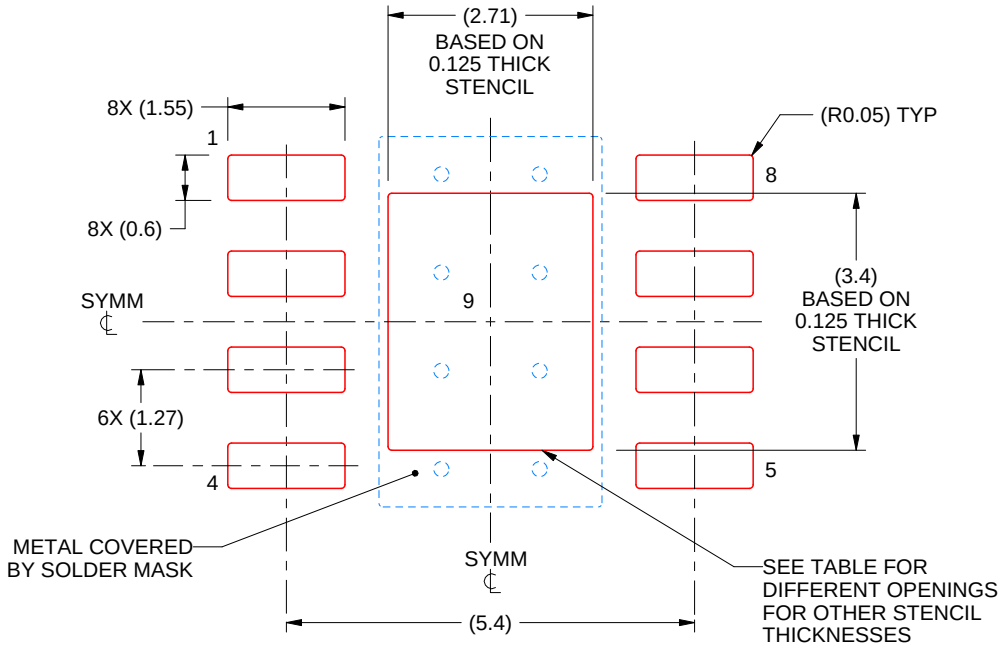
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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