TEXAS INSTRUMENTS
TPS54J060
JAJSJW7D – SEPTEMBER 2019 – REVISED JUNE 2024

TPS54J060 4V～16V 入力、6A、同期整流式降圧コンバータ、D-CAP3™ 制御および 0.9V 基準電圧付き

1 特長

- 入力範囲:2.7V～16V、外部バイアス (3.3V～3.6V) あり
- 入力範囲:4V～16V、外部バイアスなし
- 6A の連続出力電流をサポートする内蔵 MOSFET
- 高速な負荷ステップ応答を実現する D-CAP3™ 制御モード
- すべての出力コンデンサでセラミック コンデンサの使用をサポート
- 精度 ±1% の 900mV 基準電圧 (接合部温度:–40℃～+125℃)
- 出力電圧範囲:0.9V ～ 5.5V
- 自動スキップ Eco-mode により軽負荷時の効率を向上
- 外付け抵抗でプログラム可能な電流制限
- 選択可能な周波数設定 (600kHz、1100kHz、2200kHz)
- 内部固定、外部調整可能ソフト スタート
- プリバイアス付きスタートアップ機能
- 内蔵回路により、出力をゆっくり放電可能
- オープン ドレインのパワー グッド出力
- OC、UV、OV フォルトのラッチオフ
- RoHS に完全準拠
- 2.5mm × 3mm の 14 ピン WQFN-HR パッケージ、0.5mm ピッチ

2 アプリケーション

- サーバおよびクラウド・コンピューティング POL
- ブロードバンド、ネットワーク、光通信
- ワイヤレス・インフラ
- 産業用 PC
- IP ネットワーク・カメラ

3 概要

TPS54J060 デバイスは、適応型オン時間 D-CAP3 制御モードを搭載した、高効率、小型の同期整流式降圧コンバータです。スペースに制約のある電源システムで使いやすく、外部部品数が少なくて済みます。

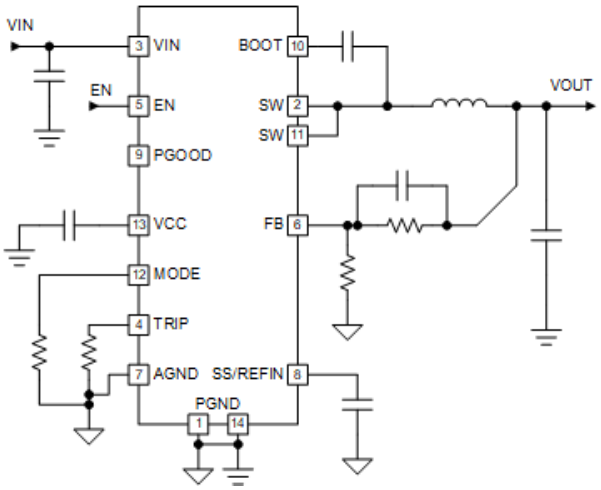
このデバイスは、高性能の内蔵 MOSFET、高精度 (±1%) の 900mV 基準電圧、–40℃～+125℃の接合部温度範囲を特長としています。競争力のある機能として、非常に少ない外付け部品点数、高速な負荷過渡応答、精密な負荷レギュレーションとライン レギュレーション、自動スキップまたは FCCM モード動作、可変ソフト スタート制御、外部補償を使わない全セラミック コンデンサ設計のサポートが挙げられます。

TPS54J060 は、14 ピンの QFN パッケージで供給されます。

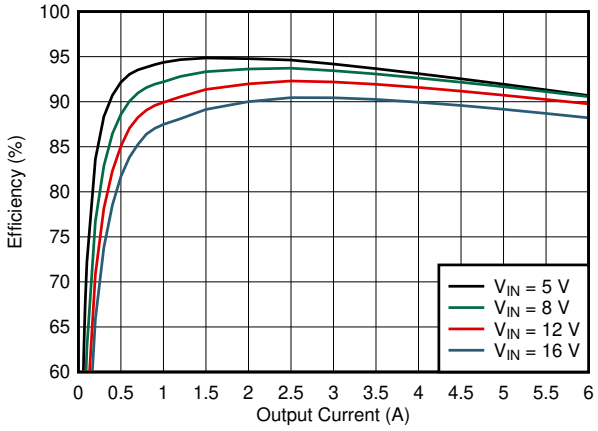
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS54J060	RPY (VQFN-HR、14)	3mm × 2mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



代表的な効率 (V_{OUT} = 1.8V、f_{SW} = 600kHz)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Pin Configuration and Functions.....3
5 Specifications.....4
5.1 Absolute Maximum Ratings.....4
5.2 ESD Ratings.....4
5.3 Recommended Operating Conditions.....4
5.4 Thermal Information.....5
5.5 Electrical Characteristics.....5
5.6 Typical Characteristics.....8
6 Detailed Description.....11
6.1 Overview.....11
6.2 Functional Block Diagram.....11
6.3 Feature Description.....12
6.4 Device Functional Modes.....17
7 Application and Implementation.....18
7.1 Application Information.....18
7.2 Typical Application.....18
7.3 Power Supply Recommendations.....29
7.4 Layout.....30
8 Device and Documentation Support.....33
8.1 Documentation Support.....33
8.2 ドキュメントの更新通知を受け取る方法.....33
8.3 サポート・リソース.....33
8.4 Trademarks.....33
8.5 静電気放電に関する注意事項.....33
8.6 用語集.....33
9 Revision History.....34
10 Mechanical, Packaging, and Ordering Information.....35

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4 Pin Configuration and Functions

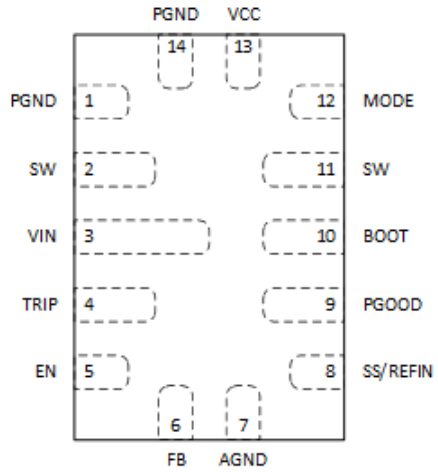


図 4-1. 14-Pin VQFN-HR, RPG Package (Top View)

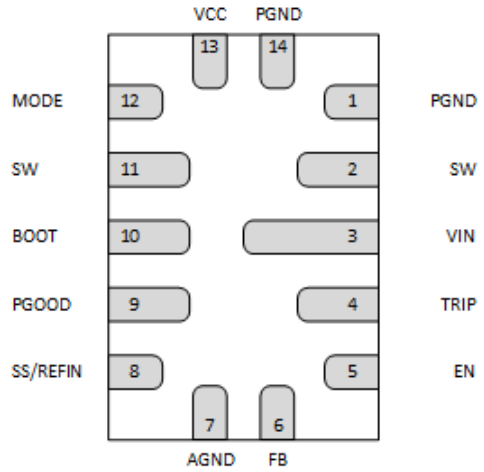


図 4-2. 14-Pin VQFN-HR, RPG Package (Bottom View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1, 14	PGND	G	Power ground of internal low-side MOSFET
2., 11	SW	O	Output switching terminal of the power converter. Connect this pin to the output inductor.
3	VIN	I	Power-supply input pins for both integrated power MOSFET pair and the internal regulator. Place the decoupling input capacitors as close as possible to VIN pins.
4	TRIP	I/O	Current limit setting pin. Connect a resistor to ground to set the current limit trip point. See *セクション 6.3.7* for detailed OCP setting.
5	EN	I	Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating the EN pin is not recommended.
6	FB	I	Output feedback input. A resistor divider from the VOUT to AGND (tapped to FB pin) sets the output voltage.
7	AGND	G	Analog ground pin, reference point for internal control circuits
8	SS/REFIN	I/O	Internal reference voltage can be overridden by an external voltage source on this pin for tracking application. Connecting a capacitor to AGND increases soft-start time.
9	PGOOD	O	Open-drain power-good status signal. A high voltage indicates the FB voltage has moved inside the specified limits.
10	BOOT	I/O	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to SW node.
12	MODE	I	The MODE pin sets the forced continuous-conduction mode (FCCM) or skip-mode operation. It also selects the operating frequency.
13	VCC	I/O	Internal 3-V LDO output. An external bias with 3.3-V ±5% voltage can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. For the decoupling, suggest a 1-µF ceramic capacitor as close to VCC pin as possible.

(1) I = Input, O = Output, P = Supply, G = Ground

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Pin voltage(2)	VIN		–0.3	18	V
	VIN – SW	DC	–0.3	18	V
	SW – PGND	DC	–0.3	18	V
	VIN – SW	Transient < 20 ns	–4.0	25	V
	SW – PGND	Transient < 20 ns	–5.0	21.5	V
	BOOT – SW		–0.3	6	V
	BOOT – PGND		–0.3	24	V
	EN, PGOOD		–0.3	6	V
	TRIP, MODE, SS/REFIN, FB		–0.3	6	V
	VCC		–0.3	6	V
Pin voltage differential	AGND - PGND		–0.3	0.3	V
Operating Junction Temperature Range, T_J			–40	150	°C
Storage Temperature Range, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	VIN with up to 3.6V external bias on VCC (1)	2.7	16	V
	VIN with internal bias	4	16	V
	VIN to enable the converter with internal bias	3.3		V
Pin voltage	SW – PGND	–0.1	16	V
	BOOT – SW	–0.1	5.3	V
	TRIP, SS/REFIN, FB	–0.1	1.5	V
	MODE	–0.1	VCC	V
	EN, PGOOD	–0.1	5.5	V
	VCC	3.0	3.6	V
Pin voltage differential	AGND - PGND	–0.1	0.1	V
Junction temperature, T_J	Operating junction temperature	–40	125	°C

(1) Ensure that under any combination of the conditions listed above that stresses on the device do not exceed those specified in the Absolute Maximum Ratings.

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5.4 Thermal Information

THERMAL METRIC[1]		TPS54J060 RPG (QFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC)	64	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (JEDEC)	40	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (JEDEC)	16.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (JEDEC)	16.2	°C/W
$R_{\theta JA(EVM)}$	Junction-to-ambient thermal resistance (EVM)	43.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter (EVM)	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter (EVM)	21	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*

5.5 Electrical Characteristics

T_J = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN operating non-switching supply current	V_{EN} = 2 V, V_{FB} = V_{INTREF} + 50mV, V_{IN} = 12 V, no external bias on VCC pin		750	900	µA
$I_{Q(VCC)}$	External VCC bias current[1]	3.3 V external bias on VCC pin, $f_{SW(FCCM)}$ = 600kHz		3		mA
		3.3 V external bias on VCC pin, $f_{SW(FCCM)}$ = 1100kHz		5.5		mA
		3.3 V external bias on VCC pin, $f_{SW(FCCM)}$ = 2200kHz		10		mA
I_{SD_VIN}	VIN shutdown supply current	V_{EN} = 0 V, V_{IN} =12 V, no external bias on VCC pin		10		µA
$VIN_{UVLO(R)}$	VIN UVLO rising threshold voltage	VIN rising, VCC = external 3.3V bias	2.1	2.4	2.7	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold voltage	VIN falling, VCC = external 3.3V bias	1.55	1.85	2.15	V
ENABLE						
V_{ENH}	EN enable threshold voltage (rising)		1.17	1.22	1.27	V
V_{ENL}	EN disable threshold voltage (falling)		0.97	1.02	1.07	V
V_{ENHYST}	EN hysteresis voltage			0.2		V
V_{ENLEAK}	EN input leakage current	V_{EN} = 3.3 V	–5	0	5	µA
	EN internal pull-down resistance	EN pin to AGND.		6500		kΩ
INTERNAL LDO						
VCC	Internal LDO output voltage	V_{IN} = 12 V, $I_{VCC(LOAD)}$ = 5 mA	2.90	3.00	3.10	V
VCC_{UVLO}	VCC undervoltage-lockout (UVLO) threshold voltage	VCC rising	2.80	2.85	2.90	V
		VCC falling	2.65	2.70	2.75	V
VCC_{UVLO}	VCC undervoltage-lockout (UVLO) threshold voltage	VCC hysteresis		0.15		V
VCC_{DO}	LDO low-droop dropout voltage	V_{IN} = 3.3 V, $I_{VCC(LOAD)}$ = 20 mA, T_J = 25°C			310	mV
	LDO overcurrent limit	All VINs, all temps	30	60		mA
REFERENCE						
V_{INTREF}	Internal REF voltage	T_J = 25°C		900		mV
	Internal REF voltage tolerance	T_J = 0°C to 70°C	896		904	mV
	Internal REF voltage tolerance	T_J = –40°C to 125°C	891		909	mV
I_{FB}	FB input current	V_{FB} = V_{INTREF}			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	VO switching frequency, FCCM operation[1]	V_{IN} = 12 V, V_{OUT}=1.2V, R_{MODE} = 0 Ω to AGND, No Load	935	1100	1265	kHz
$f_{SW(FCCM)}$	VO switching frequency, FCCM operation[1]	V_{IN} = 12 V, V_{OUT}=2.5V, R_{MODE} = 30.1 kΩ to AGND, No Load	1870	2200	2530	kHz

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5.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW(FCCM)}$	VO switching frequency, FCCM operation	V_{IN} = 12 V, V_{OUT}=1.2V, R_{MODE} = 60.4 kΩ to AGND, No Load	536	630	724	kHz
$t_{ON(min)}$	Minimum on-time	VIN=12V VOUT=1V, first pulse		70	95	ns
$t_{OFF(min)}$	Minimum off-time	T_J = 25°C, HS FET Gate falling to rising			220	ns
STARTUP						
	EN to first switching delay, internal LDO	The delay from EN goes high to the first SW rising edge with internal 3.0V LDO. VCC bypass cap = 1uF for typical value, VCC bypass cap = 2.2uF for max value. $C_{SS/REFIN}$ = 1nF		0.85	2	ms
	EN to first switching delay, external VCC bias	The delay from EN goes high to the first SW rising edge with external 3.3V VCC bias. $C_{SS/REFIN}$ = 1nF		500	700	µs
t_{SS}	Internal soft-start time	V_O rising from 0 V to 95% of final setpoint, $C_{SS/REFIN}$ = 1nF	1	1.5		ms
	SS/REFIN sourcing current	$V_{SS/REFIN}$ = 0 V		9		µA
	SS/REFIN sinking current	$V_{SS/REFIN}$ = 1 V		3		µA
	SSREFIN Detection Threshold	VIN=4V-16V, VCC=3.0V – 5.3V, -40C- 125C, TPS54J060		550		mV
	SS/REFIN to FB matching	$V_{SS/REFIN}$ = 0.5 V	-5	0	5	mV
POWER STAGE						
$R_{DS(on)HS}$	High-side MOSFET on-resistance	T_J = 25°C, BOOT-SW = 3 V, I_O = 3 A		22		mΩ
$R_{DS(on)LS}$	Low-side MOSFET on-resistance	T_J = 25°C, VCC = 3 V, I_O = 3 A		8.5		mΩ
BOOT CIRCUIT						
$I_{VBST-SW}$	VBST-SW leakage current	T_J = 25°C, $V_{VBST-SW}$ = 3.3 V		28		µA
	BOOT UVLO(1)	T_J = 25°C, Voltage rising		2.35		V
	BOOT UVLO Hysteresis(1)	T_J = 25°C		0.32		V
CURRENT DETECTION						
	Current limit clamp	Valley current on LS FET, 0-Ω ≤ R_{TRIP} ≤ 3.16-kΩ	8.1	9.5		A
R_{TRIP}	TRIP pin resistance range		3.74		30.1	kΩ
I_{OCL}	Current limit threshold	Valley current on LS FET, R_{TRIP} = 4.99 kΩ	5.1	6.0	6.9	A
K_{OCL}	K_{OCL} constant for RTRIP equation			30000		
	K_{OCL} tolerance	3.74-kΩ ≤ R_{TRIP} ≤ 4.99-kΩ	-10		10	%
	K_{OCL} tolerance	10-kΩ = R_{TRIP}	-16.5		16.5	%
I_{NOCL}	Negative current limit threshold	All VINs	-4.3	–3.5	-2.8	A
I_{ZC}	Zero-cross detection current threshold, open loop	V_{IN} = 12 V, VCC = 3 V	0	200	730	mA
UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage		113	116	119	%
V_{UVP}	Undervoltage-protection (UVP) threshold voltage		77	80	83	%
$t_{delay(OVP)}$	OVP response delay	With 100-mV overdrive		300		ns
$t_{delay(UVP)}$	UVP filter delay			64		µs
POWER GOOD						
V_{PGTH}	PGOOD threshold	FB rising, PGOOD transition low to high	89	92.5	95	%
		FB rising, PGOOD transition high to low	113	116	119	
		FB falling, PGOOD transition high to low	77	80	83	
V_{OOB}	PGOOD & Out-of-bounds threshold	FB rising	102.5	105	107.5	%
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.4 V, V_{IN} = 12 V, VCC = 3 V			5.5	mA
I_{PG}	PGOOD low-level output voltage	I_{PGOOD} = 5.5 mA, V_{IN} = 12 V, VCC = 3 V			400	mV
$t_{delay(PG)}$	PGOOD delay time	Delay for PGOOD from low to high		1	1.25	ms
		Delay for PGOOD from high to low		2	5	µs

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5.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(PG)}$	PGOOD leakage current when pulled high	T_J = 25°C, V_{PGOOD} = 3.3 V, V_{FB} = V_{INTREF}			5	µA
	PGOOD clamp low-level output voltage	V_{IN} = 0 V, VCC = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 100-kΩ resistor		750	1100	mV
		V_{IN} = 0 V, VCC = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 10-kΩ resistor		950	1250	mV
	Min VCC for valid PGOOD output				1.5	V
OUTPUT DISCHARGE						
R_{Dischg}	Output discharge resistance	V_{IN} = 12 V, VCC = 3 V, power conversion disabled		80		Ω
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Temperature rising	155	170		°C
	Thermal shutdown hysteresis(1)			38		°C

(1) Specified by design. Not production tested.

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5.6 Typical Characteristics

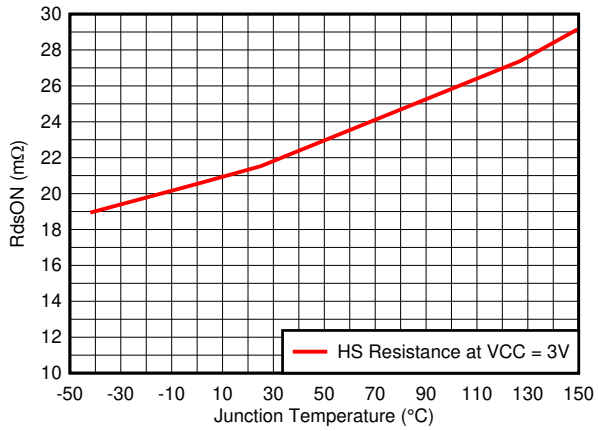


図 5-1. High-Side FET RdsON

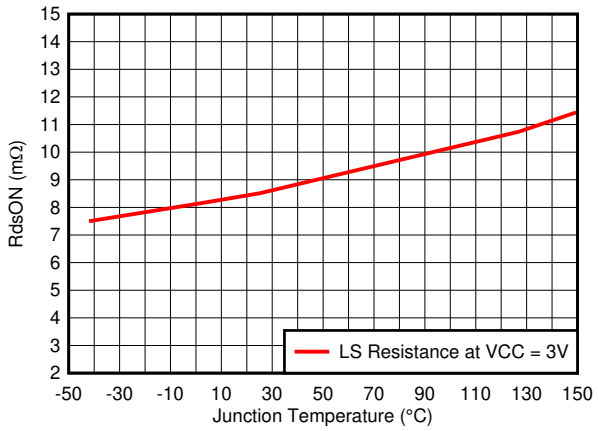


図 5-2. Low-Side FET RdsON

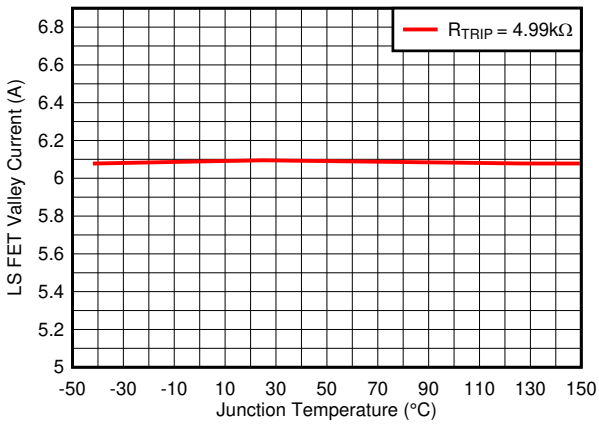


図 5-3. Overcurrent Limit

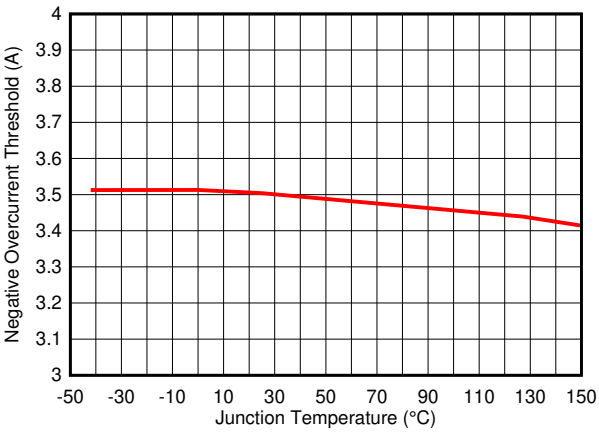


図 5-4. Negative Overcurrent Limit

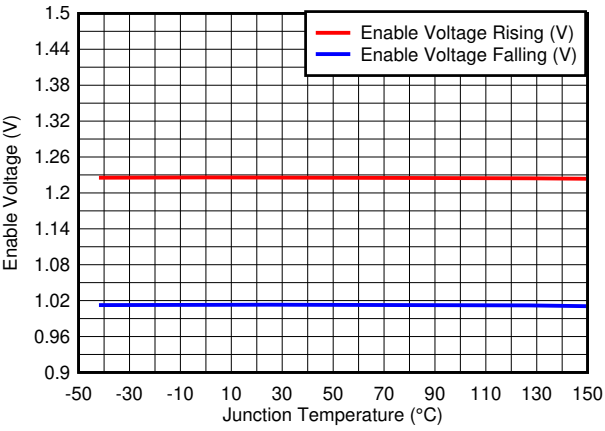


図 5-5. Enable Voltage

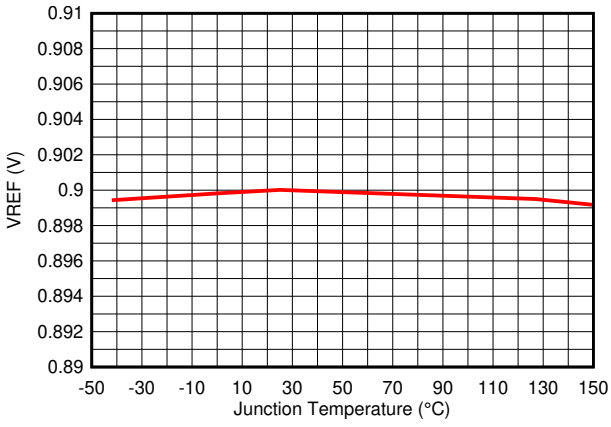


図 5-6. Vref

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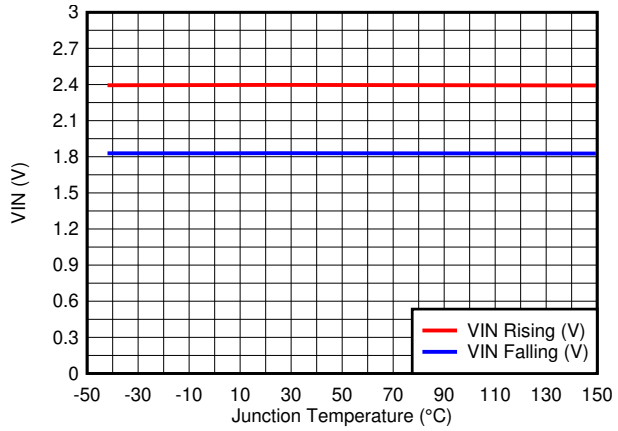


図 5-7. VIN UVLO

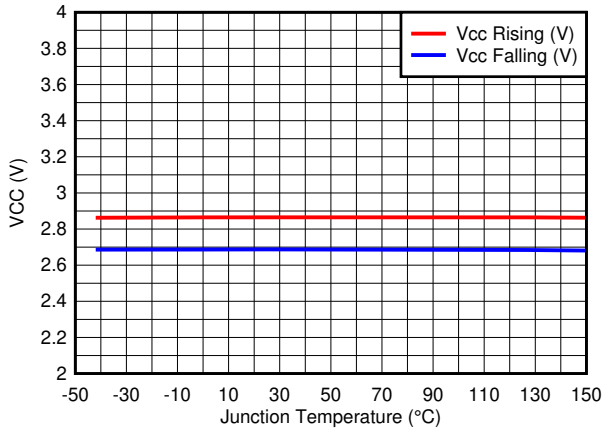


図 5-8. VCC UVLO

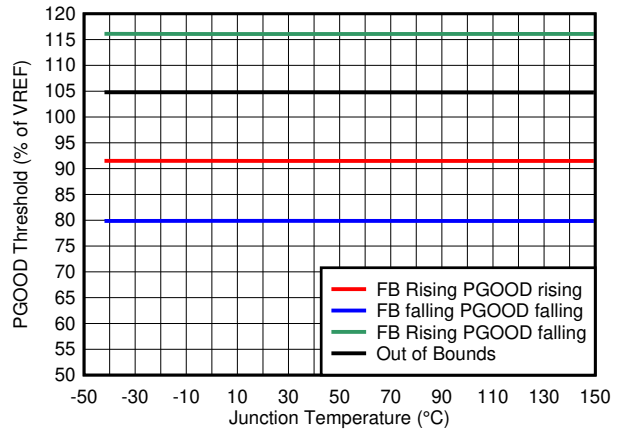


図 5-9. PGOOD Thresholds

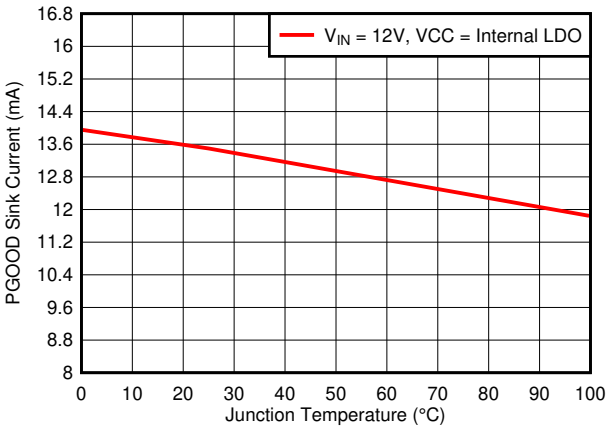


図 5-10. PGOOD Sink Current

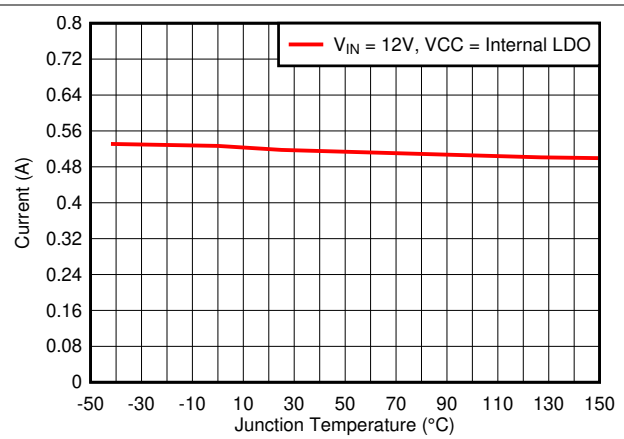


図 5-11. Zero Crossing Threshold

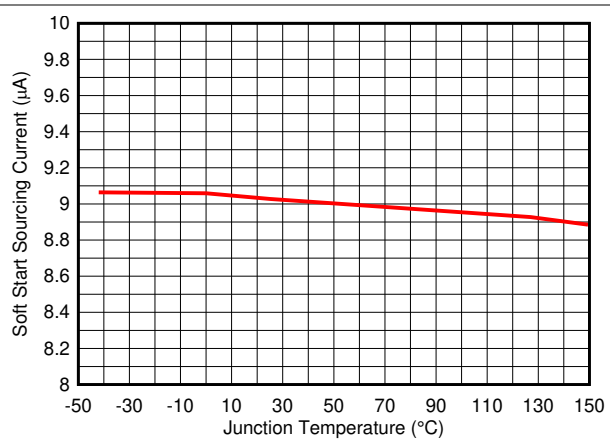


図 5-12. Soft-Start Sourcing Current

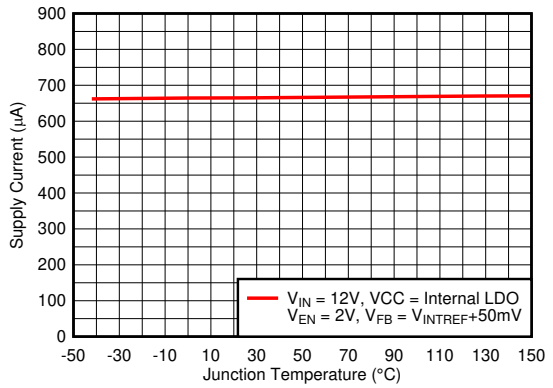


図 5-13. Non-Switching Supply Current

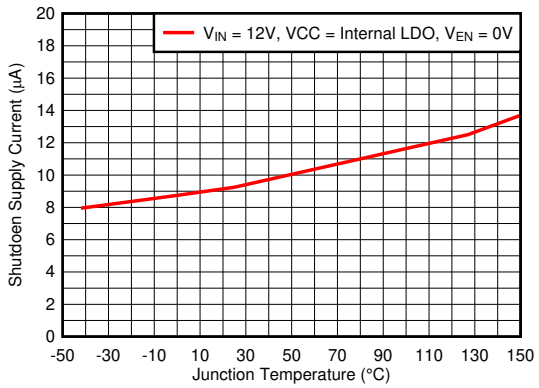
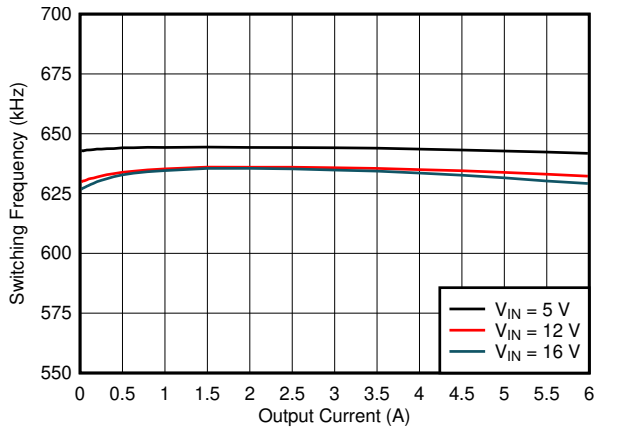
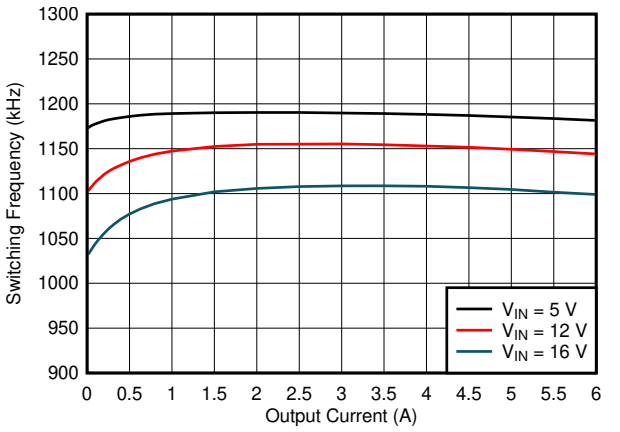


図 5-14. Shutdown Supply Current



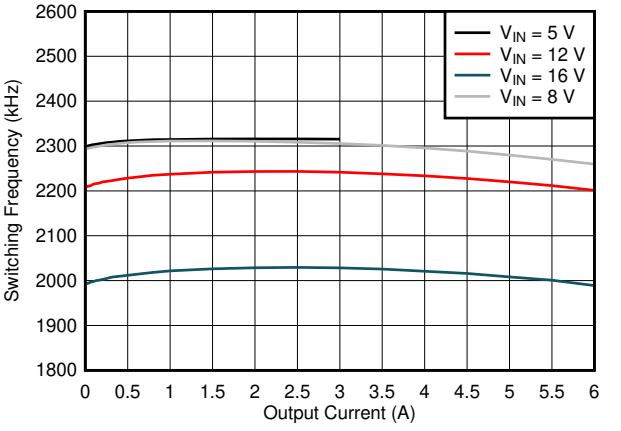
VOUT = 1.2 V L = 1 µH MODE = FCCM

図 5-15. 600-kHz Switching Frequency vs Load Current



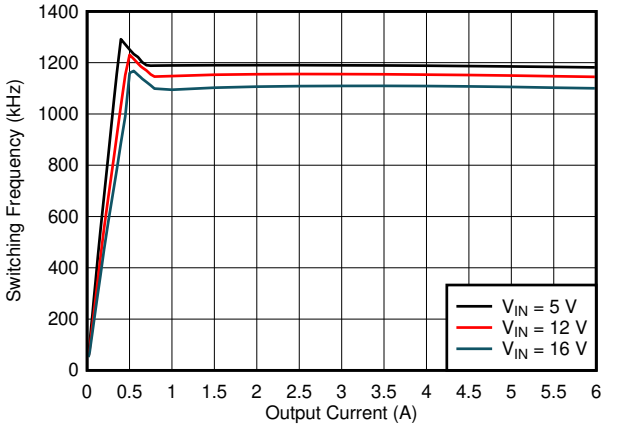
VOUT = 1.2 V L = 1 µH MODE = FCCM

図 5-16. 1100-kHz Switching Frequency vs Load Current



VOUT = 2.5 V L = 0.47 µH MODE = FCCM

図 5-17. 2200-kHz Switching Frequency vs Load Current



VOUT = 1.2 V L = 1 µH MODE = DCM

図 5-18. 1100-kHz Switching Frequency vs Load Current – DCM

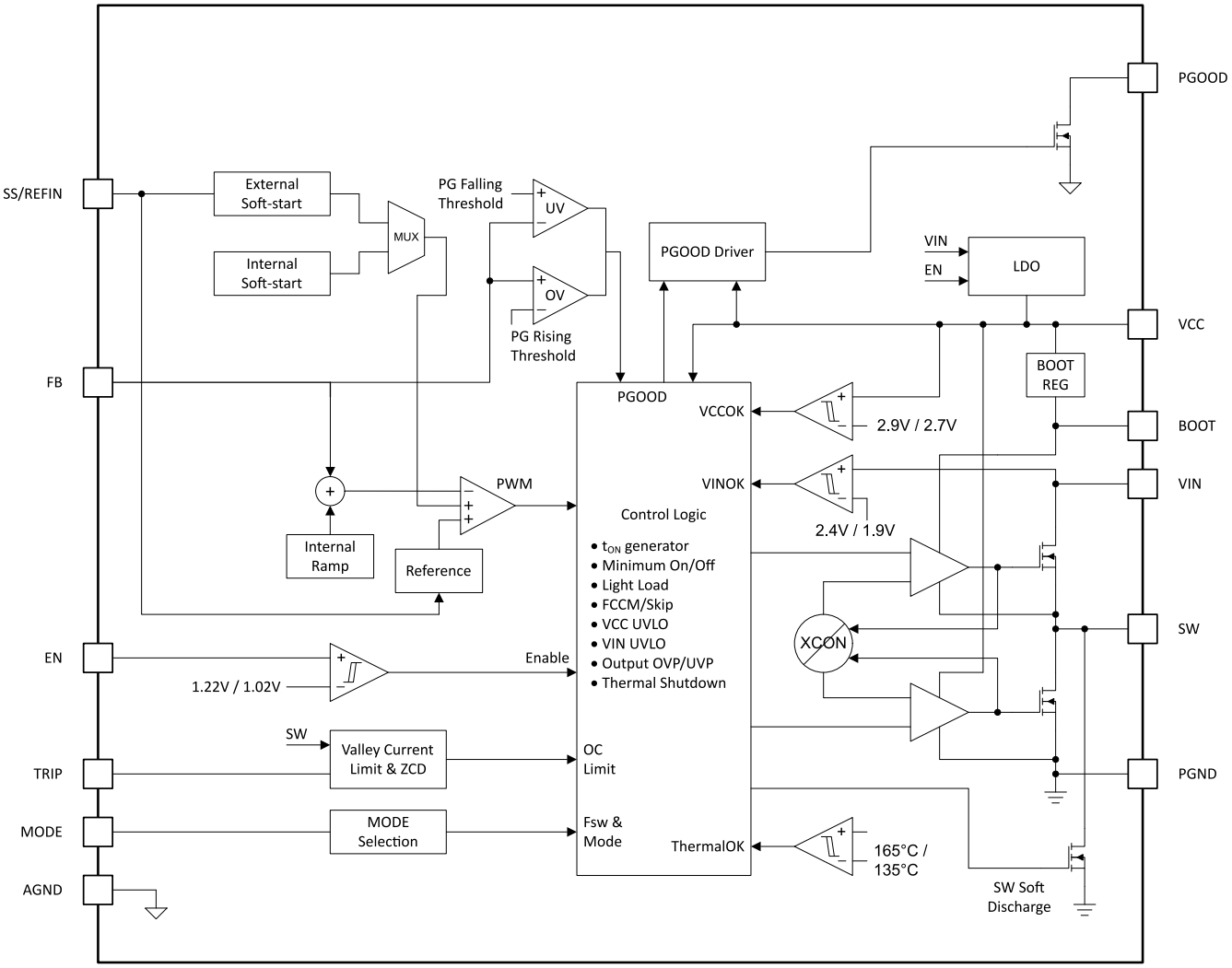
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6 Detailed Description

6.1 Overview

The TPS54J060 device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device suits low output voltage point-of-load applications with up to 6-A output current in server, storage, and similar computing applications. The TPS54J060 features proprietary D-CAP3 control mode combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC-DC converters in an ideal fashion. The output voltage ranges from 0.9 V to 5.5 V. The conversion input voltage ranges from 2.7 V to 16 V, and the VCC input voltage ranges from 3 V to 3.6 V. The D-CAP3 control mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low external component count. Further advantage of this control scheme is that it supports stable operation with all ceramic output capacitors. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Enable and Internal LDO

The TPS54J060 has an internal 3-V LDO feature using input from VIN and output to VCC. When the VIN voltage rises above the VIN_{UVLO} rising threshold (typically 2.4 V), and the EN voltage rises above enable threshold (typically 1.22 V), the internal LDO is enabled and outputs voltage to the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry. The VCC voltage also provides the supply voltage for the gate drives.

When the EN pin voltage rises above the enable threshold voltage and VCC rises above the VCC_{UVLO} rising-threshold (typically 2.85 V), the device enters the start-up sequence. The device then uses the first 400 µs to calibrate the MODE setting resistance attached to the MODE pin and sets the switching frequency internally. During this period, the MODE pin resistance determines the operation mode too. The device remains disabled state when EN pin floats due to an internal pulldown resistance with a nominal value of 6.5 MΩ.

There is an internal 2-µs filter to filter noise on the EN pin. If the pin is held low longer than the filter, then the IC shuts down. If the EN pin is taken high again after shutdown, then the sequence begins as if EN is taken high for the first time.

6.3.2 Split Rail and External LDO

The TPS54J060 can also operate with an externally supplied VCC. It is important that the external VCC voltage (3.3 V ±5%) be applied and ready before at least one of the VIN or EN signals are applied. This avoids the possibility of sinking current out of the internal LDO and thus ensures a smooth power-up sequence.

A good power-up sequence is where least one of VIN_{UVLO} rising threshold or EN rising threshold is satisfied later than the VCC_{UVLO} rising threshold. A practical example is: VIN applied is first, then the external bias applied, and then EN signal goes high. When the EN pin voltage rises above the enable threshold voltage, the device enters the start-up sequence as above. A good power-down sequence is the reverse, where either the VIN_{UVLO} falling threshold or EN falling threshold is satisfied before the VCC_{UVLO} falling threshold.

6.3.3 Output Voltage Setting

The output voltage is programmed by the voltage-divider resistors, R_{FB_HS} and R_{FB_LS}, shown in 式 1. Connect R_{FB_HS} between the FB pin and the positive node of the load, and connect R_{FB_LS} between the FB pin and AGND. TI recommends a R_{FB_LS} value between 1 kΩ to 20 kΩ. Determine R_{FB_HS} by using 式 1.

$$R_{FB_HS} = \frac{V_O - V_{INTREF}}{V_{INTREF}} \times R_{FB_LS} \quad (1)$$

R_{FB_HS} and R_{FB_LS} must be as close to the device as possible.

6.3.4 Soft Start and Output-Voltage Tracking

The TPS54J060 implements a circuit to allow both internal fixed soft start and external adjustable soft start. The internal soft-start time is typically 1.5 ms and has a 1-ms minimum value. The internal soft-start time can be increased by adding a SS capacitor between SS/REFIN and AGND. The SS capacitor value can be determined by 式 2. Note, any C_{SS} calculation that uses a soft-start time of less than 1.5 ms will be ignored by the internal soft-start time circuit. Therefore, selecting a capacitor less than or equal to 15 nF will result in the internal default 1.5 ms soft-start time (See セクション 7.2.2.7).

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{INTREF}} \quad (2)$$

The SS/REFIN pin can also be used as an analog input to accept an external reference. When an external voltage signal is applied to SS/REFIN pin, it acts as the reference voltage, thus the FB voltage follows this external voltage signal. Apply the external reference to the SS/REFIN pin before soft start. The external

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reference voltage must be equal to or higher than the internal reference level to ensure correct Power Good thresholds during soft start. With an external reference applied, the internal fixed soft start controls output voltage ramp during start-up.

After soft start, the external reference voltage signal can be in a range of 0.5 V to 1.2 V.

When driving the SS/REFIN pin with an external resistor divider, the resistance must be low enough so that the external voltage source can overdrive the internal current source. Note that the internal current source remains active.

When the TPS54J060 is enabled, an internal discharge resistance turns on to discharge external capacitance on the SS/REFIN pin and ensure soft start from 0 V. When the device is enabled with both VIN and EN above the rising thresholds, 100 Ω of resistance is connected from the SS/REFIN pin to ground. After the device detects the VCC pin is in regulation, the discharge resistance is increased to 300 Ω. The 300-Ω discharge resistance is connected to the SS/REFIN until the MODE detection time is completed. After the MODE detection time is completed, the TPS54J060 detects if an external reference is connected.

6.3.5 Frequency and Operation Mode Selection

The TPS54J060 provides forced CCM operation for tight output ripple application and auto-skipping Eco-Mode for high light-load efficiency. The device allows users to select the switching frequency and operation mode by using the MODE pin. 表 6-1 lists the resistor values for the switching frequency and operation mode selection. TI recommends 1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

The MODE status will be set and latched during the MODE pin calibration time. Changing the MODE pin resistance after the calibration time will not change the status of the device.

To make sure internal circuit detects the desired setting correctly, *do not* place any capacitor on the MODE pin.

表 6-1. MODE Pin Selection

MODE PIN CONNECTIONS	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)
Short to VCC	Skip mode	1100
243 kΩ ± 10% to AGND	Skip mode	2200
121 kΩ ± 10% to AGND	Skip mode	600
60.4 kΩ ±10% to AGND	Forced CCM	600
30.1 kΩ ±10% to AGND	Forced CCM	2200
Short to AGND	Forced CCM	1100

6.3.6 D-CAP3™ Control Mode

The TPS54J060 uses D-CAP3 control mode to achieve fast load transient while maintaining ease-of-use. The D-CAP3 control mode architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). No external current sensing network or voltage compensators are required with D-CAP3 control mode architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop. The amplitude of the ramp is determined by the R-C time-constant of the internal circuit. At different switching frequencies (f_{SW}), the R-C time-constant varies to maintain relatively constant amplitude of the internally generated ripple. Also, the device uses internal circuit to cancel the dc offset caused by the injected ramp, which significantly reduces the DC offset caused by the output ripple voltage.

For any control topologies supporting no external compensation design, there is a minimum range or maximum range (or both) of the output filter it can support. The output filter used with TPS54J060 is a low-pass L-C circuit. This L-C filter has double pole that is described in 式 3.

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$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54J060. The low frequency L-C double pole has a 180-degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase by 90 degrees a decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the double pole of 式 3 is located below the internal zero so that the phase boost provided by the internal zero provides adequate phase margin to meet the loop stability requirement.

表 6-2. Internal Zero Frequency

SWITCHING FREQUENCIES (f_{SW}) (kHz)	ZERO (f_Z) FREQUENCY (kHz)
600	10
1100	20
2200	50

After identifying the application requirements, the output inductance must be designed so that the inductor peak-to-peak ripple current is approximately between 20% and 40% of the maximum output current. Use 表 6-2 to help locate the internal zero based on the selected switching frequency. In general, where reasonable (or smaller) output capacitance is desired, set the L-C double pole frequency below the internal zero frequency to determine the necessary output capacitance for stable operation.

If MLCC output capacitors are used, derating characteristics must be accounted for to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10-µF, X5R, and 6.3 V, the deratings by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4 µF. Consult with capacitor manufacturers for specific characteristics of the capacitors used.

For higher output voltage at or above 2 V, additional phase boost can be required for sufficient phase margin due to phase delay/loss for higher output voltage (large on-time (t_{ON})) setting in a fixed on-time topology based operation.

A feedforward capacitor placed in parallel with R_{FB_HS} is found to be very effective to boost the phase margin at loop crossover. Refer to the *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application report for details.

6.3.7 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on-time of the high-side FET, the switch current increases at a linear rate determined by input voltage, output voltage, and the output inductor value. During the on-time of the low-side FET, this current decreases at a linear rate determined by the output voltage and the output inductor value. The average value of the inductor current equals to the load current, I_{OUT}.

The output overcurrent limit (OCL) in the TPS54J060 is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the OFF state by measuring the low-side FET drain-to-source current. If the measured drain-to-source current of the low-side FET is above the current limit, the low-side FET stays ON until the current level becomes lower than the OCL level. This type of behavior reduces the average output current sourced by the device. During an overcurrent condition, the current to the load exceeds the current to the output capacitors and the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold (80%), the UVP comparator shuts down the device after a wait time of 64 µs. The devices remains latched OFF state (both high-side and low-side FETs are latched off) until a reset of VCC or a re-toggling on EN pin.

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If an OCL condition happens during start-up, then the device completes the charging of the soft-start capacitor, then trips UV when soft start is complete. Latch-off follows as above.

The resistor, R_{TRIP} connected from the TRIP pin to AGND sets the valley current limit threshold. 式 4 calculates the R_{TRIP} for a given current limit threshold.

$$R_{TRIP} = \frac{30000}{I_{LIM_VALLEY}} \quad (4)$$

where

- I_{LIM_VALLEY} is the valley current limit threshold in A
- R_{TRIP} is TRIP resistor value in Ω

If an RTRIP value less than 3.74 kΩ is used, the TPS54J060 will default to an internally determined current limit clamp value.

6.3.8 Low-side FET Negative Current Limit

The device has a fixed, cycle-by-cycle negative current limit. Similar to the positive overcurrent limit, the inductor current is monitored during the OFF state. To prevent too large negative current flowing through low-side FET, when the low-side FET detects –3.5-A current (typical threshold), the device turns off the low-side FET and turns on high-side FET for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}. After the high-side FET on-time expires, the low-side FET turns on again.

6.3.9 Power Good

The device has a power-good output that indicates high when the converter output is within the target. The power-good output is an open-drain output and must be pulled up externally through a pullup resistor (usually 10 kΩ). The recommended power-good pullup resistor value is 1 kΩ to 100 kΩ. The power-good function is activated after the soft-start operation is complete.

During start-up, PGOOD transitions HIGH after soft start is complete and the output is between the UV and OV thresholds. If the FB voltage drops to 80% of the V_{INTREF} voltage or exceeds 116% of the V_{INTREF} voltage, the power-good signal latches low after a 5-µs internal delay. When using an external reference, the power-good thresholds are based on the external reference voltage. The power-good signal can only be pulled high again after re-toggling EN or a reset of VCC.

If the input supply fails to power up the device, the power-good signal clamps low by itself when PGOOD is pulled up through an external resistor.

6.3.10 Overvoltage and Undervoltage Protection

The TPS54J060 monitors the FB voltage to detect overvoltage and undervoltage. When the FB voltage becomes lower than 80% of the V_{INTREF} voltage, the UVP comparator detects and an internal UVP delay counter begins counting. After the 64-µs UVP delay time, the latches OFF both high-side and low-side FETs drivers. The UVP function enables after the soft-start period is complete.

When the FB voltage becomes higher than 116% of the V_{INTREF} voltage, the OVP comparator detects and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit I_{NOCL}. Upon reaching the negative current limit, the low-side FET is turned off, and the high-side FET is turned on again, for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}. The device operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 64 µs. After the 64-µs UVP delay time, both high-side and low-side FETs latch off. The fault is cleared with a reset of the input voltage or by re-toggling the EN pin.

During the UVP delay time, if the output voltage becomes higher than the UV threshold, so it is not qualified for UV event and the timer is reset to zero. When the output voltage triggers the UV threshold again, the UVP delay timer restarts.

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6.3.11 Out-Of-Bounds Operation (OOB)

The TPS54J060 has an out-of-bounds (OOB) overvoltage protection circuit that protects the output load at a overvoltage threshold of 5% above the V_{INTREF} voltage. OOB protection does not trigger an overvoltage fault, so the device is on non-latch mode after an OOB event. OOB protection operates as an early no-fault overvoltage protection mechanism. During the OOB operation, the controller operates in forced CCM mode. The low-side FET turns ON, discharging the inductor current below the zero current threshold and the output capacitor and pulling the output voltage to the set point. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

6.3.12 Output Voltage Discharge

When the device is disabled through EN, it enables the output voltage discharge mode. This mode forces both high-side and low-side FETs to latch off, and turns on the approximately 80-Ω discharge FET which is connected from SW to PGND, to discharge the output voltage. Once the FB voltage drops below 100 mV, then the internal LDO is turned off and the discharge FET is turned off.

The output voltage discharge mode is activated by any of below fault events:

1. EN pin goes low to disable the converter.
2. Thermal shutdown (OTP) is triggered.
3. VCC UVLO (falling) is triggered.
4. VIN UVLO (falling) is triggered.

The discharge FET will remain ON for 128 µs after leaving any of the above states.

6.3.13 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the VCC_{UVLO} off-threshold voltage, the device shuts off. If the VCC voltage increases beyond the VCC_{UVLO} on-threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

If the VIN pin voltage is lower than the VIN_{UVLO} falling-threshold voltage but VCC pin voltage is still higher than VCC_{UVLO} on-threshold voltage, the device stops switching and discharges SS. If the VIN voltage increases beyond the VIN_{UVLO} rising-threshold voltage, the device initiates the soft start and switches again. VIN UVLO is a non-latch protection.

6.3.14 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 170°C), the device stops switching and discharges SS. When the temperature falls approximately 38°C below the threshold value, the device turns back on with a initiated soft start. Thermal shutdown is a non-latch protection.

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6.4 Device Functional Modes

6.4.1 Auto-Skip Eco-Mode Light Load Operation

While the MODE pin is pulled to VCC directly or connected to AGND pin through a resistor larger than 121 kΩ, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches I_{ZC}, the zero-cross detection current threshold. I_{ZC} is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). After 16 consecutive detections of zero crossings, the TPS54J060 enters Eco-Mode and the switching frequency begins to decrease. The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{OUT(LL)}$ (for example, the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in 式 5.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (5)$$

where

- f_{SW} is the PWM switching frequency

Only using ceramic capacitors is recommended for auto-skip mode.

6.4.2 Forced Continuous-Conduction Mode

When the MODE pin is tied to the AGND pin through a resistor less than 60.4 kΩ, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

6.4.3 Pre-Bias Start-up

When the TPS54J060 begins soft start, internal circuitry detects if there is a voltage already present on the output. This can be due to a leakage current path in a multi-rail system charging the output capacitors. If the pre-biased voltage is greater than the output voltage commanded by the soft-start voltage, the TPS54J060 operates in Pulse-skip mode during the rise of soft start. When the soft-start voltage reaches a point where the commanded output voltage is greater than the pre-bias voltage, then normal switching occurs.

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7 Application and Implementation

注

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7.1 Application Information

The TPS54J060 is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device suits low output voltage point-of-load applications with 6-A or lower output current in server, storage, and similar computing applications. The device features proprietary D-CAP3 control mode combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC-DC converters in an ideal fashion. The output voltage ranges from 0.9 V to 5.5 V. The conversion input voltage ranges from 2.7 V to 16 V and the VCC input voltage ranges from 3.0 V to 3.6 V. The D-CAP3 control mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low external component count. Further advantage of this control scheme is that it supports stable operation with all ceramic output capacitors. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during a load-step transient.

7.2 Typical Application

This design example describes a D-CAP3 control mode type, 6-A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.8-V output at up to 6 A from a 12-V input bus.

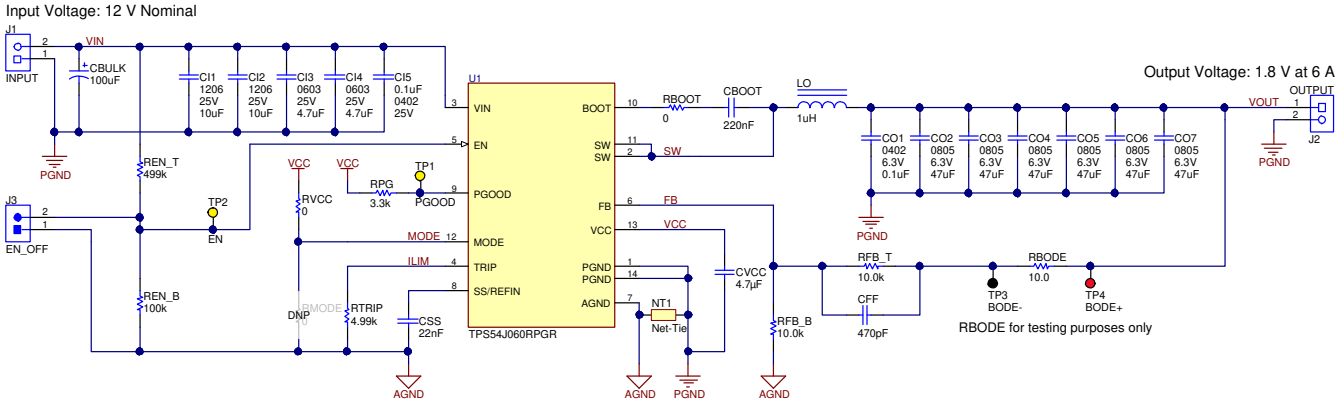


図 7-1. Application Circuit Diagram

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7.2.1 Design Requirements

This design uses the parameters listed in 表 7-1.

表 7-1. Design Example Specifications

DESIGN PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Voltage range		8	12	16	V
V_{OUT}	Output voltage			1.8		V
I_{LOAD}	Output load current				6	A
V_{RIPPLE}	Output voltage DC ripple	V_{IN} = 12 V, I_{OUT} = 6 A (CCM)		10		mV_{PP}
V_{TRANS}	Output voltage undershoot and overshoot after load step	I_{OUT} = 25% to 75% step, 1 A/µs slew rate		18		mV
I_{OUT_LIM}	Output over current limit	V_{IN} = 8 V		6.6		A
t_{SS}	Soft-start time			2		ms
f_{SW}	Switching frequency			1100		kHz

7.2.2 Detailed Design Procedure

The external components selection is a simple process using D-CAP3 control mode. Select the external components using the following steps.

7.2.2.1 Choose the Switching Frequency and Operation Mode (MODE Pin)

The switching frequency and light load mode of operation are configured by the resistor on the MODE pin. From 表 6-1, the MODE pin is connected to VCC to set a 1100-kHz switching frequency with discontinuous conduction mode and skip mode enabled at light loads.

When selecting the switching frequency of a buck converter, the minimum on-time and minimum off-time must be considered. 式 6 calculates the maximum f_{SW} before being limited by the minimum on-time. When hitting the minimum on-time limits of a converter with D-CAP3 control mode, the effective switching frequency will change to keep the output voltage regulated. This calculation ignores resistive drops in the converter to give a worst case estimation.

$$f_{SW}(max) = \frac{V_{OUT}}{V_{IN}(max)} \times \frac{1}{t_{ON_MIN}(max)} = \frac{1.8\ V}{16\ V} \times \frac{1}{95\ ns} = 1180\ kHz \quad (6)$$

式 7 calculates the maximum f_{SW} before being limited by the minimum off-time. When hitting the minimum off-time limits of a converter with D-CAP3 control mode, the operating duty cycle will max out and the output voltage will begin to drop with the input voltage. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the following step so this preliminary calculation assumes a resistance of 10 mΩ. If you are operating near the maximum f_{SW} limited by the minimum off-time, the variation in resistance across temperature must be considered when using 式 7. The selected f_{SW} of 1100 kHz is below the two calculated maximum values.

$$f_{SW}(max) = \frac{V_{IN}(min) - V_{OUT} - I_{OUT}(max) \times \left(R_{DCR} + R_{DS(ON)_HS}\right)}{t_{OFF_MIN}(max) \times \left(V_{IN}(min) - I_{OUT}(max) \times \left(R_{DS(ON)_HS} - R_{DS(ON)_LS}\right)\right)}$$

$$f_{SW}(max) = \frac{8\ V - 1.8\ V - 6\ A \times (10\ m\Omega + 25\ m\Omega)}{220\ ns \times (8\ V - 6\ A \times (25\ m\Omega - 9.2\ m\Omega))} = 3360\ kHz \quad (7)$$

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7.2.2.2 Choose the Output Inductor (L)

Calculate the inductance value to set the ripple current at approximately 0.3 times the output current using 式 8. Larger ripple current improves transient response and improves signal-to-noise ratio with the tradeoff of increased steady state output voltage ripple. Smaller ripple current reduces steady state output voltage ripple with the trade off of slower transient response and may increase jitter. The target ripple current must be between 0.6 A and 3 A. Based on the result of 式 8, a standard inductance value of 1 µH was selected.

$$L = \frac{\left(V_{IN}(max) - V_{OUT}\right) \times V_{OUT}}{I_{RIPPLE} \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 1.8\ V) \times 1.8\ V}{0.3 \times 6\ A \times 16\ V \times 1100\ kHz} = 0.81\ \mu H \quad (8)$$

式 9 calculates the ripple current with the selected inductance. 式 10 calculates the peak current in the inductor and the saturation current rating of the inductor must be greater than this. The saturation behavior of the inductor at the peak inductor current at current limit must also be considered when choosing the inductor. 式 11 calculates the RMS current in the inductor and the heat current rating of the inductor must be greater than this.

$$I_{RIPPLE} = \frac{\left(V_{IN}(max) - V_{OUT}\right) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 1.8\ V) \times 1.8\ V}{1\ \mu H \times 16\ V \times 1100\ kHz} = 1.45\ A \quad (9)$$

$$I_{L(PEAK)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 6\ A + \frac{1.45\ A}{2} = 6.73\ A \quad (10)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + I_{RIPPLE}^2} = \sqrt{6\ A^2 + 1.45\ A^2} = 6.17\ A \quad (11)$$

The selected inductance is a CMLE063T-1R0. This has a saturation current rating of 14 A, RMS current rating of 16 A and a DCR of 6.5-mΩ max. This inductor was selected for the low DCR to get high efficiency.

7.2.2.3 Set the Current Limit (TRIP)

The R_{TRIP} resistor sets the valley current limit. 式 12 calculates the recommended current limit target. This includes the tolerance of the inductor and a factor of 0.85 for the tolerance of the current limit threshold. 式 13 calculates the R_{TRIP} resistor to set the current limit. The typical valley current limit target is 6 A and the closest standard value for R_{TRIP} is 4.99 kΩ.

$$I_{LIM_VALLEY} = \left(I_{OUT} - \frac{1}{2} \times \frac{\left(V_{IN}(min) - V_{OUT}\right) \times V_{OUT}}{L \times (1 + L_{TOL}) \times V_{IN}(min) \times f_{SW}} \right) \times \frac{1}{0.85}$$

$$I_{LIM_VALLEY} = \left(6\ A - \frac{1}{2} \times \frac{(8\ V - 1.8\ V) \times 1.8\ V}{1\ \mu H \times (1 + 0.2) \times 8\ V \times 1100\ kHz} \right) \times \frac{1}{0.85} = 6.44\ A \quad (12)$$

$$R_{TRIP} = \frac{30000}{I_{LIM_VALLEY}} = \frac{30000}{6\ A} = 5.0\ k\Omega \quad (13)$$

With the current limit set, 式 14calculates the typical maximum output current at current limit. 式 15 calculates the typical peak current at current limit. As mentioned in *セクション 7.2.2.2*, the saturation behavior of the inductor at the peak current during current limit must be considered. For worst case calculations, the tolerance of the inductance and the current limit must be included.

$$I_{OUT_LIM}(min) = I_{LIM_VALLEY} + \frac{1}{2} \times \frac{\left(V_{IN}(min) - V_{OUT}\right) \times V_{OUT}}{L \times V_{IN}(min) \times f_{SW}} = 6\ A + \frac{1}{2} \times \frac{(8\ V - 1.8\ V) \times 1.8\ V}{1\ \mu H \times 8\ V \times 1100\ kHz} = 6.6\ A \quad (14)$$

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$$I_{L(PEAK)} = I_{LIM_VALLEY} + \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = 6\ A + \frac{(16\ V - 1.8\ V) \times 1.8\ V}{1\ \mu H \times 16\ V \times 1100\ kHz} = 7.45\ A \quad (15)$$

7.2.2.4 Choose the Output Capacitors (C_{OUT})

There are three considerations for selecting the value of the output capacitor:

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

First, the minimum output capacitance must be calculated based on these three requirements. 式 16 calculates the minimum capacitance to keep the LC double pole below 1/30th the f_{SW} to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero. See 表 6-2 for the location of the internal zero. 式 17 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 10 mV. This calculation is for CCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors.

$$C_{OUT_STABILITY} > \left(\frac{15}{\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{15}{\pi \times 1100\ kHz}\right)^2 \times \frac{1}{1\ \mu H} = 19\ \mu F \quad (16)$$

$$C_{OUT_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times f_{SW}} = \frac{1.45\ A}{8 \times 10\ mV \times 1100\ kHz} = 16.5\ \mu F \quad (17)$$

式 18 and 式 19 calculate the minimum capacitance to meet the transient response requirement of 18 mV with a 3-A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step.

$$C_{OUT_UNDERSHOOT} > \frac{L \times I_{STEP}^2 \times \left(\frac{V_{OUT}}{V_{IN}(min) \times f_{SW}} + t_{OFF_MIN}(max)\right)}{2 \times V_{TRANS} \times V_{OUT} \times \left(\frac{V_{IN}(min) - V_{OUT}}{V_{IN}(min) \times f_{SW}} - t_{OFF_MIN}(max)\right)}$$

$$C_{OUT_UNDERSHOOT} > \frac{1\ \mu H \times 3\ A^2 \times \left(\frac{1.8\ V}{8\ V \times 1100\ kHz} + 220\ ns\right)}{2 \times 18\ mV \times 1.8\ V \times \left(\frac{8\ V - 1.8\ V}{8\ V \times 1100\ kHz} - 220\ ns\right)} = 122\ \mu F \quad (18)$$

$$C_{OUT_OVERSHOOT} > \frac{L \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{1\ \mu H \times 3\ A^2}{2 \times 18\ mV \times 1.8\ V} = 139\ \mu F \quad (19)$$

The output capacitance needed to meet the overshoot requirement is the highest value so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance and 式 20 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the f_{SW}. It can be possible to use more output capacitance but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 6x 47-µF 0805 6.3-V ceramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to 60% the nominal value giving an effective total capacitance of 169 µF. This effective capacitance meets the minimum and maximum requirements.

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$$C_{OUT_STABILITY} < \left(\frac{50}{\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{50}{\pi \times 1100\ kHz}\right)^2 \times \frac{1}{1\ \mu H} = 209\ \mu F \quad (20)$$

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If using non-ceramic capacitors, as a starting point, the ESR must be below the values calculated in 式 21 to meet the ripple requirement and 式 22 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors must be used to determine if the ripple and transient requirements can be met.

$$R_{ESR_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{10\ mV}{1.45\ A} = 6.9\ m\Omega \quad (21)$$

$$R_{ESR_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{18\ mV}{3\ A} = 6.0\ m\Omega \quad (22)$$

7.2.2.5 Choose the Input Capacitors (C_{IN})

The TPS54J060 requires input bypass capacitors between the VIN and PGND pins to bypass the power-stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout will allow. At least 10 µF of ceramic capacitance and a 0.01-µF to 0.1-µF high frequency ceramic bypass capacitor is required. The high frequency bypass capacitor minimizes high frequency voltage overshoot across the power-stage. The ceramic capacitors must be high-quality dielectric of X5R or X7R for the high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

The input capacitance required to meet a specific input ripple target can be calculated with 式 23. A recommended target input voltage ripple is 5% the minimum input voltage, 400 mV in this example. The calculated input capacitance is 2.4 µF and the minimum input capacitance of 10 µF exceeds this. This example meets these two requirements with two 4.7-µF 0603 25-V ceramic capacitors and two 10-µF 1206 25-V ceramic capacitors.

$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}(min)}\right)}{f_{SW} \times V_{IN}(min) \times V_{IN_RIPPLE}} = \frac{1.8\ V \times 6\ A \times \left(1 - \frac{1.8\ V}{8\ V}\right)}{1100\ kHz \times 8\ V \times 400\ mV} = 2.4\ \mu F \quad (23)$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. The input RMS current the input capacitors must support is calculated by 式 24 and is 2.5 A in this example. The ceramic input capacitors have a current rating much greater than this.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}(min)} \times \frac{(V_{IN}(min) - V_{OUT})}{V_{IN}(min)}} = 6\ A \times \sqrt{\frac{1.8\ V}{8\ V} \times \frac{(8\ V - 1.8\ V)}{8\ V}} = 2.5\ A \quad (24)$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, the selection process in this article is recommended.

7.2.2.6 Feedback Network (FB Pin)

The output voltage is programmed by the voltage-divider resistors, R_{FB_T} and R_{FB_B}, shown in 式 25. Connect R_{FB_T} between the FB pin and the output, and connect R_{FB_B} between the FB pin and AGND. The recommended R_{FB_B} value is from 499 Ω to 20 kΩ. Determine R_{FB_T} using 式 25.

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$$R_{FB_T} = R_{FB_B} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) = 10\ k\Omega \times \left(\frac{1.8\ V}{0.9\ V} - 1 \right) = 10\ k\Omega \quad (25)$$

In most applications, a feedforward capacitor (C_{FF}) in parallel with R_{FB_T} is recommended. C_{FF} can improve the transient response and increase the phase margin. C_{FF} can be required for sufficient phase margin if the output voltage is greater than 1.8 V or if the LC double pole frequency is below f_{SW} / 60. The frequency of the LC double pole for this application is calculated with 式 26 to be 12.1 kHz. This is less than f_{SW} / 60 so C_{FF} is used.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} = \frac{1}{2\pi \times \sqrt{1\ \mu H \times 169\ \mu F}} = 12.2\ kHz \quad (26)$$

The recommended value for C_{FF} is calculated with 式 27. This equation selects C_{FF} to put a zero at f_{LC} × 3. In this example, the calculated value is 434 pF and a standard value of 470 pF is used. For higher output voltages, the zero from C_{FF} must be closer to the LC double pole. For example, for a 5-V application, the zero from C_{FF} must be placed at or even below the LC double pole.

$$C_{FF} = \frac{1}{2\pi \times R_{FB_T} \times 3 \times f_{LC}} = \frac{1}{2\pi \times 10\ k\Omega \times 3 \times 12.2\ kHz} = 434\ pF \quad (27)$$

7.2.2.7 Soft Start Capacitor (SS/REFIN Pin)

The capacitor placed on the SS/REFIN pin can be used to extend the soft-start time past the internal 1.5-ms soft start. This example uses a 2-ms soft start time and the required external capacitance can be calculated with 式 28. In this example, a 22-nF capacitor is used.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} = \frac{9\ \mu A \times 2\ ms}{0.9\ V} = 20\ nF \quad (28)$$

注

A minimum capacitor value of 1 nF is required at the SS/REFIN pin to help bypass noise. Also, the SS/REFIN capacitor must use the AGND pin for the ground. Note, any C_{SS} calculation that uses a soft-start time of less than 1.5 ms will be ignored by the internal soft-start time circuit. Therefore, selecting a capacitor less than or equal to 15 nF will result in the internal default 1.5 ms soft-start time.

7.2.2.8 EN Pin Resistor Divider

A resistor divider on the EN pin can be used to increase the input voltage that the converter begins the start-up sequence. Increasing the input voltage the converter starts up at can be useful in high output voltage applications. The resistor divider can be selected so the converter starts switching after the input voltage is greater than the output voltage. If the output voltage comes up before the input voltage is sufficient, UVP can be tripped and cause the converter to latch off.

To set the start voltage, first select the bottom resistor (R_{EN_B}). The recommended value is between 1 kΩ and 100 kΩ. There is an internal pulldown resistance with a nominal value of 6 MΩ and this must be included for the most accurate calculations. This is especially important when the bottom resistor is a higher value, near 100 kΩ. This example uses a 100-kΩ resistor and this combined with the internal resistance in parallel results in an equivalent bottom resistance of 98.4 kΩ. The top resistor value for the target start voltage is calculated with 式 29. In this example, the nearest standard value of 499 kΩ is selected for R_{EN_T}.

$$R_{EN_T} = \frac{R_{EN_B} \times V_{START}}{V_{ENH}} - R_{EN_B} = \frac{98.4\ k\Omega \times 7.4\ V}{1.22\ V} - 98.4\ k\Omega = 498\ k\Omega \quad (29)$$

The start and stop voltages with the selected EN resistor divider can be calculated with 式 28 and 式 31.

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$$V_{START} = V_{ENH} \times \frac{R_{EN_B} + R_{EN_T}}{R_{EN_B}} = 1.22\ V \times \frac{98.4\ k\Omega + 499\ k\Omega}{98.4\ k\Omega} = 7.41\ V \quad (30)$$

$$V_{STOP} = V_{ENL} \times \frac{R_{EN_B} + R_{EN_T}}{R_{EN_B}} = 1.02\ V \times \frac{98.4\ k\Omega + 499\ k\Omega}{98.4\ k\Omega} = 6.19\ V \quad (31)$$

7.2.2.9 VCC Bypass Capacitor

At a minimum, a 1-µF ceramic bypass capacitor is needed on VCC pin located as close to the pin as the layout will allow.

7.2.2.10 BOOT Capacitor

At a minimum, a 0.1-µF ceramic bypass capacitor is needed between the BOOT and SW pins located as close to the pin as the layout will allow.

7.2.2.11 Series BOOT Resistor and RC Snubber

A series BOOT resistor can help reduce the overshoot at the SW pin. As a best practice, include a 0-Ω series BOOT resistor in the design for 12-V or higher input applications. The BOOT resistor can be used to reduce the voltage overshoot on the SW pin to within the *Absolute Maximum Ratings* in case the overshoot is higher than normal due to parasitic inductance in PCB layout. Including a 0-Ω BOOT resistor is recommended with external VCC as the SW node overshoot is increased. The recommended BOOT resistor value to decrease the SW pin overshoot is 4.7 Ω.

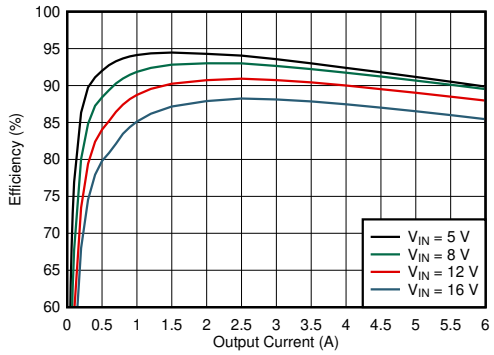
An RC snubber on the SW pin can also help reduce the high frequency voltage spikes and ringing at the SW pin. Recommended snubber values are 6.8 Ω and 220 pF. The best value for these components can vary with different layouts but these recommended values must provide a good starting point. In order for the RC snubber to be as effective as possible, it must be placed on the same side as the IC and be as close as possible to the SW pins with a very low impedance return to PGND pins.

7.2.2.12 PGOOD Pullup Resistor

The PGOOD pin is open-drain so a pullup resistor is required when using this pin. The recommended value is between 1 kΩ and 100 kΩ.

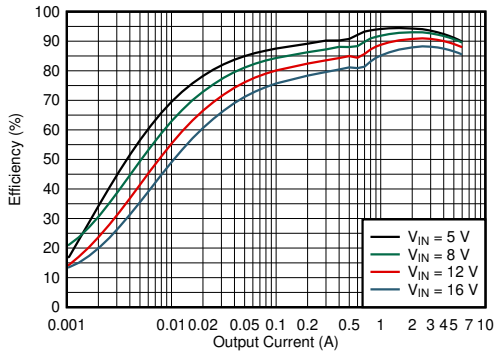
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7.2.3 Application Curves



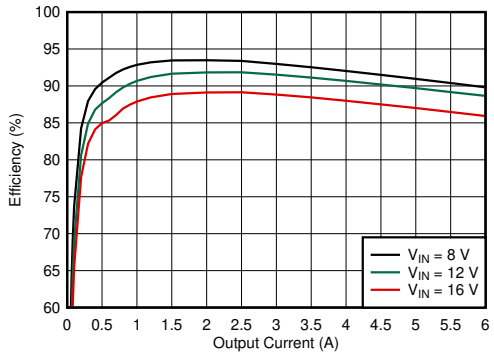
V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = FCCM
VCC = Int 3.0 V

図 7-2. Efficiency – 1100 kHz, FCCM



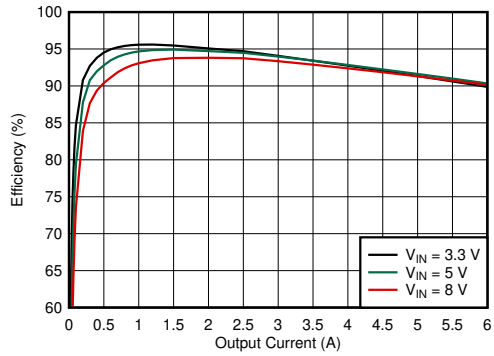
V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = DCM
VCC = Int 3.0 V

図 7-3. Efficiency – 1100 kHz, DCM



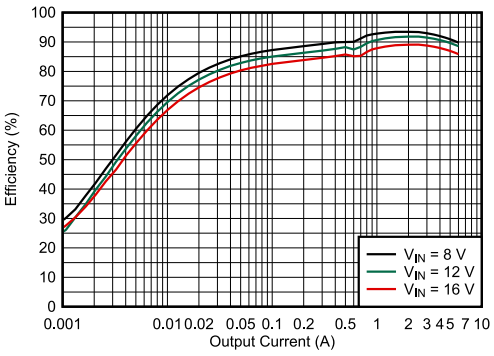
V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = FCCM
VCC = Ext 3.3 V R_{BOOT} = 4.7 Ω

図 7-4. Efficiency – 1100 kHz, FCCM, External 3.3-V VCC, 4.7-Ω R_{BOOT}



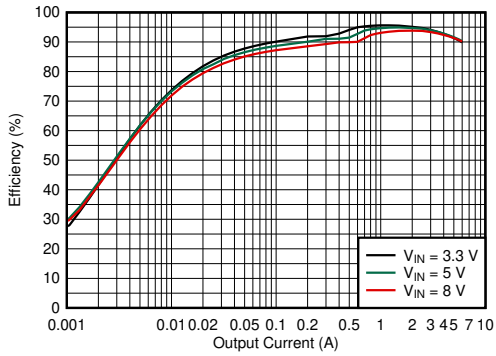
V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = FCCM
VCC = Ext 3.3 V R_{BOOT} = 0 Ω

図 7-5. Efficiency – 1100 kHz, FCCM, External 3.3-V VCC, 0-Ω R_{BOOT}



V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = DCM
VCC = Ext 3.3 V R_{BOOT} = 4.7 Ω

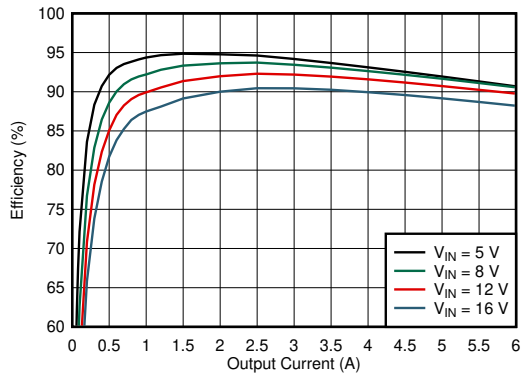
図 7-6. Efficiency – 1100 kHz, DCM, External 3.3-V VCC, 4.7-Ω R_{BOOT}



V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = DCM
VCC = Ext 3.3 V R_{BOOT} = 0 Ω

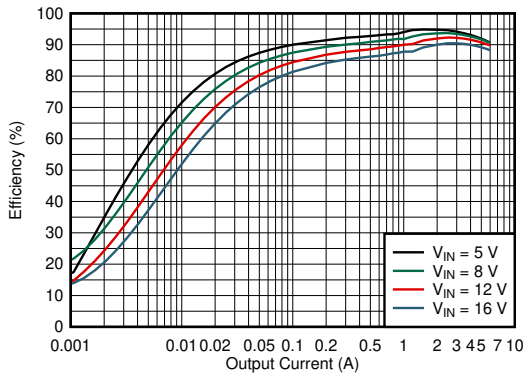
図 7-7. Efficiency – 1100 kHz, DCM, External 3.3-V VCC, 0-Ω R_{BOOT}

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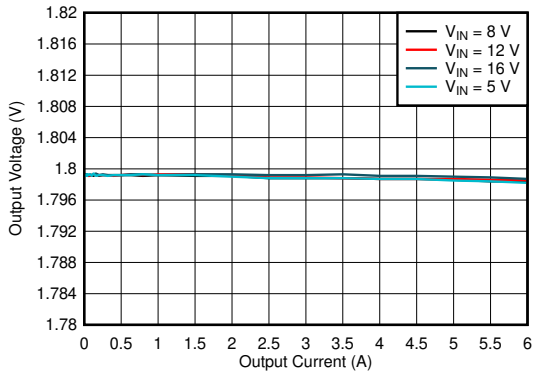
V_{OUT} = 1.8 V f_{SW} = 600 kHz MODE = FCCM
VCC = Int 3.0 V

図 7-8. Efficiency – 600 kHz, FCCM



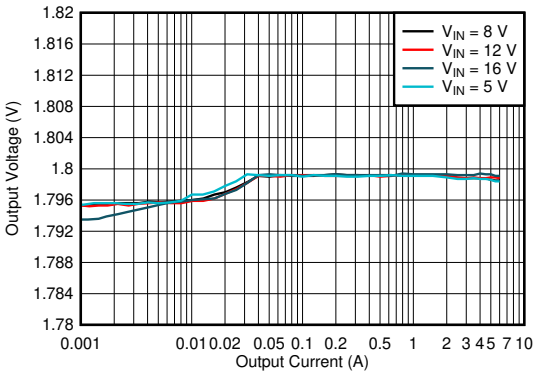
V_{OUT} = 1.8 V f_{SW} = 600 kHz MODE = DCM
VCC = Int 3.0 V

図 7-9. Efficiency – 600 kHz, DCM



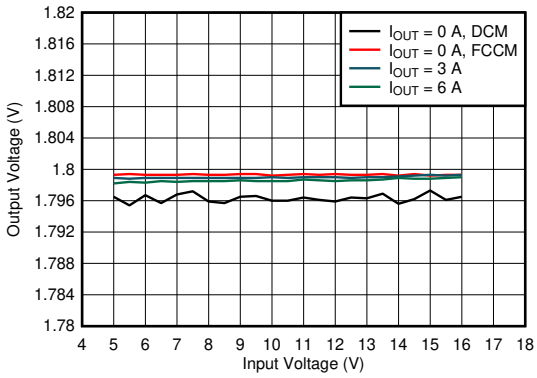
V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = FCCM

図 7-10. Output Voltage vs Output Current – FCCM



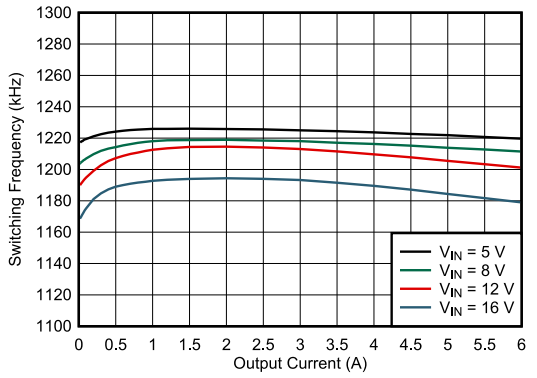
V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = DCM

図 7-11. Output Voltage vs Output Current – DCM



V_{OUT} = 1.8 V f_{SW} = 1100 kHz

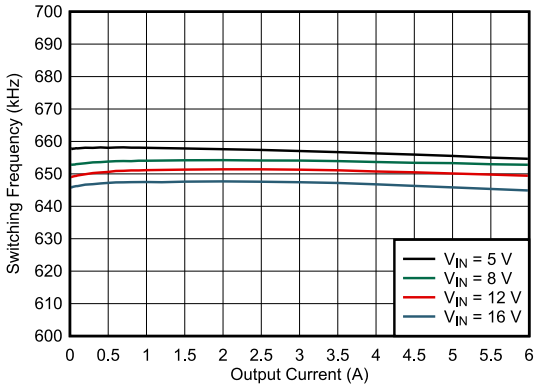
図 7-12. Output Voltage vs Input Voltage



V_{OUT} = 1.8 V f_{SW} = 1100 kHz MODE = FCCM

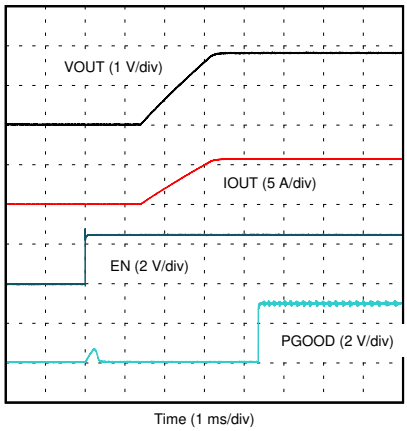
図 7-13. Switching Frequency vs Output Current – 1100 kHz

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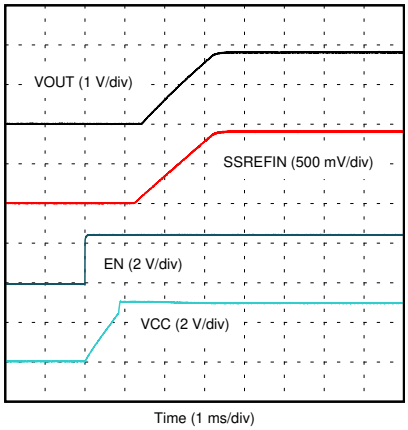
V_{OUT} = 1.8 V f_{SW} = 600 kHz MODE = FCCM

図 7-14. Switching Frequency vs Output Current – 600 kHz



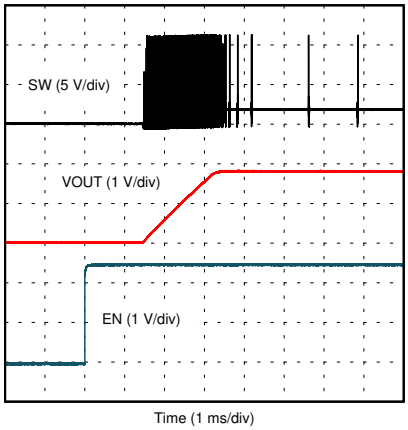
V_{IN} = 12 V R_{LOAD} = 0.3 Ω

図 7-15. EN Start-Up



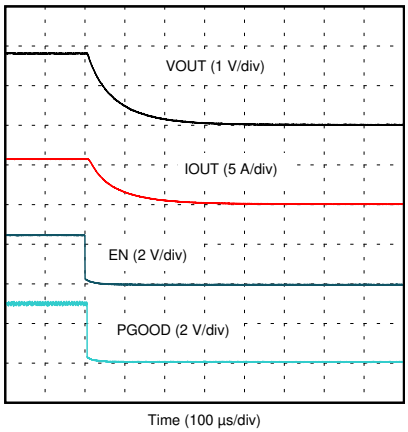
V_{IN} = 12 V R_{LOAD} = 0.3 Ω

図 7-16. EN Start-Up



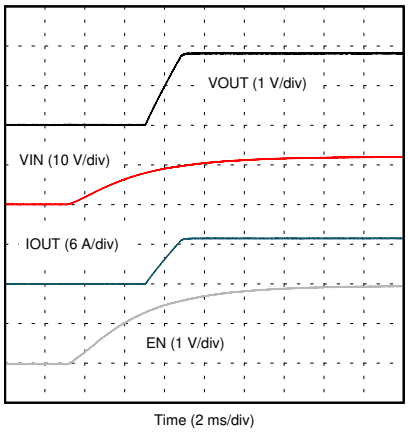
V_{IN} = 12 V I_{OUT} = 0 A MODE = DCM

図 7-17. EN Start-Up – DCM



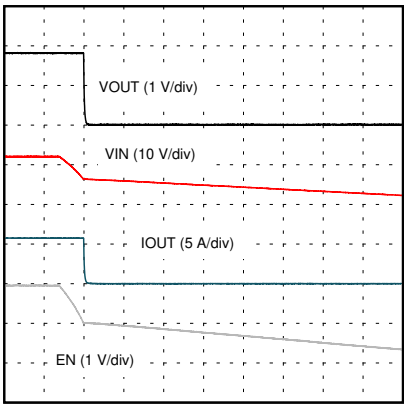
V_{IN} = 12 V R_{LOAD} = 0.3 Ω

図 7-18. EN Shutdown



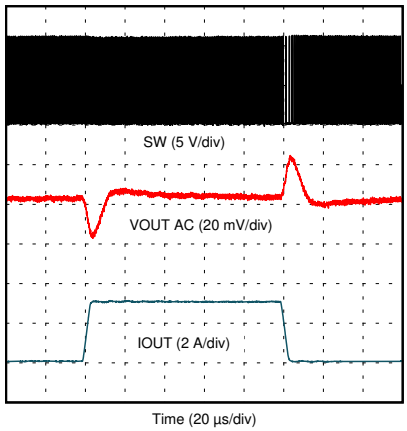
R_{LOAD} = 0.3 Ω

図 7-19. V_{IN} Start-Up



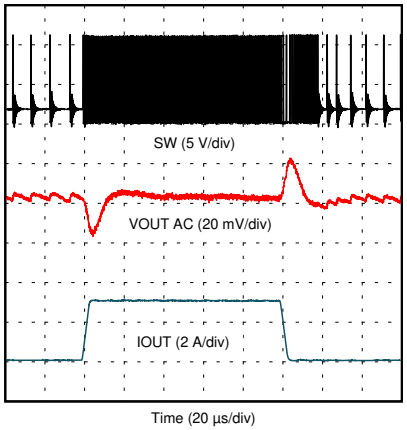
R_{LOAD} = 0.3 Ω

図 7-20. V_{IN} Shutdown



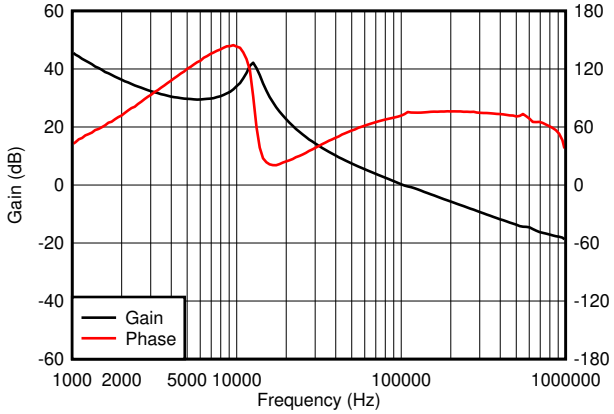
V_{IN} = 12 V　　0.1 A to 3.1 A step　　1 A/µsec
MODE = FCCM

図 7-21. Load Transient – FCCM



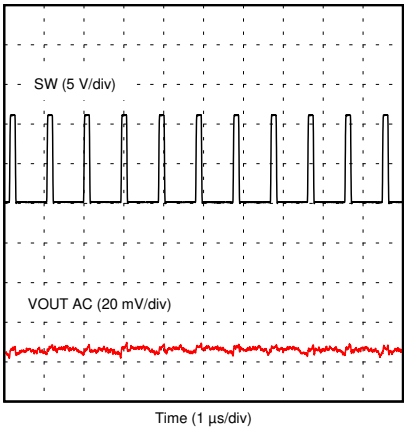
V_{IN} = 12 V　　0.1 A to 3.1 A step　　1 A /µsec
MODE = DCM

図 7-22. Load Transient – DCM



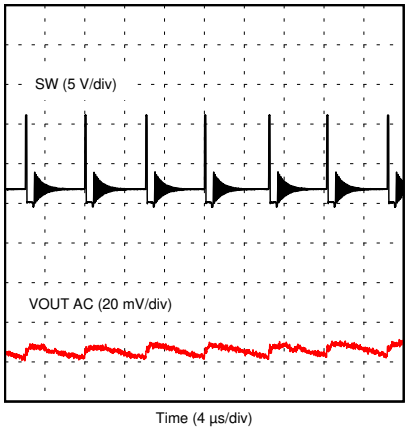
V_{IN} = 12 V　　I_{OUT} = 6 A

図 7-23. Bode Plot



V_{IN} = 12 V　　I_{LOAD} = 0.1 A　　MODE = FCCM

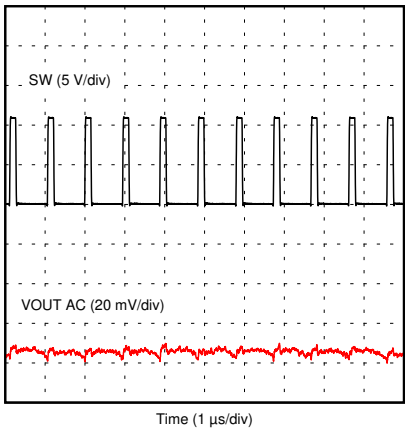
図 7-24. Output Voltage Ripple



V_{IN} = 12 V　　I_{LOAD} = 0.1 A　　MODE = DCM

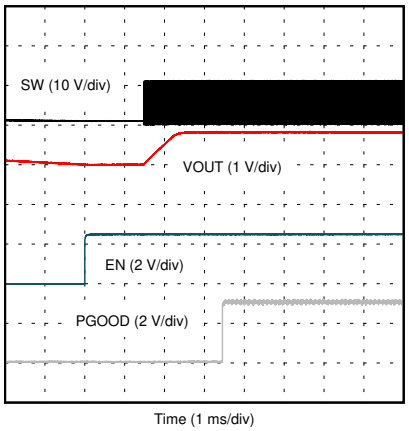
図 7-25. Output Voltage Ripple – DCM

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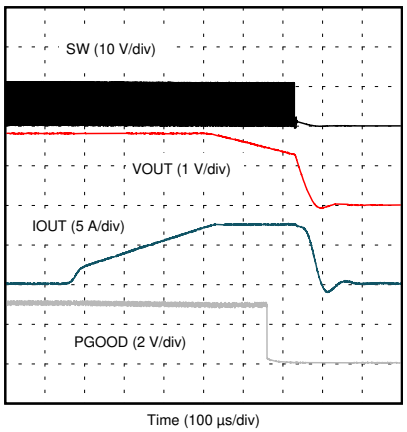
V_{IN} = 12 V I_{LOAD} = 6 A

図 7-26. Output Voltage Ripple



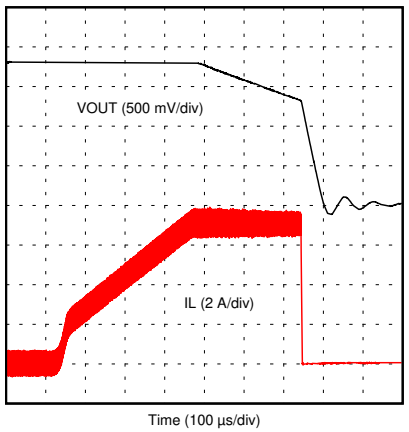
V_{IN} = 12 V I_{OUT} = 0 A Prebias = 1.0 V

図 7-27. EN Start-Up With Prebias



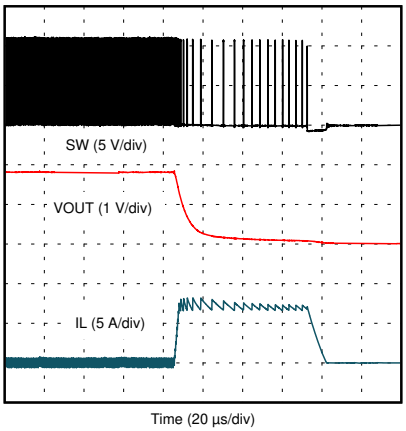
V_{IN} = 12 V I_{OUT} = 7.5-A Constant Current

図 7-28. Overcurrent Response



V_{IN} = 12 V I_{OUT} = 7.5-A Constant Current

図 7-29. Overcurrent Response



V_{IN} = 12 V I_{OUT} = Short

図 7-30. Short Circuit Response

7.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.7 V and 16 V. If you are using an input voltage below 4.0 V, the VCC pin requires external bias. Proper bypassing of input supplies (VIN)

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and internal LDO (VCC) is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in セクション 7.4.

7.4 Layout

7.4.1 Layout Guidelines

Before beginning a design using the device, consider the following:

- A 0402-sized 0.01-µF to 0.1-µF decoupling capacitor must be placed as close as possible to the VIN and PGND pins to decouple high frequency noise and help reduce switch node ringing. Larger VIN decoupling capacitors must be placed as close as possible to VIN and PGND pins behind this capacitor to further minimize the input AC-current loop.
- Place the power components (including input and output capacitors, the inductor, and the IC) on the solder side of the PCB. In order to shield and isolate the small signal traces from noisy power lines, insert and connect at least one inner plane to ground.
- All sensitive analog traces and components such as FB, PGOOD, TRIP, MODE, and SS/REFIN must be placed away from high-voltage switching nodes such as SW and BOOT to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- Place the feedback resistor near the device to minimize the FB trace distance.
- Place the OCP-setting resistor (R_{TRIP}) and mode-setting resistor (R_{MODE}) close to the device. Use the common AGND via to connect the resistors to the VCC PGND plane if applicable.
- Place the VCC decoupling capacitors as close as possible to the device. If multiple capacitors are used, provide PGND vias for each decoupling capacitor and ensure the return path is as small as possible.
- Keep the switch node connections from pins 2 and 11 to the inductor as short and wide as possible.
- Use separate traces to connect SW node to the bootstrap capacitor and RC snubber, if used, instead of combining them into one connection. Keep both the BOOT and snubber paths short for low inductance and the best possible performance. Also, to minimize inductance, avoid using vias for the RC snubber routing and use very wide traces. To be most effective, the RC snubber must be connected between a large SW copper shape and large PGND copper shape on the same side of the PCB as the TPS54J060.
- Avoid connecting AGND to the PCB ground plane (PGND) in a high current path where significant IR and L*dI/dt drops can occur.

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7.4.2 Layout Example

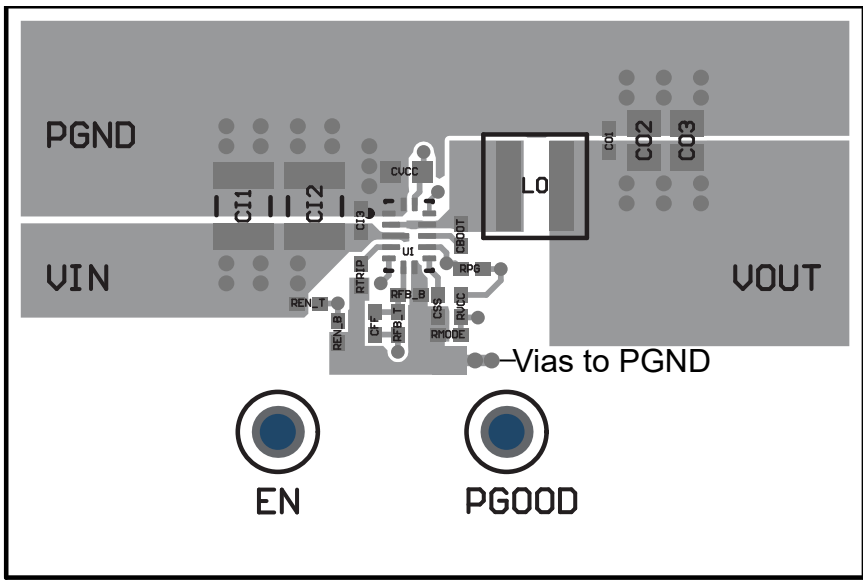


図 7-31. Top Layer Layout

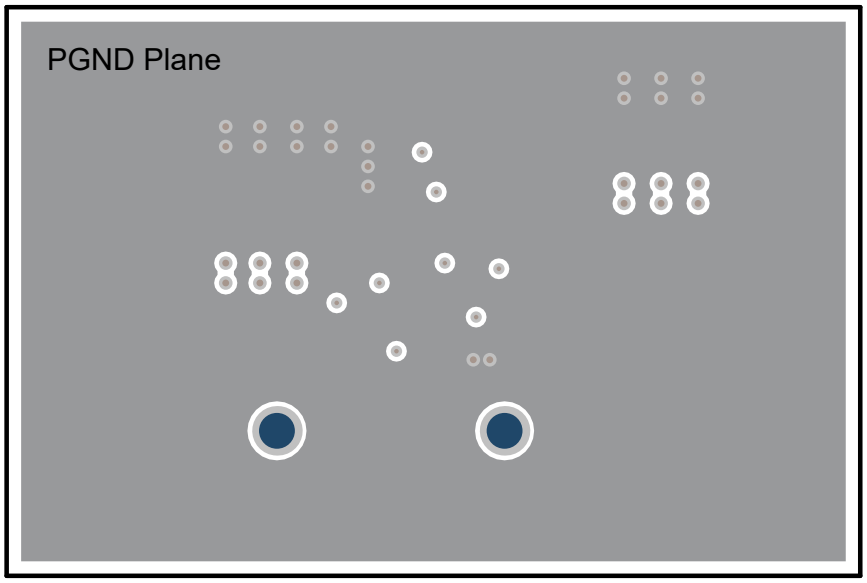


図 7-32. Signal Layer 1 Layout

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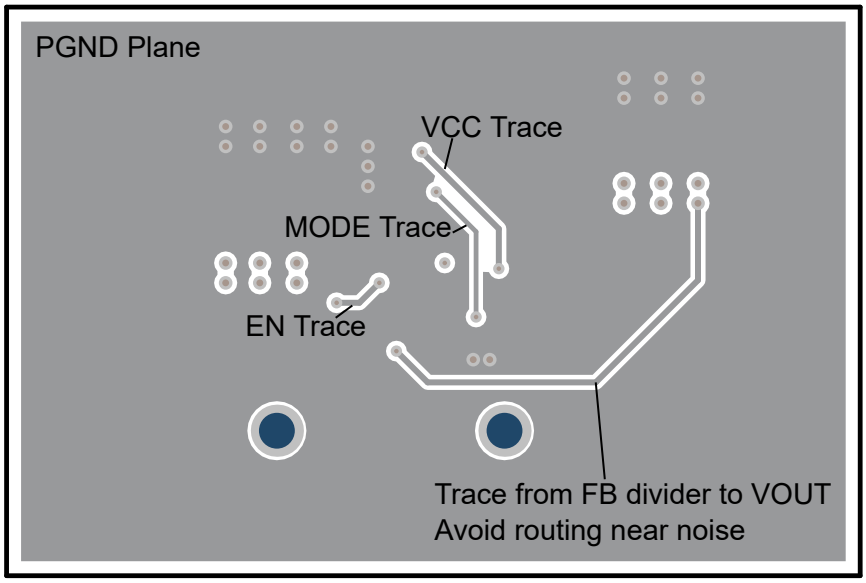


図 7-33. Signal Layer 2 Layout

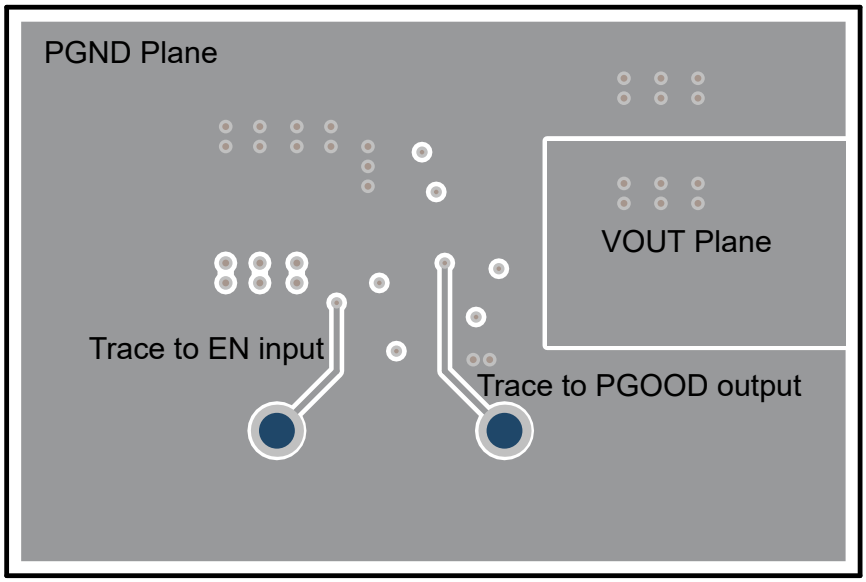


図 7-34. Bottom Layer Layout (Viewed from Top)

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor application note

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (June 2021) to Revision D (June 2024)	Page
• 商標の情報を更新	1
• Changed from JEDEC specification JESD22-C101 to ANSI/ESDA/JEDEC JS-002	4
• Changed from VCC = 3.3V to VIN rising, VCC = external 3.3V bias	5
• Added VIN UVLO falling threshold voltage	5
• Changed from VCC = 3.3V to VIN falling, VCC = external 3.3V bias	5

Changes from Revision B (October 2020) to Revision C (June 2021)	Page
• Changed VIN - SW transient < 20 ns min value to –4.0	4
• Updated セクション 6.3.4 for soft-start capacitor clarification	12
• Updated セクション 7.2.2.7 for soft-start capacitor clarification	23

Changes from Revision A (April 2020) to Revision B (October 2020)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新。	1
• 最初の公開リリース	1

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10 Mechanical, Packaging, and Ordering Information

The following pages include mechanical, packaging, and ordering information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54J060RPGR	Active	Production	VQFN-HR (RPG) | 14	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	54J060
TPS54J060RPGR.A	Active	Production	VQFN-HR (RPG) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	54J060
TPS54J060RPGR.B	Active	Production	VQFN-HR (RPG) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	54J060

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

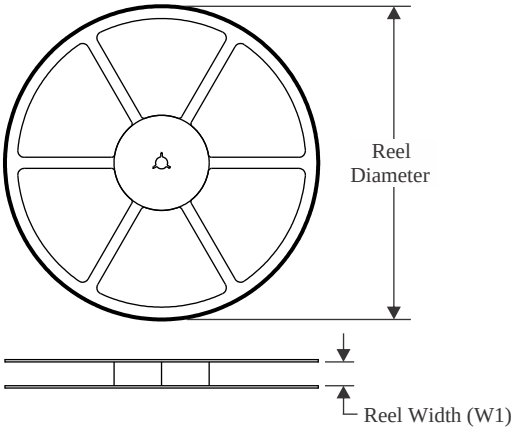
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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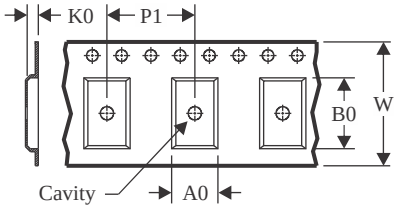
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

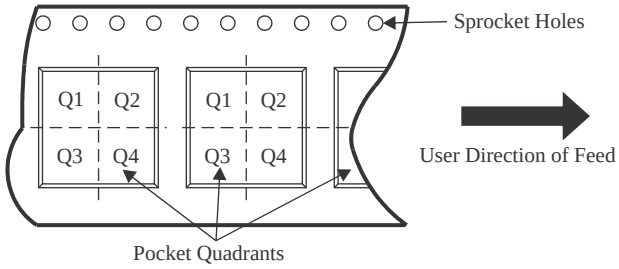


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

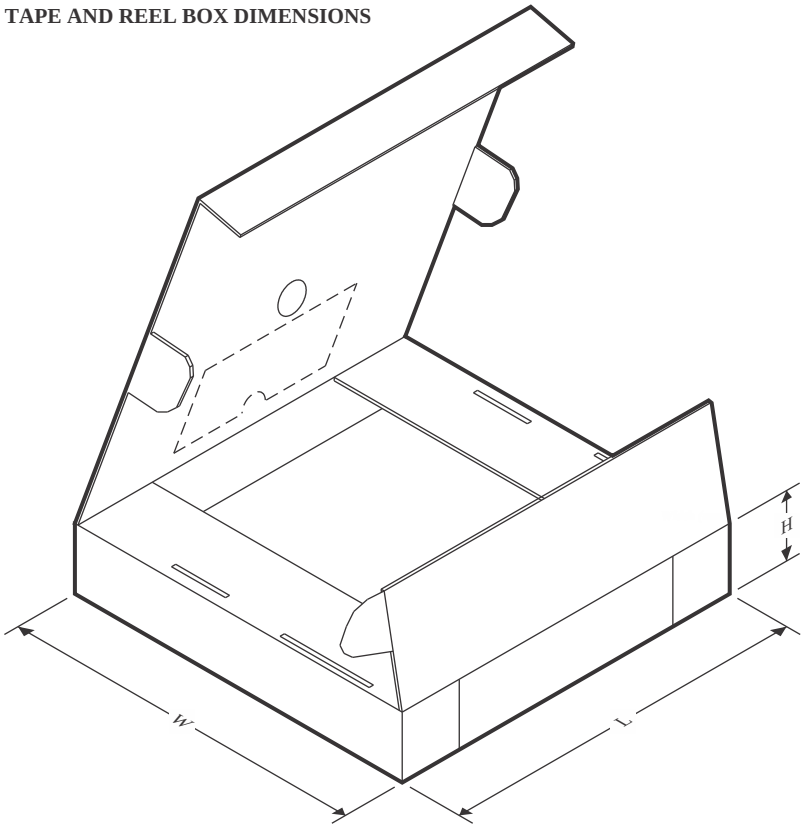
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54J060RPGR	VQFN-HR	RPG	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

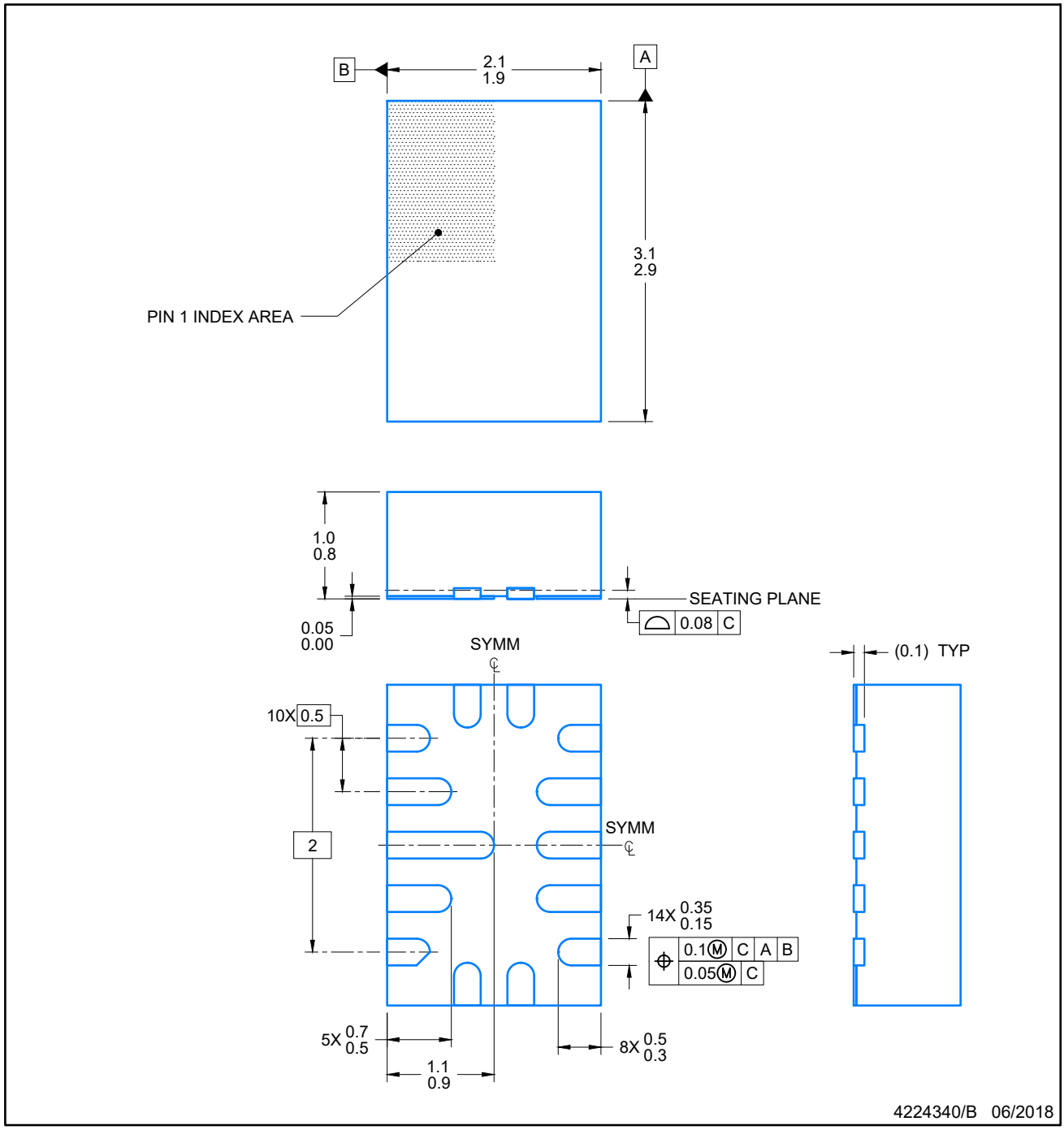
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54J060RPGR	VQFN-HR	RPG	14	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPG0014A

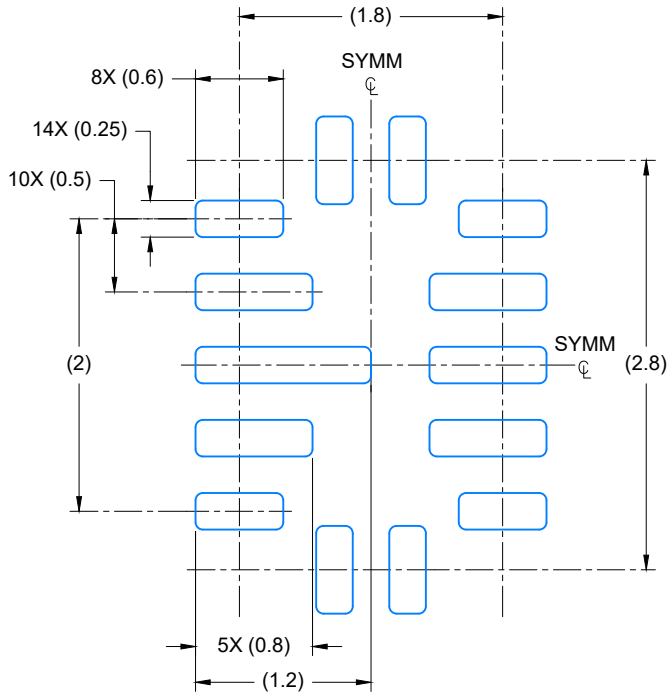
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

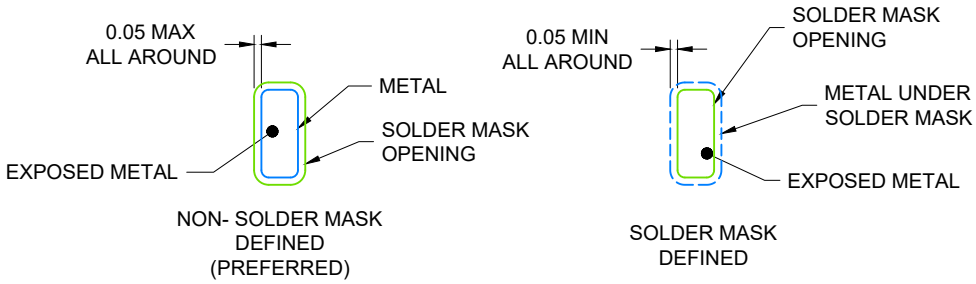


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

4224340/B 06/2018

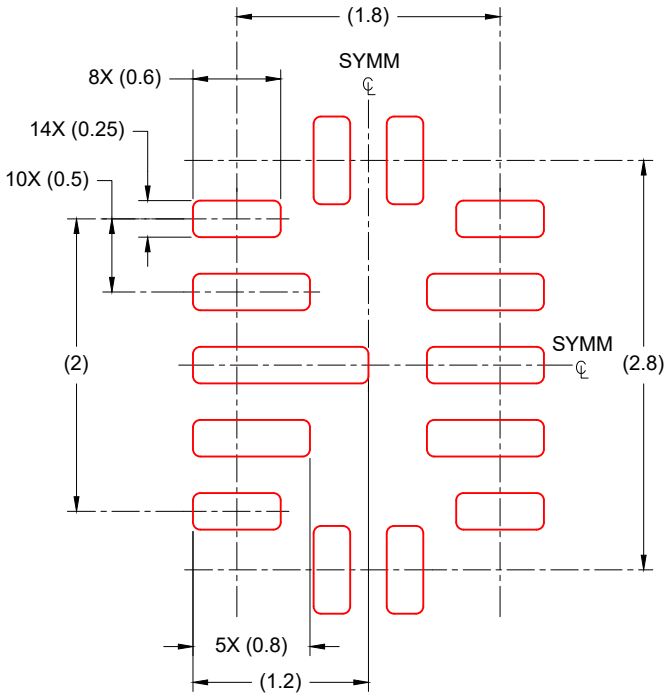
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
SCALE: 20X

4224340/B 06/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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